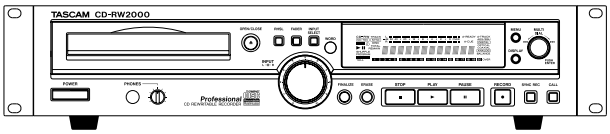


TASCAM
TEAC Professional Division

SERVICE MANUAL

CD-RW2000

Professional
CD Rewritable Recorder

CONTENTS

目次

INSTRUCTIONS FOR SERVICE PERSONNEL

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

Effective : June, 2000

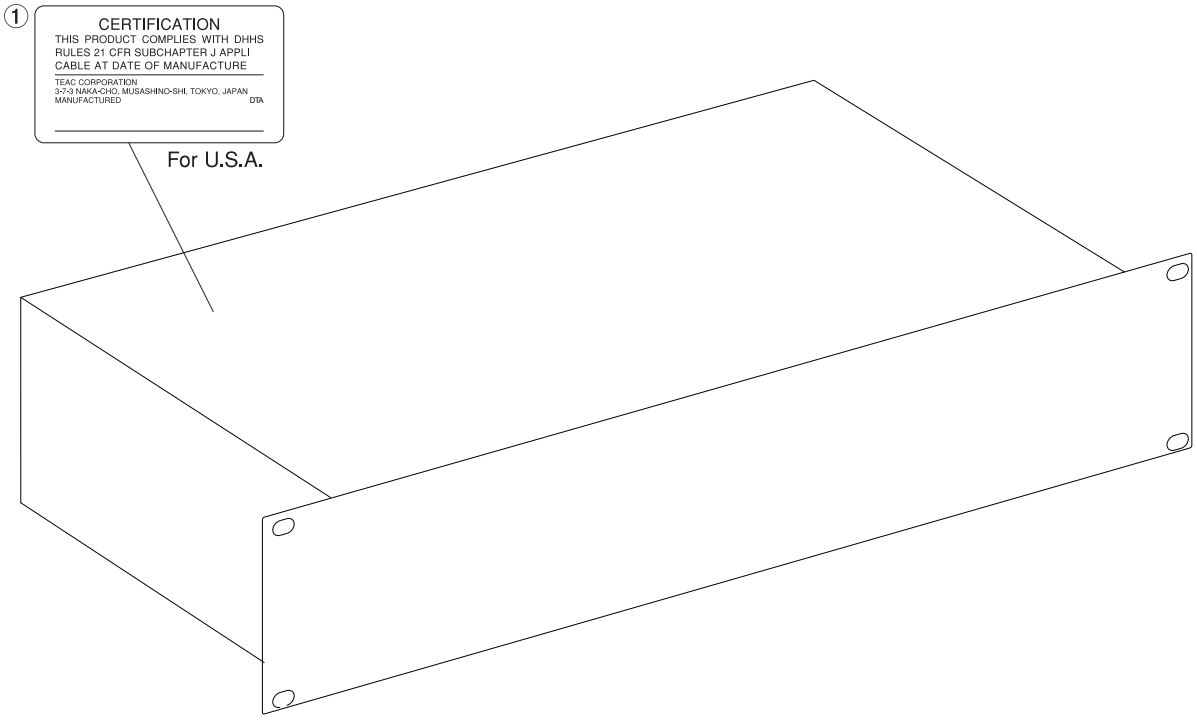
S-0026A

1. SAFETY INFORMATION

This product has been designed and manufactured according to FDA regulations "title 21, CFR, chapter 1, subchapter J, based on the Radiation Control for Health and Safety Act of 1968", and is classified as a class 1 laser product. There is no hazardous invisible laser radiation during operation because invisible laser radiation emitted inside of this product is completely confined in the protective housings.
The label required in this regulation is shown ①.

● **CAUTION**

USE OF CONTROLS OR ADJUSTMENT OR PERFORMANCE OF PROCEDURES OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.



Optical pickup:	Type	: KRS-202A or KRS-220B
	Manufacturer	: SONY Corporation
	Laser output	: Less than 0.1 mW (Play) and 32 mW (Record) on the objective lens
	Wavelength	: 777–787 nm

2. SPECIFICATIONS

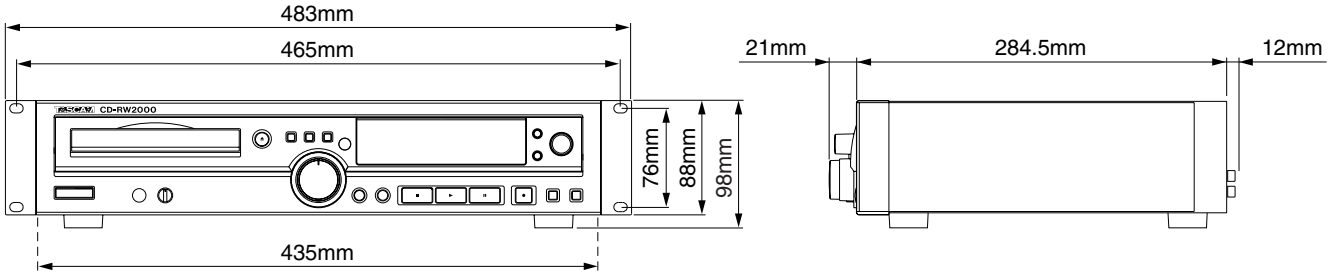
仕様

Recording media type:	CD-R, CD-R-DA CD-RW, CD-RW-DA
Recording resolution:	16-bit linear
Recording sampling frequency:	44.1 kHz
Frequency convertor input:	32 kHz - 48 kHz
Frequency response:	20 Hz - 20 kHz (playback ±0.5 dB, recording ±1.0 dB)
S/N ratio:	98 dB (playback), 92 dB (recording)
Dynamic range:	94 dB (playback), 92 dB (recording)
Total harmonic distortion:	0.004 % (playback), 0.005 % (recording)
Channel separation:	90 dB (playback : 1 kHz), 80 dB (recording : 1 kHz)
Wow & flutter:	Unmeasurable (< 0.001 %)
Analog inputs:	Balanced XLR-type
Nominal input level:	+4 dBu (FS-16dB)
Maximum input level:	+20 dBu
Input impedance:	10 kΩ (balanced)
Analog inputs:	Unbalanced RCA
Nominal input level:	-10 dBV (FS-16dB)
Maximum input level:	+6 dBV
Input impedance:	33 kΩ (unbalanced)
Analog outputs:	Balanced XLR-type
Nominal output level:	+4 dBu (FS-16dB)
Maximum output level:	+20 dBV
Ouput impedance:	75 Ω (balanced)
Analog outputs:	Unbalanced RCA
Nominal output level:	-10 dBV (FS-16dB)
Maximum output level:	+6 dBV
Ouput impedance:	800 Ω (unbalanced)
Headphone output:	6 mm (1/4") stereo
Ouput level:	35 mW + 35 mW (into 32 Ω)
Digital input:	
AES/EBU:	XLR-type, AES3-1992
COAXIAL:	RCA pin, IEC60958 TYPE II
OPTICAL:	TOSLINK, IEC60958 TYPE II
Digital output:	
AES/EBU:	XLR-type, AES3-1992
COAXIAL:	RCA pin, IEC60958 TYPE II
OPTICAL:	TOSLINK, IEC60958 TYPE II

記録ディスク：	CD-R, CD-R-DA CD-RW, CD-RW-DA
量子化ビット数：	16 bit リニア
サンプリング周波数：	44.1 kHz
再生周波数特性：	20 Hz ～20 kHz ±0.5 dB（再生時）、±1.0 dB（記録時）
S/N 比：	98 dB（再生時）、92 dB（記録時）
ダイナミックレンジ：	94 dB（再生時）、92 dB（記録時）
歪率：	0.004 %（再生時）、0.005 %（記録時）
チャンネルセパレーション：	90 dB（再生時、1 kHz） 80 dB（記録時、1 kHz）
ワウフラッター：	測定限界以下（0.001% 以下）
アナログ入力	
バランス入力：	XLR-3-31 相当
基準入力レベル：	+4 dBu（FS − 16 dB)
最大入力レベル：	+20 dBu
入力インピーダンス：	10 kΩ（平衡）
アンバランス入力：	RCA ピン
基準入力レベル：	−10 dBV（FS − 16 dB)
最大入力レベル：	+6 dBV
入力インピーダンス：	33 kΩ（不平衡）
アナログ出力	
バランス出力：	XLR-3-32 相当
基準出力レベル：	+4 dBu（FS − 16 dB)
最大出力レベル：	+20 dBu
出力インピーダンス：	75 Ω（平衡）
アンバランス出力：	RCA ピン
基準出力レベル：	−10 dBV（FS − 16 dB)
最大出力レベル：	+6 dBV
出力インピーダンス：	800 Ω（不平衡）
ヘッドホン出力：	6φステレオ 35 mW+35 mW（32 Ω 負荷）
デジタル入力	
AES/EBU：	XLR-3-31 相当、AES3-1992
COAXIAL：	RCA ピン、IEC60958 TYPE II
OPTICAL：	TOSLINK 、IEC60958 TYPE II
デジタル出力	
AES/EBU：	XLR-3-32 相当、AES3-1992
COAXIAL：	RCA ピン、IEC60958 TYPE II
OPTICAL：	TOSLINK、IEC60958 TYPE II

Voltage requirements:	USA/Canada 120 VAC, 60 Hz U.K./Europe 230 VAC, 50 Hz Australia 240 VAC, 50 Hz
Power consumption:	30 W
Applicable electromagnetic environment:	E4
Peak inrush current:	1.8 A
Dimensions w x h x d:	483 x 98 x 317.5 (mm) 19 x 3.9 x 12.5 (in)
Weight:	7 kg (15.4 lbs)
Operating temperature:	5°C to 35°C (41°F to 95°F)
Supplied accessories:	RC-RW2000 remote control unit 2 m (6 ft.) AC cord Rack mount screw kit

電源：	100 VAC, 50-60 Hz
消費電力：	30 W
重量：	7.0 kg
外形寸法（W ×H ×D）：	483 ×98 ×317.5 mm
付属品：	RC-RW2000 リモコン 電源コード（2m） ラックマウントビスキット



3. TEST MODE
テストモード

3-1. How to enter test mode

1. Turn power on while pressing and holding the MENU and CALL keys simultaneously. The display will show the model name and the system controller's version number, and the test mode is initiated.
2. Press the STOP key to exit from the test mode and return to the normal mode.

3-2. Operations in test mode

3-2-1. Front key check

1. Press the PLAY key to enter the front key check mode.
2. The display shows the name of each key to be checked; press the corresponding key.
   When the check result of the key is OK, the display shows another key name. When the result is No Good, the display continues to show the same key name.
3. The display finally shows "dial". Check the MULTI DIAL so that the displayed figure increases when the dial is rotated clockwise and decreases when it is rotated counterclockwise.
4. Press the PLAY key to exit from the front key check mode and return to the Version number display mode.

3-2-2. Display check

1. Press the DISPLAY key to enter the display check mode.
2. Press DISPLAY key a few times and ensure that each press lights the display blocks one after another.
3. When all the indicators are lit, press the DISPLAY key to exit from the display check mode and return to the Version number display mode.

3-2-3. EEPROM default setting

The following operation writes the default values in the EEPROM and checks the write data automatically.

1. Press the ERASE key.
   When the default data is written correctly, the display shows "EEPROM OK !!". If not, it shows "EEPROM NG !!".
2. Press the ERASE key again to return to the Version number display mode.

3-2-4. Converter MPU Version No. display

1. When the PAUSE key is pressed, the display shows the converter MPU version number.
2. Press the PAUSE key again to return the system controller's version number display mode.

3-2-5. Total recording time display

1. When the REC key is pressed, the display shows the time in which the pickup outputs the recording power (in the unit of hour).
2. Press the REC key again to return to the Version number display mode.

3-1. テストモードに入る方法

1. MENUキーとCALLキー押しながらPOWER ONすると、表示部に 機種名とシスコンのVersion No. が表示されテストモードに入る。
2. STOPキーを押すと、テストモードは終了し通常モードに戻る。

3-2. テストモードにおける動作

3-2-1. フロントキーチェック

1. PLAYキーを押し、フロントキーチェックモードに入る。
2. 表示部にチェックするキーの名称が表示されるので、そのキーを押す。
   チェックOKなら次のキーの名称が表示され、NGなら表示は変化しない。
3. 最後に、"dial"の表示が出るので、MULTI DIALを回して確認する。表示の数字が、右回しで増加、左回しで減少すること。
4. PLAYキーを押すと、フロントキーチェックモードを終了し Version No. 表示に戻る。

3-2-2. ディスプレイチェック

1. DISPLAYキーを押し、ディスプレイチェックモードに入る。
2. DISPLAYキーを押すたびに、表示部がブロックごとに点灯して行くことを確認する。
3. 表示部が全点灯した状態からDISPLAYキーを押すと、ディスプレイチェックモードを終了し Version No. 表示に戻る。

3-2-3. EEPROM デフォルト設定

EEPROMにデフォルト値を書き込み、自動的に書き込みチェックを行う。

1. ERASEキーを押す。
   このとき、正しく書き込めていれば、表示部に"EEROM OK !!"と表示され、不良の場合は"EEPROM NG !!"と表示される。
2. 再度 ERASEキーを押すと、Version No. 表示に戻る。

3-2-4. コンバータマイコン Version No. 表示

1. PAUSEキーを押すと、コンバータマイコンのVersion No.を表示する。
2. 再度 PAUSEキーを押すと、シスコンVersion No. 表示に戻る。

3-2-5. 記録積算時間表示

1. RECキーを押すと、ピックアップが記録パワーを出力した時間を表示する。(単位：hour)
2. 再度 RECキーを押すと、Version No. 表示に戻る。

4. AUDIO CHECKS
オーディオ確認

4-1. Playback performance　再生系

Mode: Play
Measurement point: ANALOG OUTPUT (UNBALANCED) [unless otherwise spesified　特に指示のある場合を除く]

ITEM 項　目	TEST DISC/ TRACK No.	PLAYBACK SIGNAL	SPECIFICATIONS 規　格	REMARKS 備　考
1. **Playback level** 再生レベル (BALANCE)	MCD-111 : Tr. No. 2	1 kHz, 0 dB	＋20 dBu ± 2 dB	Output terminal: ANALOG OUTPUT (BALANCED)
2. **Playback level** 再生レベル (UNBALANCE)	MCD-111 : Tr. No. 2	1 kHz, 0 dB	＋6 dBV ± 2 dB	
3. **Playback distortion** 再生歪率	MCD-111 :Tr. No. 2	1 kHz, 0 dB	0.005 % or less	400 Hz HPF in 22 kHz LPF in
4. **Playback frequency responce** 再生周波数特性	MCD-111 : Tr. No. 3～6	20 Hz～20 kHz, 0 dB	0 ± 1 dB	Reference level: 1 kHz
5. **SN ratio** SN比	MCD-111 : Tr. No. 7		94 dB or better	22 kHz LPF in IEC-A
6. **Playback channel separation** 再生チャンネル セパレーション	MCD-111 : Tr. No. 8（L→R）, Tr. No. 10（R→L）	1 kHz, 0 dB	80 dB or better	22 kHz LPF in IEC-A
7. **Emphasis effect** エンファシス効果	MCD-111 : Tr. No. 13	16 kHz, －20 dB	－20 dB ± 1 dB	
8. **Interruption** インタラプション	MCD-131 : Tr. No. 3		No sound skipping. 音飛びが無いこと。	Interruption 700 μm
9. **Black band** ブラックバンド	MCD-131 : Tr. No. 10		No sound skipping. 音飛びが無いこと。	Black band 600 μm
10. **Finger print** フィンガー プリント	MCD-131 : Tr. No. 13		No sound skipping. 音飛びが無いこと。	

4-2. Recording performance　録音系

Mode: REC Monitor
INPUT SELECT: Un Bal [unless otherwise spesified　特に指示のある場合を除く]
Input terminal: ANALOG INPUT (UNBALANCED) [unless otherwise spesified　特に指示のある場合を除く]
Measurement point: ANALOG OUTPUT (UNBALANCED) [unless otherwise spesified　特に指示のある場合を除く]

ITEM 項　目	**INPUT SIGNAL** 入力信号	**SPECIFICATIONS** 規　格	**REMARKS** 備　考
1. **Record level** 録音レベル (BALANCE)	ANALOG INPUT (BALANCED): 1 kHz, +20 dBu	Rotate the INPUT (L, R) controls to positions at which the "OVER" segments of the level meter is just about to light. AT this tine, the output level should be +20 dBu ±2 dB. INPUT (L,R)つまみを回して、レベルメータの“OVER”が点灯する直前になるようにセットする。 このとき、出力は 十20 dBu ± 2 dBであること。	INPUT SELECT: Balance Output terminal: ANALOG OUTPUT (BALANCED)
2. **Record level** 録音レベル (UNBALANCE)	1 kHz, +6 dBV	Rotate the INPUT (L, R) controls to positions at which the "OVER" segments of the level meter is just about to light. AT this tine, the output level should be +6 dBV ±2 dB. INPUT (L,R)つまみを回して、レベルメータの“OVER”が点灯する直前になるようにセットする。 このとき、出力は 十6 dBV ± 2 dBであること。	Do not vary the INPUT control positions after the adjustment. (These are their specified positions.) 調整後、INPUTつまみは動かさないこと。(規定位置)
3. **Total harmonic distortion** 総合歪率	1 kHz, +6 dBV	0.01 % or less	22 kHz LPF in 400 Hz HPF in
4. **Overall frequency responce** 録再周波数特性	20 Hz-20 kHz, +6 dBV	0 ± 1 dB	Reference level: 1 kHz
5. **Overall SN ratio** 録再SN比		88 dB min.	22 kHz LPF in IEC-A
6. **Channel separation** チャンネル セパレーション	Lch: 1 kHz, +6 dBV Rch: No signal	Ratio between the L CH and R CH outputs: 75 dB min. Also check the channel separation of L CH from R CH. Lchの出力とRchの出力の比： 75 dB 以上 Rch→Lchも同様に確認すること。	22 kHz LPF in IEC-A
7. **PHONES output level** PHONES出力 レベル	1 kHz, +6 dBV	Phones output level when the PHONE level control is set to the maximum position: 1.1 V or more. PHONESレベルつまみを最大にしたときのPHONES出力：1.1 V 以上	32Ω load

PARTS LIST SECTION

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with ∗ require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in the manual.
- ⚠Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J]: JAPAN [US/C]: U.S.A./CANADA [K]: KOREA [E]: EUROPE
  [UK]: U.K. [A]: AUSTRALIA

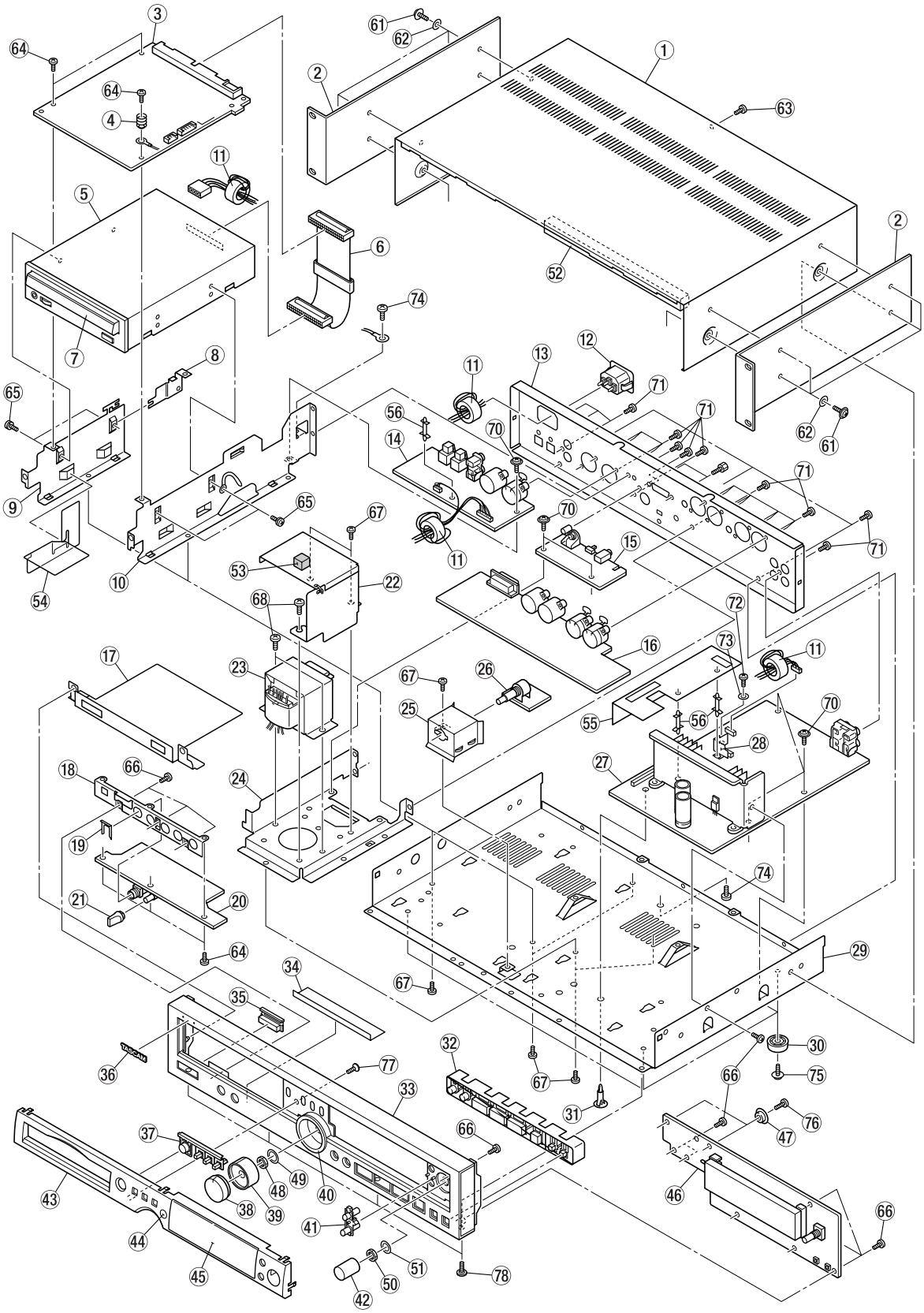
注 意

- プリント基板は部品面が示されています。
- ∗印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品及び品番のない部品は供給しません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠は安全重要部品です。
  交換する時は必ずティアック指定の部品を使用してください。
- 仕向先
  [J]: JAPAN [US/C]: U.S.A./CANADA [K]: KOREA [E]: EUROPE
  [UK]: U.K. [A]: AUSTRALIA

5. EXPLODED VIEW AND PARTS LIST

分解図とパーツリスト

EXPLODED VIEW-1



EXPLODED VIEW-1

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	*3M0058120A	BONNET	
1- 2	*3M0073210B	RACK MOUNT ANGLE,N64	
1- 3	*3E9524720B	PCB ASSY,CONVERTER	
1- 4	*3M0101500A	SPRING,EARTH BONNET	
1- 5	V00089500A	CD-W54E-A90	
1- 6	*3E0117100A	WIREA,DRIVE-CONVERT 40P	
1- 7	*3M0089930B	PANEL,TRAY 700	
1- 8	*3M0101300A	BRACKET,EARTH CVT PCB	
1- 9	*3M0088400A	BRACKET MECHA SIDE(L)	
1-10	*3M0088500C	BRACKET MECHA SIDE(R)	
1-11	*3E010000	FERRITE CORE,B18T 25X12X15	
1-12	⚠ 5332030400	AC INLET,M1816	
1-13	*3M0111000A	PANEL,REAR	
1-14		PCB ASSY,DIGITAL I/O ·····	GATHER DIGITAL I/O PCB ASSY
1-15		PCB ASSY,CONTROL I/O ·····	GATHER DIGITAL I/O PCB ASSY
1-16		PCB ASSY,BAL I/O ·····	GATHER BAL I/O PCB ASSY
1-17	*3M0100410A	SHEET,SHILD PH PCB	
1-18	*3M0088600C	BRACKET,JACK	
1-19	*3E011630	MOUNT PLATE,JACK	
1-20		PCB ASSY,PSW/HP·····	GATHER AUDIO PCB ASSY
1-21	3M0024830A	KNOB,PHONE VOLUM N66	
1-22	*3M0112300A	CASE,TRANS SHIELD	
1-23	⚠ 3E0117710A	TRANS	
1-24	*3M0110900A	BRACKET,TRANS	
1-25	*3M0096600A	CASE,SHIELD VR	
1-26		PCB ASSY,VR ·····	GATHER FRONT PCB ASSY
1-27		PCB ASSY,AUDIO ·····	GATHER AUDIO PCB ASSY
1-28	*3M0101600B	SHEET,BARRIER CONECT	
1-29	*3M0057910B	CHASSIS,MAIN	
1-30	3M001950	FOOT,21MM	
1-31	*3M0062600A	SUPPORT,PCB SCD-12	
1-32	3M0089430A	BUTTON,UNT OPE N63	
1-33	3M0088730B	PANEL,FRONT N64	
1-34	*3M0100500B	SHEET,EARTH	
1-35	3M0111200A	BUTTON,POWER N66	
1-36	5720254101	NAME PLATE,TASCAM(S)	
1-37	3M0089330A	BUTTON,UNT O/C N63	
1-38	3M0090130A	KNOB,REC(R) N66	
1-39	3M0089730A	KNOB,REC(L) N66	
1-40	3M0089130A	RING,REC KNOB N66	
1-41	3M0089230A	BUTTON,MENU N66	
1-42	3M0089830A	KNOB,D15 JOG N66	
1-43	*3M0088830A	ESCUTCHEON F,N66	
1-44	*3M0089010B	LENS,LED	
1-45	*3M0088910B	WINDOW,FL	
1-46		PCB ASSY,FRONT ·····	GATHER FRONT PCB ASSY
1-47	*3M0097400B	STOPPER,BONNET	
1-48	*3M001340	NUT,VR M9	
1-49	*3M001350	WASHER,PLAIN VR M9.1	
1-50	*3M0096900A	NUT,M7	
1-51	*3M0096800A	WASHER,PLAIN M7	

EXPLODED VIEW-1

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1-52	*3M0112800A	CUSHION,WIRE PROTECT	
1-53	*3M0112500A	CUSHION,SHIELD CASE	
1-54	*3M0110800A	SHEET,BARRIER PSW	
1-55	*3M0099200B	SHEET,BARRIER E.PWR [K,E,UK,A]	
1-56	*3M0099100A	SUPPORT,PCB CBS-15	
1-61	*3B0001812A	SCREW,J,S M3X12 (BLK)	
1-62	3M002020	WASHER,FIBER 3X8X0.3T BLK	
1-63	*3B0003808A	SCREW,VPC M3X8 BLK	
1-64	*3B0005305A	SCREW,BPB M3X5	
1-65	3B0007400A	SCREW,BPAA M3X6	
1-66	*3B0000808A	SCREW,BPP M3X8	
1-67	*3B0005708A	SCREW,BPB M3X8 (BLK)	
1-68	*3B0001908A	SCREW,J,S M4X8 (BLK)	
1-69	Vacant		
1-70	*3B0001306A	SCREW,J,S M3X6	
1-71	*3B0005708A	SCREW,BPB M3X8 (BLK)	
1-72	*3B0000106A	SCREW,BPS M3X6	
1-73	*3M0102400A	PLAIN WASHER,3.5X10X1	
1-74	*3B0005408A	SCREW,BPB M4X8	
1-75	*3B0001308A	SCREW,J,S M3X8	
1-76	*3B0000810A	SCREW,BPP M3X10	
1-77	*3B0007008A	SCREW,FPP M3X8	
1-78	*3B0007300A	SCREW,FPS TITE M3X6	

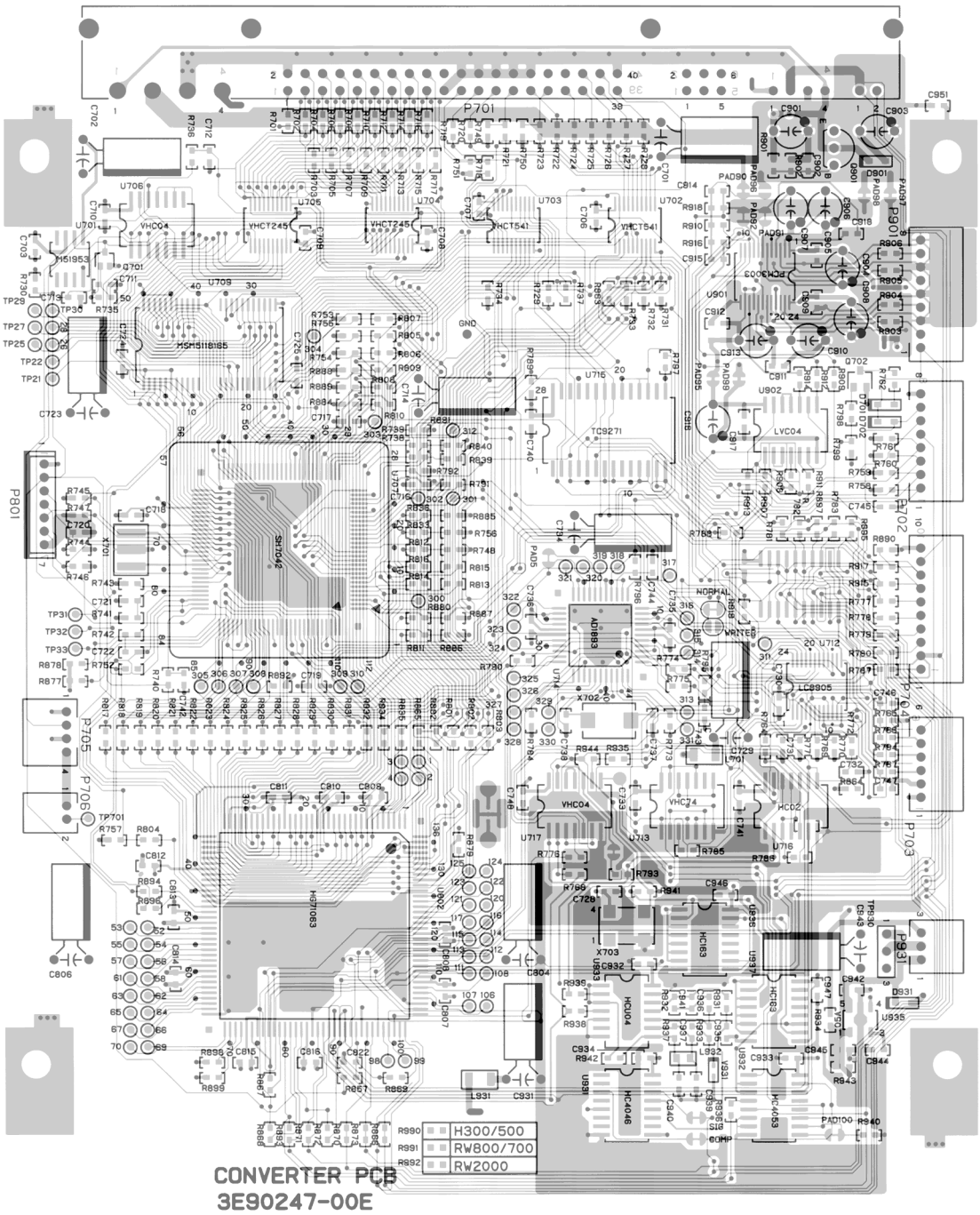
INCLUDED ACCESSORIES

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	*3D0038700A	OWNER'S MANUAL,JAPANESE [J]	
	*3D0038800A	OWNER'S MANUAL,ENGLISH [EXCEPT J]	
	*3E0137100A	REMOTE CONTROL UNIT,RC-RW2000	
	*3M0028300A	RACK MOUNT SCREW KIT	
⚠	*3E014140	POWER CORD [J]	
⚠	*3E014150	POWER CORD [US/C]	
⚠	*3E014160	POWER DORD [E]	
⚠	*3E014170	POWER CORD [UK]	
⚠	*3E014180	POWER CORD [A]	

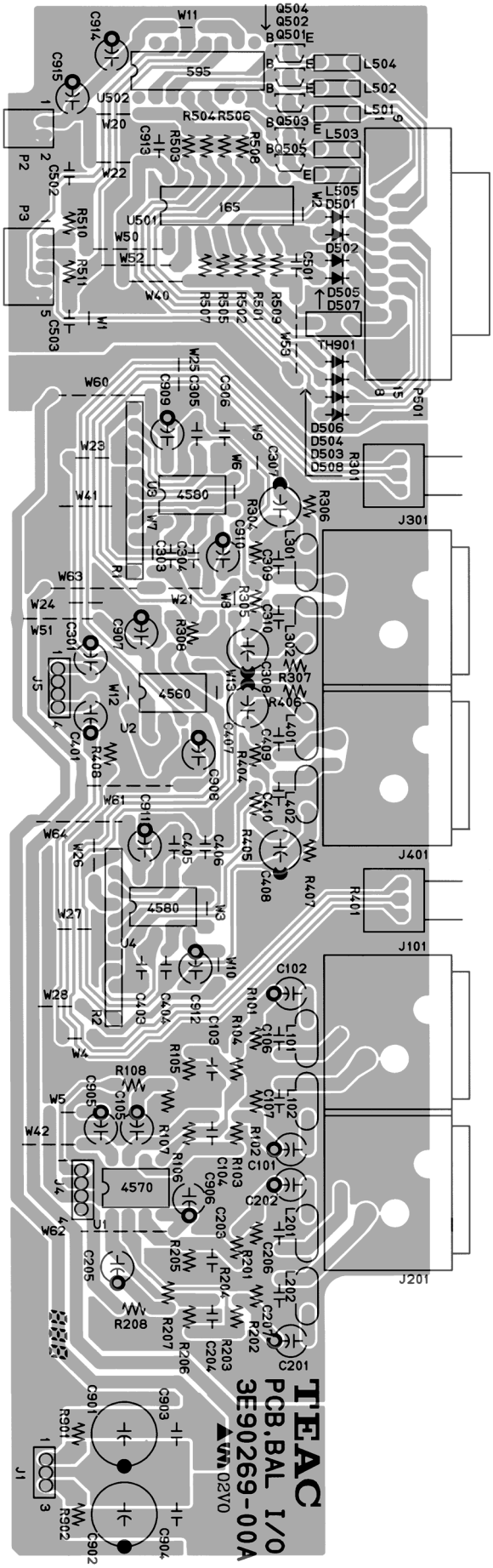
6. PC BOARDS AND PARTS LIST

基板図とパーツリスト

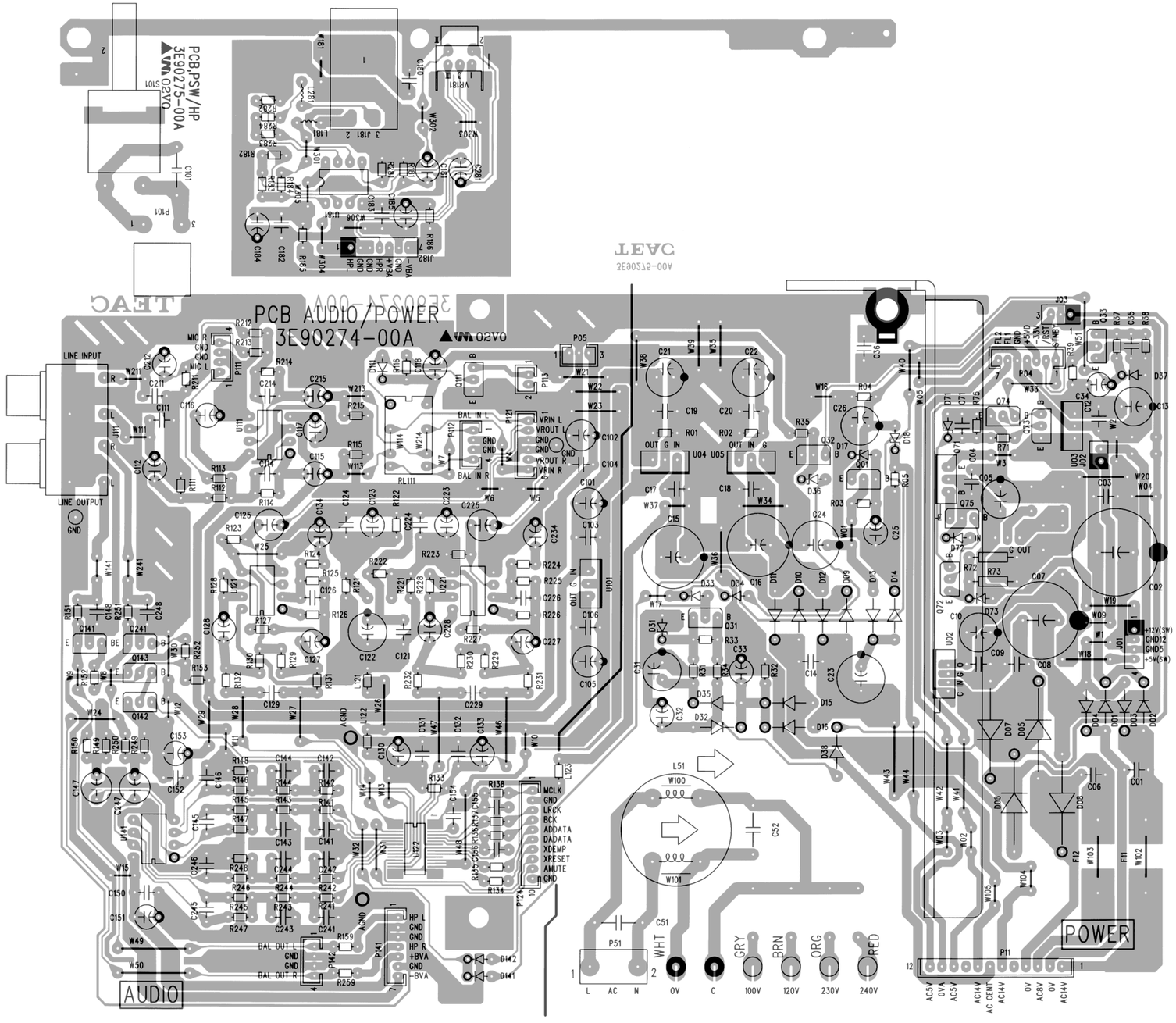
CONVERTER PCB



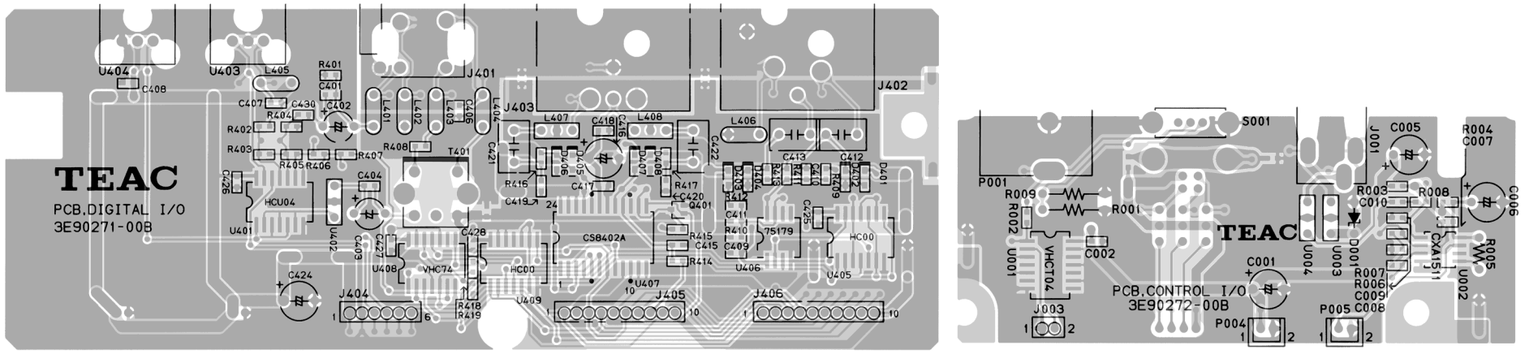
BAL I/O PCB



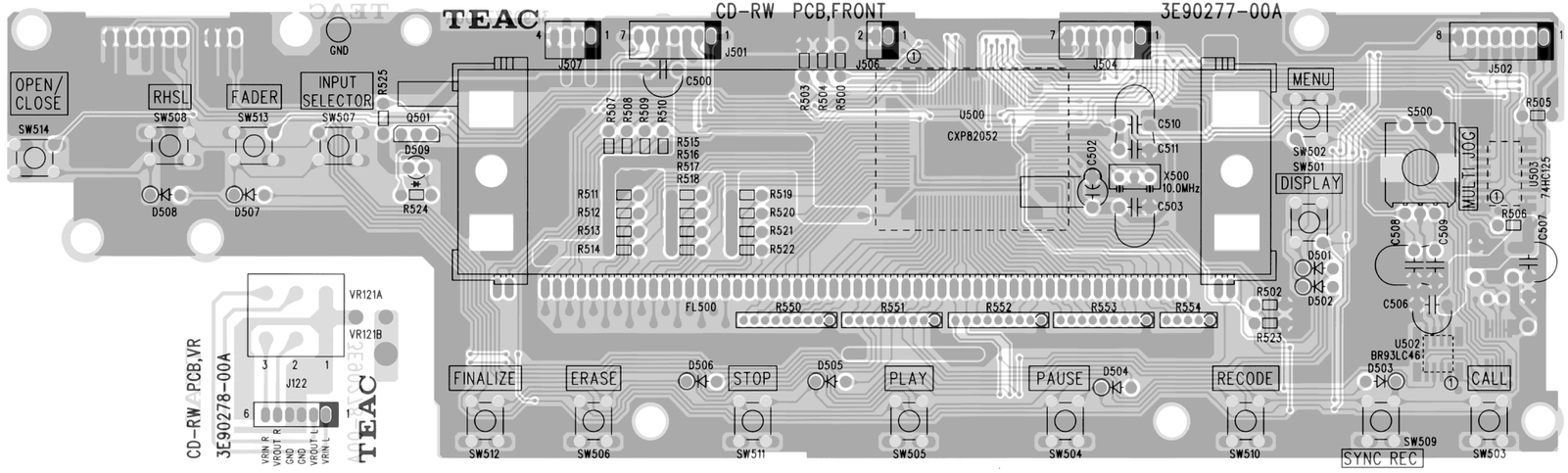
GATHER AUDIO PCB (AUDIO/POWER PCB, PSW/HP PCB)



GATHER DIGITAL I/O PCB (DIGITAL I/O PCB, CONTROL I/O PCB)



GATHER FRONT PCB (FRONT PCB, VR PCB)



CONVERTER PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*3E9524720B	PCB ASSY,CONVERTER
D701,702	3S002984	DIODE,1SS355
D931	3S002984	DIODE,1SS355
L701,931	3E014354	COIL,LQH3N 4.7UH
L932	3E014354	COIL,4.7UHLK2125
P701	3E011730	CONECT,NS-TECH CD-51 CDRW
P702	3E001340	PLUG,CONN. 8P S8B-PH-K
P703	3E001320	PLUG,CONN. S 6B-PH-K-S
P704	3E006020	PLUG,CONN. S10B-PHK (RED)
P801	3E010390	PLUG,CONN. B 7B-PH-K-S
P931	3E001290	PLUG,CONN. S 3B-PH-K-S
Q701	3S002994	TR,DTC124EUA
Q702	3S003004	TR,2SA1037AK
U702,703	S0037164	IC,TC74VHCT541AFT(EL)
U704,705	S0037174	IC,TC74VHCT245AFT(EL)
U706	3S002924	IC,TC74VHC04F(EL)SMT.TA
U707	S00386800A	IC,HD64F7044 CONVERT3
U709	S0036813	IC,MSM5118165D
U712	3S002954	IC,LC8905V
U713	3S002914	IC,TC74VHC74F(EL)SMT.TA
U714	3S002963	IC,AD1893JST
U715	3S002944	IC,TC9271F(ELP)SMT.TA
U716	3S002934	IC,TC74HC02AF(EL)SMT.TA
U717	3S002924	IC,TC74VHC04F(EL)SMT.TA
U802	S00361900A	IC,AUDIO CONVERTE CDRW
U931	3S003414	IC,TC74HC163AF(EL)
U932	3S003394	IC,TC74HC4053AF(EL)
U933	3S001344	IC,74HCU04AF
U935	3S003424	IC,NJM2370U05
U936 U937	3S003434	IC,TC74HC163AF(EL)
X701	3E011994	RES,CSTCC 7.17MG0H6-TC
X702	3E011984	X'TAL,LIM55A 16MHZ
X703	3E011974	X'TAL,11.289MHZ

GATHER BAL I/O PCB ASSY (BAL I/O PCB ASSY)

REF.NO.	PARTS NO.	DESCRIPTION
	*3E9526800A	PCB ASSY,GATHER BAL I/O
		PCB ASSY,BAL I/O
D501-507	3S000241	DIODE,1SS133 T-77
J1	3E0141100A	WIREA,POWER
J4,5	3E0141000A	WIREA,BAL I/O
J101,201	3E010320	JACK,XLR NC3FAH1
J301,401	3E010330	PLUG,XLR NC3MAH
L101,201	3E011820	FB,FBR07HA850SB-00
L102,202	3E011820	FB,FBR07HA850SB-00
L301,401	3E011820	FB,FBR07HA850SB-00
L302,402	3E011820	FB,FBR07HA850SB-00
L501-505	3E013130	FILTER,EMT103BT
P2	3E014250	PLUG,CONN. S 8B-PH-K-S
P3	3E010370	PLUG,CONN. B 5B-PH-K-S
P501	3E010920	CONECTOR,D-SUB 15P
Q501-505	3S000291	TR,DTC124ES TP
R1,2	3R0053000A	RES ARRAY,EXBF11L668FP
R301,401	3R007430	VAR RES,RK09K1110-20KB
U1	3S000280	IC,UPC4570C
U2	3S000840	IC,BA4560
U3,4	3S001700	IC,NJM4580D
U501	3S003340	IC,TC74HC165AP
U502	3S003350	IC,TC74HC595AP

GATHER AUDIO PCB ASSY
(AUDIO/POWER PCB ASSY, PSW/HP PCB)

REF.NO.		PARTS NO.	DESCRIPTION
		*3E9527300A	PCB ASSY,GATHER AUDIO
			PCB ASSY,AUDIO/POWER
		*3M0097300B	HEAT SINK
		*3M0112400A	HEAT SINK ADD
		*3E0043200A	TERMINAL,EARTH PLATE B
		*3M0101600B	SHEET,BARRIER CONNECT
		*3B0005308A	SCREW,BPB M3X8
C01	⚠	3C011640	CC,YF 50V 0.1UF Z
C02	⚠	3C012790	CE,35V 4700UF GS
C04	⚠	3C011640	CC,YF 50V 0.1UF Z
C06	⚠	3C011640	CC,YF 50V 0.1UF Z
C10	⚠	3C009700	CE,35V 100UF GS
C13	⚠	3C009700	CE,35V 100UF GS
C14	⚠	3C011640	CC,YF 50V 0.1UF Z
C15,16	⚠	3C009820	CE,25V 470PF GS
C23,24	⚠	3C009750	CE,50V 220UF GS
C31	⚠	3C009730	CE,25V 220UF GS
C32	⚠	3C000270	CE,50V 4.7UF M
C33	⚠	3C009640	CE,50V 22UF GS
C51,52	⚠	3E004300	S.KILLER,CS12-F2GA472MYAS
D01-04	⚠	3S000031	DIODE,1N4003-TR
D05-08	⚠	3S003540	DIODE,1N5404
D09-16	⚠	3S000031	DIODE,1N4003-TR
D17		3S001750	ZDI,MTZJ33B T-77
D18		3S000681	ZDI,MTZJ5.1B T-77
D31		3S002060	ZDI,MTZJ6.8B T-77
D32,35	⚠	3S000031	DIODE,1N4003-TR
D33,34		3S000241	DIODE,1SS133 T-77
D36		3S000681	ZDI,MTZJ5.1B T-77
D37		3S000241	DIODE,1SS133 T-77
D38		3S000031	DIODE,1N4003-TR
D71		3S003201	ZDI,MTZJ12B T-77
D72,73		3S000241	DIODE,1SS133 T-77
D111		3S000241	DIODE,1SS133 T-77
D141,142		3S000241	DIODE,1SS133 T-77
J01		3E0118600A	WIREA,POWER-DRIVE 4P
J02		3E0118700A	WIREA,POWER-CONVERT 4P
J03		3E0141200A	WIREA,WORD POWER
J111		3E010590	JACK,RJ-1073B-09-0320A
L51	⚠	3E004290	COIL,1MH/1.5A FKOB160MH16
L121		3E011800	COIL,1.0 UH K
L122		3E011810	COIL,47UH K
L123		3E011820	FB,FBR07HA850SB-00
P04		3E000710	PLUG,CONN. 7P B7B-PH-K
P05		3E000670	PLUG,CONN. 3P B3B-PH-K
P11		3E001240	PLUG,CONN. 12P B12B-EH-A

REF.NO.		PARTS NO.	DESCRIPTION
P51		3E002170	PIN,TERMINAL LAPPING 2P
P112		3E000680	PLUG,CONN. 4P B4B-PH-K
P113		3E014250	PLUG,CONN. S 8B-PH-K-S
P121		3E010380	PLUG,CONN. B 6B-PH-K-S
P124		3E010420	PLUG,CONN. B10B-PH-K-S
P141		3E010390	PLUG,CONN. B 7B-PH-K-S
P142		3E000680	PLUG,CONN. 4P B4B-PH-K
Q01,31	⚠	3S002300	TR,KSA733C-GTA
Q32		3S002450	TR,DTC114ESTP
Q33		3S002310	TR,KSC945C-GTA
Q71	⚠	3S000400	TR,2SB1015Y
Q72		3S002310	TR,KSC945C-GTA
Q73		3S000301	TR,DTA124ES TP
Q74		3S000291	TR,DTC124ES TP
Q75		3S002300	TR,KSA733C-GTA
Q111		3S000291	TR,DTC124ES TP
Q141,241		3S000731	TR,2SD2144S TP
Q142		3S000291	TR,DTC124ES TP
Q143		3S000301	TR,DTA124ES TP
R72,73	⚠	3R007100	RD,1/2W 470 OHM J
U02	⚠	3S003040	IC,BA05ST
U03	⚠	3S000650	IC,NJM7805FA
U04	⚠	3S002170	IC,NJM7812FA
U03,04		3M0016000A	HEAT SINK
U05	⚠	3S003030	IC,NJM7912FA
U101		3S000650	IC,NJM7805FA
U111		3S001700	IC,NJM4580D
U121,221		3S003010	IC,NJM2100D
U122		S0035883	IC,CS4223-KS
U141		3S001700	IC,NJM4580D
			PCB ASSY,PSW/HP
C101	⚠	3E004300	S.KILLER,CS12-F2GA472MYAS
J181		3E002160	JACK,JY-6313-01-030
J182		3E0116900A	WIREA,AUDIO HP 7P
L181,281		3E011800	COIL,1.0 UH K
P101		3E013990	CONNECTOR,B 3PS-VH
S101	⚠	3E013970	SW,SDKLA1-BP1
U181		3S000850	IC,NJM4560D
VR181		3R005560	VAR RES,RK09K12A-20KA

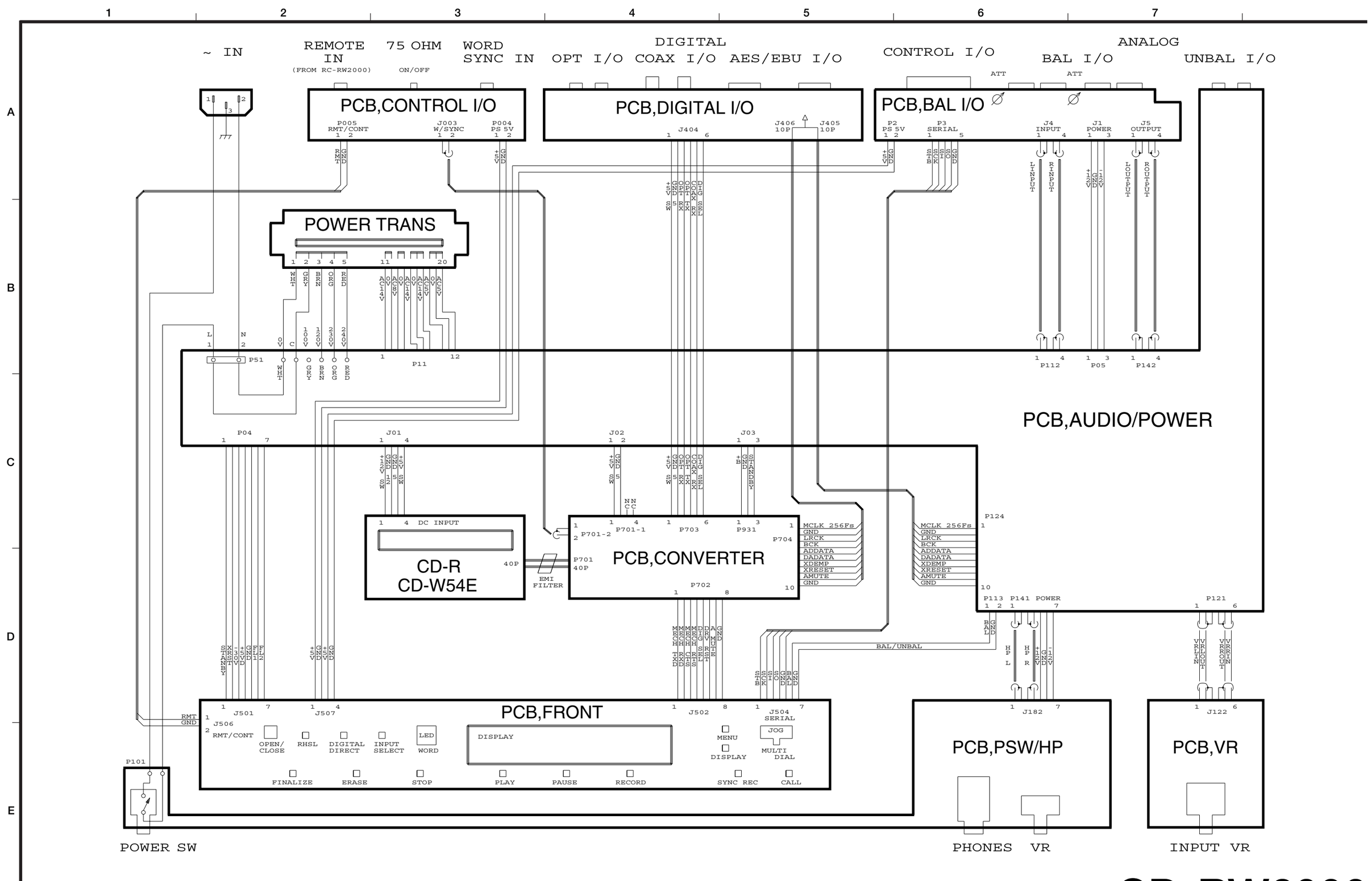
GATHER DIGITAL I/O PCB ASSY (DIGITAL I/O PCB ASSY, CONTROL I/O PCB ASSY)

REF.NO.	PARTS NO.	DESCRIPTION
	*3E9527000A	PCB ASSY,GATHER DIGITAL I/O
		PCB ASSY,DIGITAL I/O
D401-408	3S002984	DIODE,1SS355
J401	3E011850	JACK,RJ-1060A-31-0541A
J402	3E010320	JACK,XLR NC3FAH1
J403	3E010330	PLUG,XLR NC3MAH
J404	3E0140800A	WIREA,D I/O
J405	3E0141300A	WIREA,AUDIO-CON 10P
J406	3E0141310A	WIREA,AUDIO-CON
L401-L404	3E011820	FB,FBR07HA850SB-00
L405	3E011810	COIL,47UH K
L406	3E011820	COIL,FBR07HA850SB-00
L407,408	3E013950	FILTER,EMT102BT
Q401	3S002994	TR,DTC124EUA
T401	3E0132300A	PULS TRANS,S-701-001
U401	3S001344	IC,74HCU04AF
U402	3E011830	FILTER,EMT 47BT
U403	3S001680	IC,GP1F32R
U404	3S002290	IC,GP1F32T
U405	3S001624	IC,74HC00 SOP
U406	3S003364	IC,SN75179BPS
U407	3S003374	IC,CS8402A
U408	3S002914	IC,TC74VHC74F(EL)SMT.TA
		PCB ASSY,CONTROL I/O
D001	3S003451	ZDI,MTZJ2.7B T-77
J001	3E002130	JACK,MINI JY-3550A-010
J003	3E0140600A	WIREA,W/SYNC
P001	5334079700	PLUG,CONN. BNC 1P
P004	3E003810	PLUG,CONN. B2B-PH (RED)
P005	3E014250	PLUG,CONN. S 8B-PH-K-S
U001	3S003464	IC,TC74VHCT04A(EL)
U002	3S003384	IC,CXA1511M
U003	3E013130	FILTER,EMT103BT
U004	3E011830	FILTER,EMT 47BT
S001	3E013980	SW,SSSS912N-4C2-1

GATHER FRONT PCB ASSY (FRONT PCB ASSY, VR PCB ASSY)

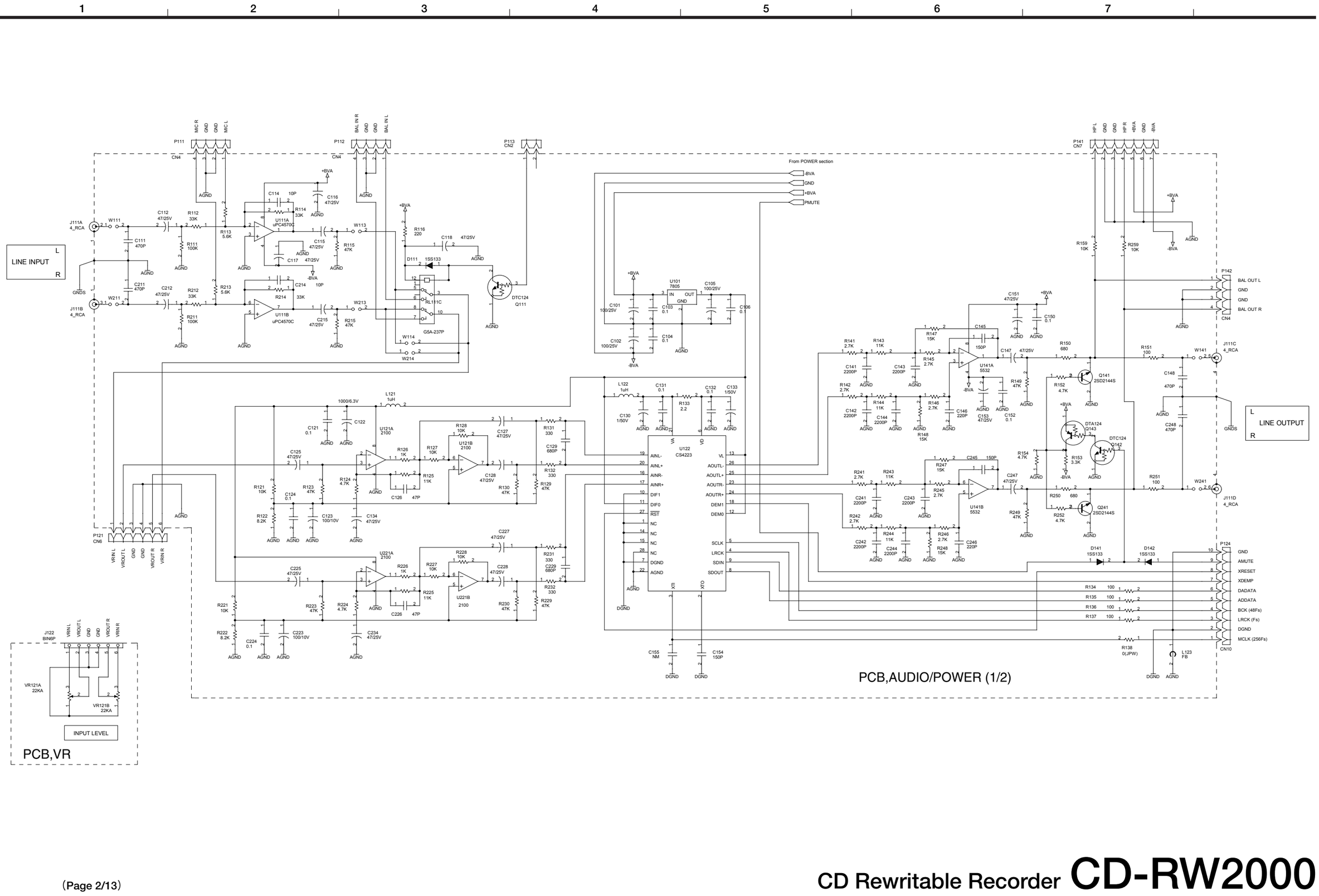
REF.NO.	PARTS NO.	DESCRIPTION
	*3E9527600A	PCB ASSY,GATHER FRONT
		PCB ASSY,FRONT
	*3M0090000B	HOLDER,FL
D501-508	3S000241	DIODE,1SS133 T-77
FL500	3E0117500A	DISPLAY,HNA-16MM23 RW(L)
J501	3E0118800A	WIREA,POWER-FRONT 7P
J502	3E0119000B	WIREA,FRONT-CONVERT 8P
J504	3E0140900A	WIREA,FRONT
J506	3E0140500A	WIREA,RMT/CONT
Q501	3S002450	TR,DTC114ESTP
SW501-514	3E002070	SW,TACT SKQSAB HMR-187
S500	3E007320	SW,ENCODER EC11B15244
U500	3S0035000A	IC,CXP82040-ROQFR
U502	3S003254	IC,BR93LC46RF-WE2 SMT TAP
U503	3S003074	IC,TC74HC125AF(EL)SMT.TA
X500	3E011740	RESONATOR,CST 10.00MTW
		PCB ASSY,VR
J122	3E0119200A	WIREA,AUDIO VR 6P
VR121	3R005550	VAR RES,RK1612220-20KA

SCHEMATIC DIAGRAM CD-RW2000 WIRING DIAGRAM

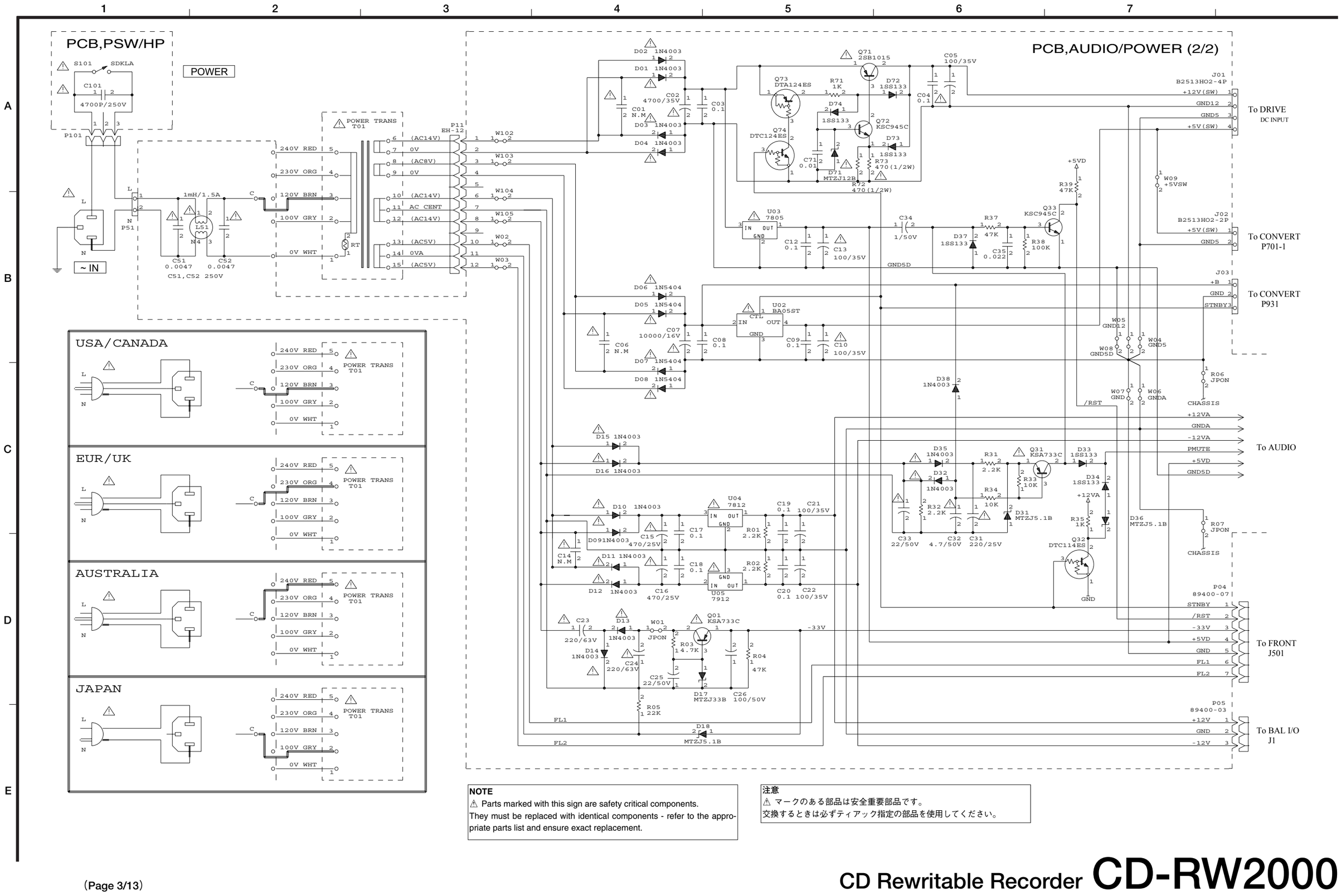


CD Rewritable Recoder **CD-RW2000**

SCHEMATIC DIAGRAM CD-RW2000 AUDIO/POWER PCB(1/2), VR PCB



SCHEMATIC DIAGRAM CD-RW2000 AUDIO/POWER PCB (2/2)

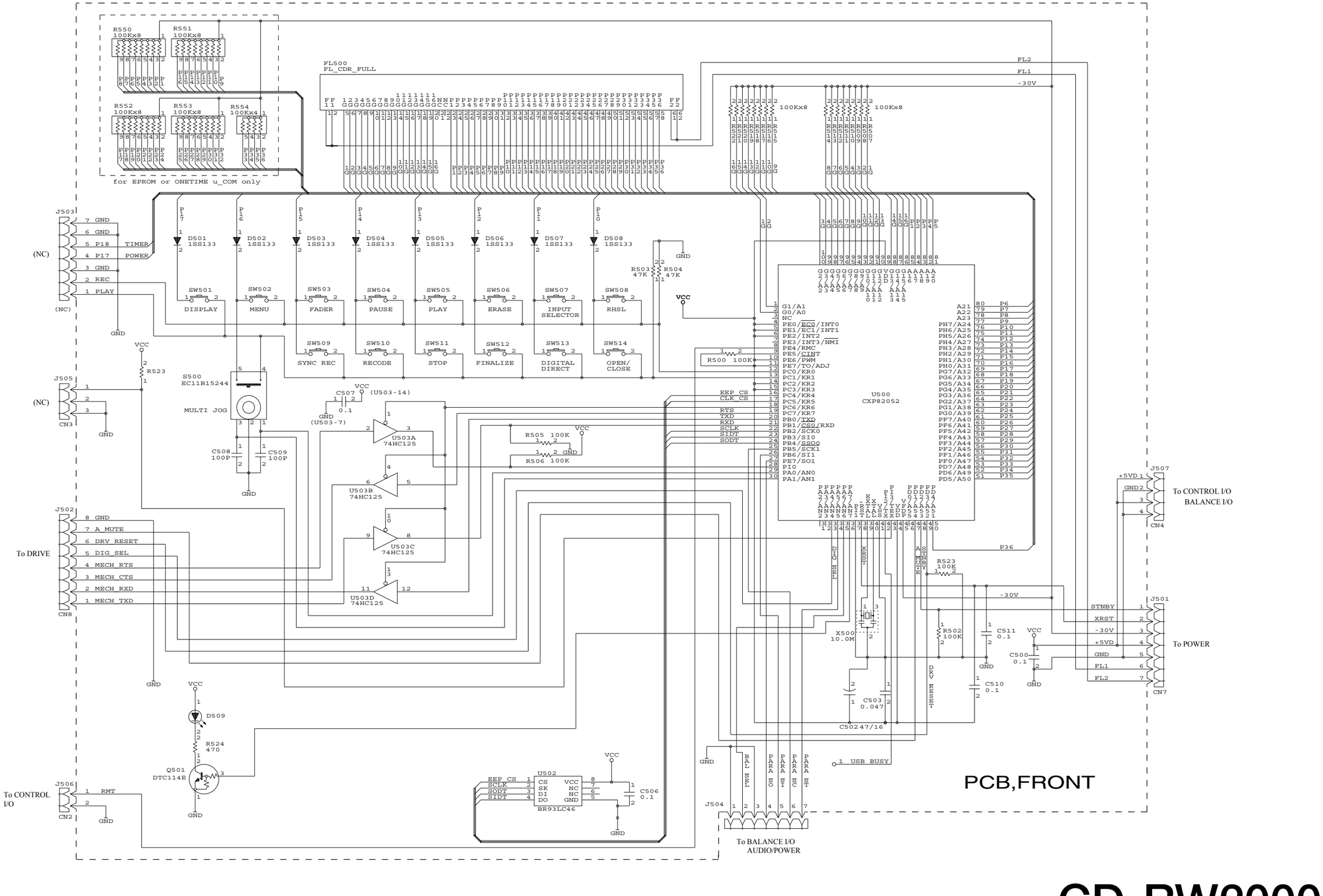


NOTE

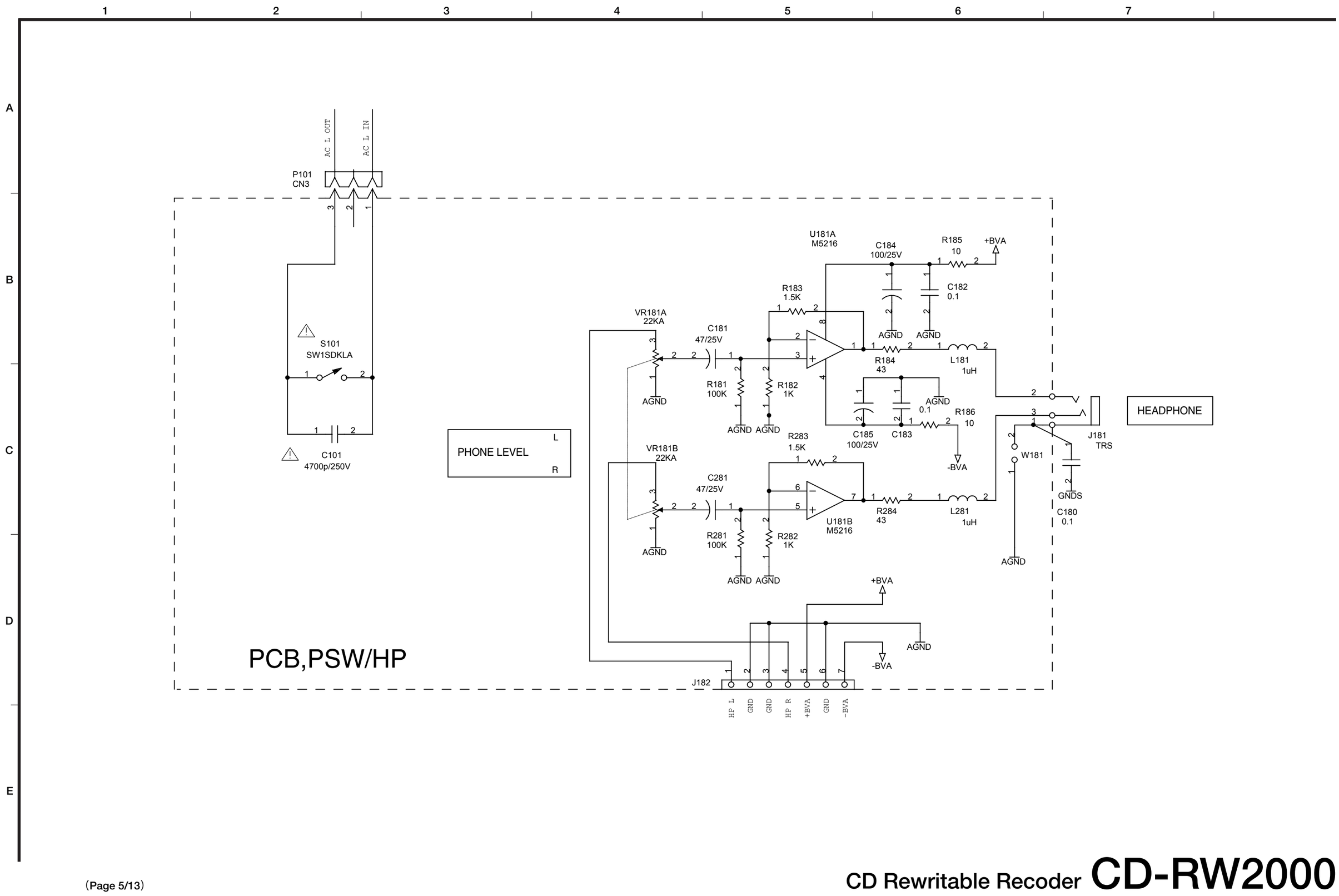
⚠ Parts marked with this sign are safety critical components.
They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.

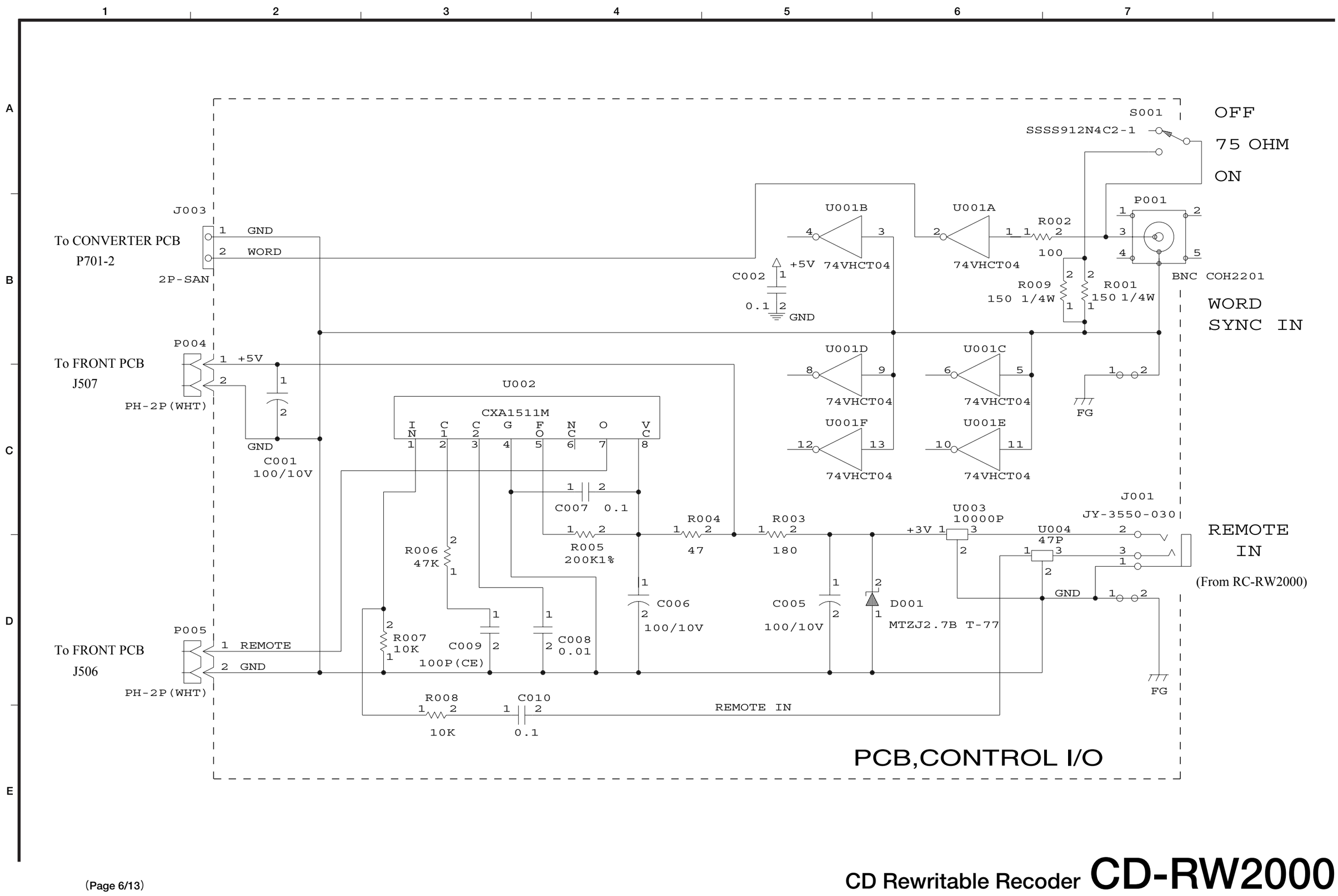
注意

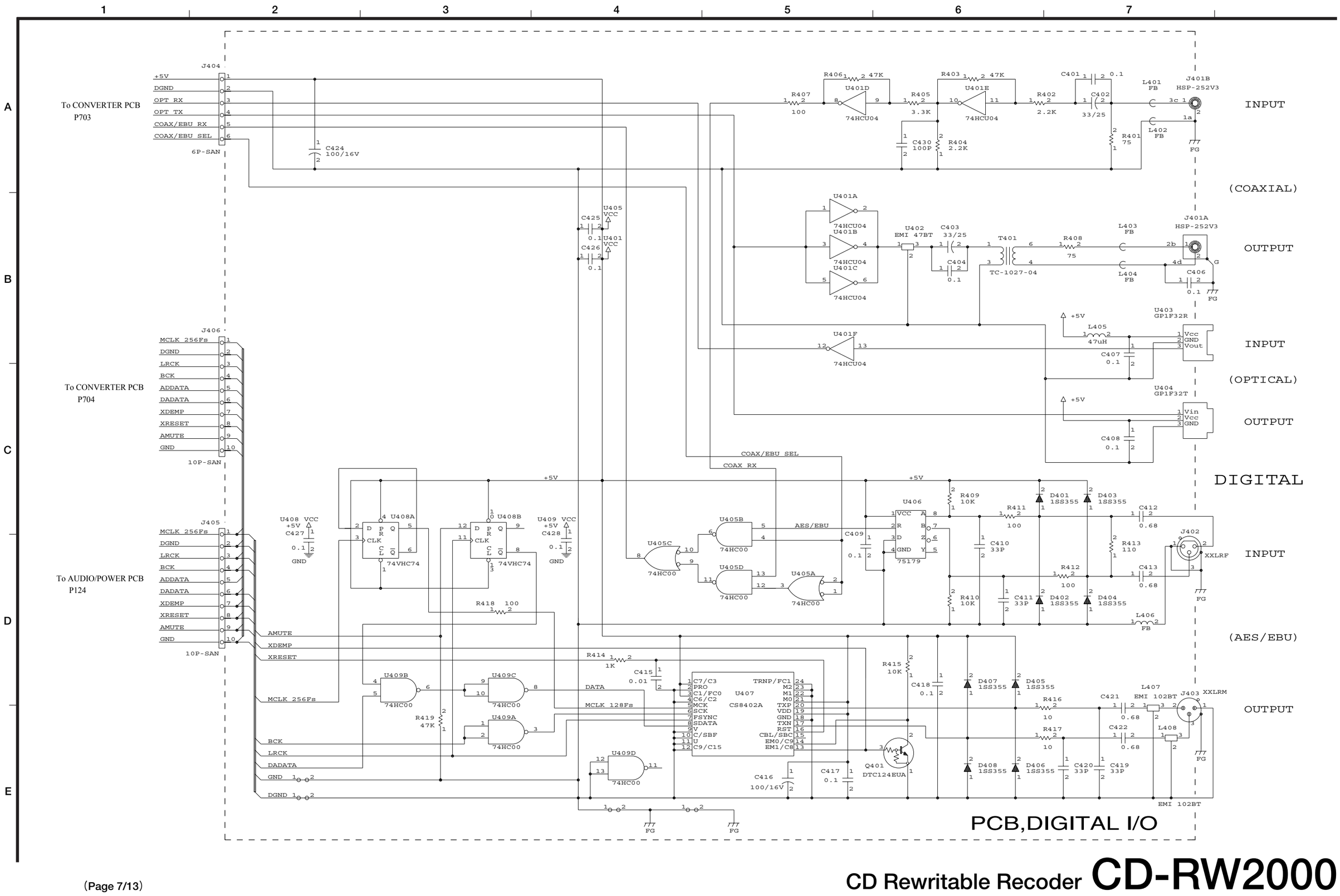
⚠ マークのある部品は安全重要部品です。
交換するときは必ずティアック指定の部品を使用してください。



CD Rewritable Recoder **CD-RW2000**


1
2
3
4
5
6
7
A
B
C
D
E
P101
CN3
AC L OUT
AC L IN
S101
SW1SDKLA
C101
4700p/250V
PHONE LEVEL
L
R
VR181A
22KA
C181
47/25V
R181
100K
R182
1K
AGND
U181A
M5216
R183
1.5K
C184
100/25V
R185
10
+BVA
C182
0.1
R184
43
L181
1uH
C185
100/25V
C183
0.1
R186
10
-BVA
R283
1.5K
VR181B
22KA
C281
47/25V
R281
100K
R282
1K
U181B
M5216
R284
43
L281
1uH
HEADPHONE
J181
TRS
W181
GNDS
C180
0.1
+BVA
-BVA
J182
HP L
GND
GND
HP R
+BVA
GND
-BVA
PCB,PSW/HP


1
2
3
4
5
6
7
A
B
C
D
E
J003
To CONVERTER PCB
P701-2
2P-SAN
1 GND
2 WORD
P004
To FRONT PCB
J507
PH-2P(WHT)
1 +5V
2
GND
C001
100/10V
U002
CXA1511M
IN C1 C2 G FO NC O VC
1 2 3 4 5 6 7 8
C007 0.1
R005
200K1%
R006
47K
R007
10K
C009
100P(CE)
C008
0.01
C006
100/10V
C005
100/10V
P005
To FRONT PCB
J506
PH-2P(WHT)
1 REMOTE
2 GND
R008
10K
C010
0.1
REMOTE IN
C002
0.1
+5V
GND
U001B
74VHCT04
U001A
74VHCT04
R002
100
R009
150 1/4W
R001
150 1/4W
S001
SSSS912N4C2-1
OFF
75 OHM
ON
P001
BNC COH2201
WORD
SYNC IN
U001D
74VHCT04
U001C
74VHCT04
FG
U001F
74VHCT04
U001E
74VHCT04
R004
47
R003
180
U003
10000P
+3V
U004
47P
J001
JY-3550-030
REMOTE
IN
(From RC-RW2000)
GND
D001
MTZJ2.7B T-77
FG
PCB,CONTROL I/O


1
2
3
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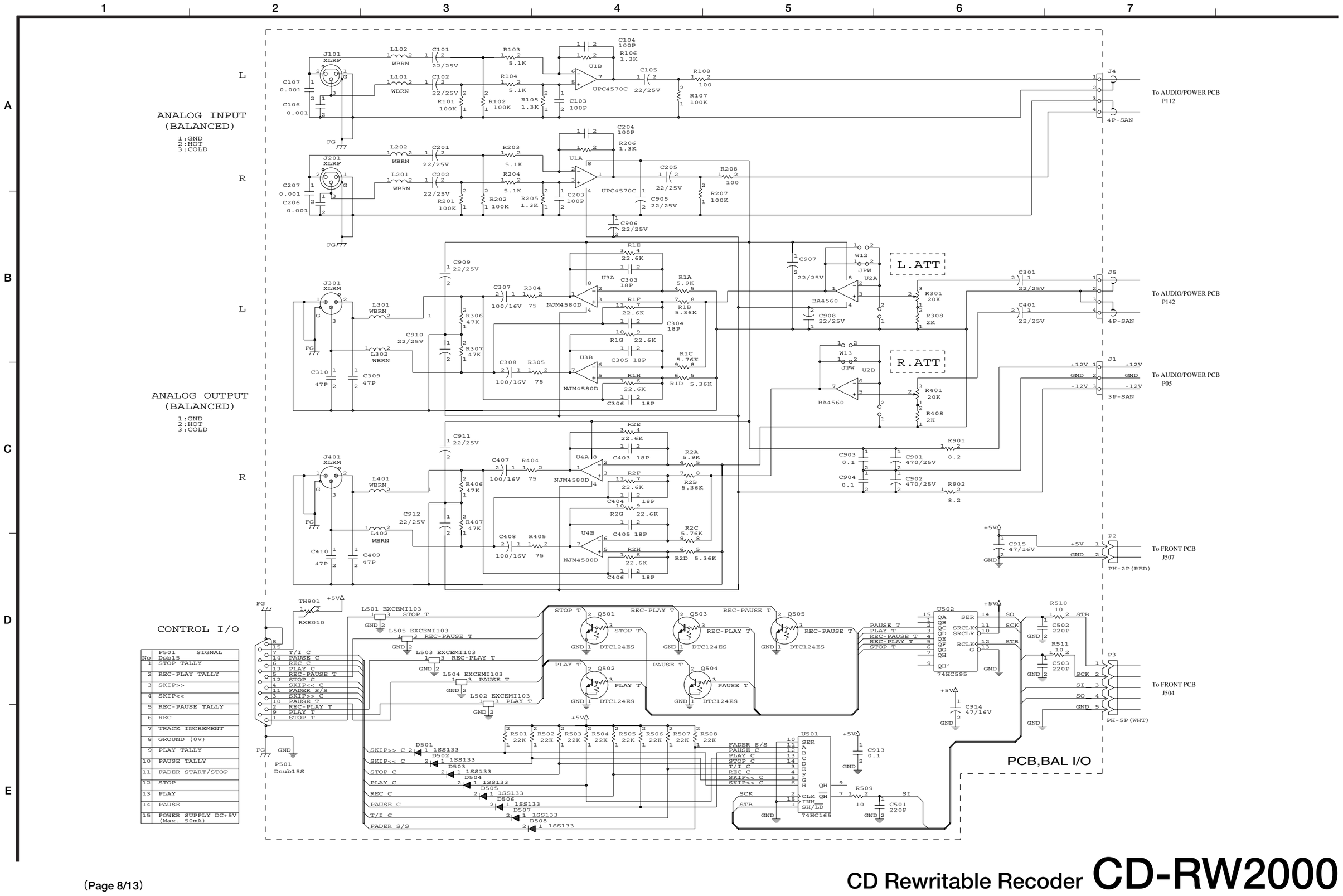
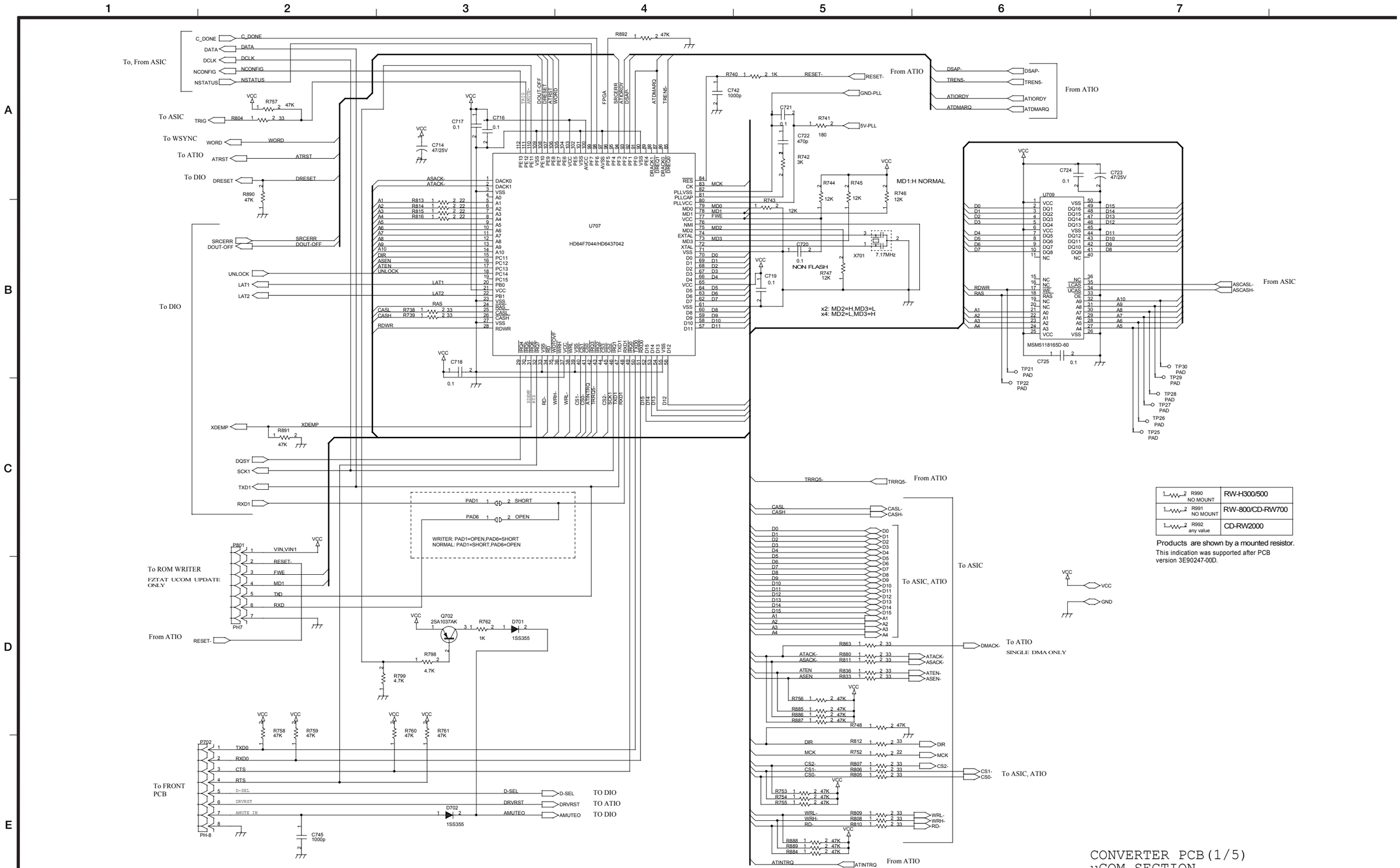
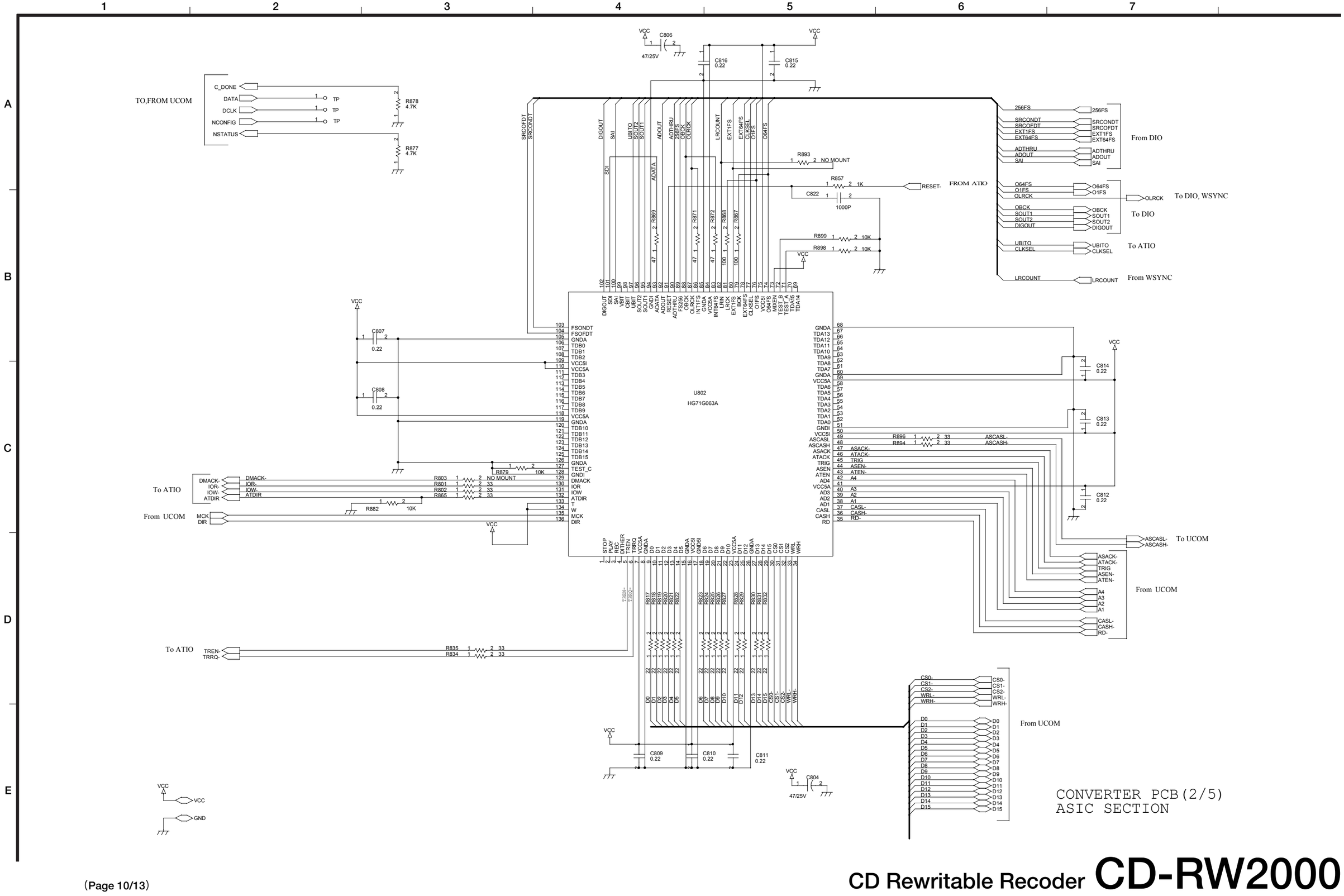
5
6
7
A
B
C
D
E
J404
+5V
DGND
OPT RX
OPT TX
COAX/EBU RX
COAX/EBU SEL
6P-SAN
To CONVERTER PCB
P703
C424
100/16V
R406 47K
R403 47K
C401 0.1
R407 100
U401D
74HCU04
R405 3.3K
U401E
74HCU04
R402 2.2K
C402 33/25
L401 FB
J401B HSP-252V3
INPUT
(COAXIAL)
C430 100P
R404 2.2K
R401 75
L402 FB
FG
U401A
74HCU04
U401B
74HCU04
U401C
74HCU04
U402 EMI 47BT
C403 33/25
T401 TC-1027-04
R408 75
L403 FB
J401A HSP-252V3
L404 FB
C404 0.1
C406 0.1
FG
OUTPUT
U405 VCC
C425 0.1
U401 VCC
C426 0.1
J406
MCLK 256Fs
DGND
LRCK
BCK
ADDATA
DADATA
XDEMP
XRESET
AMUTE
GND
10P-SAN
To CONVERTER PCB
P704
U401F
74HCU04
U403 GP1F32R
L405 47uH
C407 0.1
Vcc
GND
Vout
INPUT
(OPTICAL)
U404 GP1F32T
Vin
Vcc
GND
C408 0.1
OUTPUT
COAX/EBU SEL
COAX RX
J405
To AUDIO/POWER PCB
P124
U408 VCC
+5V
C427 0.1
GND
U408A
74VHC74
U408B
74VHC74
U409 VCC
C428 0.1
U405B
74HC00
U405C
74HC00
U405D
74HC00
U405A
74HC00
AES/EBU
U406
75179
C409 0.1
R409 10K
R411 100
C410 33P
D401 1SS355
D403 1SS355
C412 0.68
R413 110
J402 XXLRF
INPUT
R412 100
C411 33P
R410 10K
D402 1SS355
D404 1SS355
C413 0.68
FG
L406 FB
(AES/EBU)
R418 100
AMUTE
XDEMP
XRESET
MCLK 256Fs
BCK
LRCK
DADATA
GND
DGND
R414 1K
C415 0.01
U409B
74HC00
U409C
74HC00
U409A
74HC00
R419 47K
DATA
MCLK 128Fs
U409D
74HC00
U407 CS8402A
C1/C3
PRO
C1/FC0
C2/C2
MCK
SCK
FSYNC
SDATA
V
C/SBF
U
C9/C15
TRNP/FC1
M2
M1
M0
TXP
VDD
GND
TXN
RST
CBL/SBC
EM0/C9
EM1/C8
C416 100/16V
C417 0.1
Q401 DTC124EUA
R415 10K
C418 0.1
D407 1SS355
D405 1SS355
R416 10
C421 0.68
L407 EMI 102BT
J403 XXLRM
OUTPUT
R417 10
C422 0.68
L408
D408 1SS355
D406 1SS355
C420 33P
C419 33P
FG
EMI 102BT
PCB,DIGITAL I/O
DIGITAL


1
2
3
4
5
6
7
A
B
C
D
E
ANALOG INPUT
(BALANCED)
1:GND
2:HOT
3:COLD
L
R
J101
XLRF
J201
XLRF
L102
L101
L202
L201
WBRN
C101
C102
C201
C202
22/25V
C107
0.001
C106
0.001
C207
0.001
C206
0.001
FG
R103
R104
R203
R204
5.1K
R101
100K
R102
100K
R105
1.3K
R201
100K
R202
100K
R205
1.3K
C104
100P
R106
1.3K
C204
100P
R206
1.3K
U1B
U1A
UPC4570C
C103
100P
C203
100P
C105
C205
R108
R208
100
R107
100K
R207
100K
C905
22/25V
C906
22/25V
J4
4P-SAN
To AUDIO/POWER PCB
P112
ANALOG OUTPUT
(BALANCED)
1:GND
2:HOT
3:COLD
J301
XLRM
J401
XLRM
L301
L401
L302
L402
WBRN
C910
C912
C909
C911
22/25V
C310
C410
47P
C309
C409
47P
R306
47K
R307
47K
R406
47K
R407
47K
C307
C407
R304
R404
100/16V
75
C308
C408
R305
R405
NJM4580D
U3A
U4A
U3B
U4B
R1E
R2E
R1G
R2G
22.6K
R1A
R2A
5.9K
R1F
R2F
R1B
R2B
5.36K
R1C
R2C
5.76K
R1H
R2H
R1D
R2D
5.36K
C303
18P
C403
C304
C305
C405
C306
C406
C404
J5
4P-SAN
To AUDIO/POWER PCB
P142
C907
C908
22/25V
W12
W13
JPW
U2A
U2B
BA4560
L.ATT
R.ATT
R301
20K
R308
2K
R401
20K
R408
2K
C301
C401
22/25V
J1
3P-SAN
To AUDIO/POWER PCB
P05
+12V
GND
-12V
R901
8.2
C903
0.1
C904
0.1
C901
470/25V
C902
470/25V
R902
8.2
CONTROL I/O
P501 SIGNAL
No Dsub15
1 STOP TALLY
2 REC-PLAY TALLY
3 SKIP>>
4 SKIP<<
5 REC-PAUSE TALLY
6 REC
7 TRACK INCREMENT
8 GROUND (0V)
9 PLAY TALLY
10 PAUSE TALLY
11 FADER START/STOP
12 STOP
13 PLAY
14 PAUSE
15 POWER SUPPLY DC+5V
(Max. 50mA)
P501
Dsub15S
TH901
RXE010
+5V
GND
L501 EXCEMI103
L505 EXCEMI103
L503 EXCEMI103
L504 EXCEMI103
L502 EXCEMI103
STOP T
REC-PLAY T
REC-PAUSE T
PLAY T
PAUSE T
Q501
Q503
Q505
Q502
Q504
DTC124ES
T/I C
PAUSE C
REC C
PLAY C
REC-PAUSE T
STOP C
SKIP<< C
FADER S/S
SKIP>> C
PAUSE T
REC-PLAY T
PLAY T
STOP T
R501
R502
R503
R504
R505
R506
R507
R508
22K
D501
D502
D503
D504
D505
D506
D507
D508
1SS133
U501
74HC165
SER
A
B
C
D
E
F
G
H
QH
CLK
INH
SH/LD
SCK
STB
SI
C913
0.1
C501
220P
R509
10
U502
74HC595
QA
QB
QC
QD
QE
QF
QG
QH
QH'
SRCLK
SRCLR
RCLK
SO
R510
R511
C502
C503
220P
C914
47/16V
C915
47/16V
P2
P3
To FRONT PCB
J507
To FRONT PCB
J504
PH-2P(RED)
PH-5P(WHT)
PCB,BAL I/O

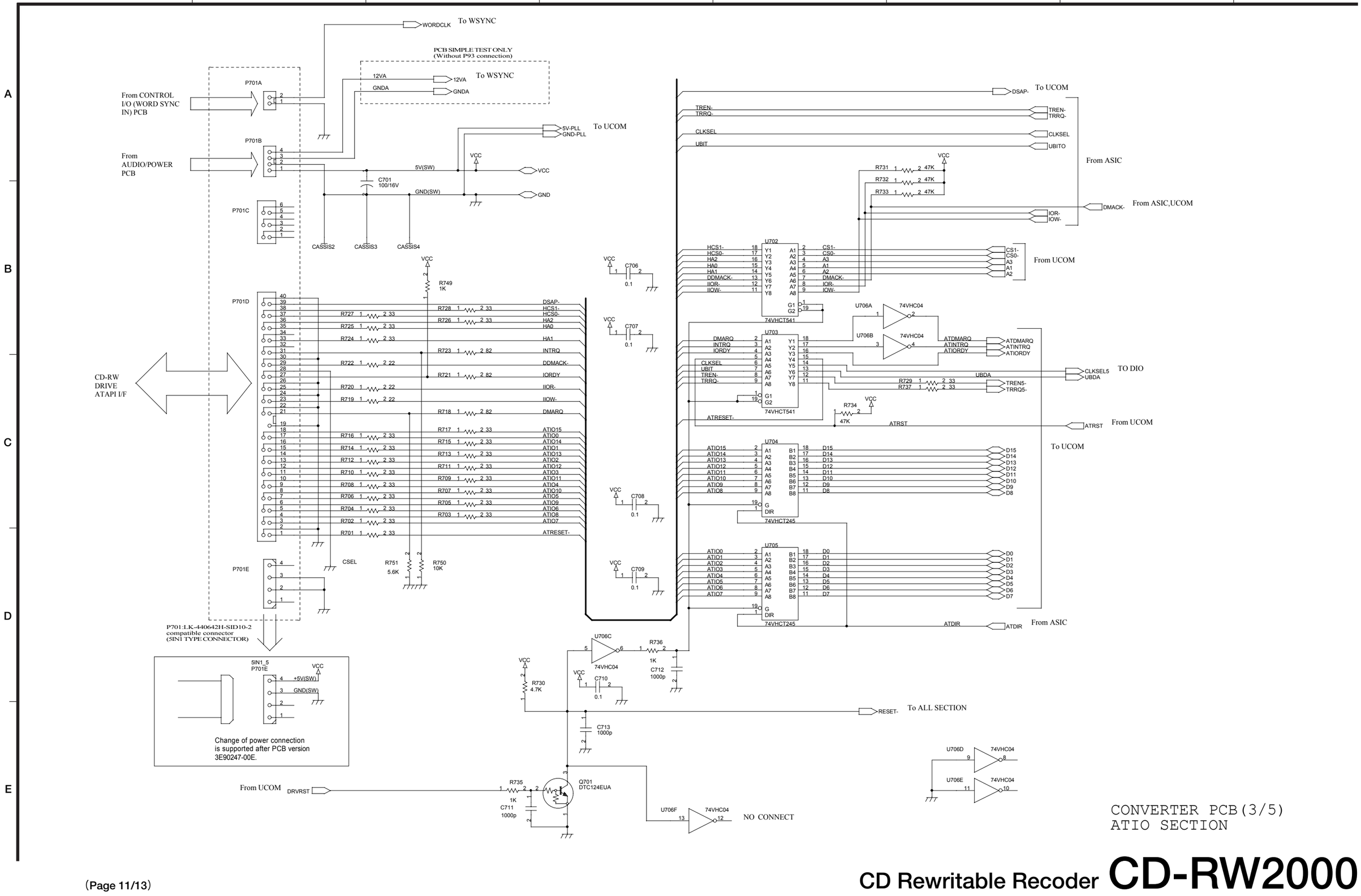
SCHEMATIC DIAGRAM CD-RW2000 CONVERTER PCB (1/5)



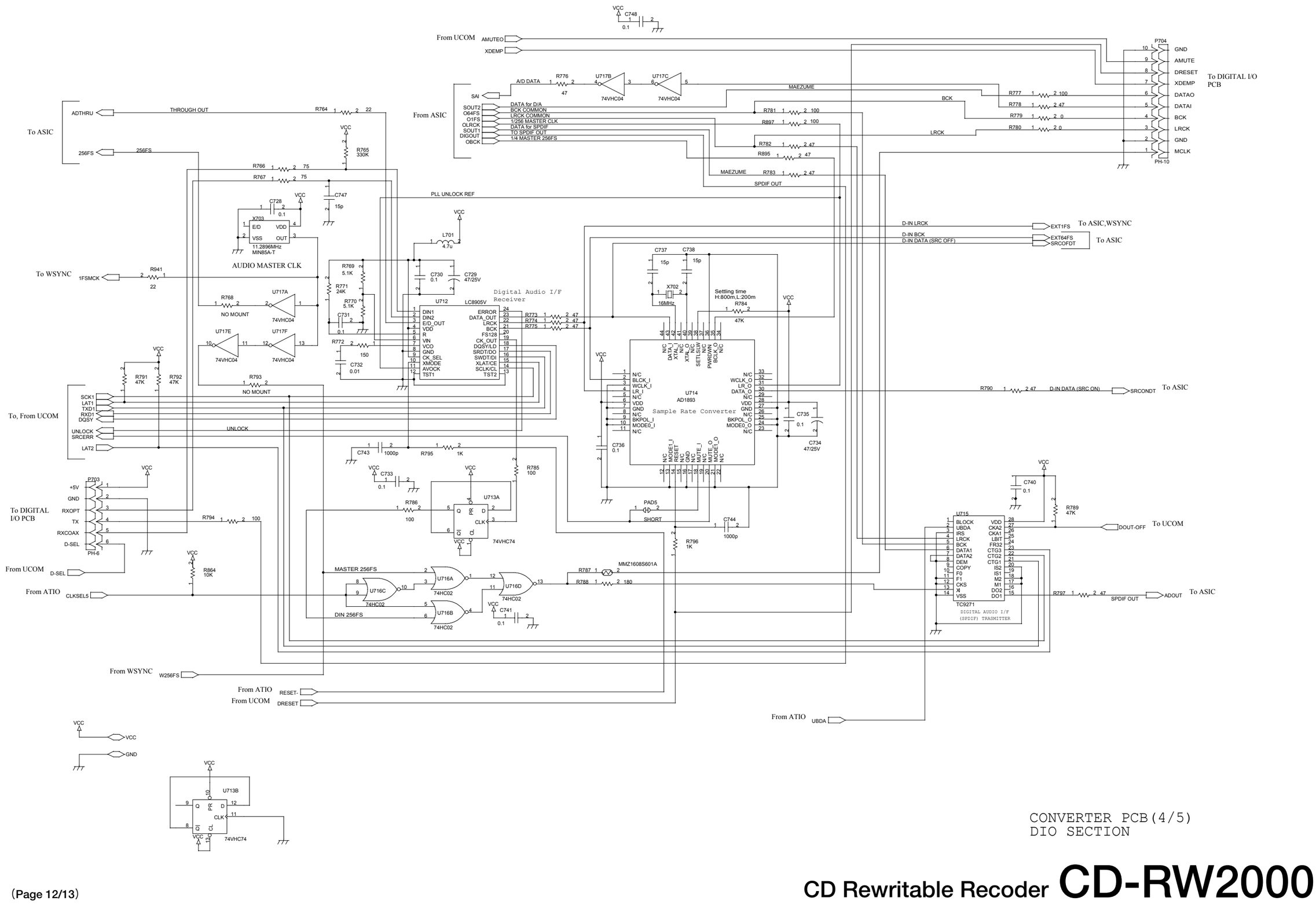
SCHEMATIC DIAGRAM CD-RW2000 CONVERTER PCB (2/5)



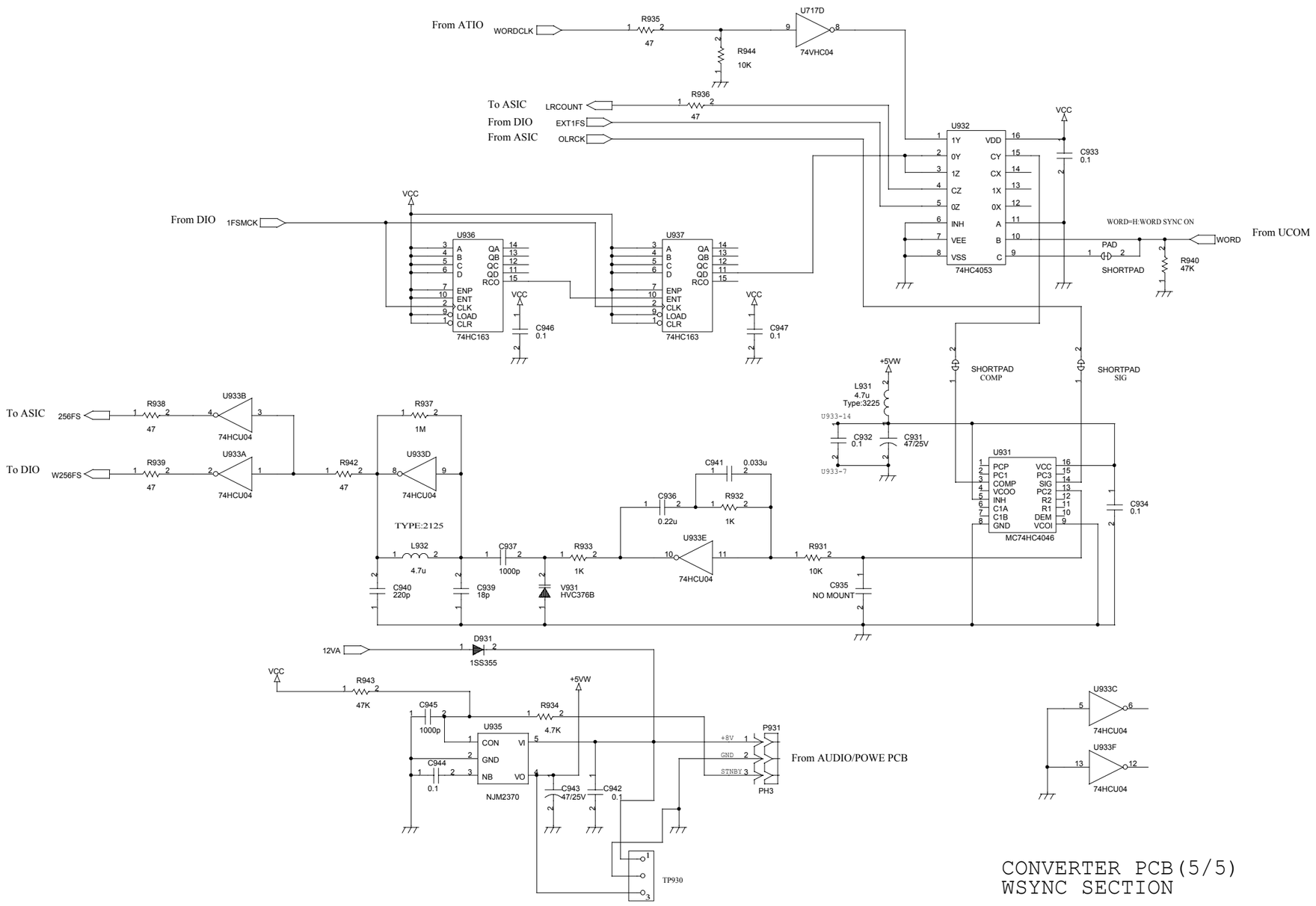
SCHEMATIC DIAGRAM CD-RW2000 CONVERTER PCB (3/5)



CONVERTER PCB(3/5)
ATIO SECTION



CONVERTER PCB(4/5)
DIO SECTION



CONVERTER PCB(5/5)
WSYNC SECTION

TASCAM
TEAC Professional Division

CD-RW2000V3

SERVICE MANUAL

SUPPLEMENT

追補版

The circuit diagrams here are applicable for CD-RW2000 S/No. 0390001 and higher.
Use this with the original CD-RW2000 Service Manual, Effective: June, 2000.

ここに記載されている回路図は、シリアル No. 0390001 以降の CD-RW2000 に適用されます。
CD-RW2000 のオリジナルサービスマニュアル、Effective: June, 2002 と共に使用してください。

Changes（変更内容）

1..To adopt a new CD-RW DRIVE, related components have been changed with renewal of Converter MPU and Front MPU accordingly.
DRAM on Converter PCB Assy has been changed due to its availability.
CD-RW DRIVEを変更するとともに、関連部品を変更しました。
DRAM入手難の為にPCBA,CONVERTER RW2 U709を変更しました。

2. To cope with above, the major difference of parts are as follows:
上記による主要な差異部品は以下の通りです。

1- 5	V00089500A	DRIVE ASSY,CD-W54E-A90	→	V00140000A	CD-W58DA-T00	
1- 7	3M0089930B	PANEL,TRAY 700	→	M02038200A	PANEL,TRAY RW2000 (ASS)	
1- 9	3M0088400A	BRACKET MECH SIDE(L)	→	M02038600A	BRACKET MECH (L) RW2000	
1-10	3M0088500C	BRACKET MECH SIDE(R)	→	M02038700A	BRACKET MECH (R) RW2000	
1-43	3M0088830A	ESCUTCHEON F,N66	→	M02038400A	ESCUTCHEON,FRONT, RW2000	
1- 3	*V00140600A	PCB ASSY,CONVERTER	→	3E9524720B	PCB ASSY,CONVERTER 2000V3	
	S00386800A	HD64F7044-CONVT3	→	3S0048510B	UCOM Assy,HD64F7044 402V3	U707 MPU
	S0036813	IC,MSM5118165D	→	S0060813	IC,T2316162A-50SIC	U709 DRAM
1-46	3E9527600A	PCB ASSY GATHER,FRONT	→	3E9527600A	PCB ASSY GATHER,FRONT	(No change)
	3S0035000A	IC,CXP82040-ROQFR	→	S00598300A	IC,CXP82040-160Q Front3 G	IC, U500

* This is newly registered P/N since CD-RW2000V3 is produced with an identical P/N.
Ensure the P/N by confirming the S/No. of the unit being repaired upon ordering it.
* CD-RW-2000V3は旧機と同一品番で生産されているため、新規に登録した品番です。
修理機の機番を確認のうえ、正しい品番で発注してください。

Effective: August, 2005

CS4223
CS4224

24-Bit 105 dB Audio Codec with Volume Control

Features

- 105 dB Dynamic Range A/D Converters
- 105 dB Dynamic Range D/A Converters
- 110 dB DAC Signal-to-Noise Ratio (EIAJ)
- Analog Volume Control (CS4224 only)
- Differential Inputs / Outputs
- On-chip Anti-aliasing and Output Smoothing Filters
- De-emphasis for 32, 44.1 and 48 kHz
- Supports Master and Slave Modes
- Single +5 V power supply
- On-Chip Crystal Oscillator
- 3 - 5 V Digital Interface

Description

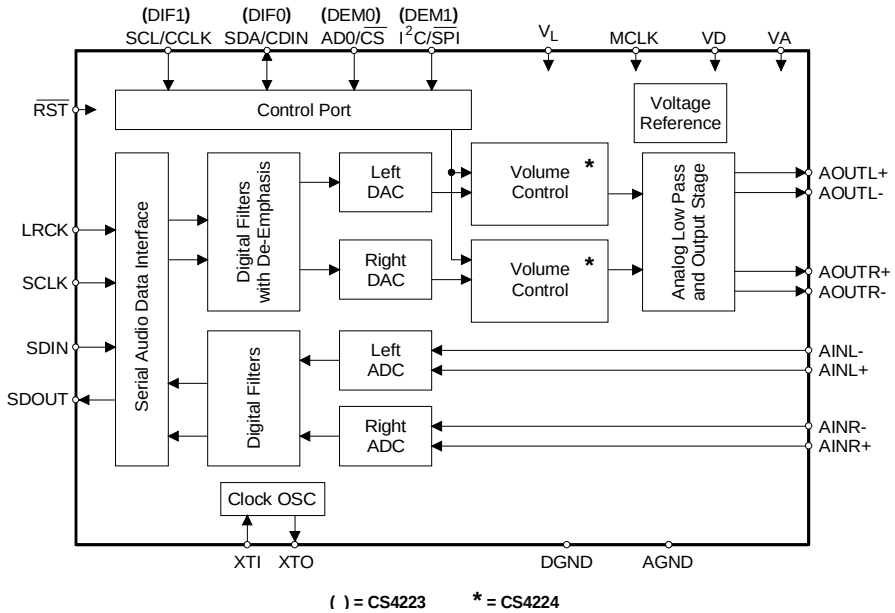
The CS4223/4 is a highly integrated, high performance, 24-bit, audio codec providing stereo analog-to-digital and stereo digital-to-analog converters using delta-sigma conversion techniques. The device operates from a single +5 V power supply, and features low power consumption. Selectable de-emphasis filter for 32, 44.1, and 48 kHz sample rates is also included.

The CS4224 includes an analog volume control capable of 113.5 dB attenuation in 0.5 dB steps. The analog volume control architecture preserves dynamic range during attenuation. Volume control changes are implemented using a "soft" ramping or zero crossing technique.

Applications include digital effects processors, DAT, and multitrack recorders.

ORDERING INFORMATION

CS4223-KS	-10 to +70 °C	28-pin SSOP
CS4223-BS	-40 to +85 °C	28-pin SSOP
CS4224-KS	-10 to +70 °C	28-pin SSOP
CS4224-BS	-40 to +85 °C	28-pin SSOP
CDB4223/4		Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

CIRRUS LOGIC®
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(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

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Contacting Cirrus Logic Support
For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25° C; VA, VD = +5 V; Full Scale Input Sine wave, 997 Hz; Fs = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in Figures 4 and 5; SPI® mode, Format 0, unless otherwise specified.)

Parameter	Symbol	CS4223/4 - KS			CS4223/4 - BS			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Input Characteristics								
ADC Resolution		-	-	24	-	-	24	Bits
Total Harmonic Distortion	THD	-	0.0014	-	-	0.0014	-	%
Dynamic Range A-weighted unweighted		100 97	105 102	- -	95 92	105 102	- -	dB dB
Total Harmonic Distortion + Noise (Note 1)	THD+N	-	-97	-92	-	-97	-87	dB
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	-	0.1	-	-	0.1	dB
Offset Error with High Pass Filter		-	-	0	-	-	0	LSB
Full Scale Input Voltage (Differential)		1.9	2.0	2.1	1.9	2.0	2.1	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Input Resistance		10	-	-	10	-	-	kΩ
Input Capacitance		-	-	15	-	-	15	pF
Common Mode Input Voltage		-	2.3	-	-	2.3	-	V
A/D Decimation Filter Characteristics								
Passband (Note 2)		0	-	21.8	0	-	21.8	kHz
Passband Ripple		-	-	±0.01	-	-	±0.01	dB
Stopband (Note 2)		30	-	6114	30	-	6114	kHz
Stopband Attenuation (Note 3)		80	-	-	80	-	-	dB
Group Delay (Fs = Output Sample Rate) (Note 4)	t_{gd}	-	15/Fs	-	-	15/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0	-	-	0	µs
High Pass Filter Characteristics								
Frequency Response -3 dB (Note 2) -0.1 dB		- -	3.7 20	- -	- -	3.7 20	- -	Hz Hz
Phase Deviation @ 20 Hz (Note 2)		-	10	-	-	10	-	Degree
Passband Ripple		-	-	0	-	-	0	dB

Notes:
1. Referenced to typical full-scale differential input voltage (2 Vrms).
2. Filter characteristics scale with output sample rate. For output sample rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.625x Fs.
3. The analog modulator samples the input at 6.144 MHz for an Fs equal to 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.8 kHz where n = 0,1,2,3...).
4. Group delay for Fs = 48 kHz, t_{gd} = 15/48 kHz = 312 µs.

ANALOG CHARACTERISTICS (CONTINUED)

Parameter	Symbol	CS4223/4 - KS			CS4223/4 - BS			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Output Characteristics - Minimum Attenuation, 10 kΩ, 100 pF load; unless otherwise specified.								
DAC Resolution		-	-	24	-	-	24	Bits
Signal-to-Noise, Idle-Channel Noise (CS4224 only) DAC muted, A-weighted		102	110	-	97	110	-	dB
Dynamic Range DAC not muted, A-weighted		100	105	-	95	105	-	dB
DAC not muted, unweighted		97	102	-	92	102	-	dB
Total Harmonic Distortion	THD	-	0.0014	-	-	0.0014	-	%
Total Harmonic Distortion + Noise	THD+N	-	-97	-92	-	-97	-87	dB
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	-	0.1	-	-	0.1	dB
Attenuation Step Size All Outputs		0.35	0.5	0.65	0.35	0.5	0.65	dB
Programmable Output Attenuation Span		110	113.5	-	110	113.5	-	dB
Differential Offset Voltage		-	±10	-	-	±10	-	mV
Common Mode Output Voltage		-	2.4	-	-	2.4	-	V
Full Scale Output Voltage		1.8	1.9	2.0	1.8	1.9	2.0	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Out-of-Band Energy Fs/2 to 2 Fs		-	-60	-	-	-60	-	dBFs
Analog Output Load Resistance		10	-	-	10	-	-	kΩ
Capacitance		-	-	100	-	-	100	pF
Combined Digital and Analog Filter Characteristics								
Frequency Response10 Hz to 20 kHz		-	±0.1	-	-	±0.1	-	dB
Deviation from Linear Phase		-	±0.5	-	-	±0.5	-	Degree
Passband: to 0.01 dB corner (Notes 5 and 6)		0	-	21.8	0	-	21.8	kHz
Passband Ripple (Note 6)		-	-	±0.01	-	-	±0.01	dB
Stopband (Notes 5 and 6)		26.2	-	-	26.2	-	-	kHz
Stopband Attenuation (Note 7)		70	-	-	70	-	-	dB
Group Delay (Fs = Input Word Rate)	t_{gd}	-	16/Fs	-	-	16/Fs	-	s
Power Supply								
Power Supply Current VA		-	46	60	-	46	60	mA
VD		-	9	20	-	9	20	mA
VL		-	3	5	-	3	5	mA
Total Power Down		-	0.4	-	-	0.4	-	mA
Power Supply Rejection Ratio 1 kHz		-	65	-	-	65	-	dB

Notes: 5. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.5465x Fs.

6. Digital filter characteristics.

7. Measurement bandwidth is 10 Hz to 3 Fs.

DIGITAL CHARACTERISTICS (T_A = 25° C; VA, VD = 4.75V - 5.25V)

Parameter		Symbol	Min	Max	Unit
High-level Input Voltage	VL = 5V	V_{IH}	2.8	VL + 0.3	V
	VL = 3V	V_{IH}	2.0	VL + 0.3	V
Low-level Input Voltage		V_{IL}	-0.3	0.8	V
High-level Output Voltage at I_O = -2.0 mA		V_{OH}	VL - 1.0	-	V
Low-level Output Voltage at I_O = 2.0 mA		V_{OL}	-	0.5	V
Input Leakage Current	Digital Inputs		-	10	µA
Output Leakage Current	High Impedance Digital Outputs		-	10	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Unit
Power Supplies	Digital	VD	-0.3	6.0	V
	Analog	VA	-0.3	6.0	V
Input Current	(Note 8)		-	±10	mA
Analog Input Voltage	(Note 9)		-0.7	VA + 0.7	V
Digital Input Voltage	(Note 9)		-0.7	VD + 0.7	V
Ambient Temperature	Power Applied		-55	+125	°C
Storage Temperature			-65	+150	°C

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	Digital	VD	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
	Digital	VL	2.7	5.0	5.25	V
	| VA - VD |		-	-	0.4	V
Ambient Operating Temperature	Commercial (KS)	T_{AC}	-10	25	70	°C
	Industrial (BS)	T_{AI}	-40	25	85	°C

Notes: 8. Any pin except supplies. Transient currents of up to 100 mA on the analog input pins will not cause SCR latch-up.

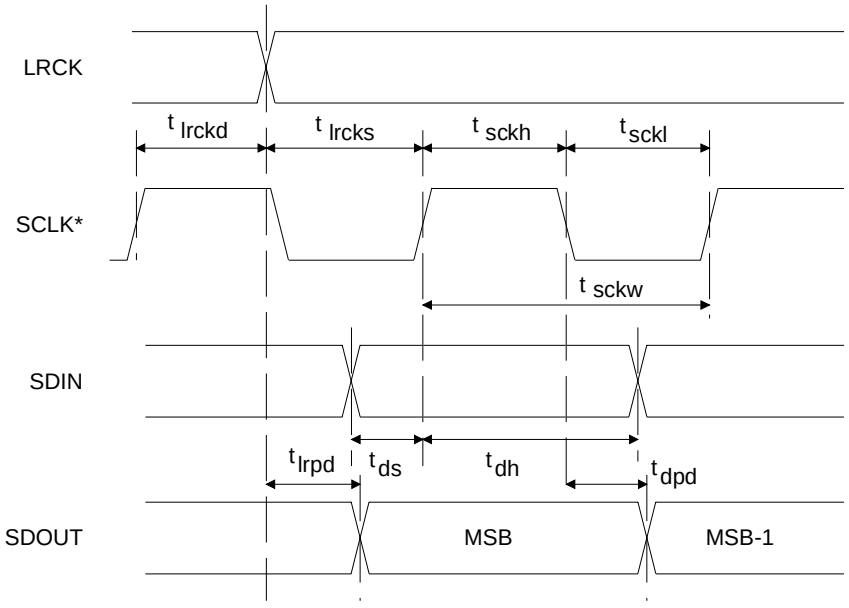
9. The maximum over or under voltage is limited by the input current.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = 25° C; VA, VD = 4.75 V - 5.25 V; outputs loaded with 30 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Audio ADC's and DAC's Sample Rate		Fs	4	-	50	kHz
XTI Frequency	XTI = 256, 384, or 512 Fs		1.024	-	26	MHz
XTI Pulse Width High	XTI = 512 Fs		13	-	-	ns
	XTI = 384 Fs		21	-	-	ns
	XTI = 256 Fs		31	-	-	ns
XTI Pulse Width Low	XTI = 512 Fs		13	-	-	ns
	XTI = 384 Fs		21	-	-	ns
	XTI = 256 Fs		31	-	-	ns
XTI Jitter Tolerance			-	500	-	psRMS
$\overline{\text{RST}}$ Low Time	(Note 10)		10	-	-	ms
SCLK falling edge to SDOUT output valid	DSCK = 0	t_{dpd}	-	-	$\frac{1}{(384)\ Fs} + 20$	ns
LRCK edge to MSB valid		t_{lrpd}	-	-	45	ns
SDIN setup time before SCLK rising edge	DSCK = 0	t_{ds}	25	-	-	ns
SDIN hold time after SCLK rising edge	DSCK = 0	t_{dh}	25	-	-	ns
SCLK Period		t_{sckw}	$\frac{1}{(128)\ Fs}$	-	-	ns
SCLK High Time		t_{sckh}	40	-	-	ns
SCLK Low Time		t_{sckl}	40	-	-	ns
SCLK rising to LRCK edge	DSCK = 0	t_{lrckd}	35	-	-	ns
LRCK edge to SCLK rising	DSCK = 0	t_{lrcks}	40	-	-	ns

Notes: 10. After powering up the CS4223/4, PDN should be held low for 10 ms to allow the power supply to settle.



*SCLK shown for DSCK = 0, SCLK inverted for DSCK = 1.

Figure 1. Serial Audio Port Data I/O Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE (CS4224)

(T_A = 25° C; VA, VD = 4.75 V - 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VD; C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SPI Mode (SPI/I2C = 0)					
CCLK Clock Frequency		f_{sck}	-	6	MHz
$\overline{RST}$ rising edge to $\overline{CS}$ falling	(Note 11)	t_{srs}	41	-	µs
CCLK edge to $\overline{CS}$ falling	(Note 12)	t_{spi}	500	-	ns
$\overline{CS}$ High Time between transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ falling to CCLK edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK rising setup time		t_{dsu}	40	-	ns
CCLK rising to DATA hold time	(Note 13)	t_{dh}	15	-	ns
Rise time of CCLK and CDIN	(Note 14)	t_{r2}	-	100	ns
Fall time of CCLK and CDIN	(Note 14)	t_{f2}	-	100	ns

Notes: 11. Not tested but guaranteed by design.

12. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

13. Data must be held for sufficient time to bridge the transition time of CCLK.

14. For F_{SCK} < 1 MHz.

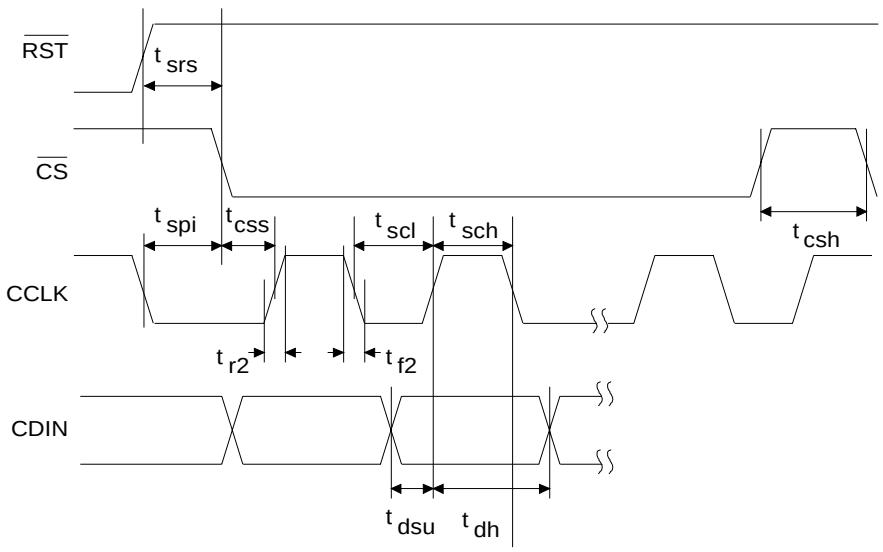


Figure 2. SPI Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I^2C MODE (CS4224)

(T_A = 25° C; VA, VD = 4.75 V - 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VD; C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
I^2C® Mode ($\overline{SPI}$/I2C = 1)				
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ rising edge to Start (Note 15)	t_{irs}	50	-	µs
Bus Free Time between transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low Time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup time for repeated Start Condition	t_{sust}	4.7	-	µs
SDA hold time for SCL falling (Note 16)	t_{hdd}	0	-	µs
SDA setup time to SCL rising	t_{sud}	250	-	ns
Rise time of SCL	t_{rc}	-	25	ns
Fall time of SCL	t_{fc}	-	25	ns
Rise time of SDA	t_{rd}	-	1	µs
Fall time of SDA	t_{fd}	-	300	ns
Setup time for Stop Condition	t_{susp}	4.7	-	µs

Notes: 15. Not tested but guaranteed by design.

16. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

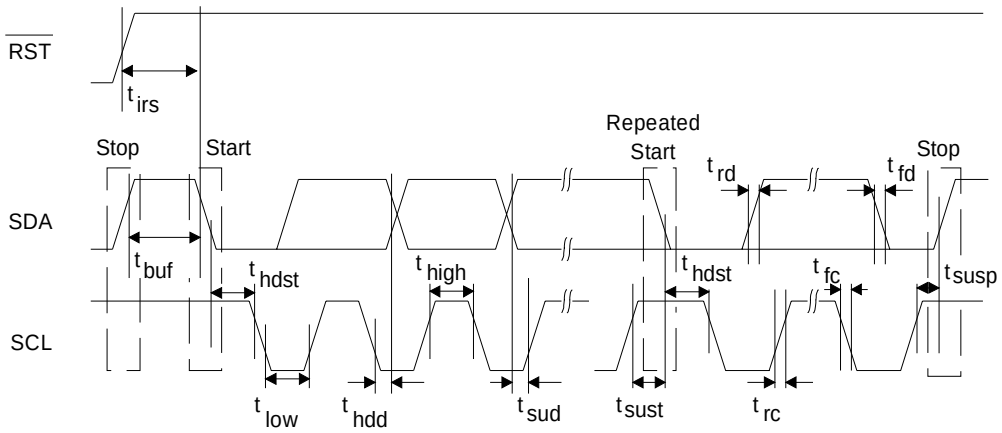


Figure 3. I^2C Control Port Timing

2. TYPICAL CONNECTION DIAGRAM — CS4223

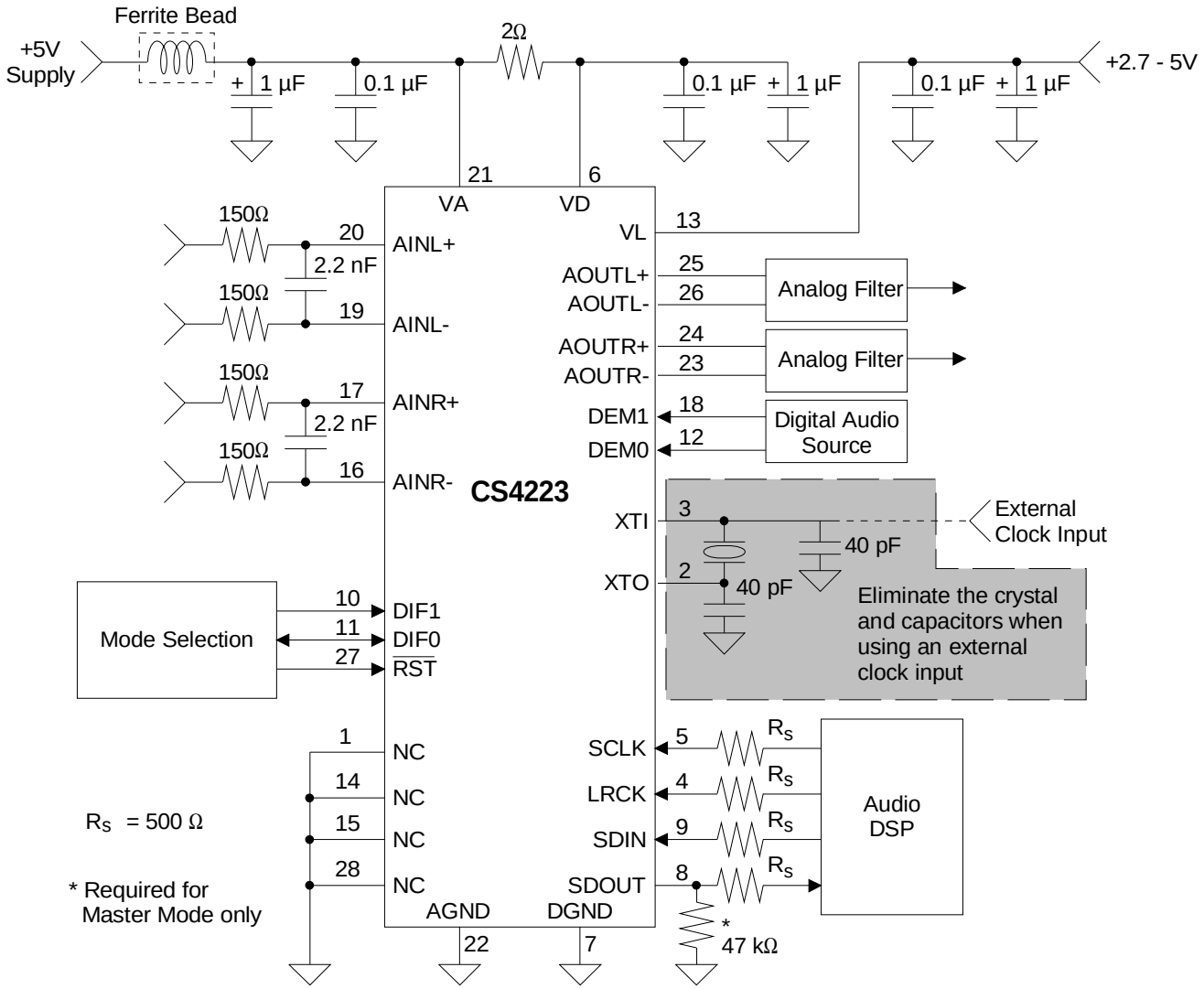


Figure 4. CS4223 Recommended Connection Diagram
(Also see *Recommended Layout Diagram*)

3. TYPICAL CONNECTION DIAGRAM — CS4224

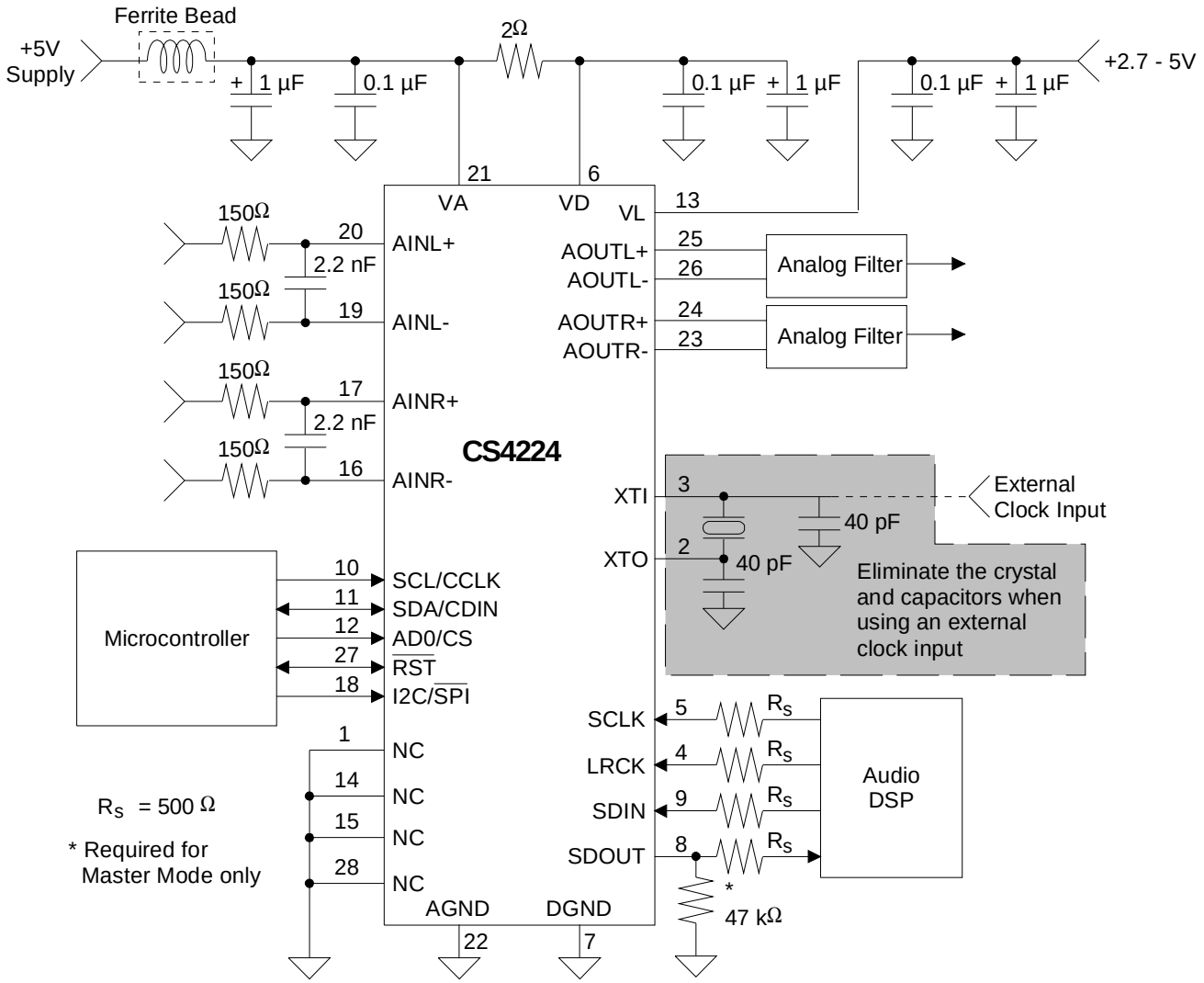


Figure 5. CS4224 Recommended Connection Diagram
(Also see *Recommended Layout Diagram*)

4. REGISTER QUICK REFERENCE - CS4224

Addr	Function	7	6	5	4	3	2	1	0
0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
1h	ADC Control	PDN	HPDR	HPDL	ADMR	ADML	CAL	CALP	CLKE
	default	0	0	0	0	0	0	0	0
2h	DAC Control	Reserved	MUTC	MUTR	MUTL	SOFT	Reserved	RMP1	RMP0
	default	0	0	0	0	0	0	0	0
3h-4h	Output Attenuator Level	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
	default	0	0	0	0	0	0	0	0
5h	DSP Port Mode	Reserved	DEM1	DEM0	DSCK	DOF1	DOF0	DIF1	DIF0
	default	0	0	0	0	0	0	0	0
6h	Converter Status Report	ACCR	ACCL	LVR2	LVR1	LVR0	LVL2	LVL1	LVL0
	default	0	0	0	0	0	0	0	0
7h	Master Clock Control	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCK1	MCK0
	default	0	0	0	0	0	0	0	0

5. REGISTER DESCRIPTIONS - CS4224

Note: All registers are read/write in I^2C mode and write-only in SPI mode, unless otherwise noted.

5.1 ADC Control (address 01h)

7	6	5	4	3	2	1	0
PDN	HPDR	HPDL	ADMR	ADML	CAL	CALP	CLKE
0	0	0	0	0	0	0	0

5.1.1 POWER DOWN ADC (PDN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The ADC will enter a low-power state when this function is enabled.

5.1.2 LEFT AND RIGHT CHANNEL HIGH PASS FILTER DEFEAT (HPDR-HPDL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The internal high-pass filter is defeated when this function is enabled. Control of the internal high-pass filter is independent for the left and right channel.

5.1.3 LEFT AND RIGHT CHANNEL ADC MUTING (ADMR-ADML)

Default = 0
0 - Disabled
1 - Enabled

Function:

The output for the selected ADC channel will be muted when this function is enabled.

5.1.4 CALIBRATION CONTROL (CAL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The device will automatically perform an offset calibration when brought out of reset, which last approximately 50 ms. When this function is enabled, a rising edge on the reset line will initiate an offset calibration.

5.1.5 CALIBRATION STATUS (CALP) (READ ONLY)

Default = 0
0 - Calibration done
1 - Calibration in progress

5.1.6 CLOCKING ERROR (CLKE) (READ ONLY)

Default = 0
0 - No error
1 - Error

5.2 DAC Control (address 02h)

7	6	5	4	3	2	1	0
Reserved	MUTC	MUTR	MUTL	SOFT	Reserved	RMP1	RMP0
0	0	0	0	0	0	0	0

5.2.1 MUTE ON CONSECUTIVE ZEROS (MUTC)

Default = 0
0 - Disabled
1 - Enabled

Function:

The DAC output will mute following the reception of 512 consecutive audio samples of static 0 or -1 when this function is enabled. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The muting function is affected, similar to volume control changes, by the SOFT bit in the DAC Control register.

5.2.2 MUTE CONTROL (MUTR-MUTL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The output for the selected DAC channel will be muted when this function is enabled. The muting function is affected, similar to volume control changes, by the SOFT bit in the DAC Control register.

5.2.3 SOFT RAMP CONTROL (SOFT)

Default = 0
0 - Soft Ramp level changes
1 - Zero Cross level changes

Function:

Soft Ramp level changes will be implemented by incrementally ramping, in 0.5 dB steps, from the current level to the new level. The rate of change defaults to 0.5 dB per 8 left/right clock periods and is adjustable through the RMP bits in the DAC Control register.

Zero Cross level changes will be implemented in a single step from the current level to the new level. The level change takes effect on a zero crossing to minimize audible artifacts. If the signal does not encounter a zero crossing, the level change will occur after a timeout period of 512 sample periods (10.7 ms at 48 kHz sample rate). Zero crossing is independently monitored and implemented for each channel. The ACCR and ACCL bits in the Converter Status Report register indicate when a level change has occurred for the right and left channel.

5.2.4 SOFT RAMP STEP RATE (RMP)

Default = 00
00 - 1 step per 8 LRCK's
01 - 1 step per 4 LRCK's
10 - 1 step per 16 LRCK's
11 - 1 step per 32 LRCK's

Function:

The rate of change for the Soft Ramp function is adjustable through the RMP bits.

5.3 Left Channel Output Attenuator Level (address 03h)

5.4 Right Channel Output Attenuator Level (address 04h)

7	6	5	4	3	2	1	0
ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0	0	0	0	0	0	0	0

5.4.1 ATTENUATION LEVEL (ATT7-ATT0)

Default = 00h

Function:

The Output Attenuator Level registers allow for attenuation of the DAC outputs in 0.5 dB increments from 0 to 113.5 dB. Level changes are implemented with an analog volume control until the residual output noise is equal to the noise floor in the mute state. At this point, volume changes are performed digitally. This technique is superior to purely digital volume control because the noise is attenuated by the same amount as the signal, thus preserving dynamic range, see Figure 16. Volume changes are performed as dictated by the SOFT bit in the DAC Control register. ATT0 represents 0.5 dB of attenuation and settings greater than 227 (decimal value) will mute the selected DAC output.

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
11100011	227	-113.5 dB
11100100	228	Muted

Table 1. Example Volume Settings

5.5 DSP Port Mode (address 05h)

7	6	5	4	3	2	1	0
Reserved	DEM1	DEM0	DSCK	DOF1	DOF0	DIF1	DIF0
0	0	0	0	0	0	0	0

5.5.1 DE-EMPHASIS CONTROL (DEM)

Default = 00
00 - 44.1 kHz de-emphasis setting
01 - 48 kHz de-emphasis setting
10 - 32 kHz de-emphasis setting
11 - De-emphasis disabled

Function:

Selects the appropriate digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates, see Figure 15.

5.5.2 SERIAL INPUT/OUTPUT DATA SCLK POLARITY SELECT (DSCK)

Default = 0
0 - Data valid on rising edge of SCLK
1 - Data valid on falling edge of SCLK

Function:

This function selects the polarity of the SCLK edge used to clock data in and out of the serial audio port.

5.5.3 SERIAL DATA OUTPUT FORMAT (DOF)

Default = 00
00 - I^2S compatible
01 - Left justified
10 - Right justified, 24-bit
11 - Right justified, 20-bit

Function:

The required relationship between the left/right clock, serial clock and output serial data is defined by the Serial Data Output Format, and the options are detailed in Figures 8-11.

Note: If the format selected is Right-Justified, SCLK must be 64 Fs when operating in slave mode.

5.5.4 SERIAL DATA INPUT FORMAT (DIF)

Default = 00
00 - I^2S compatible
01 - Left justified
10 - Right justified, 24-bit
11- Right justified, 20-bit

Function:

The required relationship between the left/right clock, serial clock and input serial data is defined by the Serial Data Input Format, and the options are detailed in Figures 8-11.

5.6 Converter Status Report (Read Only) (address 06h)

7	6	5	4	3	2	1	0
ACCR	ACCL	LVR2	LVR1	LVR0	LVL2	LVL2	LVL0
0	0	0	0	0	0	0	0

5.6.1 LEFT AND RIGHT CHANNEL ACCEPTANCE BIT (ACCR-ACCL)

Default = 0
0 - Requested setting valid
1 - New setting loaded

Function:

The ACCR and ACCL bits indicate when a change in the Output Attenuator Level has occurred for the left and right channels, respectively. The value will be high when a new setting is loaded into the Output Attenuator Level registers. The value will return low when the requested attenuation setting has taken effect.

5.6.2 LEFT AND RIGHT CHANNEL ADC OUTPUT LEVEL (LVR AND LVL)

Default = 000
000 - Normal output levels
001 - -6 dB level
010 - -5 dB level
011 - -4 dB level
100 - -3 dB level
101 - -2 dB level
110 - -1 dB level
111 - Clipping

Function:

The analog-to-digital converter is continually monitoring the peak digital signal output for both the left and right channel, prior to the digital limiter. The maximum output value is stored in the LVL and LVR bits. The LVL and LVR bits are ‘sticky’, so they are reset after each read is performed.

5.7 Master Clock Control (address 07h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCK1	MCK0
0	0	0	0	0	0	0	0

5.7.1 MASTER CLOCK CONTROL (MCK)

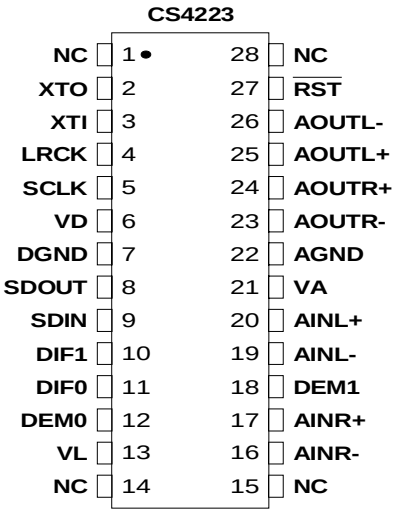
Default = 00
00 - XTI = 256 Fs for Master Mode
01 - XTI = 384 Fs for Master Mode
10 - XTI = 512 Fs for Master Mode

Function:

The MCK bits allow for control of the Master Clock, XTI, input frequency.

Note: These bits are not valid when operating in slave mode.

6. PIN DESCRIPTIONS — CS4223



NC	1,14,15, 28	**No Connect -** These pins are not connected internally and should be tied to DGND to minimize noise coupling.
XTI, XTO	2,3	**Crystal Connections (*Input/Output*) -** Input and output connections for the crystal used to clock the CS4223. Alternatively, a clock may be input into XTI. This is the clock source for the delta-sigma modulator and digital filters. The frequency of this clock must be either 256x, 384x, or 512x Fs in Slave Mode and 256x in Master Mode.

Fs (kHz)	XTI (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 2. Common Clock Frequencies

LRCK	4	**Left/Right Clock (*Input*) -** Determines which channel is currently being input/output of the serial audio data pins SDIN/SDOUT. The frequency of the Left/Right clock must be equal to the input sample rate. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.
SCLK	5	**Serial Data Clock (*Input*) -** Clocks the individual bits of the serial data into the SDIN pin and out of the SDOUT pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.
VD	6	**Digital Power (*Input*) -** Positive power supply for the digital section. Typically 5.0 VDC.
DGND	7	**Digital Ground (*Input*) -** Digital ground for the digital section.
SDOUT	8	**Serial Data Output (*Output*) -** Two's complement MSB-first serial data is output on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.

SDIN	9	**Serial Data Input (*Input*) -** Two's complement MSB-first serial data is input on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.
DIF0, DIF1	10,11	**Digital Interface Format (*Input*) -** The required relationship between the left/right clock, serial clock and serial data is defined by the Digital Interface Format. The options are detailed in Figures 8 - 11.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	I^2S, up to 24-bit data	0	8
0	1	Left Justified, up to 24-bit data	1	9
1	0	Right Justified, 24-bit Data	2	10
1	1	Right Justified, 20-bit Data	3	11

Table 3. Digital Interface Format - DIF1 and DIF0

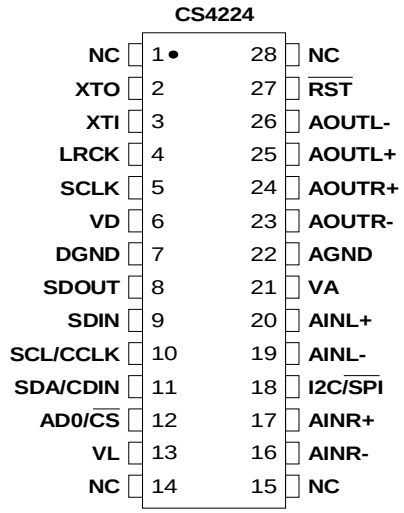
DEM0, DEM1	12,18	**De-Emphasis Select (*Input*) -** Controls the activation of the standard 50/15 µs de-emphasis filter. 32, 44.1, or 48 kHz sample rate selection defined in Table 4.

DEM0	DEM1	De-Emphasis
0	0	32 kHz
0	1	44.1 kHz
1	0	48 kHz
1	1	Disabled

Table 4. De-emphasis Control

VL	13	**Digital Logic Power (*Input*) -** Positive power supply for the digital interface section. Typically 3.0 to 5.0 VDC.
AINR-, AINR+	16,17	**Differential Right Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
AINL-, AINL+	19,20	**Differential Left Channel Analog Input (*Input*)** - The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
VA	21	**Analog Power (*Input*) -** Positive power supply for the analog section. Nominally +5 Volts.
AGND	22	**Analog Ground (*Input*) -** Analog ground reference.
AOUTR-, AOUTR+	23, 24	**Differential Right Channel Analog Output (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
AOUTL-, AOUTL+	25, 26	**Differential Left Channel Analog Output (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
$\overline{\text{RST}}$	27	**Reset (*Input*)** - When low, the device enters a low power mode and all internal registers are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

7. PIN DESCRIPTIONS — CS4224



NC	1,14,15, 28	**No Connect -** These pins are not connected internally and should be tied to DGND to minimize noise coupling.
XTI, XTO	2,3	**Crystal Connections (*Input/Output*) -** Input and output connections for the crystal used to clock the CS4224. Alternatively a clock may be input into XTI. This is the clock source for the delta-sigma modulator and digital filters. The frequency of this clock must be either 256x, 384x, or 512x Fs. The default XTI setting in Master Mode is 256x, but this may be changed to 384x or 512x through the Control Port.

Fs (kHz)	XTI (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 5. Common Clock Frequencies

LRCK	4	**Left/Right Clock (*Input*) -** Determines which channel is currently being input/output of the serial audio data pins SDIN/SDOUT. The frequency of the Left/Right clock must be equal to the input sample rate. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
SCLK	5	**Serial Data Clock (*Input*) -** Clocks the individual bits of the serial data into the SDIN pin and out of the SDOUT pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
VD	6	**Digital Power (*Input*) -** Positive power supply for the digital section. Typically 5.0 VDC.
DGND	7	**Digital Ground (*Input*) -** Digital ground for the digital section.

SDOUT	8	**Serial Data Output (*Output*) -** Two's complement MSB-first serial data is output on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
SDIN	9	**Serial Data Input (*Input*) -** Two's complement MSB-first serial data is input on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
SCL/CCLK	10	**Serial Control Port Clock (*Input*) -** Clocks the serial control bits into and out of the CS4224. In I^2C mode, SCL requires an external pull-up resistor according to the I^2C specification.
SDA/CDIN	11	**Serial Control Port Data (*Input/Output*)-** SDA is a data I/O line in I^2C mode and requires an external pull-up resistor according to the I^2C specification. CDIN in the input data line for the serial control port in SPI mode.
AD0/$\overline{\text{CS}}$	12	**Address Bit/Control Chip Select (*Input*) -** In I^2C mode, AD0 is a chip address bit. In SPI mode, $\overline{\text{CS}}$ is used to enable the control port interface on the CS4224. The CS4224 control port interface is defined by the $\overline{\text{SPI}}$/I2C pin.
VL	13	**Logic Power (*Input*) -** Positive power supply for the digital interface section. Typically 3.0 to 5.0 VDC.
AINR-, AINR+	16,17	**Differential Right Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
I2C/$\overline{\text{SPI}}$	18	**Control Port Format (*Input*)** - When this pin is high, I^2C mode is selected, when low, $\overline{\text{SPI}}$ is selected.
AINL-, AINL+	19,20	**Differential Left Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
VA	21	**Analog Power (*Input*) -** Positive power supply for the analog section. Typically 5.0 VDC.
AGND	22	**Analog Ground (*Input*) -** Analog ground reference.
AOUTR-, AOUTR+	23, 24	**Differential Right Channel Analog Outputs (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
AOUTL-, AOUTL+	25, 26	**Differential Left Channel Analog Outputs (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
$\overline{\text{RST}}$	27	**Reset (*Input*)** - When low, the device enters a low power mode and all internal registers are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

8. APPLICATIONS

8.1 Overview

The CS4223 is a stand-alone device controlled through dedicated pins. The CS4224 is controlled with an external microcontroller using the serial control port.

8.2 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4223/4 requires careful attention to power supply and grounding arrangements to optimize performance. Figures 4 and 5 shows the recommended power arrangement with VA, VD and VL connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be used on each supply pin.

8.3 High Pass Filter

The operational amplifiers in the input circuitry driving the CS4223/4 may generate a small DC offset into the A/D converter. The CS4223/4 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

8.4 Analog Outputs

The recommended off-chip analog filter is either a 2nd order Butterworth or a 3rd order Butterworth, if greater out-of-band noise filtering is desired. The CS4223/4 DAC interpolation filter has been precompensated for an external 2nd order Butterworth filter with a 3 dB corner at Fs, or a 3rd order Butterworth filter with a 3 dB corner at 0.75 Fs to provide a flat frequency response and linear phase over the passband (see Figure 14 for Fs = 48 kHz). If the recommended filter is not used, small frequency response magnitude and phase errors will occur. In addition to providing out-of-band noise attenuation, the output filters shown in Figure 14 provide differential to single-ended conversion.

8.5 Master vs. Slave Mode

The CS4223/4 may be operated in either master mode or slave mode. In master mode, SCLK and LRCK are outputs which are internally derived from MCLK. The device will operate in master mode when a 47 kΩ pulldown resistor is present on SDOUT at startup or after reset, see Figure 5. LRCK and SCLK are inputs to the CS4223/4 when operating in slave mode. See Figures 8-11 for the available clocking modes.

8.6 De-emphasis

The CS4223/4 includes digital de-emphasis for 32, 44.1, or 48 kHz sample rates. The frequency response of the de-emphasis curve, as shown in Figure 15, will scale proportionally with changes in samples rate, Fs. The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis as a means of noise reduction.

De-emphasis control is achieved with the DEM1/0 pins on the CS4223 or through the DEM1-0 bits in the DSP Port Mode Byte (#5) on the CS4224.

8.7 Power-up / Reset / Power Down Calibration

Upon power up, the user should hold $\overline{RST}$ = 0 for approximately 10 ms. In this state, the control port is reset to its default settings and the part remains in the power down mode. At the end of $\overline{RST}$, the device performs an offset calibration which lasts approximately 50 ms after which the device enters normal operation. In the CS4224, a calibration may also be initiated via the CAL bit in the ADC Control Byte (#1). The CALP bit in the ADC Control Byte is a read only bit indicating the status of the calibration.

Reset/Power Down is achieved by lowering the $\overline{RST}$ pin causing the part to enter power down.

Once $\overline{RST}$ goes high, the control port is functional and the desired settings should be loaded.

The CS4223/4 will also enter power down mode if the master clock source stops for approximately 10 µs or if the LRCK is not synchronous to the master clock. The control port will retain its current settings.

The CS4223/4 will mute the analog outputs and enter the power down mode if the supply drops below approximately 4 volts.

8.8 Control Port Interface (CS4224 only)

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI® and I^2C®, with the CS4224 operating as a slave device. The control port interface format is selected by the $\overline{SPI}$/I2C pin.

8.8.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS4224 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 6 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. Register reading from the CS4224 is not supported in the SPI mode. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into a register designated by the MAP.

The CS4224 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for successive writes. If INCR is set to a 1, then MAP will auto increment after each byte is written, allowing block writes of successive registers. Register reading from the CS4224 is not supported in the SPI mode.

8.8.2 I^2C Mode

In I^2C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 7. There is no $\overline{CS}$ pin. Pin AD0 forms the partial chip address and should be tied to VD or DGND as desired. The upper 6 bits of the 7 bit address field must be 001000. In order to communicate with the CS4224, the LSB of the chip address field (first byte sent to the CS4224) should match the setting of the AD0 pin. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

8.9 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	Reserved	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

8.9.1 AUTO-INCREMENT CONTROL (INCR)

Default = 0
0 - Disabled
1 - Enabled

8.9.2 REGISTER POINTER (MAP)

Default = 000

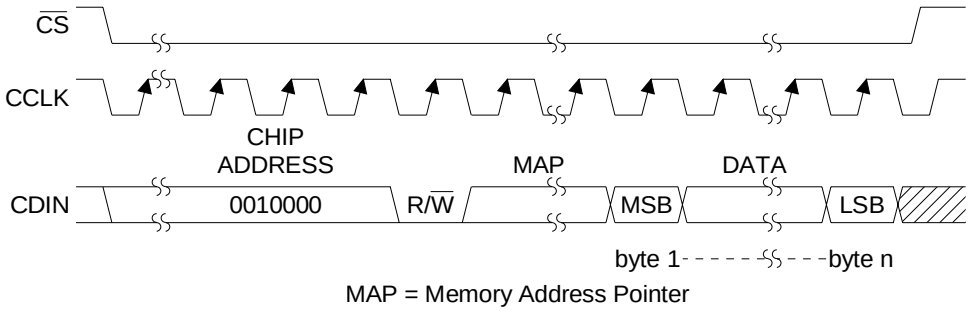


Figure 6. Control Port Timing, SPI mode

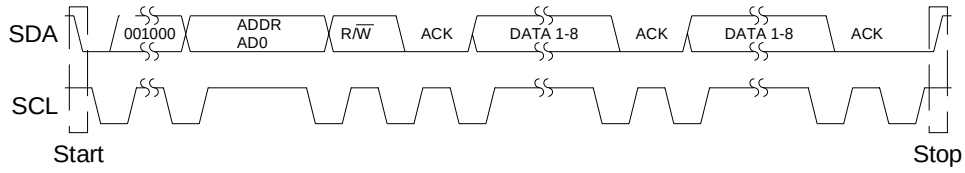
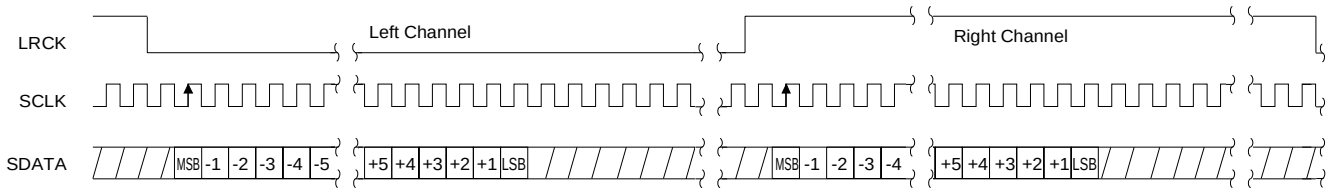
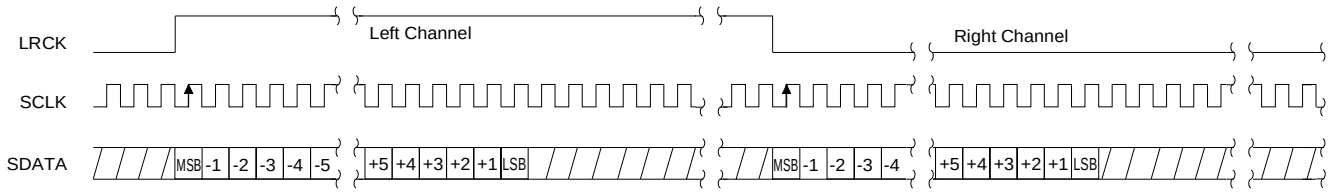


Figure 7. Control Port Timing, I^2C mode



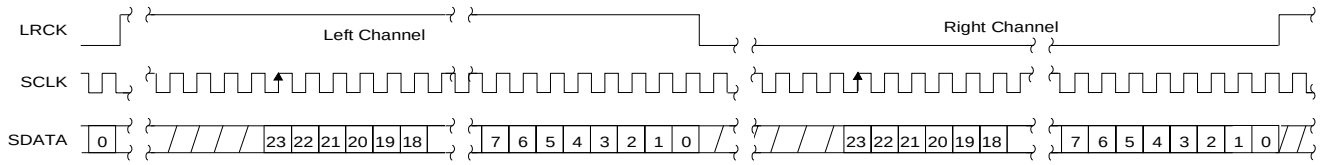
Master	Slave
I^2S, up to 24-bit data XTI=256, 384, 512 Fs (CS4223-256Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	I^2S, up to 24-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 48,64, 128 Fs

Figure 8. Serial Audio Format 0 (I^2S)



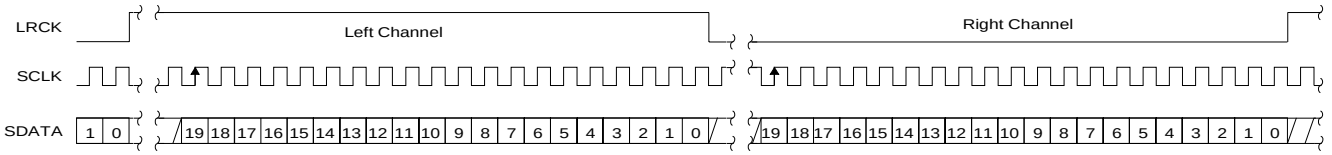
Master	Slave
Left-justified, up to 24-bit data XTI=256, 384, 512 Fs (CS4223-256Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	Left-justified, up to 24-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 48, 64, 128 Fs

Figure 9. Serial Audio Format 1



Master	Slave
Right-justified, 24-bit data XTI=256, 384, 512 Fs (CS4223-256Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	Right-justified, 24-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 64 Fs

Figure 10. Serial Audio Format 2



Master	Slave
Right-justified, 20-bit data XTI=256, 384, 512Fs (CS4223-256Fsonly) LRCK = 4 to 50 kHz SCLK = 64 Fs	Right-justified, 20-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 64 Fs

Figure 11. Serial Audio Format 3

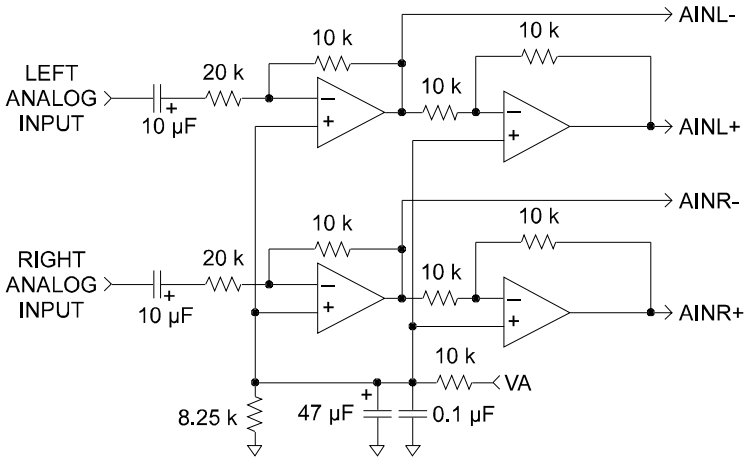


Figure 12. Optional Input Buffer

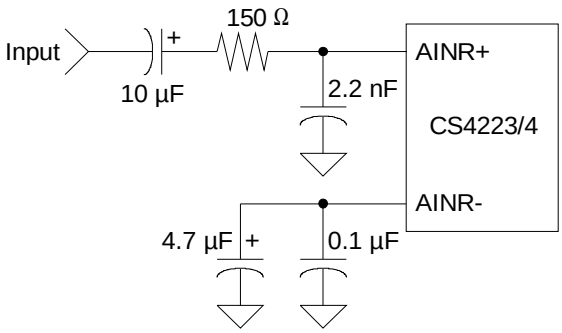
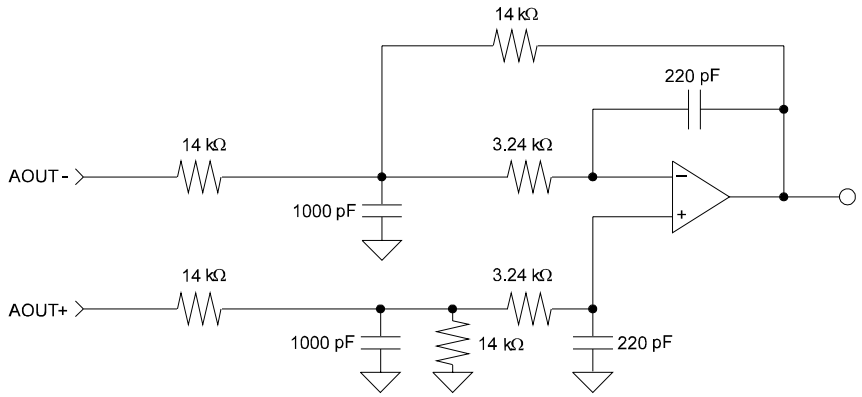
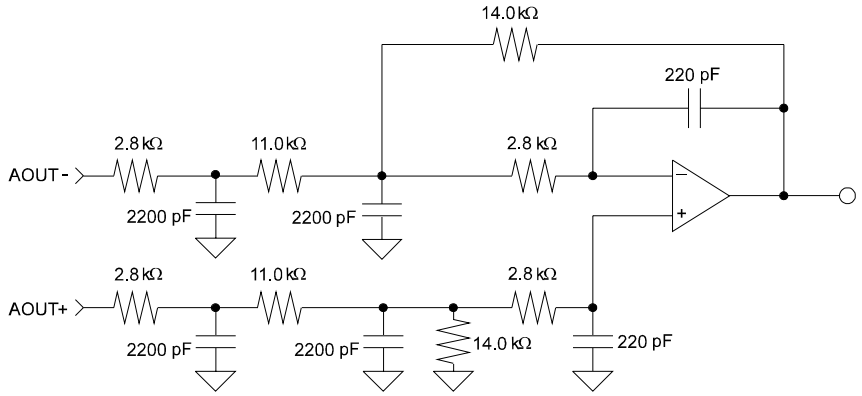


Figure 13. Single-ended Input Application



2-pole Butterworth Filter



3-pole Butterworth Filter

Figure 14. 2- and 3-Pole Butterworth Filters

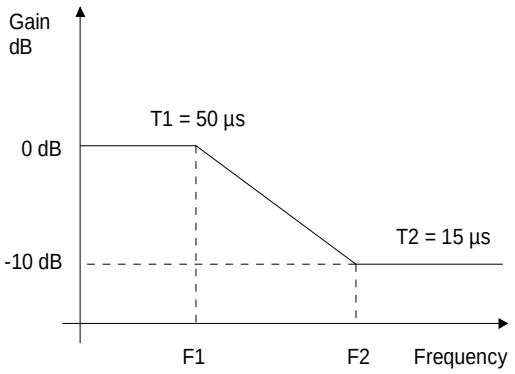


Figure 15. De-emphasis Curve

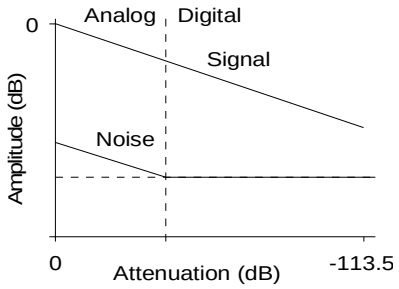


Figure 16. Hybrid Analog/Digital Attenuation

9. ADC/DAC FILTER RESPONSE

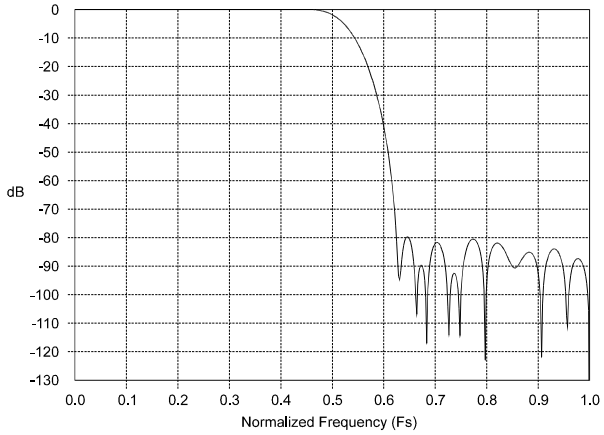


Figure 17. ADC Filter Response

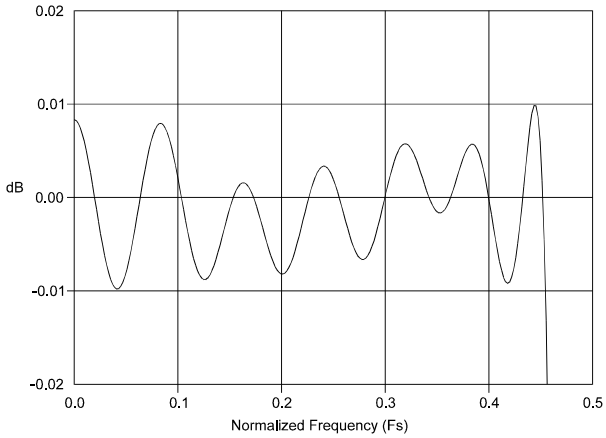


Figure 18. ADC Passband Ripple

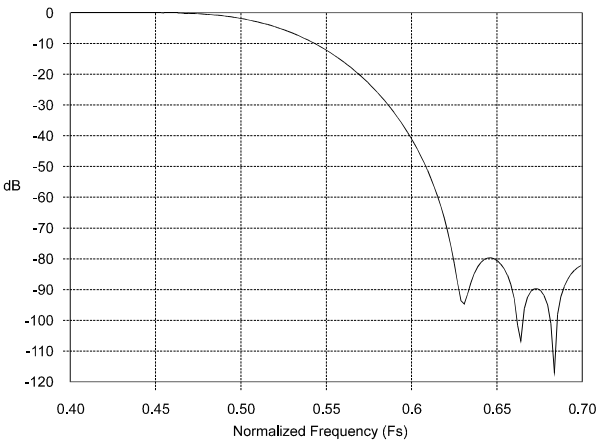


Figure 19. ADC Transition Band

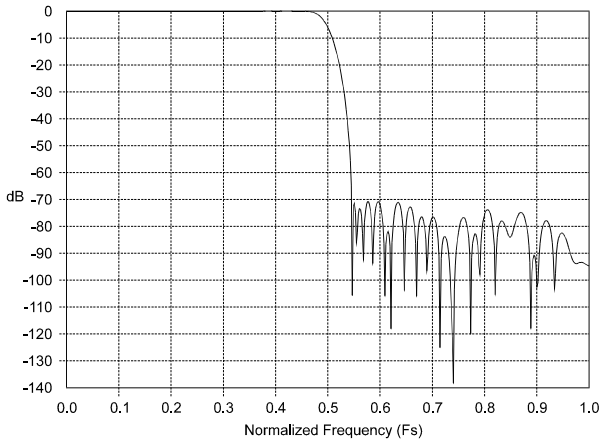


Figure 20. DAC Filter Response

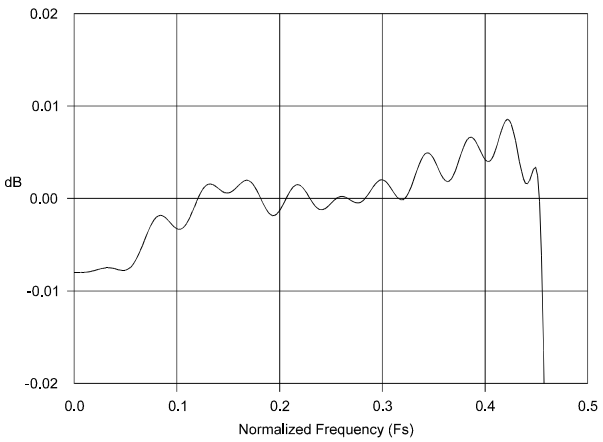


Figure 21. DAC Passband Ripple

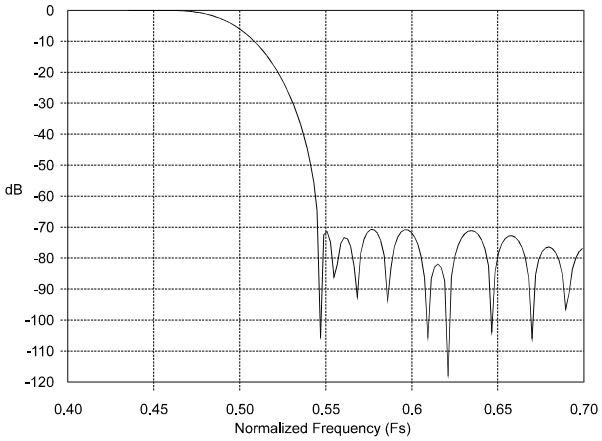


Figure 22. DAC Transition Band

10. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1 dBFS as suggested in AES17-1991 Annex A and DACs are measured at 0 dBFS.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the rms analog output level with 1 kHz full scale digital input to the rms analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal. Units in decibels.

Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 20 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

Gain Error

The deviation from the nominal full scale output for a full scale input.

Gain Drift

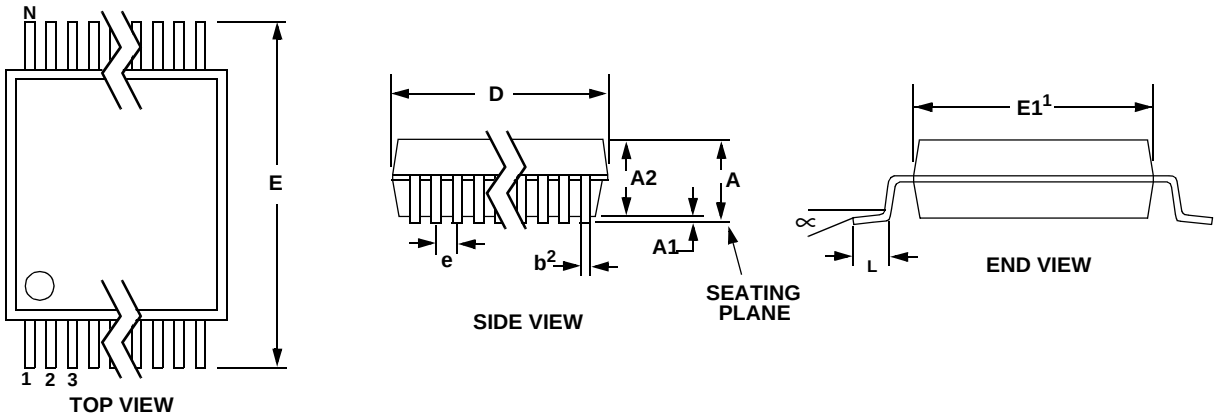
The change in gain value with temperature. Units in ppm/°C.

Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected inputs tied to a common potential. For the DAC's, the differential output voltage with mid-scale input code. Units are in volts.

11. PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.15	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

• Notes •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Since the printing of the original manual for the CD-RW2000, the following software features have been added to the latest internal software version (Front panel v3.00/ Converter v3.00).

Please take note of these new features, which we hope will be useful to you in your work, and keep this sheet with the manual for future reference.

1 International Standard Recording Code (ISRC)

If you press the **FINALIZE** key during playback, the unit now shows the ISRC data of the track currently being played back. If there is no ISRC data on the track, the unit indicateos NO ISRC DATA.

NOTE

It takes about two seconds from the start of the track to read the ISRC correctly. If you press the **FINALIZE** *key before the ISRC reading is complete, the unit shows* NO ISRC DATA *even if ISRC data is present on the track.*

2 Recorder Identification Code (RID)

When you press the **ERASE** key during playback, the unit now shows the RID data of the track currently being played back. If the track does not contain RID data, the unit indicates NO RID DATA.

NOTE

It takes about two seconds from the start of the track to read the RID correctly. If you press the **ERASE** *key before the RID reading is complete, the unit shows* NO RID DATA*, even if RID data is present on the track.*

3 Manual index increment

While the CD-RW2000 is recording, the track index can be incremented manually by pressing the **CALL** key.

4 Index increment mode

A new menu item: IndexInc>XXX has been added.

When this is enabled (set to On), and the unit is in stop, record or record pause mode, automatic index incrementing is enabled. The index number is displayed to the right of the track number in the display.

When this function is enabled, any source signals (whether audio trigger level signals or sub-Q signals, etc.) which would usually trigger a track increment now trigger an index increment.

This can be useful if more than 99 different sections are to be recorded on one disc.

NOTE

Stopping or pausing recording will cause the track number (not the index number) to be incremented. For this reason, it is advisable to edit material in advance so that material to be placed in one track for continuous playback is all together.

Changes to data format (e.g. changes in emphasis status, etc.) will also cause the track number to be incremented.

Also note that even if a track boundary is detected through a digital input, while this index mode is enabled, the index, not the track will be incremented.

The CD-RW2000 is not able to perform index searching when playing back discs.

5 New signal level setting

There is a new setting for the signal level (trigger level): MIN L. See 4.3.1, “Synchronized recording” in the manual.

This setting is used with digital sources, and it corresponds to any digital source whose audio data value is not 0 (in other words, when a signal is present).

This is useful when recording from digital sources to start recording at the exact moment when the actual source starts.

NOTE

When this setting is made, all signals received through the digital inputs with a digital audio value of 1 or over are recognized as valid sounds. Any signals from the analog inputs passed through the AD convertors are also recognized as valid sounds.

6 Indicating and changing the TRIM value

The trim values, used in synchronized recording and track division (4.5, “Rehearsal” in the manual) can now be viewed and set independently outside the rehearsal modes using two new menus.

Previously these two values were identical, and could only be set in rehearsal mode.

These menu items are `Sync_TXXXXf` and `Inc_TXXXXf`.

The maximum and values for these parameters remain the same as previously (±125 frames on either side of the original point, at 75 frames/second).

7 Meter peak hold time

A new menu item has been added to allow the meter peak hold time to a chosen value. Previously this was preset to 1.2 seconds and could not be changed.

The new menu allows peak hold settings of between 0.0 seconds and 2.5 seconds. There is also a `HOLD` setting, where peak readings are displayed and held until the **MULTI DIAL** control is pressed or the **ENTER** key of the remote control unit is pressed.

8 New media types

The TASCAM CD-RW2000 now supports High Speed CD-RW (4x to 10x) in addition to Multi Speed CD-RW (1x to 4x) media.

9 Finalization and erase times

The time taken to perform finalization and erase operations depends on the media used, as listed here:

• Finalization:

CD-R media	8x
Multi Speed CD-RW	4x
High Speed CD-RW	8x

• Erasing discs:

Multi Speed CD-RW	4x
High Speed CD-RW	8x

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TEAC **TECHNICAL INFORMATION**

TASCAM CD-RW2000, Phase Difference on Analog In/Out

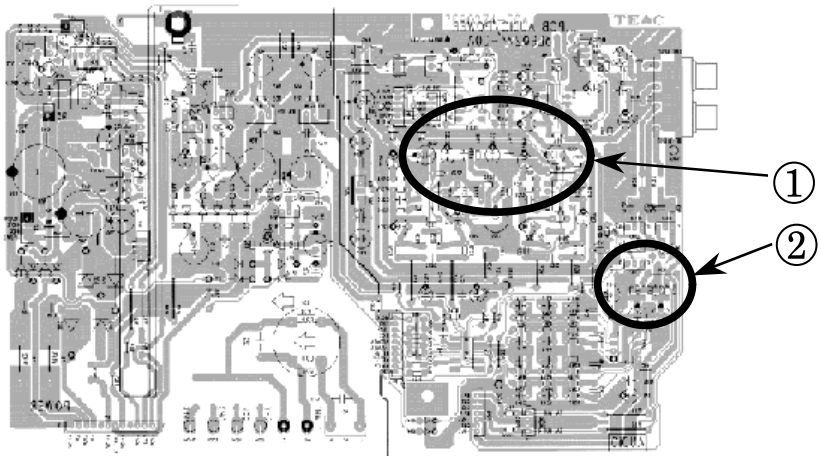
No. **0102**
DATE 15th March 2001

U122 (CRYSTAL CS4223, audio codec) on the Audio/Power PCB Assy has a native phase difference between L and R by one sample.

* No problem on digital in/out.
* No problem through AD-DA overall operation.
* No problem with a CD-R/RW media recorded by the CD-RW700 or the RW-800.

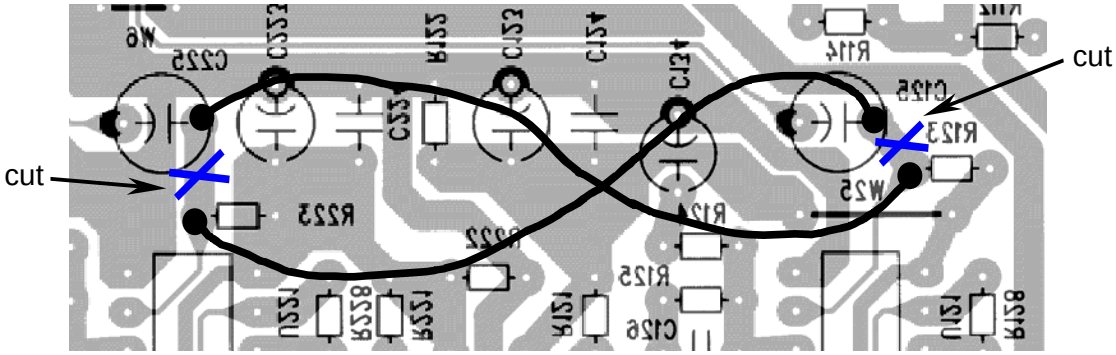
To correct the phase difference, change in the following pages has been made on the products with S/No. 0080001 and higher.

AUDIO/POWER PCB Assy (Bottom Side)



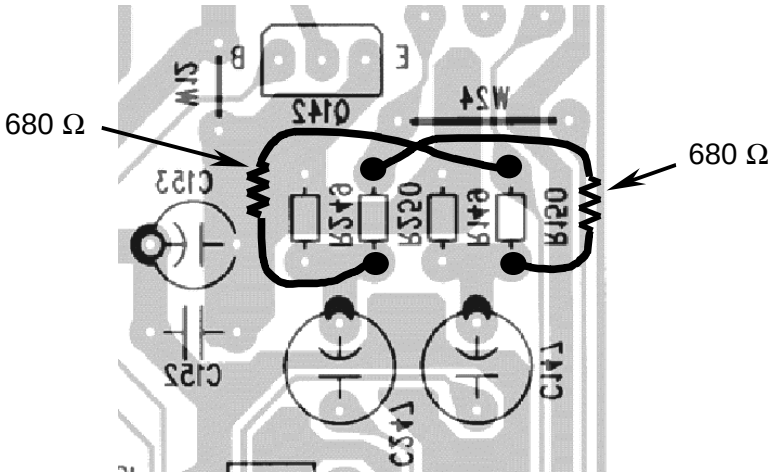
Note: ① and ② circled above correspond to enlarged drawings below.

①
- Cut foil pattern at two spots.
- Add 2 pcs of jumper wires.

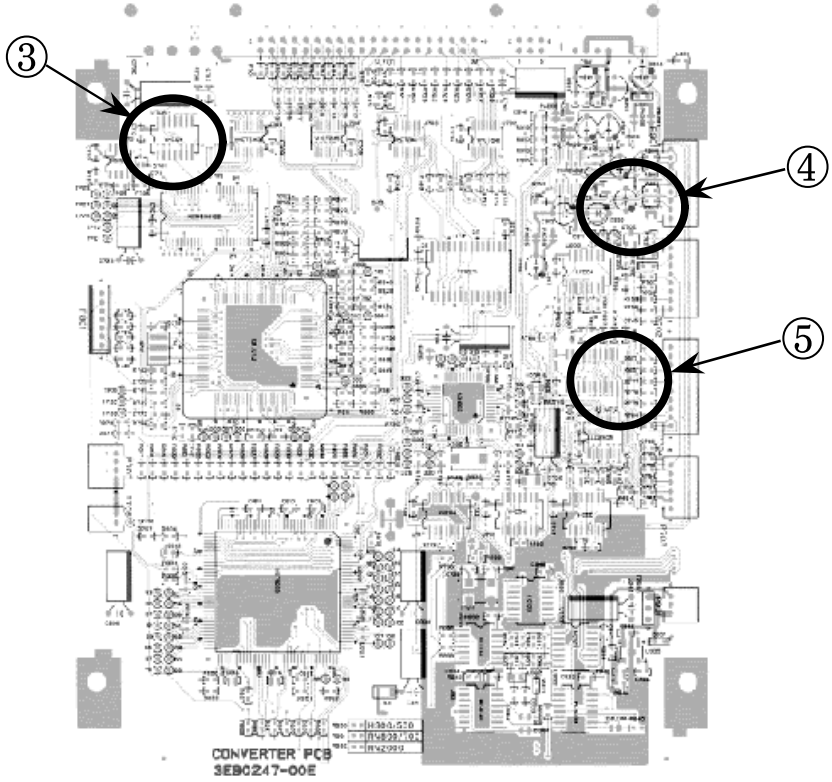


②
- Remove R150 and R250 (680 Ω).
- Mount 2 pcs of 680 Ω resistor as shown below.

  Note: Original R150/R250 are 680 Ω. Then they can be re-used but lead wire may be short requiring extension with additional wires.

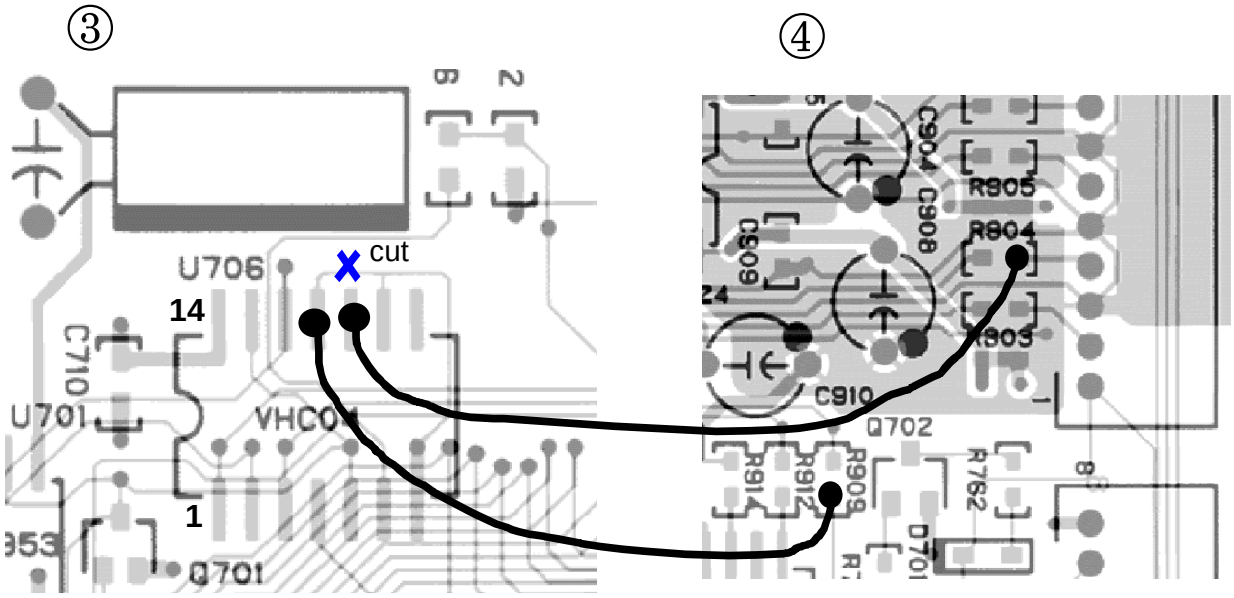


CONVERTER PCB Assy (Top Side)



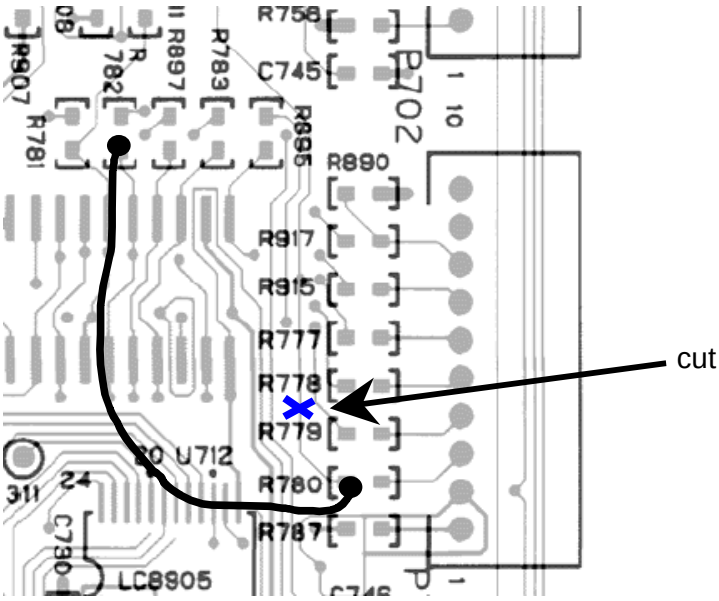
Note: ③, ④ and ⑤ circled above correspond to enlarged drawings in the following pages.

- Cut foil patter between U706-11 and GND.
- Cut foil patter between U706-11 and GND.
- Add a jumper wire between U706-10 and R904.
- Add a jumper wire between U706-11 and R909.



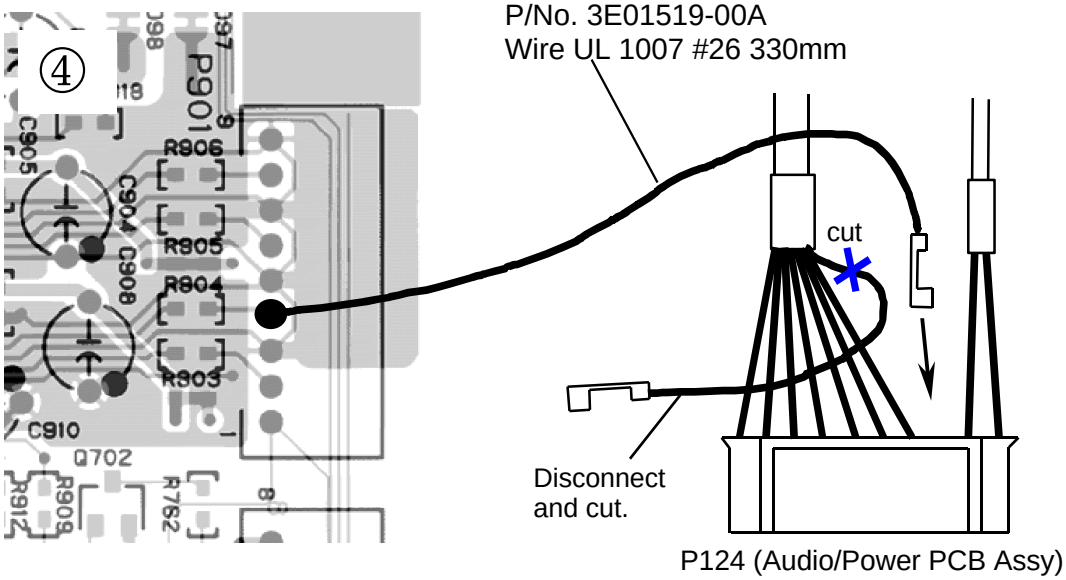
- Cut foil pattern between R780 and through hole.
- Add a jumper wire between R782 and R780.

⑤



- Disconnect and cut a wire of P124-3 (brown) on the Audio/Power PCB Assy.
- Insert a new wire to vacant pin 3.
  New wire: P/No. 3E01519-00A
  Wire UL 1007 #26 330mm BRW
- Solder the other end of the new wire to P901-4 (through hole) on the CONVERTER PCB Assy.
- Insert the P124 to original position.

④



TEAC

TECHNICAL INFORMATION

CD-RW2000V3, Service Manual Supplement Correction

No. **0705**
DATE 20th March 2007

Correction is required on the service manual as shown below.

CD-RW2000V3, page 1 at right column of the parts list

Ref. No.	✕	○
1- 3	3E9527600A PCB ASSY, CONVERTER 2000V3	3E9524720B PCB ASSY, CONVERTER 2000V3
	3S0048510A UCOM Assy, HD64F7044 402V3IC U707 MPU	3S0048510B UCOM ASSY HD64F7044 402V3 U707 MPU

The service manual on the SVHP have been corrected on 14th/March/2007.

TEAC

TECHNICAL INFORMATION

No. **0701**

DATE 16th February 2007

CD-RW402(V3)/CD-RW2000(V3), Substitution of the Drive

This information relates to previous Tech-Info No. 0505R, 0506R, 0510 and 0511R.

The Drive (CD-W58DA) introduced in both info has been replaced with a RoHS conformity Drive (CD-W58DB) on the V3 products with the following S/Nos (month started production):

CD-RW402V3: S/N 0350001 and after (Nov/2005)
CD-RW2000V3: S/N 0500001 and after (Mar/2006)
Exception: T/C - S/N 0470076 to 047125 (Nov/2005)
All - S/N 0490116 to 049215 (Feb/2006)

Parts required

Item	Qty	P/No.	Description
New bare drive	1	V00141900A	CD-W58DB-T00 G
Drive update on CD-R			"W58db1td.abf" written
Drive update on Windows			"W58db1td.exe"

Visit the **ROM Data Library** on the SVHP to download the both firmware data and follow the update procedure on the previous Tech Info to read the following change:

"T58V1tf.abf" of CD-W58DA Drive => "W58db1td.abf" for CD-W58DB Drive.
"CDW58da1tf.exe" of CD-W58DA Drive => "W58db1td.exe" of CD-W58DB Drive.

Notice:

Do not attempt to write the former CD-W58DA firmware, "T58V1tf.abf" or "CDW58da1tf.exe" onto new CD-W58DB Drive otherwise new Drive becomes totally no response since type of Flash Rom fitted is quite different by the RoHS requirement. These firmware have no capability to identify type of Drive on which targeted to update therefore.

TEAC **TECHNICAL INFORMATION**

No. **0510**

TASCAM CD-RW2000V3, Converter MPU Upgrade

DATE 20th October 2005

ROM of the Converter MPU, U707 on the Converter PCB Assy has been upgraded from Ver 3.01 to Ver 3.02 on the products of S/N 0440001 and up.

Item	P/No.	Description
Converter MPU U707	3S0048510A (Ver3.01)	3S0048510B (Ver3.02)

Problem corrected by V3.02

1. "COPY RPOHIBIT" has been resulted at the first track of recorded CD even "COPY ID" was selected to "FREE" regardless of the input source.
2. LCD shows "NO DISC" when UNFINALIZE was operated against CD-RW media on that exactly 99 tracks have been recorded. Once open and close the Tray has been required to recover the 99 tracks read out.
3. "REC ERROR" has been occurred when a particular CD was tried to Copy from Drive 1.

Note: Drive firmware has been updated from Ver 1.TD to Ver 1.TF to solve the problems however updating the Converter firmware is recommended to be done at the same time for a future provision.

Converter MPU and Drive firmware update procedure

Prepare a "Converter update CD-R" that has "conv0302mot" written on it.
Prepare a "Drive update CD-R" that has "T58V1tf.abf" written on it.

Preparation:

1. Have two blank CD-R data discs available, as well as a system capable of creating data CDs.
2. Visit the **ROM Data Library** in the TASCAM Service HP website to download both firmware data images and write the firmware file on PC to the blank CD-R discs respectively. (Use the "Disc at once" method that complies with ISO9660 Level 1: MS-DOS compatible)

Notice:

Be careful that the power supply to the unit is not interrupted during the update process otherwise firmware data of the Converter MPU or the drive could be damaged and physical replacement of related part becomes unavoidable.

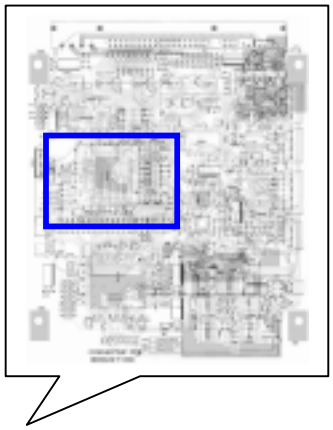
Converter MPU firmware update

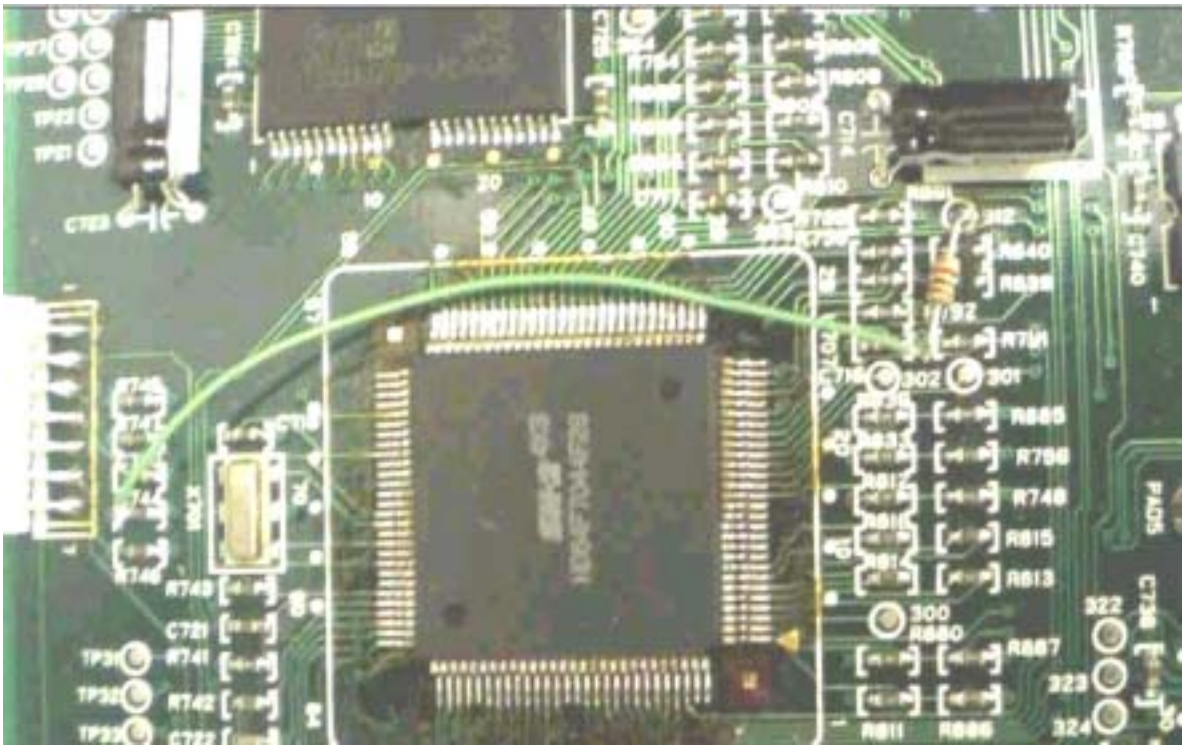
Procedure:

1. Turn on power of the unit while holding **CALL** and **MENU**.
2. Load the "Converter update CD-R" while display shows "RW2000 03.00" that is version of the Front MPU.
3. Confirm "CD" in display blinks. Then press **CALL** to check current version of drive. Existing version is "V1.TA", "V1.TB" (May/2005) and "V1.TD" as of August/2005.

4. Press **MENU** then the display shows current version and new version to be updated as "C03.0X→03.02".
5. Press **ENTER** then update will start.
6. Wait approximately 45 seconds or more to finish the update.
7. Turn off power of the unit.

A temporary work on the Converter PCB Assy to connect an oscilloscope is required to realize a successful completion. This is since the Converter PCB Assy of CD-RW2000V3 does not have necessary hardware to continue to show update sequence further. The waveform becomes Low when the **ENTER** key is pressed and goes to High approximately 45 seconds later upon end up the update as shown below:





The point to observe the waveform is a junction of additional 1kohm resistor and 60 mm wire that is connected across pin 30 (TP312) and pin 77 (R744) of the MPU (U707) as shown above.

Drive firmware update on CD-RW2000V3

1. Turn on power of the unit while holding **CALL** and **MENU**.
2. Load the "Drive update CD-R" while display shows "RW2000 03.00" that is version of the Front MPU.
3. Confirm "CD" in display blinks. Then press **CALL** to check current version of drive.
   Existing version is "V1.TA", "V1.TB" (May/2005) and "V1.TD" as of August/2005.
4. Press **MENU** then the display shows current version and new version to be updated as "D 1.TA→1.TF" for example.
5. Press **ENTER** then update will start.
   "NOW UPDATE" is displayed and "**.**" at the right most corner blinks.
6. "COMPLETE" appears to show end up of the update successfully.
7. Turn off power of the unit.

Drive firmware update on Windows

There is another way to update the drive firmware only by using PC.
Visit the **ROM Data Library** in the TASCAM Service HP website to download firmware data image of "CDW58DA_1TF.exe" into PC.

1. While PC is powered off, connect the CD-W58DA to PC and reboot.
   No need to consider Primary/Secondary and Master/Slave.
2. Double-click on "CDW58DA_1TF.exe" to run.
3. Follow the messages that will appear.

TECHNICAL INFORMATION

No. **0505R**

DATE 20th October 2005

TASCAM CD-RW2000, Substitution of the Drive

Original drive (CD-W54E) has discontinued then new drive (CD-W58DA) for CD-RW2000 V3 is used for substitution. This info introduces how to mount CD-W58DA to original CD-RW2000.

Outline of work

- Replace Converter MPU
- Replace Front MPU
- Remove C402 on Digital I/O PCB
- Replace drive
- Update drive firmware
- Mount new tray panel
- Add an insertion owner's manual for CD-RW2000 V3

Note:
The production of CD-RW2000 V3 has been started from S/No. 0390001 and up.

Parts required

Item	Qty	P/No.	Description
Converter MPU	1	3S0048510A	UCOM Assy, HD64F7044 402V3
Front MPU	1	S00598300A	IC, CXP82040-160Q Front3 G
New drive	1	V00140000A	CD-W58DA-T00
New tray panel	1	M02038200A	Panel, Tray G RW2000 ASS
Insertion owner's manual (E)	1	(3D0046200A)	Sheet, ISKRC V3 CD-RW2000
Drive update CD-R			"T58V1td.abf" written

Actual work

1. Replace Converter MPU (U707 on Converter PCB A) with new.
2. Replace Front MPU (U500 on Front PCB A) with new.
3. Just remove C402 (Electrolytic Capacitor) on Digital I/O PCB.
4. Replace drive with new.
   Note that new tray panel cannot be mounted at this stage as tray cannot be opened.
5. Update drive firmware
   By replacing Converter MPU and Front MPU in the step 4 above, update capability of drive is added now. As new drive is supplied with basic PC condition, drive firmware should be updated. Refer to "Drive firmware update procedure".
6. Turn the power of unit on, open the tray then turn the power off. Mount new tray panel.
7. Add an insertion sheet for Version 3.0.

Drive firmware update procedure

There are two ways for drive update.
1. Update on CD-RW2000.
2. Update on Windows.

1. Update on CD-RW2000

Prepare a "Drive update CD-R" that has "T58V1td.abf" written on it.

Preparation:
1. Have a blank CD-R data disc available, as well as a system capable of creating data CDs.
2. Visit the **ROM Data Library** of the TASCAM Service HP website to download the firmware data image and write the firmware file on PC to the blank CD-R disc. (Use the "Disc at once" method that complies with ISO9660 Level 1: MS-DOS compatible)

Notice:
Be careful that the power supply to the unit is not interrupted during the update process otherwise firmware data of drive could be damaged and physical replacement of drive becomes unavoidable.

Procedure:
1. Turn on power of the unit while holding **CALL** and **MENU**.
2. Load the "Drive update CD-R" while display shows "RW2000 03.00" that is version of the Front MPU. If this version is less than 03.00, drive update function does not work. Then replace the Front MPU.
3. Confirm "CD" in display blinks. Then press **CALL** to check current version of drive firmware. Existing version is "V1.TA" and "V1.TB" (the latest) as of May/2005.
4. Press **MENU** then the display shows current version and new version to be updated as "D 1.TA→1.TD" for example.
5. Press **ENTER** then update will start. "NOW UPDATE" is displayed and "." at the right most corner blinks.
6. "COMPLETE" appears to show end up of the update successfully.
7. Turn off power of the unit.

2. Update on Windows

Prepare "CDW58DA_1TD.exe" data file.

Visit the **ROM Data Library** in the TASCAM Service HP website to download firmware data image of "CDW58DA_1TD.exe" into PC.

1. While PC is powered off, connect the CD-W58DA to PC and reboot. No need to consider Primary/Secondary and Master/Slave.
2. Double-click on "CDW58DA_1TD.exe" to run.
3. Follow the messages that will appear.

TEAC **TECHNICAL INFORMATION**

TASCAM CD-RW2000, Substitution of the Drive

No. **0505**
DATE 3rd August 2005

Original drive (CD-W54E) has discontinued then new drive (CD-W58DA) for CD-RW2000 V3 is used for substitution. This info introduces how to mount CD-W58DA to original CD-RW2000.

Outline of work

- Replace Converter MPU
- Replace Front MPU
- Remove C402 on Digital I/O PCB
- Replace drive
- Update drive firmware
- Mount new tray panel
- Add an insertion owner's manual for CD-RW2000 V3

Note:
The production of CD-RW2000 V3 has been started from S/No. 0390001 and up.

Parts required

Item	Qty	P/No.	Description
Converter MPU	1	3S0048510A	UCOM Assy, HD64F7044 402V3
Front MPU	1	S00598300A	IC, CXP82040-160Q Front3 G
New drive	1	V00140000A	CD-W58DA-T00
New tray panel	1	M02038200A	Panel, Tray G RW2000 ASS
Insertion owner's manual (E)	1	(3D0046200A)	Sheet, ISKRC V3 CD-RW2000
Drive update CD-R			"T58V1td.abf" written

Actual work

1. Replace Converter MPU (U707 on Converter PCB A) with new.
2. Replace Front MPU (U500 on Front PCB A) with new.
3. Just remove C402 (Electrolytic Capacitor) on Digital I/O PCB.
4. Replace drive with new.
   Note that new tray panel cannot be mounted at this stage as tray cannot be opened.
5. Update drive firmware
   By replacing Converter MPU and Front MPU in the step 4 above, update capability of drive is added now. As new drive is supplied with basic PC condition, drive firmware should be updated. Refer to "Drive firmware update procedure".
6. Turn the power of unit on, open the tray then turn the power off. Mount new tray panel.
7. Add an insertion sheet for Version 3.0.

Drive firmware update procedure

There are two ways for drive update.
1. Update on CD-RW2000.
2. Update on Windows.

1. Update on CD-RW2000

Prepare update drive CD-R that has "T58V1td.abf" written on it.

Preparation:
1. Have a blank CD-R data disc available, as well as a system capable of creating data CDs.
2. Visit the **ROM Data Library** of the TASCAM Service HP website to download the firmware data image and write the firmware file on PC to the blank CD-R disc. (Use the "Disc at once" method that complies with ISO9660 Level 1: MS-DOS compatible)

Notice:
Be careful that the power supply to the unit is not interrupted during the update process otherwise firmware data of drive could be damaged and physical replacement of drive becomes unavoidable

Procedure:
1. Turn the power on while holding **CALL** and **MENU**.
2. Load update drive CD-R while display shows "RW2000 03.00"
   If version above is less than 03.00, drive update function does not work.
   Then replace Front MPU.
3. Confirm "CD" in display blinks. Then press **CALL** to check current version of drive.
   Existing version is "V1.TA" and "V1.TB" (the latest) as of May/2005.
4. Press **MENU**. Then the display shows current version and new version to be updated.
5. Press **ENTER** then update will start.
   "NOW UPDATE" is displayed and "**.**" at the right most corner blinks.
6. "COMPLETE" is displayed to inform the update finished successfully.
7. Turn the power off.

2. Update on Windows

Prepare "CDW58DA_1TD.exe" data file.

Visit the **ROM Data Library** in the TASCAM Service HP website to download firmware data image of "CDW58DA_1TD.exe" into PC.

1. While PC is powered off, connect the CD-W58DA to PC and reboot.
   No need to consider Primary/Secondary and Master/Slave.
2. Double-click on "CDW58DA_1TD.exe" to run.
3. Follow the messages that will appear.

TEAC TECHNICAL INFORMATION

CD-RW Recorders, Converter MPU Change

No. **0328**
DATE 15th July 2003

Converter MPU, U707 of Converter PCB Assy, of following CD-RW recorders (*) has been changed as shown in the table.

* RW-H300/H500/800, CD-RW700/RW2000, RW-02/02USB, CD-RW4U

Version of Converter MPU	P/N of Converter MPU	P/N of Converter PCB (P/N printed on PCB)	S/N adopted respective converter MPU (X mark means there is no unit to adopt the MPU)						
			RW-H300	RW-H500	RW-800	CD-RW700	CD-RW2000	RW-02/02USB	CD-RW4U
Ver. 1.00 (Flash)	S003687-00A (IC, HD64F7044 CONVERT)	3E90247-00A [See Note-1).]				0010001			
Ver. 1.01 (Flash)	S003687-00B (IC, HD64F7044 CONVERT)	3E90247-00A /00B [See Note-1).]	0010001	0010001	0010001	0011001			
Ver. 1.02 (Masked)	S003688-00A (IC, HD6437042 CONVERT)	3E90247-00C /00D	0030481	0040001	0040001	0040001			
Ver. 1.03 (Masked)	S003829-00A (IC, HD6437042 CONVERT 2)	3E90247-00D				unknown			
Ver. 1.04 (Flash)	S003868-00A (IC, HD64F7044 CONVERT 3)	3E90247-00D					0010001		
Ver. 1.04 (Masked)	S003869-00A (IC, HD6437042 CONVERT 3)	3E90247-00D				(unknown)	(unknown)	0010001	
Ver. 1.10 (Flash)	S004186-00A (IC, HD64F7044 CONVERT 4)	3E90247-00D [See Note-2).]					0090001		
Ver. 1.10 (Masked)	S004185-00A (IC, HD6437042 CONVERT 4)		0120039	0120001	0160001	0131999	0130001	0020001	0010001
Ver. 1.11 (Masked)	S004264-00A (IC, HD6437042 CONVERT 5)	3E90247-00D [See Note-1).]	(unknown)	(unknown)	(unknown)	(unknown)	(unknown)	(unknown)	(unknown)

Note:
1) The latest Ver. 1.11 is supplied when you order the Converter MPU. However the Ver. 1.11 cannot be used with earlier two Converter PCBs, 3E90247-00A/00B. If the Ver 1.11 is mounted on the two Converter PCBs, unit doesn't work. In the case, replacing Converter PCB Assy is required.
2) This change is to support CD-RW4U.
3) RW-02/02USB and CD-RW4U have Main PCB E901168-00A instead of Converter PCB. On the models, Converter MPU is mounted on the Main PCB Assy as U109.
4) The Converter MPU U707 is a QPD SMD soldered on the Converter PCB without socket.

Fixed Problems

- V1.01 (Flash)

1) When "D-IN UNLOCK" is displayed, click noise is heard.
2) When sync-recording through digital input with certain MD recorder, unit doesn't stop even if the MD recorder stops.
3) When recording through digital input, sync-recording doesn't start even if 5 seconds or more elapses from beginning of track.

- V1.02 (Masked)

This change is to produce the V1.01 (Flash) by means of masked ROM method to reduce cost. There is no change of features.

- V1.03 (Masked)

To reduce Mech Assy vibration resulting some noise, rotational speed of disc in play mode is reduced from 8 times to 4 times.

- V1.04 (Flash)

This change is to support CD-RW2000.

- V1.04 (Masked)

This change is to produce the V1.04 (Flash) by means of masked ROM method to reduce cost. There is no change of features.

- V1.10 (Flash)

This change is to support CD-RW4U.

- V1.10 (Masked)

This change is to produce the V1.10 (Flash) by means of masked ROM method to reduce cost. There is no change of features.

- V1.11 (Masked)

Level meter indication disappears when following steps are operated:
1) Record a sound by Sync-record method.
2) Set the unit to digital in monitor mode.
3) Level meter indication disappears when following a) or b) feature starts:
   a) Sync record
   b) Index increment

Note: This appears with V1.10 (Flash/Masked) only.

TEAC **TECHNICAL INFORMATION**

RW-800/CD-RW700/CD-RW2000, Change of Capacitor

No. **0206**
DATE 31st May 2002

Symptom: Various. No display, Suddenly stops, does not boot and so on.
Cause: Defective C07 (Electrolytic Capacitor, 10000µF/16V) on the AUDIO/POWER PCB Assy.
Product quality of the capacitor seems to be low.
Remedy: C07 capacitor has been changed to another manufacturer's one as follows:

	Original	New
Part Number	3C001350 (YEC)	C0037740
Manufacturer	YEC	nichicon

New capacitor has been mounted on the following products.
- RW-800 S/No. 0250001 and higher
- CD-RW700 S/No. 0260001 and higher
- CD-RW2000 S/No. 0140001 and higher

Additional Information
1. It has been reported that "pressure relief vent" of the defective C07 would open like Fig. 1.
2. C07 is fixed by an adhesive bond. This looks like a "leak" but not. See Fig. 2.

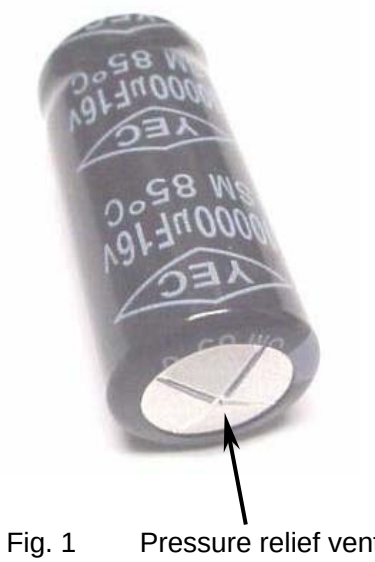


Fig. 1 Pressure relief vent

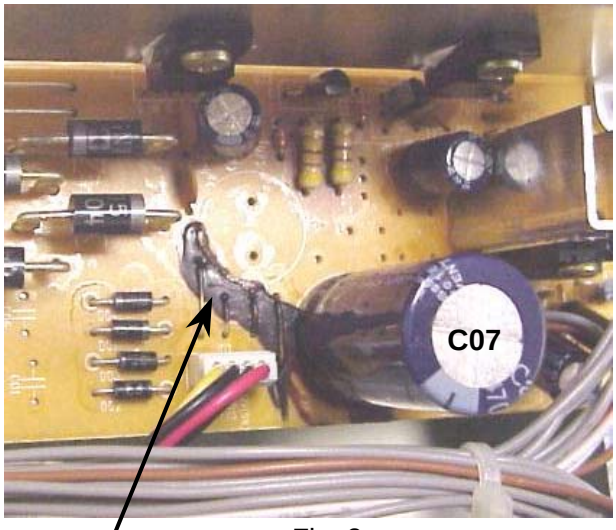


Fig. 2
This is not a leak but an adhesive bond.