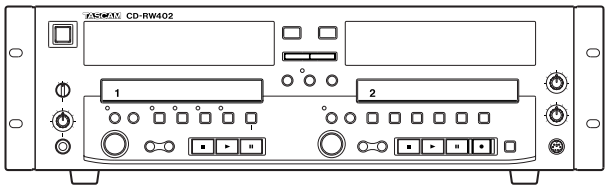


TASCAM
TEAC Professional Division

SERVICE MANUAL

CD-RW402

CD Recorder/Duplicator

COMPACT disc Recordable ReWritable

CONTENTS

目次

INSTRUCTIONS FOR SERVICE PERSONNEL

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

Effective : January, 2002

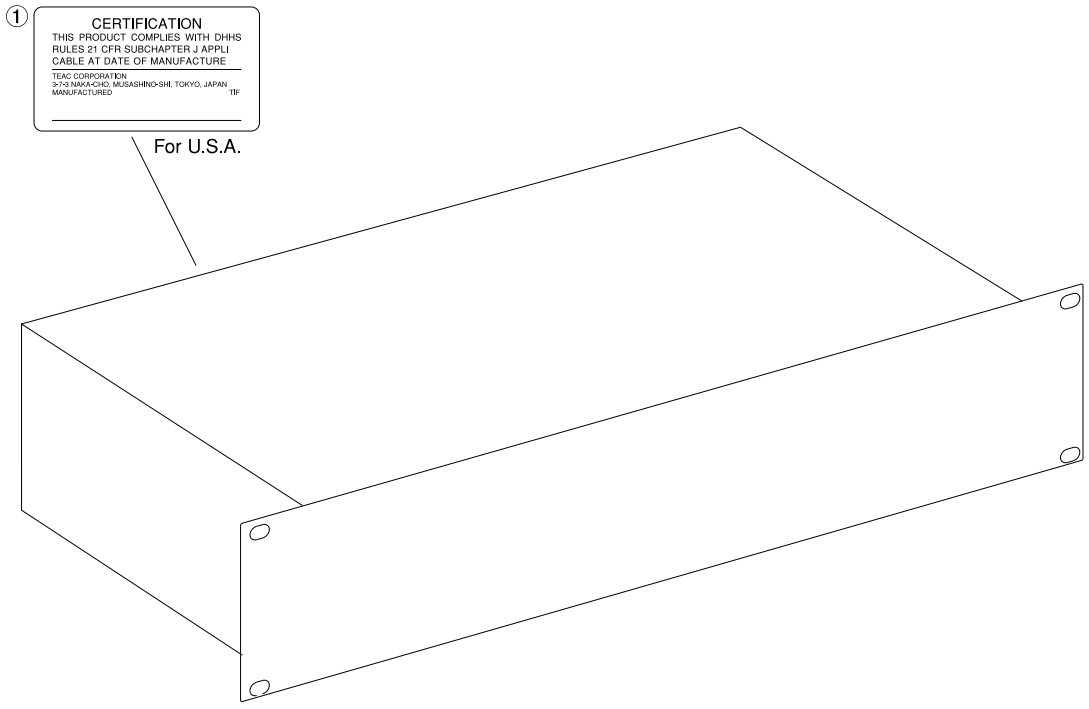
S-0049

1. SAFETY INFORMATION
セーフティーインフォメーション

This product has been designed and manufactured according to FDA regulations "title 21, CFR, chapter 1, subchapter J, based on the Radiation Control for Health and Safety Act of 1968", and is classified as a class 1 laser product. There is no hazardous invisible laser radiation during operation because invisible laser radiation emitted inside of this product is completely confined in the protective housings.
The label required in this regulation is shown ①.

● **CAUTION**

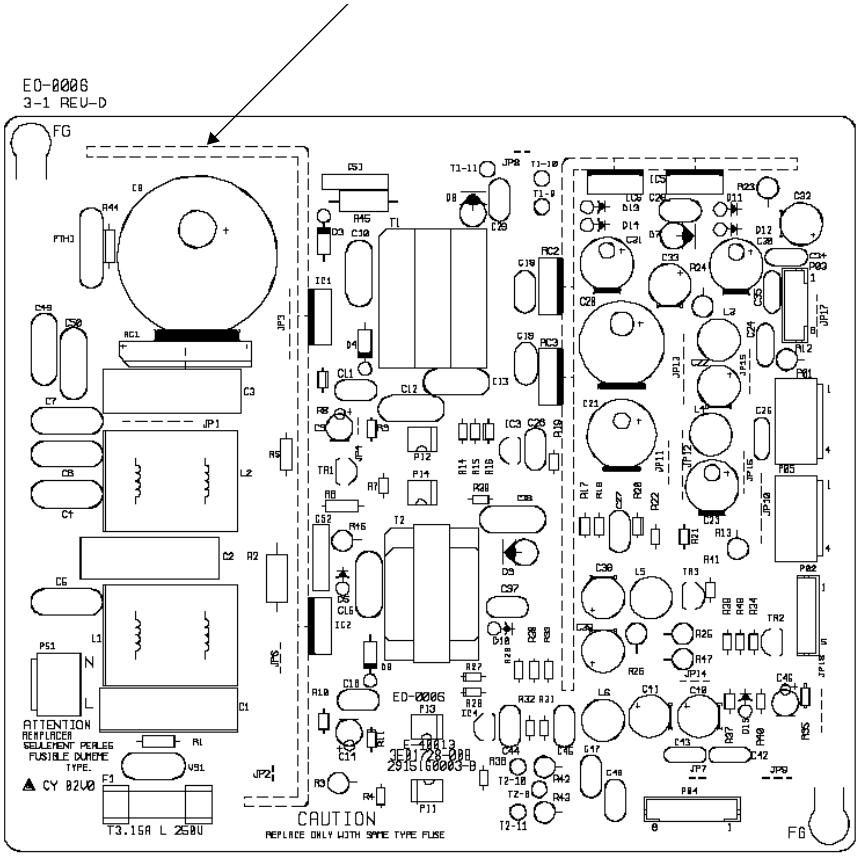
USE OF CONTROLS OR ADJUSTMENT OR PERFORMANCE OF PROCEDURES OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.



Drive 1 (CD-ROM)	
Optical pickup:	KSS-575B
Manufacturer:	SONY Corporation
Laser Output::	Less than 0.4 mW on the objective lens
Wavelength:	760 - 780 nm
Drive 2 (CD-RW)	
Optical pickup type :	KRS-202A or KRS-220B
Manufacturer :	SONY Corporation
Laser output :	Less than 0.1 mW (Play) and 32 mW (Record) on the objective lens
Wavelength :	777 - 787 nm

This heatsink of SW power supply is on the primary side.
There is danger of receiving an electric shock if you touch when power is turned on.

SW 電源のこのヒートシンクは 1 次側です。
電源を入れた状態で触れると感電しますので注意してください。



2. SPECIFICATIONS
仕様

Drive 1

Media type: CD-R, CD-RW, CD-RDA, CD-RWDA
Frequency response: 20 Hz — 20 kHz (playback ±0.8 dB)
S/N ratio: > 95 dB (playback)
Dynamic range: > 95 dB (playback)
Total harmonic distortion: < 0.005% (playback)
Channel separation: 90 dB (playback: 1 kHz)
Wow & flutter: Unmeasurable (< 0.001%)

Drive 2

Recording media type: CD-R, CD-RW, CD-RDA, CD-RWDA
Recording resolution: 16-bit linear
Recording sampling frequency: 44.1 kHz
Frequency convertor input: 32 kHz — 48 kHz
Frequency response:
20 Hz — 20 kHz (playback ±0.8 dB, recording ±1 dB)
S/N ratio: > 95 dB (playback), > 90 dB (recording)
Dynamic range: > 95 dB (playback), > 90 dB (recording)
Total harmonic distortion:
< 0.005% (playback)
< 0.008% (recording)
Channel separation:
90 dB (playback: 1 kHz)
80 dB (recording: 1 kHz)
Wow & flutter: Unmeasurable (< 0.001%)

Digital I/O

Digital inputs (drive 2 only)
COAXIAL RCA pin, IEC-60958 TYPE I, TYPE II — auto-detect
OPTICAL TOSLINK, IEC-60958 TYPE I, TYPE II — auto-detect
Digital outputs (drives 1 and 2)
COAXIAL RCA pin, IEC-60958 TYPE II (SPDIF)
OPTICAL TOSLINK, IEC-60958 TYPE II (SPDIF)

Analog I/O

UNBALANCED LINE OUTPUTS (1, 2, COMMON)
Unbalanced RCA
Nominal output level: –10 dBV (FS –16 dB)
Maximum output level: +6 dBV
Output impedance: 570 Ω(unbalanced)
BALANCED LINE OUTPUTS 1, 2
XLR-3 type (male) (1-gnd, 2=hot, 3=cold)
Nominal output level: +4 dBu (FS –16 dB)
Maximum output level: +20 dBu
Output impedance: 75 Ω
UNBALANCED LINE INPUTS (2)
Unbalanced RCA
Nominal input level: –10 dBV (FS –16 dB)
Maximum input level: + 6dBV
Input impedance: 23 kΩ
BALANCED LINE INPUTS (2)
XLR-type (female) (1-gnd, 2=hot, 3=cold)
Nominal input level: +4 dBu (FS –16 dB)
Maximum input level: +20dBu
Input impedance: 12 kΩ

ドライブ 1 性能仕様

ドライブタイプ： CD 再生機
再生可能ディスク： CD/CD-R/CD-RW
量子化ビット数： 16 ビットリニア
サンプリング周波数： 44.1kHz
再生周波数特性： 20 ～20kHz, ± 0.8dB （再生時）
S/N 比： 95dB 以上
ダイナミックレンジ： 95dB 以上
歪率： 0.005 %以下
チャンネルセパレーション： 90dB （1kHz ）以上
ワウフラッター：測定限界以下（0.001 %以下）

ドライブ 2 性能仕様

ドライブタイプ： CD-R/CD-RW 録音／再生機
記録スピード：× 1 、× 2 、× 4
記録可能ディスク： CD-R 、CD-R-DA 、CD-RW 、CD-RW-DA
再生可能ディスク： CD/CD-R/CD-RW
量子化ビット数： 16 ビットリニア
サンプリング周波数： 44.1kHz
再生周波数特性： 20 ～20kHz
± 0.8dB （再生時）
± 1.0dB （記録時）
S/N 比： 95dB 以上（再生時）、80dB 以上（記録時）
ダイナミックレンジ：
95dB 以上（再生時）、80dB 以上（記録時）
歪率： 0.005 %以下（再生時）、0.008 %以下（記録時）
チャンネルセパレーション：
90dB 以上（再生時 1kHz ）
80dB 以上（記録時 1kHz ）
ワウフラッター：測定限界以下（0.001 %以下）

デジタル入出力仕様

デジタル入力（ドライブ 2 のみ）
INPUT（COAXIAL ）： RCA ピン
IEC-60958 TYPE I,TYPE II 規格準拠（自動検出）
INPUT（OPTICAL ）： TOSLINK
IEC-60958 TYPE I,TYPE II 規格準拠（自動検出）
デジタル出力（ドライブ 1 、2）
OUTPUT（COAXIAL ）： RCA ピン
IEC-60958 TYPE II（S/PDIF ）
OUTPUT（OPTICAL ）： TOSLINK
IEC-60958 TYPE II（S/PDIF ）

アナログ入出力仕様

アナログ入力（ドライブ 2 のみ）
ANALOG（UNBALANCED ）INPUT ： RCA ピン
基準入力レベル：－ 10dBV（FS －16dB ）
最大入力レベル：＋ 6dBV
入力インピーダンス： 23k Ω
ANALOG（BALANCED ）INPUT ： XLR バランス
（1 番：グランド、2 番：ホット、3 番：コールド）
基準入力レベル：＋ 4dBu（FS －16dB ）
最大入力レベル：＋ 20dBu
入力インピーダンス： 12k Ω

PHONES output (switchable 1, 2 or COMMON)

6 mm (1/4") stereo
Output level: 20 mW + 20 mW (into 32 Ω)

Control

CONTROL I/O: D-sub 25-pin female
KEYBOARD: Mini-DIN 6pin (conforms to PS/2 standard)
REMOTE IN: 3.5 mm mini-jack (only for use with RC-RW402)

Writable disc formats

CD-DA (including CD-TEXT), CD-ROM (IS09660), CD Extra.
When copying CD Extra discs, DISC copying allows copying of audio data, and DAO copying allows copying of data.

General specifications

Voltage requirements:
USA/Canada 120 VAC, 60 Hz
U.K./Europe 230 VAC, 50 Hz
Australia 240 VAC, 50 Hz
Power consumption:
100 V — 120 V: 34 W, 220 V — 240 V: 39 W
Applicable electromagnetic environment: E4
Peak inrush current: 6.1 A (Pro CE)
Dimensions: 483 x 138 x 301 (mm), 19 x 5.4 x 11.6 (in)
Weight: 8 kg (17.6 lb.)
Operating temperature: 5°C to 35°C (41°F to 95°F)
Supplied accessories:
RC-RW402 remote control unit
2m (6 ft.) AC cord
Rack mount screw kit
Quick start guide

● Specifications and appearance subject to change without notice.

アナログ出力（ドライブ１、２、COMMON）

ANALOG （UNBALANCED ）OUTPUT ： RCA ピン
基準出力レベル：－ 10dBV（FS － 16dB ）
最大出力レベル：＋ 6dBV
出力インピーダンス：570 Ω
ANALOG （BALANCED ）OUTPUT ： XLR バランス
（1 番：グランド、2 番：ホット、3 番：コールド）
基準出力レベル：＋ 4dBu（FS － 16dB ）
最大出力レベル：＋ 20dBu
出力インピーダンス：75 Ω

ヘッドホン出力仕様

6 φステレオ
20mW ＋ 20mW （32 Ω負荷時）

リモート端子仕様

CONTROL I/O 端子： Dsub 25pin
KEYBOARD 端子： MINI DIN 6pin (PS/2 準拠)
REMOTE IN 端子： RC-RW402 専用

書き込みフォーマット

CD-DA（CD-TEXT 対応）、
CD-ROM（ISO9660 ）
CD Extra*

＊ CD Extra は、DISC コピーと DAO が選択できます。ただし、DISC コピーの場合はオーディオトラックのみの記録になります。その後のデータ部分までコピーしたいときは、DAO を選択してください。

一般

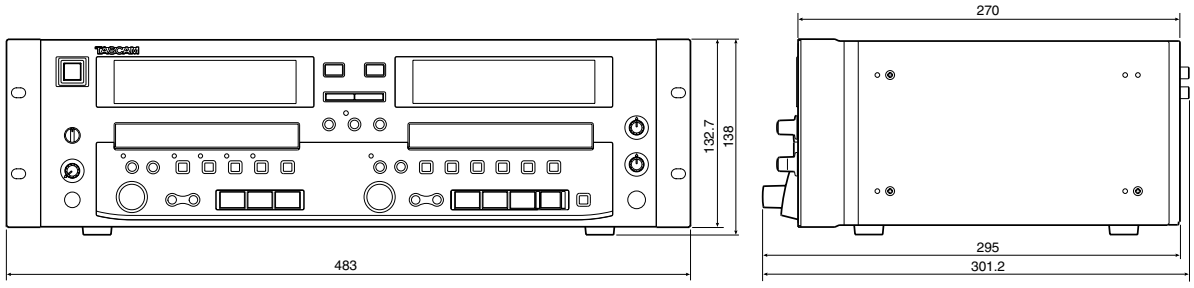
電源： 100VAC 、50 － 60Hz
消費電力： 34W
外形寸法（幅×高さ×奥行き）： 483 × 138 × 301mm
質量： 8kg

付属品

RC-RW402 リモートコントロールユニット
ラックマウントビスキット（ビス 4 本、ワッシャー 4 本）
電源コード

● 仕様および外観は、改善のため予告なく変更することがあります。

Dimensional drawing　寸法図



3. TEST MODE
テストモード

3-1. How to enter test mode

1. Hold down STOP + PLAY + READY by the side of Drive 1 and power to the unit.
   The unit will run into test mode, the display showing the Front MPU Version No.
2. Pressing STOP while the Version No. is shown terminates the test mode and the unit goes back to normal mode.

3-2. Checks in test mode

3-2-1. Front key check (Drive 1/Drive 2 Separate)

1. Press the PLAY key to enter the front key check mode.
2. The display shows the name of each key to be checked; press the corresponding key.
   When the check result of the key is OK, the display shows another key name. When the result is No Good, the display continues to show the same key name.
3. The display finally shows “dial50”. Check the MULTI DIAL so that the displayed figure increases when the dial is rotated clockwise and decreases when it is rotated counterclockwise.
4. Press the PLAY key to exit from the front key check mode and return to the Version No. display mode.

3-2-2. Display/LED check (Drive 1/Drive 2 Separate)

1. Press the DISPLAY key to enter the display check mode.
2. Press DISPLAY key a few times and ensure that each press lights the display blocks one after another. (For Drive 2, all LEDs are also lit up upon completion of the process.)
3. When all the indicators are lit, press the DISPLAY key to exit from the display check mode and return to the Version No. display mode.

3-2-3. EEPROM default setting (Drive2 only)

The following operation writes the default data in the EEPROM and checks the write data automatically.

1. Press the ERASE key.
   When the default data is written correctly, the display shows “EEPROM OK !!”. If not, it shows “EEPROM NG!!”.
2. Press the ERASE key again to return to the Version No. display mode.

Note: When setting EEPROM to default settings, recycle the power.

3-2-4. Converter MPU Version No. display (Drive 1/Drive 2 Separate)

1. When the READY key is pressed, the display shows the converter MPU version number.
2. Press the READY key again to return to the Version No. display mode.

3-1. テストモードの入り方

1. Drive 1 側の STOP キー＋ PLAY キー＋ READY キーを押しながら POWER ON すると、表示部に Front マイコンの Version No. が表示されテストモードに入る。
2. Version No. 表示中に STOP キーを押すと、テストモードは終了し通常の動作に戻る。

3-2. テストモードでのチェック

3-2-1. フロントキーチェック（Drive 1/Drive 2 独立）

1. PLAY キーを押し、フロントキーチェックモードに入る。
2. 表示部にチェックするキーの名称が表示されるので、そのキーを押す。チェック OK なら次のキーの名称が表示され、NG なら表示は変化しない。
3. 一通りキーの確認が終了すると、ディスプレイに“dial50”と表示される。MULTI DIAL を回し、表示の数字が右回しで増加、左回しで減少することを確認する。
4. PLAY キーを押すと、フロントキーチェックモードを終了し Version No. 表示に戻る。

3-2-2. ディスプレイ/LED チェック（Drive 1/Drive 2 独立）

1. DISPLAY キーを押し、ディスプレイチェックモードに入る。
2. DISPLAY キーを押すたびに、表示部がブロックごとに点灯することを確認する。（Drive 2 側では、最後に LED も全点灯する）
3. 表示部が全点灯した状態から DISPLAY キーを押すと、ディスプレイチェックモードを終了し Version No. 表示に戻る。

3-2-3. EEPROM デフォルト設定（Drive 2 のみ）

EEPROM にデフォルト値を書き込み、自動的に書き込みチェックを行う。

1. ERASE キーを押す。
   このとき、正しく書き込めていれば、表示部に“EEPROM OK !!”と表示され、不良の場合は“EEPROM NG !!”と表示される。
2. 再度 ERASE キーを押すと、Version No. 表示に戻る。

注）EEPROM をデフォルトにした場合は、1 度電源を切ってください。

3-2-4. コンバータマイコンバージョン表示（Drive 1/Drive 2 独立）

1. READY キーを押すと、コンバータマイコンのバージョンを表示する。
2. 再度 READY キーを押すと、Version No. 表示に戻る。

3-2-5. Drive unit Version No. display

1. When the CALL key is pressed, the display shows the drive unit version number.
2. Press the CALL key again to return to the Version No. display mode.

3-2-6. Upgrading the Converter or Drive F/W

1. Push the Converter/Drive F/W Upgrading disk in the necessary drive.
2. Press the MENU key.
   The display will show both the new and old version numbers. Also, to the left of the old version display will show "C" in the case of the Converter F/W or "D" in the case of the Drive F/W. (Example: C02.00→02.01)
3. Push the MULTI DIAL and "NOW UPDATE" will show and a dot (.) will blink in the right corner of the display.
4. When about 1 minute is up, the display will switch back to show the Version No.

3-2-5. ドライブバージョン表示

1. CALL キーを押すと、ドライブユニットのバージョンを表示する。
2. 再度 CALL キーを押すと、Version No. 表示に戻る。

3-2-6. コンバータ／ドライブ F/W バージョンアップ

1. コンバータまたはドライブ F/W バージョンアップ用ディスクをバージョンアップする Drive に入れる。
2. MENU キーを押す。
   ディスプレイに旧バージョンと新バージョンが表示される。また、旧バージョン表示の左側に、コンバータ F/W なら"C"、ドライブ F/W なら"D"を表示する。
   （例：C02.00→02.01）
3. MULTI DIAL を押すと、"NOW UPDATE"と表示され、右隅の "." が点滅する。
4. 約 1 分後に、Version No.表示に戻る。

4. AUDIO CHECKS
オーディオ確認

4-1. Playback performance (Drive 1/Drive 2)　再生系（Drive 1/Drive 2)

Mode : PLAY
Measurement point : ANALOG OUTPUT (COMMON)

ITEM 項目	TEST DISC テストディスク	PLAYBACK SIGNAL 再生信号	SPECIFICATIONS 規格	REMARKS 備考
1. **Playback level** **再生レベル**	MCD-111 Track 2	1 kHz, 0 dB	2.0 ± 0.4 V	
2. **Playback frequency responce** **再生周波数特性**	MCD-111 Track 3–6	20 Hz–20 kHz, 0 dB	0 ± 0.8 dB	reference : 1 kHz 1 kHz 基準
3. **Playback distortion** **再生歪率**	MCD-111 Track 2	1 kHz, 0 dB	0.005 % or less	20 kHz LPF
4. **Playback SN ratio** **再生 SN 比**	MCD-111 Track 7	– ∞ dB	95 dB or better	20 kHz LPF ＋ IEC-A
5. **Playback channel separation** **再生チャンネルセパレーション**	MCD-111 Track 8, 10	1 kHz, 0 dB	90 dB or better	IEC-A

4-2. Monitor performance (Drive 2 only)　モニター系（Drive 2 のみ）

Mode : REC Monitor
Input terminal : ANALOG (UNBALANCED) INPUT (DRIVE 2)
Measurement point : ANALOG (UNBALANCED) OUTPUT (DRIVE 2)

ITEM 項目	INPUT SIGNAL 入力信号	SPECIFICATIONS 規格	REMARKS 備考
1. **Record level** **録音レベル**	1 kHz, +6 dBV	+6 dBV ± 2 dB	Select "DIG VOLUME" from "REC MENU 1" in the menu group, and rotate MULTI DIAL for 0 dB. Turn the INPUT control to position at which the "OVER" segments of the level meter is just about to light. Once done, keep this adjustment unchanged until all the necessary measurements have been made. メニューグループの "REC MENU 1"で、"DIG VOLUME" を選び、MULTI DIAL を回して 0 dB に設定する。 INPUT つまみを回して、レベルメーターの "OVER" が点灯する直前になるように調整する。 調整後は全ての測定が終わるまでこの状態にしておく。
2. **Monitor frequency responce** **モニター周波数特性**	20 Hz–20 kHz, –10 dBV	0 ± 1 dB	reference : 1 kHz 1 kHz 基準
3. **Monitor SN ratio** **モニター SN 比**		90 dB or better	Ratio of output level at +6 dB input to noise level ＋ 6 dBV 入力時の出力レベルとノイズレベルとの比 20 kHz LPF ＋ IEC-A
4. **Monitor channel separation** **モニターチャンネルセパレーション**	L (R) ch : 1 kHz, +6 dBV R (L) ch : No signal L ch : 10 kHz, +6 dBV R ch : No signal	80 dB or better 60 dB or better	Ratio of Lch output level to Rch output level Lch 出力と Rch 出力の比 IEC-A
5. **Monitor distortion** **モニター歪率**	1 kHz, +5 dBV	0.008 % or better	20 kHz LPF

PARTS LIST SECTION

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with ∗ require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in the manual.
- ⚠Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J]: JAPAN [US/C]: U.S.A./CANADA [K]: KOREA [E]: EUROPE
  [UK]: U.K. [A]: AUSTRALIA

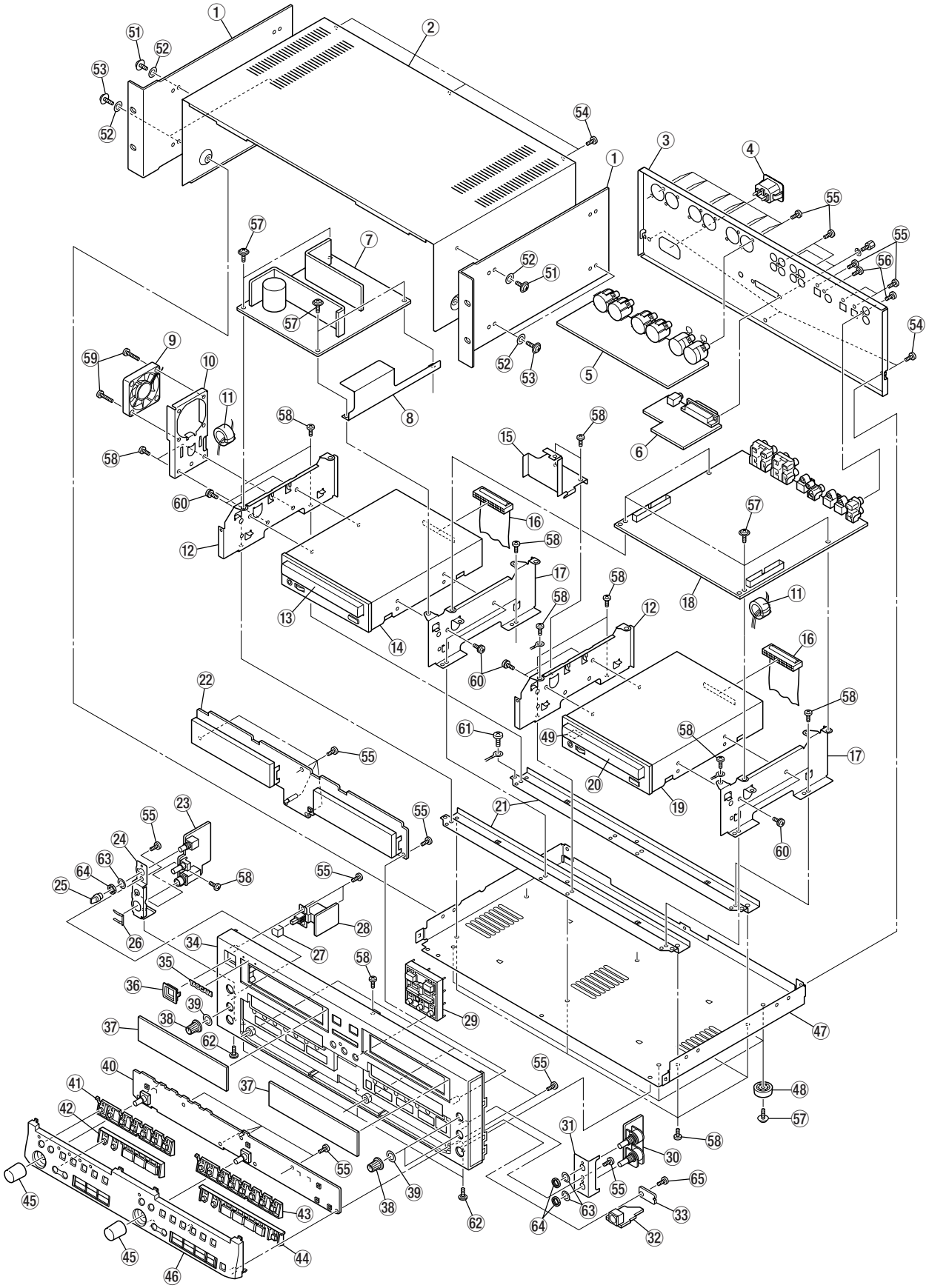
注 意

- プリント基板は部品面が示されています。
- ∗印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品及び品番のない部品は供給しません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠は安全重要部品です。
  交換する時は必ずティアック指定の部品を使用してください。
- 仕向先
  [J]: JAPAN [US/C]: U.S.A./CANADA [K]: KOREA [E]: EUROPE
  [UK]: U.K. [A]: AUSTRALIA

5. EXPLODED VIEW AND PARTS LIST

分解図とパーツリスト

EXPLODED VIEW-1



EXPLODED VIEW-1

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	3M0026601A	RACK MOUNTING N64(3U)	
1- 2	*3M0026010A	BONNET	
1- 3	*M01334500A	PANEL,REAR	
1- 4	*5332030400	AC INLET	
1- 5		PCB ASSY,BAL ·····	PCB ASSY,GATHER B (Refer to page 14)
1- 6		PCB ASSY,CONTROL ·····	PCB ASSY,GATHER A (Refer to page 14)
1- 7	3E0172800B	SW RGLTD PS,EO-0006	
1- 8	*M01366400A	COVER,PCB	
1- 9	M01353600A	FAN MOT ASSY,MF52A12LT002	
1-10	*M01366200A	BRACKET,FAN(52)	
1-11	*3E010000	FER.CORE,B18T 25X12X15	
1-12	*M01334700A	BRACKET,MECH(L)	
1-13	3M0093901B	PANEL,TRAY(1)	
1-14	3Y0045900A	DRIVE ASSY,CD-532E AV	
1-15	*M01366300A	BRACKET,CENTER	
1-16	3E0175100A	CABLE ASSY,40P-L330	
1-17	*M01334800A	BRACKET,MECH(R)	
1-18	*3E9536400A	PCB ASSY,MAIN	
1-19	3Y0046000A	DRIVE ASSY,CD-W54E TEXT	
1-20	3M0093902B	PANEL,TRAY(2)	
1-21	*M01334600A	BRACKET,BOTTOM	
1-22		PCB ASSY,FRONT1 ·····	PCB ASSY,GATHER FRONT1 (Refer to page 13)
1-23		PCB ASSY,PHONE ·····	PCB ASSY,GATHER A (Refer to page 14)
1-24	*M01335200A	BRACKET,PHONE	
1-25	M01335000A	KNOB,ROTARY	
1-26	*3E011630	MOUNT PLATE JACK	
1-27	M01335100A	BUTTON,POWER	
1-28		PCB ASSY,P-SW ·····	PCB ASSY,GATHER A (Refer to page 14)
1-29	M01334400B	BUTTON,CENTER	
1-30		PCB ASSY,VR ·····	PCB ASSY,GATHER A (Refer to page 14)
1-31	*M01335300A	BRACKET,INPUT	
1-32		PCB ASSY,KEYBOARD ·····	PCB ASSY,GATHER A (Refer to page 14)
1-34	M01333800C	PANEL,FRONT	
1-35	5720254101	NAME PLATE,TASCAM(S)	
1-36	M01334900A	ESCUTCHEON,POWER	
1-37	M01335400A	WINDOW,FL	
1-38	M00002503A	KNOB,GB	
1-39	*M01388100A	POLYEST WASHER,D14	
1-40		PCB ASSY,FRONT2 ·····	PCB ASSY,GATHER A (Refer to page 14)
1-41	M01334000B	BUTTON,(L1)	
1-42	M01334200A	BUTTON,(L2)	
1-43	M01334100A	BUTTON,(R1)	
1-44	M01334300A	BUTTON,(R2)	
1-45	M01335500A	KNOB,D17	
1-46	*M01333900A	ESCUTCHEON,FRONT	
1-47	M01335600A	CHASSIS,BOTTOM	
1-48	3M001950	FOOT,21MM	
1-49	*M01388200A	SPACER,12.5X12.5	

EXPLODED VIEW-1

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1-51	3B0001806A	SCREW,J,S M3X6 (BLK)	
1-52	*3M002020	FIBER WASHER,3X8X0.3T (BLK)	
1-53	3B0001812B	SCREW,J,S M3X12 (BLK)	
1-54	*3B0003808A	SCREW,VPC M3X8 (BLK)	
1-55	*3B0004808A	SCREW,BPP M3X8 (BLK)	
1-56	*3B0005708B	SCREW,BPB M3X8 (BLK)	
1-57	*3B0001306A	SCREW,J,S M3X6	
1-58	*3B0005308A	SCREW,BPB M3X8	
1-59	*3B0000112A	SCREW,BPS M3X12	
1-60	*3B0007400A	SCREW,BPAA M3X6	
1-61	*3B0001908A	SCREW,J,S M4X8 (BLK)	
1-62	*B0117800A	SCREW,DPB M3X8 FZC	
1-63	*3M0096900A	NUT,M7	
1-64	M00002503A	KNOB,GB	
1-65	*3B0004810A	SCREW,BPP M3X10 (BLK)	

6. PC BOARDS AND PARTS LIST

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MAIN PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*3E9536400A	PCB ASSY,MAIN
D101	3S002984	DIODE,1SS355 TE-17 TP
D301	3S002984	DIODE,1SS355 TE-17 TP
D501-504	3S002984	DIODE,1SS355 TE-17 TP
D601-604	3S002984	DIODE,1SS355 TE-17 TP
D701-713	3S002984	DIODE,1SS355 TE-17 TP
D950	3S002984	DIODE,1SS355 TE-17 TP
J101	3E013000	RCA 1P PIN JACK,RJ-1081
J301	3E017600	JACK,RJ-1060A-31-0341A
J501,502	3E010590	JACK,RJ-1073B-09-0320A
L101	3E017290	COIL,RCH-875 47UH
L103	E0013294	COIL,LQH3N 4.7 UH
L104	3E014354	COIL,4.7UH LK2125 4R7K T
L105,106	3E011820	FB,FBR07HA850SB-00
L302	E0013294	COIL,LQH3N 4.7 UH
L303-306	3E011820	FB,FBR07HA850SB-00
P101	3E015110	CONNECTOR,40P 3675P40VUA0
P102	3E0173400A	HARNESS ASSY,5P RM
P103	3E0173800A	HARNESS ASSY,9P F1M1
P104	3E010390	CONNECT PLUG,B7B-PH-K-S
P105	3E001180	CONNECT PLUG,6P B6B-EH-A
P201	3E003810	CONNECT PLUG,B2B-PH (RED)
P202	3E001140	CONNECT PLUG,2P B2B-EH-A
P301	3E015110	CONNECTOR,40P 3675P40VUA0
P303	3E0173900A	HARNESS ASSY,9P F1M2
P304	3E010390	CONNECT PLUG,B7B-PH-K-S
P501	3E010380	CONNECT PLUG,B6B-PH-K-S
P502	3E006080	CONNECT PLUG,B4B-PH-K (BLK)
P503	3E003830	CONNECT PLUG,B4B-PH (RED)
P504	3E010360	CONNECT PLUG,B4B-PH-K-S
P505	3E010410	CONNECT PLUG,B9B-PH-K-S
P506	3E010350	CONNECT PLUG,B3B-PH-K-S
P507	3E0173500A	HARNESS ASSY,6P RM RW402
P508	3E014770	CONNECT PLUG,B3B-PH (RED)
P950	3E010340	CONNECT PLUG,B2B-PH-K-S
Q101	3S002994	TR,DTC124EUA T106 TP
Q301	3S002994	TR,DTC124EUA T106 TP
Q501-507	S0041624	TR,2SD2114K T146 W
Q601-607	S0041624	TR,2SD2114K T146 W
Q701-703	S0041574	TR,DTA124EUA T106
Q704	3S002994	TR,DTC124EUA T106 TP
Q705,706	S0041574	TR,DTA124EUA T106
RA101-104	R0017404	RES ARRAY,1/16W 4X33 J
RA301-304	R0017404	RES ARRAY,1/16W 4X33 J
T101,301	3E01323-00A	PULS TRANS,S-701-001
U101	S0037164	IC,TC74VHCT541AFT(EL)TSSO
U102,103	S0037174	IC,TC74VHCT245AFT(EL)TSSO
U104	3S00485-00C	UCOM ASSY,HD64F7044
U105	S0039753	IC,M11B16161A-45T
U106	S003619-00A	IC,AUDIO CONVERTER

MAIN PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
U107	3S0048400A	CPLD ASSY,XC9536-15PC44C2
U108	3S002934	IC,TC74HC02AF(EL) SMT.TA
U109	3S003424	IC,NJM2370U05
U110	3S003414	IC,MC74HC4046AFR1
U111	3S001344	IC,TC74HCU04AF(EL)
U112	S0042044	IC,TC9271FS
U113	3E017640	OPT CONN,TOTX178A
U114	3S001344	IC,TC74HCU04AF(EL)
U115	3E011830	FILTER,EMT470BT
U301	S0037164	IC,TC74VHCT541AFT(EL)TSSO
U302,303	S0037174	IC,TC74VHCT245AFT(EL)TSSO
U304	3S0048500C	UCOM ASSY,HD64F7044
U305	S0039753	IC,M11B16161A-45T
U306	S00361900A	IC,AUDIO CONVERTER
U307	3S004884	IC,TC74HC04AF(EL) SMT TA
U308	3S004884	IC,TC74HC04AF(EL) SMT TA
U309	3S002954	IC,LC8905V
U310	S0041563	IC,SM5844AF
U311	S0042044	IC,TC9271FS
U312	3S002914	IC,TC74VHC74F(EL) SMT.TA
U313	3S002934	IC,TC74HC02AF(EL) SMT.TA
U314	3S001344	IC,TC74HCU04AF(EL)
U315	3E011830	FILTER,EMT470BT
U316	3E017630	OPT CONN,TORX178B
U317	3E017640	OPT CONN,TOTX178A
U501-509	3S004894	IC,NJM4580V(SSOP) IA
U701,702	S0035883	IC,CS4223-KS
U703	3S004884	IC,TC74HC04AF(EL) SMT TA
U704	3S000650	IC,NJM7805FA
U901-903	3S004914	IC,IDTQS3384Q
U950	3S002420	IC,NJM7809FA
VC101	S0035214	DIODE,HVC376B-TRF
X101 X301	3E011994	RESONATOR,CSTCC 7.17MG0H6
X302	3E011974	X'TAL,11.2896MHZ

GATHER FRONT1 PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*3E9537400A	PCB ASSY,GATHER FRONT1 [J,US/C]
	*3E9537401A	PCB ASSY,GATHER FRONT1 [E,K,UK,A]
		PCB ASSY,FRONT1
	3E9037500A	PCB,BRACKET(A)
	3E9037600A	PCB,BRACKET(B)
	3M01240-01A	SPACER,LED L=15.5
	3M00909-00A	HOLDER,FL

GATHER FRONT1 PCB ASSY

REF.NO.		PARTS NO.	DESCRIPTION
		M013878-00A	PROTECTOR,FL
D1-5		3S000241	D,1SS133 T-77
D6		3S001891	ZD,MTZJ6.2B T-77
D10		3S003480	LED,LSE2040 ORG
FL1,2		3E0117500A	DISPLAY,HNA-16MM23 RW(L)
G1		3E0019900A	MAIN GND WIRE ASSY
P2		3E010370	CONNECT PLUG,B5B-PH-K-S
P3		3E010410	CONNECT PLUG,B9B-PH-K-S
P4		3E003880	CONNECT PLUG,B9B-PH RED
P5		3E010400	CONNECT PLUG,B8B-PH-K-S
P6		3E010360	CONNECT PLUG,B4B-PH-K-S
P7		3E010430	CONNECT PLUG,B11B-PH-K-S
P8		3E010450	CONNECT PLUG,B13B-PH-K-S
Q10		3S000291	TR,DTC124ES TP
SW10-16		3E002070	SW,TACT SKQSAB HMR-187
U1,2		3S00487-00A	IC,CXP82040-137Q
U3		3S003254	IC,BR93LC46RF-WE2 SMT TAP
X1,2		3E011740	RESONATOR,CST10.00MTW

GATHER A PCB ASSY

REF.NO.		PARTS NO.	DESCRIPTION
		*3E9536600B	PCB ASSY,GATHER A
			PCB ASSY,FRONT2
		3M0124000A	SPACER,LED L=2.5
D20-24		3S003480	LED,LSE2040 ORG
D40		3S003480	LED,LSE2040 ORG
P10		3E0174700A	HARN ASSY,13P F1F2
P9		3E0174800A	HARN ASSY,11P F1F2
Q20-24		3S000291	TR,DTC124ES TP
Q40		3S000291	TR,DTC124ES TP
SW20-26		3E002070	SW,TACT SKQSAB HMR-187
SW27		3E017270	ENCODER,EC11E15244L15 30C
SW28-32		3E002070	SW,TACT SKQSAB HMR-187
SW40-47		3E002070	SW,TACT SKQSAB HMR-187
SW48		3E017270	ENCODER,EC11E15244L15 30C
SW49-55		3E002070	SW,TACT SKQSAB HMR-187
			PCB ASSY,PHONE
J571		3E002160	JACK,JY-6313-01-030
P571		3E0174200A	HARNESS ASSY,9P MPS
P572		3E0174100A	HARNESS ASSY,3P MP1
S571		3E007360	SW,ROTARY SRBM13N
VR571		3R007950	VAR RES,RK09K12AW/C50KAx2
			PCB ASSY,P-SW
C1	⚠	3E004300	S.KILLER,CS12-F2GA472MYAS
P1		3E013990	CONNECTOR,B 2P3S-VH
SW1	⚠	3E017720	SW,POWER SDDLB13300

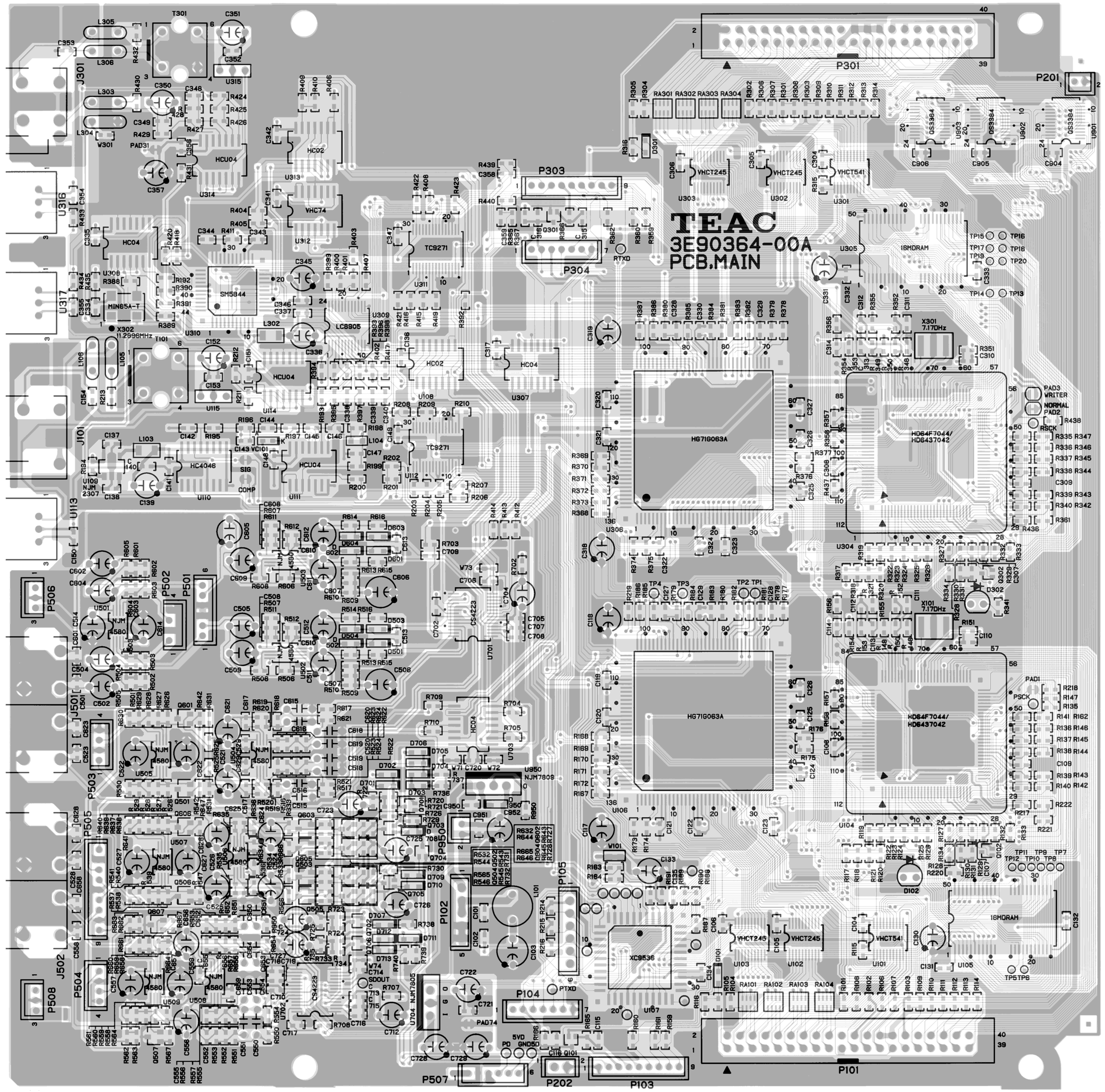
GATHER A PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
		PCB ASSY,VR
P591	3E0174000A	HARNESS ASSY,6P MV RW402
VR591	3R007960	VAR RES,RK16312L20 10KAx2
VR592	3R007970	VAR RES,RK16312C-T 10KBx2
		PCB ASSY,KEYBOARD
G71	3E0019900A	MAIN GND WIRE ASSY
J71	3E017300	CONNECTOR,DIN 6P JY-5017
P71	3E0174900A	HARNESS ASSY,6P F1K RW402
U71	3S003074	IC,TC74HC125AF(EL) SMT.TA
		PCB ASSY,CONTROL
D801	3S003451	ZD,MTZJ2.7B T-77
D802-809	3S000241	D,1SS133 T-77
J801	3E002130	JACK,MINI JY-3550-01-030
P801	3E0175000A	HARNESS ASSY,7P F1C
P802	3E016320	D-SUB 25P,DB-25SLUM IN/IN
Q801-806	3S000291	TR,DTC124ES TP
TH801	E0039030	CKT PTCT,RXE017
U801	3S003384	IC,CXA1511M-T4
U802	3E013130	FILTER,EMT103DT
U803	3E011830	FILTER,EMT470BT
U804	3S003350	IC,TC74HC595AP
U805	3S003340	IC,TC74HC165AP
U806-811	3E013130	FILTER,EMT103DT

GATHER B PCB ASSY

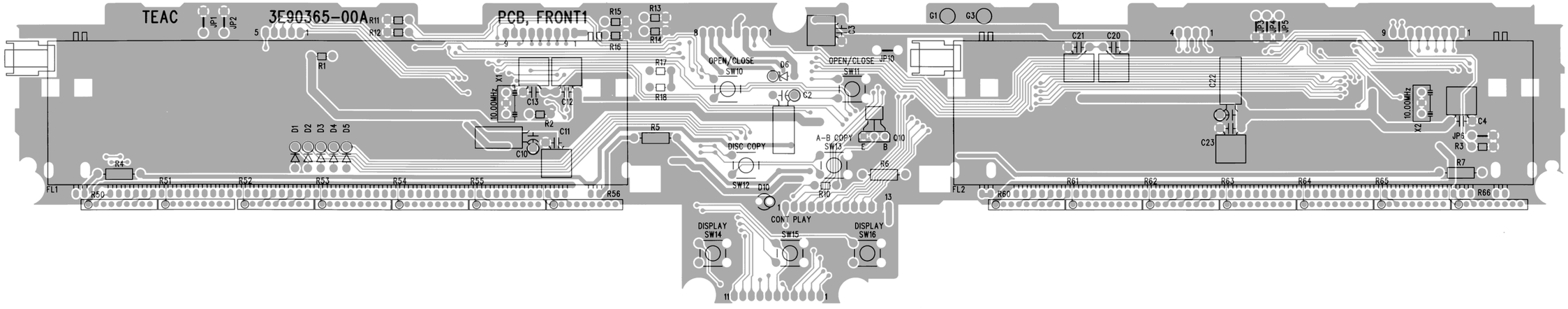
REF.NO.	PARTS NO.	DESCRIPTION
	*3E9536200B	PCB ASSY,GATHER B
		PCB ASSY,BAL
R306,406	R00978500A	RES,ARRY,M-6277
R506,606	R00978500A	RES,ARRY,M-6277
J101,201	3E010320	JACK,XLR NC3FAH1
J301,401	3E017310	PLUG,XLR M JY-5032A-030
J501,601	3E017310	PLUG,XLR M JY-5032A-030
L101,201	3E011820	FB,FBR07HA850SB-00
L102,202	3E011820	FB,FBR07HA850SB-00
L301,401	3E011820	FB,FBR07HA850SB-00
L302,402	3E011820	FB,FBR07HA850SB-00
L501,601	3E011820	FB,FBR07HA850SB-00
L502,602	3E011820	FB,FBR07HA850SB-00
P1	3E0174500A	HARNESS ASSY,4P MB1
P2	3E0174400A	HARNESS ASSY,4P MB02
P3	3E0174300A	HARNESS ASSY,4P MB01
P4	3E0174600A	HARNESS ASSY,3P MBP
U1-5	3S004860	IC,NJM4580L (SIP)

MAIN PCB



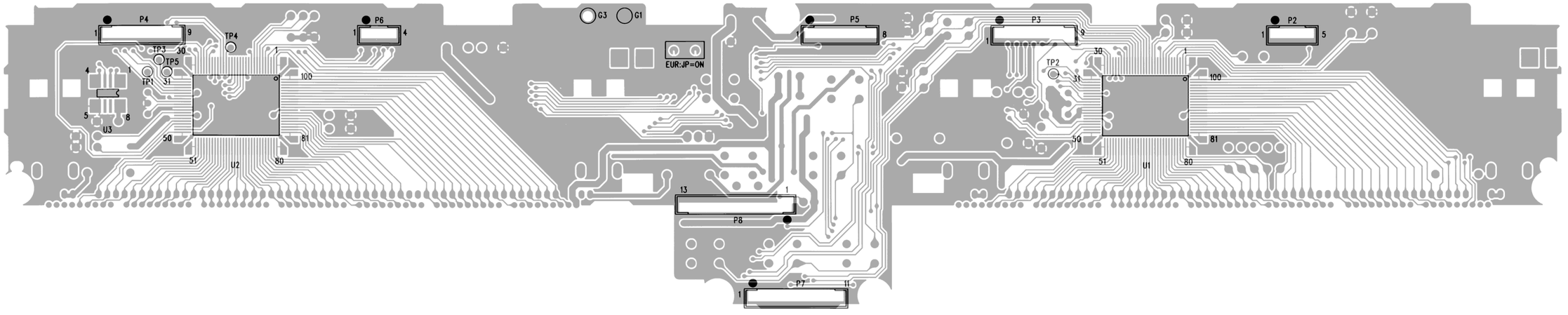
FRONT1 PCB

SIDE A

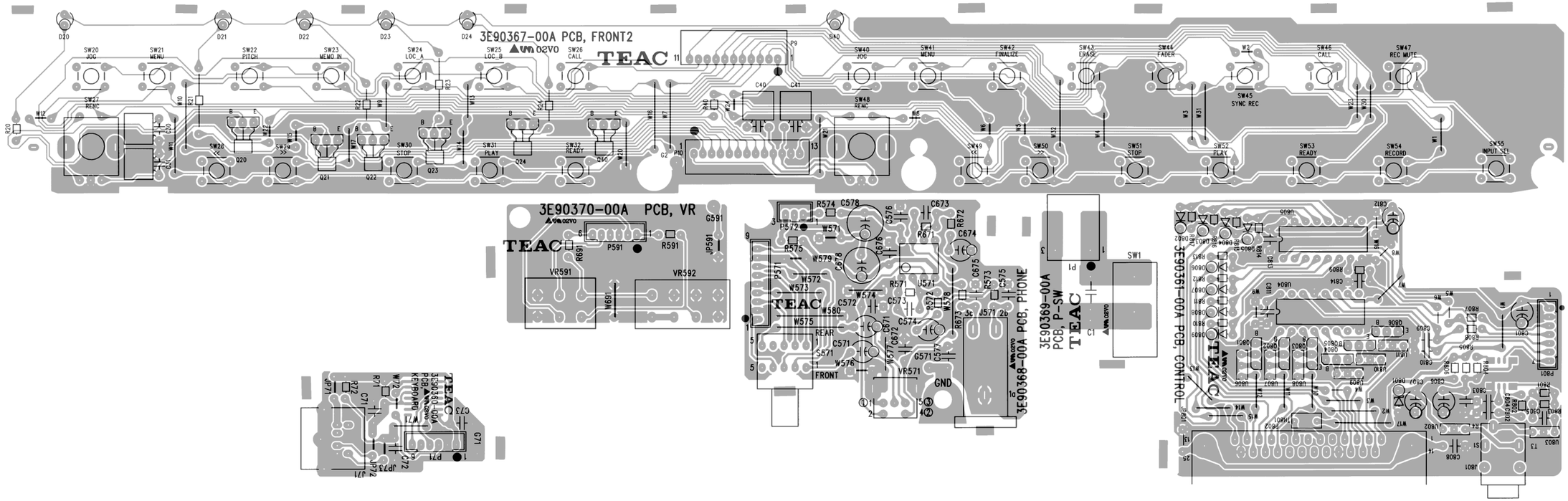


FRONT1 PCB

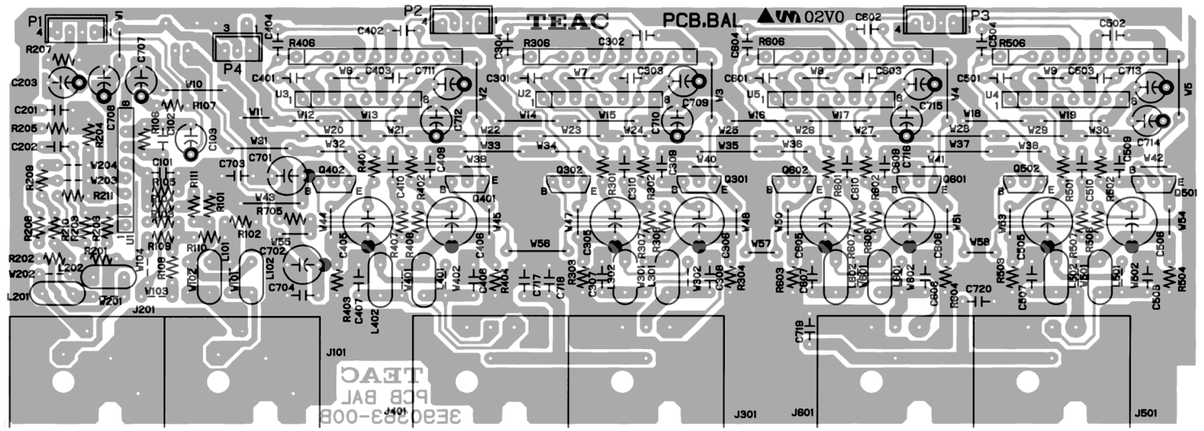
SIDE B



GATHER A PCB (FRONT2 PCB, PHONE PCB, P-SW PCB, VR PCB, KEYBOARD PCB, CONTROL PCB)



BAL PCB



7. INCLUDED ACCESSORIES
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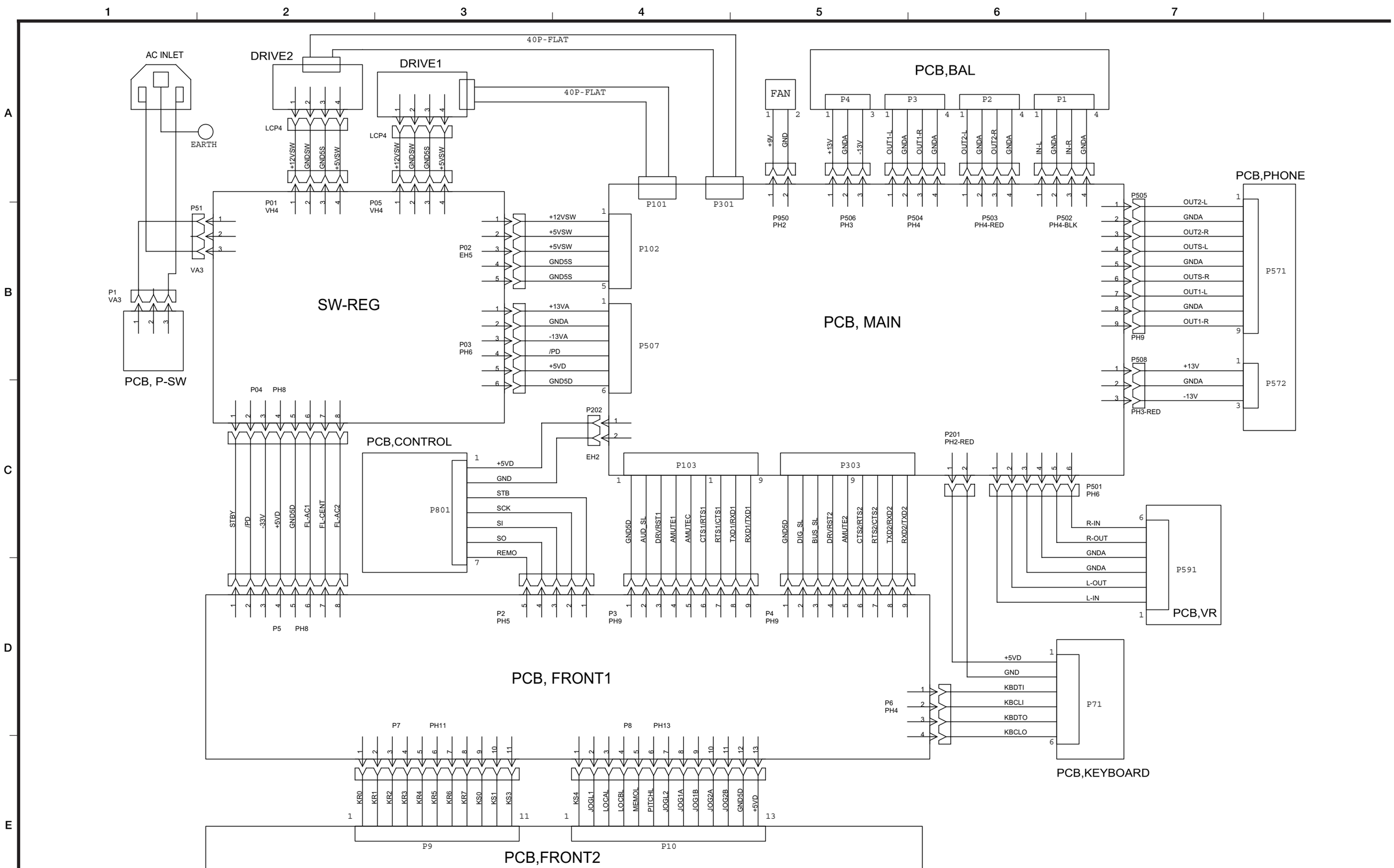
INCLUDED ACCESSORIES

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	*D00631500A	OWNER'S MANUAL,JAPANESE [J]	
	*D00631501B	OWNER'S MANUAL,ENGLISH [EXCEPT J]	
	*D00631600A	OWNER'S MANUAL,QSG E [EXCEPT J]	
	*D00631601A	OWNER'S MANUAL,QSG F [E]	
	*D00631602A	OWNER'S MANUAL,QSG G [E]	
	*D00631603A	OWNER'S MANUAL,QSG I [E]	
	*D00631604A	OWNER'S MANUAL,QSG S [E]	
	*3E014140	POWER CORD [J]	
	*3E014150	POWER CORD [US/C]	
	*3E014160	POWER CORD [E]	
	*3E014170	POWER CORD [UK]	
	*3E014180	POWER CORD [A]	
	*E00679800A	REMOTE CONTROL UNIT,RC-RW402	
	3M0028300A	RACK MOUNT SCREW KIT	

SCHEMATIC DIAGRAMS
回路図

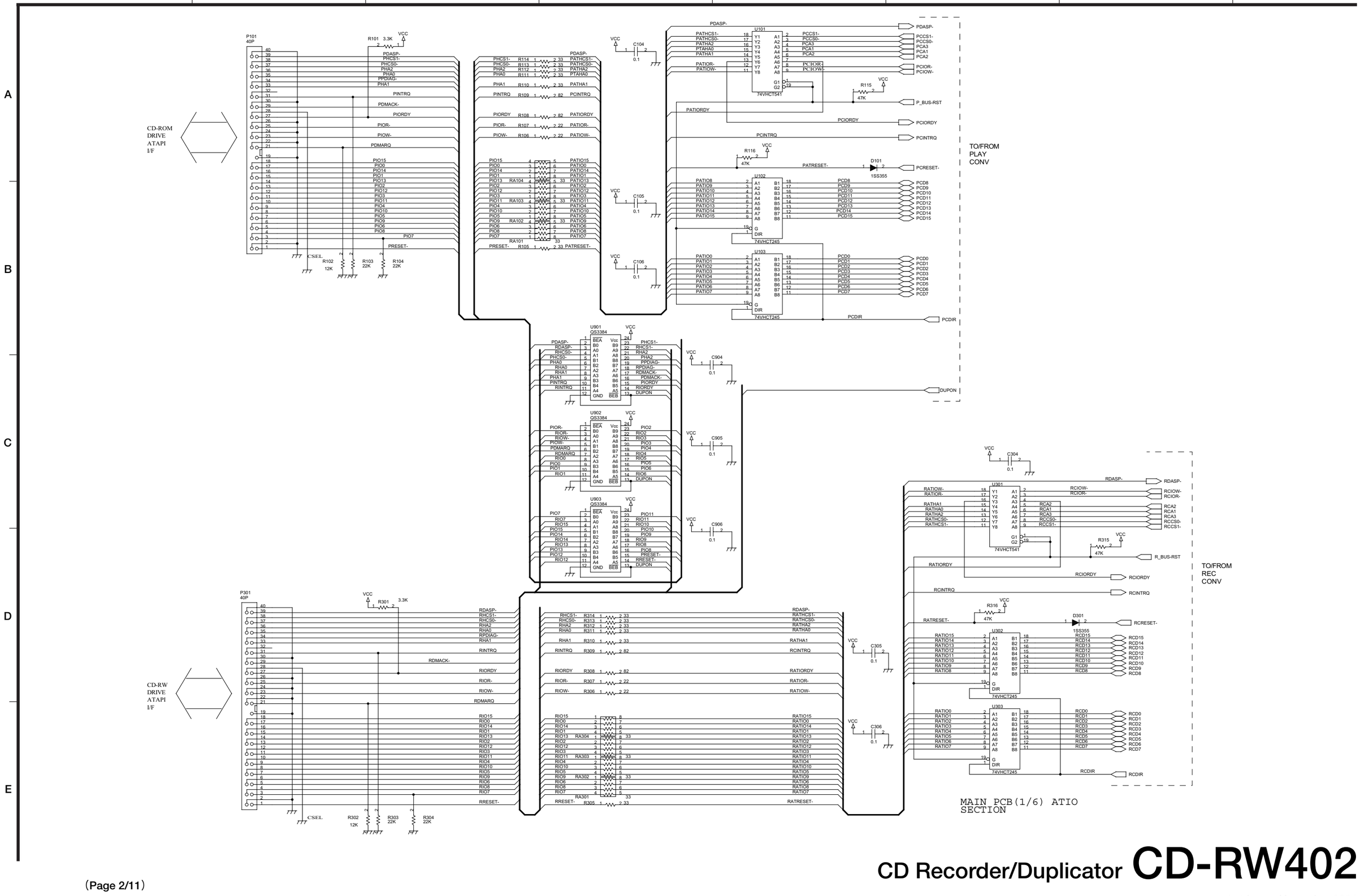
CONTENTS 目次



CD Recorder/Duplicator CD-RW402

1 st Issue; November 2001

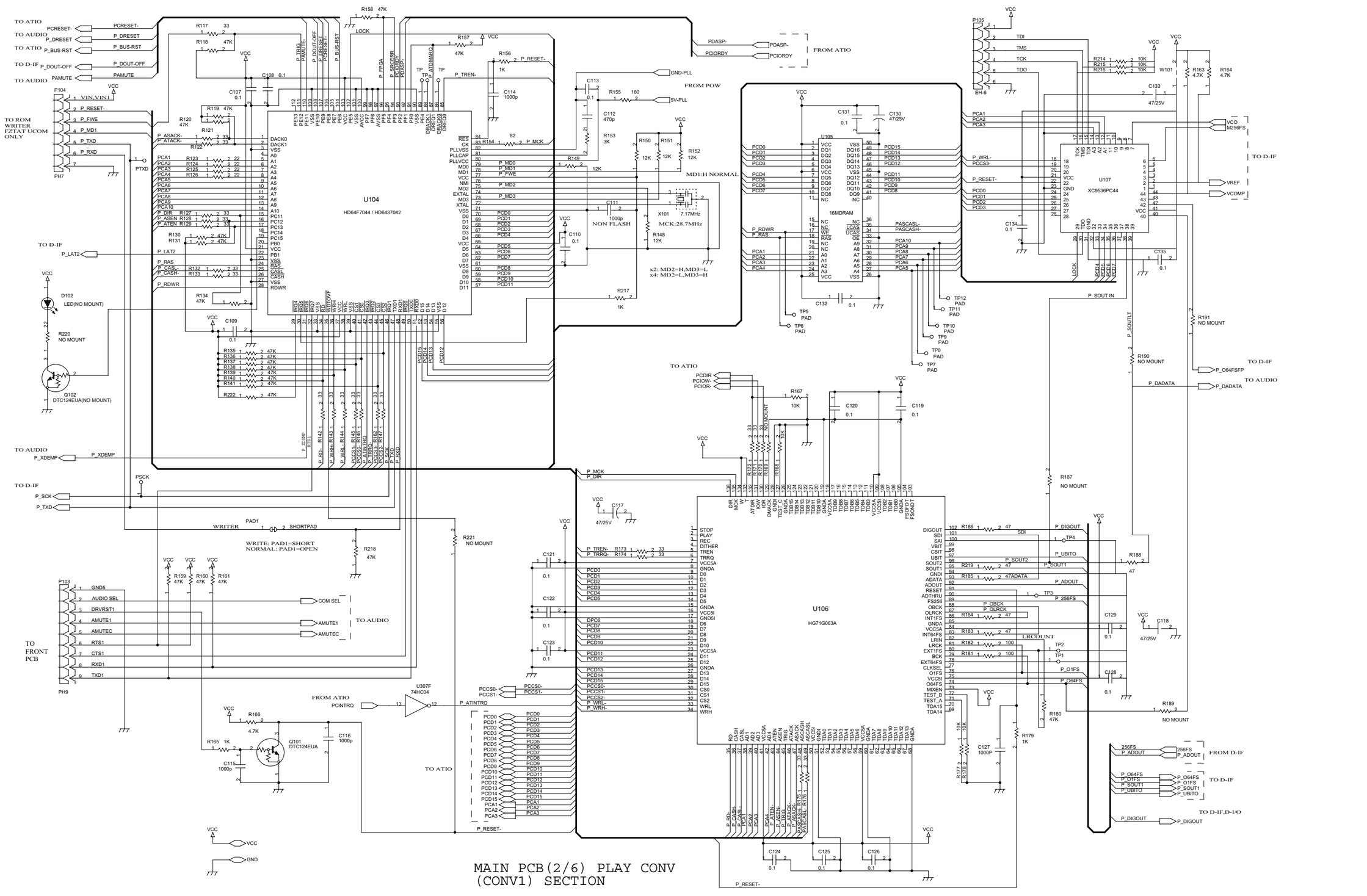
SCHEMATIC DIAGRAM CD-RW402 MAIN PCB (1/6)



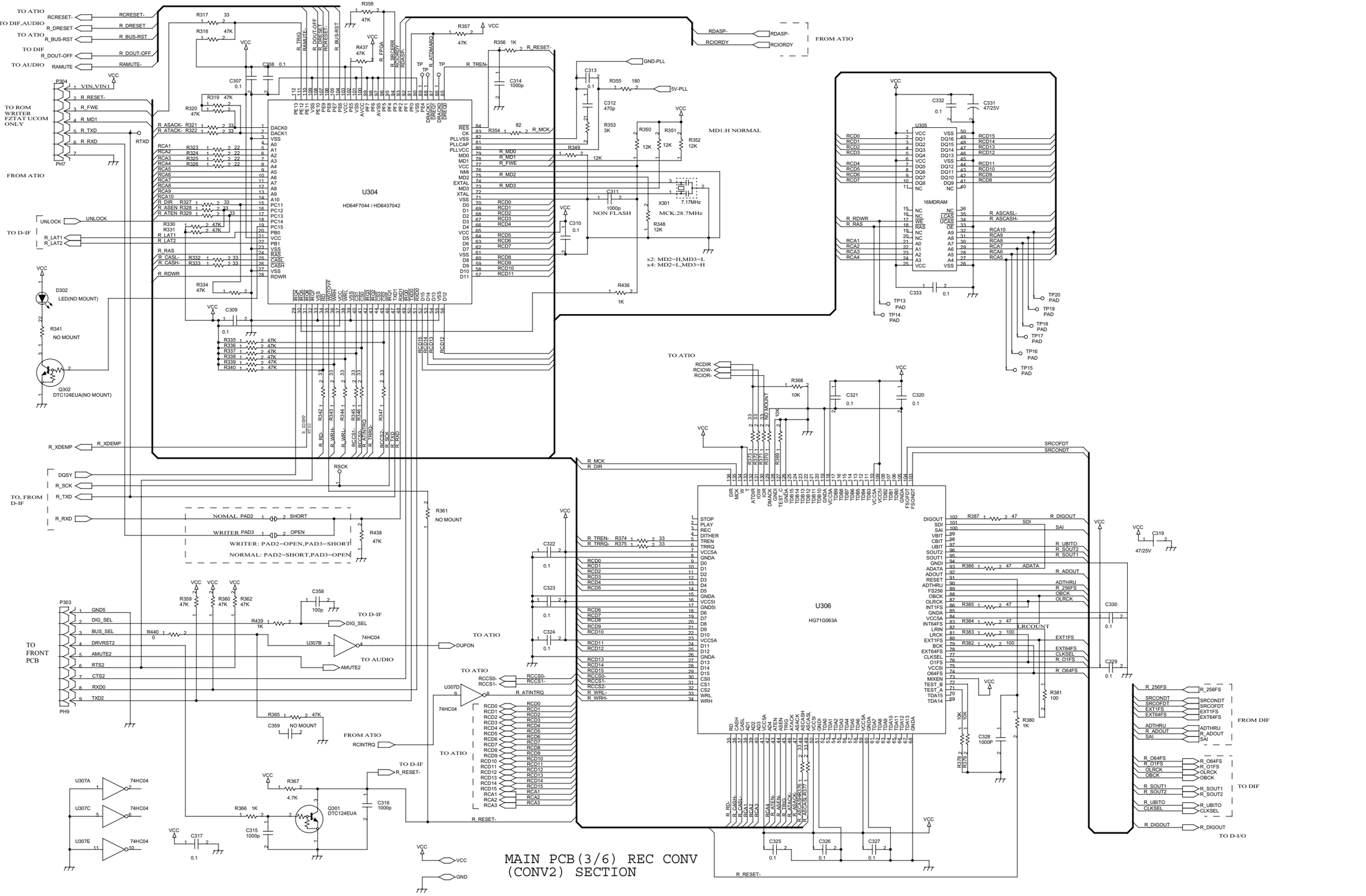
CD Recorder/Duplicator **CD-RW402**

1 st Issue; November 2001

SCHEMATIC DIAGRAM CD-RW402 MAIN PCB (2/6)

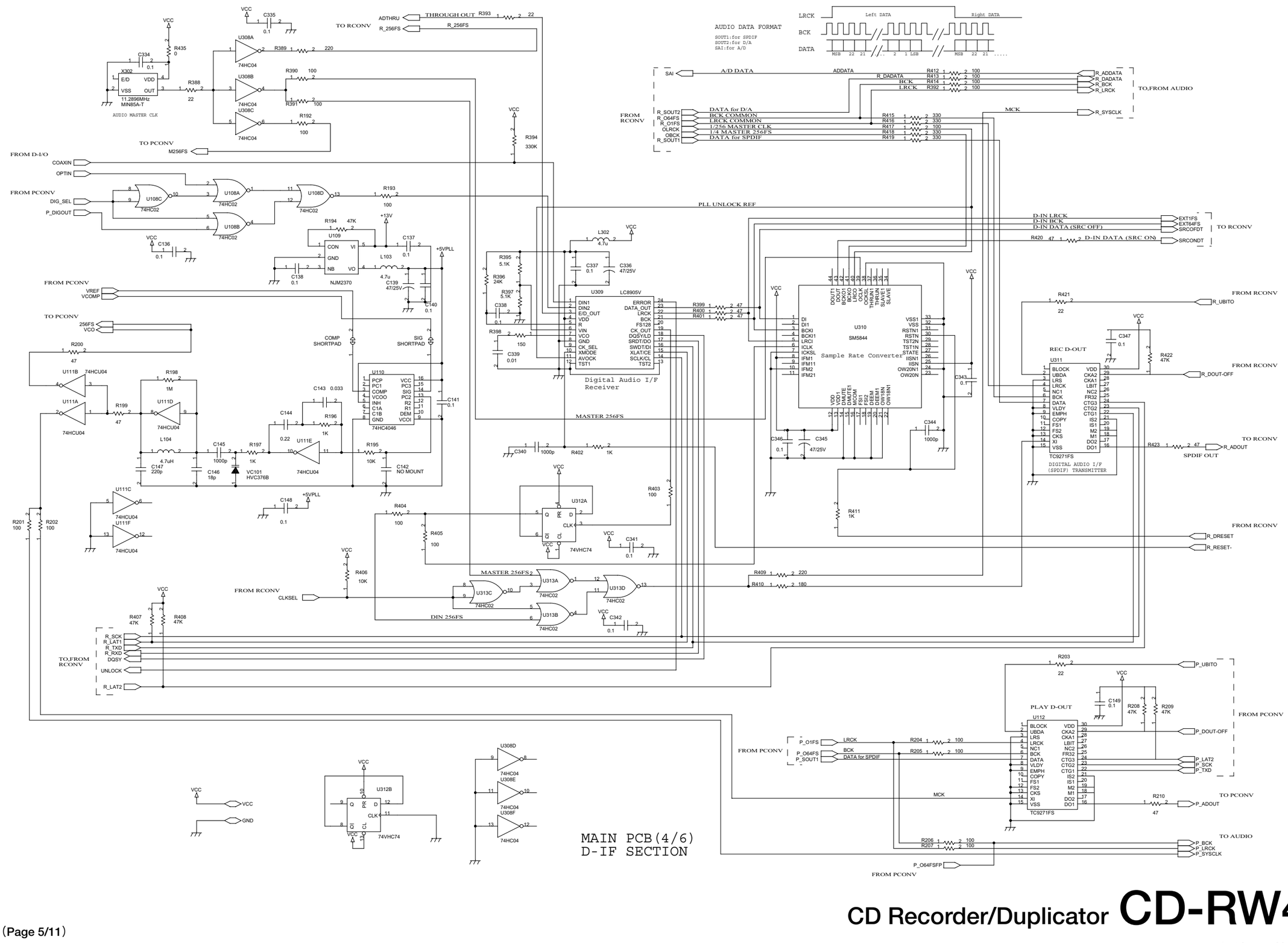


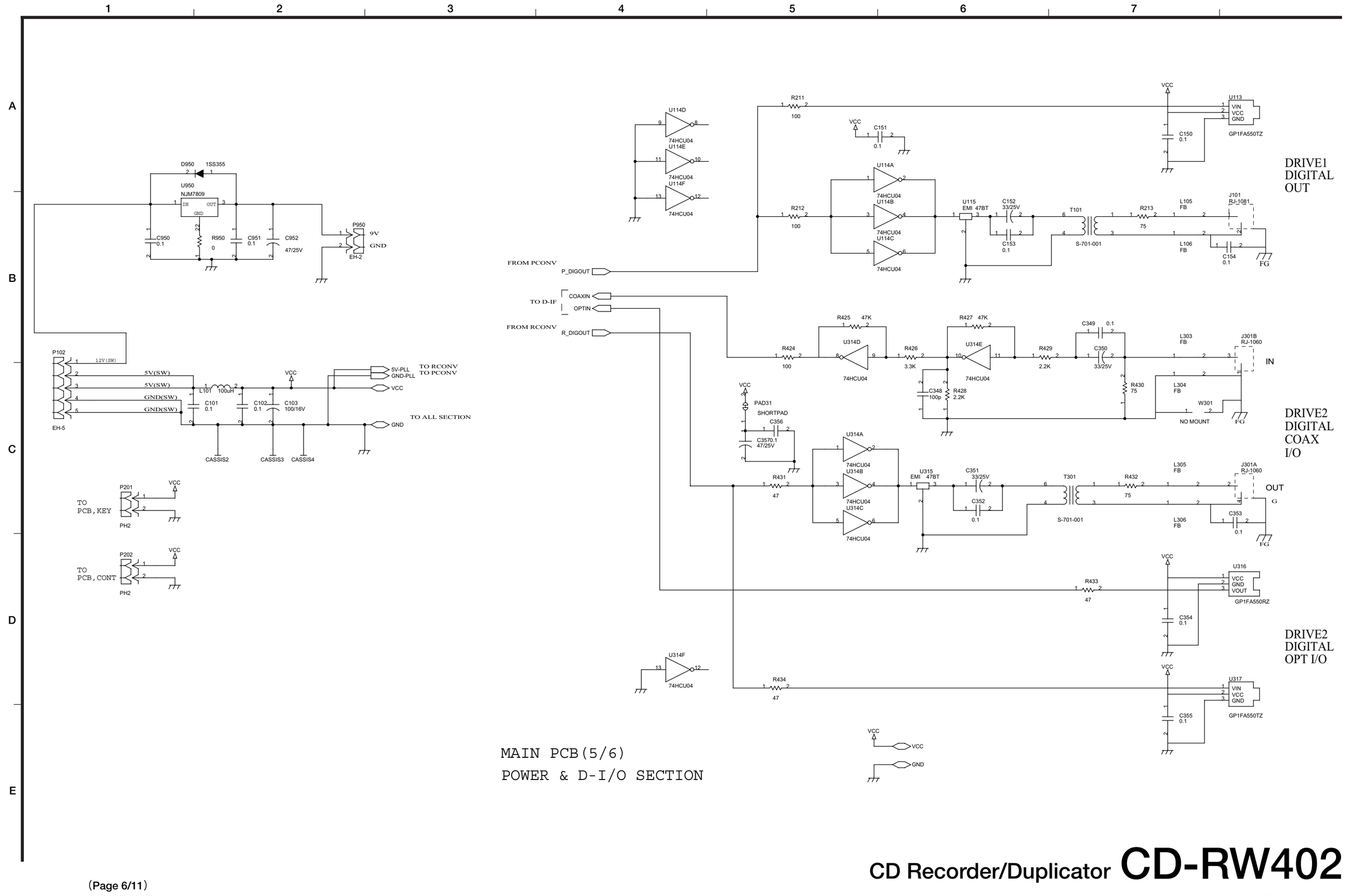
SCHEMATIC DIAGRAM CD-RW402 MAIN PCB (3/6)



1 st Issue; November 2001

SCHEMATIC DIAGRAM CD-RW402 MAIN PCB (4/6)

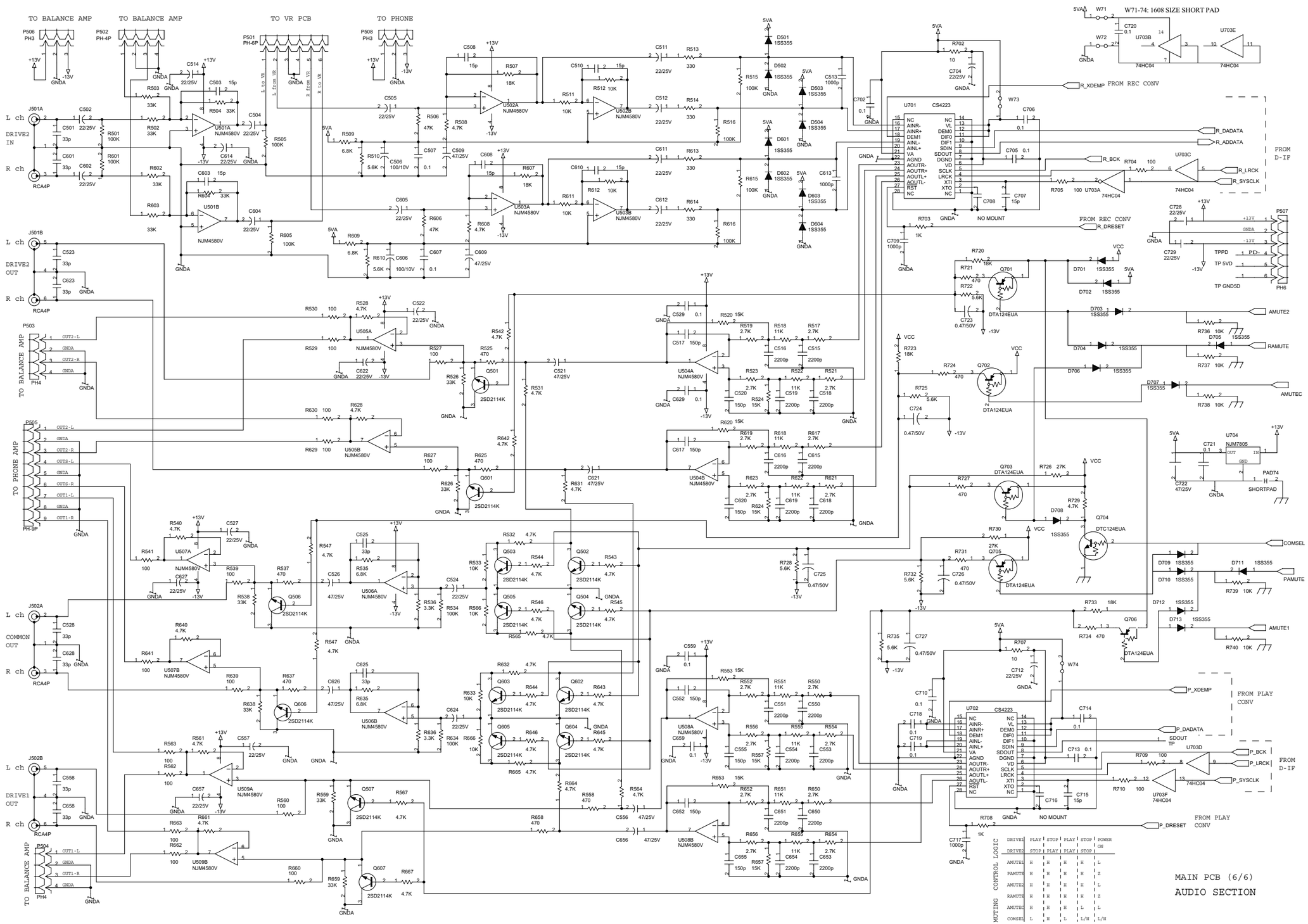




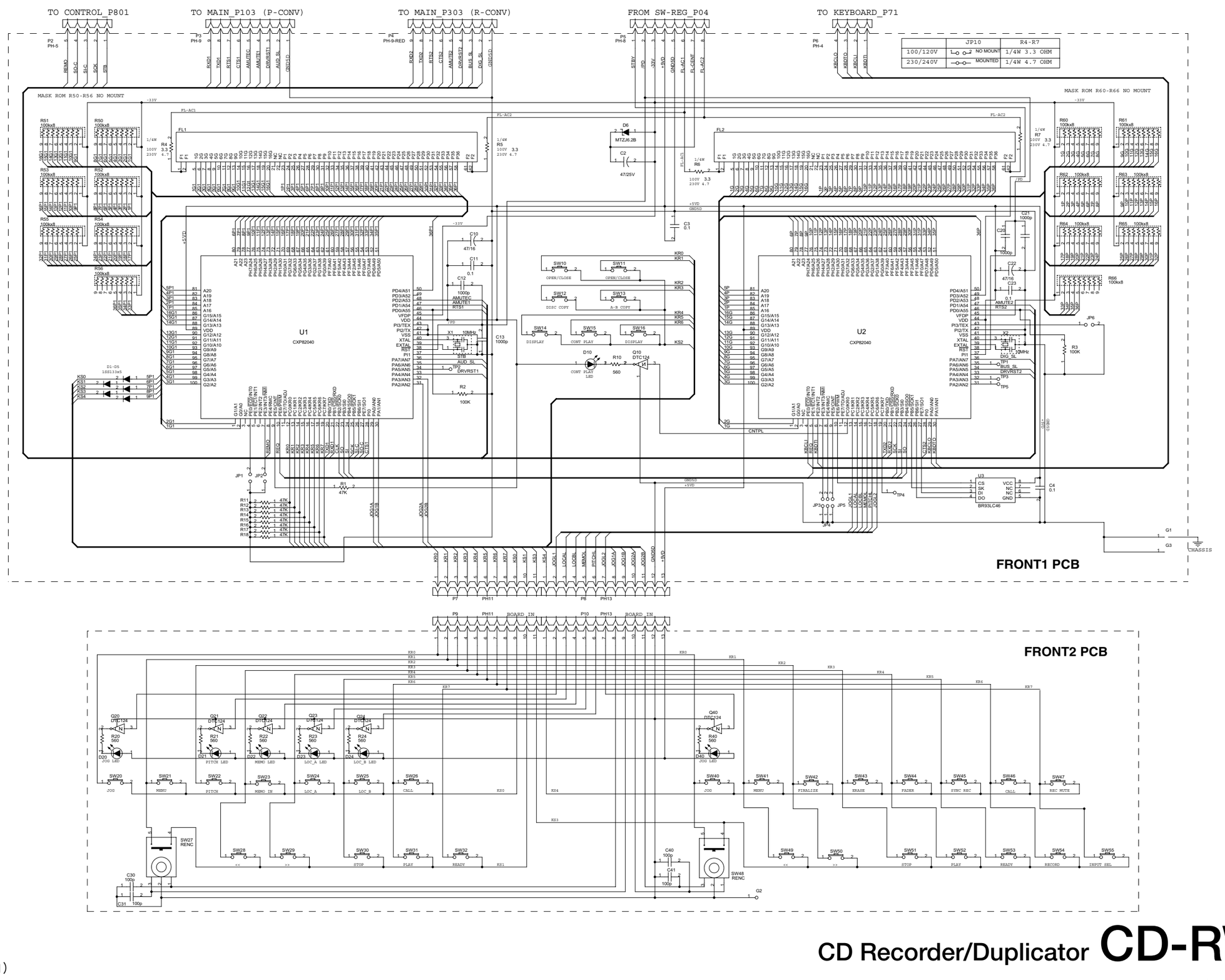
CD Recorder/Duplicator **CD-RW402**

1 st Issue; November 2001

SCHEMATIC DIAGRAM CD-RW402 MAIN PCB (6/6)

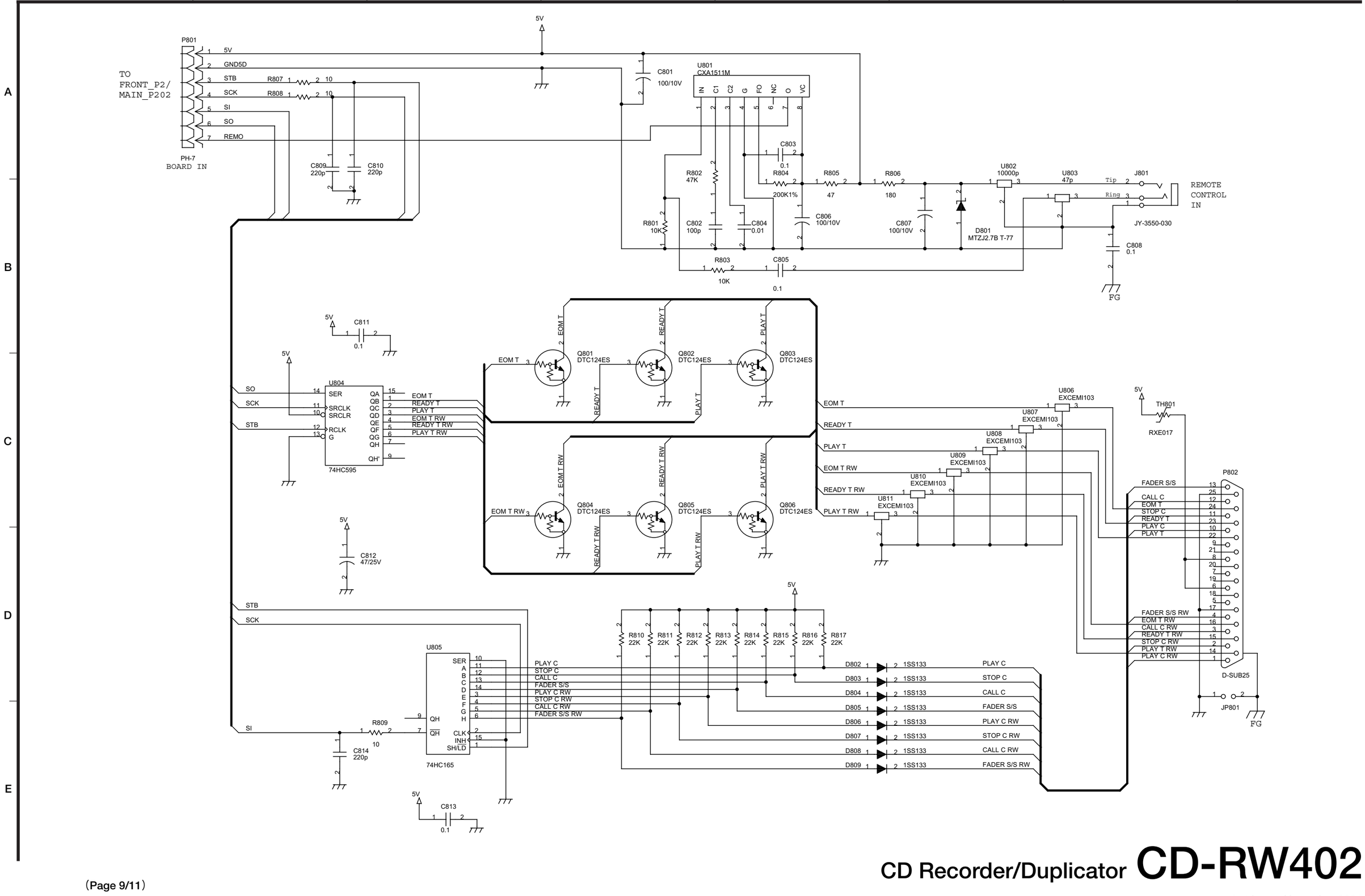


CD Recorder/Duplicator CD-RW402
1 st Issue; November 2001



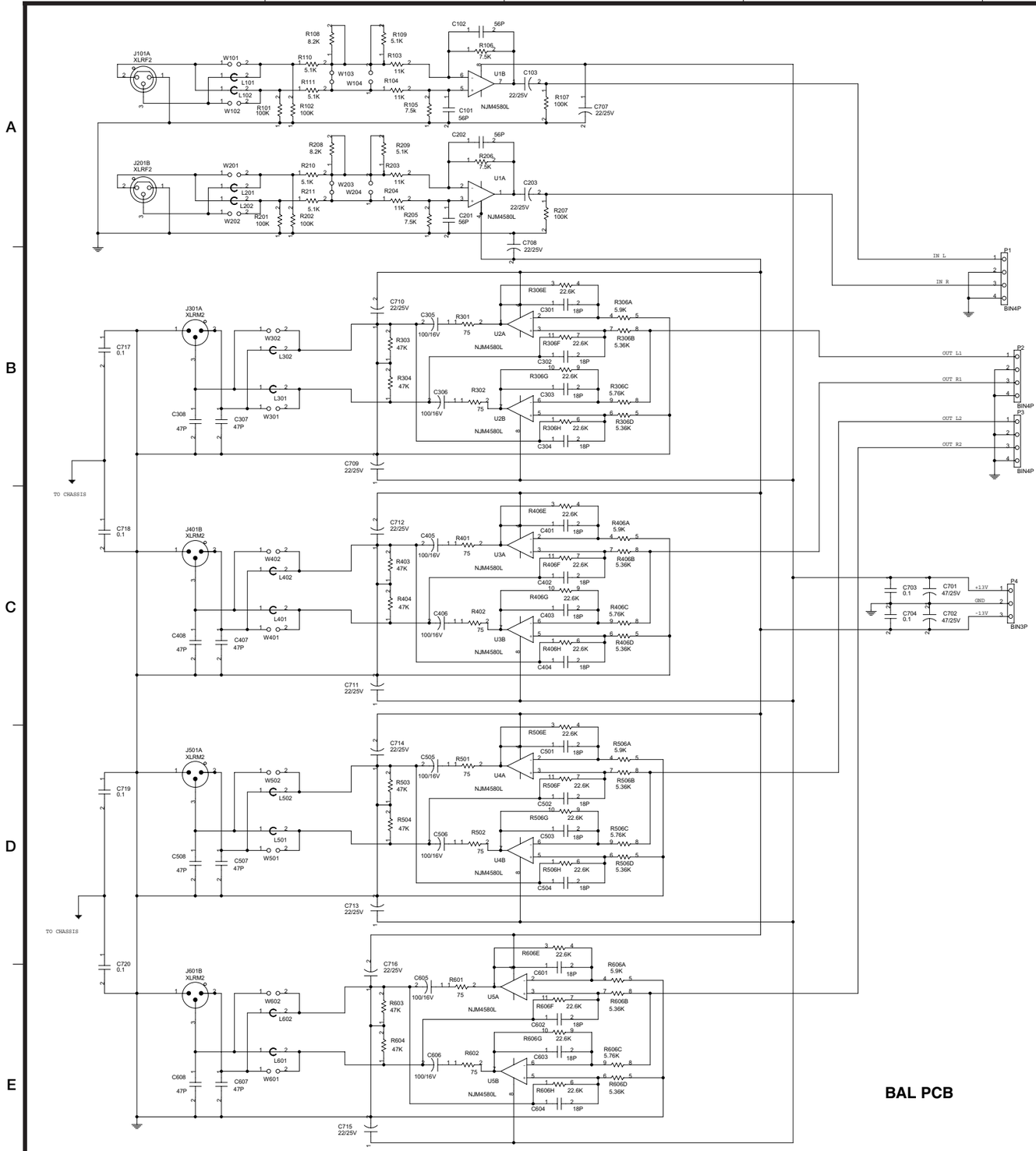
CD Recorder/Duplicator CD-RW402

1 st Issue; November 2001



CD Recorder/Duplicator CD-RW402

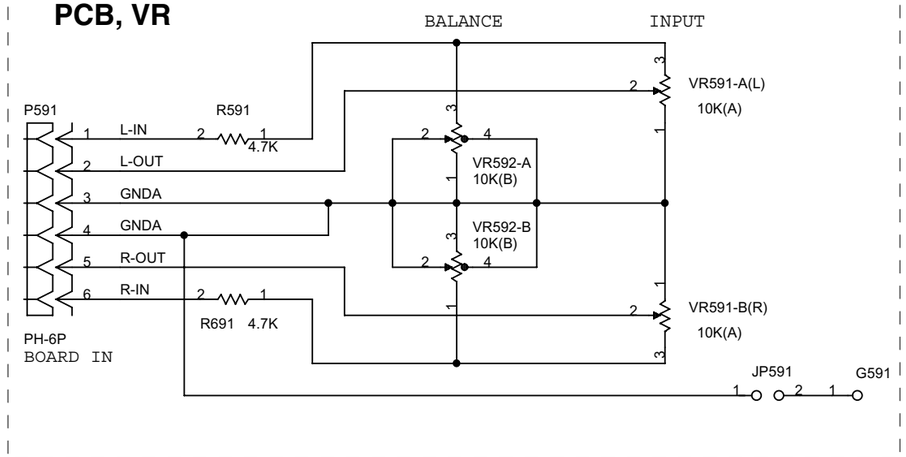
1 st Issue; November 2001



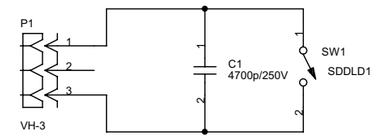
BAL PCB

TO MAIN
P501

PCB, VR

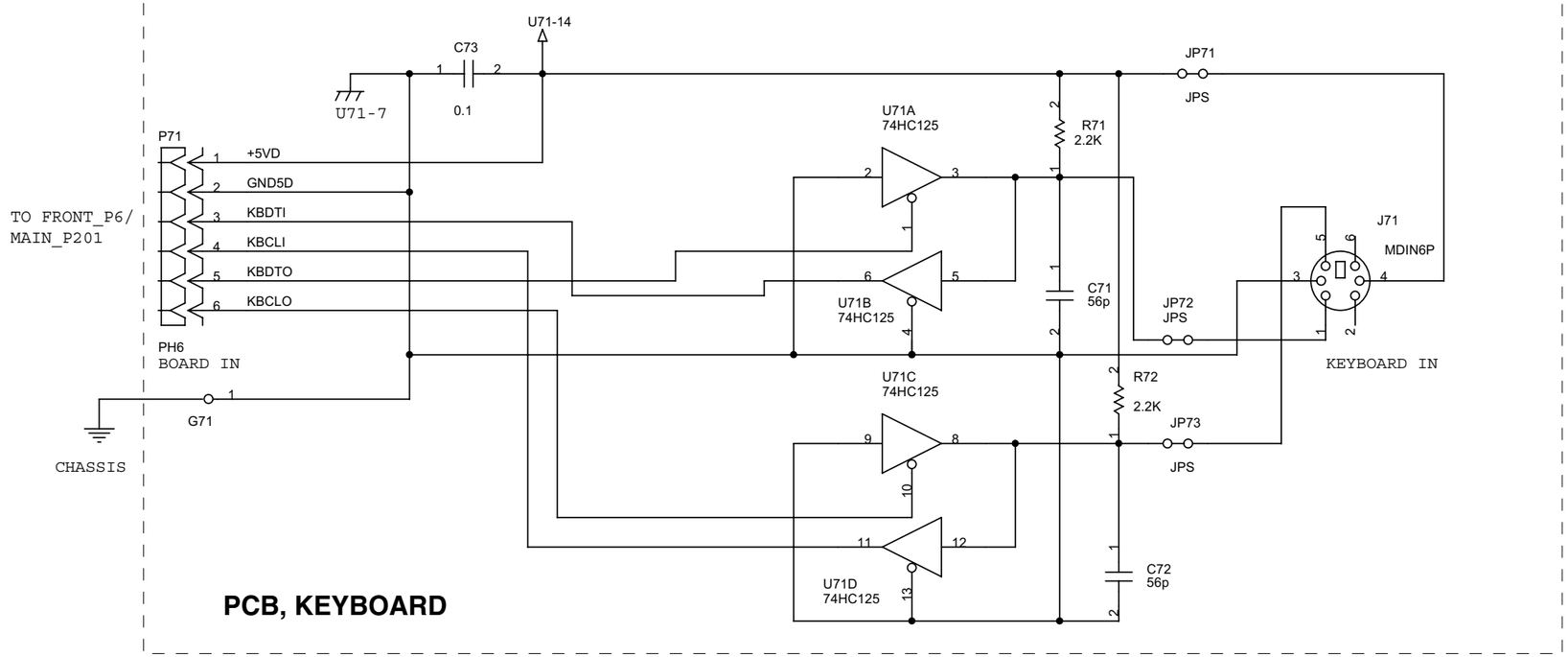


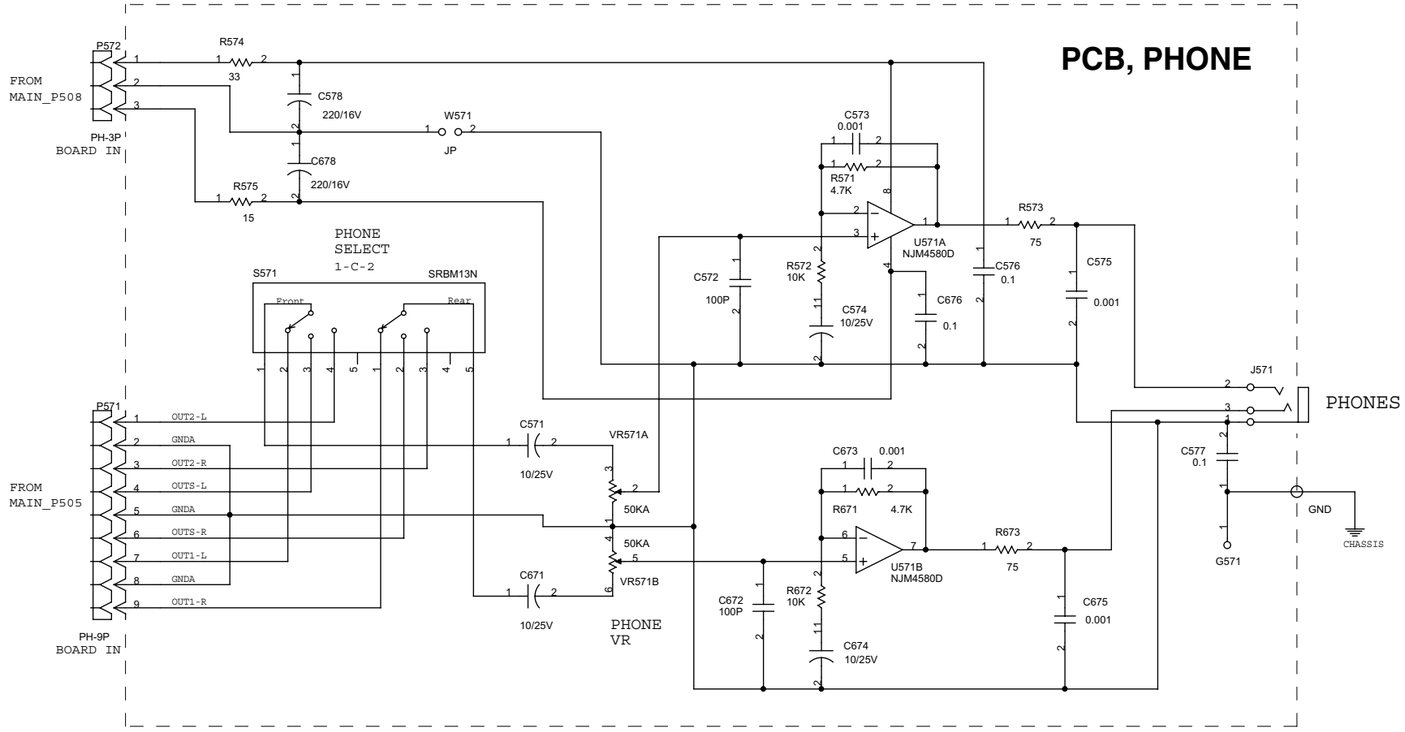
PCB, P-SW



CD Recorder/Duplicator CD-RW402

1 st Issue; November 2001





CD Recorder/Duplicator CD-RW402

1 st Issue; November 2001

CS4223
CS4224

24-Bit 105 dB Audio Codec with Volume Control

Features

- 105 dB Dynamic Range A/D Converters
- 105 dB Dynamic Range D/A Converters
- 110 dB DAC Signal-to-Noise Ratio (EIAJ)
- Analog Volume Control (CS4224 only)
- Differential Inputs / Outputs
- On-chip Anti-aliasing and Output Smoothing Filters
- De-emphasis for 32, 44.1 and 48 kHz
- Supports Master and Slave Modes
- Single +5 V power supply
- On-Chip Crystal Oscillator
- 3 - 5 V Digital Interface

Description

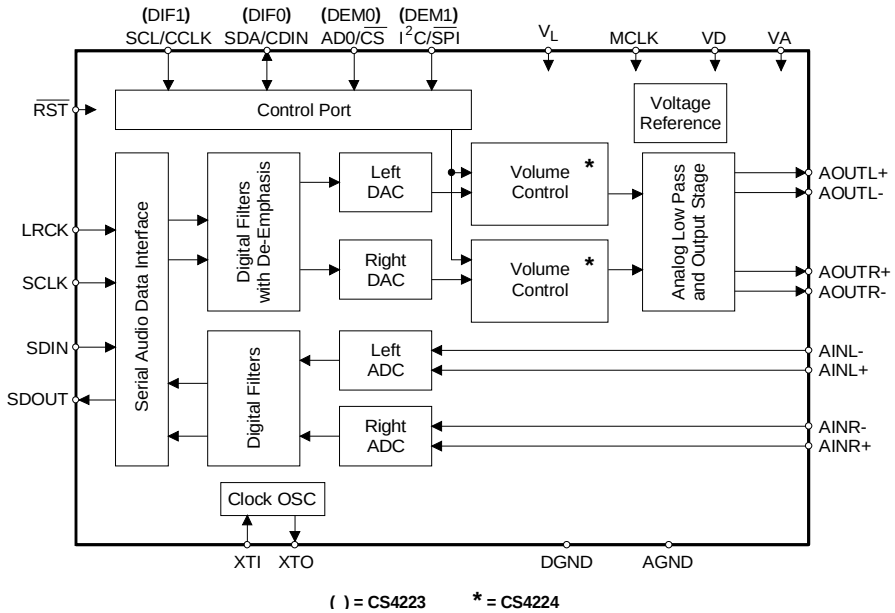
The CS4223/4 is a highly integrated, high performance, 24-bit, audio codec providing stereo analog-to-digital and stereo digital-to-analog converters using delta-sigma conversion techniques. The device operates from a single +5 V power supply, and features low power consumption. Selectable de-emphasis filter for 32, 44.1, and 48 kHz sample rates is also included.

The CS4224 includes an analog volume control capable of 113.5 dB attenuation in 0.5 dB steps. The analog volume control architecture preserves dynamic range during attenuation. Volume control changes are implemented using a "soft" ramping or zero crossing technique.

Applications include digital effects processors, DAT, and multitrack recorders.

ORDERING INFORMATION

CS4223-KS	-10 to +70 °C	28-pin SSOP
CS4223-BS	-40 to +85 °C	28-pin SSOP
CS4224-KS	-10 to +70 °C	28-pin SSOP
CS4224-BS	-40 to +85 °C	28-pin SSOP
CDB4223/4		Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

CIRRUS LOGIC®
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25° C; VA, VD = +5 V; Full Scale Input Sine wave, 997 Hz; Fs = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in Figures 4 and 5; SPI® mode, Format 0, unless otherwise specified.)

Parameter	Symbol	CS4223/4 - KS			CS4223/4 - BS			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Input Characteristics								
ADC Resolution		-	-	24	-	-	24	Bits
Total Harmonic Distortion	THD	-	0.0014	-	-	0.0014	-	%
Dynamic Range A-weighted unweighted		100 97	105 102	- -	95 92	105 102	- -	dB dB
Total Harmonic Distortion + Noise (Note 1)	THD+N	-	-97	-92	-	-97	-87	dB
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	-	0.1	-	-	0.1	dB
Offset Error with High Pass Filter		-	-	0	-	-	0	LSB
Full Scale Input Voltage (Differential)		1.9	2.0	2.1	1.9	2.0	2.1	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Input Resistance		10	-	-	10	-	-	kΩ
Input Capacitance		-	-	15	-	-	15	pF
Common Mode Input Voltage		-	2.3	-	-	2.3	-	V
A/D Decimation Filter Characteristics								
Passband (Note 2)		0	-	21.8	0	-	21.8	kHz
Passband Ripple		-	-	±0.01	-	-	±0.01	dB
Stopband (Note 2)		30	-	6114	30	-	6114	kHz
Stopband Attenuation (Note 3)		80	-	-	80	-	-	dB
Group Delay (Fs = Output Sample Rate) (Note 4)	t_{gd}	-	15/Fs	-	-	15/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0	-	-	0	µs
High Pass Filter Characteristics								
Frequency Response -3 dB (Note 2) -0.1 dB		- -	3.7 20	- -	- -	3.7 20	- -	Hz Hz
Phase Deviation @ 20 Hz (Note 2)		-	10	-	-	10	-	Degree
Passband Ripple		-	-	0	-	-	0	dB

Notes:
1. Referenced to typical full-scale differential input voltage (2 Vrms).
2. Filter characteristics scale with output sample rate. For output sample rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.625x Fs.
3. The analog modulator samples the input at 6.144 MHz for an Fs equal to 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.8 kHz where n = 0,1,2,3...).
4. Group delay for Fs = 48 kHz, t_{gd} = 15/48 kHz = 312 µs.

ANALOG CHARACTERISTICS (CONTINUED)

Parameter	Symbol	CS4223/4 - KS			CS4223/4 - BS			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Output Characteristics - Minimum Attenuation, 10 kΩ, 100 pF load; unless otherwise specified.								
DAC Resolution		-	-	24	-	-	24	Bits
Signal-to-Noise, Idle-Channel Noise (CS4224 only) DAC muted, A-weighted		102	110	-	97	110	-	dB
Dynamic Range DAC not muted, A-weighted		100	105	-	95	105	-	dB
DAC not muted, unweighted		97	102	-	92	102	-	dB
Total Harmonic Distortion	THD	-	0.0014	-	-	0.0014	-	%
Total Harmonic Distortion + Noise	THD+N	-	-97	-92	-	-97	-87	dB
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	-	0.1	-	-	0.1	dB
Attenuation Step Size All Outputs		0.35	0.5	0.65	0.35	0.5	0.65	dB
Programmable Output Attenuation Span		110	113.5	-	110	113.5	-	dB
Differential Offset Voltage		-	±10	-	-	±10	-	mV
Common Mode Output Voltage		-	2.4	-	-	2.4	-	V
Full Scale Output Voltage		1.8	1.9	2.0	1.8	1.9	2.0	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Out-of-Band Energy Fs/2 to 2 Fs		-	-60	-	-	-60	-	dBFs
Analog Output Load Resistance		10	-	-	10	-	-	kΩ
Capacitance		-	-	100	-	-	100	pF
Combined Digital and Analog Filter Characteristics								
Frequency Response10 Hz to 20 kHz		-	±0.1	-	-	±0.1	-	dB
Deviation from Linear Phase		-	±0.5	-	-	±0.5	-	Degree
Passband: to 0.01 dB corner (Notes 5 and 6)		0	-	21.8	0	-	21.8	kHz
Passband Ripple (Note 6)		-	-	±0.01	-	-	±0.01	dB
Stopband (Notes 5 and 6)		26.2	-	-	26.2	-	-	kHz
Stopband Attenuation (Note 7)		70	-	-	70	-	-	dB
Group Delay (Fs = Input Word Rate)	t_{gd}	-	16/Fs	-	-	16/Fs	-	s
Power Supply								
Power Supply Current VA		-	46	60	-	46	60	mA
VD		-	9	20	-	9	20	mA
VL		-	3	5	-	3	5	mA
Total Power Down		-	0.4	-	-	0.4	-	mA
Power Supply Rejection Ratio 1 kHz		-	65	-	-	65	-	dB

Notes: 5. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.5465x Fs.

6. Digital filter characteristics.

7. Measurement bandwidth is 10 Hz to 3 Fs.

DIGITAL CHARACTERISTICS (T_A = 25° C; VA, VD = 4.75V - 5.25V)

Parameter		Symbol	Min	Max	Unit
High-level Input Voltage	VL = 5V	V_{IH}	2.8	VL + 0.3	V
	VL = 3V	V_{IH}	2.0	VL + 0.3	V
Low-level Input Voltage		V_{IL}	-0.3	0.8	V
High-level Output Voltage at I_O = -2.0 mA		V_{OH}	VL - 1.0	-	V
Low-level Output Voltage at I_O = 2.0 mA		V_{OL}	-	0.5	V
Input Leakage Current	Digital Inputs		-	10	µA
Output Leakage Current	High Impedance Digital Outputs		-	10	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Unit
Power Supplies	Digital	VD	-0.3	6.0	V
	Analog	VA	-0.3	6.0	V
Input Current	(Note 8)		-	±10	mA
Analog Input Voltage	(Note 9)		-0.7	VA + 0.7	V
Digital Input Voltage	(Note 9)		-0.7	VD + 0.7	V
Ambient Temperature	Power Applied		-55	+125	°C
Storage Temperature			-65	+150	°C

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	Digital	VD	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
	Digital	VL	2.7	5.0	5.25	V
	| VA - VD |		-	-	0.4	V
Ambient Operating Temperature	Commercial (KS)	T_{AC}	-10	25	70	°C
	Industrial (BS)	T_{AI}	-40	25	85	°C

Notes: 8. Any pin except supplies. Transient currents of up to 100 mA on the analog input pins will not cause SCR latch-up.

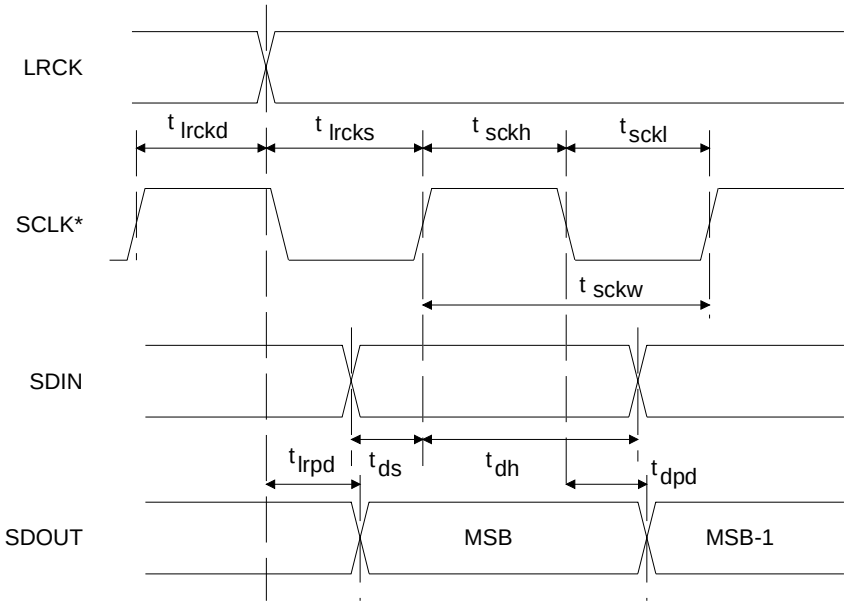
9. The maximum over or under voltage is limited by the input current.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = 25° C; VA, VD = 4.75 V - 5.25 V; outputs loaded with 30 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Audio ADC's and DAC's Sample Rate		Fs	4	-	50	kHz
XTI Frequency	XTI = 256, 384, or 512 Fs		1.024	-	26	MHz
XTI Pulse Width High	XTI = 512 Fs		13	-	-	ns
	XTI = 384 Fs		21	-	-	ns
	XTI = 256 Fs		31	-	-	ns
XTI Pulse Width Low	XTI = 512 Fs		13	-	-	ns
	XTI = 384 Fs		21	-	-	ns
	XTI = 256 Fs		31	-	-	ns
XTI Jitter Tolerance			-	500	-	psRMS
$\overline{\text{RST}}$ Low Time	(Note 10)		10	-	-	ms
SCLK falling edge to SDOUT output valid	DSCK = 0	t_{dpd}	-	-	$\frac{1}{(384)\ Fs} + 20$	ns
LRCK edge to MSB valid		t_{lrpd}	-	-	45	ns
SDIN setup time before SCLK rising edge	DSCK = 0	t_{ds}	25	-	-	ns
SDIN hold time after SCLK rising edge	DSCK = 0	t_{dh}	25	-	-	ns
SCLK Period		t_{sckw}	$\frac{1}{(128)\ Fs}$	-	-	ns
SCLK High Time		t_{sckh}	40	-	-	ns
SCLK Low Time		t_{sckl}	40	-	-	ns
SCLK rising to LRCK edge	DSCK = 0	t_{lrckd}	35	-	-	ns
LRCK edge to SCLK rising	DSCK = 0	t_{lrcks}	40	-	-	ns

Notes: 10. After powering up the CS4223/4, PDN should be held low for 10 ms to allow the power supply to settle.



*SCLK shown for DSCK = 0, SCLK inverted for DSCK = 1.

Figure 1. Serial Audio Port Data I/O Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE (CS4224)

(T_A = 25° C; VA, VD = 4.75 V - 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VD; C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SPI Mode (SPI/I2C = 0)					
CCLK Clock Frequency		f_{sck}	-	6	MHz
$\overline{RST}$ rising edge to $\overline{CS}$ falling	(Note 11)	t_{srs}	41	-	µs
CCLK edge to $\overline{CS}$ falling	(Note 12)	t_{spi}	500	-	ns
$\overline{CS}$ High Time between transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ falling to CCLK edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK rising setup time		t_{dsu}	40	-	ns
CCLK rising to DATA hold time	(Note 13)	t_{dh}	15	-	ns
Rise time of CCLK and CDIN	(Note 14)	t_{r2}	-	100	ns
Fall time of CCLK and CDIN	(Note 14)	t_{f2}	-	100	ns

Notes: 11. Not tested but guaranteed by design.

12. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

13. Data must be held for sufficient time to bridge the transition time of CCLK.

14. For F_{SCK} < 1 MHz.

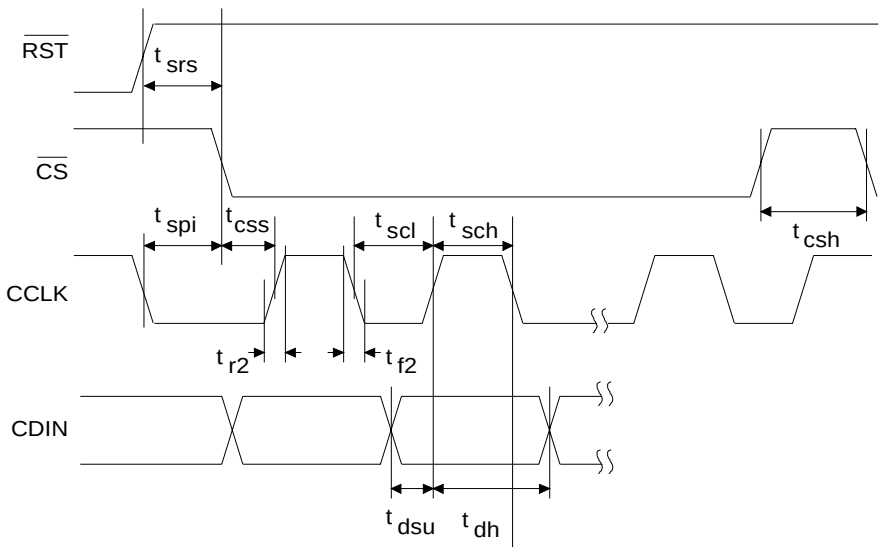


Figure 2. SPI Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I^2C MODE (CS4224)

(T_A = 25° C; VA, VD = 4.75 V - 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VD; C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
I^2C® Mode ($\overline{SPI}$/I2C = 1)				
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ rising edge to Start (Note 15)	t_{irs}	50	-	µs
Bus Free Time between transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low Time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup time for repeated Start Condition	t_{sust}	4.7	-	µs
SDA hold time for SCL falling (Note 16)	t_{hdd}	0	-	µs
SDA setup time to SCL rising	t_{sud}	250	-	ns
Rise time of SCL	t_{rc}	-	25	ns
Fall time of SCL	t_{fc}	-	25	ns
Rise time of SDA	t_{rd}	-	1	µs
Fall time of SDA	t_{fd}	-	300	ns
Setup time for Stop Condition	t_{susp}	4.7	-	µs

Notes: 15. Not tested but guaranteed by design.

16. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

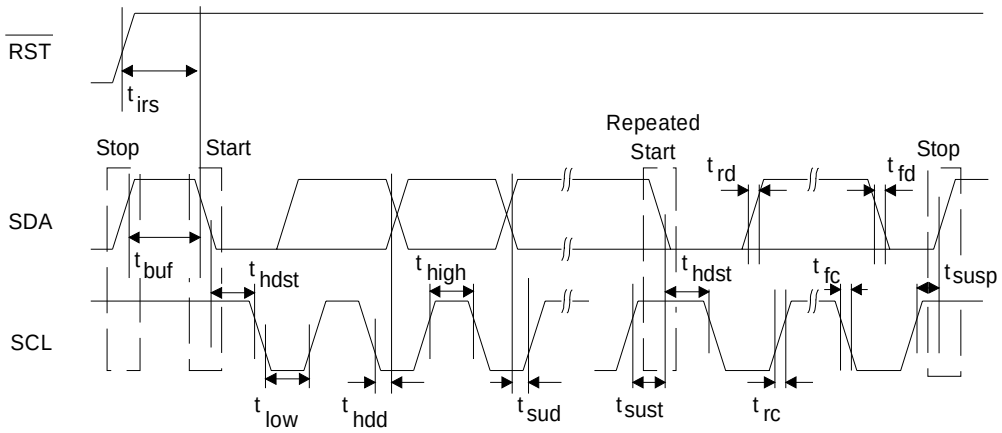


Figure 3. I^2C Control Port Timing

2. TYPICAL CONNECTION DIAGRAM — CS4223

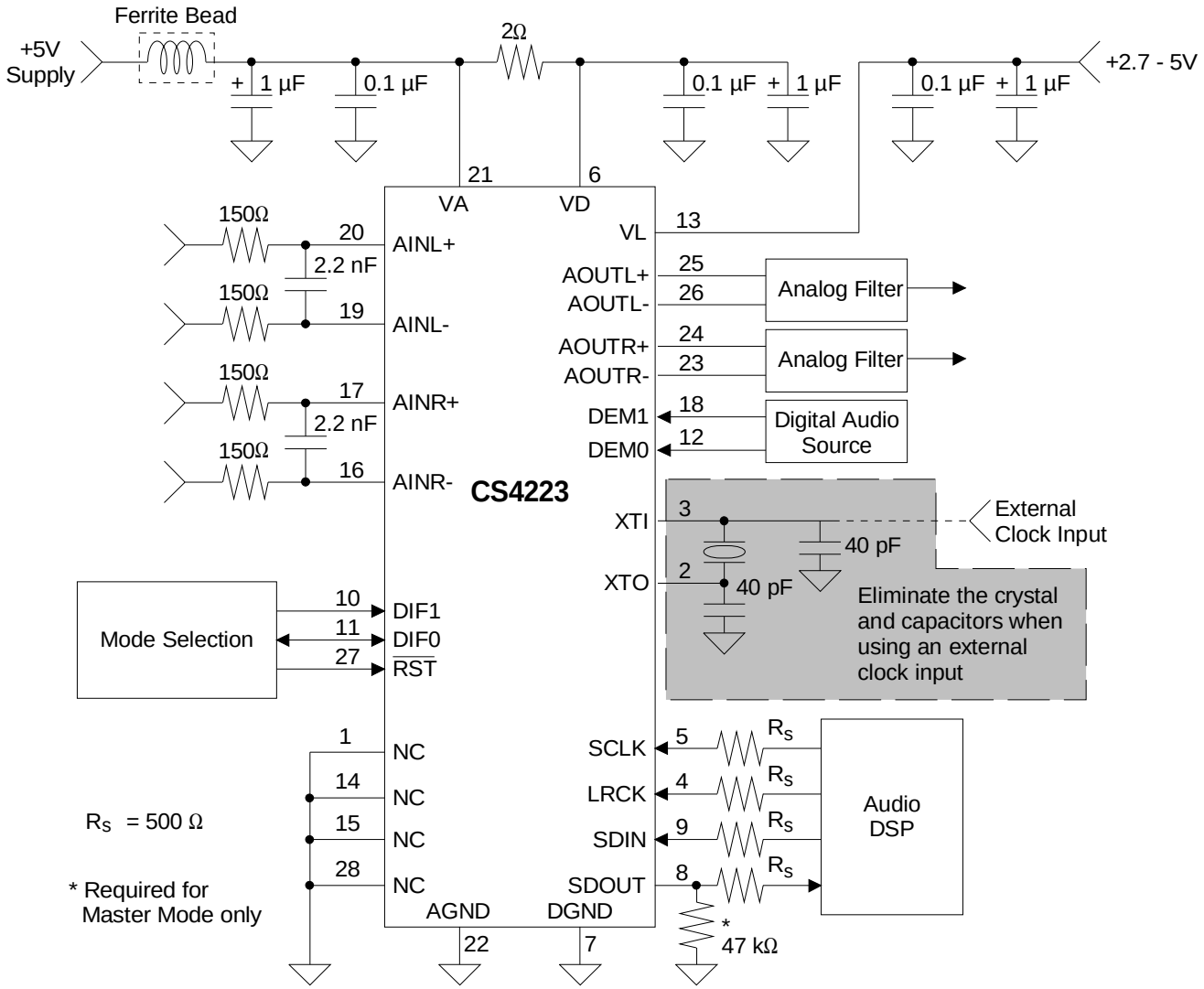


Figure 4. CS4223 Recommended Connection Diagram
(Also see *Recommended Layout Diagram*)

3. TYPICAL CONNECTION DIAGRAM — CS4224

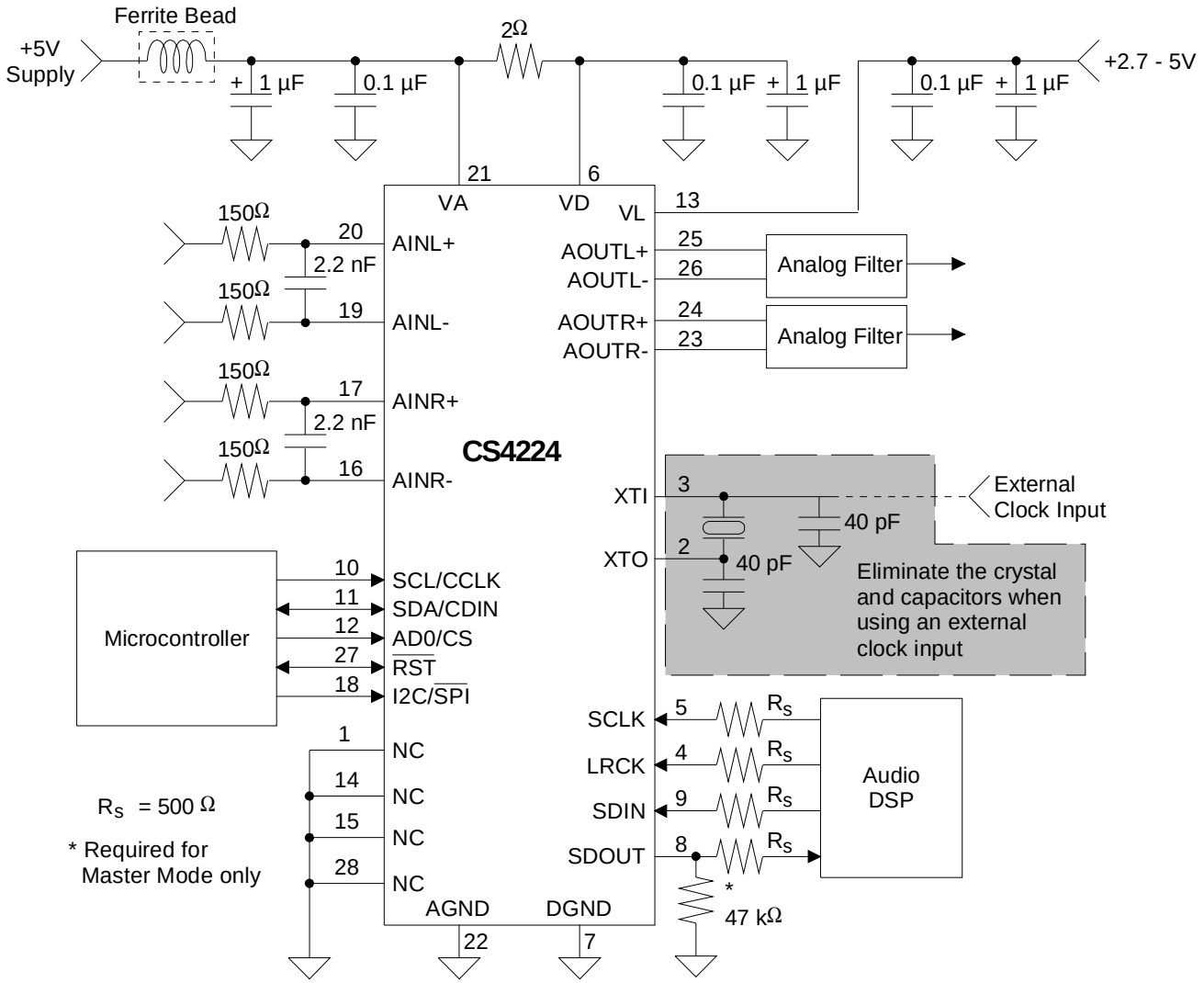


Figure 5. CS4224 Recommended Connection Diagram
(Also see *Recommended Layout Diagram*)

4. REGISTER QUICK REFERENCE - CS4224

Addr	Function	7	6	5	4	3	2	1	0
0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
1h	ADC Control	PDN	HPDR	HPDL	ADMR	ADML	CAL	CALP	CLKE
	default	0	0	0	0	0	0	0	0
2h	DAC Control	Reserved	MUTC	MUTR	MUTL	SOFT	Reserved	RMP1	RMP0
	default	0	0	0	0	0	0	0	0
3h-4h	Output Attenuator Level	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
	default	0	0	0	0	0	0	0	0
5h	DSP Port Mode	Reserved	DEM1	DEM0	DSCK	DOF1	DOF0	DIF1	DIF0
	default	0	0	0	0	0	0	0	0
6h	Converter Status Report	ACCR	ACCL	LVR2	LVR1	LVR0	LVL2	LVL1	LVL0
	default	0	0	0	0	0	0	0	0
7h	Master Clock Control	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCK1	MCK0
	default	0	0	0	0	0	0	0	0

5. REGISTER DESCRIPTIONS - CS4224

Note: All registers are read/write in I^2C mode and write-only in SPI mode, unless otherwise noted.

5.1 ADC Control (address 01h)

7	6	5	4	3	2	1	0
PDN	HPDR	HPDL	ADMR	ADML	CAL	CALP	CLKE
0	0	0	0	0	0	0	0

5.1.1 POWER DOWN ADC (PDN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The ADC will enter a low-power state when this function is enabled.

5.1.2 LEFT AND RIGHT CHANNEL HIGH PASS FILTER DEFEAT (HPDR-HPDL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The internal high-pass filter is defeated when this function is enabled. Control of the internal high-pass filter is independent for the left and right channel.

5.1.3 LEFT AND RIGHT CHANNEL ADC MUTING (ADMR-ADML)

Default = 0
0 - Disabled
1 - Enabled

Function:

The output for the selected ADC channel will be muted when this function is enabled.

5.1.4 CALIBRATION CONTROL (CAL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The device will automatically perform an offset calibration when brought out of reset, which last approximately 50 ms. When this function is enabled, a rising edge on the reset line will initiate an offset calibration.

5.1.5 CALIBRATION STATUS (CALP) (READ ONLY)

Default = 0
0 - Calibration done
1 - Calibration in progress

5.1.6 CLOCKING ERROR (CLKE) (READ ONLY)

Default = 0
0 - No error
1 - Error

5.2 DAC Control (address 02h)

7	6	5	4	3	2	1	0
Reserved	MUTC	MUTR	MUTL	SOFT	Reserved	RMP1	RMP0
0	0	0	0	0	0	0	0

5.2.1 MUTE ON CONSECUTIVE ZEROS (MUTC)

Default = 0
0 - Disabled
1 - Enabled

Function:

The DAC output will mute following the reception of 512 consecutive audio samples of static 0 or -1 when this function is enabled. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The muting function is affected, similar to volume control changes, by the SOFT bit in the DAC Control register.

5.2.2 MUTE CONTROL (MUTR-MUTL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The output for the selected DAC channel will be muted when this function is enabled. The muting function is affected, similar to volume control changes, by the SOFT bit in the DAC Control register.

5.2.3 SOFT RAMP CONTROL (SOFT)

Default = 0
0 - Soft Ramp level changes
1 - Zero Cross level changes

Function:

Soft Ramp level changes will be implemented by incrementally ramping, in 0.5 dB steps, from the current level to the new level. The rate of change defaults to 0.5 dB per 8 left/right clock periods and is adjustable through the RMP bits in the DAC Control register.

Zero Cross level changes will be implemented in a single step from the current level to the new level. The level change takes effect on a zero crossing to minimize audible artifacts. If the signal does not encounter a zero crossing, the level change will occur after a timeout period of 512 sample periods (10.7 ms at 48 kHz sample rate). Zero crossing is independently monitored and implemented for each channel. The ACCR and ACCL bits in the Converter Status Report register indicate when a level change has occurred for the right and left channel.

5.2.4 SOFT RAMP STEP RATE (RMP)

Default = 00
00 - 1 step per 8 LRCK's
01 - 1 step per 4 LRCK's
10 - 1 step per 16 LRCK's
11 - 1 step per 32 LRCK's

Function:

The rate of change for the Soft Ramp function is adjustable through the RMP bits.

5.3 Left Channel Output Attenuator Level (address 03h)

5.4 Right Channel Output Attenuator Level (address 04h)

7	6	5	4	3	2	1	0
ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0	0	0	0	0	0	0	0

5.4.1 ATTENUATION LEVEL (ATT7-ATT0)

Default = 00h

Function:

The Output Attenuator Level registers allow for attenuation of the DAC outputs in 0.5 dB increments from 0 to 113.5 dB. Level changes are implemented with an analog volume control until the residual output noise is equal to the noise floor in the mute state. At this point, volume changes are performed digitally. This technique is superior to purely digital volume control because the noise is attenuated by the same amount as the signal, thus preserving dynamic range, see Figure 16. Volume changes are performed as dictated by the SOFT bit in the DAC Control register. ATT0 represents 0.5 dB of attenuation and settings greater than 227 (decimal value) will mute the selected DAC output.

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
11100011	227	-113.5 dB
11100100	228	Muted

Table 1. Example Volume Settings

5.5 DSP Port Mode (address 05h)

7	6	5	4	3	2	1	0
Reserved	DEM1	DEM0	DSCK	DOF1	DOF0	DIF1	DIF0
0	0	0	0	0	0	0	0

5.5.1 DE-EMPHASIS CONTROL (DEM)

Default = 00
00 - 44.1 kHz de-emphasis setting
01 - 48 kHz de-emphasis setting
10 - 32 kHz de-emphasis setting
11 - De-emphasis disabled

Function:

Selects the appropriate digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates, see Figure 15.

5.5.2 SERIAL INPUT/OUTPUT DATA SCLK POLARITY SELECT (DSCK)

Default = 0
0 - Data valid on rising edge of SCLK
1 - Data valid on falling edge of SCLK

Function:

This function selects the polarity of the SCLK edge used to clock data in and out of the serial audio port.

5.5.3 SERIAL DATA OUTPUT FORMAT (DOF)

Default = 00
00 - I^2S compatible
01 - Left justified
10 - Right justified, 24-bit
11 - Right justified, 20-bit

Function:

The required relationship between the left/right clock, serial clock and output serial data is defined by the Serial Data Output Format, and the options are detailed in Figures 8-11.

Note: If the format selected is Right-Justified, SCLK must be 64 Fs when operating in slave mode.

5.5.4 SERIAL DATA INPUT FORMAT (DIF)

Default = 00
00 - I^2S compatible
01 - Left justified
10 - Right justified, 24-bit
11- Right justified, 20-bit

Function:

The required relationship between the left/right clock, serial clock and input serial data is defined by the Serial Data Input Format, and the options are detailed in Figures 8-11.

5.6 Converter Status Report (Read Only) (address 06h)

7	6	5	4	3	2	1	0
ACCR	ACCL	LVR2	LVR1	LVR0	LVL2	LVL2	LVL0
0	0	0	0	0	0	0	0

5.6.1 LEFT AND RIGHT CHANNEL ACCEPTANCE BIT (ACCR-ACCL)

Default = 0
0 - Requested setting valid
1 - New setting loaded

Function:

The ACCR and ACCL bits indicate when a change in the Output Attenuator Level has occurred for the left and right channels, respectively. The value will be high when a new setting is loaded into the Output Attenuator Level registers. The value will return low when the requested attenuation setting has taken effect.

5.6.2 LEFT AND RIGHT CHANNEL ADC OUTPUT LEVEL (LVR AND LVL)

Default = 000
000 - Normal output levels
001 - -6 dB level
010 - -5 dB level
011 - -4 dB level
100 - -3 dB level
101 - -2 dB level
110 - -1 dB level
111 - Clipping

Function:

The analog-to-digital converter is continually monitoring the peak digital signal output for both the left and right channel, prior to the digital limiter. The maximum output value is stored in the LVL and LVR bits. The LVL and LVR bits are ‘sticky’, so they are reset after each read is performed.

5.7 Master Clock Control (address 07h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCK1	MCK0
0	0	0	0	0	0	0	0

5.7.1 MASTER CLOCK CONTROL (MCK)

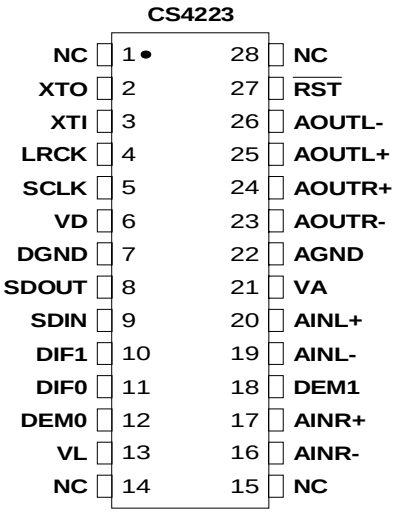
Default = 00
00 - XTI = 256 Fs for Master Mode
01 - XTI = 384 Fs for Master Mode
10 - XTI = 512 Fs for Master Mode

Function:

The MCK bits allow for control of the Master Clock, XTI, input frequency.

Note: These bits are not valid when operating in slave mode.

6. PIN DESCRIPTIONS — CS4223



NC	1,14,15, 28	**No Connect -** These pins are not connected internally and should be tied to DGND to minimize noise coupling.
XTI, XTO	2,3	**Crystal Connections (*Input/Output*) -** Input and output connections for the crystal used to clock the CS4223. Alternatively, a clock may be input into XTI. This is the clock source for the delta-sigma modulator and digital filters. The frequency of this clock must be either 256x, 384x, or 512x Fs in Slave Mode and 256x in Master Mode.

Fs (kHz)	XTI (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 2. Common Clock Frequencies

LRCK	4	**Left/Right Clock (*Input*) -** Determines which channel is currently being input/output of the serial audio data pins SDIN/SDOUT. The frequency of the Left/Right clock must be equal to the input sample rate. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.
SCLK	5	**Serial Data Clock (*Input*) -** Clocks the individual bits of the serial data into the SDIN pin and out of the SDOUT pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.
VD	6	**Digital Power (*Input*) -** Positive power supply for the digital section. Typically 5.0 VDC.
DGND	7	**Digital Ground (*Input*) -** Digital ground for the digital section.
SDOUT	8	**Serial Data Output (*Output*) -** Two's complement MSB-first serial data is output on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.

SDIN	9	**Serial Data Input (*Input*) -** Two's complement MSB-first serial data is input on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.
DIF0, DIF1	10,11	**Digital Interface Format (*Input*) -** The required relationship between the left/right clock, serial clock and serial data is defined by the Digital Interface Format. The options are detailed in Figures 8 - 11.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	I^2S, up to 24-bit data	0	8
0	1	Left Justified, up to 24-bit data	1	9
1	0	Right Justified, 24-bit Data	2	10
1	1	Right Justified, 20-bit Data	3	11

Table 3. Digital Interface Format - DIF1 and DIF0

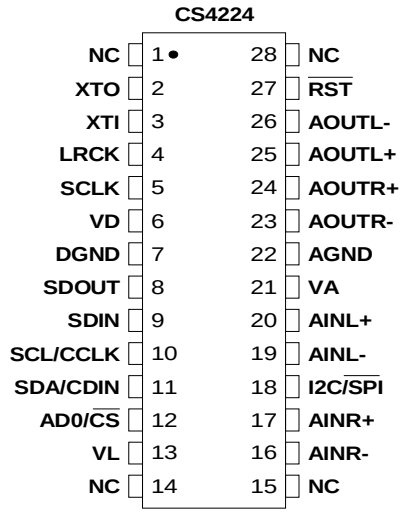
DEM0, DEM1	12,18	**De-Emphasis Select (*Input*) -** Controls the activation of the standard 50/15 µs de-emphasis filter. 32, 44.1, or 48 kHz sample rate selection defined in Table 4.

DEM0	DEM1	De-Emphasis
0	0	32 kHz
0	1	44.1 kHz
1	0	48 kHz
1	1	Disabled

Table 4. De-emphasis Control

VL	13	**Digital Logic Power (*Input*) -** Positive power supply for the digital interface section. Typically 3.0 to 5.0 VDC.
AINR-, AINR+	16,17	**Differential Right Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
AINL-, AINL+	19,20	**Differential Left Channel Analog Input (*Input*)** - The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
VA	21	**Analog Power (*Input*) -** Positive power supply for the analog section. Nominally +5 Volts.
AGND	22	**Analog Ground (*Input*) -** Analog ground reference.
AOUTR-, AOUTR+	23, 24	**Differential Right Channel Analog Output (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
AOUTL-, AOUTL+	25, 26	**Differential Left Channel Analog Output (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
$\overline{\text{RST}}$	27	**Reset (*Input*)** - When low, the device enters a low power mode and all internal registers are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

7. PIN DESCRIPTIONS — CS4224



NC	1,14,15, 28	**No Connect -** These pins are not connected internally and should be tied to DGND to minimize noise coupling.
XTI, XTO	2,3	**Crystal Connections (*Input/Output*) -** Input and output connections for the crystal used to clock the CS4224. Alternatively a clock may be input into XTI. This is the clock source for the delta-sigma modulator and digital filters. The frequency of this clock must be either 256x, 384x, or 512x Fs. The default XTI setting in Master Mode is 256x, but this may be changed to 384x or 512x through the Control Port.

Fs (kHz)	XTI (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 5. Common Clock Frequencies

LRCK	4	**Left/Right Clock (*Input*) -** Determines which channel is currently being input/output of the serial audio data pins SDIN/SDOUT. The frequency of the Left/Right clock must be equal to the input sample rate. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
SCLK	5	**Serial Data Clock (*Input*) -** Clocks the individual bits of the serial data into the SDIN pin and out of the SDOUT pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
VD	6	**Digital Power (*Input*) -** Positive power supply for the digital section. Typically 5.0 VDC.
DGND	7	**Digital Ground (*Input*) -** Digital ground for the digital section.

SDOUT	8	**Serial Data Output (*Output*) -** Two's complement MSB-first serial data is output on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
SDIN	9	**Serial Data Input (*Input*) -** Two's complement MSB-first serial data is input on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
SCL/CCLK	10	**Serial Control Port Clock (*Input*) -** Clocks the serial control bits into and out of the CS4224. In I^2C mode, SCL requires an external pull-up resistor according to the I^2C specification.
SDA/CDIN	11	**Serial Control Port Data (*Input/Output*)-** SDA is a data I/O line in I^2C mode and requires an external pull-up resistor according to the I^2C specification. CDIN in the input data line for the serial control port in SPI mode.
AD0/$\overline{\text{CS}}$	12	**Address Bit/Control Chip Select (*Input*) -** In I^2C mode, AD0 is a chip address bit. In SPI mode, $\overline{\text{CS}}$ is used to enable the control port interface on the CS4224. The CS4224 control port interface is defined by the $\overline{\text{SPI}}$/I2C pin.
VL	13	**Logic Power (*Input*) -** Positive power supply for the digital interface section. Typically 3.0 to 5.0 VDC.
AINR-, AINR+	16,17	**Differential Right Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
I2C/$\overline{\text{SPI}}$	18	**Control Port Format (*Input*)** - When this pin is high, I^2C mode is selected, when low, $\overline{\text{SPI}}$ is selected.
AINL-, AINL+	19,20	**Differential Left Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
VA	21	**Analog Power (*Input*) -** Positive power supply for the analog section. Typically 5.0 VDC.
AGND	22	**Analog Ground (*Input*) -** Analog ground reference.
AOUTR-, AOUTR+	23, 24	**Differential Right Channel Analog Outputs (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
AOUTL-, AOUTL+	25, 26	**Differential Left Channel Analog Outputs (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
$\overline{\text{RST}}$	27	**Reset (*Input*)** - When low, the device enters a low power mode and all internal registers are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

8. APPLICATIONS

8.1 Overview

The CS4223 is a stand-alone device controlled through dedicated pins. The CS4224 is controlled with an external microcontroller using the serial control port.

8.2 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4223/4 requires careful attention to power supply and grounding arrangements to optimize performance. Figures 4 and 5 shows the recommended power arrangement with VA, VD and VL connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be used on each supply pin.

8.3 High Pass Filter

The operational amplifiers in the input circuitry driving the CS4223/4 may generate a small DC offset into the A/D converter. The CS4223/4 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

8.4 Analog Outputs

The recommended off-chip analog filter is either a 2nd order Butterworth or a 3rd order Butterworth, if greater out-of-band noise filtering is desired. The CS4223/4 DAC interpolation filter has been precompensated for an external 2nd order Butterworth filter with a 3 dB corner at Fs, or a 3rd order Butterworth filter with a 3 dB corner at 0.75 Fs to provide a flat frequency response and linear phase over the passband (see Figure 14 for Fs = 48 kHz). If the recommended filter is not used, small frequency response magnitude and phase errors will occur. In addition to providing out-of-band noise attenuation, the output filters shown in Figure 14 provide differential to single-ended conversion.

8.5 Master vs. Slave Mode

The CS4223/4 may be operated in either master mode or slave mode. In master mode, SCLK and LRCK are outputs which are internally derived from MCLK. The device will operate in master mode when a 47 kΩ pulldown resistor is present on SDOUT at startup or after reset, see Figure 5. LRCK and SCLK are inputs to the CS4223/4 when operating in slave mode. See Figures 8-11 for the available clocking modes.

8.6 De-emphasis

The CS4223/4 includes digital de-emphasis for 32, 44.1, or 48 kHz sample rates. The frequency response of the de-emphasis curve, as shown in Figure 15, will scale proportionally with changes in samples rate, Fs. The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis as a means of noise reduction.

De-emphasis control is achieved with the DEM1/0 pins on the CS4223 or through the DEM1-0 bits in the DSP Port Mode Byte (#5) on the CS4224.

8.7 Power-up / Reset / Power Down Calibration

Upon power up, the user should hold $\overline{RST}$ = 0 for approximately 10 ms. In this state, the control port is reset to its default settings and the part remains in the power down mode. At the end of $\overline{RST}$, the device performs an offset calibration which lasts approximately 50 ms after which the device enters normal operation. In the CS4224, a calibration may also be initiated via the CAL bit in the ADC Control Byte (#1). The CALP bit in the ADC Control Byte is a read only bit indicating the status of the calibration.

Reset/Power Down is achieved by lowering the $\overline{RST}$ pin causing the part to enter power down.

Once $\overline{RST}$ goes high, the control port is functional and the desired settings should be loaded.

The CS4223/4 will also enter power down mode if the master clock source stops for approximately 10 µs or if the LRCK is not synchronous to the master clock. The control port will retain its current settings.

The CS4223/4 will mute the analog outputs and enter the power down mode if the supply drops below approximately 4 volts.

8.8 Control Port Interface (CS4224 only)

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI® and I^2C®, with the CS4224 operating as a slave device. The control port interface format is selected by the $\overline{SPI}$/I2C pin.

8.8.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS4224 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 6 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. Register reading from the CS4224 is not supported in the SPI mode. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into a register designated by the MAP.

The CS4224 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for successive writes. If INCR is set to a 1, then MAP will auto increment after each byte is written, allowing block writes of successive registers. Register reading from the CS4224 is not supported in the SPI mode.

8.8.2 I^2C Mode

In I^2C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 7. There is no $\overline{CS}$ pin. Pin AD0 forms the partial chip address and should be tied to VD or DGND as desired. The upper 6 bits of the 7 bit address field must be 001000. In order to communicate with the CS4224, the LSB of the chip address field (first byte sent to the CS4224) should match the setting of the AD0 pin. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

8.9 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	Reserved	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

8.9.1 AUTO-INCREMENT CONTROL (INCR)

Default = 0
0 - Disabled
1 - Enabled

8.9.2 REGISTER POINTER (MAP)

Default = 000

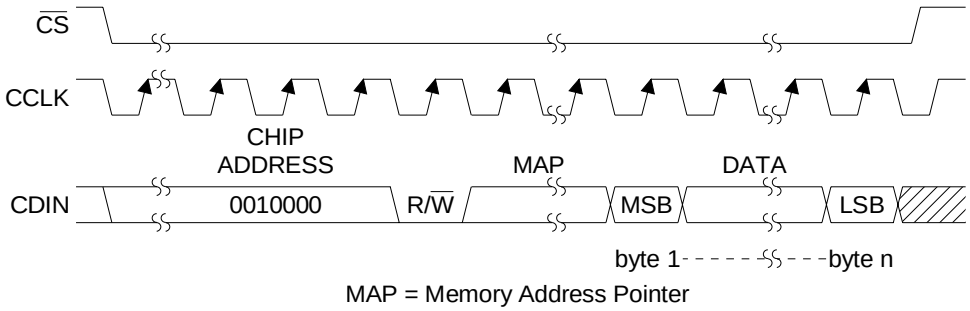


Figure 6. Control Port Timing, SPI mode

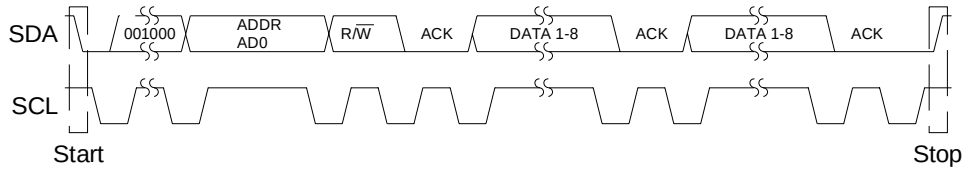
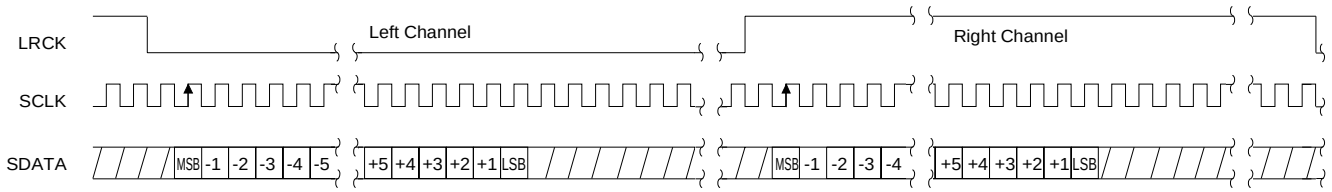
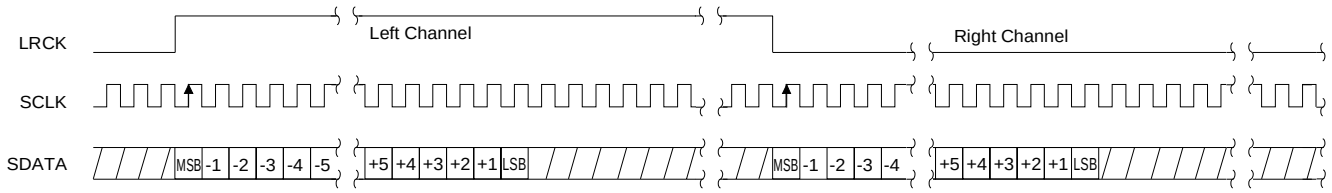


Figure 7. Control Port Timing, I^2C mode



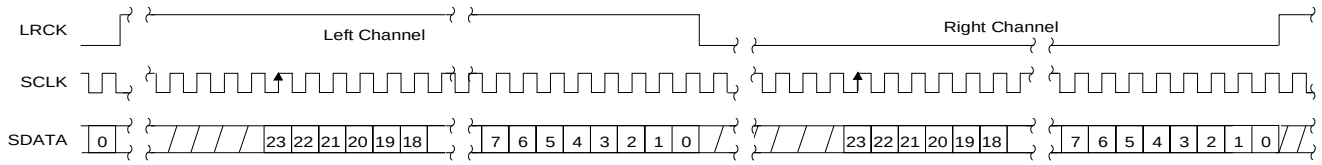
Master	Slave
I^2S, up to 24-bit data XTI=256, 384, 512 Fs (CS4223-256Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	I^2S, up to 24-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 48,64, 128 Fs

Figure 8. Serial Audio Format 0 (I^2S)



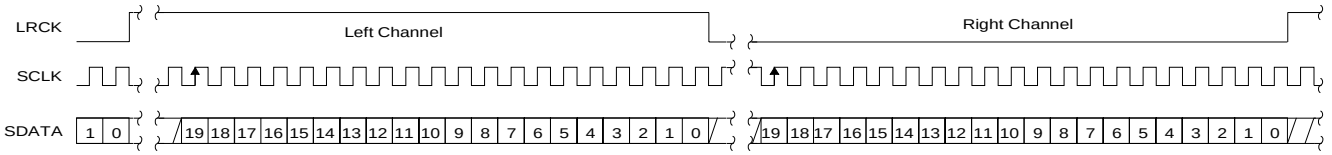
Master	Slave
Left-justified, up to 24-bit data XTI=256, 384, 512 Fs (CS4223-256Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	Left-justified, up to 24-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 48, 64, 128 Fs

Figure 9. Serial Audio Format 1



Master	Slave
Right-justified, 24-bit data XTI=256, 384, 512 Fs (CS4223-256Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	Right-justified, 24-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 64 Fs

Figure 10. Serial Audio Format 2



Master	Slave
Right-justified, 20-bit data XTI=256, 384, 512Fs (CS4223-256Fsonly) LRCK = 4 to 50 kHz SCLK = 64 Fs	Right-justified, 20-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 64 Fs

Figure 11. Serial Audio Format 3

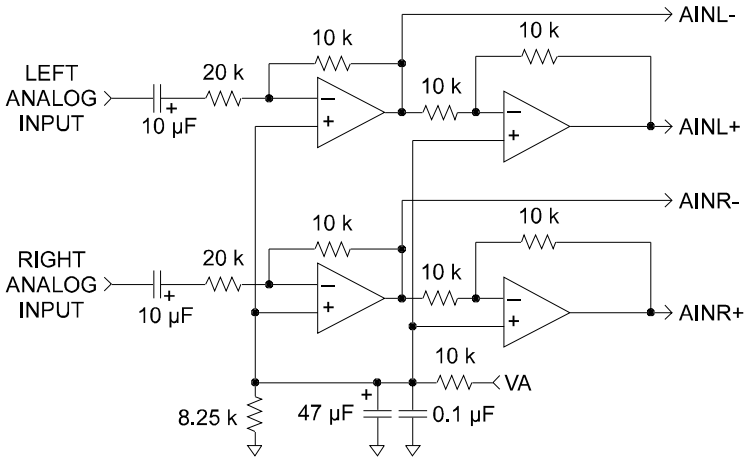


Figure 12. Optional Input Buffer

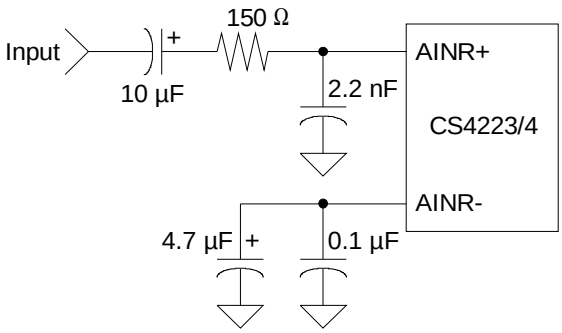
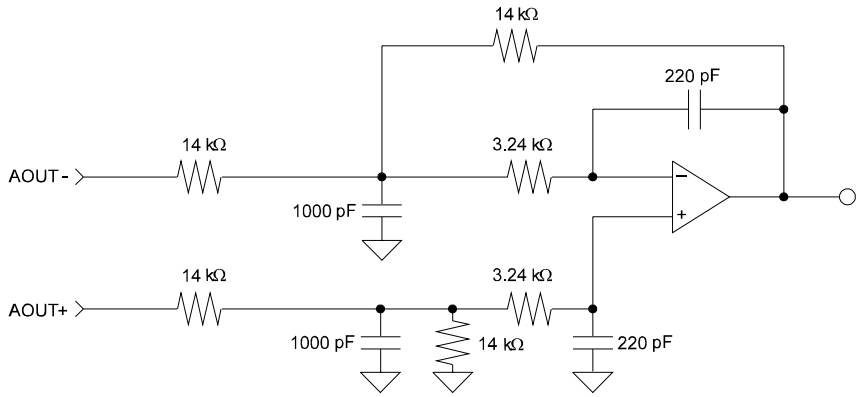
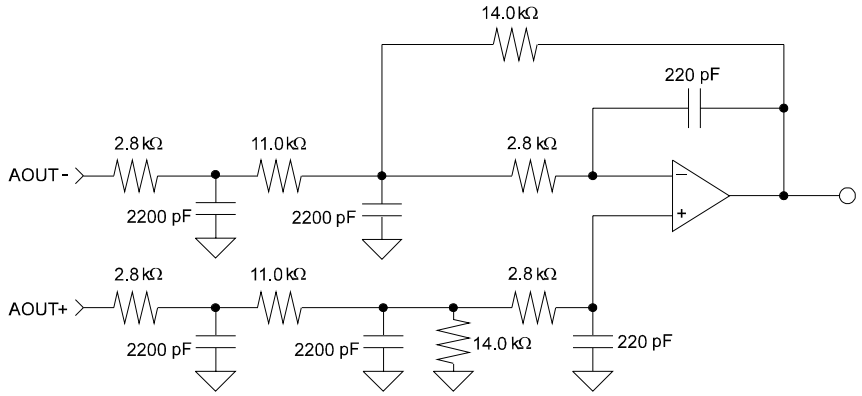


Figure 13. Single-ended Input Application



2-pole Butterworth Filter



3-pole Butterworth Filter

Figure 14. 2- and 3-Pole Butterworth Filters

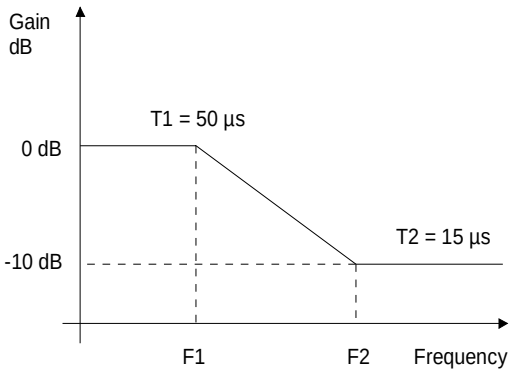


Figure 15. De-emphasis Curve

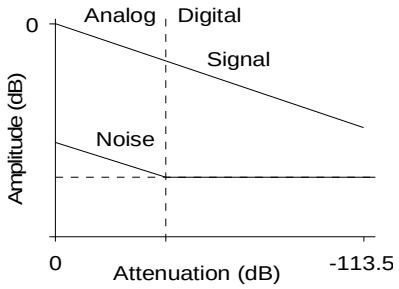


Figure 16. Hybrid Analog/Digital Attenuation

9. ADC/DAC FILTER RESPONSE

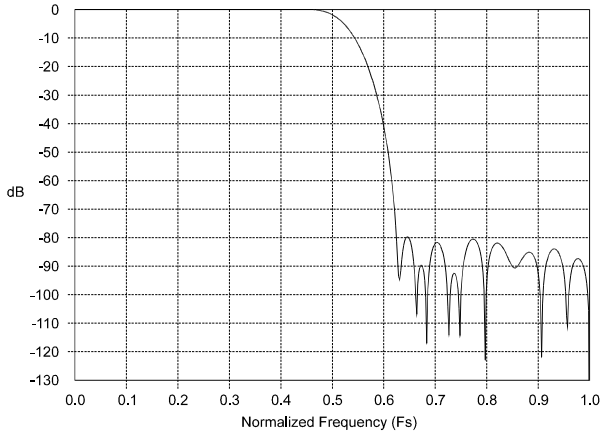


Figure 17. ADC Filter Response

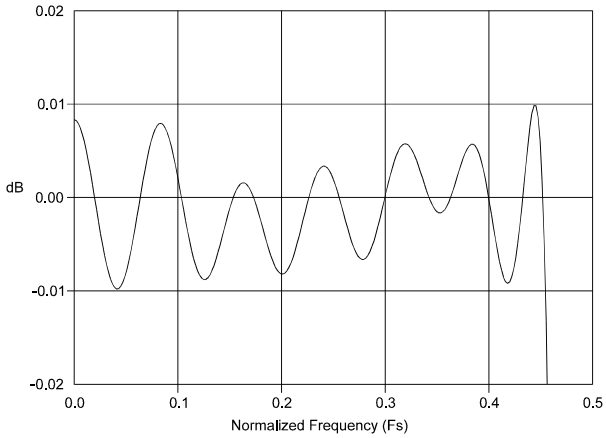


Figure 18. ADC Passband Ripple

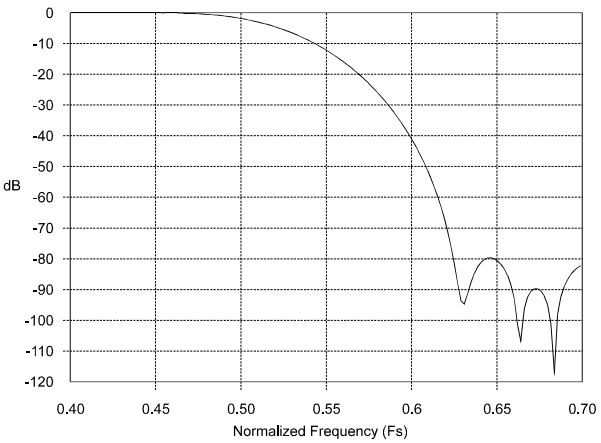


Figure 19. ADC Transition Band

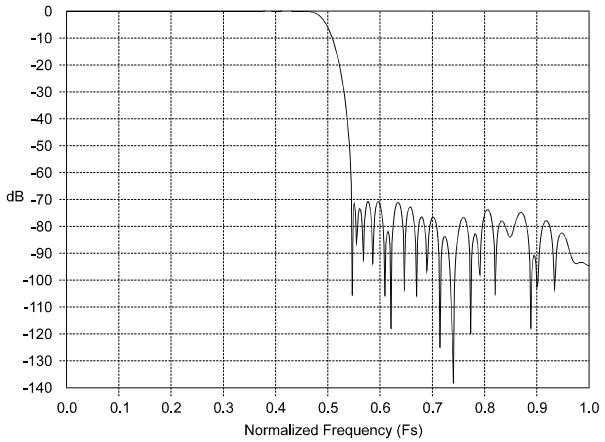


Figure 20. DAC Filter Response

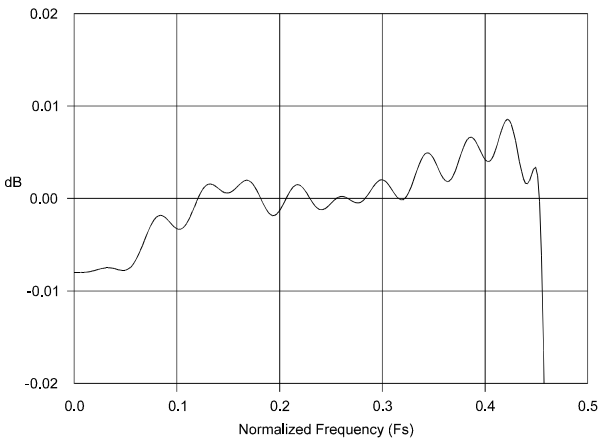


Figure 21. DAC Passband Ripple

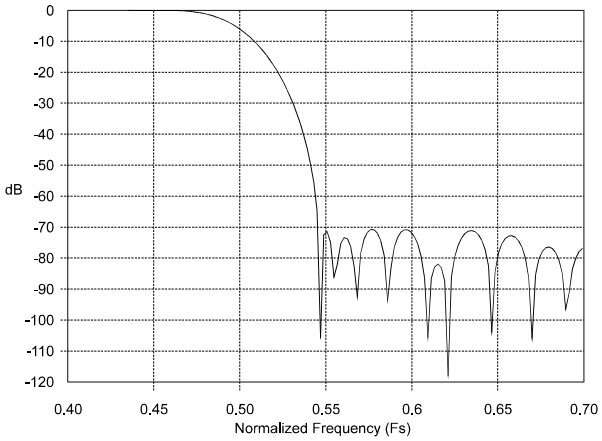


Figure 22. DAC Transition Band

10. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1 dBFS as suggested in AES17-1991 Annex A and DACs are measured at 0 dBFS.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the rms analog output level with 1 kHz full scale digital input to the rms analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal. Units in decibels.

Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 20 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

Gain Error

The deviation from the nominal full scale output for a full scale input.

Gain Drift

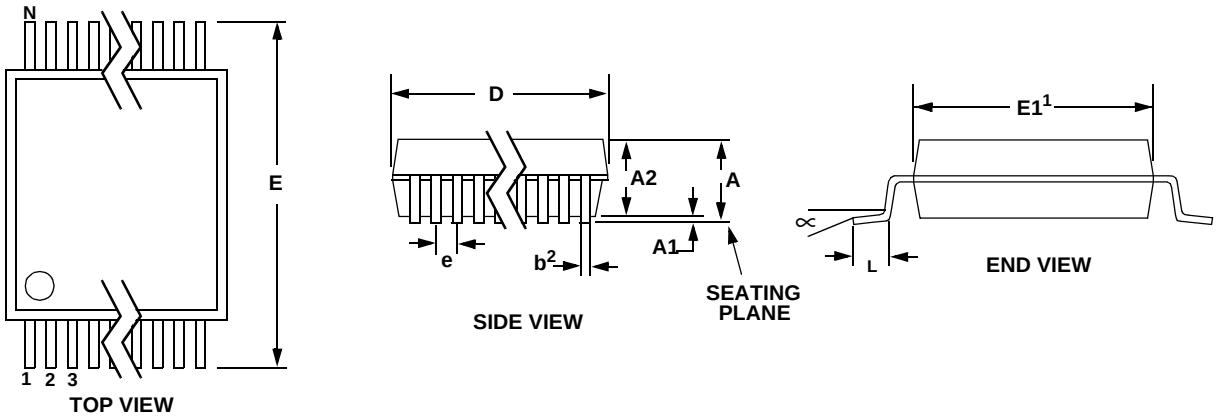
The change in gain value with temperature. Units in ppm/°C.

Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected inputs tied to a common potential. For the DAC's, the differential output voltage with mid-scale input code. Units are in volts.

11. PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.15	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

• Notes •


SMART
Analog
™

TASCAM
TEAC Professional Division

CD-RW402V3

SERVICE MANUAL

SUPPLEMENT

追補版

The circuit diagrams and PC board here are applicable for CD-RW402 S/No. 0270001 and higher.
Use this with the original CD-RW402 Service Manual, Effective: January, 2002.

ここに記載されている回路図と基板図は、シリアル No. 0270001 以降の CD-RW402に適用されます。 CD-RW402 オリジナルサービスマニュアル、Effective: January, 2002 と共に使用してください。

Changes（変更内容）

1. To adopt a new CD-RW DRIVE, related components have only been changed. Main PCB Assy has been changed due to availability of DI Transmitter IC.

   CD-RW DRIVEを変更するとともに、関連部品を変更しました。
   IC変更の為にMAIN PCBを変更しました。

2. To cope with above, the major difference of parts are as follows:

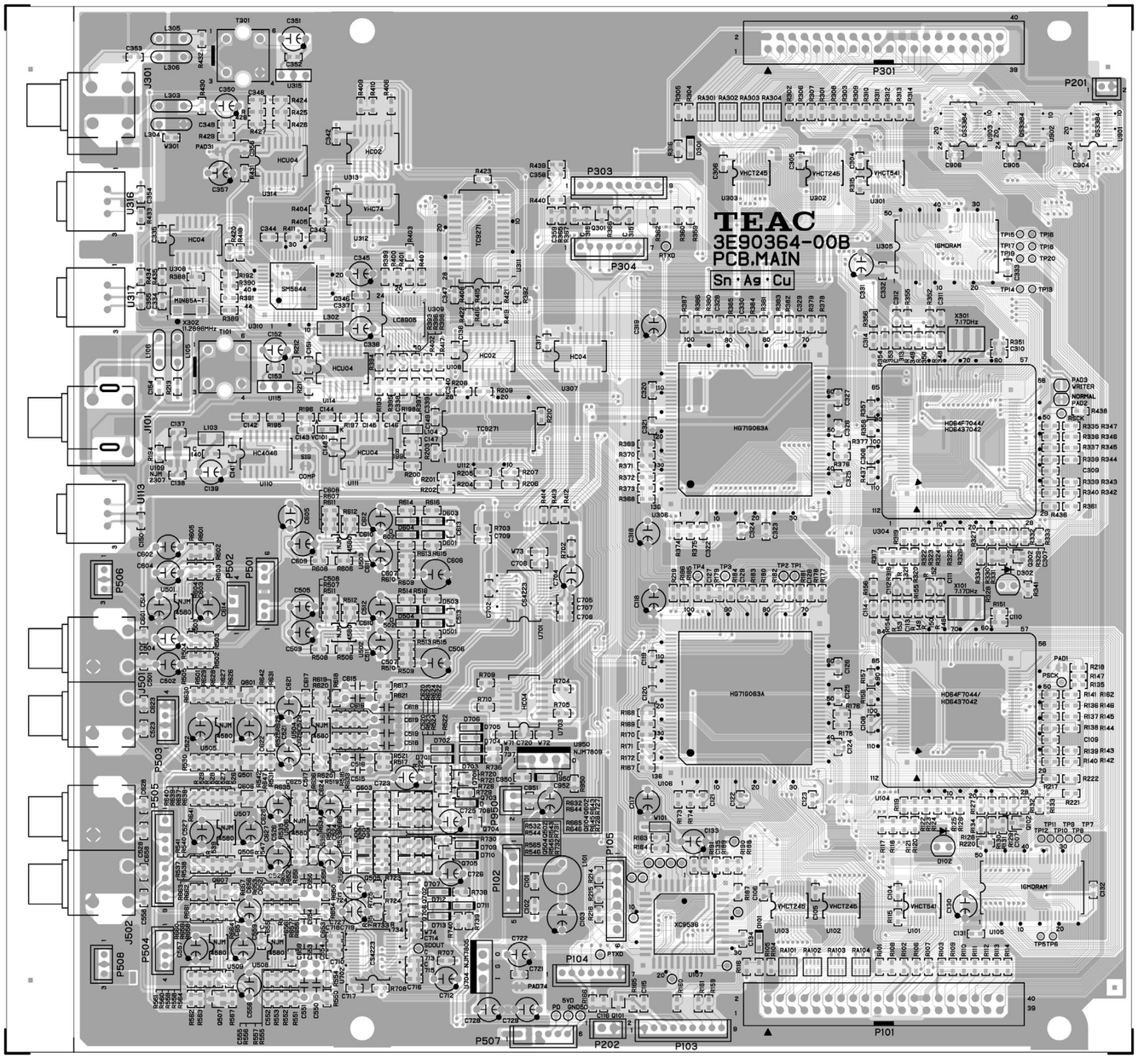
   上記による主要な差異部品は以下の通りです。

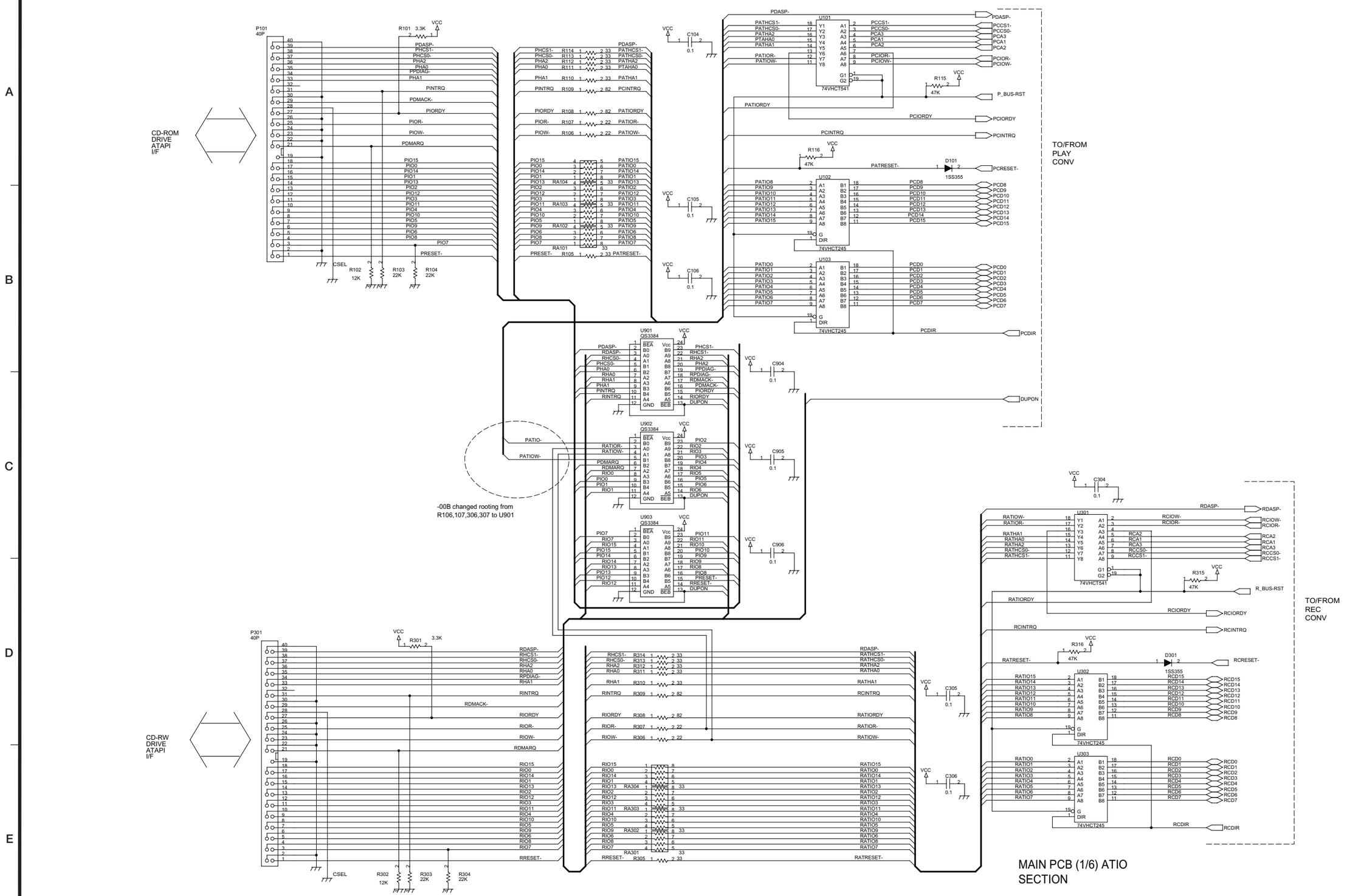
1-19	3Y0046000A	DRIVE ASSY,CD-RW54E TEXT	→	V00140000A	CD-W58DA-T00	
1-20	3M0093902B	PANEL,TRAY(2) CD-RW402	→	M02038100A	PANEL,TRAY(2) RW402 ASS	
1-14	3Y0045900A	DRIVE ASSY,CD-532E AV	→	Y00274300A	DRIVE ASSY,CD-532 AV	(CCCD supported)
1-16	3E0175100A	40P-L330	→	E01059100A	40P DRV2 RW402	CABLE ASSY
1-18	3E9536400A	PCB ASSY,MAIN RW402	→	3E9536400A	PCB ASSY,MAIN RW402	(No change)
	S0042044	IC,TC9271FS	→	3S002944G	IC,TC9271F(ELP)SMT.TA G	U112/U311
	S0039753	IC,M11B16161A-45T	→	S0060813	IC,T2316162A-50S	U105/U305

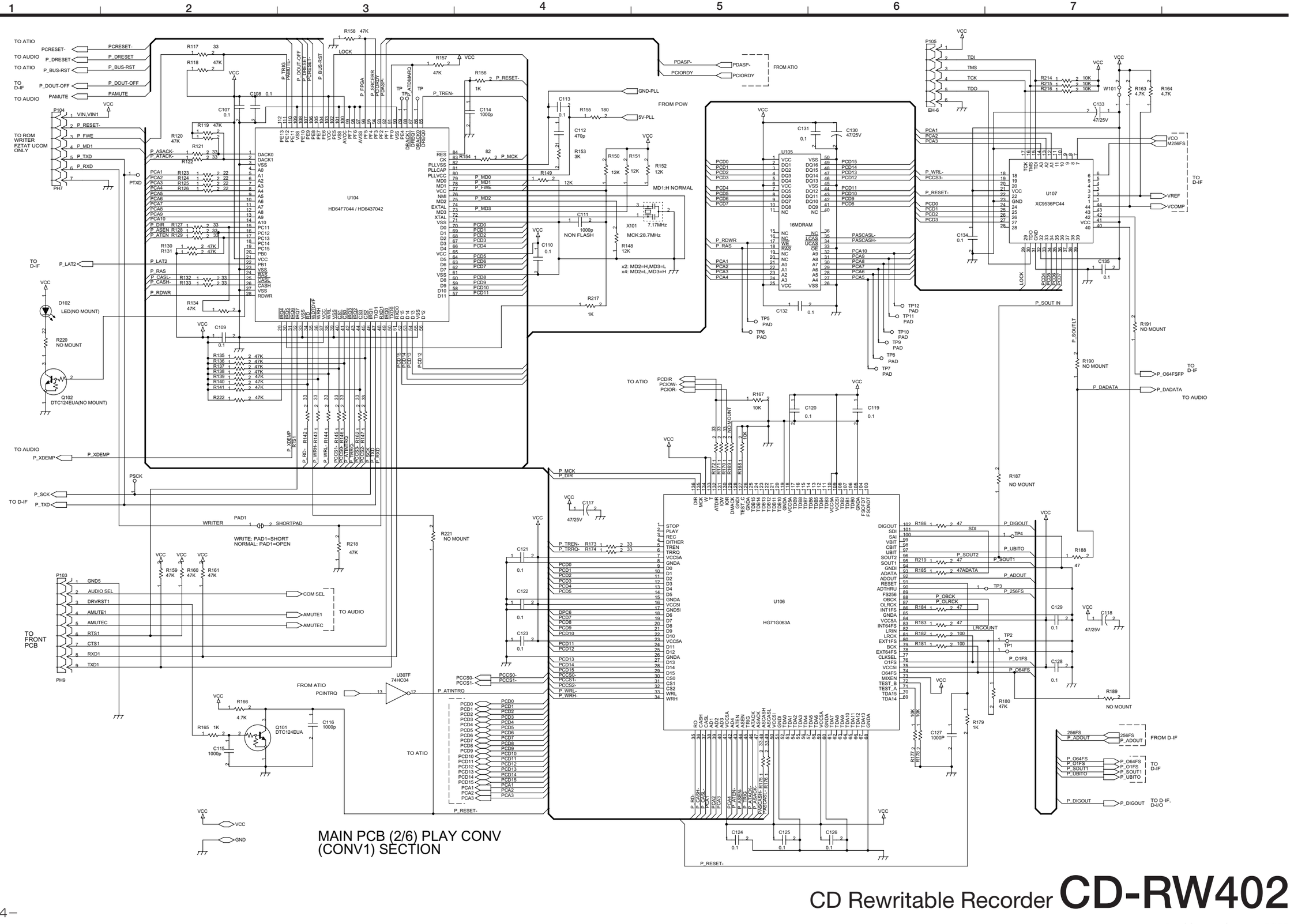
Effective: August, 2005

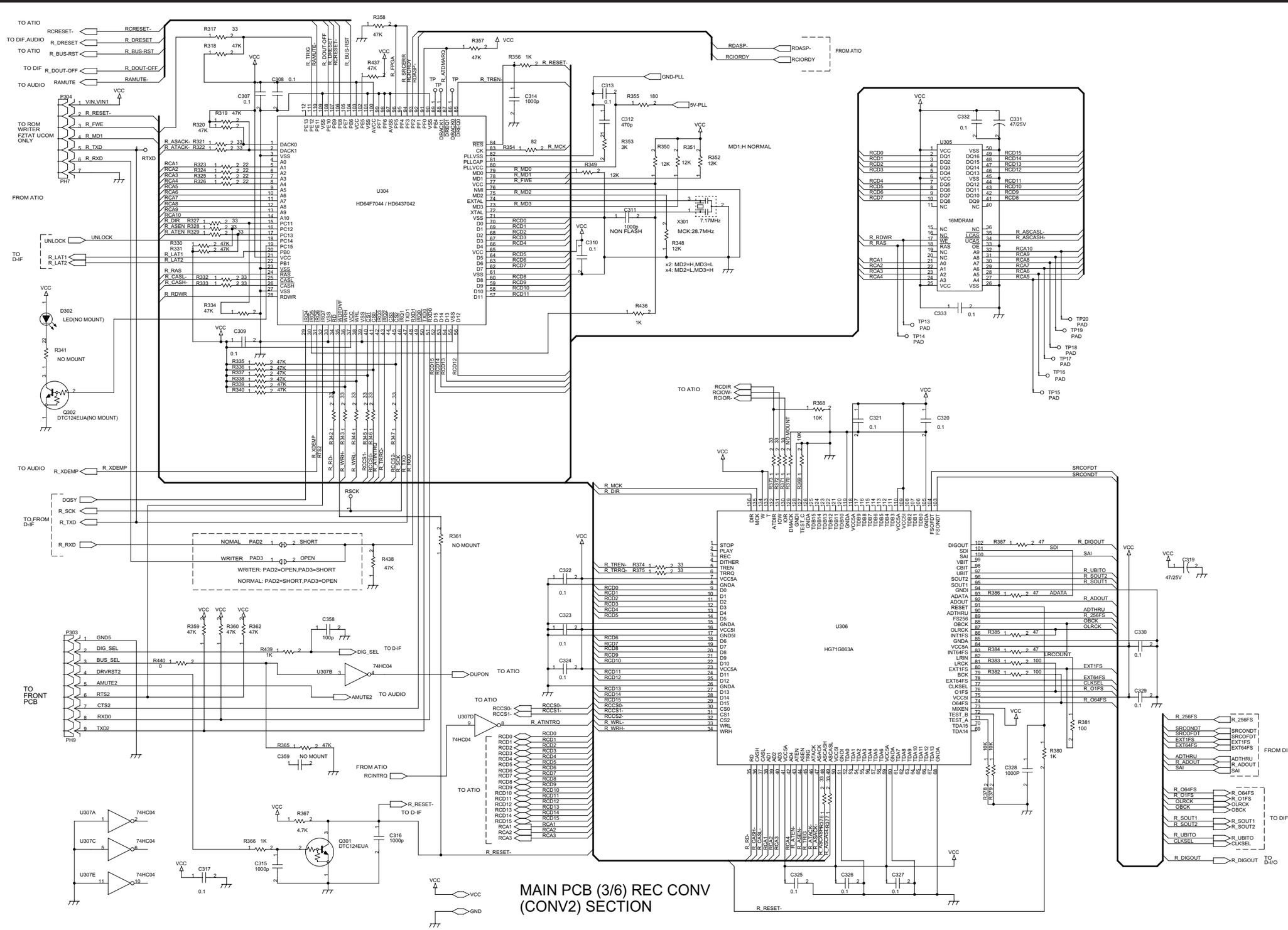
PC BOARDS
基板図

MAIN PCB



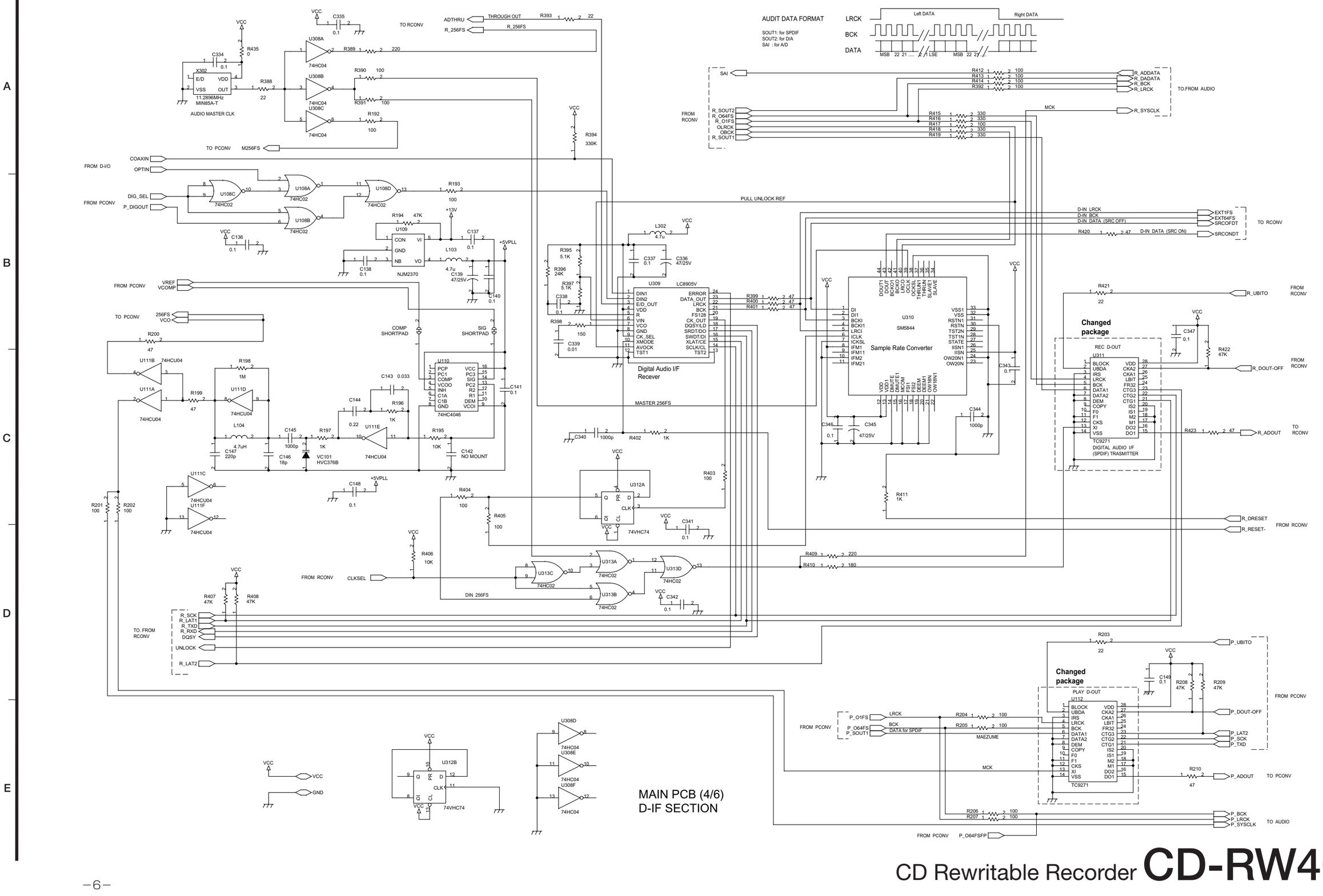

1
2
3
4
5
6
7
A
B
C
D
E
CD-ROM DRIVE ATAPI I/F
P101 40P
R101 3.3K
VCC
PDASP-
PHCS1-
PHCS0-
PHA2
PHA0
PPDIAG-
PHA1
PINTRQ
PDMACK-
PIORDY
PIOR-
PIOW-
PDMARQ
PIO15
PIO0
PIO14
PIO1
PIO13
PIO2
PIO12
PIO3
PIO11
PIO4
PIO10
PIO5
PIO9
PIO6
PIO8
PIO7
PRESET-
CSEL
R102 12K
R103 22K
R104 22K
PHCS1- R114 33 PATHCS1-
PHCS0- R113 33 PATHCS0-
PHA2 R112 33 PATHA2
PHA0 R111 33 PTAHA0
PHA1 R110 33 PATHA1
PINTRQ R109 82 PCINTRQ
PIORDY R108 82 PATIORDY
PIOR- R107 22 PATIOR-
PIOW- R106 22 PATIOW-
PIO15 PATIO15
PIO0 PATIO0
PIO14 PATIO14
PIO1 PATIO1
PIO13 RA104 33 PATIO13
PIO2 PATIO2
PIO12 PATIO12
PIO3 PATIO3
PIO11 RA103 33 PATIO11
PIO4 PATIO4
PIO10 PATIO10
PIO5 PATIO5
PIO9 RA102 33 PATIO9
PIO6 PATIO6
PIO8 PATIO8
PIO7 PATIO7
RA101 33
PRESET- R105 33 PATRESET-
C104 0.1
C105 0.1
C106 0.1
U101
PATHCS1-
PATHCS0-
PATHA2
PTAHA0
PATHA1
PATIOR-
PATIOW-
74VHCT541
PCCS1-
PCCS0-
PCA3
PCA1
PCA2
PCIOR-
PCIOW-
R115 47K
P_BUS-RST
PCIORDY
PCINTRQ
R116 47K
PATRESET-
D101 1SS355
PCRESET-
U102
PATIO8
PATIO9
PATIO10
PATIO11
PATIO12
PATIO13
PATIO14
PATIO15
74VHCT245
PCD8
PCD9
PCD10
PCD11
PCD12
PCD13
PCD14
PCD15
U103
PATIO0
PATIO1
PATIO2
PATIO3
PATIO4
PATIO5
PATIO6
PATIO7
PCD0
PCD1
PCD2
PCD3
PCD4
PCD5
PCD6
PCD7
PCDIR
TO/FROM PLAY CONV
U901 QS3384
U902 QS3384
U903 QS3384
BEA
BEB
Vcc
GND
PDASP-
RDASP-
RHCS0-
PHCS0-
PHA0
RHA0
RHA1
PINTRQ
RINTRQ
PHCS1-
RHCS1-
RHA2
PHA2
PPDIAG-
RPDIAG-
PDMACK-
RDMACK-
PIORDY
RIORDY
DUPON
C904 0.1
C905 0.1
C906 0.1
PATIO-
RATIOR-
RATIOW-
PDMARQ
RDMARQ
RIO0
PIO0
RIO1
PIO1
PIO2
RIO2
RIO3
PIO3
RIO4
PIO4
RIO5
PIO5
RIO6
PIO6
PIO7
RIO7
PIO8
RIO8
PIO9
RIO9
PIO10
RIO10
PIO11
RIO11
PIO12
RIO12
PIO13
RIO13
PIO14
RIO14
PIO15
RIO15
RRESET-
PRESET-
-00B changed rooting from R106,107,306,307 to U901
C304 0.1
U301
RATIOW-
RATIOR-
RATHA1
RATHA0
RATHA2
RATHCS0-
RATHCS1-
74VHCT541
RCIOW-
RCIOR-
RCA2
RCA1
RCA3
RCCS0-
RCCS1-
R315 47K
R_BUS-RST
RATIORDY
RCIORDY
RCINTRQ
R316 47K
RATRESET-
D301 1SS355
RCRESET-
U302
RATIO15
RATIO14
RATIO13
RATIO12
RATIO11
RATIO10
RATIO9
RATIO8
74VHCT245
RCD15
RCD14
RCD13
RCD12
RCD11
RCD10
RCD9
RCD8
U303
RATIO0
RATIO1
RATIO2
RATIO3
RATIO4
RATIO5
RATIO6
RATIO7
RCD0
RCD1
RCD2
RCD3
RCD4
RCD5
RCD6
RCD7
RCDIR
TO/FROM REC CONV
P301 40P
R301 3.3K
CD-RW DRIVE ATAPI I/F
RDASP-
RHCS1-
RHCS0-
RHA2
RHA0
RPDIAG-
RHA1
RINTRQ
RDMACK-
RIORDY
RIOR-
RIOW-
RDMARQ
RIO15
RIO0
RIO14
RIO1
RIO13
RIO2
RIO12
RIO3
RIO11
RIO4
RIO10
RIO5
RIO9
RIO6
RIO8
RIO7
RRESET-
CSEL
R302 12K
R303 22K
R304 22K
RHCS1- R314 33
RHCS0- R313 33
RHA2 R312 33
RHA0 R311 33
RHA1 R310 33
RINTRQ R309 82
RIORDY R308 82
RIOR- R307 22
RIOW- R306 22
RIO15
RIO0
RIO14
RIO1
RIO13 RA304 33
RIO2
RIO12
RIO3
RIO11 RA303 33
RIO4
RIO10
RIO5
RIO9 RA302 33
RIO6
RIO8
RIO7
RA301 33
RRESET- R305 33
RATHA1
RCINTRQ
RATIORDY
RATIOR-
RATIOW-
RATRESET-
C305 0.1
C306 0.1
MAIN PCB (1/6) ATIO SECTION


U104
HD64F7044 / HD6437042
U105
16MDRAM
U106
HG71G063A
U107
XC9536PC44
X101
7.17MHz
MCK:28.7MHz
NON FLASH
MD1:H NORMAL
x2: MD2=H,MD3=L
x4: MD2=L,MD3=H
LED(NO MOUNT)
Q102
DTC124EUA(NO MOUNT)
Q101
DTC124EUA
U307F
74HC04
WRITER
SHORTPAD
WRITE: PAD1=SHORT
NORMAL: PAD1=OPEN
COM SEL
AUDIO SEL
DRVRST1
AMUTE1
AMUTEC
RTS1
CTS1
RXD1
TXD1
TO ATIO
TO AUDIO
TO D-IF
TO ROM WRITER FZTAT UCOM ONLY
TO FRONT PCB
FROM ATIO
FROM POW
FROM D-IF
TO D-I/O
MAIN PCB (2/6) PLAY CONV
(CONV1) SECTION

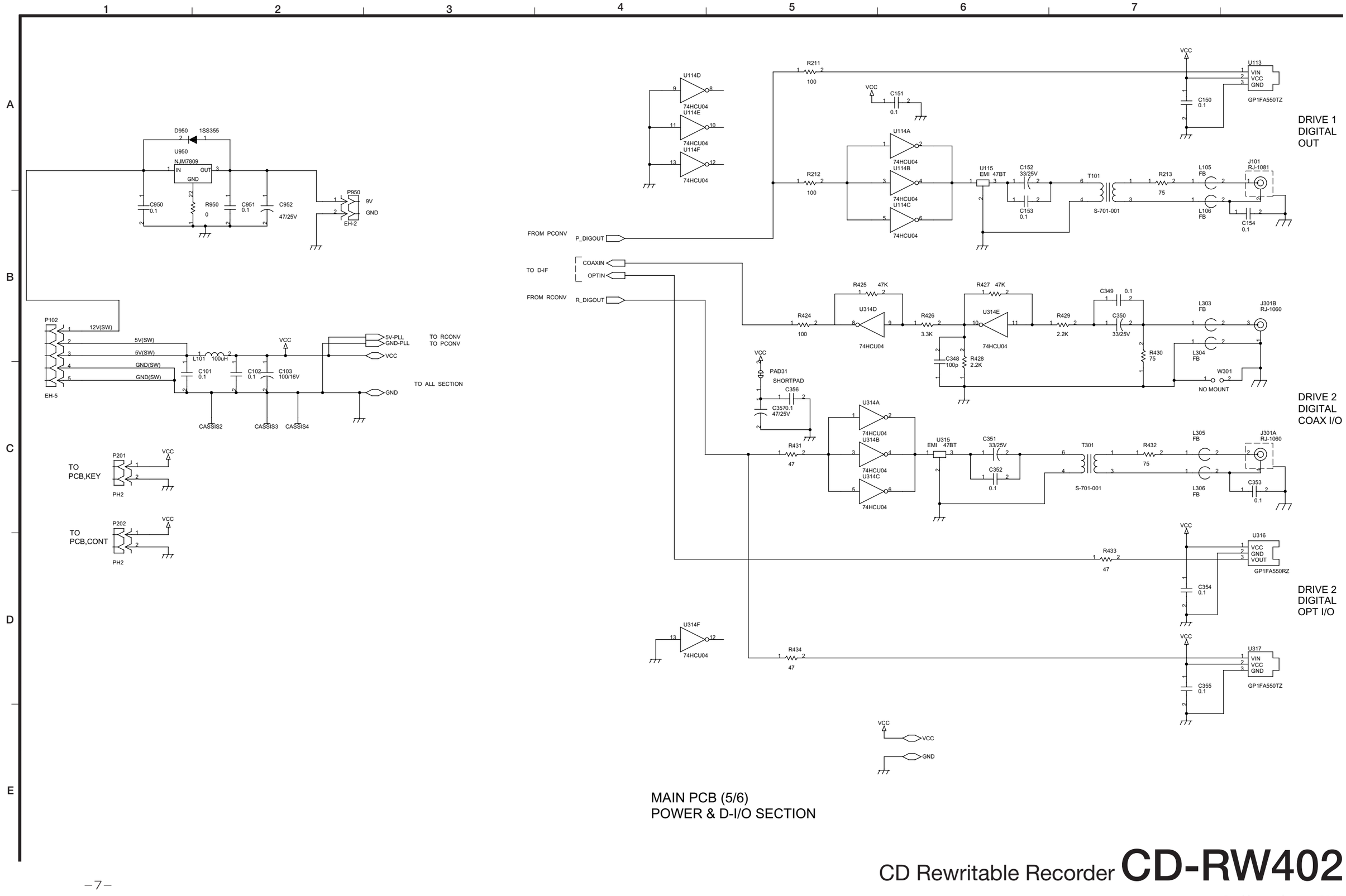


CD Rewritable Recorder **CD-RW402**

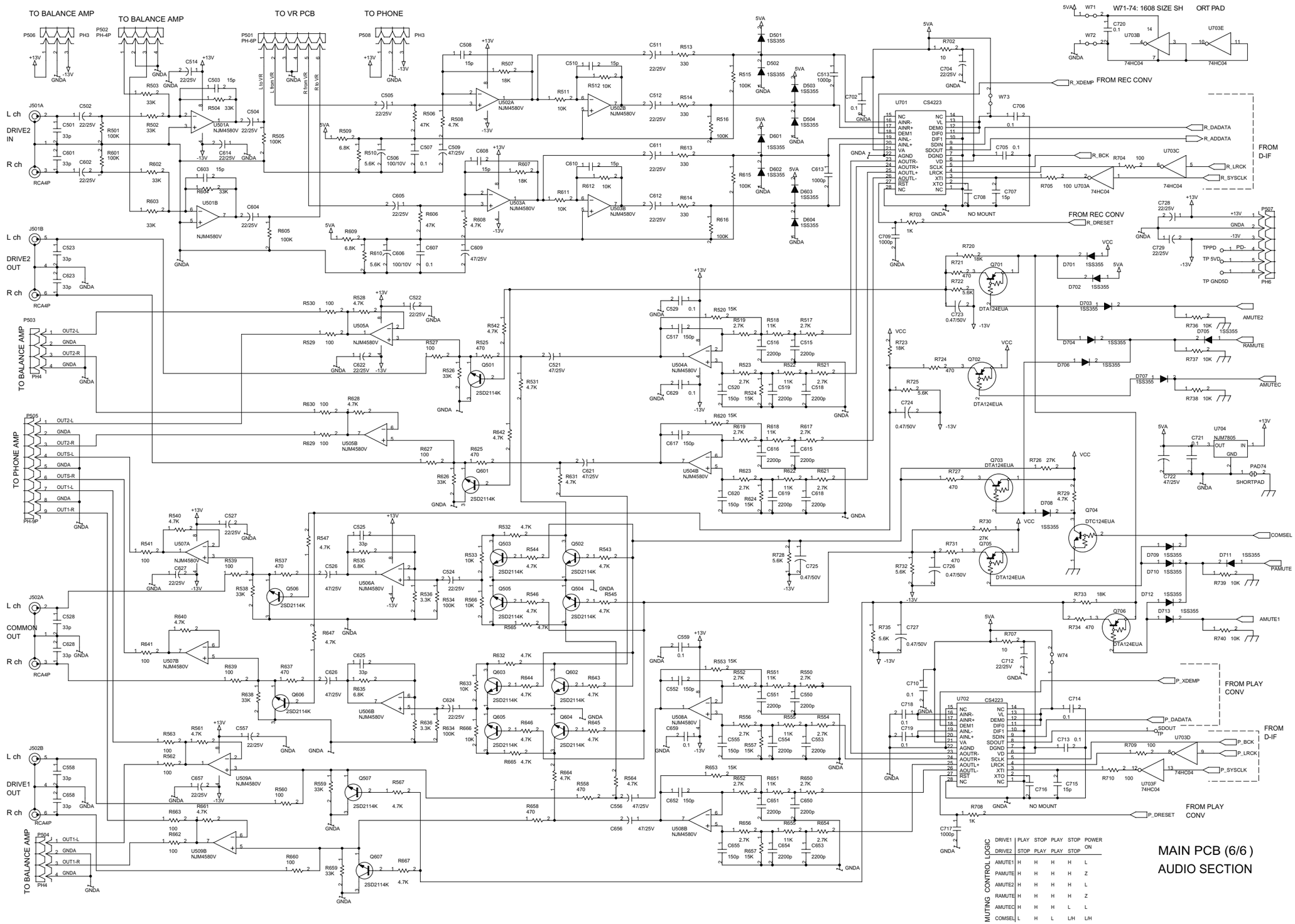
2 nd Issue; August 2005



CD Rewritable Recorder **CD-RW402**



MAIN PCB (5/6)
POWER & D-I/O SECTION


TO BALANCE AMP
TO BALANCE AMP
TO VR PCB
TO PHONE
L ch
DRIVE2 IN
R ch
RCA4P
L ch
DRIVE2 OUT
R ch
RCA4P
TO BALANCE AMP
TO PHONE AMP
TO BALANCE AMP
L ch
COMMON OUT
R ch
RCA4P
L ch
DRIVE1 OUT
R ch
RCA4P
TO BALANCE AMP
NJM4580V
2SD2114K
U701 CS4223
U702 CS4223
FROM REC CONV
R_XDEMP
R_DADATA
R_ADDATA
R_BCK
R_LRCK
R_SYSCLK
FROM D-IF
NO MOUNT
FROM REC CONV
R_DRESET
FROM PLAY CONV
P_XDEMP
P_DADATA
P_BCK
P_LRCK
P_SYSCLK
FROM D-IF
FROM PLAY CONV
P_DRESET
W71-74: 1608 SIZE SH ORT PAD
74HC04
DTA124EUA
NJM7805
SHORTPAD
AMUTE2
RAMUTE
AMUTEC
PAMUTE
AMUTE1
COMSEL
MUTING CONTROL LOGIC
DRIVE1 PLAY STOP PLAY STOP POWER ON
DRIVE2 STOP PLAY PLAY STOP
AMUTE1 H H H H L
PAMUTE H H H H Z
AMUTE2 H H H H L
RAMUTE H H H H Z
AMUTEC H H H L L
COMSEL L H L L/H L/H
MAIN PCB (6/6)
AUDIO SECTION

TEAC TECHNICAL INFORMATION

TASCAM CD-RW402, Substitution of the Drive

No. **0506**
DATE 3rd August 2005

Original drive (CD-W54E) has discontinued then new drive (CD-W58DA) for CD-RW402 V3 is used for substitution. This info introduces how to mount CD-W58DA to original CD-RW402.

Outline of work

- Short dumping resistors on Main PCB
- Modify 40P flat cable
- Replace drive
- Main PCB firmware update
- Drive firmware update
- Mount new tray panel
- Add an insertion owner's manual for CD-RW402 V3

Note:
The production of CD-RW402 V3 has been started from S/No. 0270001 and up.

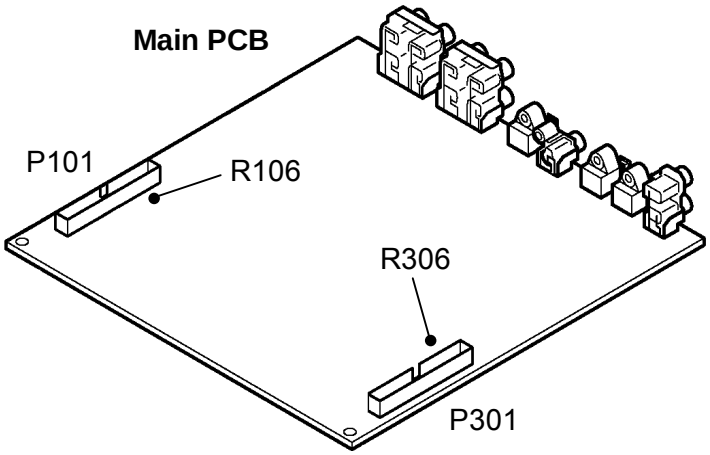
Parts required

Item	Qty	P/No.	Description
Resistor	2		22 ohm (lead type)
New drive	1	V00140000A	CD-W58DA-T00
New tray panel	1	M02038100A	Panel, Tray (2) G RW402 (ASS)
Insertion owner's manual (E)	1	(D00870800A)	Sheet, Insertion CD-RW402 V3
Converter MPU update CD-R	1		"conv0301.mot" written
Drive update CD-R	1		"T58V1td.abf" written

Actual work

1. Short R106 and R306 (22 Ω, chip) on Main PCB.
2. Modify 40P flat cables connecting Main PCB P101/P301 and drive 1/2 with referring to page 2.
3. Replace drive with new.
   Note that new tray panel cannot be mounted at this stage as tray cannot be opened.
4. Update Converter MPU (U104/U304) on Main PCB. (U104 is for drive 1 and U304 for drive 2.)
   Note: Once U104 is updated, the unit does not boot up normally unless U304 is updated.
   A care must be taken not to interrupt the procedure described in page 3.
5. Update drive firmware.
   By updating Converter MPU in the step 4 above, update capability of drive firmware is added now. As new drive is supplied with basic PC condition, drive firmware should be updated.
   Follow the repeated loop procedure steps in page 3.
6. Turn the power of unit on, open the tray then turn the power off. Mount new tray panel.
7. Add an insertion sheet for Version 3.0.

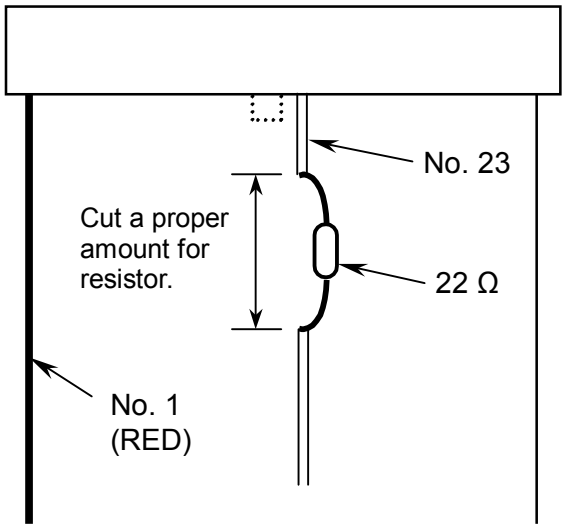
Location of R106/R306 on Main PCB

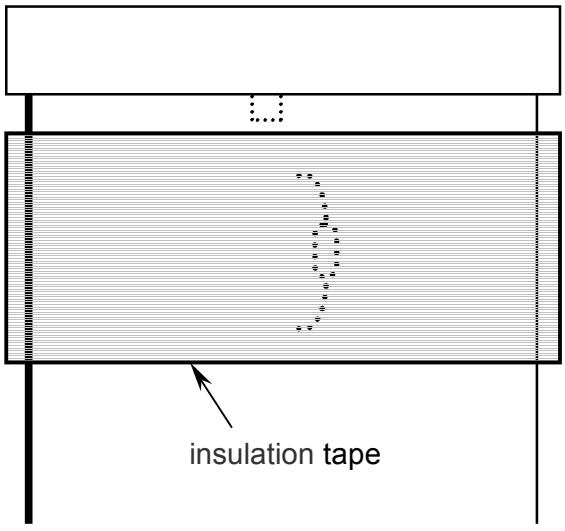


Modify 40 P flat cables

Insert a 22 Ω resistor into No. 23 wire of following cable. (Actually both cables are the same.)
- 40 P flat cable connecting Main PCB P101 and drive 1.
- 40 P flat cable connecting Main PCB P301 and drive 2.

Notice:
1. Resistor should be inserted at Main PCB side (**NOT** drive side) and close to connector as much as possible.
2. Finally wrap the resistor and the cable with insulation tape.





Converter MPU and Drive firmware update procedure

Prepare update Converter CD-R that has "conv0301.mot" written on it.
Prepare update Drive CD-R that has "T58V1tb.abf" written on it.

Preparation:

1. Have two blank CD-R data discs available, as well as a system capable of creating data CDs.
2. Visit the **ROM Data Library** in the TASCAM Service HP website to download both firmware data images and write the firmware file on PC to the blank CD-R discs respectively. (Use the "Disc at once" method that complies with ISO9660 Level 1: MS-DOS compatible)

Notice:

Be careful that the power supply to the unit is not interrupted during the update process otherwise firmware data of the Converter MPU or the drive could be damaged and physical replacement of related part becomes unavoidable.

Procedure:

1. Turn the power on while holding **STOP**, **PLAY** and **READY** of Drive 1 side to enter the test mode. Then the display shows "Front1 (and 2) 01.00" at Drive 1 and Drive 2 respectively.
2. Load the Converter CD-R (or the Drive CD-R) into Drive 1 (or 2 in the next cycles).
3. Confirm "CD" in display blinks. Then press **MENU**.
   ("CXX.XX→XX.XY" is displayed when the Converter CD-R is being loaded.
   "DXX.XX→XX.XY" is displayed when the Drive CD-R is being loaded.)
4. Press **ENTER** then update will start.
   "NOW UPDATE" is displayed and "**.**" at the right most corner blinks.
5. It takes about 1 minute, the display returns to "Front1 01.00" to inform the update finished successfully.
6. Return to step 1 above to update Drive 2 with using the Converter CD-R.
7. Return to step 1 above to update Drive 1 with using the Drive CD-R.
8. Press **STOP** of Drive 1 side to escape the test mode.
9. Return to step 1 above to update Drive 2 with using the Drive CD-R.
10. Press **STOP** of Drive 2 side to escape the test mode.

Drive firmware update on Windows

There is another way to update the drive firmware only by using PC.
Visit the **ROM Data Library** in the TASCAM Service HP website to download firmware data image of "CDW58DA_1TD.exe" into PC.

1. While PC is powered off, connect the CD-W58DA to PC and reboot.
   No need to consider Primary/Secondary and Master/Slave.
2. Double-click on "CDW58DA_1TD.exe" to run.
3. Follow the messages that will appear.

TEAC

TECHNICAL INFORMATION

No. **0701**

DATE 16th February 2007

CD-RW402(V3)/CD-RW2000(V3), Substitution of the Drive

This information relates to previous Tech-Info No. 0505R, 0506R, 0510 and 0511R.

The Drive (CD-W58DA) introduced in both info has been replaced with a RoHS conformity Drive (CD-W58DB) on the V3 products with the following S/Nos (month started production):

CD-RW402V3: S/N 0350001 and after (Nov/2005)
CD-RW2000V3: S/N 0500001 and after (Mar/2006)
Exception: T/C - S/N 0470076 to 047125 (Nov/2005)
All - S/N 0490116 to 049215 (Feb/2006)

Parts required

Item	Qty	P/No.	Description
New bare drive	1	V00141900A	CD-W58DB-T00 G
Drive update on CD-R			"W58db1td.abf" written
Drive update on Windows			"W58db1td.exe"

Visit the **ROM Data Library** on the SVHP to download the both firmware data and follow the update procedure on the previous Tech Info to read the following change:

"T58V1tf.abf" of CD-W58DA Drive => "W58db1td.abf" for CD-W58DB Drive.
"CDW58da1tf.exe" of CD-W58DA Drive => "W58db1td.exe" of CD-W58DB Drive.

Notice:

Do not attempt to write the former CD-W58DA firmware, "T58V1tf.abf" or "CDW58da1tf.exe" onto new CD-W58DB Drive otherwise new Drive becomes totally no response since type of Flash Rom fitted is quite different by the RoHS requirement. These firmware have no capability to identify type of Drive on which targeted to update therefore.

TEAC

TECHNICAL INFORMATION

No. **0511R**

DATE 1st November 2005

TASCAM CD-RW402V3, Converter MPU Upgrade

ROM of the Converter MPU, U104/304 on the Main PCB Assy has been upgraded from Ver 3.01 to Ver 3.02 on the products of S/N 0330001 and up.

Item	P/No.	Description
Converter MPU U104/304	3S0048510A (Ver3.01)	3S0048510B (Ver3.02)

Problem corrected by V3.02

1. A momentary sound gap has been created consistently at the record time of 40:58 seconds when Copy was made from Drive 1.
2. "COPY PROHIBIT" has been resulted at the first track even "COPY ID" was selected to "FREE" regardless of the input source.
3. LCD shows "NO DISC" when UNFINALIZE was operated against CD-RW media on that exactly 99 tracks have been recorded. Once open and close the Tray has been required to recover the 99 tracks read out.
4. "REC ERROR" has occurred when a particular CD was tried to Copy from Drive 1.

Note: Converter MPU has been updated to reduce play speed of Drive 1 from 16 times to 10 times to solve the problem 1. Drive firmware has been updated from Ver 1.TD to Ver 1.TF to solve problem 2., 3. and 4.

How to update Converter MPU and Drive firmware

Prepare update Converter CD-R that has "conv0302mot" written on it.
Prepare update Drive CD-R that has "T58V1tf.abf" written on it.

Preparation:

1. Have two blank CD-R data discs available, as well as a system capable of creating data CDs.
2. Visit the **ROM Data Library** in the TASCAM Service HP website to download both firmware data images and write the firmware file on PC to the blank CD-R discs respectively. (Use the "Disc at once" method that complies with ISO9660 Level 1: MS-DOS compatible)

Notice:

Be careful that the power supply to the unit is not interrupted during the update process otherwise firmware data of the Converter MPU or the drive could be damaged and physical replacement of related part becomes unavoidable.

Procedure:

Updating the Converter MPU Firmware on Drives 1 & 2

1. Turn the power on while simultaneously holding down the **STOP**, **PLAY** and **READY** buttons of Drive 1 to enter the TEST mode. The Drive1 display will show "Front1 01.00" and the Drive2 display will show "Front2 01.00".
2. Load the Converter CD-R into Drive 1.
3. Confirm that the "CD" indicator in the display remains solid and press **MENU**. ("CXX.XX→XX.XY" is displayed while the Converter CD-R is being loaded.)
4. Press **ENTER** (the MULTI DIAL knob) and the update will start. "NOW UPDATE" is displayed and "." At the right most corner of the display blinks.
5. In approximately 1 minute, the display returns to "Front1 01.00" to indicate that the update has finished successfully.
6. Repeat Steps 2 through 5 to update the Converter MPU Firmware of Drive 2.

Updating the Drive Firmware - (Drive 2 only)

1. When "Front2 01.00" is displayed, load the Drive Firmware CD-R into Drive 2.
2. Confirm that the "CD" indicator in the display remains solid and press **MENU**. ("D X.XX→X.XY" is displayed while the Drive Firmware CD-R is being loaded.)
3. Press **ENTER** (the MULTI DIAL knob) and the update will start. "NOW UPDATE" is displayed and "." At the right most corner of the display blinks.
4. In approximately 1 minute, the display returns to "Front2 01.00" to indicate that the update has finished successfully.
5. Press the **STOP** button of Drive 2 to exit the TEST mode.
6. Eject the disc and turn the unit off.

Confirming the Updates

1. Turn the power on while simultaneously holding down the **STOP**, **PLAY** and **READY** buttons of Drive 1 to enter the TEST mode. The Drive1 display will show "Front1 01.00" and the Drive2 display will show "Front2 01.00".
2. Load the Converter CD-R into Drive 1.
3. Confirm that the "CD" indicator in the display remains solid and press **MENU**.
4. Confirm that CXX.XY equals → XX.XY in the display of Drive 1. Press the **STOP** button of Drive2.
5. Eject the Converter CD-R disc from Drive 1 and load it into Drive 2.
6. Confirm that the "CD" indicator in the display remains solid and press **MENU**.
7. Confirm that CXX.XY equals → XX.XY in the display of Drive 2. Press the **STOP** button of Drive2.
8. Eject the Converter CD-R disc from Drive 2 and load the Drive Firmware disc into Drive 2.
9. Confirm that the "CD" indicator in the display remains solid and press **MENU**.
10. Confirm that D X.XY equals → X.XY in the display of Drive 2. Press the **STOP** button of Drive2.
11. Eject the disc and turn the unit off.

Updating Drive firmware on Windows

There is another way to update the drive firmware only by using PC.

Visit the **ROM Data Library** in the TASCAM Service HP website to download firmware data image of "CDW58DA_1TF.exe" into PC.

1. While PC is powered off, connect the CD-W58DA to PC and reboot. No need to consider Primary/Secondary and Master/Slave.
2. Double-click on "CDW58DA_1TF.exe" to run.
3. Follow the messages that will appear.

TECHNICAL INFORMATION

No. **0511**

DATE 20th October 2005

TASCAM CD-RW402V3, Converter MPU Upgrade

ROM of the Converter MPU, U104/304 on the Main PCB Assy has been upgraded from Ver 3.01 to Ver 3.02 on the products of S/N 0330001 and up.

Item	P/No.	Description
Converter MPU U104/304	3S0048510A (Ver3.01)	3S0048510B (Ver3.02)

Problem corrected by V3.02

1. A momentary sound gap has been created consistently at the record time of 40:58 seconds when Copy was made from Drive 1.
2. "COPY PROHIBIT" has been resulted at the first track even "COPY ID" was selected to "FREE" regardless of the input source.
3. LCD shows "NO DISC" when UNFINALIZE was operated against CD-RW media on that exactly 99 tracks have been recorded. Once open and close the Tray has been required to recover the 99 tracks read out.
4. "REC ERROR" has occurred when a particular CD was tried to Copy from Drive 1.

Note: Converter MPU has been updated to reduce play speed of Drive 1 from 16 times to 10 times to solve the problem 1. Drive firmware has been updated from Ver 1.TD to Ver 1.TF to solve problem 2., 3. and 4.

Converter MPU and Drive firmware update procedure

Prepare update Converter CD-R that has "conv0302mot" written on it.
Prepare update Drive CD-R that has "T58V1tf.abf" written on it.

Preparation:

1. Have two blank CD-R data discs available, as well as a system capable of creating data CDs.
2. Visit the **ROM Data Library** in the TASCAM Service HP website to download both firmware data images and write the firmware file on PC to the blank CD-R discs respectively. (Use the "Disc at once" method that complies with ISO9660 Level 1: MS-DOS compatible)

Notice:

Be careful that the power supply to the unit is not interrupted during the update process otherwise firmware data of the Converter MPU or the drive could be damaged and physical replacement of related part becomes unavoidable.

Procedure:

1. Turn the power on while holding **STOP**, **PLAY** and **READY** of Drive 1 side to enter the test mode. Then the display shows “Front1 (and 2) 01.00” at Drive 1 and Drive 2 respectively.
2. Load the Converter CD-R (or the Drive CD-R) into Drive 1 (or 2 in the next cycles).
3. Confirm “CD” in display blinks. Then press **MENU**.
   (“CXX.XX→XX.XY” is displayed when the Converter CD-R is being loaded.
   “DXX.XX→XX.XY” is displayed when the Drive CD-R is being loaded.)
4. Press **ENTER** then update will start.
   “NOW UPDATE” is displayed and “**.**” at the right most corner blinks.
5. It takes about 1 minute, the display returns to “Front1 01.00” to inform the update finished successfully.
6. Return to step 1 above to update Drive 2 with using the Converter CD-R.
7. Return to step 1 above to update Drive 1 with using the Drive CD-R.
8. Press **STOP** of Drive 1 side to escape the test mode.
9. Return to step 1 above to update Drive 2 with using the Drive CD-R.
10. Press **STOP** of Drive 2 side to escape the test mode.

Drive firmware update on Windows

There is another way to update the drive firmware only by using PC.
Visit the **ROM Data Library** in the TASCAM Service HP website to download firmware data image of “CDW58DA_1TF.exe” into PC.

1. While PC is powered off, connect the CD-W58DA to PC and reboot.
   No need to consider Primary/Secondary and Master/Slave.
2. Double-click on “CDW58DA_1TF.exe” to run.
3. Follow the messages that will appear.

TEAC

TECHNICAL INFORMATION

TASCAM CD-RW402, Substitution of the Drive

No. **0506R**
DATE 1st November 2005

Original drive (CD-W54E) has discontinued then new drive (CD-W58DA) for CD-RW402 V3 is used for substitution. This info introduces how to mount CD-W58DA to original CD-RW402.

Outline of work

- Short dumping resistors on Main PCB
- Modify 40P flat cable
- Replace drive
- Main PCB firmware update
- Drive firmware update
- Mount new tray panel
- Add an insertion owner's manual for CD-RW402 V3

Note:
The production of CD-RW402 V3 has been started from S/No. 0270001 and up.

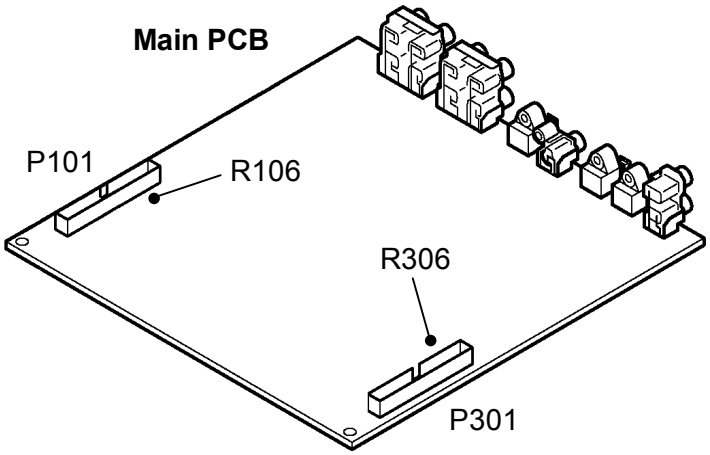
Parts required

Item	Qty	P/No.	Description
Resistor	2		22 ohm (lead type)
New drive	1	V00140000A	CD-W58DA-T00
New tray panel	1	M02038100A	Panel, Tray (2) G RW402 (ASS)
Insertion owner's manual (E)	1	(D00870800A)	Sheet, Insertion CD-RW402 V3
Converter MPU update CD-R	1		"conv0301.mot" written
Drive update CD-R	1		"T58V1td.abf" written

Actual work

1. Short R106 and R306 (22 Ω, chip) on Main PCB.
2. Modify 40P flat cables connecting Main PCB P101/P301 and drive 1/2 with referring to page 2.
3. Replace drive with new.
   Note that new tray panel cannot be mounted at this stage as tray cannot be opened.
4. Update Converter MPU (U104/U304) on Main PCB. (U104 is for drive 1 and U304 for drive 2.)
   Note: Once U104 is updated, the unit does not boot up normally unless U304 is updated.
   A care must be taken not to interrupt the procedure described in page 3.
5. Update drive firmware.
   By updating Converter MPU in the step 4 above, update capability of drive firmware is added now. As new drive is supplied with basic PC condition, drive firmware should be updated.
   Follow the repeated loop procedure steps in page 3.
6. Turn the power of unit on, open the tray then turn the power off. Mount new tray panel.
7. Add an insertion sheet for Version 3.0.

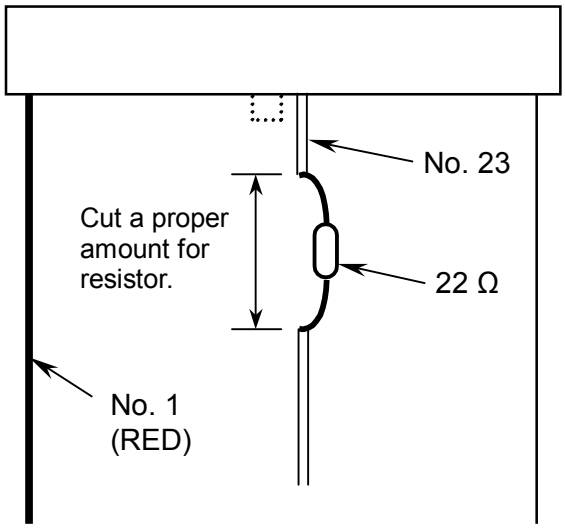
Location of R106/R306 on Main PCB

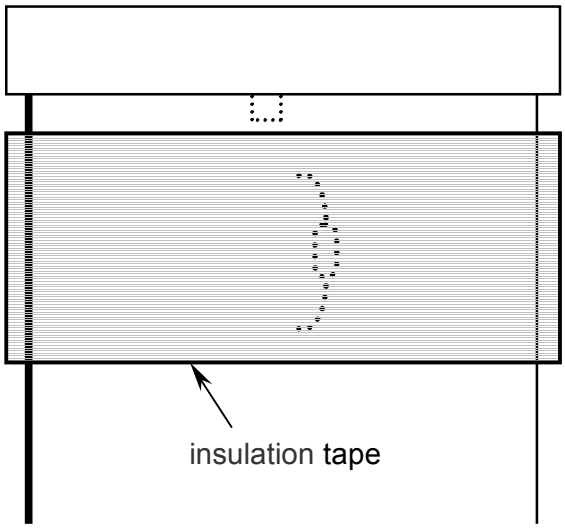


Modify 40 P flat cables

Insert a 22 Ω resistor into No. 23 wire of following cable. (Actually both cables are the same.)
- 40 P flat cable connecting Main PCB P101 and drive 1.
- 40 P flat cable connecting Main PCB P301 and drive 2.

Notice:
1. Resistor should be inserted at Main PCB side (**NOT** drive side) and close to connector as much as possible.
2. Finally wrap the resistor and the cable with insulation tape.





How to update Converter MPU and Drive firmware

Prepare update Converter CD-R that has "conv0301.mot" written on it.
Prepare update Drive CD-R that has "T58V1tb.abf" written on it.

Preparation:

1. Have two blank CD-R data discs available, as well as a system capable of creating data CDs.
2. Visit the **ROM Data Library** in the TASCAM Service HP website to download both firmware data images and write the firmware file on PC to the blank CD-R discs respectively. (Use the "Disc at once" method that complies with ISO9660 Level 1: MS-DOS compatible)

Notice:

Be careful that the power supply to the unit is not interrupted during the update process otherwise firmware data of the Converter MPU or the drive could be damaged and physical replacement of related part becomes unavoidable.

Procedure:

Updating the Converter MPU Firmware on Drives 1 & 2

1. Turn the power on while simultaneously holding down the **STOP**, **PLAY** and **READY** buttons of Drive 1 to enter the TEST mode. The Drive1 display will show "Front1 01.00" and the Drive2 display will show "Front2 01.00".
2. Load the Converter CD-R into Drive 1.
3. Confirm that the "CD" indicator in the display remains solid and press **MENU**. ("CXX.XX→XX.XY" is displayed while the Converter CD-R is being loaded.)
4. Press **ENTER** (the MULTI DIAL knob) and the update will start. "NOW UPDATE" is displayed and "." At the right most corner of the display blinks.
5. In approximately 1 minute, the display returns to "Front1 01.00" to indicate that the update has finished successfully.
6. Repeat Steps 2 through 5 to update the Converter MPU Firmware of Drive 2.

Updating the Drive Firmware - (Drive 2 only)

1. When "Front2 01.00" is displayed, load the Drive Firmware CD-R into Drive 2.
2. Confirm that the "CD" indicator in the display remains solid and press **MENU**. ("D X.XX→X.XY" is displayed while the Drive Firmware CD-R is being loaded.)
3. Press **ENTER** (the MULTI DIAL knob) and the update will start. "NOW UPDATE" is displayed and "." At the right most corner of the display blinks.
4. In approximately 1 minute, the display returns to "Front2 01.00" to indicate that the update has finished successfully.
5. Press the **STOP** button of Drive 2 to exit the TEST mode.
6. Eject the disc and turn the unit off.

Confirming the Updates

1. Turn the power on while simultaneously holding down the **STOP**, **PLAY** and **READY** buttons of Drive 1 to enter the TEST mode. The Drive1 display will show "Front1 01.00" and the Drive2 display will show "Front2 01.00".
2. Load the Converter CD-R into Drive 1.
3. Confirm that the "CD" indicator in the display remains solid and press **MENU**.
4. Confirm that CXX.XY equals → XX.XY in the display of Drive 1. Press the **STOP** button of Drive2.
5. Eject the Converter CD-R disc from Drive 1 and load it into Drive 2.
6. Confirm that the "CD" indicator in the display remains solid and press **MENU**.
7. Confirm that CXX.XY equals → XX.XY in the display of Drive 2. Press the **STOP** button of Drive2.
8. Eject the Converter CD-R disc from Drive 2 and load the Drive Firmware disc into Drive 2.
9. Confirm that the "CD" indicator in the display remains solid and press **MENU**.
10. Confirm that D X.XY equals → X.XY in the display of Drive 2. Press the **STOP** button of Drive2.
11. Eject the disc and turn the unit off.

Updating Drive firmware on Windows

There is another way to update the drive firmware only by using PC.
Visit the **ROM Data Library** in the TASCAM Service HP website to download firmware data image of "CDW58DA_1TD.exe" into PC.

1. While PC is powered off, connect the CD-W58DA to PC and reboot.
   No need to consider Primary/Secondary and Master/Slave.
2. Double-click on "CDW58DA_1TD.exe" to run.
3. Follow the messages that will appear.