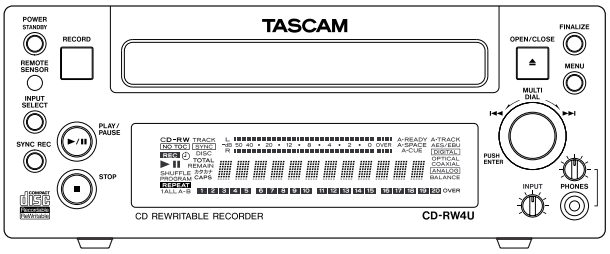


TASCAM

TEAC Professional Division

SERVICE MANUAL

CD-RW4U

CD Rewritable Recorder

Professional

COMPACT disc Recordable ReWritable

CONTENTS

目次

INSTRUCTIONS FOR SERVICE PERSONNEL

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

Effective : May, 2001

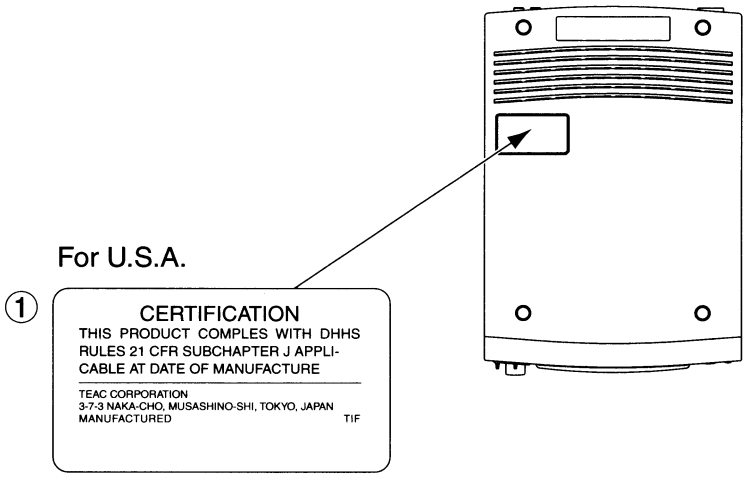
S-0040

1. SAFETY INFORMATION

This product has been designed and manufactured according to FDA regulations "title 21, CFR, chapter 1, subchapter J, based on the Radiation Control for Health and Safety Act of 1968", and is classified as a class 1 laser product. There is no hazardous invisible laser radiation during operation because invisible laser radiation emitted inside of this product is completely confined in the protective housings.
The label required in this regulation is shown ①.

● **CAUTION**

USE OF CONTROLS OR ADJUSTMENT OR PERFORMANCE OF PROCEDURES OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.



Optical pickup: Type: KRS-202A or KRS-220B
Manufacturer : SONY Corporation
Laser output : Less than 0.1 mW (Play) and 32 mW (Record) on the objective lens
Wavelength : 777 - 787 nm

2. SPECIFICATIONS

仕様

Recording media type : CD-R, CD-RW, CD-R-DA, CD-RW-DA
Recording resolution : 16-bit linear
Recording sampling frequency : 44.1 kHz
Input sampling frequency : 32 kHz — 48 kHz
Frequency response :
20 Hz — 20 kHz (playback ±0.8 dB, recording ±1.0 dB)
S/N ratio : > 88 dB (playback), > 83 dB (recording)
Dynamic range : > 88 dB (playback), > 83 dB (recording)
Total harmonic distortion : < 0.012% (playback), < 0.015% (recording)
Channel separation : 80dB (playback: 1kHz), 70dB (recording: 1kHz)
Wow & flutter : Unmeasurable (< 0.001%)

Analog inputs : Unbalanced RCA
Nominal input level : –10 dBV (FS –16 dB)
Maximum input level : +6 dBV
Input impedance : 20 kΩ
Analog outputs : Unbalanced RCA
Nominal output level : –10 dBV (FS –16 dB)
Maximum output level : +6 dBV
Output impedance : -1 kΩ
Headphone output : 3.5 mm stereo
Maximum output level : 10 mW + 10mW (into 32 Ω)
Digital input (COAXIAL): RCA
IEC60958 TYPE I/II
Digital output (COAXIAL): RCA
IEC60958 TYPE II

Voltage requirements :
USA/Canada : 120 VAC, 60 Hz
U.K./Europe : 230 VAC, 50 Hz
Australia : 240 VAC, 50 Hz
Power consumption :
14W (120V)
16W (230V – 240V)
Dimensions (w x d x h) :
215 x 310 x 83 (mm)
8.5 x 12.2 x 3.3 (in)
Weight : 3.3kg (7.25lbs)
Operating temperature : 5°C to 35°C (41°F to 95°F)

USB interface : USB 1.1
Types of disc read :
CD, CD-DA, CD-R, CD-RW (including 80 minute media)
Read speed : Maximum 12Mbps (USB full speed data transfer)
6 x (data), 5 x (audio) *
* data transfer rate is dependent on other operations taking place at the same time.
Types of disc that can be written :
CD-R, CD-RW, CD-R-DA, CD-RW-DA (up to 80-minute media)
Write speed :
CD-R : 4x, 2x, 1x
CD-RW : 4x, 2x, 1x
Writable formats :
CD-DA (including CD-TEXT), CD-ROM (MODE 1), CD-ROM XA MODE 2 (FORM 1, FORM 2), Photo CD™ multi-session, CD-I, Video CD, CD Extra (CD Plus)

記録ディスク : CD-R、CD-R-DA、CD-RW、CD-RW-DA
量子化ビット数 : 16 bit リニア
録音サンプリング周波数 : 44.1 kHz
入力サンプリング周波数 : 32 kHz ～ 48 kHz
周波数特性 :
20 Hz ～20 kHz
（再生時 : ± 0.8 dB 、記録時 : ± 1.0 dB）
S/N 比 : 88 dB 以上（再生時）、83 dB 以上（記録時）
ダイナミックレンジ :
88 dB 以上（再生時）、83 dB 以上（記録時）
歪率 : 0.012 %以下（再生時）、0.015 %以下（記録時）
チャンネルセパレーション :
80 dB 以上（再生時, 1 KHz）、70 dB 以上（記録時, 1 kHz）
ワウフラッター : 測定限界以下（0.001 %以下）

アナログ入力 : RCA ピン（不平衡）
基準入力レベル : － 10 dBV（FS － 16 dB）
最大入力レベル : ＋6 dBV
入力インピーダンス : 20 kΩ
アナログ出力 : RCA ピン（不平衡）
基準出力レベル : － 10 dBV（FS － 16 dB）
最大出力レベル : ＋6 dBV
出力インピーダンス : 1 kΩ
ヘッドホン出力 : 3.5 φステレオ
最大出力レベル : 10 mW ＋ 10 mW（32 Ω負荷）
デジタル入力（COAXIAL）: RCA ピン
IEC-60958 Type I/II
デジタル出力（COAXIAL）: RCA ピン
IEC-60958 Type II

電源 : 100 VAC, 50 － 60 Hz
消費電力 : 14 W
外形寸法（幅×高さ×奥行き）: 215 × 83 × 310 mm
質量 : 3.3 kg
動作保証温度 : 5 ℃～ 35 ℃

USB インターフェース : USB1.1
読み込み対応 CD : CD、CD-DA、CD-R、CD-RW
読み込み速度 : 最大 12 Mbps（= USB 最大転送速度）
[6 倍速（データ CD）／ 5 倍速（オーディオ CD)相当]
* 実際の転送速度は、動作環境に依存します。
書き込み対応 CD : CD-R、CD-RW、CD-R-DA、CD-RW-DA
(80 分メディア対応)
書き込み速度 (2 倍速を推奨) :
CD-R : 4 ／ 2 ／ 1 倍速
CD-RW : 4 ／ 2 ／ 1 倍速
書き込みフォーマット :
CD-DA（CD-TEXT 対応）、CD-ROM（MODE 1）、
CD-ROM XA MODE 2（FORM 1、FORM 2）
Photo CD™ マルチセッション、CD-I、Video CD、
CD Extra（CD Plus）
書き込み方式 :
トラックアットワンス、ディスクアットワンス、
マルチセッション、パケットライト
* 書き込みの際には、他の USB 機器を動作させないでください。

Writing modes :
Track at Once (TAO), Disc at Once(DAO), multi-session, packet write
Average seek time : 85ms
Data buffer : 2 MB
Supported platforms :
PC/AT platform :
Windows 98 SE, Windows Me, Windows 2000
Host computer must be equipped with a UHCI USB interface controller
Macintosh platform :
Mac OS 9
iBook, iMac or Power Macintosh G3/G4 models

Supplied accessories :
RC-RW700 remote control unit, 4 x feet for vertical mounting, USB cable, 1/4" to 3.5 mm stereo headphone adapter, 3.5" diskette containing driver software, CD-ROM containing CD-writing software, 2 x AA batteries, Owner's manual, USB Operation Guide, Quick Start guide

● Specifications and appearance subject to change without notice.
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平均シーク時間：85 msec
データバッファ：2 MB

動作環境（PC/AT 互換機）：
対応 OS：
Windows 98 SE 、Windows Me 、Windows 2000
対応機種：
USB インターフェイス（UHCI）を備えたコンピュータ
動作環境（Macintosh）：
対応 OS：Mac OS 9
対応機種：iMac 、iBook 、Power Macintosh G3/G4

付属品:
RC-RW700 リモコン× 1、縦置き用の足× 4、USB ケーブル× 1、標準（φ 6.3）→ミニ（φ 3.5）プラグ変換アダプター× 1、フロッピーディスク（ドライブソフトウエア）× 1 CD-ROM（CD ライティングソフトウエア）× 1、単 3 乾電池× 2、取扱説明書× 1、セットアップガイド× 1

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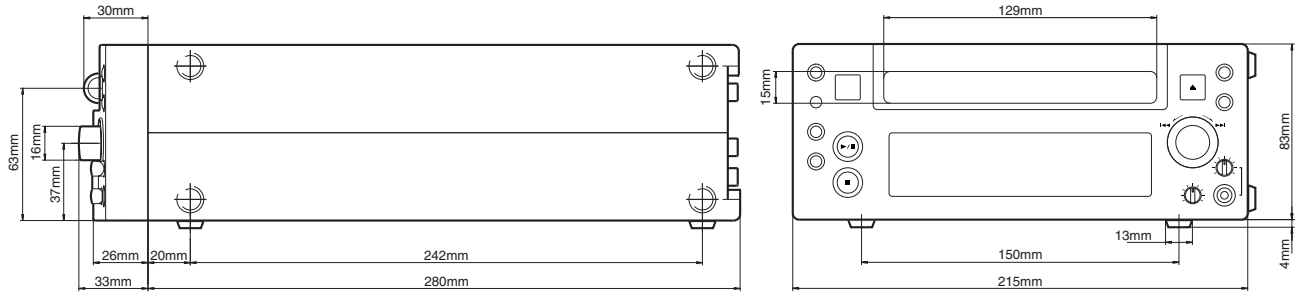
Macintosh 、Mac 、Power Macintosh 、iMac 、iBook 、Mac OS は、米国 Apple Computer, Inc.の商標または登録商標です。



3. ADJUSTMENTS AND CHECKS
調整と確認

3-1. How to enter test mode

1. In Standby mode, press and hold the STOP + PLAY/PAUSE + PRECORD keys simultaneously for 5 seconds. The display will show the model name and the system controller's version number, and the test mode is initiated.
2. Press the STOP key to exit from the test mode and return to the standby mode.

3-2. Checks in test mode

3-2-1. Front key check

1. Press the PLAY/PAUSE key to enter the front key check mode.
2. The display shows the name of each key to be checked; press the corresponding key.
   When the check result of the key is OK, the display shows another key name. When the result is No Good, the display continues to show the same key name.
3. The display finally shows "Dial50". Check the MULTI DIAL so that the displayed figure increases when the dial is rotated clockwise and decreases when it is rotated counter-clockwise.
4. Press the PLAY/PAUSE key to exit from the front key check mode and return to the Version number display mode.

3-2-2. Display check

1. Press the MENU key to enter the display check mode.
2. Press MENU key a few times and ensure that each press lights the display blocks one after another.
3. When all the indicators are lit, press the MENU key to exit from the display check mode and return to the Version number display mode.

3-2-3. EEPROM default setting

The following operation writes the default data in the EEPROM and checks the write data automatically.

1. Press the FINALISE key.
   When the default data is written correctly, the display shows "EEPROM OK !!". If not, it shows "EEPROM NG!!".
2. Press the FINALISE key again to return to the Version number display mode.

3-2-4. Converter MPU Version No. display

1. When the SYNC REC key is pressed, the display shows the converter MPU version number "CONV **.**".
2. Press the SYNC REC key again to return to the Version number display mode.

3-1. テストモードの入り方

1. スタンバイモードの状態で、
   STOP キー＋ PLAY/PAUSE キー＋ RECORD キーを 5 秒間押し続けると、表示部に機種名とシスコンの Version No. が表示されテストモードに入る。
2. STOP キーを押すと、テストモードは終了しスタンバイモードに戻る。

3-2. テストモードでのチェック

3-2-1. フロントキーチェック

1. PLAY/PAUSE キーを押し、フロントキーチェックモードに入る。
2. 表示部にチェックするキーの名称が表示されるので、そのキーを押す。チェック OK なら次のキーの名称が表示され、NG なら表示は変化しない。
3. 一通りキーの確認が終了すると、ディスプレイに "dial50" と表示される。MULTI DIAL を回し、表示の数字が右回しで増加、左回しで減少することを確認する。
4. PLAY/PAUSE キーを押すと、フロントキーチェックモードを終了し Version No. 表示に戻る。

3-2-2. ディスプレイチェック

1. MENU キーを押し、ディスプレイチェックモードに入る。
2. MENU キーを押すたびに、表示部がブロックごとに点灯することを確認する。
3. 表示部が全点灯した状態から MENU キーを押すと、ディスプレイチェックモードを終了し Version No. 表示に戻る。

3-2-3. EEPROM デフォルト設定

EEPROM にデフォルト値を書き込み、自動的に書き込みチェックを行う。

1. FINALIZE キーを押す。
   このとき、正しく書き込めていれば、表示部に "EEPROM OK !!" と表示され、不良の場合は "EEPROM NG !!" と表示される。
2. 再度 FINALIZE キーを押すと、Version No. 表示に戻る。

3-2-4. コンバータマイコンバージョン表示

1. SYNC REC キーを押すと、コンバータマイコンのバージョンを表示 "CONV **.**" する。
2. 再度 SYNC REC キーを押すと、Version No. 表示に戻る。

3-2-5. Drive unit Version No. display

1. When the INPUT SELECT key is pressed, the display shows the drive unit version number “DRV **.**”.
2. Press the INPUT SELECT key again to return to the Version number display mode.

3-2-6. Total recording time display

1. When the REC key is pressed, the display shows the time in which the pickup outputs the recording power in the unit of hour “R_TM=******h”.
2. Press the REC key again to return to the Version number display mode.

3-3. Adjusting the level difference in anlog input between the left and right channels

1. Using the INPUT SELECT key, select ANALOG for input.
2. Apply a 1 kHz, –10 dBV square wave signal to the ANALOG IN jack.
3. Adjust the INPUT control knob situated on the front panel so that the output level of the right channel reads –10 dBV.
4. Adjust the VR751 potentiometer (a variable resistor to fine adjust the left channel level) on the BAL PCB so that there is no level difference between the right and left channels.
   In spec-precision terms, the level difference between the channels is 0+/-0.5 dB when they are handling practically the same input and output levels.

3-2-5. ドライブバージョン表示

1. INPUT SELECT キーを押すと、ドライブユニットのバージョンを表示“DRV **.**”する。
2. 再度 INPUT SELECT キーを押すと、Version No. 表示に戻る。

3-2-6. 記録積算時間表示

1. RECORD キーを押すと、ピックアップが記録パワーを出力した時間を表示“R_TM=******h”する。
   （単位： hour）
2. 再度 RECORD キーを押すと、Version No. 表示に戻る。

3-3. アナログ入力 L-R チャンネル間レベル差調整

1. INPUT SELECT キーで、ANALOG 入力を選択する。
2. ANALOG IN 端子に、1 kHz, －10 dBV の正弦波を入力する。
3. R チャンネルの出力レベルが、－10 dBV になるようにフロントパネルの INPUT つまみを調整する。
4. R チャンネルと L チャンネルの出力レベルが等しくなるように、BAL PCB 上の半固定抵抗 VR751（L チャンネル微調整 VR）を調整する。
   尚、チャンネル間レベル差の規格は、入出力レベルがほぼ等しい状態で、0 ± 0.5 dB です。

3-4. Audio checks オーディオ確認

3-4-1. Playback performance 再生系

Mode : PLAY
Measurement point : ANALOG OUT

ITEM 項目	TEST DISC テストディスク	PLAYBACK SIGNAL 再生信号	SPECIFICATIONS 規格	REMARKS 備考
1. **Playback level** **再生レベル**	MCD-111 Track 2	1 kHz, 0 dB	2.0 ± 0.4 V	
2. **Playback frequency responce** **再生周波数特性**	MCD-111 Track 3–6	20 Hz–20 kHz, 0 dB	0 ± 0.8 dB	reference : 1 kHz 1 kHz 基準
3. **Playback distortion** **再生歪率**	MCD-111 Track 2	1 kHz, 0 dB	0.012 % or less	20 kHz LPF
4. **Playback SN ratio** **再生 SN 比**	MCD-111 Track 7	– ∞ dB	88 dB or better	20 kHz LPF + IEC-A
5. **Playback channel separation** **再生チャンネルセパレーション**	MCD-111 Track 8, 10	1 kHz, 0 dB	80 dB or better	IEC-A

3-4-2. Monitor performance モニター系

Mode : REC Monitor
Input terminal : ANALOG IN
Measurement point : ANALOG OUT

ITEM 項目	INPUT SIGNAL 入力信号	SPECIFICATIONS 規格	REMARKS 備考
1. **Record level** **録音レベル**	1 kHz, +6 dBV	+6 dBV ± 2 dB	By pressing the MENU key, select "VOLUME **dB", then turn the MULTI DIAL knob for 0 dB. Turn the INPUT control to position at which the "OVER" segments of the level meter is just about to light. Once done, keep this adjustment unchanged until all the necessary measurements have been made. MENU キーを押して "VOLUME **dB" を選び、MULTI DIAL を回して 0 dB に設定する。 INPUT つまみを回して、レベルメーターの "OVER" が点灯する直前になるように調整する。 調整後は全ての測定が終わるまでこの状態にしておく。
2. **Monitor frequency responce** **モニター周波数特性**	20 Hz–20 kHz, –10 dBV	0 ± 1 dB	reference : 1 kHz 1 kHz 基準
3. **Monitor SN ratio** **モニター SN 比**		83 dB or better	Ratio of output level at +6 dB input to noise level + 6 dBV 入力時の出力レベルとノイズレベルとの比 20 kHz LPF + IEC-A
4. **Monitor channel separation** **モニターチャンネルセパレーション**	L (R) ch : 1 kHz, +6 dBV R (L) ch : No signal	70 dB or better	Ratio of Lch output level to Rch output level Lch 出力と Rch 出力の比 IEC-A
	L ch : 10 kHz, +6 dBV R ch : No signal	55 dB or better	
5. **Monitor distortion** **モニター歪率**	1 kHz, +5 dBV	0.015 % or better	20 kHz LPF

PARTS LIST SECTION

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with ∗ require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in the manual.
- ⚠Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J] : JAPAN [US/C] : U.S.A./CANADA [K] : KOREA [E] : EUROPE
  [UK] : U.K. [A] : AUSTRALIA

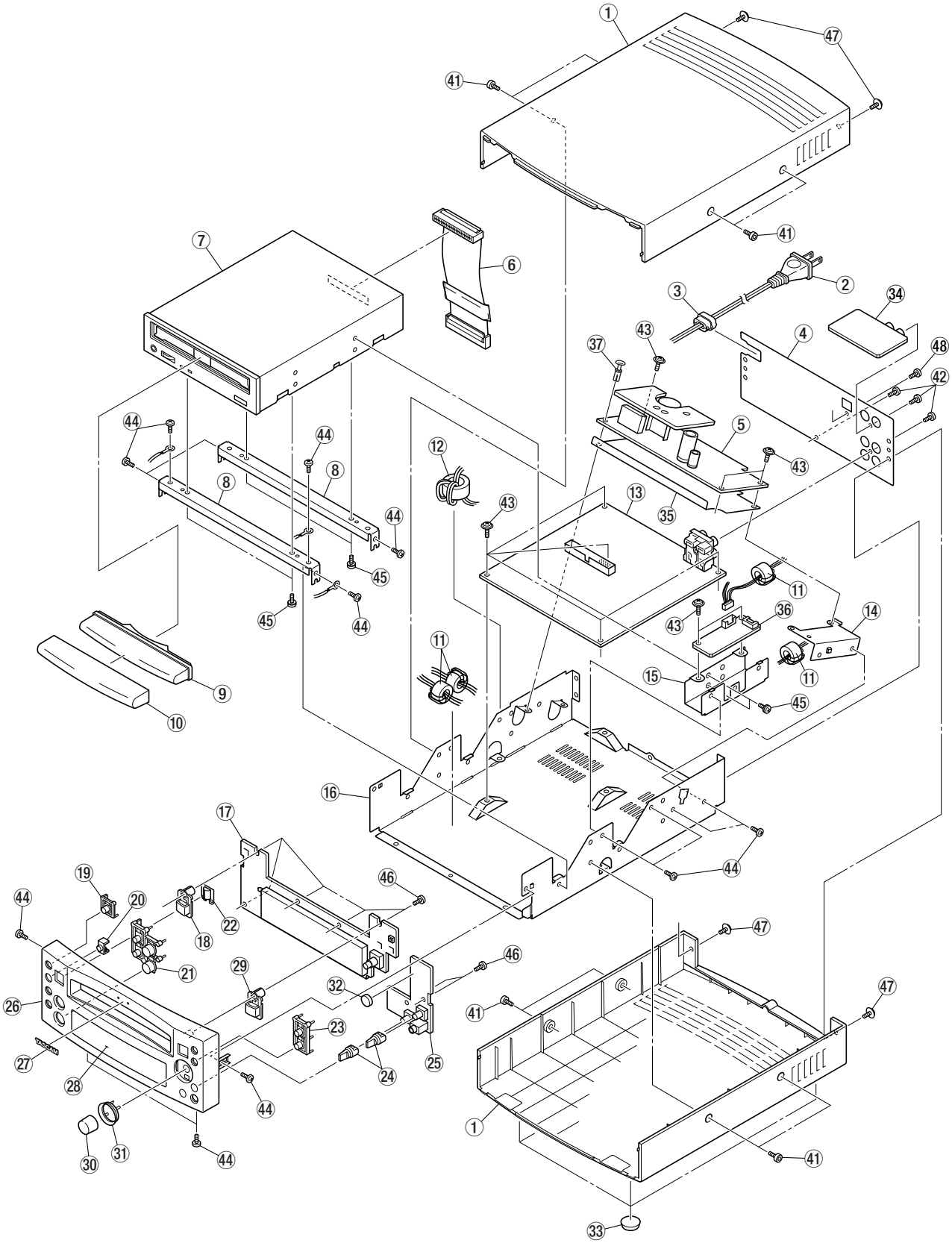
注 意

- プリント基板は部品面が示されています。
- ＊印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品及び品番のない部品は供給しません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠は安全重要部品です。
  交換する時は必ずティアック指定の部品を使用してください。
- 仕向先
  [J] : JAPAN [US/C] : U.S.A./CANADA [K] : KOREA [E] : EUROPE
  [UK] : U.K. [A] : AUSTRALIA

4. EXPLODED VIEW AND PARTS LIST

分解図とパーツリスト

EXPLODED VIEW-1



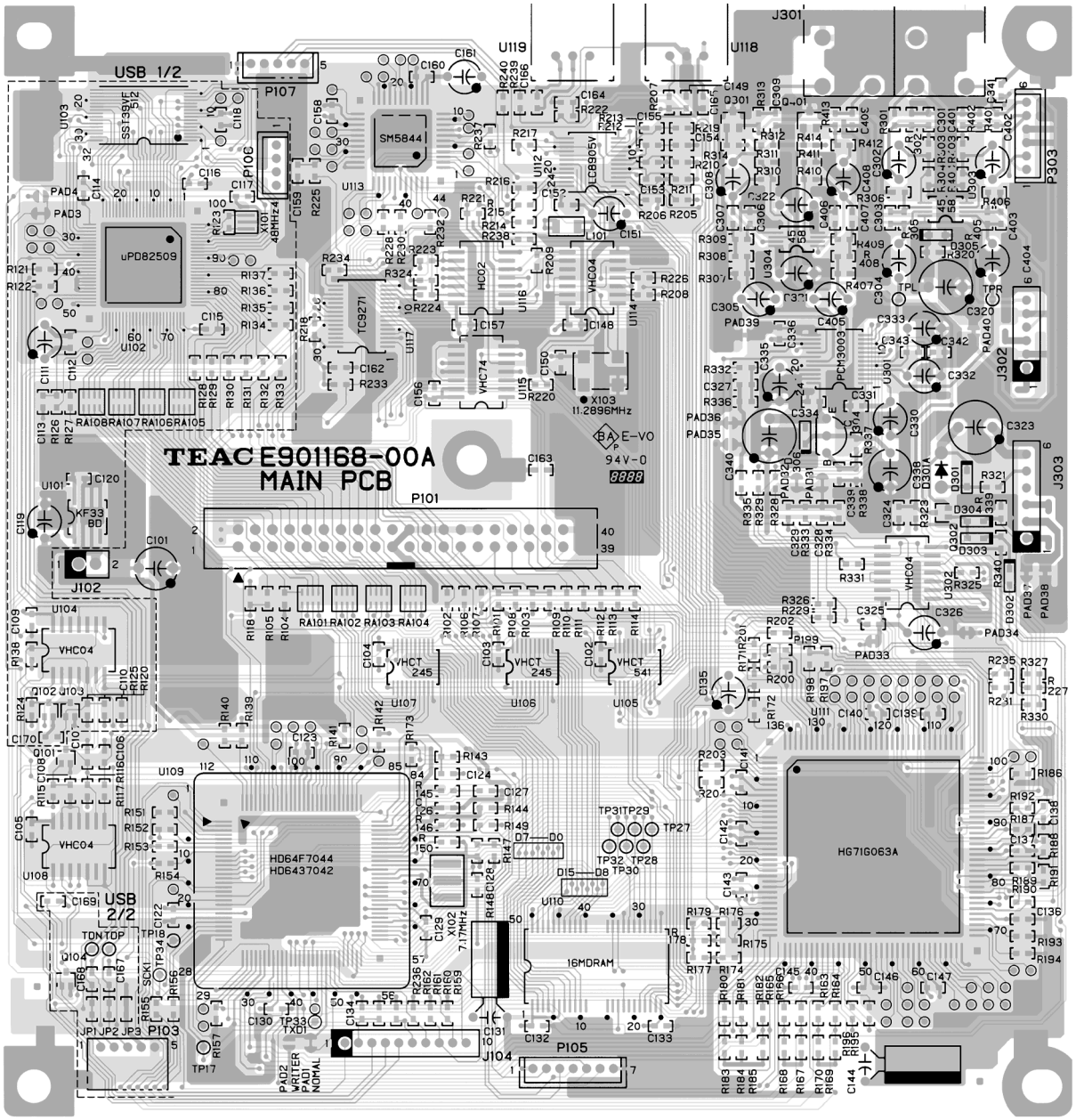
EXPLODED VIEW-1

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	*M01223710A	COVER,OUTER	
1- 2	*3E002120	POWER CORD [J]	
	*3E009230	POWER CORD [US/C]	
	*3E015170	POWER CORD [K]	
	*3E015160	POWER CORD [E]	
	*3E015140	POWER CORD [UK]	
	*3E015150	POWER CORD [A]	
1- 3	*3M000880	BUSHING,#2271	
1- 4	*M01223610A	REAR PANEL	
1- 5	*E00646900A	SW RGLTD PS,EO-0005 [J,US/C]	
	*E00646800A	SW RGLTD PS,EO-0004 [K,E,UK,A]	
1- 6	*E00637600A	HARNESS ASSY,DRIVE-MAIN 40P	
1- 7	V00100900A	CD-W54E-A91	
1- 8	*M01223300A	BRACKET,DRIVE	
1- 9	*M01224110A	ESCUTCHEON,TRAY	
1-10	*M01224020A	PANEL,TRAY	
1-11	*3E002720	FERRITE CORE,K5AT 18.3X10X10	
1-12	*3E010000	FERRITE CORE,B18T 25X12X15	
1-13	*E95116820A	PCB,ASSY MAIN	
1-14	*M01279800A	BRACKET,PCB POWER	
1-15	*M01280800A	SHIELD PLATE	
1-16	*M01223200A	CHASSIS,MAIN	
1-17		PCB ASSY,FRONT ·····	PCB ASSY,GATHER FRONT (Refer to page 14)
1-18	M01224810A	BUTTON,REC	
1-19	M01224600A	BUTTON,B	
1-20	M01248600A	FILTER,RMTCONT SNSR	
1-21	M01224700A	BUTTON,C	
1-22	M01224900A	LENS,BUTTON REC	
1-23	M01224500A	BUTTON,A	
1-24	M01224200A	KNOB,D9 PHONE	
1-25		PCB ASSY,PH/VR ·····	PCB ASSY,GATHER FRONT (Refer to page 14)
1-26	M01279100A	FRONT PANEL	
1-27	*9260271101	BADGE TASCAM SILVER	
1-28	M01223910A	WINDOW,FL	
1-29	M01224820A	BUTTON,O/C	
1-30	M01224300A	KNOB,D16 JOG	
1-31	M01224410A	RING,JOG	
1-32	3M0066900A	FOOT	
1-33	M01267300A	FOOT,D12.7 H3.6 3M 3J5012	
1-34		PCB ASSY,I/O ·····	PCB ASSY,GATHER I/O (Refer to page 14)
1-35	*M01279700A	VINYL SHEET,ISOLATE	
1-36		PCB ASSY,BAL ·····	PCB ASSY,GATHER I/O (Refer to page 14)
1-37	M01305700A	RIVET,NYLON SR3-5.5	
1-41	*B00117900A	SCREW JHB M3X8 FNI	
1-42	*3B0005708B	SCREW,BPB M3X8 (BLK)	
1-43	*3B0001306A	SCREW,J,S M3X6	
1-44	*3B0005308A	SCREW,BPB M3X8	
1-45	*3B0007400A	SCREW,BPAA M3X6	
1-46	*3B0000808A	SCREW,BPP M3X8	
1-47	*3B0001812B	SCREW,J,S M3X12 BLK	
1-48	*3B0004408A	SCREW,BPS M3X8 (BLK)	

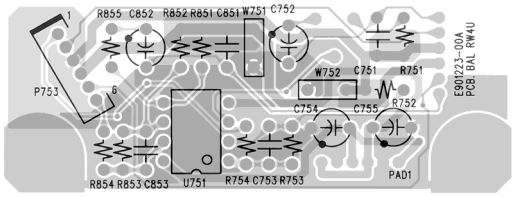
5. PC BOARDS AND PARTS LIST

基板図とパーツリスト

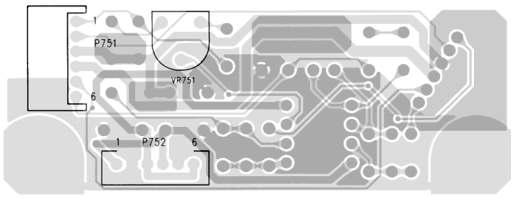
MAIN PCB



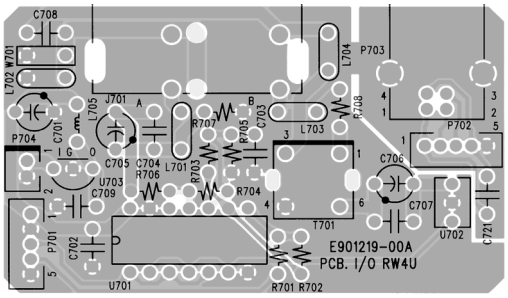
BAL PCB SIDE A



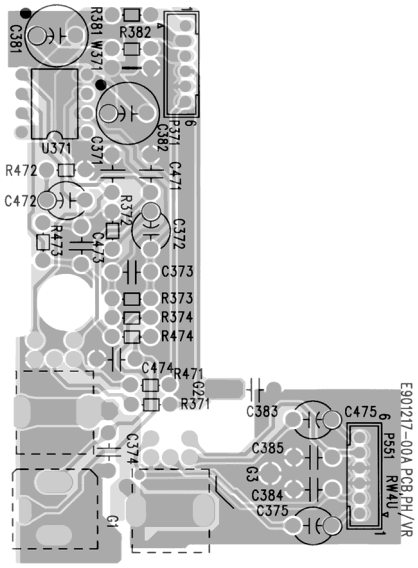
BAL PCB SIDE B



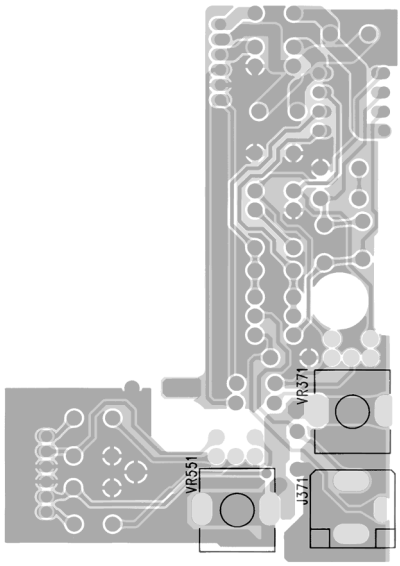
I/O PCB



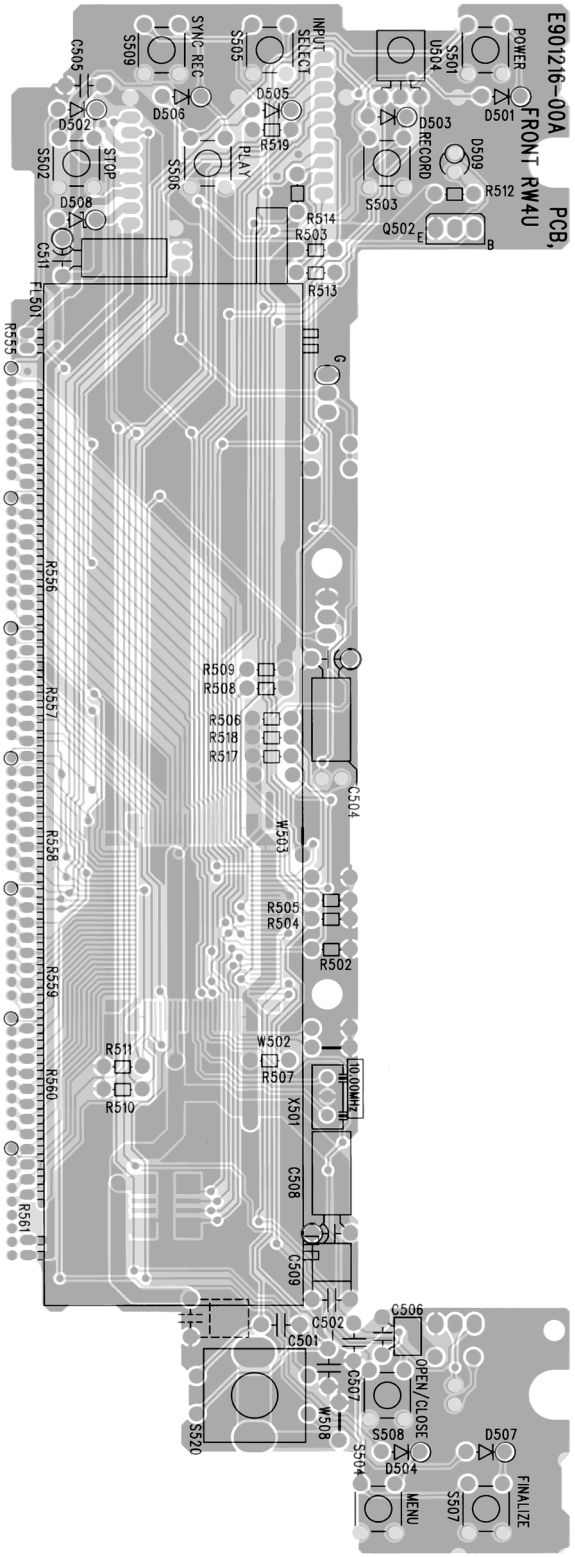
PH/VR PCB SIDE A



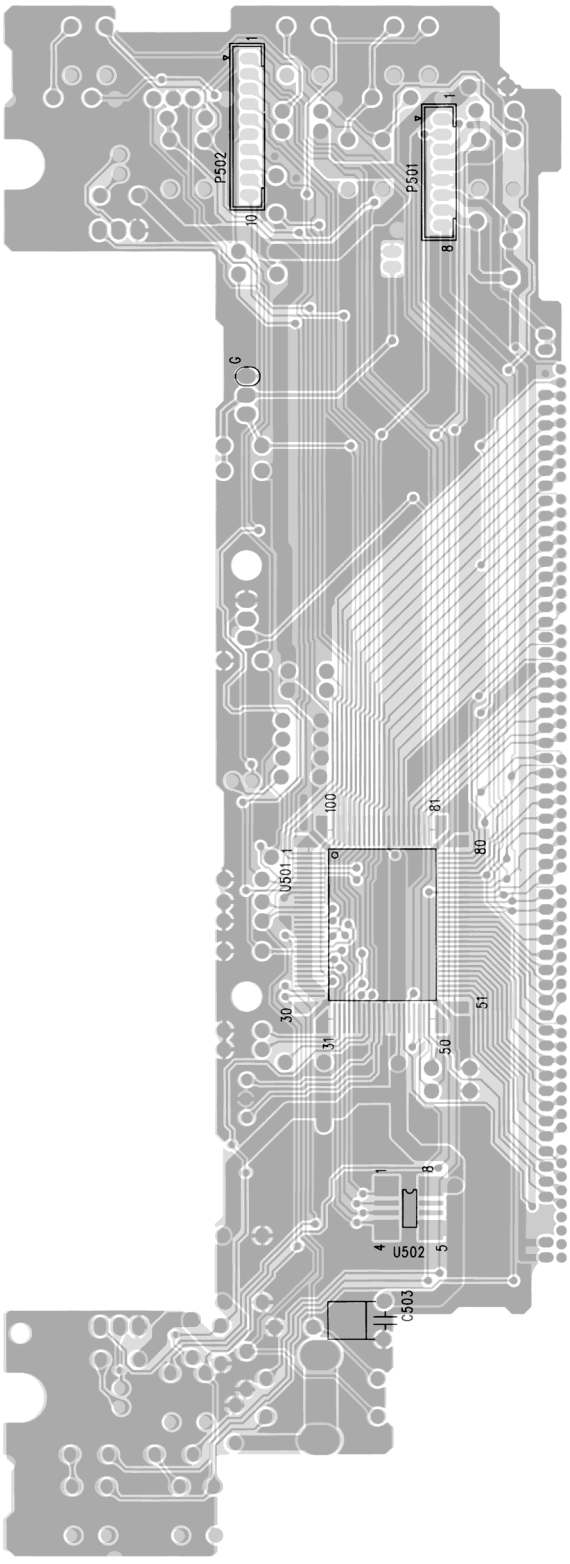
PH/VR PCB SIDE B



FRONT PCB SIDE A



FRONT PCB SIDE B



MAIN PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95116820A	PCB ASSY,MAIN
	*3E002720	FER.CORE,K5AT 18.3X10X10
D301-D304	3S002984	DIODE,1SS355
D305	S0036744	ZENER DIODE,UDZS TE-17 6.2B
J301	3E010590	JACK,RJ-1073B-09-0320A
L101	E0013294	COIL,LQH3N 4.7UH
P101	3E015110	CONNECTOR,40P 3675P40VUA0
P103	3E014240	CONNECT PLUG,S5B-PH-K-S
P303	3E010380	CONNECT PLUG,B 6B-PH-K-S
Q101-104	3S002994	TR,DTC124EUA
Q301,401	S0041624	TR,2SD2114K T146 W
Q302	S0041574	TR,DTA124EUA T106
RA101-108	R0017404	RES ARRAY,1/16W 4X33 J
R324	E0036654	BEAD COIL,ACB1608M-300-T
U101	S0035124	IC,KF33BD-TR
U102	S00347000A	IC,UPD82509GC-XXX-7EA
U103	S00433200A	ROM ASSY,39VF512
U104	3S002924	IC,TC74VHC04F(EL)SMT
U105	S0037164	IC,TC74VHCT541AFT(EL)
U106,107	S0037174	IC,TC74VHCT245AFT(EL)
U108	3S002924	IC,TC74VHC04F(EL)SMT
U109	S00418500A	IC,HD6437042 CONVERT4
U110	S0039753	IC,M11B16161A-45T
U111	S00361900A	IC,AUDIO CONVERTER
U112	3S002954	IC,LC8905V
U113	S0041563	IC,SM5844AF
U114	3S002924	IC,TC74VHC04F(EL)SMT
U115	3S002914	IC,TC74VHC74F(EL)SMT
U116	3S002934	IC,TC74HC02AF(EL)SMT
U117	S0042044	IC,TC9271FS
U301	3S003084	IC,PCM3003E
U302	3S002924	IC,TC74VHC04F(EL)SMT
U303,304	3S003144	IC,NJM4558V SMT
X101	E0059064	RESONATOR,CSTCW4800MX4117
X102	3E011994	RES,CSTCC 7.17MG0H6-TC
X103	3E011974	X'TAL,11.289MHZ

GATHER I/O PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95121800A	PCB ASSY,GATHER I/O
		PCB ASSY,BAL
P751	3E001320	CONNECT PLUG,S 6B-PH-K-S
P752	3E003850	CONNECT PLUG,B6B-PH(RED)
U751	3S000260	IC,NJM4558D
VR751	3R004590	VR,SEMI-FIXED RH0615-10K

GATHER I/O PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
		PCB ASSY,I/O
J701	3E010890	JACK,RCA 2P(ORANGE)
L701-704	3E011820	FB,FBR07HA850SB-00
L705	3E015630	COIL,220UH K
P701	3E003840	CONNECT PLUG,B5B-PH RED
P702	3E010370	CONNECT PLUG,B 5B-PH-K-S
P703	E0064560	CONNECTOR,USB UBB-4R-D14C
T701	3E0132300A	PULS TRANS,S-701-001
U701	3S001660	IC,TC74HCU04AP (DIP)
U702	3E011830	FILTER,EMT 47BT
U703	3S000380	IC,TA78L005AP

GATHER FRONT PCB ASSY

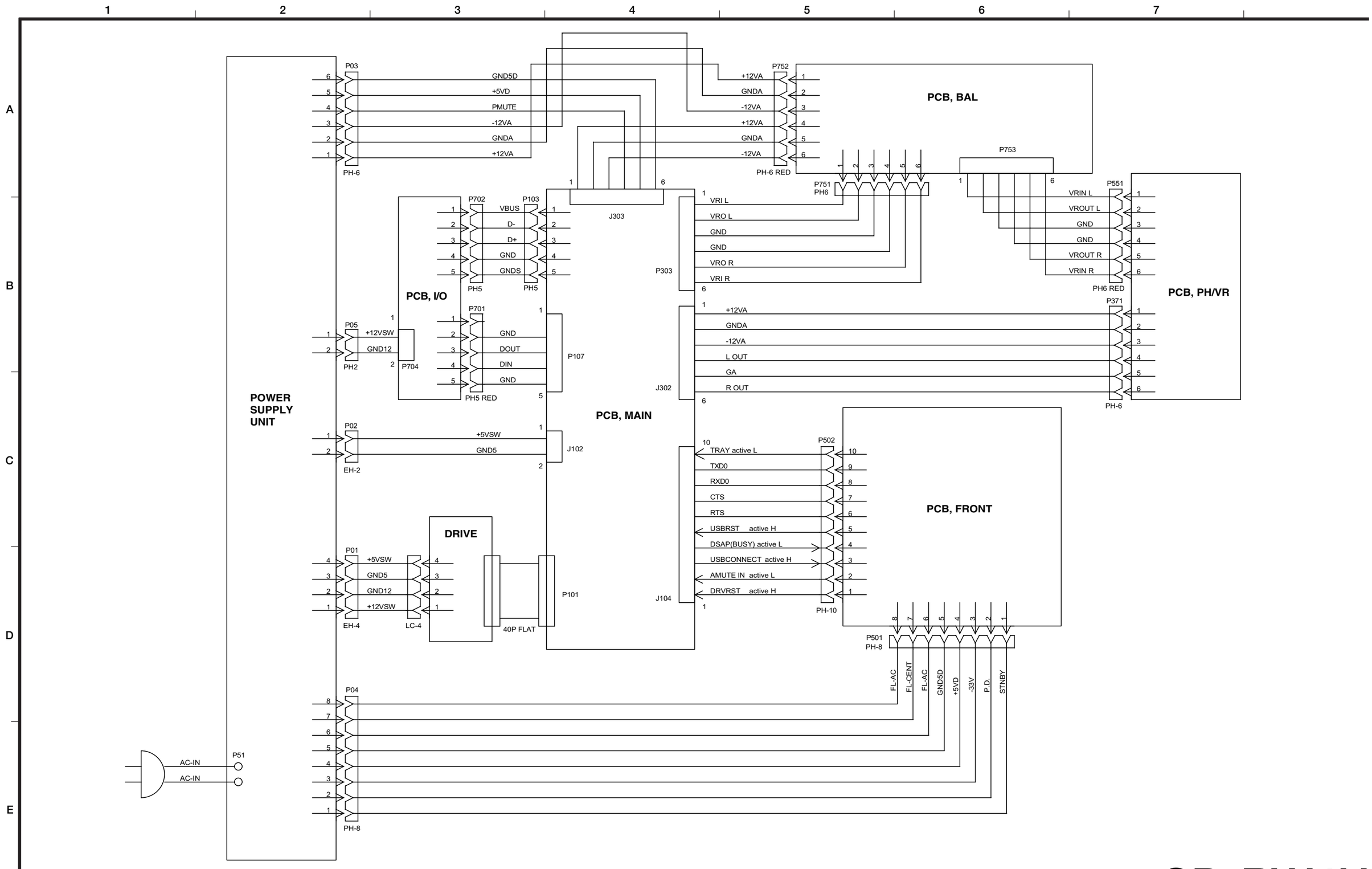
REF.NO.	PARTS NO.	DESCRIPTION
	*E95121500A	PCB ASSY,GATHER FRONT
		PCB ASSY,PH/VR
J371	E0062060	JACK,PHONE 3.5 YKB21-5220
P371	3E010380	CONNECT PLUG,B 6B-PH-K-S
P551	3E003850	CONNECT PLUG,B6B-PH(RED)
U371	3S000850	IC,NJM4560D
VR371	R0097840	VAR RES,50KAX2 RK09K12C
VR551	R0097960	VAR RES,10KAX2 RK09K12C
		PCB ASSY,FRONT
	*M01253500B	SPACER,RC 5X5X3
	*M01268500A	SPACER,FL
D501-507	3S000241	DIODE,1SS133
D508	3S001891	ZDI,MTZJ6.2B
D509	S0042160	LED,RED-3DIA-GL3HD43
FL501	3E0117500A	DISPLAY,HNA-16MM23 RW(L)
P501	3E010400	CONNECT PLUG,B 8B-PH-K-S
P502	3E010420	CONNECT PLUG,B10B-PH-K-S
Q502	3S000291	TR,DTC124ES TP
R555-561	3R007510	RES,ARRAY 100KX8
S501-509	3E002070	SW,TACT SKQSAB HMR-187
S520	E0062050	ENCODER,ROTARY EC12E24244
U501	3S0036600A	IC,CXP82040-130Q
U502	3S003254	IC,BR93LC46RF-WE2 SMT
U504	E0062220	RMCN RCVR,RPM6938-V4
X501	3E011740	RESONATOR,CST 10.00MTW

6. INCLUDED ACCESSORIES
付属品

INCLUDED ACCESSORIES

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	*D00597400A	OWNER'S MANUAL,JAPANESE [J]	
	*D00604500A	OWNER'S MANUAL,SETUP JAPANESE [J]	
	*D00607000A	MANUAL,BS QUICK WIN JAPANESE [J]	
	*D00607100A	MANUAL,BS QUICK MAC JAPANESE [J]	
	*D00597410A	OWNER'S MANUAL,ENGLISH [EXCEPT J]	
	*D00604400A	OWNER'S MANUAL,USB ENGLISH [EXCEPT J]	
	*D00607200A	MANUAL,BS QUICK WIN ENGLISH [EXCEPT J]	
	*D00607300A	MANUAL,BS QUICK MAC ENGLISH [EXCEPT J]	
	*D00607700A	OWNER'S MANUAL,QSG E [E]	
	*D00607710A	OWNER'S MANUAL,QSG F [E]	
	*D00607720A	OWNER'S MANUAL,QSG G [E]	
	*D00607730A	OWNER'S MANUAL,QSG I [E]	
	*D00607740A	OWNER'S MANUAL,QSG S [E]	
	*M01253100B	DISC KIT,USB SETUP JPN [J]	
	*T00068000A	DISC,BS WIN/MAC JPN [J]	
	*M01279400A	DISC KIT,USB SETUP EXP [EXCEPT J]	
	*T00068100A	DISC,BS WIN/MAC ENG [EXCEPT J]	
	*3E0123700B	REMOTE CONTROL UNIT,RC-RW700	
	*3E003660	BATTERY,UM-3(2P X ED)	
	*M01267300A	FOOT,D12.7 H3.6 3M 3J5012	
	*3E015120	CABLE,USB 1.5M	
	*3E0156200A	ADAPTER,HP PLG AV316-0.18	

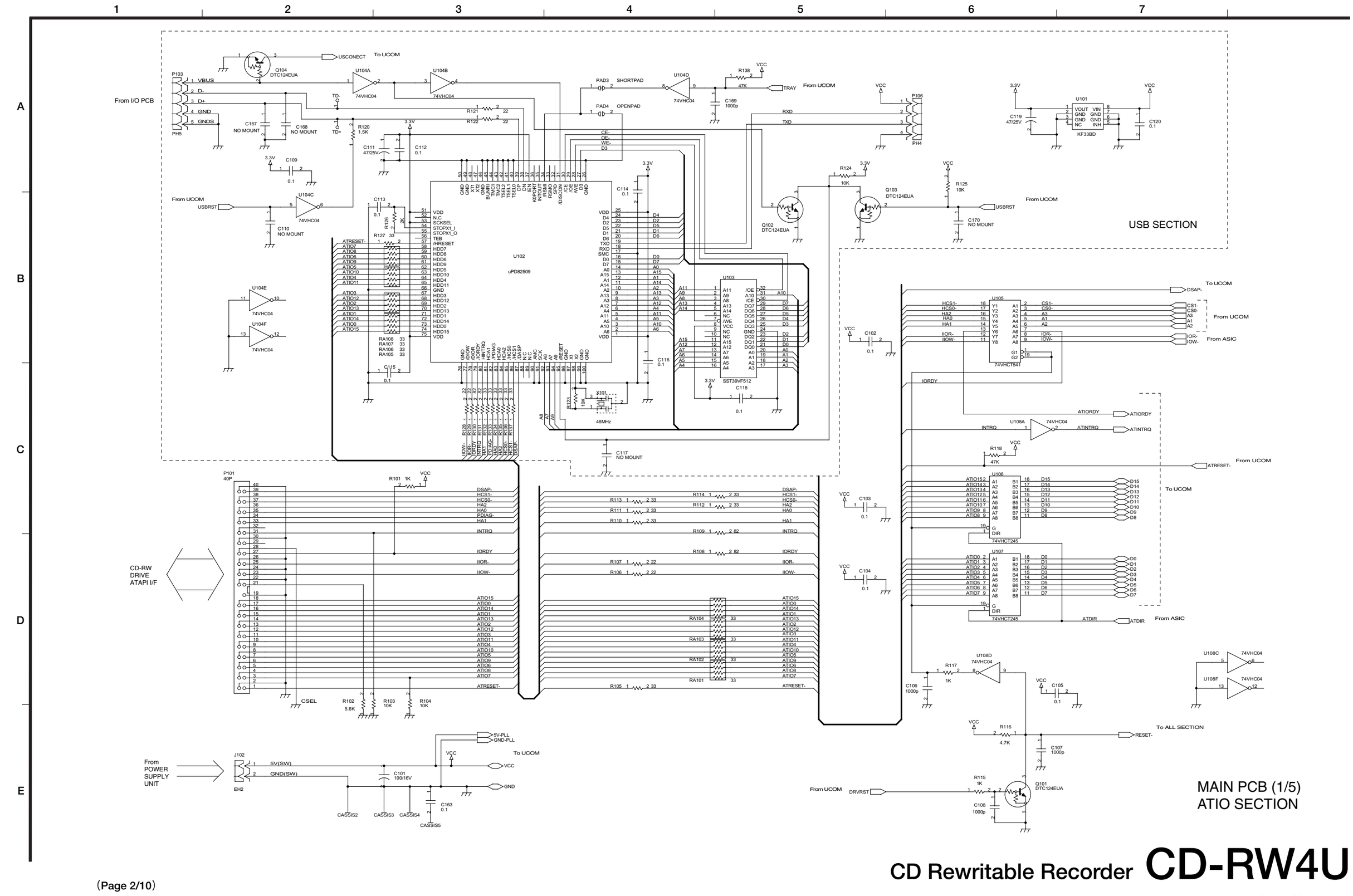
SCHEMATIC DIAGRAM CD-RW4U WIRING



CD Rewritable Recorder **CD-RW4U**

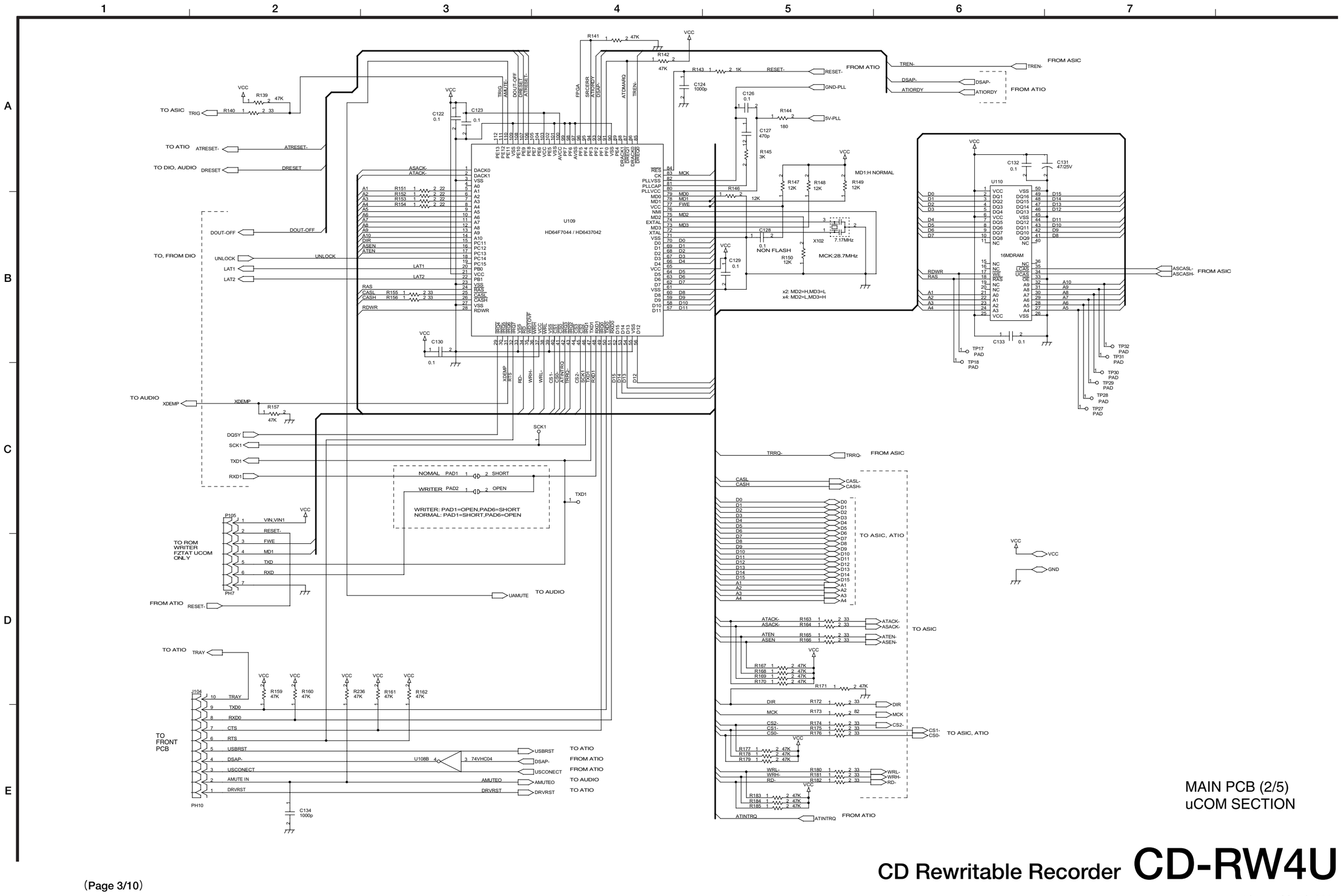
1 st Issue; March 2001

SCHEMATIC DIAGRAM CD-RW4U MAIN PCB (1/5)



CD Rewritable Recorder **CD-RW4U**

1 st Issue; March 2001

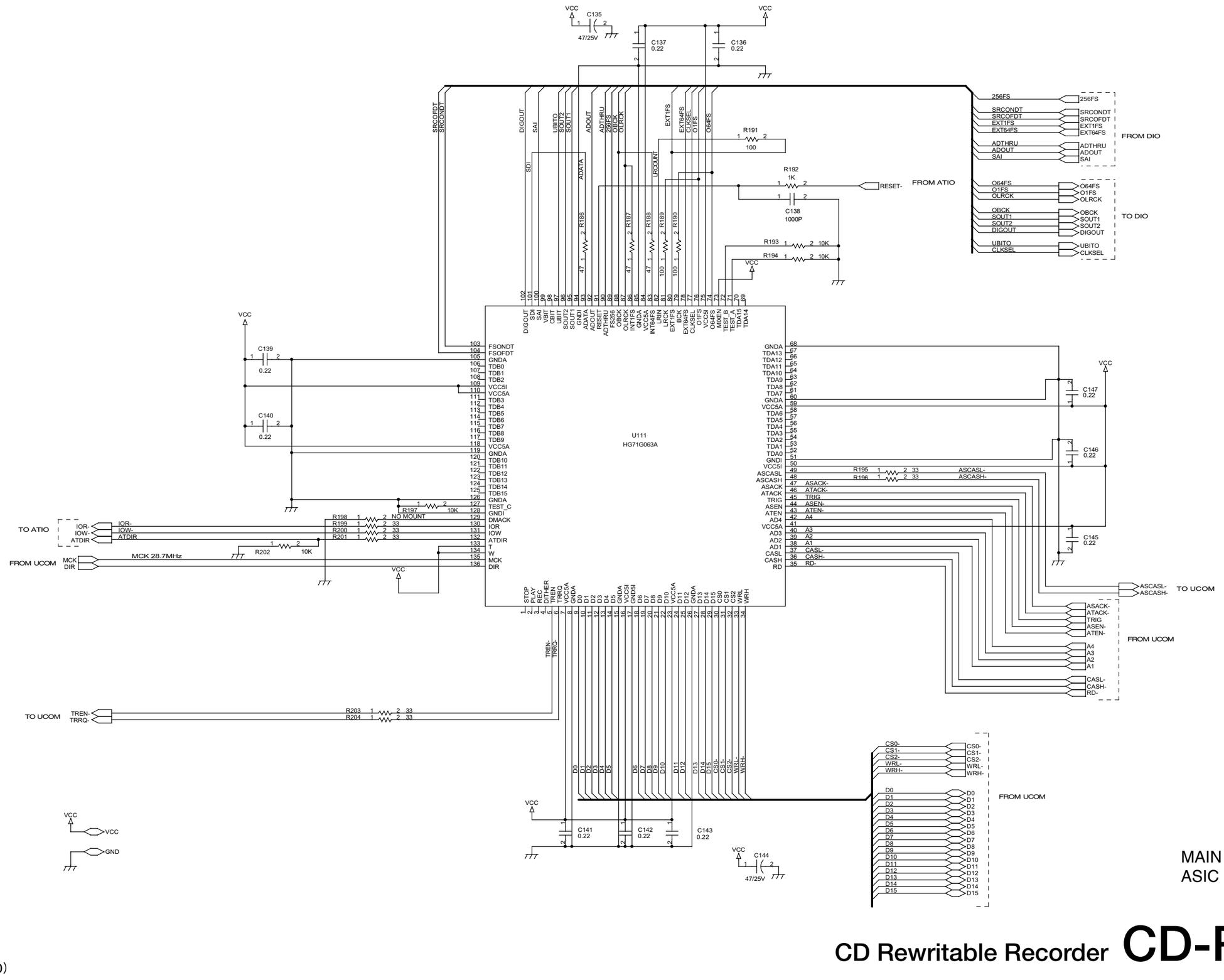


MAIN PCB (2/5)
uCOM SECTION

CD Rewritable Recorder **CD-RW4U**

1 st Issue; March 2001

SCHEMATIC DIAGRAM CD-RW4U MAIN PCB (3/5)



MAIN PCB (3/5)
ASIC SECTION

CD Rewritable Recorder **CD-RW4U**

1 st Issue; March 2001

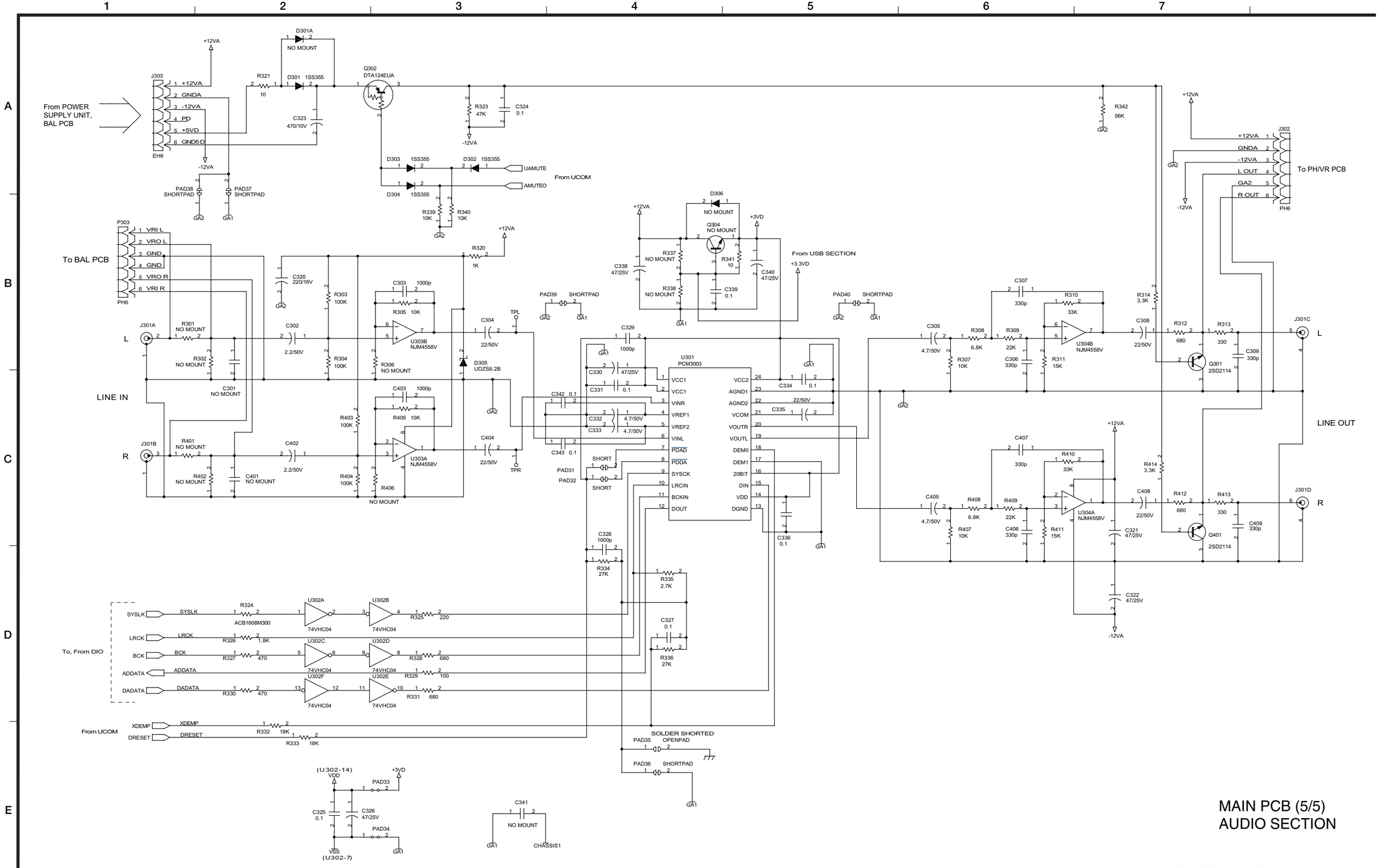
SCHEMATIC DIAGRAM CD-RW4U MAIN PCB (4/5)

MAIN PCB (4/5)
DIO SECTION

CD Rewritable Recorder **CD-RW4U**

1 st Issue; March 2001

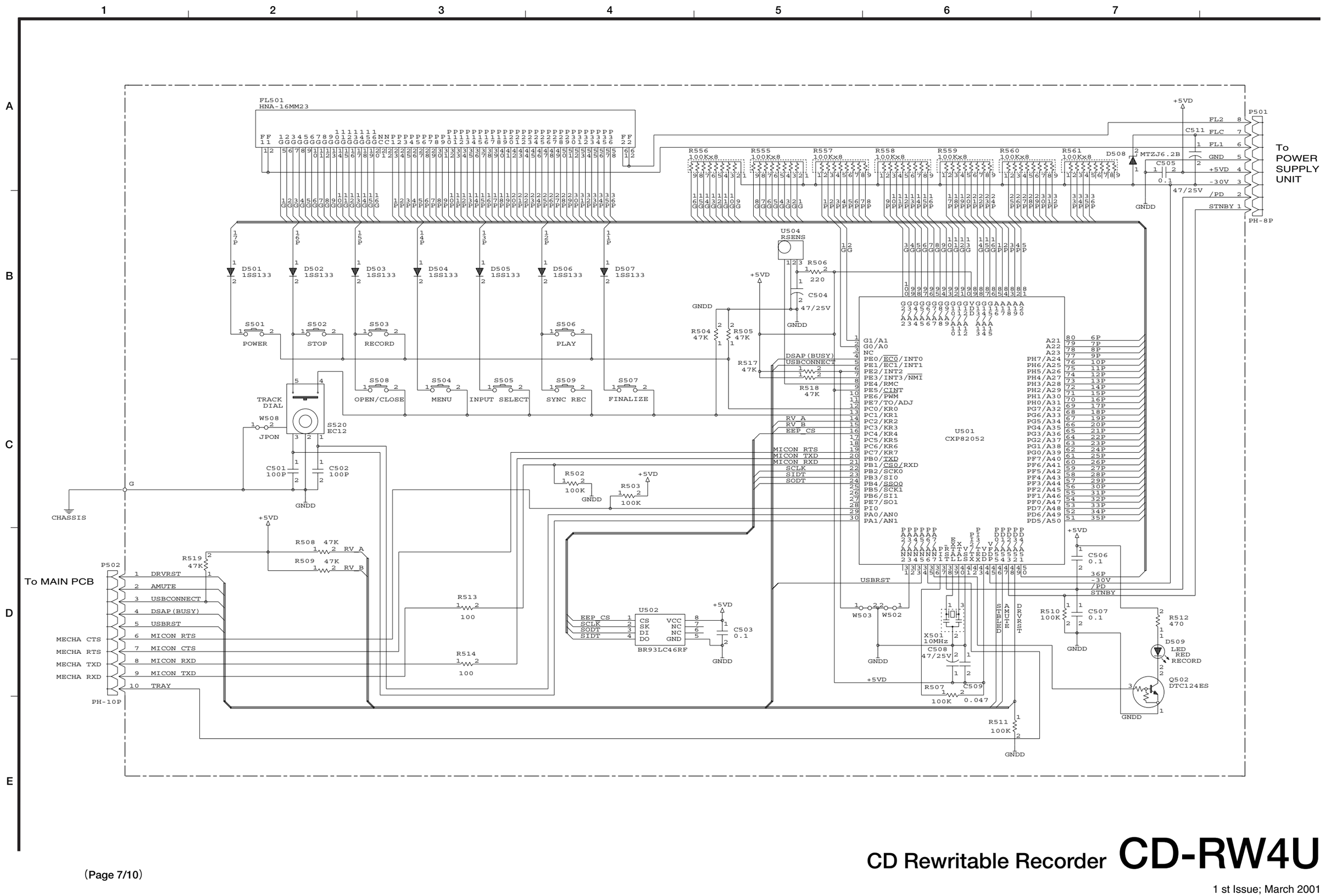
SCHEMATIC DIAGRAM CD-RW4U MAIN PCB (5/5)



MAIN PCB (5/5)
AUDIO SECTION

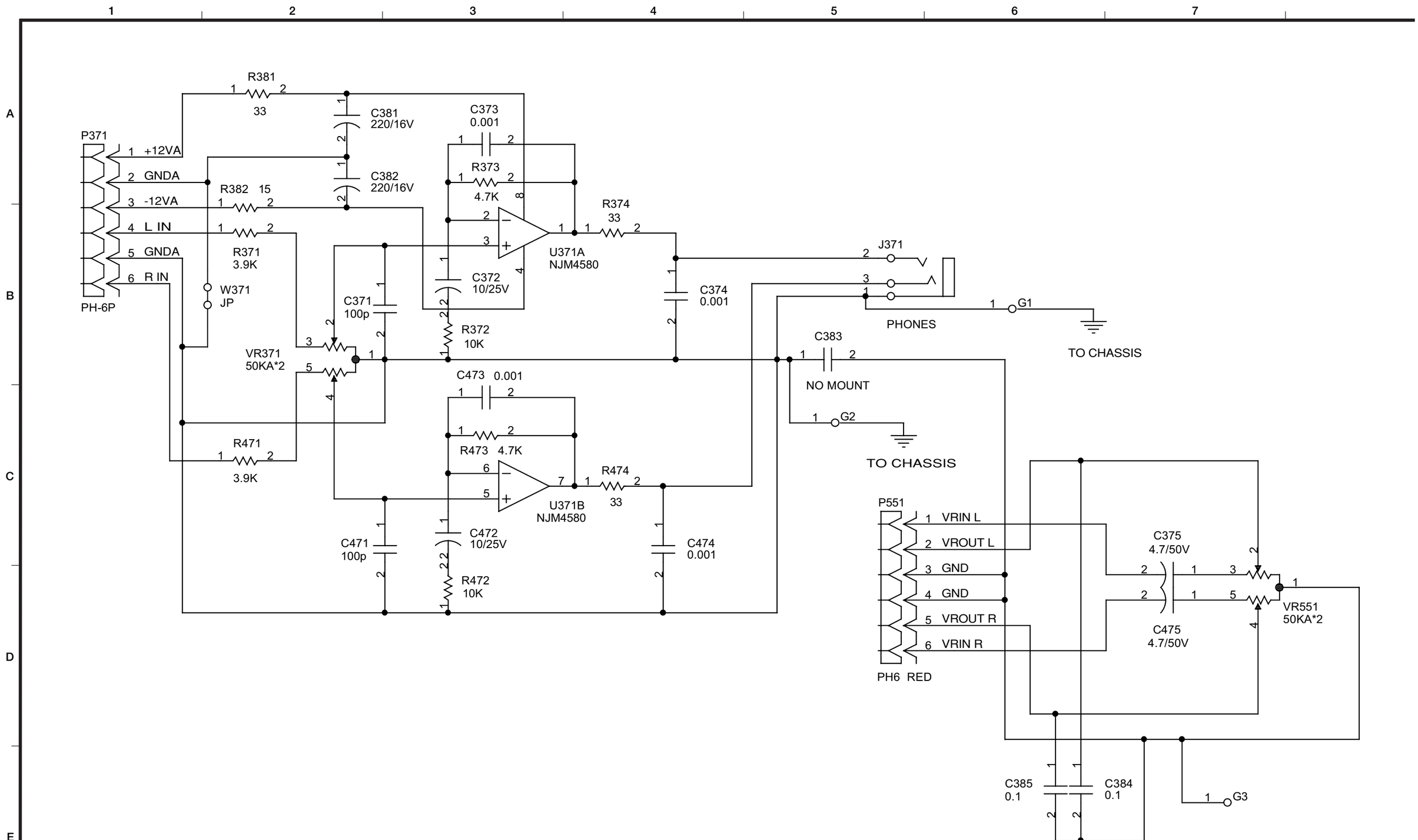
CD Rewritable Recorder **CD-RW4U**

1 st Issue; March 2001



CD Rewritable Recorder **CD-RW4U**

1 st Issue; March 2001

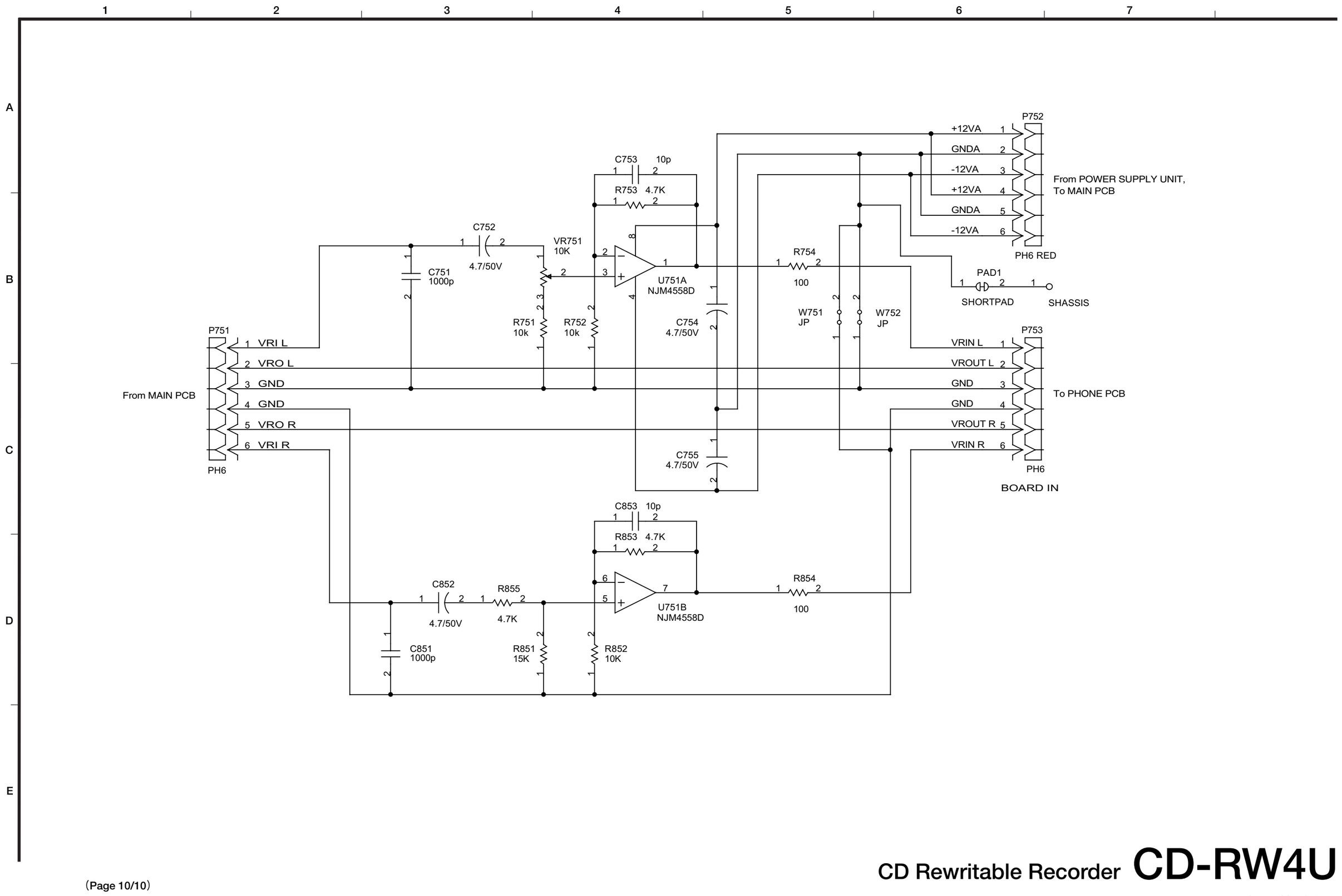


CD Rewritable Recorder **CD-RW4U**

1 st Issue; March 2001

CD Rewritable Recorder **CD-RW4U**

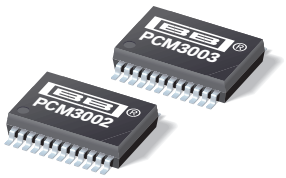
1 st Issue; March 2001



CD Rewritable Recorder **CD-RW4U**

1 st Issue; March 2001

BURR - BROWN®



PCM3002
PCM3003

For most current data sheet and other product information, visit www.burr-brown.com

16-/20-Bit Single-Ended Analog Input/Output SoundPLUS™ STEREO AUDIO CODECs

FEATURES

- MONOLITHIC 20-BIT ΔΣ ADC AND DAC
- 16-/20-BIT INPUT/OUTPUT DATA
- SOFTWARE CONTROL: PCM3002
- HARDWARE CONTROL: PCM3003
- STEREO ADC:
  - Single-Ended Voltage Input
  - 64X Oversampling
  - High Performance
    - THD+N: –86dB
    - SNR: 90dB
    - Dynamic Range: 90dB
- STEREO DAC:
  - Single-Ended Voltage Output
  - Analog Low Pass Filter
  - 64X Oversampling
  - High Performance
    - THD+N: –86dB
    - SNR: 94dB
    - Dynamic Range: 94dB
- SPECIAL FEATURES
  - Digital De-emphasis
  - Digital Attenuation (256 Steps)
  - Soft Mute
  - Digital Loop Back
  - Power Down: ADC/DAC Independent
- SAMPLING RATE: Up to 48kHz
- SYSTEM CLOCK: $256f_S$, $384f_S$, $512f_S$
- SINGLE +3V POWER SUPPLY
- SMALL PACKAGE: SSOP-24

DESCRIPTION

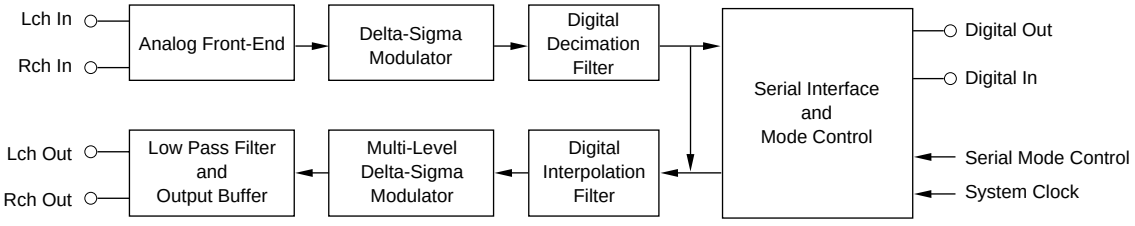
The PCM3002 and PCM3003 are low cost single chip stereo audio CODECs (analog-to-digital and digital-to-analog converters) with single-ended analog voltage input and output.

The ADCs and DACs employ delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter, and the DACs include an 8X oversampling digital interpolation filter. The DACs also include digital attenuation, de-emphasis, infinite zero detection and soft mute to form a complete subsystem. PCM3002 and PCM3003 operate with left-justified, and right-justified formats, while the PCM3002 also supports the I^2S data format.

PCM3002 and PCM3003 provide a power-down mode that operates on the ADCs and DACs independently.

Fabricated on a highly advanced CMOS process, PCM3002 and PCM3003 are suitable for a wide variety of cost-sensitive consumer applications where good performance is required.

PCM3002's programmable functions are controlled by software and the PCM3003's functions include de-emphasis, power down, and audio data format selections, which are controlled by hardware.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1414C
Printed in U.S.A. January, 2000
SBAS079

SPECIFICATIONS

All specifications at +25°C, V_{DD} = V_{CC} = 3.0V, f_S = 44.1kHz, SYSCLK = 384f_S, and 16-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM3002E/3003E MIN	PCM3002E/3003E TYP	PCM3002E/3003E MAX	UNITS
DIGITAL INPUT/OUTPUT					
Input Logic					
Input Logic Level: V_{IH}(1, 2, 3)		0.7 x V_{DD}			VDC
V_{IL}(1, 2, 3)				0.3 x V_{DD}	VDC
Input Logic Current: I_{IN}(2)				±1	µA
Input Logic Current: I_{IN}(1)				100	µA
Output Logic					
Output Logic Level: V_{OH}(5)	I_{OUT} = –1mA	V_{DD} –0.3			VDC
V_{OL}(5)	I_{OUT} = +1mA			0.3	VDC
Output Logic Level: V_{OL}(4)	I_{OUT} = +1mA			0.3	VDC
CLOCK FREQUENCY					
Sampling Frequency (f_S)		32(7)	44.1	48	kHz
System Clock Frequency	256f_S	8.1920	11.2896	12.2880	MHz
	384f_S	12.2880	16.9344	18.4320	MHz
	512f_S	16.3840	22.5792	24.5760	MHz
ADC CHARACTERISTICS					
RESOLUTION			20		Bits
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±3.0	% of FSR
Gain Error			±2.0	±5.0	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error	High-Pass Filter Disabled(6)		±1.7		% of FSR
Bipolar Zero Drift	High-Pass Filter Disabled(6)		±20		ppm of FSR/°C
DYNAMIC PERFORMANCE(8)					
THD+N: V_{IN} = –0.5dB			–86	–80	dB
V_{IN} = –60dB			–28		dB
Dynamic Range	A-Weighted	86	90		dB
Signal-to-Noise Ratio	A-Weighted	86	90		dB
Channel Separation		84	88		dB
DIGITAL FILTER PERFORMANCE					
Passband				0.454f_S	Hz
Stopband		0.583f_S			Hz
Passband Ripple				±0.05	dB
Stopband Attenuation		–65			dB
Delay Time			17.4/f_S		sec
HPF Frequency Response	–3dB		0.019f_S		mHz
ANALOG INPUT					
Voltage Range			0.60 V_{CC}		Vp-p
Center Voltage			0.50 V_{CC}		V
Input Impedance			30		kΩ
Anti-Aliasing Filter Frequency Response	–3dB		150		kHz

NOTES: (1) Pins 7, 8, 17 and 18: $\overline{RST}$, ML, MD, MC for the PCM3002; $\overline{PDAD}$, $\overline{PDDA}$, DEM1, DEM0 for PCM3003 (Schmitt-Trigger input with 100kΩ typical internal pull-down resistor). (2) Pins 9, 10, 11, 15: SYSCLK, LRCIN, BCKIN, DIN (Schmitt Trigger input). (3) Pin16: 20BIT for PCM3003 (Schmitt-Trigger input, 100kΩ typical internal pull-down resistor). (4) Pin 12: DOUT. (5) Pin 16: $\overline{ZFLG}$ (open drain output). (6) High Pass Filter for Offset Cancel. (7) Refer to Application Bulletin AB-148 for information relating to operation at lower sampling frequencies. (8) f_{IN} = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (9) f_{OUT} = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (10) Applies for voltages between 2.4V to 2.7V for 0°C to +70°C and 256f_S/512f_S operation (384f_S not available). (11) SYSCLK, BCKIN, and LRCIN are stopped.

SPECIFICATIONS

All specifications at +25°C, V_{DD} = V_{CC} = 3.0V, f_S = 44.1kHz, SYSCLK = 384f_S, CLKIO Input, 18-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM3002E/3003E MIN	PCM3002E/3003E TYP	PCM3002E/3003E MAX	UNITS
DAC CHARACTERISTICS					
RESOLUTION			20		Bits
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±3	% of FSR
Gain Error			±1.0	±5	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error			±1.0		% of FSR
Bipolar Zero Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE[9]					
THD+N: V_{OUT} = 0dB (Full Scale)			–86	–80	dB
V_{OUT} = –60dB			–28		dB
Dynamic Range	EIAJ, A-Weighted	88	94		dB
Signal-to-Noise Ratio	EIAJ, A-Weighted	88	94		dB
Channel Separation		86	91		dB
DIGITAL FILTER PERFORMANCE					
Passband				0.445f_S	Hz
Stopband		0.555f_S			Hz
Passband Ripple				±0.17	dB
Stopband Attenuation		–35			dB
Delay Time			11.1/f_S		sec
ANALOG OUTPUT					
Voltage Range			0.60 x V_{CC}		Vp-p
Center Voltage			0.5 x V_{CC}		VDC
Load Impedance	AC-Coupling	10			kΩ
LPF Frequency Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range: V_{CC}, V_{DD}	–25°C to +85°C	2.7	3.0	3.6	VDC
	0° C to +70°C[10]	2.4	3.0	3.6	VDC
Supply Current: Operation	V_{CC} = V_{DD} = 3.0V		18	24	mA
Power-Down	V_{CC} = V_{DD} = 3.0V		50		µA
Power Dissipation: Operation	V_{CC} = V_{DD} = 3.0V		54	72	mW
Power-Down[11]	V_{CC} = V_{DD} = 3.0V		150		µW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C
Thermal Resistance, Θ_{JA}			100		°C/W

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
PCM3002E	SSOP-24	338	–25°C to +85°C	PCM3002E	PCM3002E	Rails
"	"	"	"	"	PCM3002E/2K	Tape and Reel
PCM3003E	SSOP-24	338	–25°C to +85°C	PCM3003E	PCM3003E	Rails
"	"	"	"	"	PCM3003E/2K	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM3002E/2K" will get a single 2000-piece Tape and Reel.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
$+V_{DD}$, $+V_{CC}1$, $+V_{CC}2$ ..... +6.5V
Supply Voltage Differences ..... ±0.1V
GND Voltage Differences ..... ±0.1V
Digital Input Voltage ..... –0.3 to V_{DD} + 0.3V
Analog Input Voltage ..... –0.3 to $V_{CC}1$, $V_{CC}2$ + 0.3V
Power Dissipation 300mW
Input Current ..... ±10mA
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature ..... –55°C to +125°C
Lead Temperature (soldering, 5s) ..... +260°C
(reflow, 10s) ..... +235°C

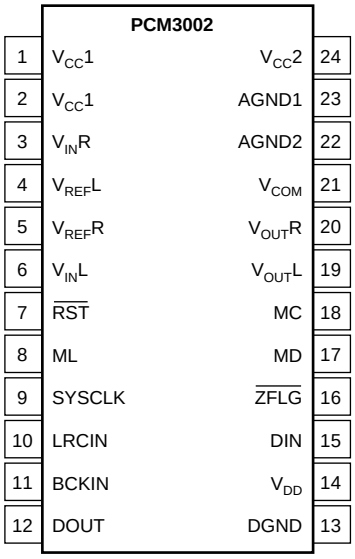
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

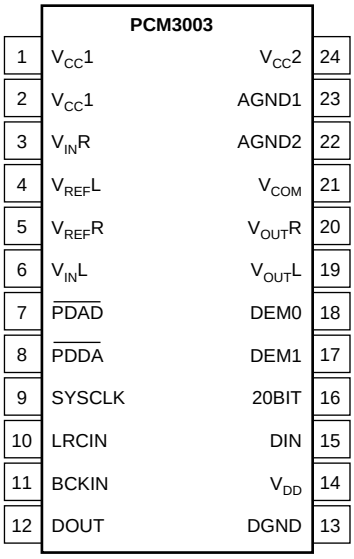
PIN CONFIGURATION—PCM3002

Top View **SSOP**



PIN CONFIGURATION—PCM3003

Top View **SSOP**



PIN ASSIGNMENTS—PCM3002

PIN	NAME	I/O	DESCRIPTION
1	$V_{CC}1$	—	ADC Analog Power Supply
2	$V_{CC}1$	—	ADC Analog Power Supply
3	$V_{IN}R$	IN	ADC Analog Input, Rch
4	$V_{REF}L$	—	ADC Reference, Lch
5	$V_{REF}R$	—	ADC Reference, Rch
6	$V_{IN}L$	IN	ADC Analog Input, Lch
7	$\overline{RST}$	IN	Reset, Active LOW(1, 2)
8	ML	IN	Strobe Pulse for Mode Control(1, 2)
9	SYSCLK	IN	System Clock Input(2)
10	LRCIN	IN	Sample Rate Clock Input (f_S)(2)
11	BCKIN	IN	Bit Clock Input(2)
12	DOUT	OUT	Data Output
13	DGND	—	Digital Ground
14	V_{DD}	—	Digital Power Supply
15	DIN	IN	Data Input(2)
16	$\overline{ZFLG}$	OUT	Zero Flag Output, Active LOW(3)
17	MD	IN	Serial Data for Mode Control(1, 2)
18	MC	IN	Bit Clock for Mode Control(1, 2)
19	$V_{OUT}L$	OUT	DAC Analog Output, Lch
20	$V_{OUT}R$	OUT	DAC Analog Output, Rch
21	V_{COM}	—	ADC/DAC Common
22	AGND2	—	DAC Analog Ground
23	AGND1	—	ADC Analog Ground
24	$V_{CC}2$	—	DAC Analog Power Supply

NOTES: (1) With 100kΩ typical internal pull-down resistor. (2) Schmitt-Trigger input. (3) Open drain output.

PIN ASSIGNMENTS—PCM3003

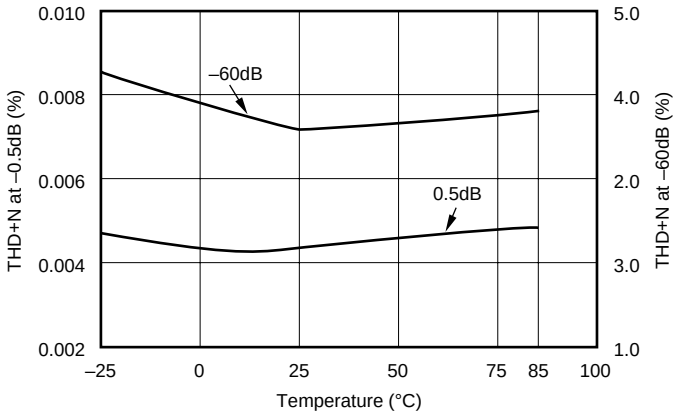
PIN	NAME	I/O	DESCRIPTION
1	$V_{CC}1$	—	ADC Analog Power Supply
2	$V_{CC}1$	—	ADC Analog Power Supply
3	$V_{IN}R$	IN	ADC Analog Input, Rch
4	$V_{REF}L$	—	ADC Reference, Lch
5	$V_{REF}R$	—	ADC Reference, Rch
6	$V_{IN}L$	IN	ADC Analog Input, Lch
7	$\overline{PDAD}$	IN	ADC Power Down, Active LOW(1, 2)
8	$\overline{PDDA}$	IN	DAC Power Down, Active LOW(1, 2)
9	SYSCLK	IN	System Clock Input(2)
10	LRCIN	IN	Sample Rate Clock Input (f_S)(2)
11	BCKIN	IN	Bit Clock Input(2)
12	DOUT	OUT	Data Output
13	DGND	—	Digital Ground
14	V_{DD}	—	Digital Power Supply
15	DIN	IN	Data Input
16	20BIT	IN	20-Bit Format Select(1, 2)
17	DEM1	IN	De-emphasis Control(1, 2)
18	DEM0	IN	De-emphasis Control 0(1, 2)
19	$V_{OUT}L$	OUT	DAC Analog Output, Lch
20	$V_{OUT}R$	OUT	DAC Analog Output, Rch
21	V_{COM}	—	ADC/DAC Common
22	AGND2	—	DAC Analog Ground
23	AGND1	—	ADC Analog Ground
24	$V_{CC}2$	—	DAC Analog Power Supply

NOTE: (1) With 100kΩ typical internal pull-down resistor. (2) Schmitt-Trigger input.

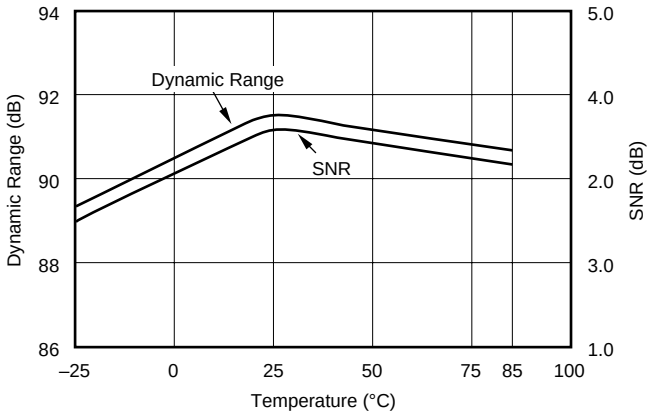
TYPICAL PERFORMANCE CURVES
ADC SECTION

At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, and F_{SIGNAL} = 1kHz, unless otherwise noted.

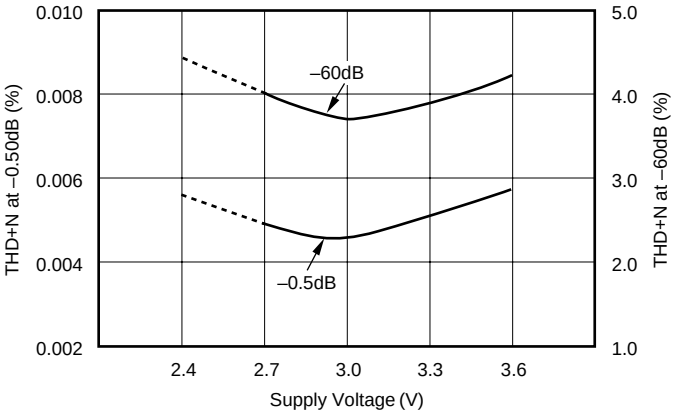
THD+N vs TEMPERATURE



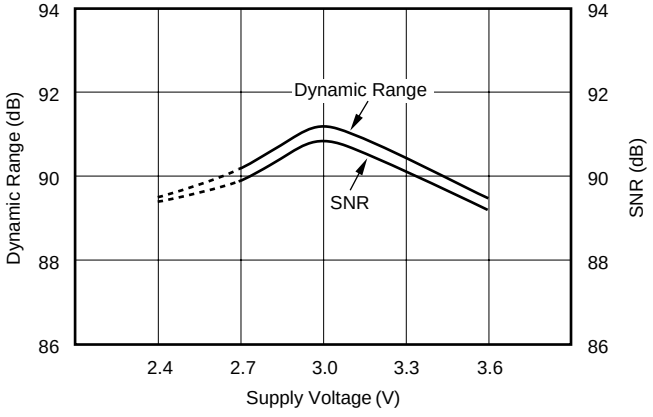
DYNAMIC RANGE and SNR vs TEMPERATURE



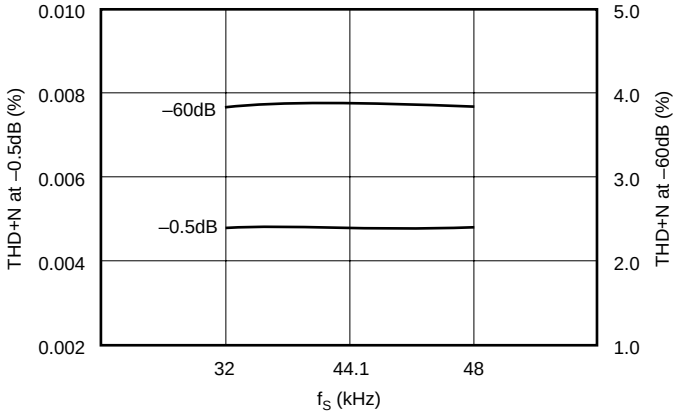
THD+N vs SUPPLY VOLTAGE



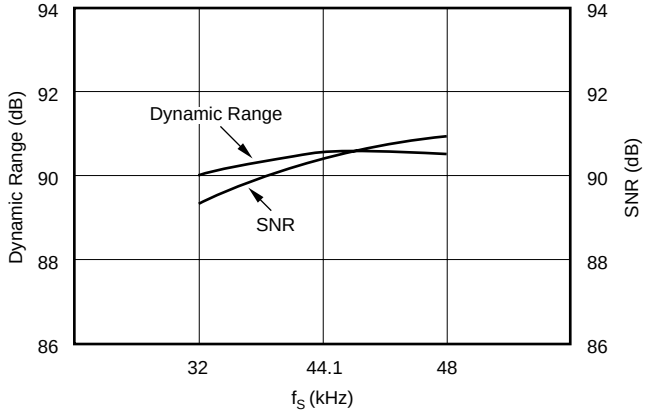
DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE



THD+N vs SAMPLING FREQUENCY



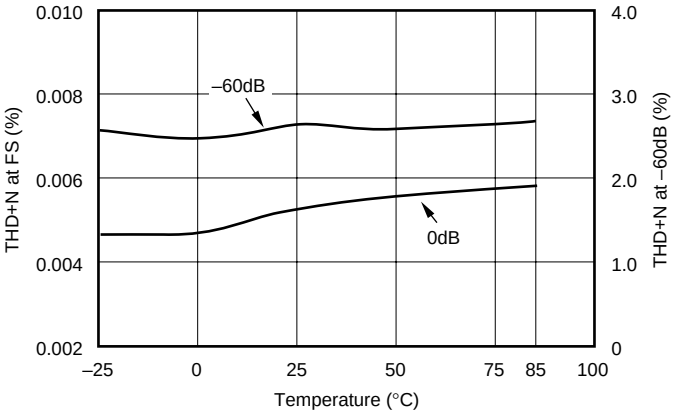
DYNAMIC RANGE and SNR vs SAMPLING FREQUENCY



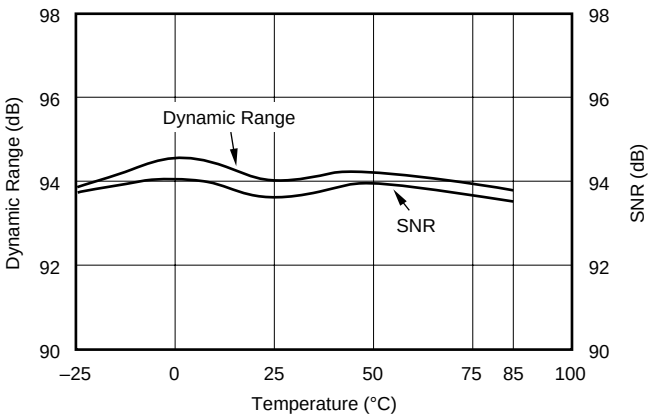
TYPICAL PERFORMANCE CURVES
DAC SECTION

At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, and F_{SIGNAL} = 1kHz, unless otherwise noted.

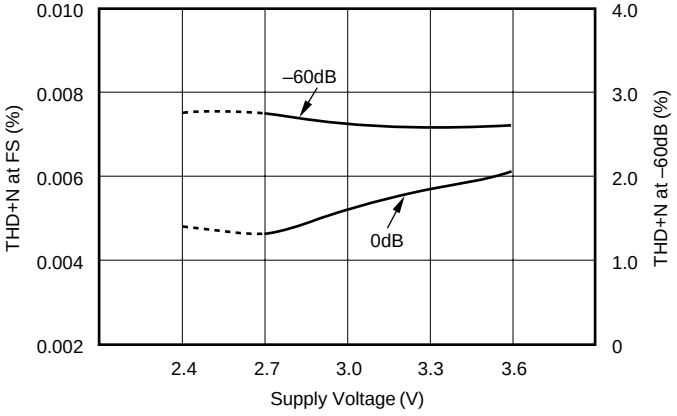
THD+N vs TEMPERATURE



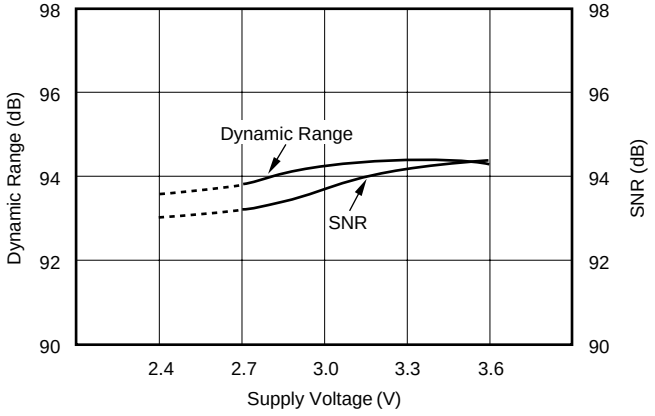
DYNAMIC RANGE and SNR vs TEMPERATURE



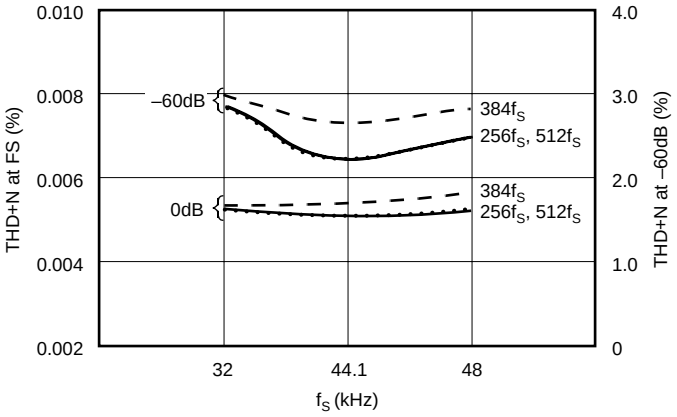
THD+N vs SUPPLY VOLTAGE



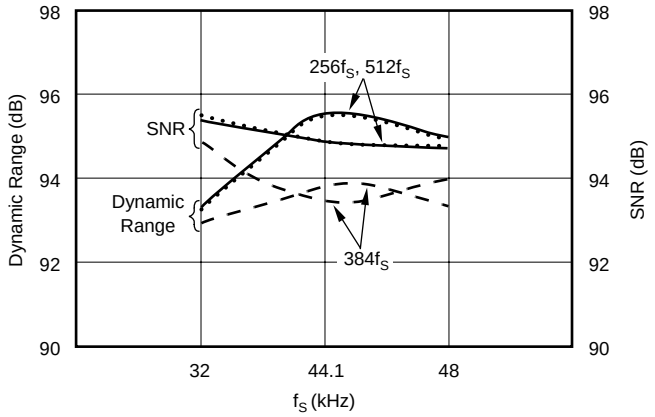
DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE



THD+N vs SAMPLING FREQUENCY
and SYSTEM CLOCK



DYNAMIC RANGE and SNR
vs SAMPLING FREQUENCY and SYSTEM CLOCK

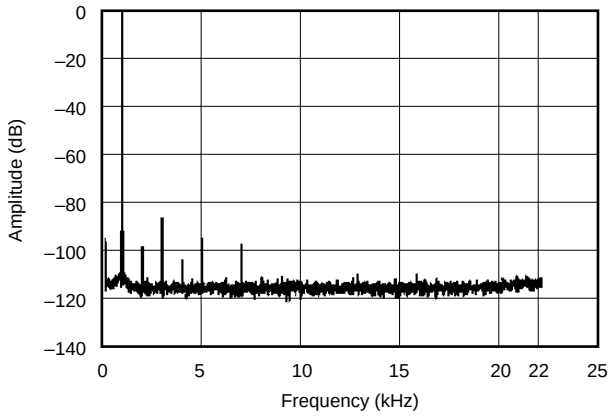


TYPICAL PERFORMANCE CURVES
Output Spectrum

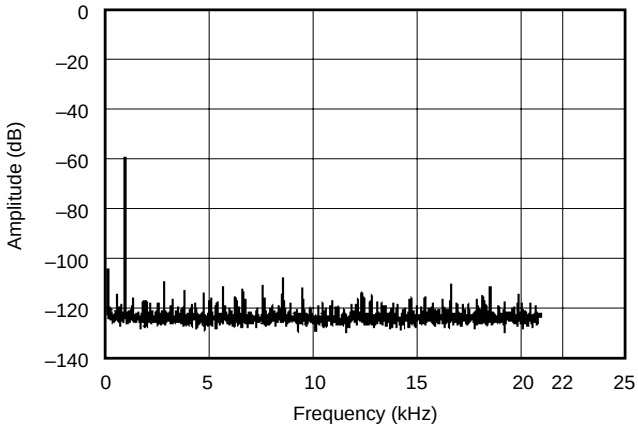
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, and F_{SIGNAL} = 1kHz, unless otherwise noted.

DACs

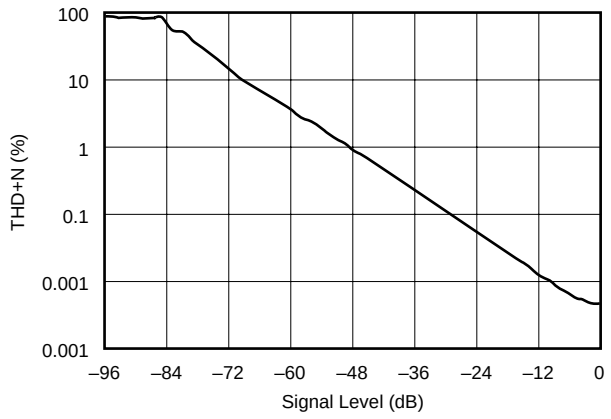
OUTPUT SPECTRUM (0dB, N = 8192)



OUTPUT SPECTRUM (–60dB, N = 8192)

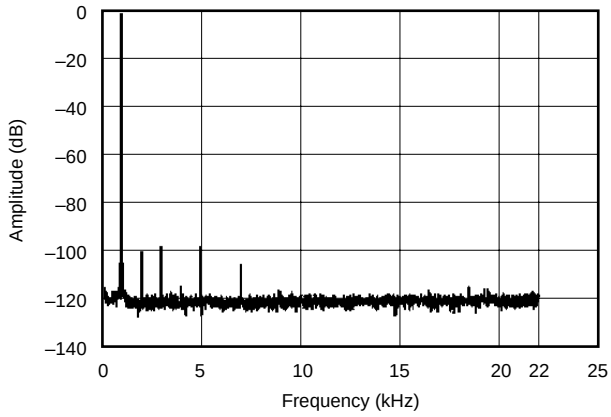


THD+N vs SIGNAL LEVEL

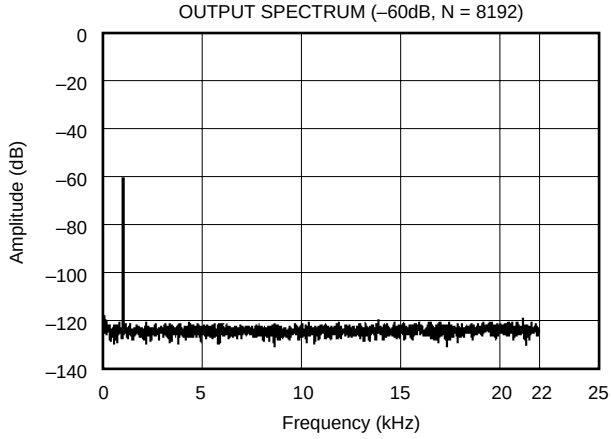


ADCs

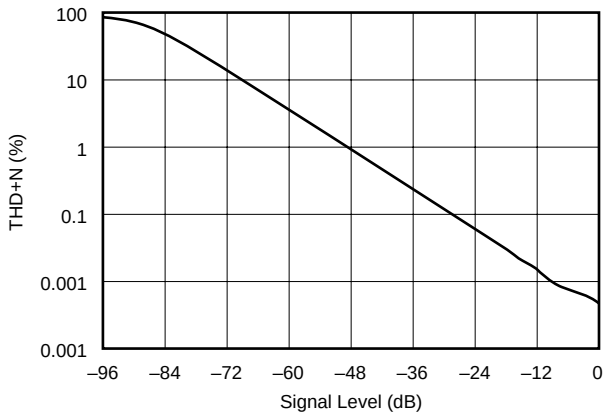
OUTPUT SPECTRUM (0dB, N = 8192)



OUTPUT SPECTRUM (–60dB, N = 8192)



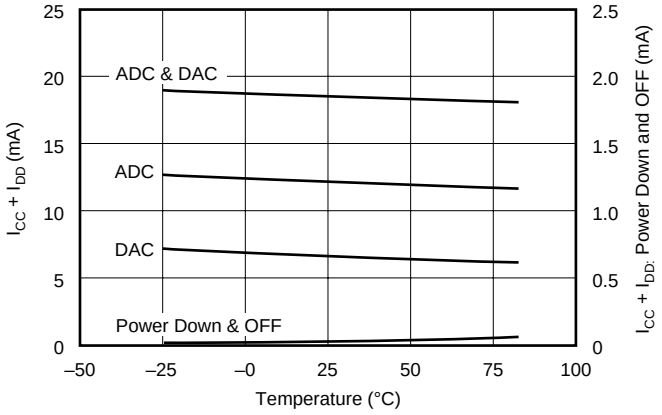
THD+N vs SIGNAL LEVEL



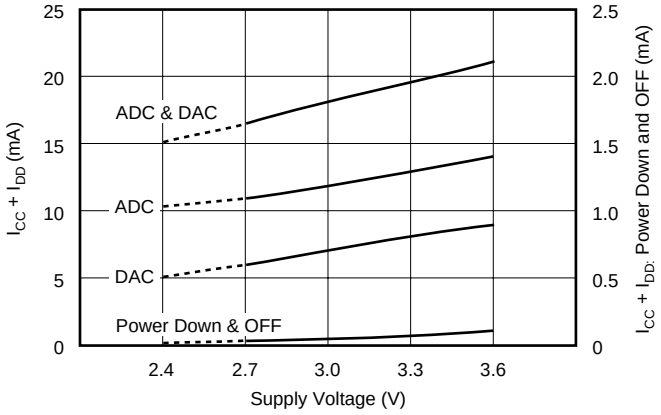
TYPICAL PERFORMANCE CURVES
Supply Current

At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, DIN = BPZ, and V_{IN} = BPZ, unless otherwise noted.

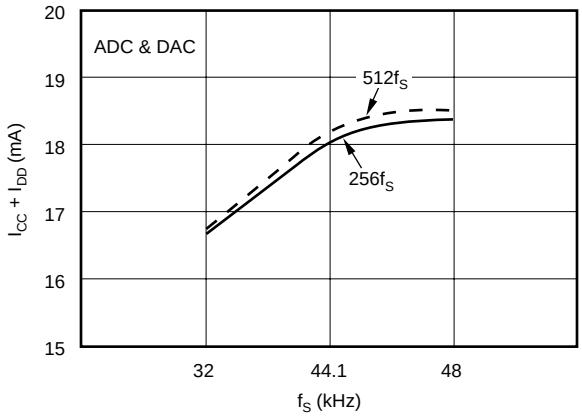
I_{CC} + I_{DD} vs TEMPERATURE



I_{CC} + I_{DD} vs SUPPLY VOLTAGE



I_{CC} + I_{DD} vs SAMPLING FREQUENCY

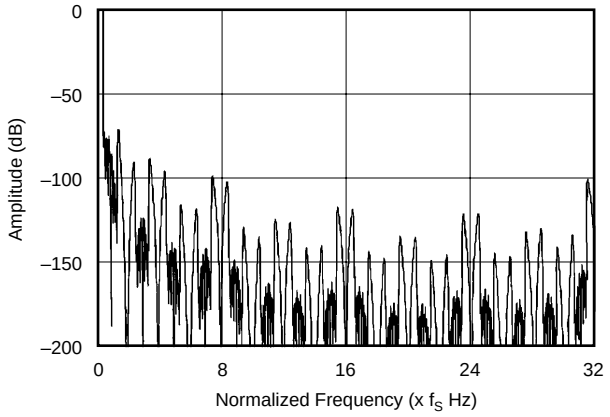


TYPICAL PERFORMANCE CURVES

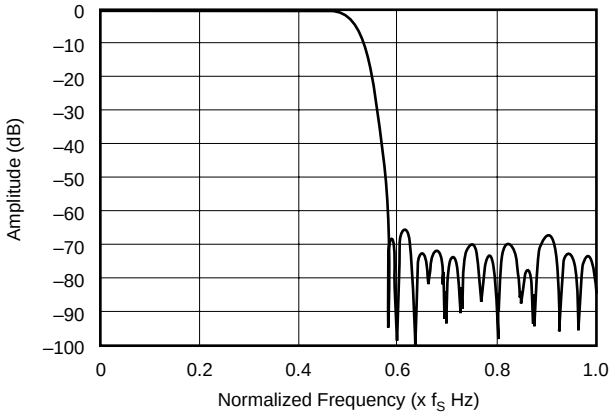
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, and f_{SYSCLK} = 384f_S, unless otherwise noted.

ADC DIGITAL FILTER

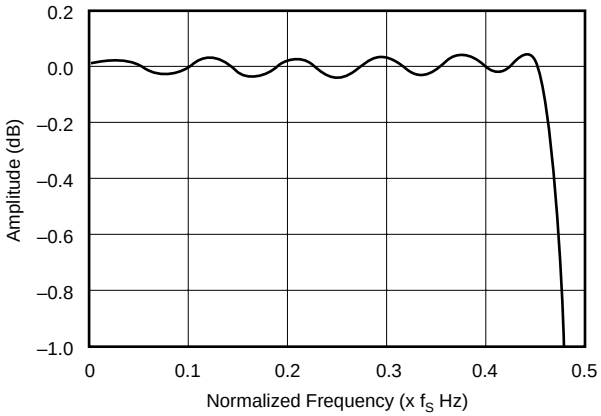
OVERALL CHARACTERISTICS



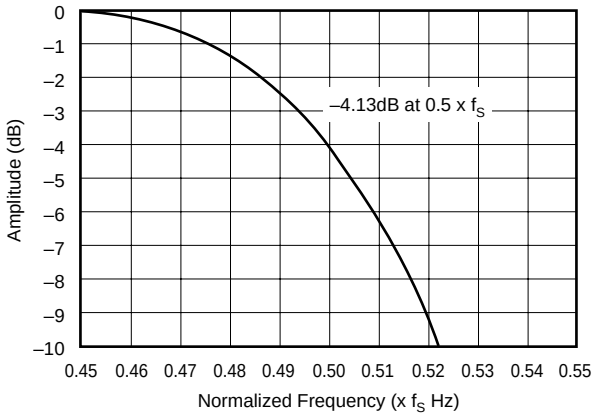
STOPBAND ATTENUATION CHARACTERISTICS



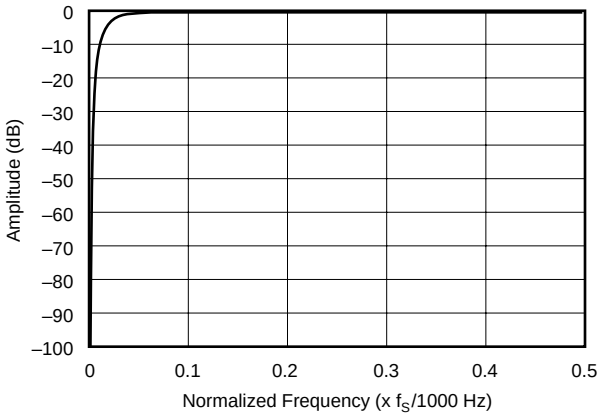
PASSBAND RIPPLE CHARACTERISTICS



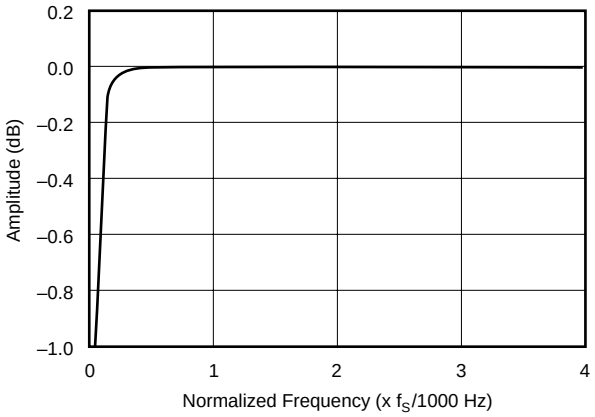
TRANSITION BAND CHARACTERISTICS



HIGH PASS FILTER RESPONSE



HIGH PASS FILTER RESPONSE

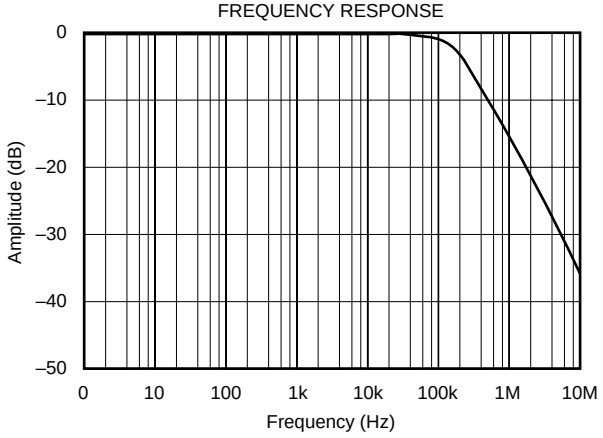


TYPICAL PERFORMANCE CURVES

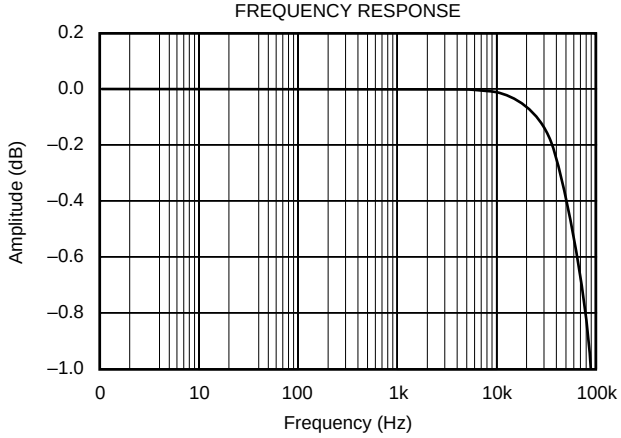
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, and f_{SYSCLK} = 384f_S, unless otherwise noted.

ANTI-ALIASING FILTER

ANTI-ALIASING FILTER OVERALL FREQUENCY RESPONSE



ANTI-ALIASING FILTER PASSBAND FREQUENCY RESPONSE

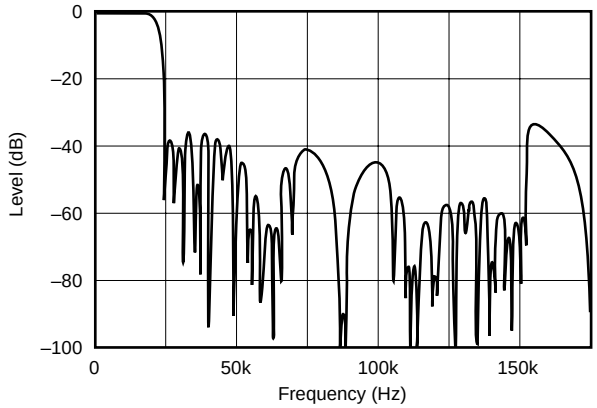


TYPICAL PERFORMANCE CURVES

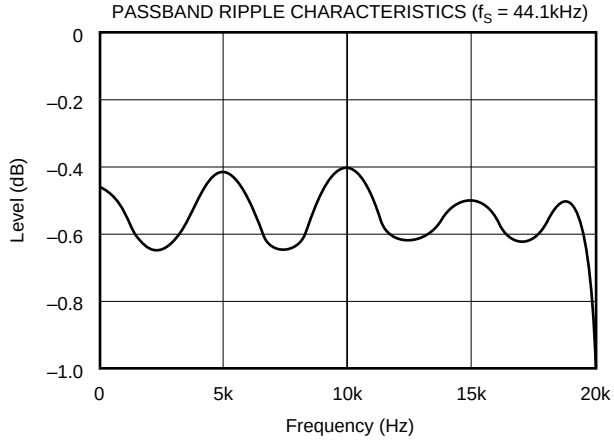
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, and f_{SYSCLK} = 384f_S, unless otherwise noted.

DAC DIGITAL FILTER

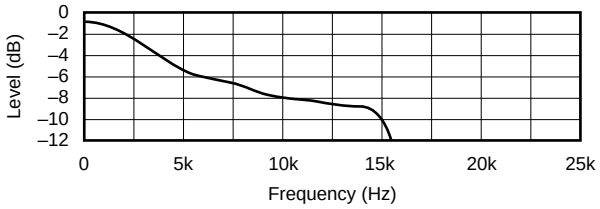
OVERALL FREQUENCY CHARACTERISTICS (f_S = 44.1kHz)



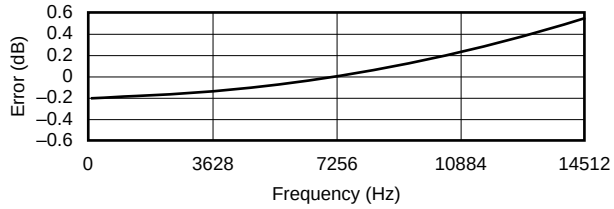
PASSBAND RIPPLE CHARACTERISTICS (f_S = 44.1kHz)



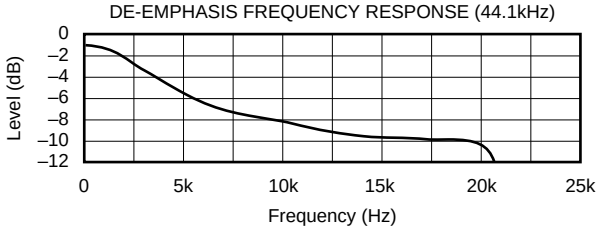
DE-EMPHASIS FREQUENCY RESPONSE (32kHz)



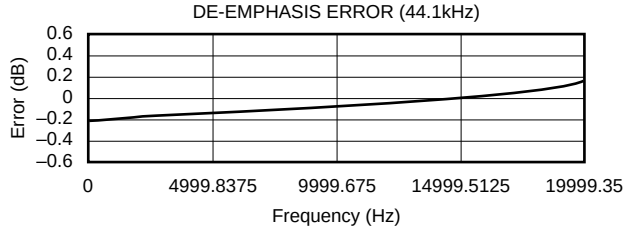
DE-EMPHASIS ERROR (32kHz)



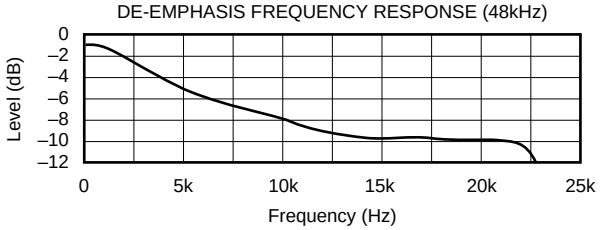
DE-EMPHASIS FREQUENCY RESPONSE (44.1kHz)



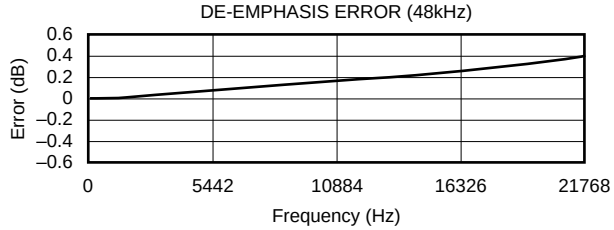
DE-EMPHASIS ERROR (44.1kHz)



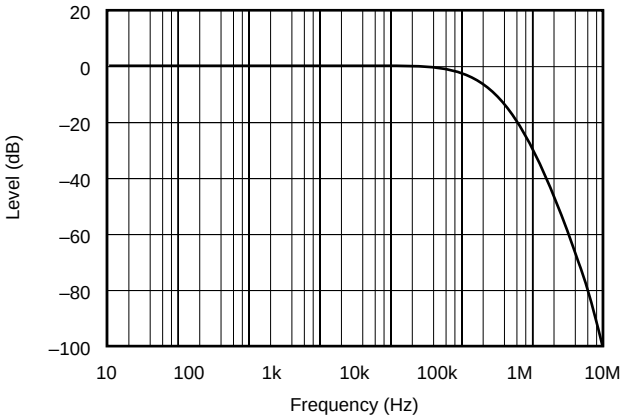
DE-EMPHASIS FREQUENCY RESPONSE (48kHz)



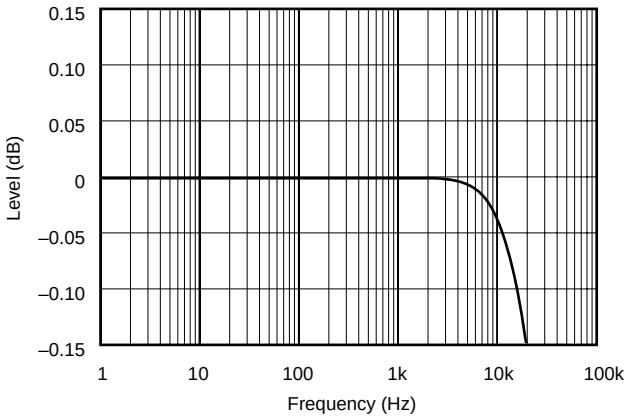
DE-EMPHASIS ERROR (48kHz)



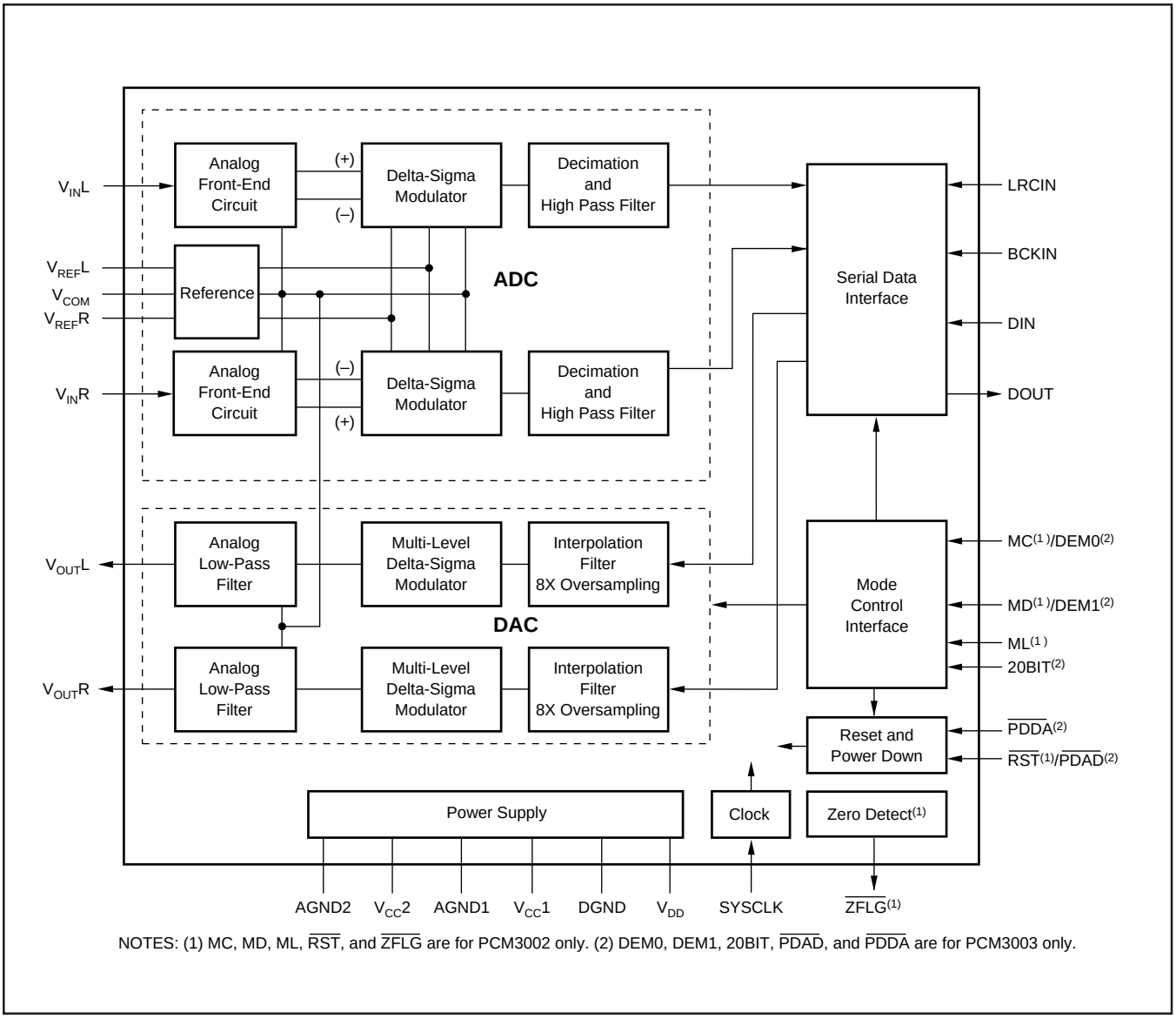
INTERNAL ANALOG FILTER FREQUENCY RESPONSE (10Hz~10MHz)



INTERNAL ANALOG FILTER FREQUENCY RESPONSE (1Hz~20kHz)



BLOCK DIAGRAM



NOTES: (1) MC, MD, ML, $\overline{RST}$, and $\overline{ZFLG}$ are for PCM3002 only. (2) DEM0, DEM1, 20BIT, $\overline{PDAD}$, and $\overline{PDDA}$ are for PCM3003 only.

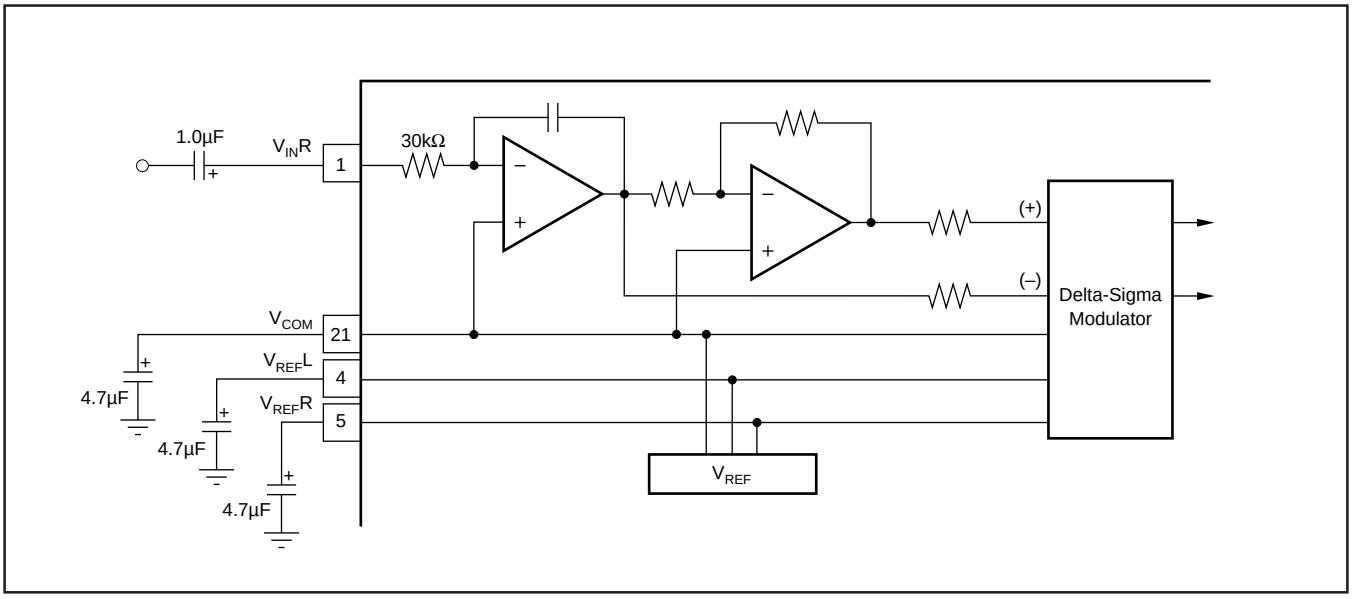


FIGURE 1. Analog Front-End (Single-Channel).

PCM AUDIO INTERFACE

The four-wire digital audio interface for PCM3002/3003 is comprised of: LRCIN (pin 10), BCKIN (pin 11), DIN (pin 15), and DOUT (pin 12). The PCM3002 may be used with any of the four input/output data formats (Formats 0 - 3), while the PCM3003 may only be used with selected input/output formats (Formats 0 - 1). For the PCM3002, these formats are selected through PROGRAM REGISTER 3 in the software mode. For the PCM3003, data formats are selected by the 20BIT input (pin 16). Figures 2, 3 and 4 illustrate audio data input/output formats and timing.

The PCM3002/3003 can accept 32-, 48-, or 64-bit clocks (BCKIN) in one clock of LRCIN. Only 16-bit data formats can be selected when 32-bit clocks/LRCIN are applied.

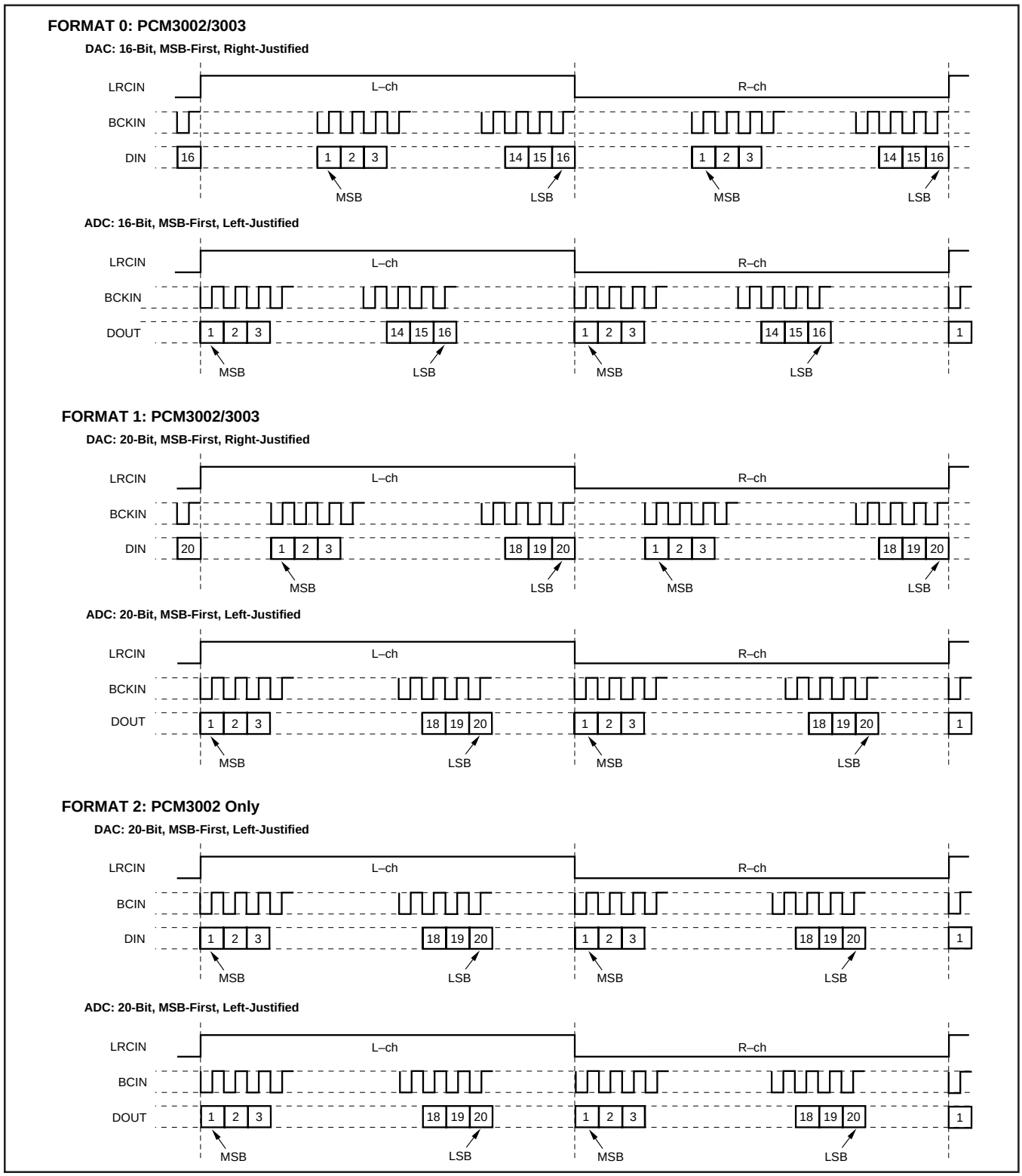


FIGURE 2. Audio Data Input/Output Format.

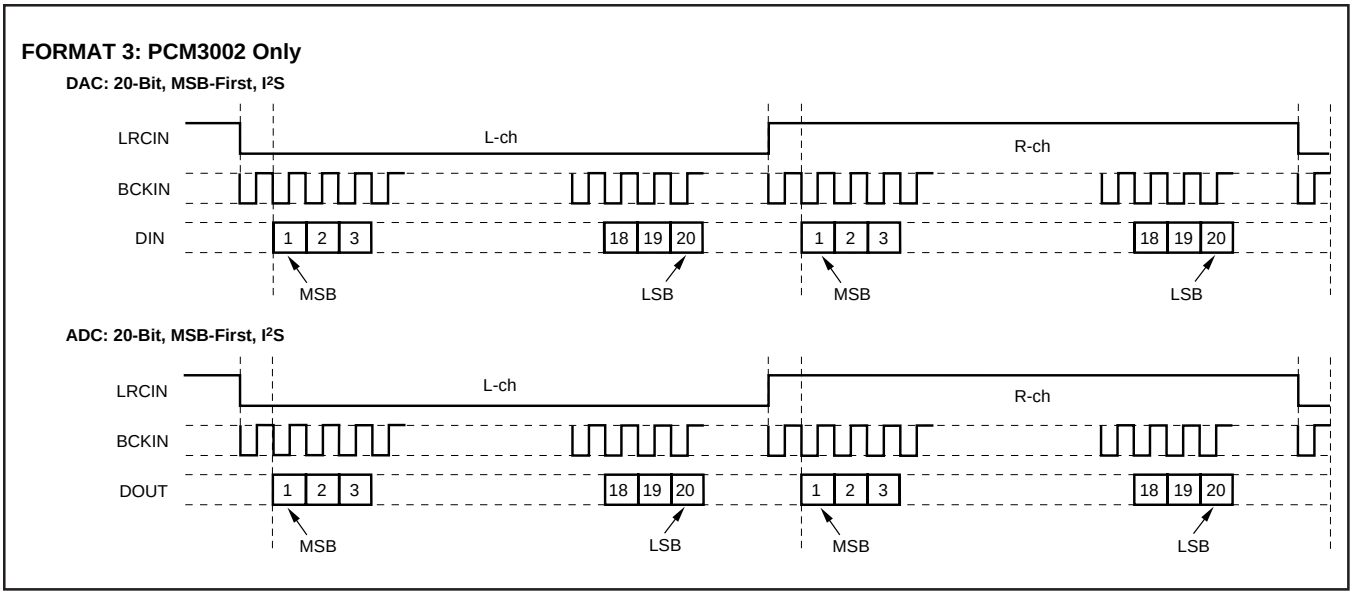
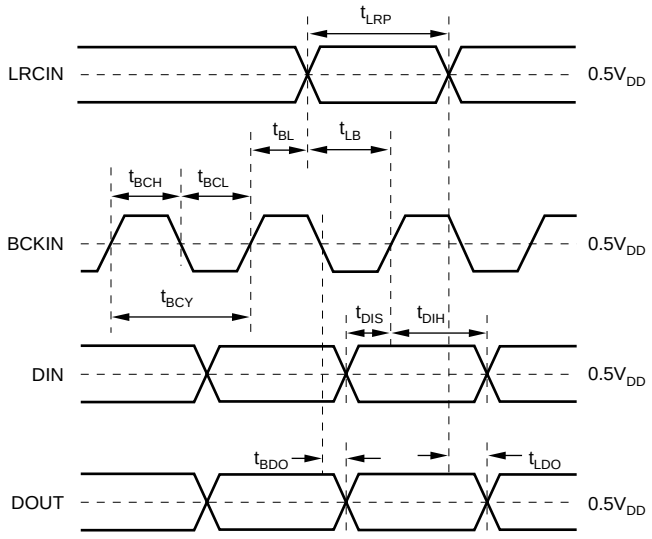


FIGURE 3. Audio Data Input/Output Format.



BCKIN Pulse Cycle Time	t_{BCY}	300ns (min)
BCKIN Pulse Width High	t_{BCH}	120ns (min)
BCKIN Pulse Width Low	t_{BCL}	120ns (min)
BCKIN Rising Edge to LRCIN Edge	t_{BL}	40ns (min)
LRCIN Edge to BCKIN Rising Edge	t_{LB}	40ns (min)
LRCIN Pulse Width	t_{LRP}	t_{BCY} (min)
DIN Set-up Time	t_{DIS}	40ns (min)
DIN Hold Time	t_{DIH}	40ns (min)
DOUT Delay Time to BCKIN Falling Edge	t_{BDO}	40ns (max)
DOUT Delay Time to LRCIN Edge	t_{LDO}	40ns (max)
Rising Time of All Signals	t_{RISE}	20ns (max)
Falling Time of All Signals	t_{FALL}	20ns (max)

FIGURE 4. Audio Data Input/Output Timing.

SYSTEM CLOCK

The system clock for PCM3002/3003 must be either $256f_S$, $384f_S$ or $512f_S$, where f_S is the audio sampling frequency. The system clock should be provided at the SYSCLK input (pin 9).

The PCM3002/3003 also has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$, $384f_S$, or $512f_S$. When $384f_S$ or $512f_S$ system clock is used, the clock is divided into $256f_S$ automatically. The $256f_S$ clock is used to operate the digital filters and the delta-sigma modulators.

Table I lists the relationship of typical sampling frequencies and system clock frequencies, while Figure 5 illustrates the system clock timing.

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	$256f_S$	$384f_S$	$512f_S$
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9340	22.5792
48	12.2880	18.4320	24.5760

TABLE I. System Clock Frequencies.

POWER-ON RESET

Both the PCM3002 and PCM3003 have internal power-on reset circuitry. Power-on reset occurs when system clock (SYSCLK) is active and $V_{DD} > 2.2V$. For the PCM3003, the SYSCLK must complete a minimum of 3 complete cycles prior to $V_{DD} > 2.2V$ to ensure proper reset operation. The initialization sequence requires 1024 SYSCLK cycles for completion, as shown in Figure 6. Figure 8 shows the state of the DAC and ADC outputs during and after the reset sequence.

EXTERNAL RESET

The PCM3002 includes a reset input, RST (pin 7), while the PCM3003 utilizes both PDAD (pin 7) and PDDA (pin 8) for external reset control. As shown in Figure 7, the external reset signal must drive RST or PDAD/PDDA low for a minimum of 40 nanoseconds while SYSCLK is active in order to initiate the reset sequence. Initialization starts on the rising edge of RST or PDAD/PDDA, and requires 1024 SYSCLK cycles for completion. Figure 8 shows the state of the DAC and ADC outputs during and after the reset sequence.

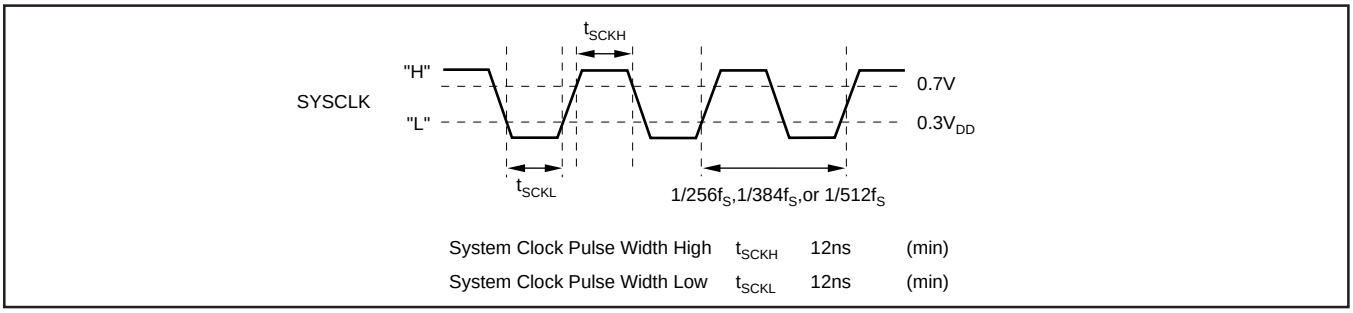


FIGURE 5. System Clock Timing.

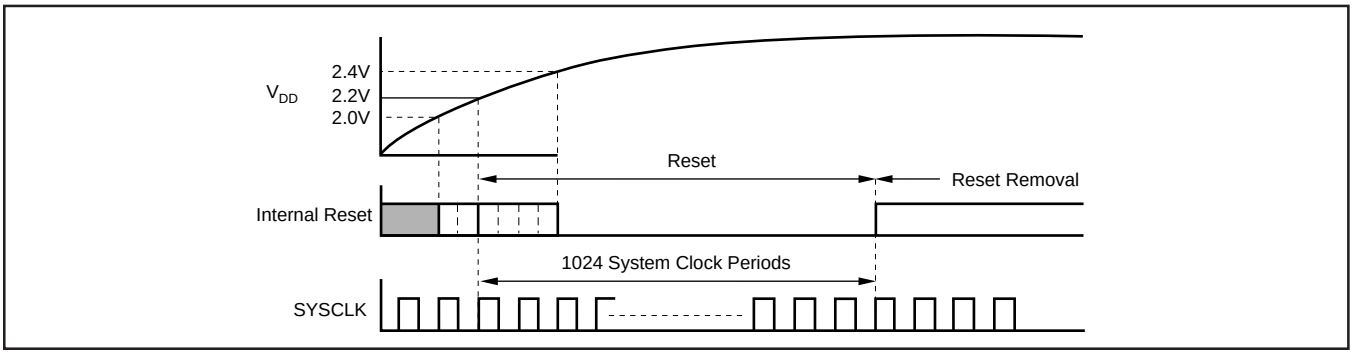


FIGURE 6. Internal Power-On Reset Timing.

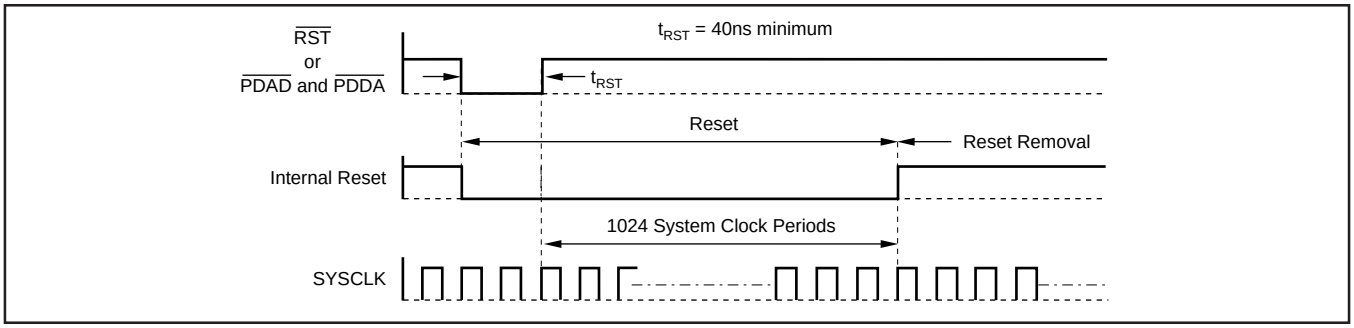


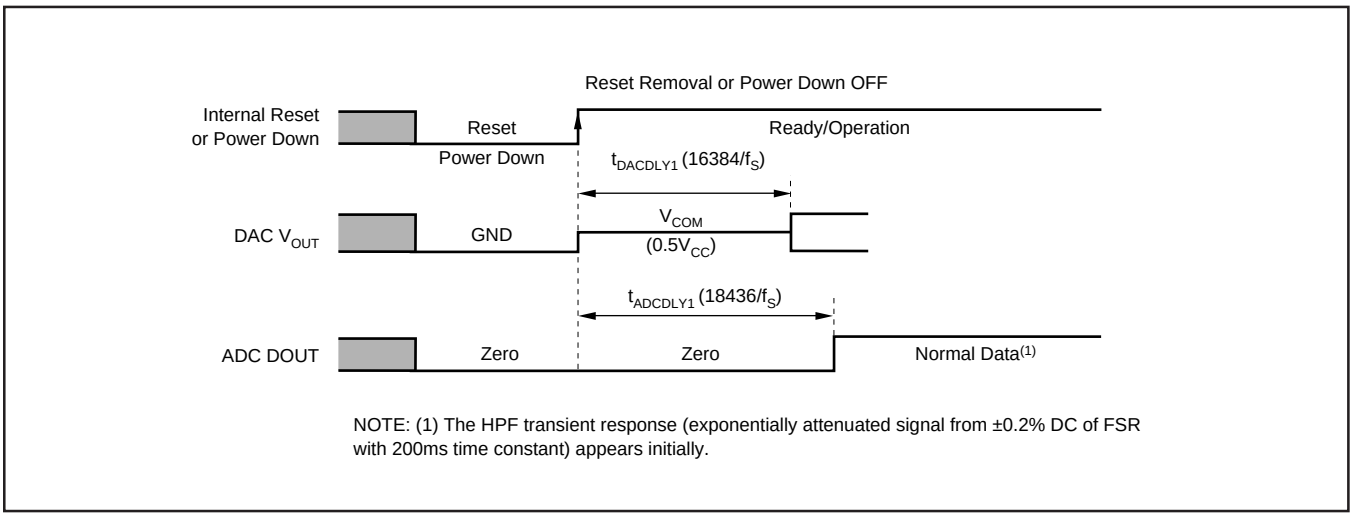
FIGURE 7. External Forced Reset Timing.

SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

The PCM3002/3003 operates with LRCIN synchronized to the system clock. PCM3002/3003 does not require any specific phase relationship between LRCIN and the system clock, but there must be synchronization. If the synchronization between the system clock and LRCIN changes more than 6 bit clocks (BCKIN) during one sample (LRCIN) period because of phase jitter on LRCIN, internal operation of the DAC will stop within $1/f_S$, and the analog output will be forced to bipolar zero ($0.5V_{CC}$) until the system clock is re-synchronized to LRCIN followed by $t_{DACDLY2}$ delay time. Internal operation of the ADC will also stop within $1/f_S$, and the digital output codes will be set to bipolar zero until re-synchronization occurs followed by $t_{ADCDLY2}$ delay time. If LRCIN is synchronized with 5 or less bit clocks to the system clock, operation will be normal. Figure 9 illustrates the effects on the output when synchronization is lost. Before the outputs are forced to bipolar zero ($<1/f_S$ seconds), the outputs are not defined and some noise may occur. During the transitions between normal data and undefined states, the output has discontinuities, which will cause output noise.

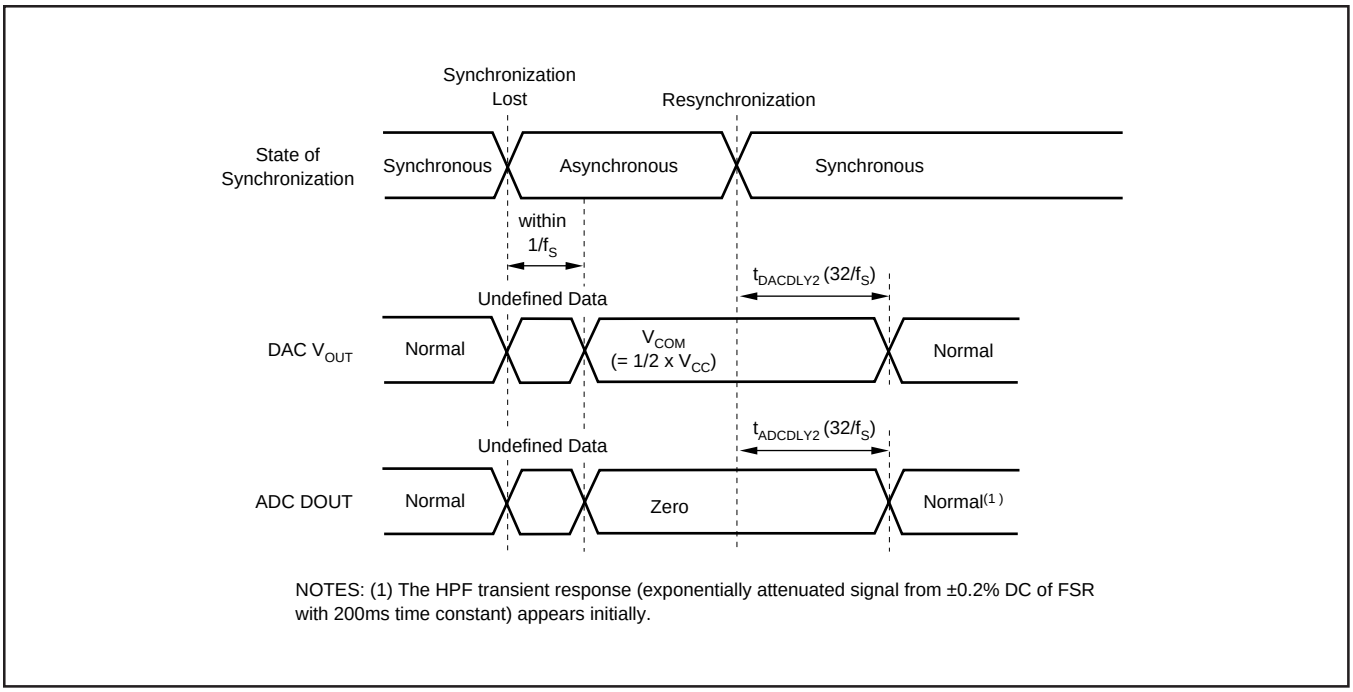
ZERO FLAG OUTPUT: PCM3002 ONLY

Pin 16 is an open-drain output, used as the infinite zero detection flag on the PCM3002 only. When input data is continuously zero for 65,536 BCKIN cycles, $\overline{ZFLG}$ is LOW, otherwise, $\overline{ZFLG}$ is in a high-impedance state.



NOTE: (1) The HPF transient response (exponentially attenuated signal from ±0.2% DC of FSR with 200ms time constant) appears initially.

FIGURE 8. DAC Output and ADC Output for Reset and Power Down.



NOTES: (1) The HPF transient response (exponentially attenuated signal from ±0.2% DC of FSR with 200ms time constant) appears initially.

FIGURE 9. DAC Output and ADC Output for Loss of Synchronization.

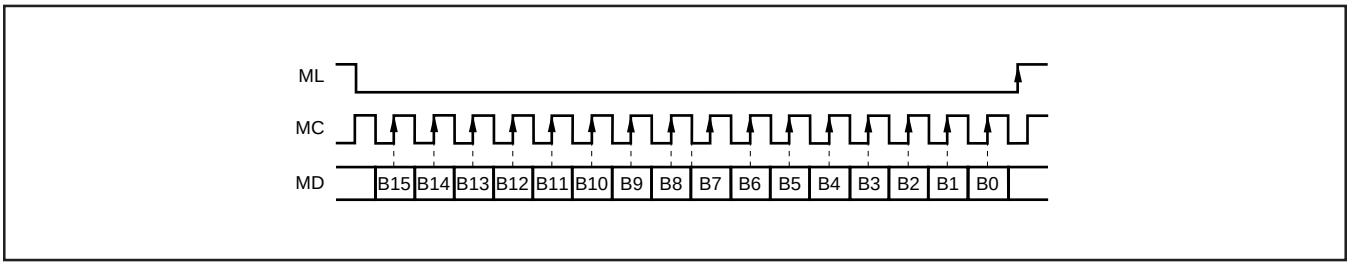
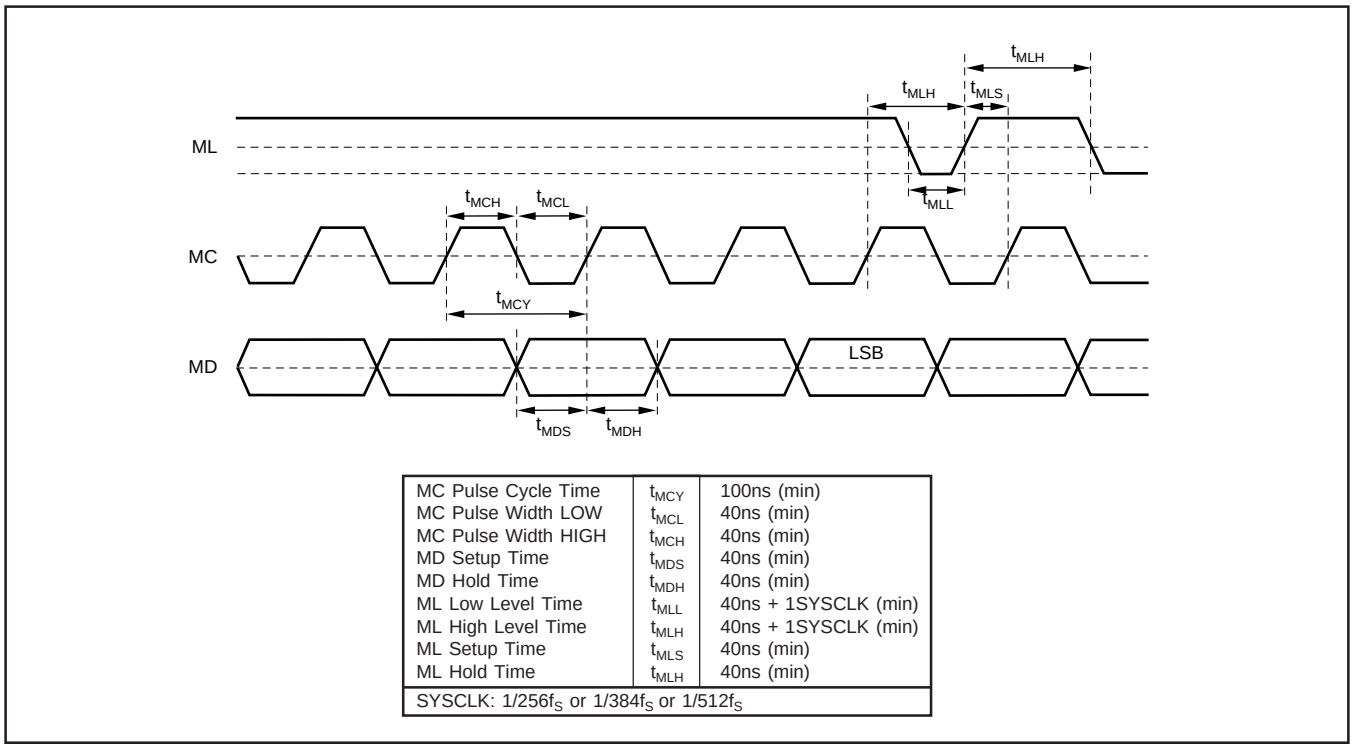


FIGURE 10. Control Data Input Format.



MC Pulse Cycle Time	t_{MCY}	100ns (min)
MC Pulse Width LOW	t_{MCL}	40ns (min)
MC Pulse Width HIGH	t_{MCH}	40ns (min)
MD Setup Time	t_{MDS}	40ns (min)
MD Hold Time	t_{MDH}	40ns (min)
ML Low Level Time	t_{MLL}	40ns + 1SYSCLK (min)
ML High Level Time	t_{MLH}	40ns + 1SYSCLK (min)
ML Setup Time	t_{MLS}	40ns (min)
ML Hold Time	t_{MLH}	40ns (min)
SYSCLK: $1/256f_S$ or $1/384f_S$ or $1/512f_S$		

FIGURE 11. Control Data Input Timing.

FUNCTION	ADC/DAC	PCM3002	PCM3003
Audio Data Format	ADC/DAC	4 Selectable Formats	2 Selectable Formats
LRCIN Polarity	ADC/DAC	O	X
Loop-Back Control	ADC/DAC	O	X
Left Channel Attenuation	DAC	O	X
Right Channel Attenuation	DAC	O	X
Attenuation Control	DAC	O	X
Infinite Zero Detection	DAC	O	X
DAC Output Control	DAC	O	X
Soft Mute Control	DAC	O	X
De-Emphasis (OFF, 32kHz, 44.1kHz, 48kHz)	DAC	O	O
ADC Power-Down Control	ADC	O	O
DAC Power-Down Control	DAC	O	O
High Pass Filter Operation	ADC	O	X

TABLE II. Selectable Functions (O = User Selectable; X = Not Available).

OPERATIONAL CONTROL

PCM3002 can be controlled in a software mode with a three-wire serial interface on MC (pin 18), MD (pin 17), and ML (pin 8). Table II indicates selectable functions, and Figure 10 and 11 illustrate the control data input format and timing. PCM3003 only allows for control of 16-/20-bit data format, digital de-emphasis, and Power-Down Control by hardware pins.

MAPPING OF PROGRAM REGISTERS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
REGISTER 1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
REGISTER 2	res	res	res	res	res	A1	A0	PDAD	BYPS	PDDA	ATC	IZD	OUT	DEM1	DEM0	MUT
REGISTER 3	res	res	res	res	res	A1	A0	res	res	res	LOP	res	FMT1	FMT0	LRP	res

SOFTWARE CONTROL (PCM3002)

PCM3002's special functions are controlled using four program registers which are 16 bits long. There are four distinct registers, with bits 9 and 10 determining which register is in use. Table III describes the functions of the four registers.

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	A (1:0)	Register Address "00"
	res	Reserved, should be set to "0"
	LDL	DAC Attenuation Data Load Control for Lch
	AL (7:0)	Attenuation Data for Lch
Register 1	A (1:0)	Register Address "01"
	res	Reserved, should be set to "0"
	LDR	DAC Attenuation Data Load Control for Rch
	AR (7:0)	DAC Attenuation for Rch
Register 2	A (1:0)	Register Address "10"
	res	Reserved, should be set to "0"
	PDAD	ADC Power-Down Control
	PDDA	DAC Power-Down Control
	BYPS	ADC High-Pass Filter Operation Control
	ATC	DAC Attenuation Data Mode Control
	IZD	DAC Infinite Zero Detection Circuit Control
	OUT	DAC Output Enable Control
	DEM (1:0)	DAC De-emphasis Control
	MUT	Lch and Rch Soft Mute Control
Register 3	A (1:0)	Register Address "11"
	res	Reserved, should be set to "0"
	LOP	ADC/DAC Analog Loop-Back Control
	FMT (1:0)	ADC/DAC Audio Data Format Selection
	LRP	ADC/DAC Polarity of LR-clock Selection

TABLE III. Functions of the Registers.

PROGRAM REGISTER 0

A (1:0): Bit 10, 9 Register Address

These bits define the address for REGISTER 0:

A1	A0	
0	0	Register 0

res: Bit 11 : 15 Reserved

These bits are reserved and should be set to "0".

LDL: Bit 8 DAC Attenuation Data Load Control for Left Channel

This bit is used to simultaneously set analog outputs of the left and right channels. The output level is controlled by AL (7:0) attenuation data when this bit is set to "1". When set to "0", the new attenuation data will be ignored, and the output level will remain at the previous attenuation level. The LDR bit in REGISTER 1 has the equivalent function as LDL. When either LDL or LDR is set to "1", the output level of the left and right channels are simultaneously controlled.

AL (7:0): Bit 7:0 DAC Attenuation Data for Left Channel

AL7 and AL0 are MSB and LSB, respectively. The attenuation level (ATT) is given by:

$ATT = 20 \times \log_{10}$ (ATT data/255) (dB)

AL (7:0)	ATTENUATION LEVEL
00h	–∞dB (Mute)
01h	–48.16dB
:	:
FEh	–0.07dB
FFh	0dB (default)

PROGRAM REGISTER 1

A (1:0): Register Address

These bits define the address for REGISTER 1:

A1	A0	
0	1	Register 1

res: Bit 15:11 Reserved

These bits are reserved and should be set to "0"

LDR: Bit 8 DAC Attenuation Data Load Control for Right Channel

This bit is used to simultaneously set analog outputs of the left and right channels. The output level is controlled by AL (7:0) attenuation data when this bit is set to "1". When set to "0", the new attenuation data will be ignored, and the output level will remain at the previous attenuation level. The LDL bit in REGISTER 0 has the equivalent function as LDR. When either LDL or LDR is set to "1", the output level of the left and right channels are simultaneously controlled.

AR (7:0): Bit 7:0 DAC Attenuation Data for Left Channel

AR7 and AR0 are MSB and LSB respectively. See REGISTER 0 for the attenuation formula.

PROGRAM REGISTER 2

A (1:0): Bit 10, 9 Register Address

These bits define the address for REGISTER 2:

A1	A0	
1	0	Register 2

res: Bit 15:11, 6 Reserved

These bits are reserved and should be set to “0”.

PDAD: Bit 8 ADC Power-Down Control

This bit places the ADC section in the lowest power consumption mode. The ADC operation is stopped by cutting the supply current to the ADC section, and DOUT is fixed to zero during ADC Power-down mode enable. Figure 8 illustrates the ADC DOUT response for ADC power-down ON/OFF. This does not affect the DAC operation.

PDAD	DAC POWER-DOWN
0	Power Down Mode Disabled (default)
1	Power Down Mode Enabled

BYPS: Bit 7 ADC High-Pass Filter Bypass Control

This bit enables or disables the high-pass filter for the ADC.

BYPS	
0	High-Pass Filter Enabled (default)
1	High-Pass Filter Disabled (bypassed)

PDDA: Bit 6 DAC Power-Down Control

This bit places the DAC section in the lowest power consumption mode. The DAC operation is stopped by cutting the supply current to the DAC section and V_{OUT} is fixed to GND during DAC Power-Down Mode enable. Figure 8 illustrates the DAC V_{OUT} response for DAC Power-Down ON/OFF. This does not affect the ADC operation.

PDDA	
0	Power-Down Mode Disabled (default)
1	Power-Down Mode Enabled

ATC: Bit 5 DAC Attenuation Channel Control

When set to “1”, the REGISTER 0 attenuation data can be used for both DAC channels. In this case, the REGISTER 1 attenuation data is ignored.

ATC	
0	Individual Channel Attenuation Data Control (default)
1	Common Channel Attenuation Data Control

IZD: Bit 4 DAC Infinite Zero Detection Circuit Control

This bit enables the Infinite Zero Detection Circuit in PCM3002. When enabled, this circuit will disconnect the analog output amplifier from the delta-sigma DAC when the input is continuously zero for 65,536 consecutive cycles of BCKIN.

IZD	
0	Infinite Zero Detection Disabled (default)
1	Infinite Zero Detection Enabled

OUT: Bit 3 DAC Output Enable Control

When set to “1”, the outputs are forced to $V_{CC}/2$ (bipolar zero). In this case, all registers in PCM3002 hold the present data. Therefore, when set to “0”, the outputs return to the previous programmed state.

OUT	
0	DAC Outputs Enabled (default normal operation)
1	DAC Outputs Disabled (forced to BPZ)

DEM (1:0): Bit 2,1 DAC De-emphasis Control

These bits select the de-emphasis mode as shown below:

DEM1	DEM0	
0	0	De-emphasis 44.1kHz ON
0	1	De-emphasis OFF (default)
1	0	De-emphasis 48kHz ON
1	1	De-emphasis 32kHz ON

MUT: Bit 0 DAC Soft Mute Control

When set to “1”, both left and right-channel DAC outputs are muted at the same time. This muting is done by attenuating the data in the digital filter, so there is no audible click noise when soft mute is turned on.

MUT	
0	Mute Disable (default)
1	Mute Enable

PROGRAM REGISTER 3

A (1:0): Bit 10:9 Register Address

These bits define the address for REGISTER 3:

A1	A0	
1	1	Register 3

res: Bit 15:11, 8:6, 4:0 Reserved

These bits are reserved, and should be set to “0”.

LOP: Bit 5 ADC to DAC Loop-Back Control

When this bit is set to "1", the ADC's audio data is sent directly to the DAC. The data format will default to I^2S. In Format 3 (I^2S Frame), Loop-back is not supported.

LOP	
0	Loop-back Disable (default)
1	Loop-back Enable

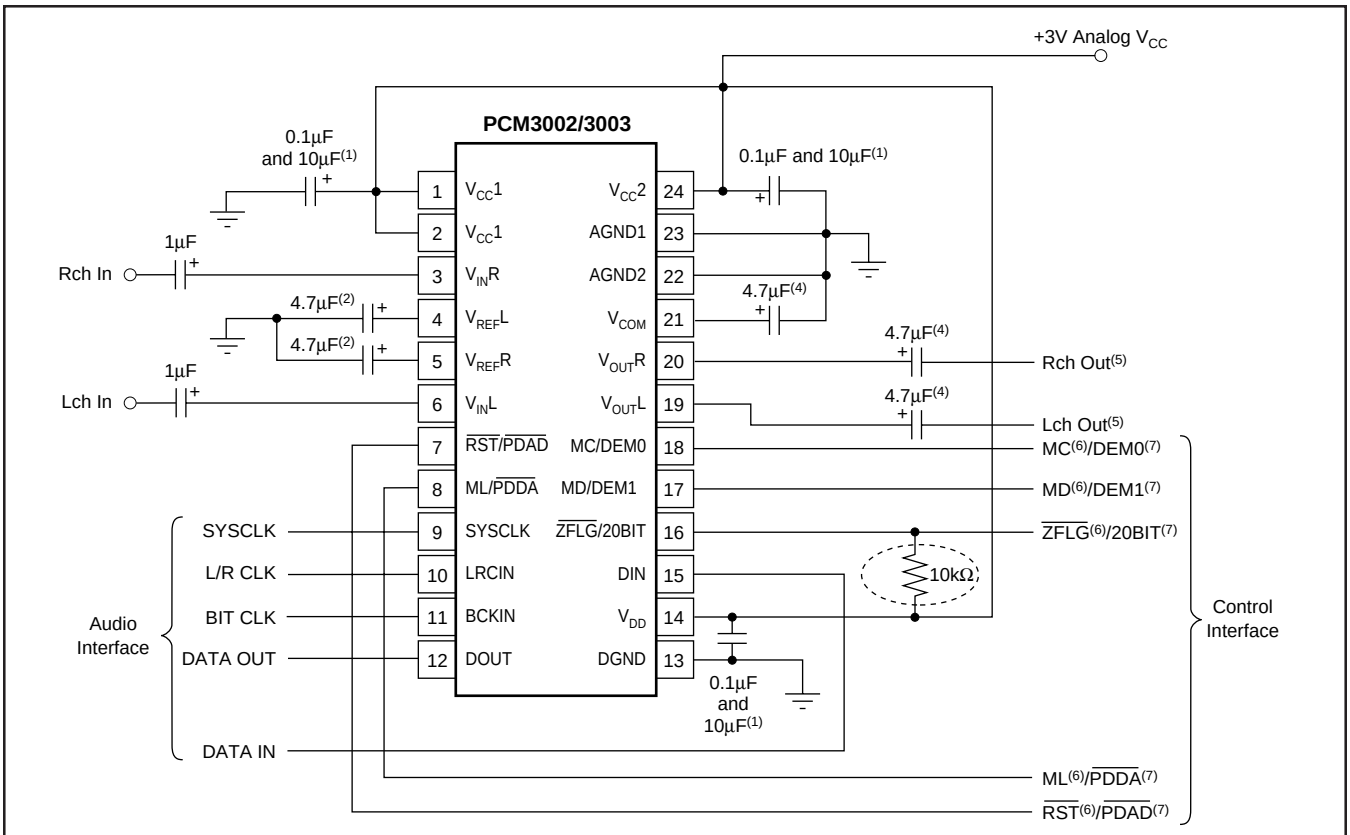
FMT (1,0) Bit 3:2 Audio Data Format Select

These bits determine the input and output audio data formats.

FMT1	FMT0	DAC Data Format	ADC Data Format	NAME
0	0	16-bit, MSB-first, Right-justified	16-bit, MSB-first, Left-justified	Format 0 (default)
0	1	20-bit, MSB-first, Right-justified	20-bit, MSB-first, Left-justified	Format 1
1	0	20-bit, MSB-first, Left-justified	20-bit, MSB-first, Left-justified	Format 2
1	1	20-bit, MSB-first, I^2S	20-bit, MSB-first, I^2S	Format 3

LRP: Bit 1 Polarity of LRCIN Applies only to Formats 0 through 2.

LRP	
0	Left-channel is "H", Right-channel is "L". (default)
1	Left-channel is "L", Right-channel is "H".



NOTES: (1) 0.1µF ceramic and 10µF tantalum, typical, depending on power supply quality and pattern layout. (2) 4.7µF typical, gives settling time with 30ms (4.7µF x 6.4kΩ) time constant in Power ON and Power-Down OFF period. (3) 1µF typical, gives 5.3Hz cut-off frequency of input HPF in normal operation and gives settling time with 30ms (1µF x 30kΩ) time constant in Power ON and Power -Down OFF period. (4) 4.7µF typical, gives 3.4Hz cut-off frequency of output HPF in normal operation and gives settling time with 47ms (4.7µF x 10kΩ) time constant in Power ON and Power-Down OFF period. (5) Post low pass filter with R_{IN} >10kΩ, depending on requirement of system performance. (6) MC, MD, ML, ZFLG, RST and 10kΩ pull-up resistor are for the PCM3002. (7) DEM0, DEM1, 20BIT, PDAD, PDDA are for the PCM3003.

FIGURE 12. Typical Connection Diagram for PCM3002/3003.

PCM3003 DATA FORMAT CONTROL

PCM3003 has hardware functional control using $\overline{\text{PDAD}}$ (pin 7) and $\overline{\text{PDDA}}$ (pin 8) for Power-Down Control; DEM0 (pin 18) and DEM1 (pin 17) for de-emphasis; and 20BIT (pin 16) for 16-/20-bit format selection.

Power-Down Control (Pin 7 and Pin 8)

Both the ADC's and DAC's Power-Down Control pins place the ADC or DAC section in the lowest power consumption mode. The ADC/DAC operation is stopped by cutting the supply current to the ADC/DAC section. DOUT is fixed to zero during ADC Power-Down Mode enable and V_{OUT} is fixed to GND during DAC Power-Down Mode enable. Figure 8 illustrates the ADC and DAC output response for Power-Down ON/OFF.

$\overline{\text{PDAD}}$	$\overline{\text{PDDA}}$	POWER DOWN
Low	Low	Reset (ADC/DAC Power-Down Enable)
Low	High	ADC Power-Down/DAC Operates
High	Low	ADC Operates/DAC Power-Down
High	High	ADC and DAC Normal Operation

De-Emphasis Control (Pin 17 and Pin 18)

DEM0 (pin 18) and DEM1 (pin 17) are used as de-emphasis control pins.

DEM1	DEM0	DE-EMPHASIS
Low	Low	De-Emphasis Enabled for 44.1kHz
Low	High	De-Emphasis Disabled
High	Low	De-Emphasis Enabled for 48kHz
High	High	De-Emphasis Enabled for 32kHz

20BIT Audio Data Selection (Pin 16)

20BIT	FORMAT
Low	ADC: 16-bit MSB-first, Left-justified DAC: 16-bit MSB-first, Right-justified
High	ADC: 20-bit MSB-first, Left-justified DAC: 20-bit MSB-first, Right-justified

APPLICATION AND LAYOUT CONSIDERATIONS

POWER SUPPLY BYPASSING

The digital and analog power supply lines to PCM3002/3003 should be bypassed to the corresponding ground pins with both 0.1µF ceramic and 10µF tantalum capacitors as close to the device pins as possible. Although PCM3002/3003 has three power supply lines to optimize dynamic performance, the use of one common power supply is generally recommended to avoid unexpected latch-up or pop noise due to power supply sequencing problems. If separate power supplies are used, back-to-back diodes are recommended to avoid latch-up problems.

GROUNDING

In order to optimize the dynamic performance of PCM3002/3003, the analog and digital grounds are not connected internally. The PCM3002/3003 performance is optimized with a single ground plane for all returns. It is recommended to tie all PCM3002/3003 ground pins with low impedance connections to the analog ground plane. PCM3002/3003 should reside entirely over this plane to avoid coupling high frequency digital switching noise into the analog ground plane.

VOLTAGE INPUT PINS

A tantalum or aluminum electrolytic capacitor, between 1µF and 10µF, is recommended as an AC-coupling capacitor at the inputs. Combined with the 30kΩ characteristic input impedance, a 1.0µF coupling capacitor will establish a 5.3Hz cut-off frequency for blocking DC. The input voltage range can be increased by adding a series resistor on the analog input line. This series resistor, when combined with the 30kΩ input impedance, creates a voltage divider and enables larger input ranges.

V_{REF} INPUTS

A 4.7µF to 10µF tantalum capacitor is recommended between $V_{REF}L$, $V_{REF}R$, and AGND to ensure low source impedance for the ADC's references. These capacitors should be located as close as possible to the reference pins to reduce dynamic errors on the ADC reference.

V_{COM} INPUTS

A 4.7µF to 10µF tantalum capacitor is recommended between V_{COM} and AGND to ensure low source impedance of the ADC and DAC common voltage. This capacitor should be located as close as possible to the V_{COM} pin to reduce dynamic errors on the DC common mode voltage.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance of both the ADC and DAC in the PCM3002/3003. The duty cycle and jitter at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCKIN) and a word clock (LCRIN) should also be supplied simultaneously. Failure to supply the audio clocks will result in a power dissipation increase of up to three times normal dissipation and may degrade long term reliability if the maximum power dissipation limit is exceeded.

EXTERNAL MUTE CONTROL

For Power-Down ON/OFF control without click noise which is generated by DAC output DC level change, an external mute control is recommended. The control sequence, which is external mute ON, CODEC Power-Down ON, SYSCLK stop and resume if necessary, CODEC Power-down OFF, and external mute OFF is recommended.

THEORY OF OPERATION

ADC SECTION

The PCM3002/3003 ADC consists of two reference circuits, a stereo single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The Block Diagram in this data sheet illustrates the architecture of the ADC section, Figure 1 shows the single-to-differential converter, and Figure 13 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal reference circuit with three external capacitors provides all reference voltages which are required by the ADC, which defines the full scale range for the converter. The internal single-to-differential voltage converter saves the space and extra parts needed for external circuitry required by many delta-sigma converters. The internal full-differential signal processing architecture provides a wide dynamic range and excellent power supply rejection performance. The input signal is sampled at 64X oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying anti-alias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator and a feedback loop consisting of a one-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The $64f_S$ one-bit data stream from the modulator is converted to $1f_S$ 18-bit data words by the decimation filter, which also acts as a low pass filter to remove the shaped quantization noise. The DC components are removed by a high pass filter function contained within the decimation filter.

THEORY OF OPERATION

DAC SECTION

The delta-sigma DAC section of PCM3002/3003 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 14. This 5-level delta-sigma modulator has the advantage of improved stability and reduced clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is $64f_S$ for a 256fS system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 15.

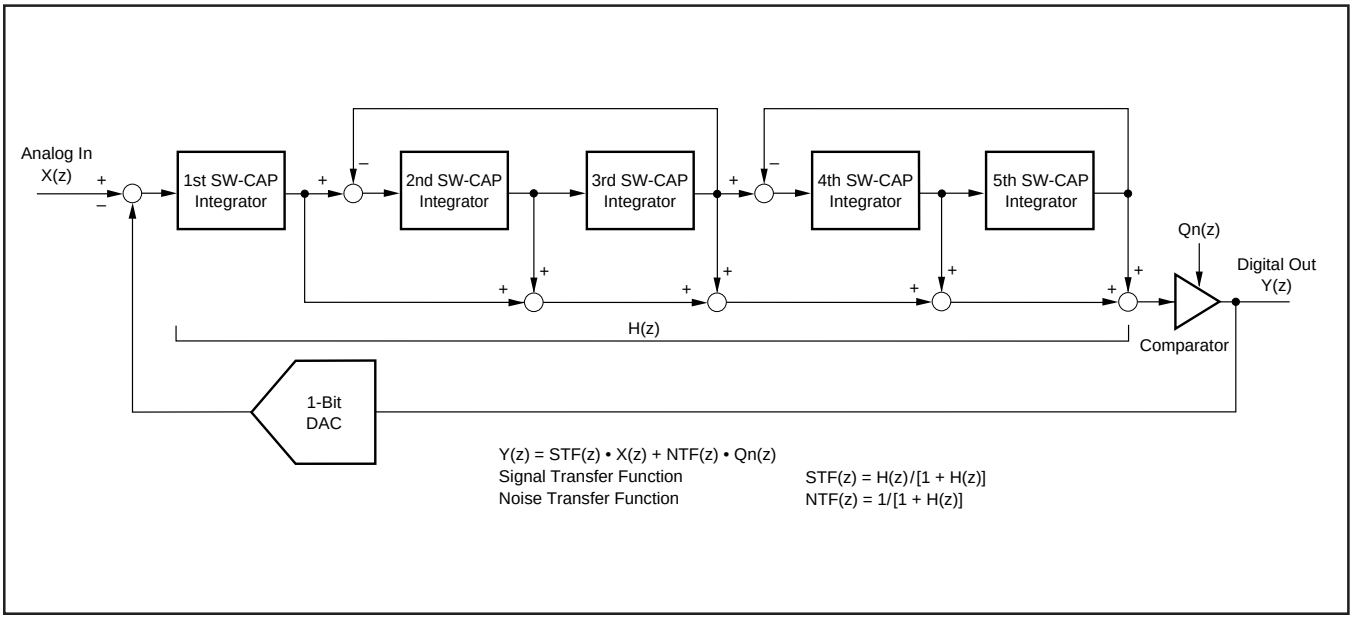


FIGURE 13. Simplified 5th-Order Delta-Sigma Modulator.

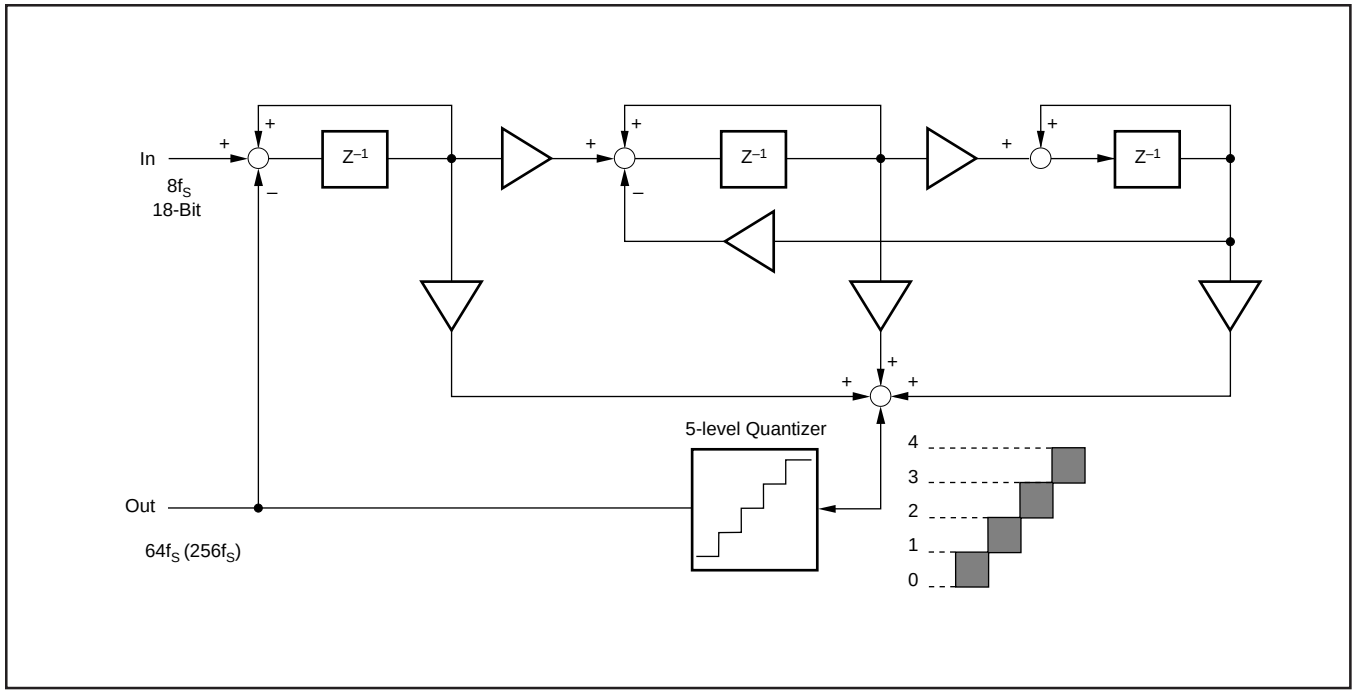


FIGURE 14. 5-Level Delta-Sigma Modulator Block Diagram.

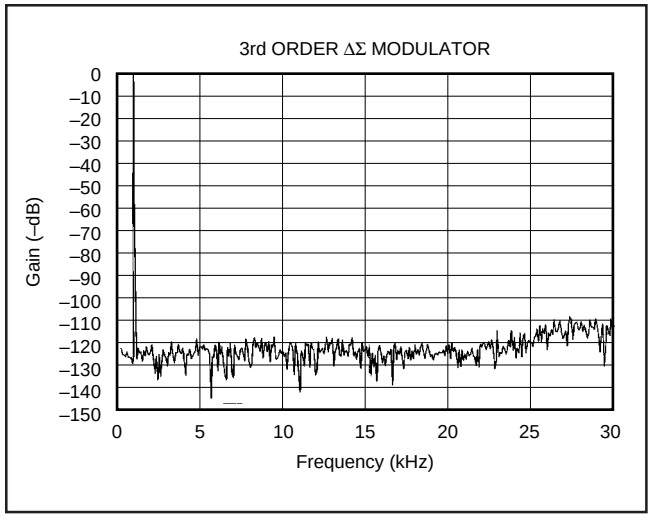


FIGURE 15. Quantization Noise Spectrum.

Multi Level Delta Sigma

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TEAC TECHNICAL INFORMATION

CD-RW Recorders, Converter MPU Change

No. **0328**
DATE 15th July 2003

Converter MPU, U707 of Converter PCB Assy, of following CD-RW recorders (*) has been changed as shown in the table.

* RW-H300/H500/800, CD-RW700/RW2000, RW-02/02USB, CD-RW4U

Version of Converter MPU	P/N of Converter MPU	P/N of Converter PCB (P/N printed on PCB)	S/N adopted respective converter MPU (X mark means there is no unit to adopt the MPU)						
			RW-H300	RW-H500	RW-800	CD-RW700	CD-RW2000	RW-02/02USB	CD-RW4U
Ver. 1.00 (Flash)	S003687-00A (IC, HD64F7044 CONVERT)	3E90247-00A [See Note-1).]				0010001			
Ver. 1.01 (Flash)	S003687-00B (IC, HD64F7044 CONVERT)	3E90247-00A /00B [See Note-1).]	0010001	0010001	0010001	0011001			
Ver. 1.02 (Masked)	S003688-00A (IC, HD6437042 CONVERT)	3E90247-00C /00D	0030481	0040001	0040001	0040001			
Ver. 1.03 (Masked)	S003829-00A (IC, HD6437042 CONVERT 2)	3E90247-00D				unknown			
Ver. 1.04 (Flash)	S003868-00A (IC, HD64F7044 CONVERT 3)	3E90247-00D					0010001		
Ver. 1.04 (Masked)	S003869-00A (IC, HD6437042 CONVERT 3)	3E90247-00D				(unknown)	(unknown)	0010001	
Ver. 1.10 (Flash)	S004186-00A (IC, HD64F7044 CONVERT 4)	3E90247-00D [See Note-2).]					0090001		
Ver. 1.10 (Masked)	S004185-00A (IC, HD6437042 CONVERT 4)		0120039	0120001	0160001	0131999	0130001	0020001	0010001
Ver. 1.11 (Masked)	S004264-00A (IC, HD6437042 CONVERT 5)	3E90247-00D [See Note-1).]	(unknown)	(unknown)	(unknown)	(unknown)	(unknown)	(unknown)	(unknown)

Note:
1) The latest Ver. 1.11 is supplied when you order the Converter MPU. However the Ver. 1.11 cannot be used with earlier two Converter PCBs, 3E90247-00A/00B. If the Ver 1.11 is mounted on the two Converter PCBs, unit doesn't work. In the case, replacing Converter PCB Assy is required.
2) This change is to support CD-RW4U.
3) RW-02/02USB and CD-RW4U have Main PCB E901168-00A instead of Converter PCB. On the models, Converter MPU is mounted on the Main PCB Assy as U109.
4) The Converter MPU U707 is a QPD SMD soldered on the Converter PCB without socket.

Fixed Problems

- V1.01 (Flash)

1) When "D-IN UNLOCK" is displayed, click noise is heard.
2) When sync-recording through digital input with certain MD recorder, unit doesn't stop even if the MD recorder stops.
3) When recording through digital input, sync-recording doesn't start even if 5 seconds or more elapses from beginning of track.

- V1.02 (Masked)

This change is to produce the V1.01 (Flash) by means of masked ROM method to reduce cost. There is no change of features.

- V1.03 (Masked)

To reduce Mech Assy vibration resulting some noise, rotational speed of disc in play mode is reduced from 8 times to 4 times.

- V1.04 (Flash)

This change is to support CD-RW2000.

- V1.04 (Masked)

This change is to produce the V1.04 (Flash) by means of masked ROM method to reduce cost. There is no change of features.

- V1.10 (Flash)

This change is to support CD-RW4U.

- V1.10 (Masked)

This change is to produce the V1.10 (Flash) by means of masked ROM method to reduce cost. There is no change of features.

- V1.11 (Masked)

Level meter indication disappears when following steps are operated:
1) Record a sound by Sync-record method.
2) Set the unit to digital in monitor mode.
3) Level meter indication disappears when following a) or b) feature starts:
   a) Sync record
   b) Index increment

Note: This appears with V1.10 (Flash/Masked) only.