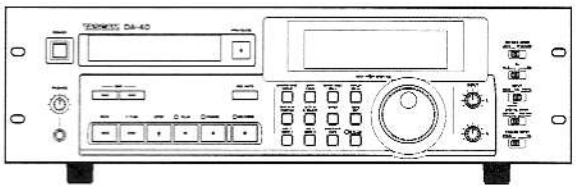

TASCAM
TEAC Professional Division

SERVICE MANUAL

DA-40

Digital Audio Tape Deck

INSTRUCTIONS FOR SERVICE PERSONNEL

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE - CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

Effective : Feburuary, 1999 4A2988

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テストモード

1-1. SW test mode

1. Activating the test mode
   Press the **POWER** switch to ON while pressing the **OPEN/CLOSE** button, **REC MUTE** key and **RECORD** key to engage the SW test mode. All indications on the display will go off.
2. Ending the test mode
   Turn the power OFF to end the test mode.

* For all tact switches, the name of the key that you press is shown on the display. When the **PLAY** key, **PAUSE** key, **RECORD** key or **SHIFT** key is pressed, the corresponding LED lights.
* While the **F FWD** key and **STOP** key are pressed simultaneously, the **RECORD MODE** switch settings are shown on the display.
* While the **STOP** key and **PLAY** key are pressed simultaneously, the **Fs** switch settings are shown on the display.
* While the **PLAY** key and **PAUSE** key are pressed simultaneously, the **INPUT** switch settings are shown on the display.
* While the **PAUSE** key and **RECORD** key are pressed simultaneously, the **DIGITAL INPUT** switch settings are shown on the display.
* Set the **Fs** switch to **48k** to show **"Jog 0 Shtl 0"** on the display.
  - When turning the DATA dial, make sure that the **"Jog 0"** indication changes from 0 to f.
  - When turning the SHUTTLE knob, make sure that the **"Shtl 0"** indication changes from 0 to f.

1-2. Display test mode

Press the ▶▶| key together with the |◀◀ key in the SW test mode to engage the display test mode. **"24 BIT"** will light on the display.
Press the ▶▶| key together with the |◀◀ key in the display test mode to restore the SW test mode.

* When you press the **REC MUTE** key, the points on the L and R level meters light consecutively.
* When you press the **RECORD** key, the digits in the counter section light consecutively.
* When you press the **COUNTER MODE** key, the meter scale, **"ABS"**, **"PGM"**, **"REMAIN"**, **"H"**, **"M"**, **"S"**, **"PNO"**, **"F"**, **"MARG"**, **"."**, **"%"** and **"dB"** all are illuminated simultaneously.
* When you press the **CHAR** key, **"EXT"**, **"TC"**, **"TOC"**, **"CHAR"**, **"EDIT"**, **"CAPS"**, **"ALL"**, **"REPEAT"**, **"A-B"** and **"PROGRAM"** all are illuminated simultaneously.
* When you press the **MARGIN RESET** key, **"SINGLE"**, **"START ID"**, **"48.0k"**, **"32.0k"**, **"SKIP PLAY"**, **"SKIP ID"**, **"44.1k"**, and **"LP"** all are illuminated simultaneously.
* When you press the **DISPLAY** key, **"DIGITAL IN"**, **"WORD"**, **"INT"**, **"H"**, **"M"**, **"S"**, **"PNO"** and **"VIDEO"** all are illuminated simultaneously.
* When you press the **SKIP PLAY** key, **"AUTO ID"**, **"START"**, **"CHAR"**, **"SKIP"**, **"WRT"**, **"END"**, **"ERASE"**, **"TOC"** and **"RENUM"** all are illuminated simultaneously.
* When you press the **STOP** key, all indications go out (except for **"24 BIT"**).
* Press the **PLAY** key to light up all indications on the display.

1-1. SWテストモード

1. テストモード起動
   OPEN/CLOSEボタン、REC MUTEキー、RECORDキーを押しながらPOWERスイッチをONにすると、SWテストモードになります。このとき、ディスプレイ内の表示が全消灯します。
2. テストモード終了
   電源をOFFにすると、テストモードは終了します。

*すべてのタクトSWについて、押されたキーの名称をディスプレイに表示する。
また、PLAYキー、PAUSEキー、RECORDキー、SHIFTキーの各キーを押したときは、そのキーに対応したLEDが点灯する。
*F FWDキーとSTOPキーを同時に押している間、RECORD MODEスイッチの設定内容をディスプレイに表示する。
*STOPキーとPLAYキーを同時に押している間、Fsスイッチの設定内容をディスプレイに表示する。
*PLAYキーとPAUSEキーを同時に押している間、INPUTスイッチの設定内容をディスプレイに表示する。
*PAUSEキーとRECORDキーを同時に押している間、DIGITAL INPUTスイッチの設定内容をディスプレイに表示する。
*Fsスイッチを48kに設定し、ディスプレイに"Jog 0 Shtl 0"と表示させる。
  - DATAダイアルを回すと、"Jog 0"の表示が0～fまで変化すること。
  - SHUTTLEノブを回すと、"Shtl 0"の表示が0～fまで変化すること。

1-2. 表示テストモード

SWテストモード時に、|◀◀ キーを押しながら、▶▶| キーを押すと表示テストモードになります。このとき、ディスプレイに"24 BIT"が点灯します。
また、表示テストモード時に、|◀◀ キーを押しながら、▶▶| キーを押すとSWテストモードに戻ります。

*REC MUTEキーを押すと、レベルメーターL, Rのドットが順番に点灯する。
*RECORDキーを押すと、カウンター部が順番に点灯する。
*COUNTER MODEキーを押すと、メーターケール、"ABS"、"PGM"、"REMAIN"、"H"、"M"、"S"、"PNO"、"F"、"MARG"、"."、"%"、"dB"が同時に点灯する。
*CHARキーを押すと、"EXT"、"TC"、"TOC"、"CHAR"、"EDIT"、"CAPS"、"ALL"、"REPEAT"、"A-B"、"PROGRAM"が同時に点灯する。
*MARGIN RESETキーを押すと、"SINGLE"、"START ID"、"48.0k"、"32.0k"、"SKIP PLAY"、"SKIP ID"、"44.1k"、"LP"が同時に点灯する。
*DISPLAYキーを押すと、"DIGITAL IN"、"WORD"、"INT"、"VIDEO"が同時に点灯する。
*SKIP PLAYキーを押すと、"AUTO ID"、"START"、"CHAR"、"SKIP"、"WRT"、"END"、"ERASE"、"TOC"、"RENUM"が同時に点灯する。
*STOPキーを押すと、ディスプレイ内の表示が全消灯する。
("24 BIT"表示を除く)
*PLAYキーを押すと、ディスプレイ内の表示が全点灯する。

1-3. DIGITAL IN information and tape recording information display function

1. Activating the display mode
   Press the **SHIFT** key to ON, then press the **STOP** key, **REC MUTE** key and **EDIT** key simultaneously to engage this mode. "**CLK XX 0000**" will be shown on the display.
2. Display switching
   Press the **EDIT** key to switch the display from A to J as shown below.
   * Press the **DEL/−** key to reverse the display order.
3. Ending the display mode
   Press the **SHIFT** key to OFF, then press the **COUNTER MODE** key to restore the normal mode.

A. DIGITAL INPUT clock accuracy indication

"CLK XX 0000"

Set the **INPUT** switch to **DIGITAL**, then input a digital signal to the input jacks selected with the **DIGITAL INPUT** switch to set the mode to INPUT MONITOR. When the digital input signal is locked (**DIGITAL IN** lit), Fs and clock accuracy are shown.

Fs is shown in the XX section.
The clock's accuracy is displayed with hexadecimal digit and +/− with respect to 0000. With one count, a shift of about 43 ppm occurs. (0.1 % = 1000 ppm)
For example, when the indication is "**+0016**", it is converted to +22 in decimals, causing a shift of about +1000 ppm.

B. C-bit/PLL Lock information indication (1)

"D I a B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0 "

B_7 : RCAT
  1 : DAT or DATP category code
  0 : All others
B_6, B_5 : RE2, RE1
  0 0 : no emphasis 0 1 : emphasis 50/15 μs
B_4 : RCPY
  1 : Copy prohibited 0 : Copy permited
B_3 : RDA
  1 : Digital data 0 : Audio data
B_2 : RPC
  1 : Professional use 0 : Consumer use
B_1 : Not used
B_0 : UNLK
  1 : PLL unlock 0 : PLL lock

1-3. DIGITAL IN情報およびテープ記録内容の表示機能

1. 表示モード起動
   SHIFTキーを押してONにした後、STOPキー、REC MUTEキー、EDITキーを同時に押すと、このモードになります。このとき、ディスプレイに "CLK XX 0000" が表示されます。
2. 表示切り換え
   EDITキーを押すことにより、下記のAからJまでの表示を切り換えることができます。
   *逆順に表示を換えたいときは、DEL/−キーを押します。
3. 表示モード終了
   SHIFTキーを押してOFFにした後、COUNTER MODEキーを押すと、通常モードになります。

A. DIGITAL INPUTのクロック精度表示

"CLK XX 0000"

INPUTスイッチをDIGITALにして、DIGITAL INPUTスイッチで選択した入力端子にデジタル信号を入力し、INPUT MONITORモードにします。

デジタル入力信号がロックしているとき（DIGITAL IN点灯）、Fsとクロック精度を表示します。

上記XX部にFsを表示します。
クロック精度は、0000を中心にして+/−で16進表示します。
1カウントで約43 ppm程度のずれとなります。
(0.1 % = 1000 ppm)
例えば、表示が "+0016" なら10進に直すと+22カウントとなり、約+1000 ppmのずれとなります。

B. C-bit/PLL Lock情報表示 (1)

"D I a B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0 "

B_7 : RCAT
  1 : カテゴリーコードがDATまたはDATP
  0 : それ以外
B_6, B_5 : RE2, RE1
  0 0 : no emphasis 0 1 : emphasis 50/15 μs
B_4 : RCPY
  1 : コピー禁止 0 : コピー許可
B_3 : RDA
  1 : デジタルデータ 0 : オーディオデータ
B_2 : RPC
  1 : プロ 0 : コンシューマ
B_1 : 未使用
B_0 : UNLK
  1 : PLLアンロック 0 : PLLロック

C. C-bit/U-bit information indication (2)

"DIb B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7 : RST
1 : START-ID
B_6 : RSH
1 : SKIP-ID
B_5, B_4 : RF2, RF1
0 0 : Fs 48k 0 1 : Fs 44.1k 10 : Fs 32k
B_3, B_2, B_1 : Not used
B_0 : STID
Track space information from CD
1 : Space between tracks 0 : The middle of a track

D. C-bit category information indication when formatted for consumer use

"CAT. B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7 ~ B_0 : C7 ~ C0
Category code
Example. DAT :1 1 0 0 0 0 0 0
DATP :1 1 0 0 0 0 0 1
CD :1 0 0 0 0 0 0 0

E. Digital output mode setting indication

"DO B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7 : 0
B_6 : 0/1
B_5 : PRCN
Digital output format setting
1 : Professional use 0 : Consumer use
B_4 : 1
B_3 : 0
B_2, B_1 : Not used
B_0 : XOFF
START ID or SKIP ID transmission setting
1 : Not transmitted 0 : Transmitted

F. Format-ID, ID-1, ID-2 and ID-3 indications recorded on the tape

"IDa B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7, B_6 : Format-ID
0 0 : Audio 0 1 : Data 1 0 : reserved 1 1 : reserved
B_5, B_4 : ID-1 (Emphasis)
0 0 : off 0 1 : 50/15 μs 1 0 : reserved
1 1 : reserved
B_3, B_2 : ID-2 (Fs)
0 0 : 48k 0 1 : 44.1k 1 0 : 32k 1 1 : reserved
B_1, B_0 : ID-3 (Channel)
0 0 : 2ch 0 1 : 4ch 1 0 : reserved 1 1 : reserved

C. C-bit/U-bit情報表示 (2)

"DIb B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7 : RST
1 : START-ID
B_6 : RSH
1 : SKIP-ID
B_5, B_4 : RF2, RF1
0 0 : Fs 48k 0 1 : Fs 44.1k 10 : Fs 32k
B_3, B_2, B_1 : 未使用
B_0 : STID
CDからの曲間情報 1 : 曲間 0 : 曲中

D. コンシューマフォーマット時のC-bitカテゴリー情報表示

"CAT. B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7 ~ B_0 : C7 ~ C0
カテゴリーコード8ビットを2進数で表示
例. DAT :1 1 0 0 0 0 0 0
DATP :1 1 0 0 0 0 0 1
CD :1 0 0 0 0 0 0 0

E. DIGITAL OUTPUTモード設定表示

"DO B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7 : 0
B_6 : 0/1
B_5 : PRCN
デジタル出力のフォーマットの設定
1 : プロ 0 : コンシューマ
B_4 : 1
B_3 : 0
B_2, B_1 : 未使用
B_0 : XOFF
スタートID, スキップIDの送信を止めるか否かの設定
1 : 送信しない 0 : 送信する

F. テープに記録されているFormat-ID、ID-1、ID-2、ID-3表示

"IDa B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7, B_6 : Format-ID
0 0 : Audio 0 1 : Data 1 0 : reserved 1 1 : reserved
B_5, B_4 : ID-1 (Emphasis)
0 0 : off 0 1 : 50/15 μs 1 0 : reserved
1 1 : reserved
B_3, B_2 : ID-2 (Fs)
0 0 : 48k 0 1 : 44.1k 1 0 : 32k 1 1 : reserved
B_1, B_0 : ID-3 (Channel)
0 0 : 2ch 0 1 : 4ch 1 0 : reserved 1 1 : reserved

G. ID-4, ID-5, ID-6 and ID-7 indications recorded on the tape

"IDb B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7, B_6 : ID-4 (Quantization)
0 0 : 16bits 0 1 : 12bits 1 0 : reserved
1 1 : reserved
B_5, B_4 : ID-5 (Track pitch)
0 0 : normal 0 1 : wide 1 0 : reserved
1 1 : reserved
B_3, B_2 : ID-6 (Digital copy)
0 0 : permitted 0 1 : reserved 1 0 : prohibited
1 1 : special
B_1, B_0 : ID-7 (Pack)
Pack contents

H. Pack Item indication recorded on the tape

"Item XXXXXXX"

Pack Item	Contents
0	Not provided
1	Program time
2	Absolute time
3	Running time
4	TOC
5	Date
6	Catalog number
7	International standard recording code
8	Pro binary
9	Character

Example :

DA-40	2100000 or 2190000
DA-30MK2	2100000
DA-60MK2	2213800
PCM-7050	3333328
DTC-790	2222111

I. System internal mode indication

"Mode AABBCC"

J. System control microprocessor version indication

"ROM Ver 1.00"

G. テープに記録されているID-4、ID-5、ID-6、ID-7表示

"IDb B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0"

B_7, B_6 : ID-4 (Quantization)
0 0 : 16bits 0 1 : 12bits 1 0 : reserved
1 1 : reserved
B_5, B_4 : ID-5 (Track pitch)
0 0 : normal 0 1 : wide 1 0 : reserved
1 1 : reserved
B_3, B_2 : ID-6 (Digital copy)
0 0 : permitted 0 1 : reserved 1 0 : prohibited
1 1 : special
B_1, B_0 : ID-7 (Pack)
Pack contents

H. テープに記録されているPack Item表示

"Item XXXXXXX"

Pack Item	内容
0	未規定
1	プログラム時間
2	絶対時間
3	ランニング時間
4	TOC
5	日付
6	カタログ番号
7	国際標準記録コード
8	プロバイナリー
9	文字

例.

DA-40	2100000 or 2190000
DA-30MK2	2100000
DA-60MK2	2213800
PCM-7050	3333328
DTC-790	2222111

I. システム内部モード表示

"Mode AABBCC"

J. システムコントロールマイコンROMバージョン表示

"ROM Ver 1.00"

1-4. Mechanism mode display function

1. Display method
Press the **STOP** key, **REC MUTE** key and **DISPLAY** key simultaneously to engage this mode. Various information is shown with hexadecimal characters on the 6-digit display at the right of the counter. To restore the normal display, press the **DISPLAY** key.

2. Display contents

"U V W X Y Z"

U : The current mechanism mode is shown.

0 : TrayOpen	1 : TrayClose	2 : Upload
3 : Stop	4 : Pause	5 : Play
6 : Cue	7 : Review	8 : Rec
9 : FF	A : Rew	

V : When PLAY in the SP mode is "1" (normal speed), the current capstan speed is shown (with hexadecimal characters) by how many times faster it runs than at normal speed.
1 − F : 1 to 15 times normal speed

W : The current mechanical switch status is shown with hexadecimal characters.
bit 3 : Tray SW 1
bit 2 : Tray SW 2
bit 1 : Tray SW 3
bit 0 : Tray SW 4

X : The current mechanical switch status is shown with hexadecimal characters.

bit 3 : Cassette	L = set
bti 2 : A. E. P	L = hole closed (Possible to record)
bit 1 : RH3 (wide track)	L = hole close (Normal track)
bti 0 : RH2 (thin tape)	L = hole close (Normal 13 μ m)

* A. E. P : Accidental erasure prevention

Y : The current mechanism status is shown with the hexadecimal
bit 3 : The mechanism mode is being changed
H = Being changed
bit 2 : Tape position detection flag
H = Detected

bit 1 : Drum lock monitor	H = Lock
bit 0 : Capstan lock monitor	H = Lock

* bit 2 : Tape position detection flag
When the servo control is applied for high-speed running with FF or REW, tape position detection is necessary. When the tape is loaded, the tape position is not detected. However, once the tape has been run briefly in PLAY or CUE mode, the tape position can be detected.

Z : The current mechanism status is shown with hexadecimal characters.
bit 3 : − − − −
bit 2 : Monitoring the mechanism mode transition direction H = Transition for unloading
bit 1 : EOT H = EOT
bit 0 : BOT H = BOT

1-4. メカモード表示機能

1. 表示方法
STOPキー、**REC MUTE**キー、**DISPLAY**キーを同時に押すと、このモードになります。ディスプレイのカウンター部の右6桁にメカモードの各種情報を16進の数値で表示します。
表示を通常に戻すには、**DISPALY**キーを押します。

2. 表示内容

"U V W X Y Z"

U : 現在のメカモードを表示します。

0 : TrayOpen	1 : TrayClose	2 : Upload
3 : Stop	4 : Pause	5 : Play
6 : Cue	7 : Review	8 : Rec
9 : FF	A : Rew	

V : 現在のキャプスタンスピードをSPモードのPLAYを"1"として、その何倍速で走行しているかを16進数で表示します。
1 ～ F : 1 ～ 15倍速

W : 現在のメカスイッチ状態を16進数で表示します。
bit 3 : Tray SW 1
bit 2 : Tray SW 2
bit 1 : Tray SW 3
bit 0 : Tray SW 4

X : 現在のメカスイッチ状態を16進数で表示します。

bit 3 : Cassette	L = set
bti 2 : A. E. P	L = hole closed (Possible to record)
bit 1 : RH3 (wide track)	L = hole closed (Normal track)
bti 0 : RH2 (thin tape)	L = hole closed (Normal 13 μ m)

* A. E. P : Accidental erasure prevention (誤消去防止)

Y : 現在のメカ状態を16進数で表示します。

bit 3 : メカモード移行中	H = 移行中
bit 2 : テープ位置認識フラグ	H = 認識済み
bit 1 : ドラムロックモニタ	H = ロック
bit 0 : キャプスタンロックモニタ	H = ロック

* bit 2 : テープ位置認識フラグ
FF、REWで高速走行のサーボ制御をする場合、テープの位置を認識している必要があります。
テープをセットした時点では認識していませんが、テープをPLAY、CUE等で少しの間、走行させることで認識します。

Z : 現在のメカ状態を16進数で表示します。
bit 3 : − − − −
bit 2 : メカモード移行方向モニタ
H = Unloading方向に移行中
bit 1 : EOT H = EOT
bit 0 : BOT H = BOT

2. REMOVAL OF MECHANICAL PARTS
機構部品の外し方

This section primarily shows the disassembly procedure ; to reassemble, reverse the procedure.

2-1. Cautions in handling the mechanism ass'y

1. When lifting the mechanism ass'y, do NOT hold both edges with one hand ; hold the right and left edges of the chassis with two hands.
2. Do NOT touch the head drum.
3. After removing the mechanism ass'y, always place it with its right side up.
   If it must be placed upside down for any reason, place a protective sheet such as bubble packing, etc. underneath to protect the exterior of the cassette holder.
4. Do NOT touch the tip of the flexible PC board. Also do NOT pull or bend it strongly.
5. Do NOT lift the mechanism ass'y by the flexible PC board or leads.
6. Do NOT touch the guide roller with your bare hands. To clean dirt or dust off the roller, wipe it gently with a cotton swab moistened with alcohol.
7. Do NOT touch the portions of the posts which come into contact with the tape.
8. Do NOT touch the rubber portions of the pinch roller or belt and the felt portion of the tension band, etc. with greasy fingers.
9. Do NOT touch the pulley over which the belt is hooked with greasy fingers, etc.
10. If a screw secured with screw－locking compound is removed, reapply the compound after reinstalling it. Tightening screws with too much torque may strip the screw threads ; be careful.
11. When removing the coil spring, take care so that the hook is NOT deformed.
12. When the head becomes dirty, use a cleaning tape.
13. When reassembling, take care NOT to let leads or cables be pinched by the chassis, etc.
14. Do NOT touch the surface of the drum with which the tape comes into contact.
15. When lifting the drum, hold both sides of its base.
16. When placing the drum on a work bench, place it on a soft mat so that no load or impact is applied to the rotor of the drum and motor.
17. Do NOT lift the drum by its leads.
18. Do NOT perform any soldering near the drum.
19. Do NOT apply an external force to the upper drum.
20. Do NOT let the tip of a screwdriver or metallic object come into contact with the rotor. Especially magnets (or magnetized objects) should NOT be brought close to the rotor.
21. Do NOT touch the PG sensor with your fingers.
22. Do NOT lift the motor by the flexible PC board.

この項では外し方を主に記述しますが、組立は分解の逆の手順で行なって下さい。

2-1. メカニズム Ass'y取扱上の注意

1. メカニズム
   1) メカニズム Ass'yを掴むときは、片手で両側を強く掴まないこと。シャーシの左右の端を両手で掴むこと。
   2) シリンダーのドラム部には、手を触れないこと。
   3) メカニズム Ass'yを置くときは、衝撃を与えないように置くこと。また、メカニズム Ass'yは通常方向に置くこととし、やむおえず逆さまに置く場合は、下にエア・パッキン等保護材を敷き、カセット・ホルダーの外装部品を保護すること。
   4) フレキの先端部に手を触れないこと。また、フレキを強く引っ張ったり曲げたりしないこと。
   5) フレキまたはリード線を持って、メカニズム Ass'yを持ち上げないこと。
   6) ガイド・ローラーのローラーには、手で触らないこと。
   汚れを拭くときは、アルコールを綿棒に浸して軽く拭くこと。
   7) 各ポストのテープ走行面には、手で触らないこと。
   ピンセットやドライバー等で傷を付けないこと。また、磁化されたピンセット，ドライバーで触らないこと。
   8) ピンチローラー，ベルト等のゴム部、テンション・バンド等のフェルト部に油のついた手で触らないこと。
   9) ベルトのかかるプーリー等にグリスの付いた手で触らないこと。
   10) ネジ・ロックが付いているネジを外した場合は、取り付け後もネジ・ロックをすること。強く締めすぎるとネジバカになるので注意すること。
   11) コイル・スプリングを外すときは、フックの変形に注意をすること。
   12) ヘッドが汚れたときは、クリーニング・テープを使用すること。
   13) 組立の際、線材をシャーシー等に挟み込むことのないように注意すること。

2. シリンダー
   1) シリンダーのテープ走行面には、手を触れないこと。
   2) シリンダーを掴むときは、シリンダー・ベースの両端を持つこと。
   3) シリンダーを置く場合は、ドラム及びモーターのローターに荷重、衝撃を与えないように軟らかい物の上に置くこと。
   4) リード線を持ってシリンダーを持ち上げないこと。
   5) シリンダーの近くで半田付けをしないこと。
   6) 上ドラムに外力を加えないこと。

3. キャプスタン・モーター
   1) ローターにはドライバーの先を接触させたり、金属の物などを当てないこと。特に磁石（磁化したもの）は近付けないこと。
   2) PGセンサーには、手を触れないこと。
   3) フレキを持ってモーターを持ち上げないこと。

2-2. Disassembly of the Mechanism Base Unit-1

2-2. メカニズムベースユニットの分解－1

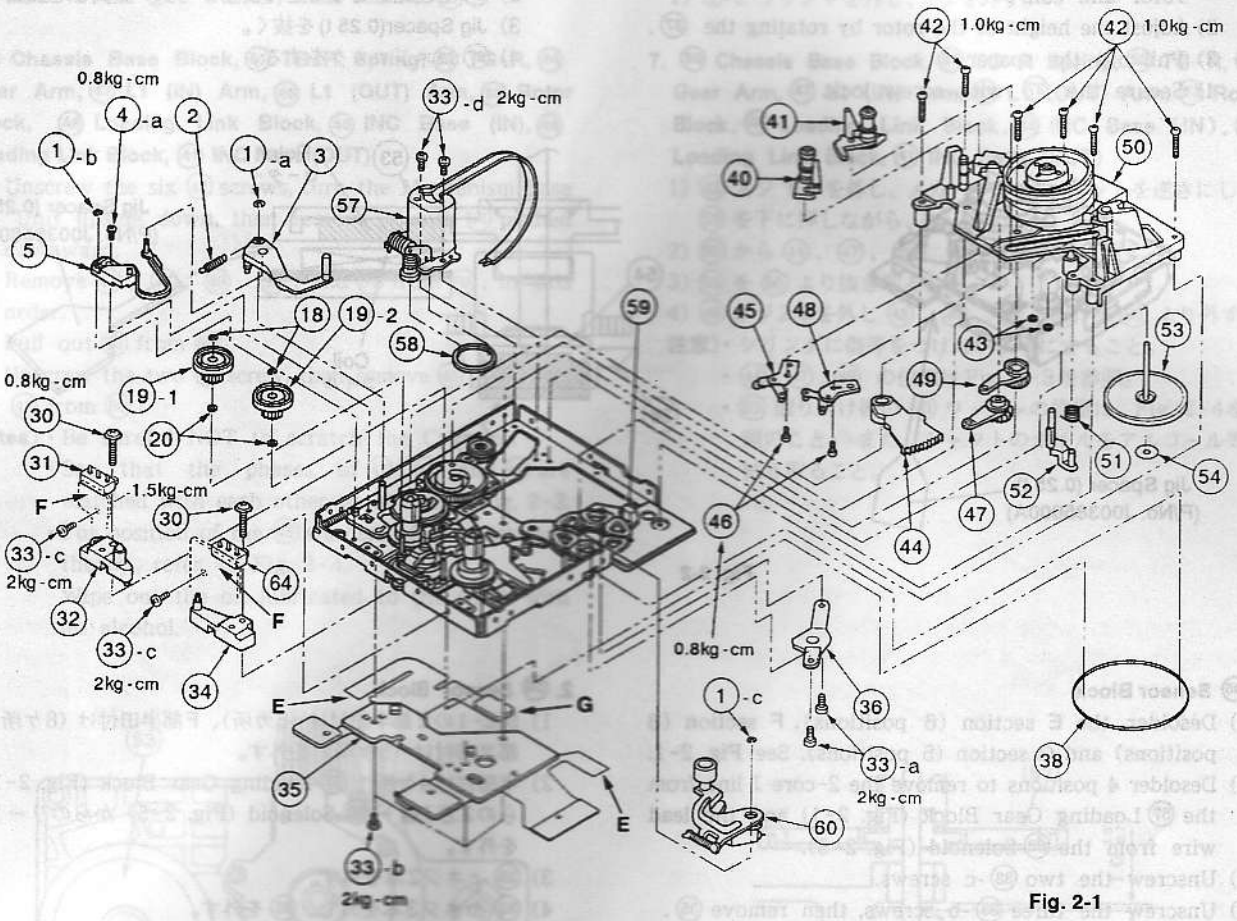


Fig. 2-1

1. ㊱ Capstan Bracket, ㊹ Capstan Flange, ㊳ Capstan Belt

1) Unscrew the two ㉝-a screws, then remove ㊱.
2) Remove ㊹ from the ㊸ Rotor Block, then detach ㊳.

Notes)

- Be careful NOT to scratch the Cylinder.
- When removing ㊹, be careful NOT to widen the inner diameter of it.
- When removing ㊳, be careful NOT to lengthen the Belt.
- When ㊸ is not replaced, the ㊲ Wheel Shaft Retainer (Fig. 2-2) should not be removed.
- When reinstalling the ㊸, procedure indicated next page. (refer to Fig. 2-2)

1. ㊱ Capstan Bracket, ㊹ Capstan Flange, ㊳ Capstan Belt

1) ㉝-aネジ2本を外し、㊱を外す。
2) ㊸ Rotor Blockから ㊹ を外し、㊳ を外す。

注意)

- シリンダに傷などをつけないようにすること。
- ㊹ を外すときに内径をひろげないようにすること。
- ㊳ を外すとき、ベルトを伸ばさないようにすること。
- ㊲ Wheel軸受け（図2-2）は、㊸ を交換しないときは外さないこと。
- ㊸ を取り付けるときは、次ページの手順を行ってください。（図2-2参照）

1) Insert a jig spacer(0.25 t), P/No. J00385600A between rotor and coil.
2) Adjust the height of the rotor by rotating the ㊲.
3) Pull out the spacer.
4) Secure the ㊲ with screw lock.

1) Jig Spacer(0.25 t)をローターとコイルの間に差し込む。
2) ㊲を回転させることによりローターの高さを調整する。
3) Jig Spacer(0.25 t)を抜く。
4) ㊲にネジロックをする。

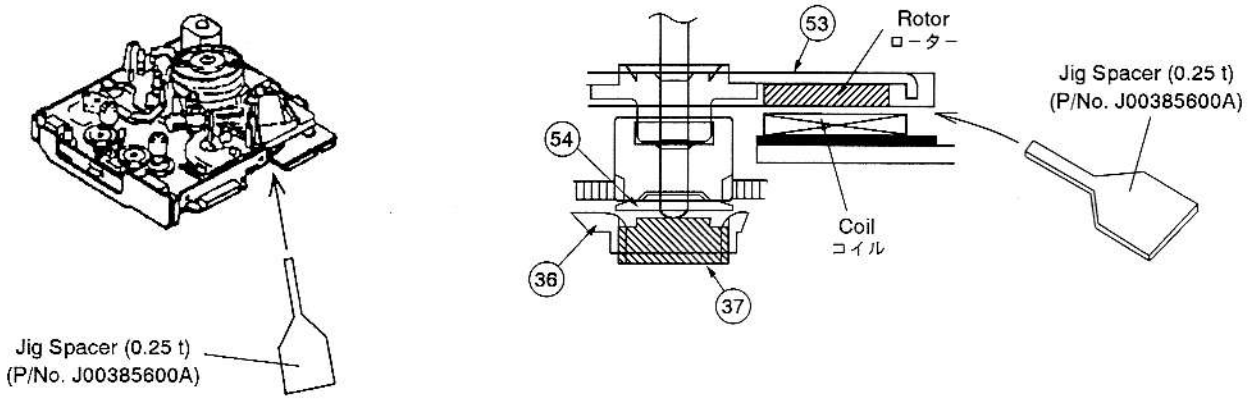


Fig. 2-2

2. ㉟ Sensor Block

1) Desolder the E section (6 positions), F section (8 positions) and G section (5 positions). See Fig. 2-1.
2) Desolder 4 positions to remove the 2-core J line from the ㊼ Loading Gear Block (Fig. 2-1) and the lead wire from the ㊷ Solenoid (Fig. 2-5).
3) Unscrew the two ㉝-c screws.
4) Unscrew the three ㉝-b screws, then remove ㉟.

Note) When soldering during assembly, make sure the J line of ㊼ is aligned in the correct direction.

3. ㉛ ㊹ Push SWs, ㉜ ID Spacer (L), ㉞ ID Spacer (R)

1) Unscrew the two ㉚ screws, then remove ㉛, ㊹, ㉜, and ㉞.

Note) When reinstalling, be careful NOT to tighten the ㉚ screw slantwise (because the switch is mounted obliquely).

4. ⑲-1 TU Ass'y, ⑲-2 TU Ass'y

1) Remove the two ⑱ washers, detach ⑲-1 and ⑲-2.

Note) When reinstalling ⑲-1 and ⑲-2, apply Molicoat to the shaft.

5. ③ BT Arm, ② BT Spring, ⑤ BT Band Ass'y

1) Remove the ①-a washer, then disengage ②.
2) Remove the hook of ⑤ from ③, then detach ③.
3) Remove the ①-b washer and the ④-a screw, then detach ⑤.

Notes) • Pay attention NOT to deform the band of ⑤.
• Refer to item 3-1 for the Back Tension Torque adjustment.

2. ㉟ Sensor Block

1) 図2-1のE部半田付け（6カ所）、F部半田付け（8ケ所）、G部半田付け（5ケ所）を外す。
2) 半田付け4ケ所［㊼ Loading Gear Block (Fig. 2-1) からの2芯J線＋ ㊷ Solenoid (Fig. 2-5) からのリード線］を外す。
3) ㉝-cネジ2本を外す。
4) ㉝-bネジ3本を外し、㉟を外す。

注意) 組立時に半田付けするとき、㊼のJ線の向きに注意すること。

3. ㉛ ㊹ Push SW, ㉜ ID Spacer (L), ㉞ ID Spacer (R)

1) ㉚ネジ2本を外し、㉛, ㊹, ㉜, ㉞を外す。

注意) 取り付けのときは、㉚ネジを斜めに締めつけないこと。(Switchが斜めになるため)

4. ⑲-1 TU Ass'y, ⑲-2 TU Ass'y

1) ⑱ワッシャ2個を外し、⑲-1, ⑲-2を外し、⑳ワッシャ2個を外す。

注意) 取り付けのときは、軸にモリコートを塗布すること。

5. ③ BT Arm, ② BT Spring, ⑤ BT Band Ass'y

1) ①-a ワッシャを外し、②を外す。
2) ⑤のフックを③より外し、③を外す。
3) ①-b ワッシャ、④-aネジを外し、⑤を外す。

注意) • ⑤のBandの変形に注意すること。
• バックテンショントルク調整は3-1項を参照。

6. ⑥⓪ Loading Lever Block

1) Remove the ①-c washer, then remove ⑥⓪.

7. ⑤⓪ Chassis Base Block, ⑤① TG-R Spring, ⑤② TG-R, ④④ Gear Arm, ④⑦ L1 (IN) Arm, ④⑨ L1 (OUT) Arm, ⑤③ Rotor Block, ④⑤ Loading Link Block, ④⓪ INC Base (IN), ④⑧ Loading Link Block, ④① INC Base (OUT)

1) Unscrew the six ④② screws, turn the Mechanism Base Unit upside down, then remove ⑤⓪ with ⑤③ pushed downward.
2) Remove ④④, ④⑦, ④⑨, ⑤②, and ⑤① from ⑤⓪, in this order.
3) Pull out ⑤③ from ⑤⓪
4) Unscrew the two ④⑥ screw, then remove ④⑤, ④⓪, ④⑧, ④① from ⑤⓪.

Notes) • Be careful NOT to scratch the Cylinder.
• See that the phases of ④④, ④⑦, and ④⑨ are matched with each other, as shown in Fig. 2-3.
• For position of the ④③ washers after reinstalling the ⑤③, refer to Fig. 2-4.
Wipe out the oil lubricated to the shaft with an alcohol.

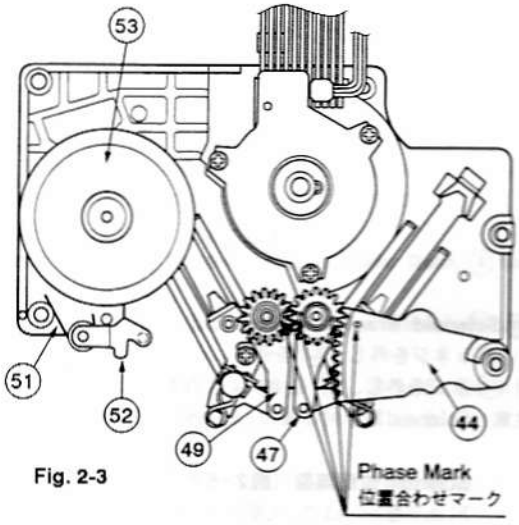


Fig. 2-3

8. ⑤⑧ Loading Belt, ⑤⑦ Loading Gear Block

1) Remove ⑤⑧ from the Mechanism Base Unit.
2) Unscrew the two ③③-d screws, then remove ⑤⑦.

Notes) • Be careful NOT to scratch the gear of ⑤⑦.
• Be careful NOT to let grease adhere to ⑤⑧.

6. ⑥⓪ Loading Lever Block

1) ①-c ワッシャを外し、⑥⓪ を外す。

7. ⑤⓪ Chassis Base Block, ⑤① TG-R Spring, ⑤② TG-R, ④④ Gear Arm, ④⑦ L1 (IN) Arm, ④⑨ L1 (OUT) Arm, ⑤③ Rotor Block, ④⑤ Loading Link Block, ④⓪ INC Base (IN), ④⑧ Loading Link Block, ④① INC Base (OUT)

1) ④② ネジ 6本を外し、メカ・ベース・ユニットを逆さにして、⑤③ を下に押しながら、⑤⓪ を外す。
2) ⑤⓪ から ④④, ④⑦, ④⑨, ⑤②, ⑤① の順に外す。
3) ⑤③ を ⑤⓪ より抜き取る。
4) ④⑥ ネジ2本を外し ④⑤, ④⓪, ④⑧, ④① を ⑤⓪ より外す。

注意) • シリンダに傷等をつけないようにすること。
• ④④, ④⑦, ④⑨ の位相はFig. 2-3を参照。
• ⑤③ 取り付け後の ④③ ワッシャの位置は、Fig. 2-4を参照のこと。また、シャフトのオイルをアルコール等で拭き取ること。

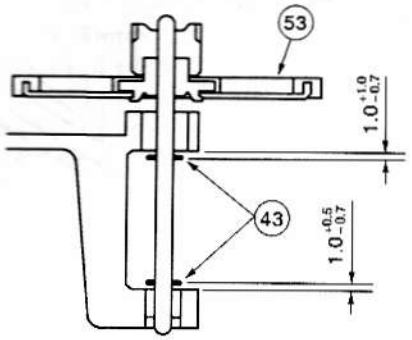


Fig. 2-4

8. ⑤⑧ Loading Belt, ⑤⑦ Loading Gear Block

1) メカ・ベース・ユニットより、⑤⑧ をを外す。
2) ③③-d ネジ 2本を外し、⑤⑦ を外す。

注意) • ⑤⑦ のギアに傷等をつけないようにすること。
• ⑤⑧ にグリス等をつけないようにすること。

2-3. Disassembly of the Mechanism Base Unit-2

2-3. メカニズムベースユニットの分解－2

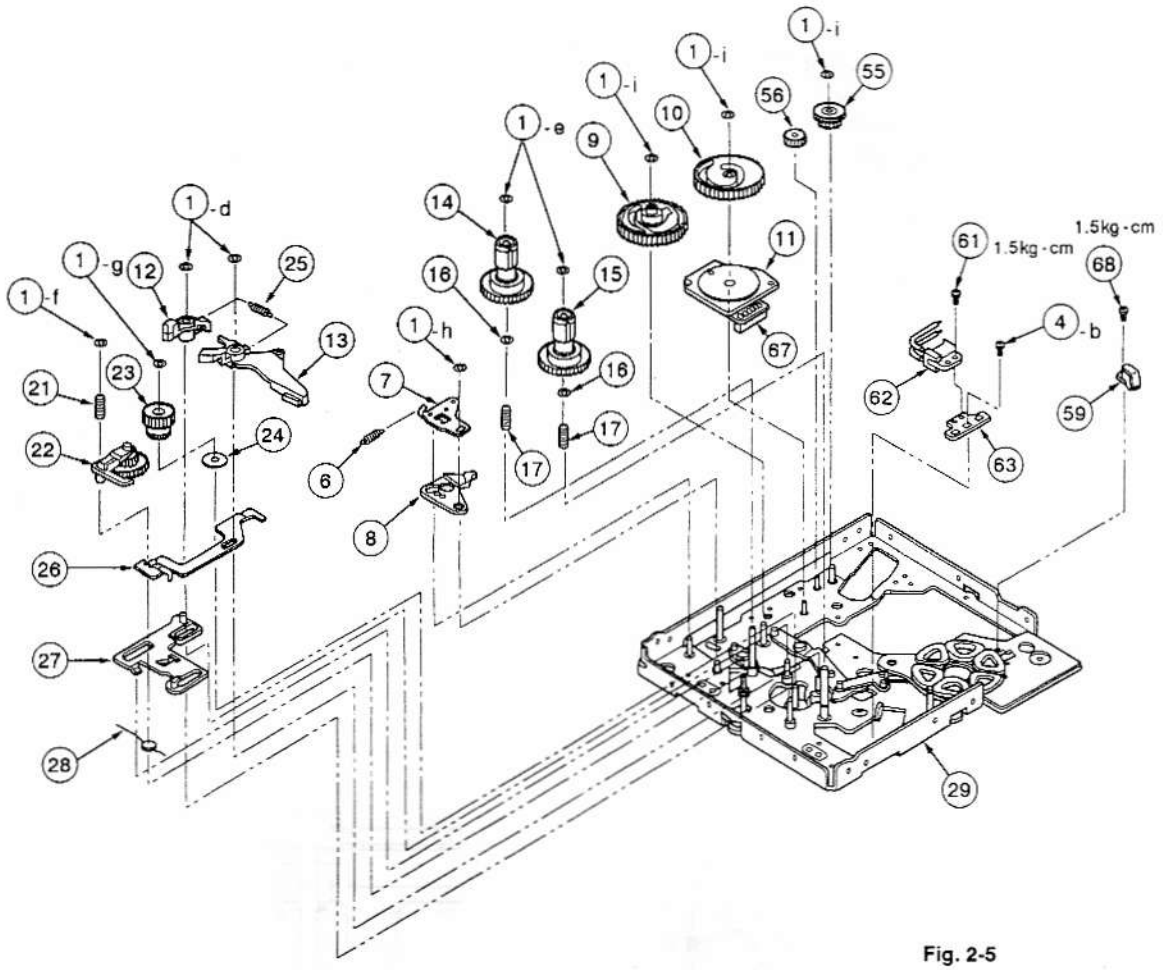


Fig. 2-5

1. ⑥③ Solenoid Bracket, ⑥② Solenoid

1) Unscrew the ④-b screw, then remove ⑥② .
2) Unscrew the ⑥① screw, then remove ⑥③ from ⑥② .

Note) When reinstalling the Solenoid, carry out the adjustment of the position of the Solenoid.

Adjusting the position of the Solenoid
(Refer to Fig. 2-6)

Loosen the ④-b screw, then move the Solenoid (⑥③ , ⑥②) back and forth (↗B) so that no space at "A" portion can be obtained in Play mode. After checking that the brakes are not applied in FF mode, tighten the ④-b screw with a torque of 1.5 kg-cm, then apply the screw-locking compound to it.

1. ⑥③ Solenoid Bracket, ⑥② Solenoid

1) ④-bネジを外し、⑥② を外す。
2) ⑥① ネジを外し、⑥③ を ⑥② より外す。

注意) Solenoid取り付け後は、Solenoidの位置調整を行うこと。

Solenoid位置調整（図2-6参照）

PLAYモードにて、A部の隙間が無い様に ④-bネジを緩めてSolenoid (⑥③ , ⑥②) を前後に動かして（↗B）調整する。またFFモードにてブレーキがかかっていないことを確認し、④-bネジを1.5 kg-cmで締め付けネジ・ロックをする。

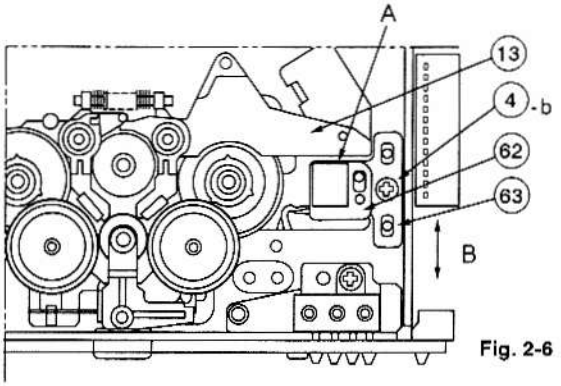


Fig. 2-6

2. ㉕ Brake Spring, ⑬ Loading Lever Block, ⑫ SU Brake Arm

1) Disengage ㉕.
2) Remove the two ①-d washers, then detach ⑬ and ⑫.

3. ⑭ Reel Ass'y(SU), ⑮ Reel Ass'y(TU), ⑰ SU Reel Spring

1) Take off the two ①-e washers, then remove ⑭, ⑮, two ⑰, and two ⑯ washers.

Notes) • Apply Molicoat to the spindle when reinstalling ⑭ and ⑮.
• See that no Molicoat is applied to the reflector plate of ⑭ and ⑮.
• See that the serrated portion of ⑭ and ⑮ is free from Molicoat coating, scratches and indentation.

4. ㉑ Idle Spring, ㉒ Idle Gear, ㉓ Center Pulley, ㉖ Cam Plate, ㉗ Idle Cam, ㉘ Cam Plate Spring, ⑥ BT Lever Spring, ⑦ BT Lever, ⑧ BT Cam Lever

1) Take off the ①-f washer, then remove ㉑ and ㉒.
2) Remove the ①-g washer, then detach ㉓ and ㉔ washer.
3) Disengage ㉘ from the hook, remove ㉖ and ㉗, then take off ㉘.
4) Disengage ⑥.
5) Remove the ①-h washer, then detach ⑦ and ⑧.

Notes) • Apply Molicoat to the spindle when incorporating ㉓.
• When reinstalling ㉖, apply Molicoat to two oblong holes and the spring hook.

5. ㊺ Worm Wheel, ㊻ Center Gear, ⑩ Mode Gear, ⑨ Mode Cam, ⑪ Mode Switch

1) Remove the three ①-i washers, then detach ㊺, ㊻, ⑩, ⑨, and ⑪, in this order.

Notes) • See that the phases of ⑩ and ⑨ when reinstalling are matched with each other, as shown in Fig. 2-7.
• After the phases are matched, move ⑩ in the direction of arrow A by an angle of about 40 degrees.

6. ㊾ MR Sensor

1) Desolder the four soldered portions, unscrew the ④-c screw, then detach ㊾.

2. ㉕ Brake Spring, ⑬ Loading Lever Block, ⑫ SU Brake Arm

1) ㉕ を外す。
2) ①-d ワッシャ 2ヶを外し、⑬, ⑫ を外す。

3. ⑭ Reel Ass'y (SU), ⑮ Reel Ass'y (TU), ⑰ SU Reel Spring

1) ①-e ワッシャ 2ヶを外し、⑭, ⑮, ⑰ 2ヶ、⑯ ワッシャ 2ヶを外す。

注意) • ⑭, ⑮ の組込み時には、軸にモリコートを塗布すること。
• ⑭, ⑮ の反射板にモリコートをつけないこと。
• ⑭, ⑮ の挽目部にモリコート及び傷、打痕をつけないこと。

4. ㉑ Idle Spring, ㉒ Idle Gear, ㉓ Center Pulley, ㉖ Cam Plate, ㉗ Idle Cam, ㉘ Cam Plate Spring, ⑥ BT Lever Spring, ⑦ BT Lever, ⑧ BT Cam Lever

1) ①-f ワッシャを外し、㉑, ㉒ を外す。
2) ①-g ワッシャを外し、㉓, ㉔ ワッシャを外す。
3) ㉘ をフックから外して ㉖, ㉗ を外し、㉘ を外す。
4) ⑥を外す。
5) ①-h ワッシャを外し、⑦, ⑧を外す。

注意) • ㉓ の組込み時には、軸にモリコートを塗布すること。
• ㉖ の組込み時に長穴 (2ヶ所) 及びバネ・フック部にモリコートを塗布すること。

5. ㊺ Worm Wheel, ㊻ Center Gear, ⑩ Mode Gear, ⑨ Mode Cam, ⑪ Mode Switch

1) ①-i ワッシャ 3ヶを外し、㊺, ㊻, ⑩, ⑨, ⑪ の順に外す。

注意) • 組立時の ⑩ と ⑨ との位相は、Fig. 2-7 を参照。
• 位相合わせ後は ⑩ を矢印A方向に約40° 動かしておくこと。

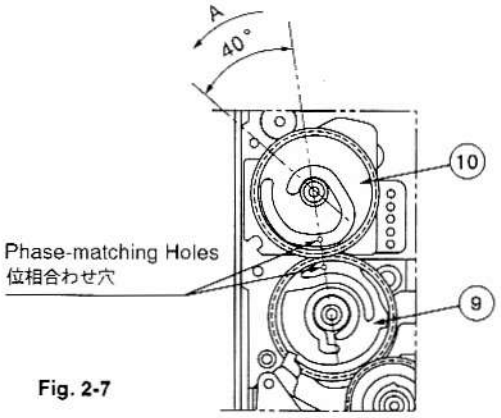


Fig. 2-7

6. ㊾ MR Sensor

1) 半田付け4ヶ所を外し、④-c ネジを外し、㊾ を外す。

2-4. CYL ASSY BLK Replacement

1. Removal (Fig. 2-8)

1) Remove three screws ㊱, and remove part ㉝-1.
2) Dissolve the screw-locking compound at ⓑ with an appropriate solvent, then loosen screw ㉟ with a hexagonal wrench (Fig. 2-9) and remove part ㉝-2.
   Note) Remove part ㉝-2 before the screw-locking compound coagulates again.
   After removing part ㉝-2, clean its bearing with a cotton swab moistened with solvent.
3) Remove three posts ㉞, and remove the CYL ASSY BLK.
   Note) After removing posts ㉞, scratch the screw-locking compound at ⓒ.
   Do NOT use solvent (this will cause trouble if penetrated the motor coil or others).

2. Installation

Install the CYL Head Ass'y in reverse order of disassembly. Remember, however, the following :

* Do NOT touch the surface of the CYL ASSY BLK with naked hands. (It is recommended that you draw on gloves.)
* When mounting part ㉝-2, use a 0.35 mm thick spacer to allow the necessary clearance as shown in Fig. 2-9.
  Position adjustment method is explained on page 18.
* When mounting part ㉝-1, insert a center spacer for the clearance shown in Fig. 2-10 to be even.
* Tightening torque for screws ㊱ and posts ㉞ should be 0.3 kg・cm. You need the following tools :
  ・Torque screwdriver 0.2－1.5 kg (part no. 5772827800)
  ・Attachment bit, crisscross (+) (part no. J0025300)
  ・Attachment bit, flat blade (－) (part no. J0025310)
* When removing the hexagonal wrench after fully tightening screw ㉟, be careful NOT to loosen the screw.
* After completion of installation, slowly rotate the upper drum with your fingers to check that it turns freely and without binding.
* After tightening the screws and posts, apply the screw-locking compound to ⓐ, ⓑ, and ⓒ to prevent them from loosening.

2-4. CYL ASSY BLKの交換

1. 取り外し（図2-8参照）

1) ㊱ ネジ3本を外し ㉝-1を外す。
2) ⓑ 部のネジロックをアルコールで溶かしてから、㉟ ネジをヘックス・レンチ（図2-9）で緩めて ㉝-2を外す。
   注意) ネジロックが固まらないうちに、素早く ㉝-2を外すこと。
   また、㉝-2を外した後は、㉝-2の軸受け内部をアルコールを付けた綿棒できれいにすること。
3) ㉞ ポスト3本を外して、CYL ASSY BLKを外す。
   注意) ㉞ を外した後、ⓒ部のネジロックを削り取ること。尚、アルコールは使用しないこと。（モーターコイル等に流れ込むとトラブルを発生する可能性があるため）

2. 取り付け

取り付けは、取り外しの逆の手順で行うこと。
但し、以下のことに注意すること。

* 作業中、CYL ASSY BLKの表面には触らないこと。（手袋を使用することが望ましい）
* ㉝-2を取り付けるときは、図2-9のように厚さ0.35mmのスペーサーを挿入して、隙間が0.35mmになるように取り付けること。
  また、位置合わせについては18ページ参照のこと。
* ㉝-1を取り付けるときは、図2-10の隙間が均等になるようにセンター・スペーサーを挿入して取り付けること。
* ㊱ ネジおよび ㉞ ポストの締め付けトルクは0.3kg・cm厳守のこと。
  ・トルクドライバー 0.2～1.5kg：品番5772827800
  ・トルクドライバー用ビット（+）：品番J0025300
  ・トルクドライバー用ビット（－）：品番J0025310
* ㉟ ネジの締め付け後、ヘックス・レンチを抜くときは、絶対にネジが緩む方向に力を加えないこと。
* 取り付け後、上ドラムを指でゆっくり回転させ、スレ等の異常がないかを確認する。
* 各ネジおよびポストを締め付け後は、ⓐ, ⓑ, ⓒ部をネジロックで固定すること。

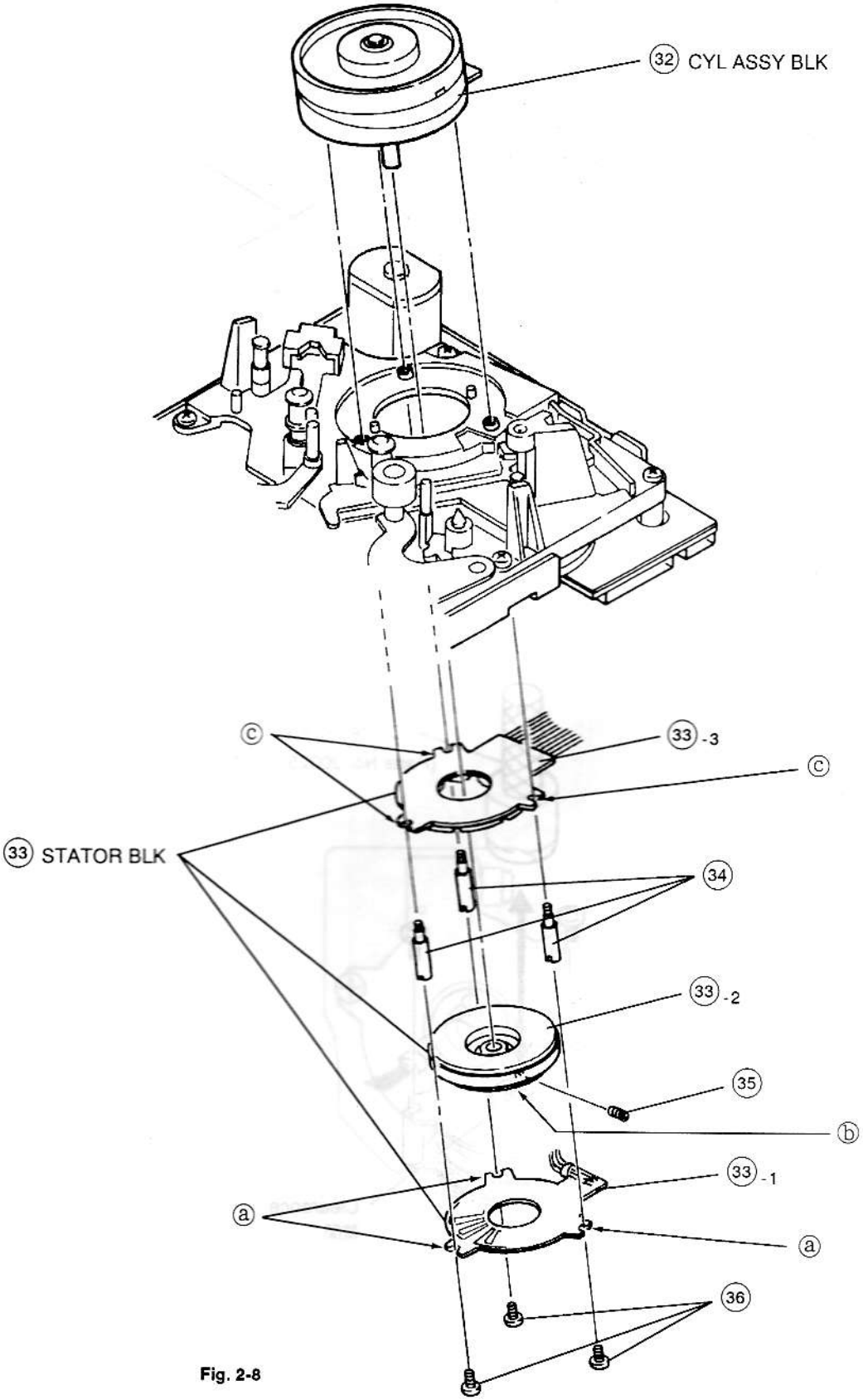


Fig. 2-8

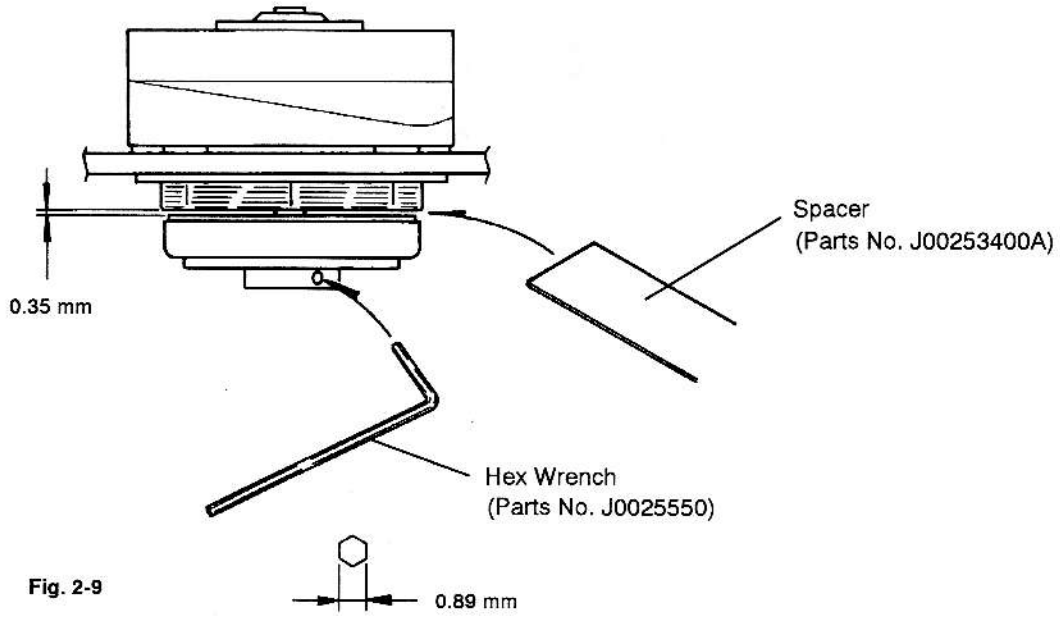


Fig. 2-9

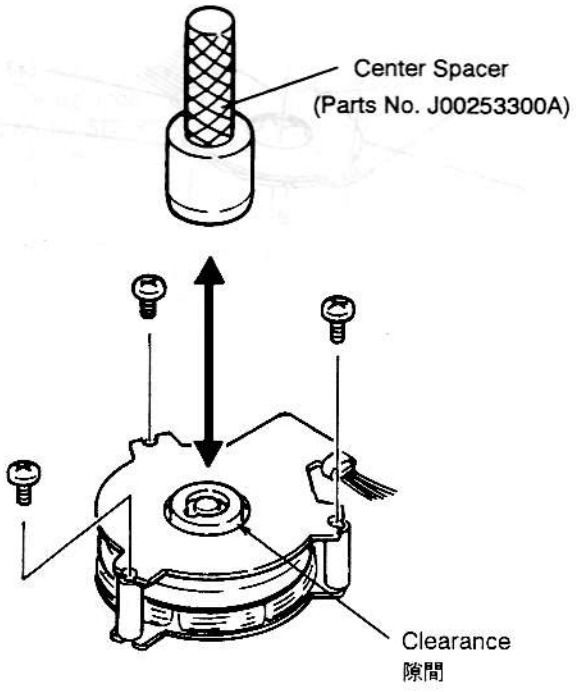


Fig. 2-10

Position adjustment

Using the diagrams below as a guide, match part ⑲ and the shaft. The Figure 2-11 shows the alignment when viewing the mechanism assembly from above and the Figure 2-12 shows the alignment viewed from below.

位置合わせ

メカAss'yを上から見たときに図2-11の位置に、下側から見たときに図2-12の位置になるように取り付けてください。

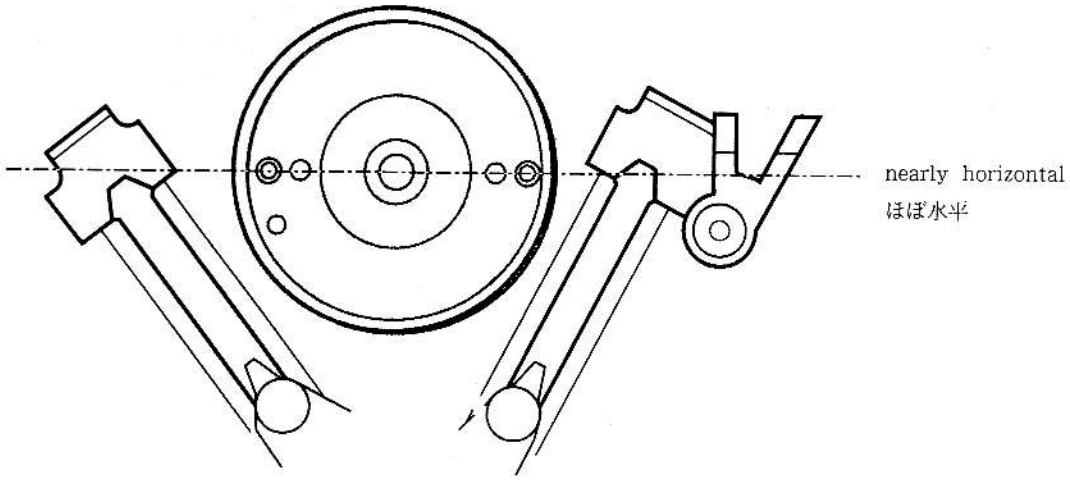


Fig. 2-11

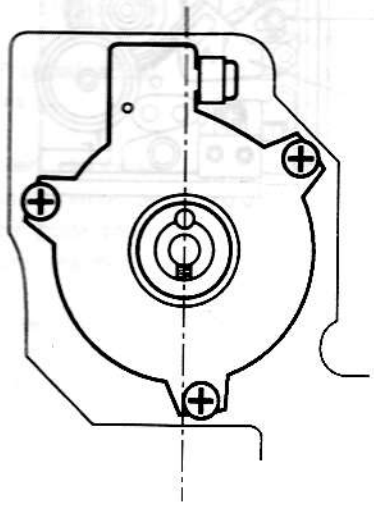


Fig. 2-12

3. ADJUSTMENT OF THE MECHANISM
機構部調整

This adjustment is performed when mechanical parts have been replaced or when torque value or tape travel is erratic.

この調整は、機構部品を交換したときまたは又はトルク値、テープの走りが悪い場合に行って下さい。

3-1. Back Tension Torque Adjustment

1. Load a torque measurement tape (TW-7131 manufactured by SONY), then measure the back tension torque with the deck in REC/PLAY mode.
2. So that the center value of the back tension torque swing falls within a range of 5 to 7 g・cm, adjust by loosening the ④ screw in Fig. 3-1 then by moving the ⑤ BT Band Assy to the right and left as shown in A of Fig. 3-1.
3. After adjusting, tighten the ④ screw with a torque of 0.8 kg・cm, then apply the screw-locking compound to it.

3-1. バックテンショントルク調整

1. トルク測定用テープ（SONY製 TW-7131）を装着し、REC/PLAYモードにてバックテンショントルクを測定する。
2. バックテンショントルク値の振れ幅の中心が5 ～7 g・cmとなるように、Fig. 3-1の④ネジをゆるめて⑤BT Band AssyをFig. 3-1のAの様に左右に動かして、調整する。
3. 調整後、④ネジを0.8kg・cmで締め付けてネジロックをする。

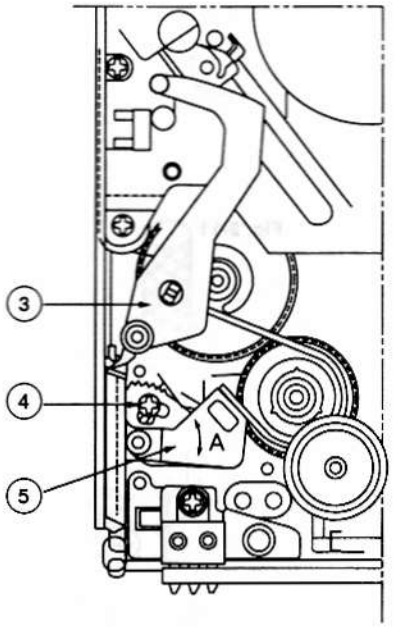


Fig. 3-1

3-2. Tape Travel Adjustment

Prior to adjustment, clean dirt and dust off all posts and the head drum other than the guide roller, using a cotton swab moistened with Diflon.
Gently wipe the guide roller with a cotton swab moistened with alcohol.

3-2. テープ走行調整

調整の前にガイドローラー以外の各走行ポスト及びシリンダーの汚れを、ダイフロンを綿棒に浸し拭きとって下さい。
尚、ガイドローラーはアルコールを綿棒に浸し、軽く拭きとってください。

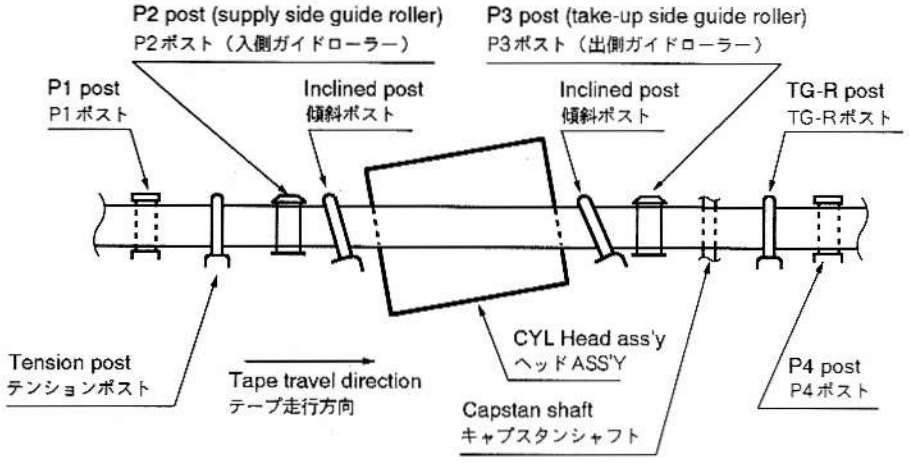


Fig. 3-2

1. Set the servo adjustment menu 4 (CHK TapePass). (Refer to page 23.)
2. Load a tracking test tape (**TY-7251** manufactured by SONY), then set the deck to PLAY mode.
3. Connect CH1 of the oscilloscope to **TP435 (PBRF)** on the **MAIN PCB** and CH2 to **TP403 (SWP)**.
   While observing the envelope of the RF signal, adjust the height of the guide roller as follows :
   1) Turn the **P2 post (supply side guide roller)** clockwise using a wrench until the margin area on the envelope (supply side) disappears, then turn the guide roller counterclockwise until the margin area reappears. (Refer to Fig. 3-3)
   2) Turn the **P3 post (take-up side guide roller)** clockwise using a wrench until the margin area on the envelope (take-up side) disappears, then turn the guide roller counterclockwise until the margin area reappears. (Refer to Fig. 3-4)

1. サーボ調整メニュー4（CHK TapePass）にする。
（☞23ページ）
2. トラッキング・テープ（SONY製TY-7251）を装着し、PLAYモードにする。
3. オシロスコープのCH1をMAIN PCBのTP435 (PBRF)に、CH2をTP403 (SWP)に接続し、RF信号のエンベロープを観測しながら、以下のようにガイドローラーの高さを調整する。
   1) P2ポスト（入側ガイドローラー）を二股レンチにて右に回し、エンベロープの入側のマージン・エリア部が無くなるまで下げ、今度はガイドローラーを左に回し、マージン・エリア部が出るまで戻す。（Fig. 3-3参照）
   2) P3ポスト（出側ガイドローラー）を二股レンチにて右に回し、エンベロープの出側のマージン・エリア部が無くなるまで下げ、今度はガイドローラーを左に回し、マージン・エリア部が出るまで戻す。（Fig. 3-4参照）

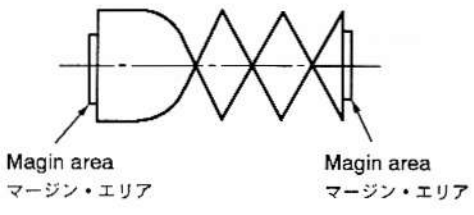


Fig. 3-3

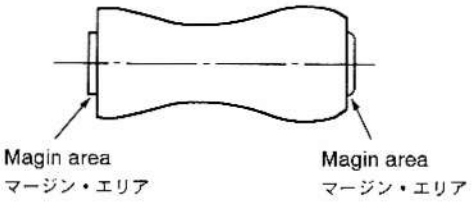


Fig. 3-4

3) Gently turn the guide rollers on both sides until the envelope becomes as shown in Fig. 3-5.
   At this time, the lower edge of the tape should be completely on the drum lead.
4) Gently turn the guide rollers on both sides counterclockwise until the envelope becomes as shown in Fig. 3-6.
   Reference) The shape of the envelope when the tape is running outside the drum lead is shown in Fig. 3-7.

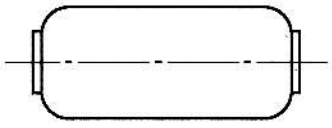


Fig. 3-5

3) 両側のガイドローラーを少しずつ調整して、エンベロープをFig. 3-5 のような形状にする。
   このとき、テープの下エッジがドラムのリードに完全に乗っている状態になります。
4) 両側のガイドローラーを互いに少しずつ左側に回し、エンベロープをFig. 3-6 のような形状にする。
   参考) テープがドラムのリードから外れて走行している場合のエンベロープの形状は、Fig. 3-7のようになります。

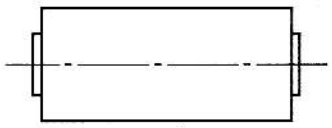


Fig. 3-6

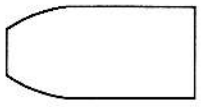
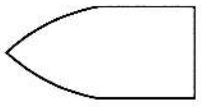
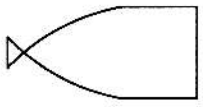
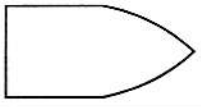
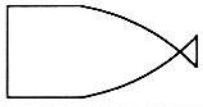
	Small deviation 外れ量 小	Medium deviation 外れ量 中	Large deviation 外れ量 大
Input side 入側			
Output side 出側			

Fig. 3-7

5) After the adjustment is complete, eject the tape, then load it again and confirm whether or not the envelope is as shown in Fig. 3-6. If NOT, go back to 1), and perform the adjustment again.
6) After the adjustment is complete, check to make sure that the tape is NOT curled around the guide rollers.

5) 調整後、一度テープをEJECTし、再度ローディングを行ないエンベロープがFig. 3-6のような形状になっているかを確認する。なっていない場合には、再度 1)項に戻って調整する。
6) 調整終了後、ガイドローラーでテープがカールしていないことを確認する。

4. ELECTRICAL ADJUSTMENT
電気系調整

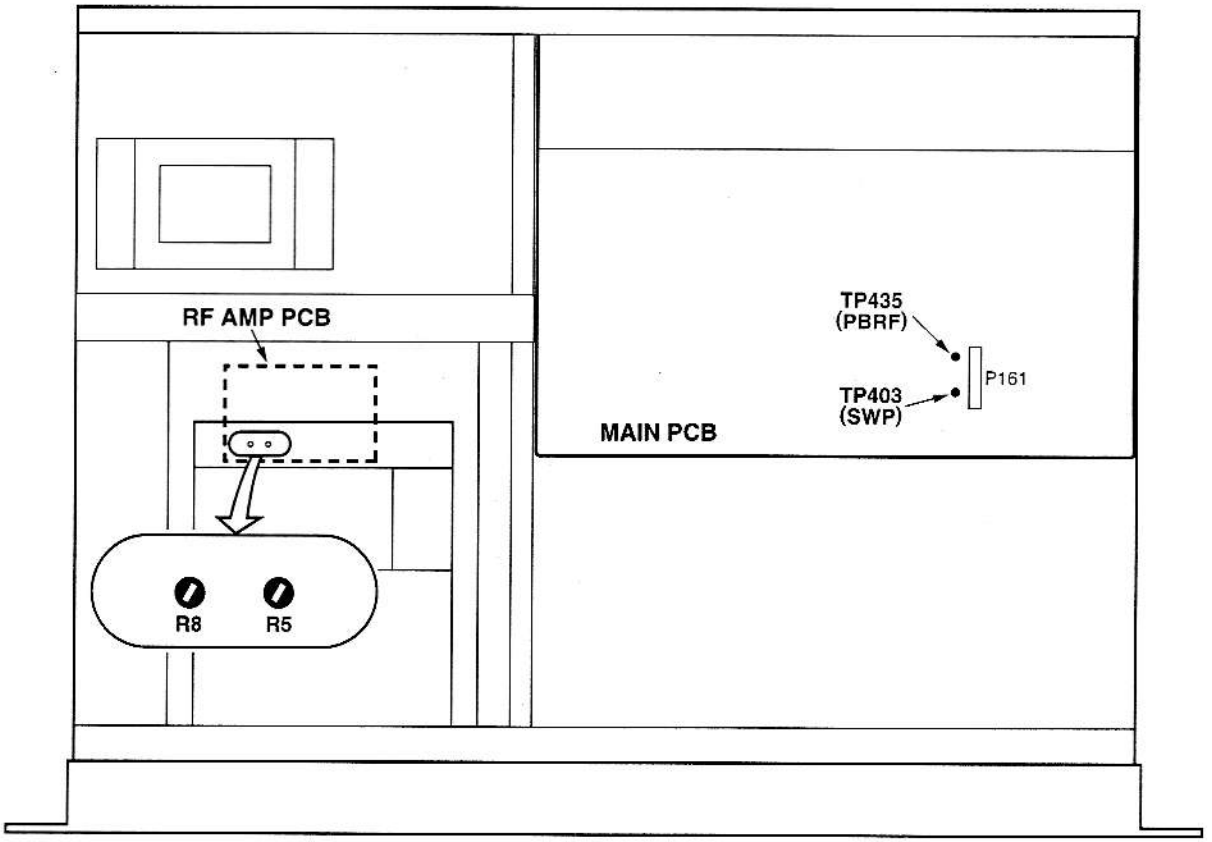


Fig. 4-1 Adjustment and test poins
調整箇所およびテストポイント

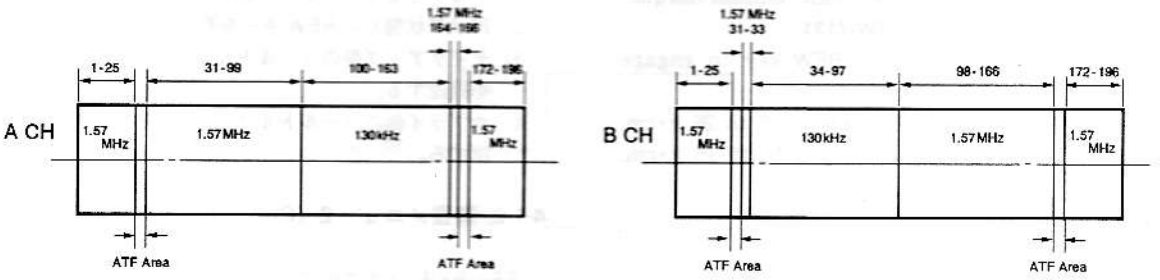


Fig. 4-2 Frequency patterns of the level checking test tape (TY-7111)
レベル用テープ（TY-7111）周波数パターン

● **Test tape**

Torque cassette	:	TW-7131 manufactured by SONY TW-7231A manufactured by SONY
Tracking tape	:	TY-7251 manufactured by SONY
Level tape	:	TY-7111 (TY-7111X) manufactured by SONY (Refer to Fig. 4-2)
Function tape	:	TY-7551 manufactured by SONY
Blank tape	:	TY-30B (TW-30BX) manufactured by SONY

Note) When using the new type TY-7111X level test tape, use the new type TY-30BX blank tape for recording as well.

4-1. Servo adjustment menu

Adjust the servo system using the servo adjustment menu mode.

1. Activating the adjustment mode
   1) Press the SHIFT key to ON.
   2) While pressing the STOP key, press the MARGIN RESET key and MENU key simultaneously. In this case, "FactoryCHK" is shown on the display.
2. Selecting an adjustment menu
   Select the desired adjustment menu with the MENU key. The selected menu is shown on the display.
3. Ending the adjustment mode
   Press the SHIFT key to OFF and then press the COUNTER MODE key.

4-1-1. Adjustment menu 1 (CHK PB Torque)

1. Check the PLAY take-up torque/back tension torque.
   1) Play back the torque cassette (TW-7131).
   2) Check that the take-up reel torque is 7 to 20 g•cm.
   3) Check that the supply reel torque is 4 to 8 g•cm.
2. Check the REV take-up torque/back tension torque.
   1) Load the torque cassette (TW-7131).
   2) In the PLAY mode, press the REW key to engage the REV PLAY mode.
   3) Check that the take-up reel torque is 10 to 26 g•cm.
   4) Check that the supply reel torque is 10 to 16 g•cm.

4-1-2. Adjustment menu 2 (CHK FF Torque)

1. Check the FF/REW torque.
   1) Load the torque cassette (TW-7231A).
   2) Check that the take-up reel torque is 40 g•cm or more in the FF and REW modes.

● **テストテープ**

トルクカセット	:	TW-7131 (SONY製) TW-7231A (SONY製)
トラッキングテープ	:	TY-7251 (SONY製)
レベルテープ	:	TY-7111 (TY-7111X) (SONY製) (図4-2参照)
ファンクションテープ	:	TY-7551 (SONY製)
ブランクテープ	:	TY-30B (TY-30BX) (SONY製)

注) レベルテープが新タイプのTY-7111Xの場合は、ブランクテープも新タイプのTY-30BXを使用してください。

4-1. サーボ調整用メニューモード

サーボ系の調整は、サーボ調整用メニューモードにして行います。

1. 調整モードの起動
   1) SHIFTキーを押してONにする。
   2) STOPキーを押しながら、MARGIN RESETキーとMENUキーを同時に押す。
      このとき、ディスプレイに"FactoryCHK"と表示される。
2. 各調整メニューの選択
   MENUキーにより選択する。
   選択内容は、ディスプレイに表示される。
3. 調整モードの終了
   SHIFTキーを押してOFFさせた後、COUNTER MODEキーを押す。

4-1-1. 調整メニュー1 (CHK PB Torque)

1. PLAY テイクアップトルク/バックテンショントルク確認
   1) トルクカセット (TW-7131) をPLAYする。
   2) テイクアップ側のリールトルクが7～20g・cmであることを確認する。
   3) サプライ側のリールトルクが4～8g・cmであることを確認する。
2. REV テイクアップトルク/バックテンショントルク確認
   1) トルクカセット (TW-7131) を装着する。
   2) PLAY状態からREWキーを押して、REV PLAYにする。
   3) テイクアップ側のリールトルクが10～26g・cmであることを確認する。
   4) サプライ側のリールトルクが10～16g・cmであることを確認する。

4-1-2. 調整メニュー2 (CHK FF Torque)

1. FF/REW トルク確認
   1) トルクカセット (TW-7231A) を装着する。
   2) FFおよびREWモードにおいて、テイクアップ側のリールトルクが40g・cm以上であることを確認する。

4-1-3. Adjustment menu 3 (DPGadj XXXX)

1. DPG adjustment
   1) Connect the oscilloscope's CH1 to the MAIN PCB's TP435 (PBRF) and CH2 to TP403 (SWP).
   2) Play back the tracking tape (TY-7251).
   3) Press the CHAR key to show "1700".
   4) Adjust DPG with the INS/+ key and DEL/− key so that the time between the SWP signal (TP403) fall and the RF signal (TP435) marker is 650 ± 15 μs. (Refer to Fig. 4-3)
   5) Press the MEMO 1 key to store this setting in memory.

4-1-3. 調整メニュー3 (DPGadj XXXX)

1. DPG調整
   1) オシロスコープのCH1をMAIN PCBのTP435 (PBRF) にCH2をTP403 (SWP) に接続する。
   2) トラッキングテープ (TY-7251) を再生する。
   3) CHARキーを押し、"1700" を表示させる。
   4) SWP信号 (TP403) の立ち下がりからRF信号 (TP435) のマーカーまでの時間が650 ± 15 μsになるように、INS/+キー、DEL/−キーで調整する。
   (図4-3参照)
   5) MEMO 1キーを押して、メモリーに記憶させる。

Oscilloscope Range :
CH1 : AC 200 mV/div., 0.1ms/div.
CH2 : DC 5V/div.

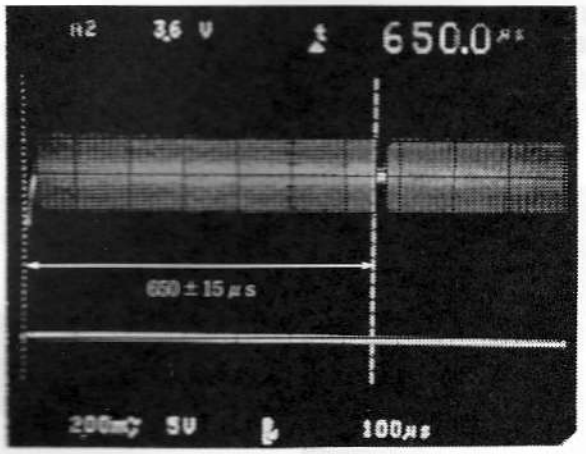


Fig. 4-3

4-1-4. Adjustment menu 4 (CHK TapePass)

1. Check the tape pass
   1) Connect CH1 of the oscilloscope to the TP435 (PBRF) on the MAIN PCB and CH2 to the TP403 (SWP).
   2) Play back the tracking tape (TY-7251).
   3) Check that the flatness of the RF waveform is 75% or more as shown in Fig. 4-4.

4-1-4. 調整メニュー4 (CHK TapePass)

1. テープパス確認
   1) オシロスコープのCH1をMAIN PCBのTP435 (PBRF) にCH2をTP403 (SWP) に接続する。
   2) トラッキングテープ (TY-7251) を再生する。
   3) 図4-4のように、RF波形の平坦度が75%以上あることを確認する。

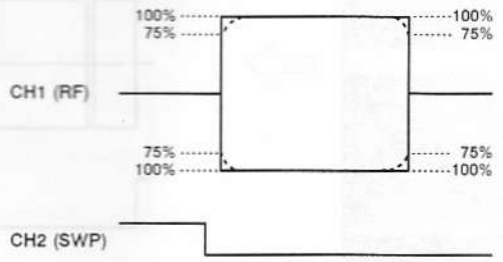


Fig. 4-4

4-1-5. Recording current adjustment (TestRec f/6)

1. Set the INPUT switch to ANALOG.
2. Connect the oscilloscope's CH1 to the MAIN PCB's TP435 (PBRF) and CH2 to TP403 (SWP).
3. Play back the level tape (TY-7111).
4. Write down the signal level of the pilot signal (130 kHz) for the A head and B head as shown in Fig. 4-5.
5. Load a blank tape (TY-30B) and record no signal.
6. When the section recorded in step 5 is played back, make sure that the signal level of the pilot signal (130 kHz) is within ±2 dB (0.8 to 1.25 times) against the level written in step 4.
7. When the level is out of standard, adjust the RF AMP PCB's R8 (A ch) and R5 (B ch), then repeat steps 5 and 6.

4-1-5. 記録電流調整（TestRec f/6）

1. INPUTスイッチをANALOGにする。
2. オシロスコープのCH1をMAIN PCBのTP435（PBRF）にCH2をTP403（SWP）に接続する。
3. レベルテープ（TY-7111）を再生する。
4. 図4-5のように、A head、B headのパイロット信号（130kHz）の信号レベルを記録（メモ）しておく。
5. 記録用ブランクテープ（TY-30B）を装着し、未使用部分に無信号録音をする。
6. ステップ5で記録した部分を再生したとき、パイロット信号（130kHz）の信号レベルがステップ4で記録（メモ）したレベルに対して±2dB以内（0.8～1.25倍）であることを確認する。
7. 規格に入らない場合は、RF AMP PCBのR8（A ch）, R5（B ch）を調整後、ステップ5、6を行う。

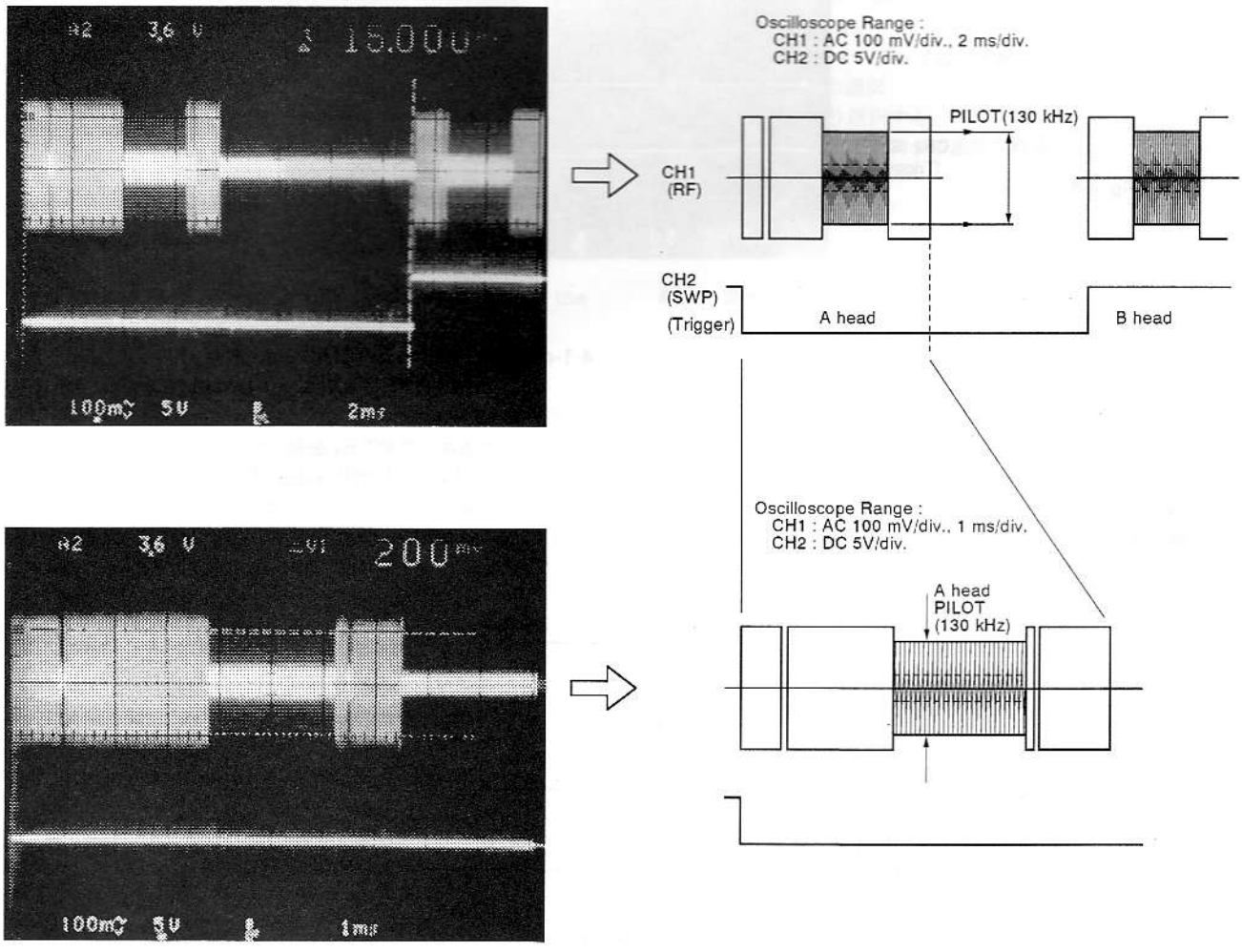


Fig. 4-5

4-2. Error rate check

1. Self-recording/playback error rate (LP mode)
   1) Load a blank tape for recording (**TY-30B**).
   2) Press the **DISPLAY** key several times to engage the error rate display mode (display : **E** – – – –).
   3) Set the **RECORD MODE** switch to **LONG**.
   4) Set Fs to 44.1 kHz to record no signal on the blank tape.
   5) When the recorded section is played back, make sure that the error rate of the A head and B head is below 9×10^{-3} (display : **0090**).
      (Switching between the A head and B head is performed with the **MENU** key.)
2. Self-recording/playback error rate (SP mode)
   1) Load a blank tape for recording (**TY-30B**).
   2) Set the **RECORD MODE** switch to **STANDARD**.
   3) Set Fs to 44.1 kHz to record no signal on the blank tape.
   4) When the recorded section is played back, make sure that the error rate is below 6×10^{-3} (display : **0060**).

4-2. エラーレート確認

1. 自己録再エラーレート（LPモード）
   1) 記録用ブランクテープ（**TY-30B**）を装着する。
   2) **DISPLAY**キーを何度か押して、エラーレート表示モードにする。（表示：**E** – – – –）
   3) **RECORD MODE**スイッチを**LONG**にする。
   4) Fsを**44.1kHz**にし、未使用部分に無信号録音をする。
   5) 記録した部分を再生したときのAヘッド、Bヘッドのエラーレートが9×10^{-3}（表示：**0090**）以下であることを確認する。
      （Aヘッド、Bヘッドの切り換えは、**MENU**キーにより行う）
2. 自己録再エラーレート（SPモード）
   1) 記録用ブランクテープ（**TY-30B**）を装着する。
   2) **RECORD MODE**スイッチを**STANDARD**にする。
   3) Fsを**44.1kHz**にし、未使用部分に無信号録音をする。
   4) 記録した部分を再生したときのエラーレートが6×10^{-3}（表示：**0060**）以下であることを確認する。

5. AUDIO CHECK
オーディオ部確認

5-1. Playback System　再生系

Mode : PLAY
Test Tape : TY-7551
XLR VR : MAX
Measurement Points : LINE OUT

CHECK ITEM 確認項目	PLAYBACK SIGNAL 再生信号	SPECIFICATIONS 規格値	REMARKS 備考
1. Playback output level 再生出力レベル	PGM NO."1" 1kHz, 0dB	UNBAL :　+6dBV ± 2dB BAL :　+20dBu ± 2dB	
2. Playback frequency response 再生周波数特性	PGM NO."1"　1kHz PGM NO."2"　20Hz PGM NO."5"　20kHz	20Hz～20kHz ± 1.0dB	
3. Playback distortion factor 再生歪率	PGM NO."1" 1kHz, 0dB	UNBAL, BAL : 0.006 % or less	400Hz HPF : IN 22kHz LPF : IN
4. Playback S/N ratio 再生S/N	PGM NO."1" 1kHz, 0dB PGM NO."6" -∞	Using PGM NO."1" (0dB) as a reference, when PGM NO."6" (-∞) is played, the S/N ratio should be 95 dB or more. PGM NO."1" (0dB) を基準にし、PGM NO."6" (-∞) を再生したときのS/N値は95dB以上であること。	22kHz LPF : IN IEC-A : IN
5. Playback crosstalk 再生クロストーク	PGM NO."8" 10kHz, L PGM NO."10" 10kHz, R	When PGM NO."8" (10kHz, L) to R and PGM NO."10" (10kHz, R) to L are played back, the crosstalk with respect to the play nominal output should be 80 dB or more. 再生基準出力に対して、 PGM NO."8" (10kHz, L) →R PGM NO."10" (10kHz, R) →L を再生したときのクロストークは80dB以上であること。	22kHz LPF : IN IEC-A : IN

5-2. Recording System 録音系

Mode : Input Monitor
Measurement Points : UNBAL OUT

CHECK ITEM 確認項目	INPUT SIGNAL 入力信号	SPECIFICATIONS 規格値	REMARKS 備考
1. Recording input/ output level 録音入出力レベル	BAL : 1kHz, + 20dBu UNBAL : 1kHz, +6dBV	Turn the INPUT control, and set the level at which the OVER indicator of the level meter almost lights. The output level at this point should be + 6 dBV ± 2 dB. INPUTつまみを回し、レベルメーターのOVERインジケーターが点灯直前になるようにセットする。このときの出力レベルは、+ 6dBV ± 2dBであること。	INPUT switch : BAL, UNBAL RECORD MODE switch : STANDARD
2. Recording frequency response 録音周波数特性	UNBAL : 20Hz～20kHz, +6dBV	With the deck in the condition of step 1, when the input signal varies from 20 Hz to 20 kHz, the recording frequency response with respect to the 1 kHz output level should be as follows : 20 Hz to 20 kHz ± 1.0 dB ステップ1の状態で、入力信号の周波数を変化させたとき、1kHzの出力レベルに対しての録音周波数特性は以下の通りであること。 20Hz～20kHz ± 1.0dB	
3. Recording S/N ratio 録音S/N	No input 無入力	The S/N ratio with respect to the output level in step 1 should be 88 dB or more. ステップ1の出力レベルに対してのS/N値は88dB以上であること。	22kHz LPF : IN IEC-A : IN
4. Recording crosstalk 録音クロストーク	UNBAL : 1kHz, +6dBV	When the deck is in the condition of step 1, the ratio between the output when a signal is input to one channel and the output at the other channel should be 80 dB or more. ステップ1の状態で、入力信号を片チャンネルに加えたときの出力に対して、もう片チャンネルの出力との比は80dB以上であること。	22kHz LPF : IN IEC-A : IN
5. Recording distortion factor 録音歪率	UNBAL : 1kHz, +6dBV	0.008 % or less	400Hz HPF : IN 22kHz LPF : IN
6. Headphone output level ヘッドホン出力レベル	UNBAL : 1kHz, +6dBV	With the deck is in the condition of step 1, turn the PHONES control all the way to its maximum position and check for 1.2 V or more at PHONES OUT under 32 Ω load. ステップ1の状態で、PHONESつまみを最大にしたときのPHONES OUTの出力レベルは1.2V以上（32Ω負荷）であること。	

6. SPECIFICATIONS

仕様

Audio specifications

Tape speed : 8.15 mm/s (SP mode)
4.075 mm/s (LP mode)
Recording time (with 120-minute tape) :
120 minutes (SP mode)
240 minutes (LP mode)
Head drum speed : 2,000 rpm (SP mode)
1,000 rpm (LP mode)
Fast winding time : 60 seconds with 120-minute tape
Sampling frequency : 44.1 kHz, 48 kHz
32 kHz (LP mode)
Recording resolution : 16-bit linear (SP mode)
12-bit non-linear (LP mode)
Frequency response :
20 Hz to 20 kHz, ± 0.5 dB (SP mode)
20 Hz to 14.5 kHz, ± 0.5 dB (LP mode)
S/N ratio : More than 92 dB
Dynamic range : More than 93 dB
Total harmonic distortion (1 kHz @ FS – 0.1 dB) :
Less than 0.005 % (SP mode)
Less than 0.075 % (LP mode)
Channel separation : More than 90 dB (1 kHz @ FS))
Wow and flutter : Unmeasurable (less than 0.001 %)

I/O specifications

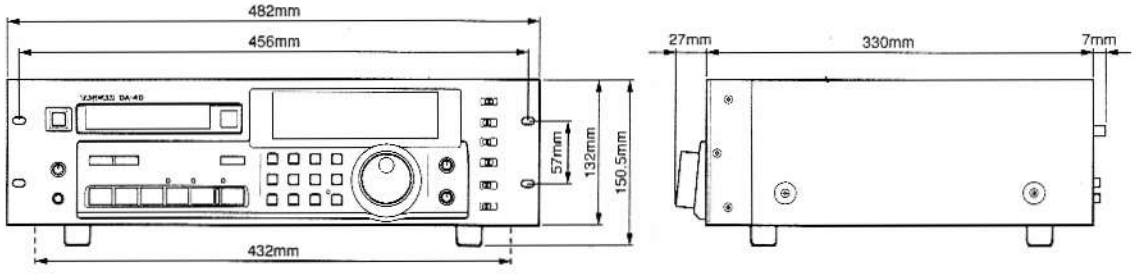
Analog inputs (balanced XLR-3-31 type) :
Nominal input level : + 4 dBu (FS – 16 dB)
Maximum input level : + 20 dBu
Input impedance : More than 10 k Ω
Analog inputs (unbalanced RCA) :
Nominal input level : – 10 dBV
Maximum input level : + 6 dBV (2 Vrms)
Input impedance : More than 50 k Ω
Analog outputs (balanced XLR-3-32 type) :
Nominal output level : + 4 dBu (FS – 16 dB)
Maximum output level : + 20 dBu
Output impedance : Less than 100 Ω
Analog outputs (unbalanced RCA) :
Nominal output level : – 10 dBV
Maximum output level : + 6 dBV (2 Vrms)
Output impedance : Less than 1 k Ω
Headphone 1/4" stereo jack : 2 × 50 mW into 32 Ω
Digital input AES/EBU (balanced XLR-3-31 type) :
AES3-1992 or IEC60958 Type II (auto-detect)
Digital input COAXIAL (unbalanced RCA) :
IEC60958 Type I or Type II (auto-detect)
Digital output AES/EBU (balanced XLR-3-31 type) :
AES3-1992 or IEC60958 Type II (menu-selectable)
Digital output COAXIAL (unbalanced RCA) :
IEC60958 Type I or Type II (menu-selectable)
Parallel I/O port : 15-pin, D-sub connector
REMOTE IN (3.5 mm mini-jack) :
For use with RC-D45 only

Physical specifications

Voltage requirements :
USA/Canada : 120 VAC, 60 Hz
Europe/UK : 230 VAC, 50 Hz
Australia : 240 VAC, 50 Hz
Japan : 100 VAC, 50-60 Hz
Power Consumption : 21 W
Dimensions (W x H x D) : 482 × 150.5 × 364 mm
(19 × 5.9 × 14.3 inch)
Weight : 8 kg (17.6 lbs)

* In these specifications, 0 dBV is referenced to 1.0 Vrms, and 0 dBu is referenced to 0.775 Vrms.
* Changes in specifications and features may be made without notice or obligation.

* 0 dBV = 1.0Vrms、0 dBu = 0.775Vrmsで表記しています。
* 仕様・外観などは、予告なく変更することがあります。



PARTS LIST SECTION

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with ＊ require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in this manual.
- ⚠ Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J]:JAPAN [US/C]:U. S. A. /CANADA [E]:EUROPE [K]:KOREA
  [UK]:U. K. [A]:AUSTRALIA

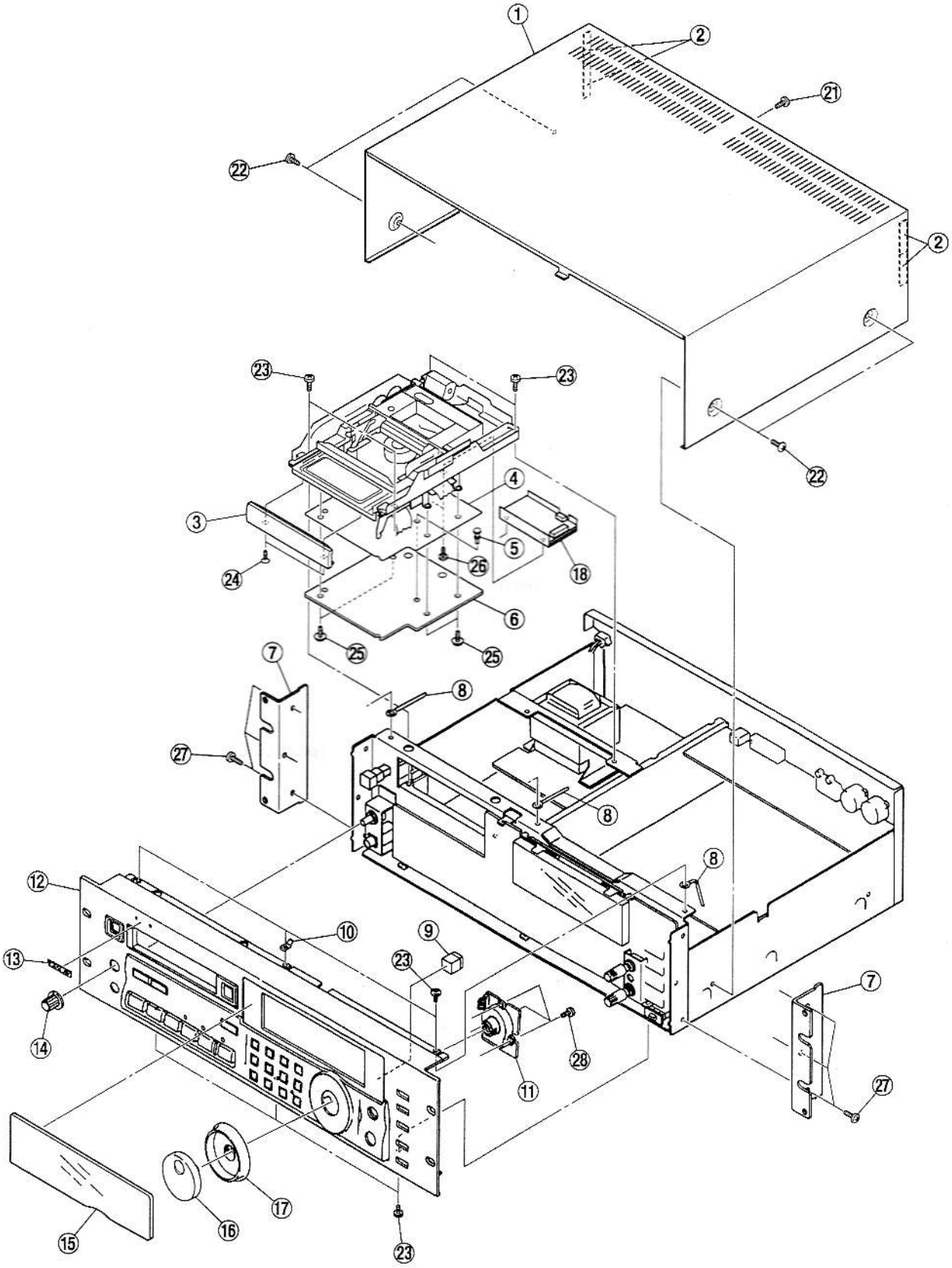
注　意

- プリント基板図は部品面が示されています。
- ＊印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品及び品番のない部品は供給しません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠印は安全重要部品です。
  交換する時は必ずティアック指定の部品を使用してください。
- 仕向先
  [J]:JAPAN [US/C]:U. S. A. /CANADA [E]:EUROPE [K]:KOREA
  [UK]:U. K. [A]:AUSTRALIA

7. EXPLODED VIEWS AND PARTS LIST

分解図とパーツリスト

EXPLODED VIEW-1



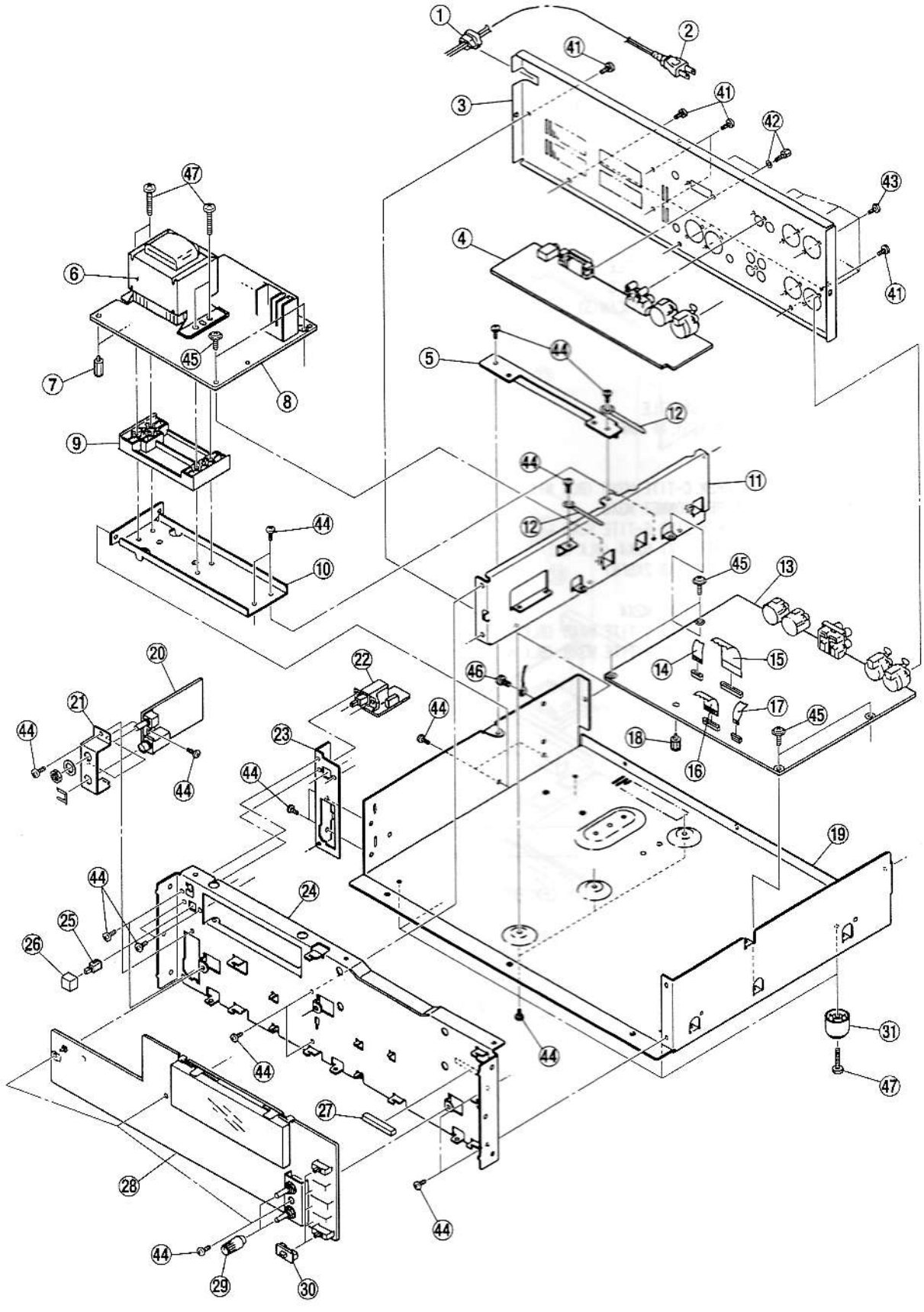
EXPLODED VIEW-1

REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	*5801350900	BONNET (B)	
1- 2	*5555570000	CUSHION B, BONNET	
1- 3	*M00000500A	COVER, TRAY B	
1- 4	*M00789700B	SHIELD SHEET, SERVO	
1- 5	*5786610200	RIVET, PUSH RP-3045-NB	
1- 6	*E95073501A	PCB ASSY, SERVO	
1- 7	*5801348702	ANGLE	
1- 8	*5786713000	CLIP, HARNESS 3.0X9.1X50	
1- 9	*M00844900A	SPACER, FRONT B	
1-10	*M00549800A	PLATE, EARTH	
1-11	*E95077100A	PCB ASSY, SHUTTLE	
1-12	*M00757801A	FRONT PNL ASSY, B	
1-13	*5720254101	NAME PLATE, TASCAM(S)	
1-14	M00002503A	KNOB, GB	
1-15	*M00758600B	WINDOW, FL	
1-16	M00757500A	KNOB, JOG	
1-17	M00757600A	KNOB, SHUTTLE	
1-18	*E95074501A	PCB ASSY, RF AMP	
1-21	*5783613008	SCREW, C-TITE M3X8 (BLK NI)	
1-22	*5800612400	SCREW, BONNET M3X8	
1-23	*5783033006	SCREW, BIND S-TITE M3X6	
1-24	*5780222004	SCREW, FLAT M2X4 (BLK NI)	
1-25	*B0005020	SCREW, PPAB 2X5FNI	
1-26	*5780002004	SCREW, BIND M2X4	
1-27	*5783804008	SCREW, BIND C-TITE M4X8 (BLK NI)	
1-28	*5783543008	SCREW, BIND P-TITE M3X8 (BLK NI)	

INCLUDED ACCESSORIES

REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
	*D00410800A	OWNER'S MANUAL, JAPANESE [J]	
	*D00410900A	OWNER'S MANUAL, ENGLISH [EXCEPT J]	
	*5740004100	MOUNT SCREW KIT, DX-2D	
	*E00454900A	REMOTE CONTROL UNIT, RC-D45 [J]	

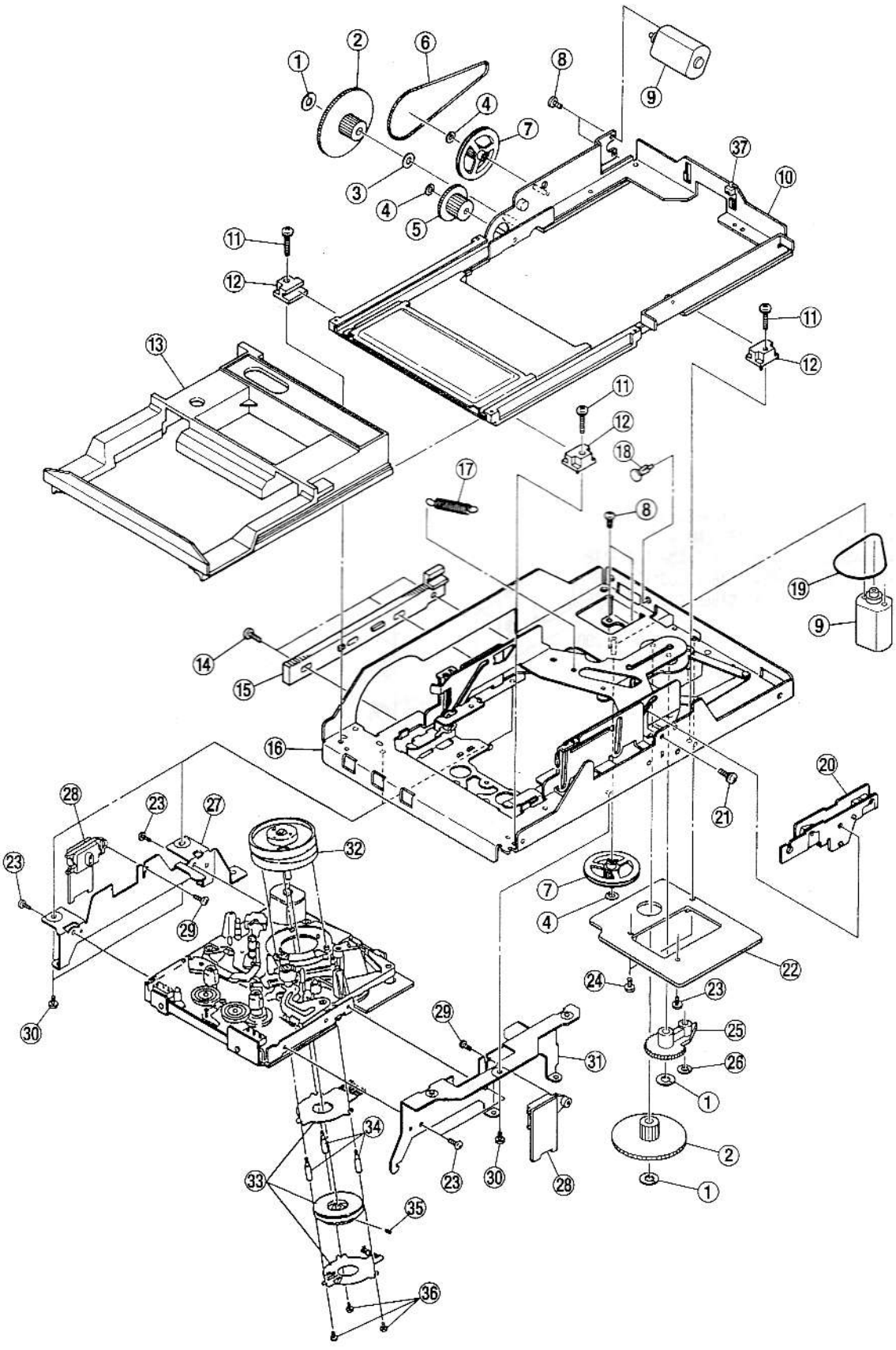
EXPLODED VIEW-2



EXPLODED VIEW-2

REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
2- 1	⚠ 5317003400	BUSHING, 2271 [J, E, K, UK, A]	
	⚠ 5317005600	BUSHING, 2272 [US/C]	
2- 2	⚠ 5350015200	AC CORD, MP-220 [J]	
	⚠ E00526500A	POWER CORD [US/C]	
	⚠ E00528800A	POWER CORD [E]	
	⚠ E00423900A	POWER CORD, 3A 250V [K]	
	⚠ E00120800A	POWER CORD, 5A W/PLUG [UK]	
	⚠ 5350018200	AC CORD [A]	
2- 3	※M00756501C	REAR PANEL, B	
2- 4	※E95074600A	PCB ASSY, I/O	
2- 5	※M00756600A	BRACKET, TRANSPORT	
2- 6	⚠ E00463600A	TRANSFORMER, POWER	
2- 7	※M0082300	SPACER, STBS-10U	
2- 8	※E95074201A	PCB ASSY, POWER [J]	
	※E95074211A	PCB ASSY, POWER [US/C]	
	※E95074241A	PCB ASSY, POWER [E, K, UK]	
	※E95074261A	PCB ASSY, POWER [A]	
2- 9	※5801406000	BASE, TRANS	
2-10	※M00756800A	BRACKET, PS	
2-11	※M00756400A	FRAME, CENTER	
2-12	※5786713000	CLIP, HARNESS 3.0X9.1X50	
2-13	※E95074400A	PCB ASSY, MAIN	
2-14	※E00445700A	FLAT CABLE, CUJ(1.0)-11F	
2-15	※E00445900A	FLAT CABLE, CUJ(1.0)-26F	
2-16	※E00445800A	FLAT CABLE, CUJ(1.0)-17F	
2-17	※E00525200A	FLAT CABLE, CUJ1.0-7F-200	
2-18	※5787030800	SUPPORT, PCB PS-8NS	
2-19	※M00756200C	CHASSIS, MAIN	
2-20	※E95077200A	PCB ASSY, HP	
2-21	※M00756900A	BRACKET, HP	
2-22	※E95074300A	PCB ASSY, SW AC	
2-23	※M00760900B	BRACKET, FRONT CHASSIS	
2-24	※M00756300C	CHASSIS, FRONT	
2-25	M00757300A	ROD, EXTENTION	
2-26	M00001500A	BUTTON, C	
2-27	※M00844800A	SPACER, FRONT A	
2-28	※E95077001A	PCB ASSY, FRONT	
2-29	M00757400A	KNOB, VOL	
2-30	M00757700A	KNOB, SLIDE	
2-31	※5504676000	FOOT, 19L	
2-41	※5783693006	SCREW, BIND S-TITE M3X6 (BLK NI)	
2-42	※5801536400	SCREW, DSUB LOCK M2.6X0.45	
2-43	※5783543008	SCREW, BIND P-TITE M3X8 (BLK NI)	
2-44	※5783033006	SCREW, BIND S-TITE M3X6	
2-45	※5783073006	SCREW, PAN CUP S-TITE M3X6	
2-46	※5783034006	SCREW, BIND S-TITE M4X6	
2-47	※5783034020	SCREW, BIND S-TITE M4X20	

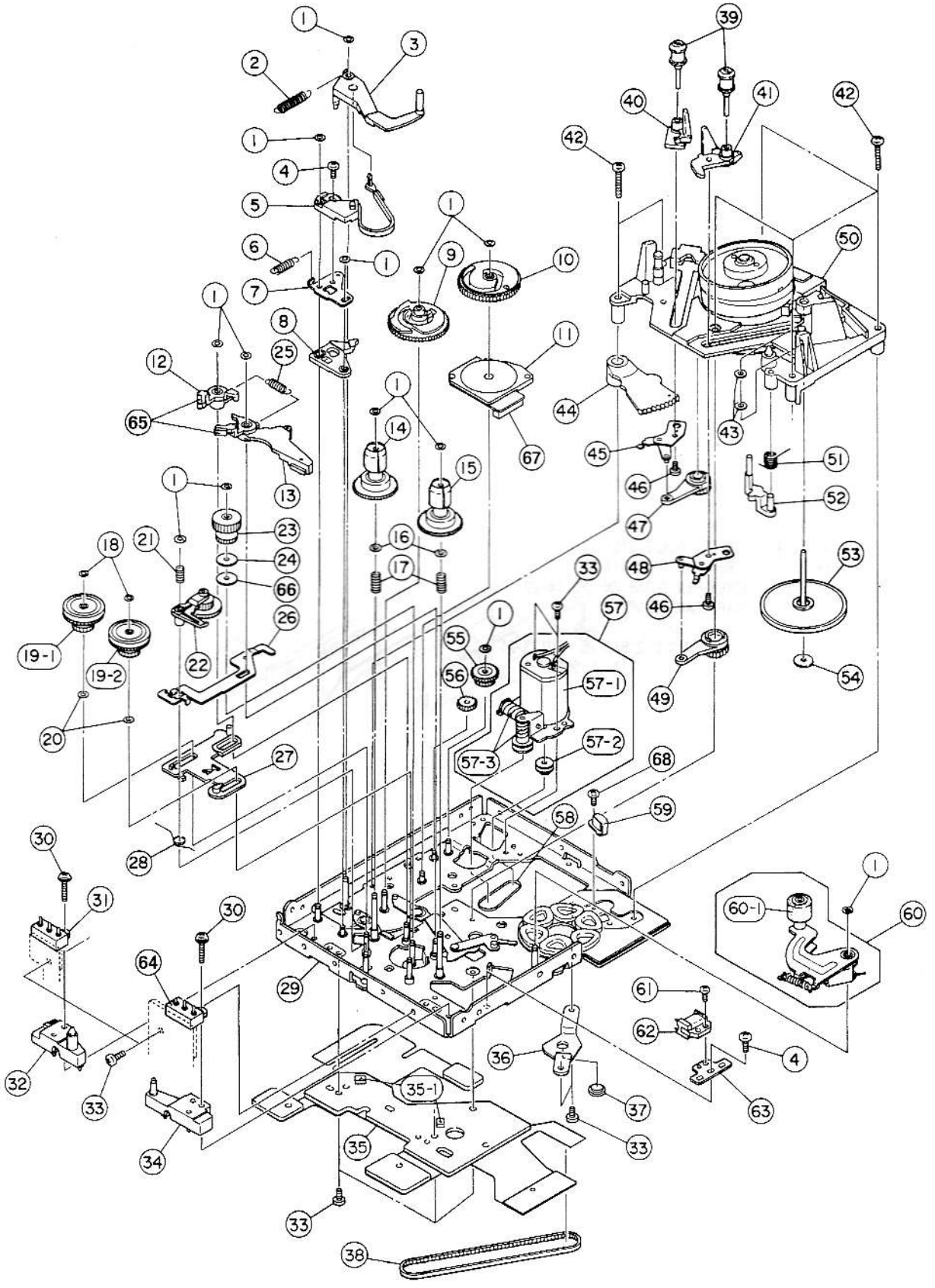
EXPLODED VIEW-3



EXPLODED VIEW-3

REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
3- 1	*5761817100	W LUMIRROR C, 3.5X0.25 FJ123-22	
3- 2	5761816801	GEAR DRIVE, SD168-21	
3- 3	*V00020000A	W PORI, 4.1X0.25	
3- 4	*5761688400	W LUMIRROR, FJ123-14	
3- 5	5761819001	GEAR TIMING, SD169-21	
3- 6	V00085000A	BELT DRIVE, SF117-12	
3- 7	5761816701	GEAR PULLEY, SD170-21	
3- 8	*5761815200	SCREW, PAN 1 2.0X2.0 NI FG121-16	
3- 9	5761816601	MTR BLK, S525S019	
3-10	*V00019400A	HOLDER BLK	
3-11	*5761819300	SCREW, PAN 2.6X10 ZN UG19W-11	
3-12	5761819101	BUSHING TRAY, SD164-21	
3-13	*5761819201	HOLDER CASSETTE, SD162-21	
3-14	*5761791800	SCREW, PAN 2.6X5 2N FG114-14	
3-15	5761819401	PACK GEAR, SD167-21	
3-16	*V00019600A	HOLDER BASE BLK	
3-17	5761815800	SPRING, SK142-11	
3-18	*5761852100	PUSH RIVET	
3-19	V00085100A	BELT DRIVE, SF118-12	
3-20	V00084100A	SENSOR BLK, S758S035	
3-21	*5761817500	SCREW, PAN 2.0X5 ZN FG114-23	
3-22	*V00083900A	PCB CTL BLK, S737S036	
3-23	*5761813600	SCREW, PAN TT 2.0X4 ZN	
3-24	*5761817200	SCREW, PAN 2.0X8 ZN FG114-22	
3-25	5761816901	GEAR CRANK, SD172-21	
3-26	*5761816000	W LUMIRROR C, 2.6X0.25 FJ123-21	
3-27	*V00084500A	W LUMIRROR C, PLATE L, SC307-51	
3-28	V00084600A	SENSOR BLK, S758S038	
3-29	*5761689500	SCREW, 2X6 UG12H-11	
3-30	*V00020800A	SCREW, PAN TT M2.6X5	
3-31	*V00084400A	SIDE PLATE R, SC306-51	
3-32	V00015200B	CYL ASSY BLK	
3-33	V00083700A	STATOR BLK, T524S027	
3-34	*V00015400A	POST	
3-35	*V00015500A	HS HIRA, M2.0X3	
3-36	*5761809600	SCREW, PAN 1 1.7X2.5 NI UG15K-12	
3-37	*5786720400	CABLE TIE, 08432	

EXPLODED VIEW-4



EXPLODED VIEW-4

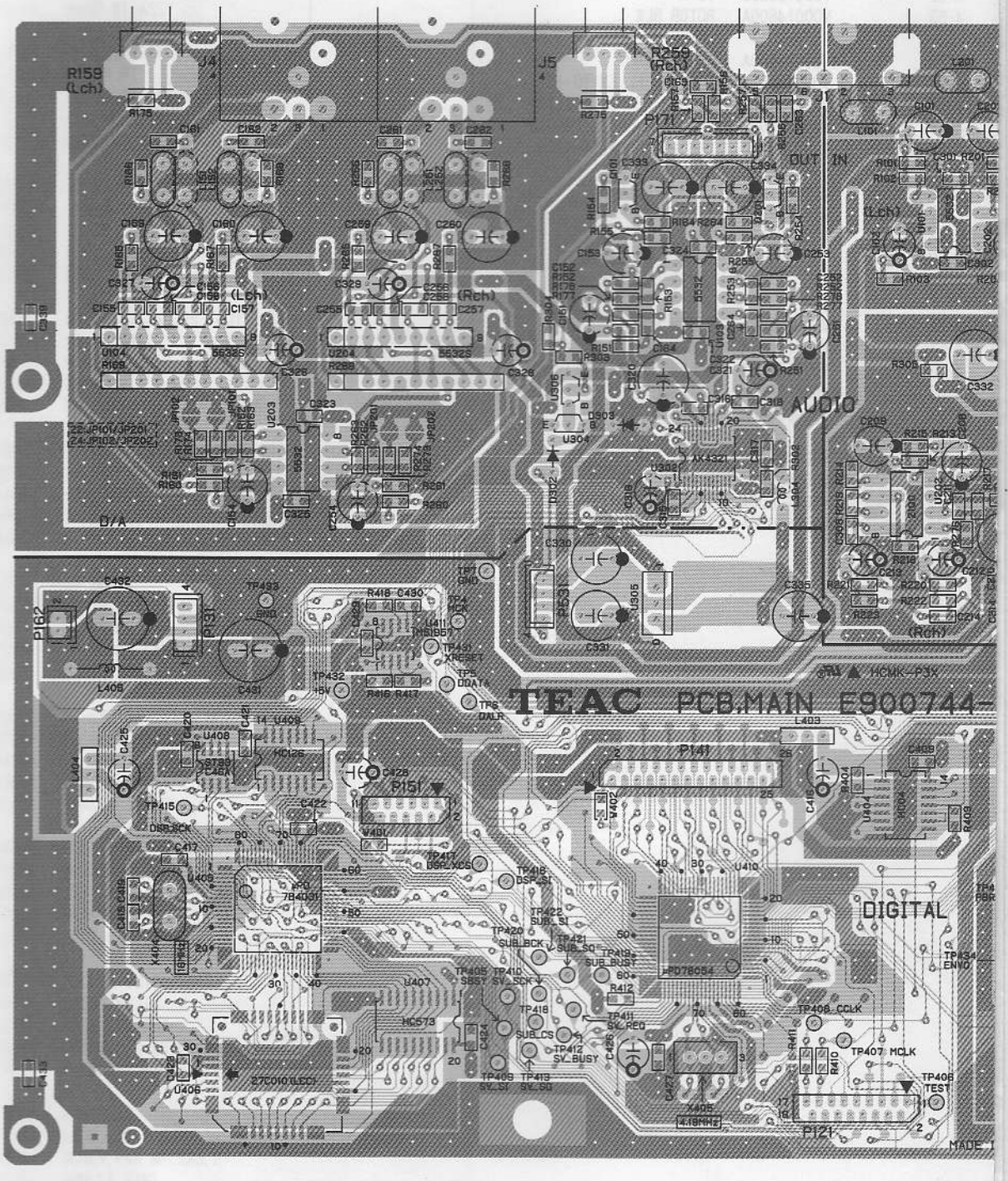
REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
4- 1	*V00011400A	W LUMIRROR, C1230025	
4- 2	V00016800A	SP BT	
4- 3	V00016100A	ARM BT	
4- 4	*V00011900A	SCREW, PAN #0 M1.7X2.5	
4- 5	V00018600A	BAND BT ASSY	
4- 6	V00016900A	SP LEVER BT	
4- 7	V00015800A	LEVER BT	
4- 8	V00016300A	LEVER CAM BT	
4- 9	V00017300C	CAM MODE, SN164-14	
4-10	V00071200A	GEAR MODE, SN173-14	
4-11	V00018800A	SW MODE	
4-12	V00070500A	ARM SU BRAKE, SZ129-13	
4-13	V00013200B	LEVER LDG BLK, S682S030	
4-14	V00018200A	REEL ASSY	
4-15	V00018300A	REEL ASSY	
4-16	*5761839400	W POLY, 2.1X0.25 FJ111-18	
4-17	V00017200A	SP SU REEL	
4-18	*5761806200	W LUMIRROR C, 0.9X0.25	
4-19-1	V00018100A	TU ASSY	
4-19-2	V00019000A	TU ASSY	
4-20	*5761806000	W POLY, 1.4X0.25 FJ111-16	
4-21	V00016600A	SP IDLE	
4-22	V00018400A	GEAR IDLE	
4-23	V00017900A	PULLEY CENTER	
4-24	*V00069300A	W RUMIRROR, 2.1X0.3	
4-25	V00016700A	SP BRAKE	
4-26	*V00015600A	PLATE CAM	
4-27	*V00016200A	CAM IDLE	
4-28	V00017000A	SP PLATE CAM	
4-29	*V00069500A	CHASSIS BASE BLK, S612S025	
4-30	*5761690100	SCREW, TAP-TITE UG12R-11	
4-31	V00069700A	PUSH SW, UE20J-11	
4-32	V00016400A	SPACER ID, (L)	
4-33	*5761813600	SCREW, PAN TT 2.0X4 ZN	
4-34	V00016500A	SPACER ID, (R)	
4-35	*V00083400A	SENSOR BLK, S758S037	
4-35-1	*V00014100A	GP2S04	
4-36	*V00015700A	BKT CAP	
4-37	*V00059200A	BEARING, THRUST FM177-33	
4-38	V00019200A	BELT CAP, SF122-11	
4-39	V00071000A	ROLLER GUIDE, SQ132-11	
4-40	V00033400A	BASE INC IN	
4-41	V00014400B	BASE INC OUT	
4-42	*V00011600A	SCREW, PAN #0 M1.7X10	
4-43	*V00011500A	W LUMIRROR, 1.4X0.25	
4-44	V00017400A	ARM GEAR	
4-45	V00012000A	LINK LDG BLK	
4-46	*V00011700A	SCREW, PAN M1.7X3.5	
4-47	V00017500A	ARM L1, (IN)	
4-48	V00012200A	LINK LDG BLK	

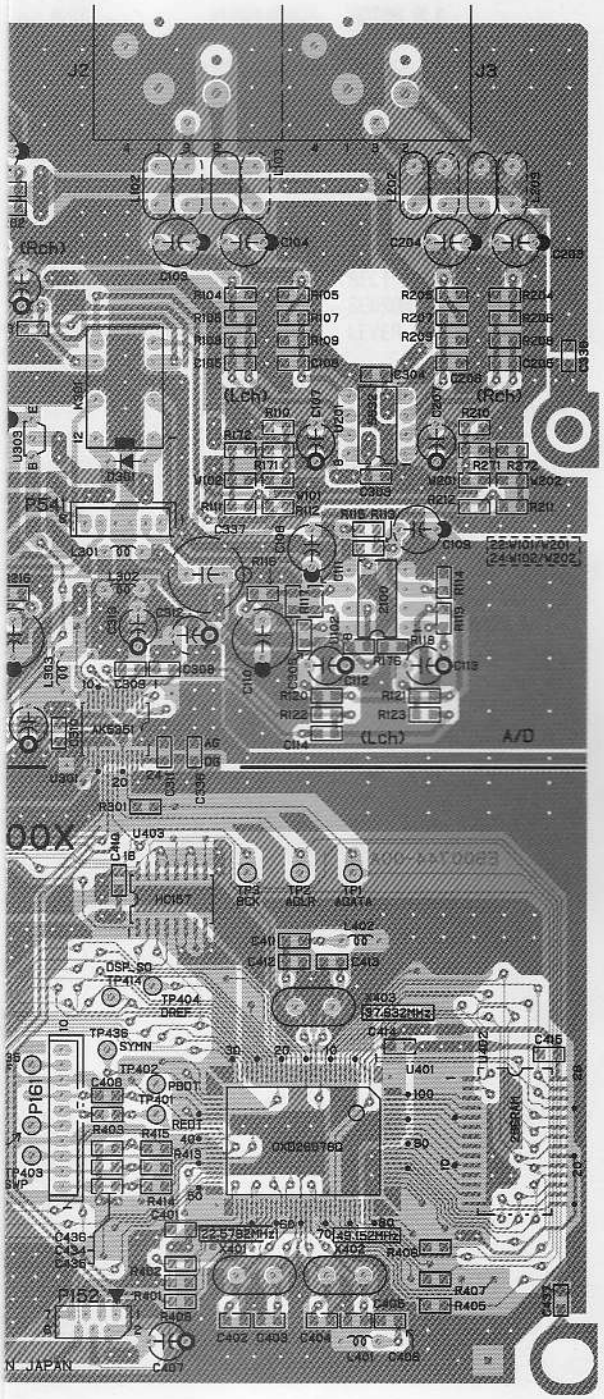
EXPLODED VIEW-4

REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
4-49	V00017600A	ARM L1, (OUT)	
4-50	V00083600A	CYL ASSY, CYKF2W804A	
4-51	*V00017100A	SPRING, TG-R	
4-52	V00016000B	TG-R	
4-53	V00014600A	ROTOR BLK	
4-54	*V00014900A	FRANGE CAP	
4-55	V00070300A	WORM WHEEL, SN170-12	
4-56	V00070400A	CENTER GEAR, SN171-12	
4-57	V00013300C	GEAR LDG BLK, S729S018	
4-57-1	V00025600B	LDG MOTOR, SW131-11	
4-57-2	V00025700B	MOTOR PULLY	
4-57-3	V00025800B	GEAR ASSY	
4-58	V00013500B	BELT LDG	
4-59	V00014800B	SENSOR MR, EZ71B-00	
4-60	V00012700A	LEVER LDG BLK	
4-60-1	V00012800A	PINCH ROLLER	
4-61	*V00011800A	SCREW, PAN #0 M1.4X2.5	
4-62	V00018500B	SOLENOID, SW133-11	
4-63	*V00015900A	BKT SOL	
4-64	V00069800A	PUSH SW, UE20J-12	
4-65	V00025900A	BRAKE PAD	
4-66	*V00053400A	W PORI, 3XT0.45 UJ16E-11	
4-67	V00070600A	TERMINAL, 5PIN UH12S-11	
4-68	*V00056000A	SCREW, M1.2X4, UG23R-11	

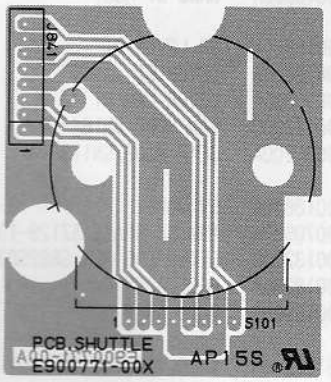
8. PC BOARDS AND PARTS LIST
基板図とパーツリスト

MAIN PCB

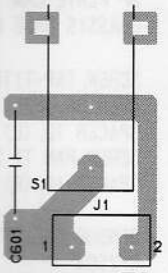




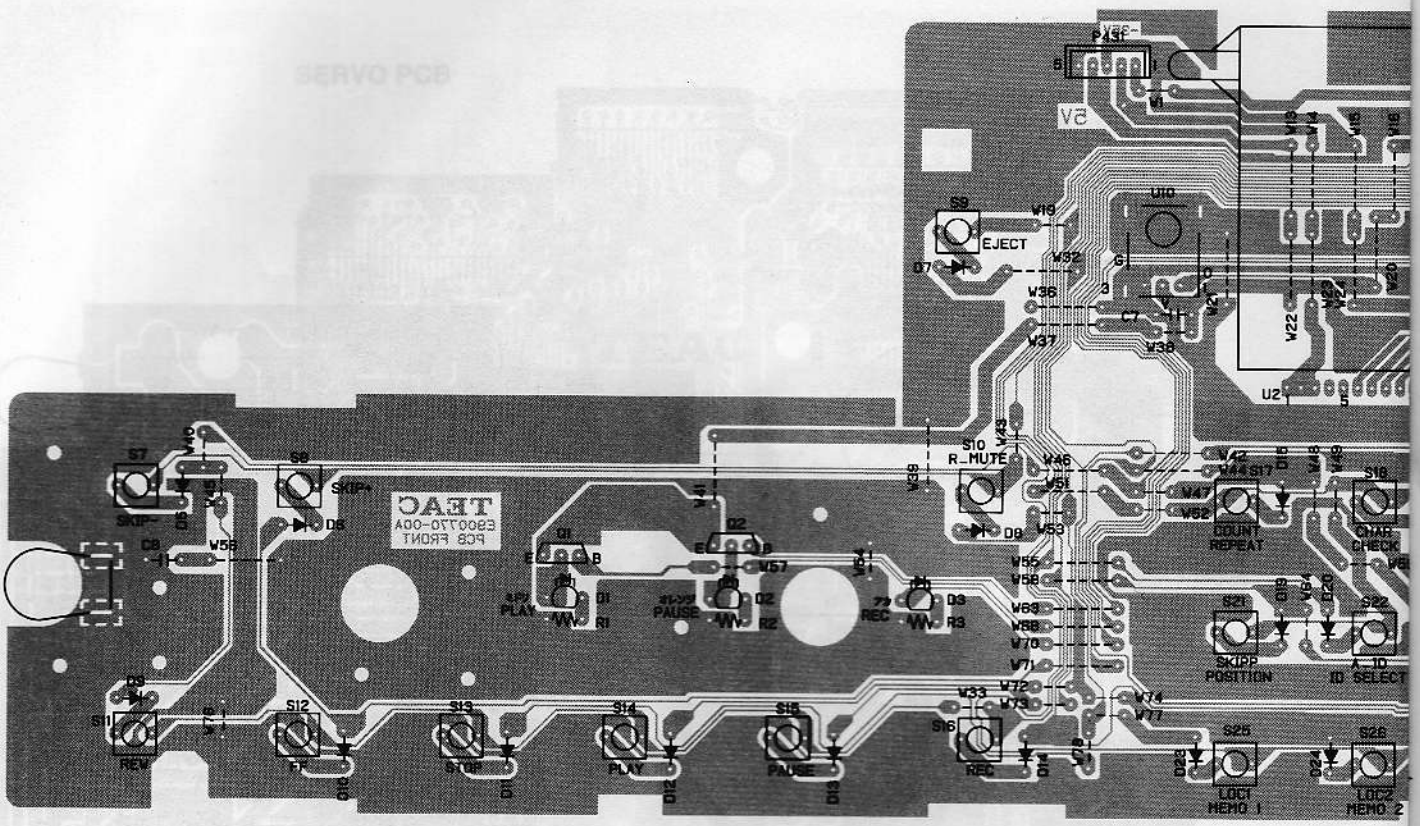
SHUTTLE PCB



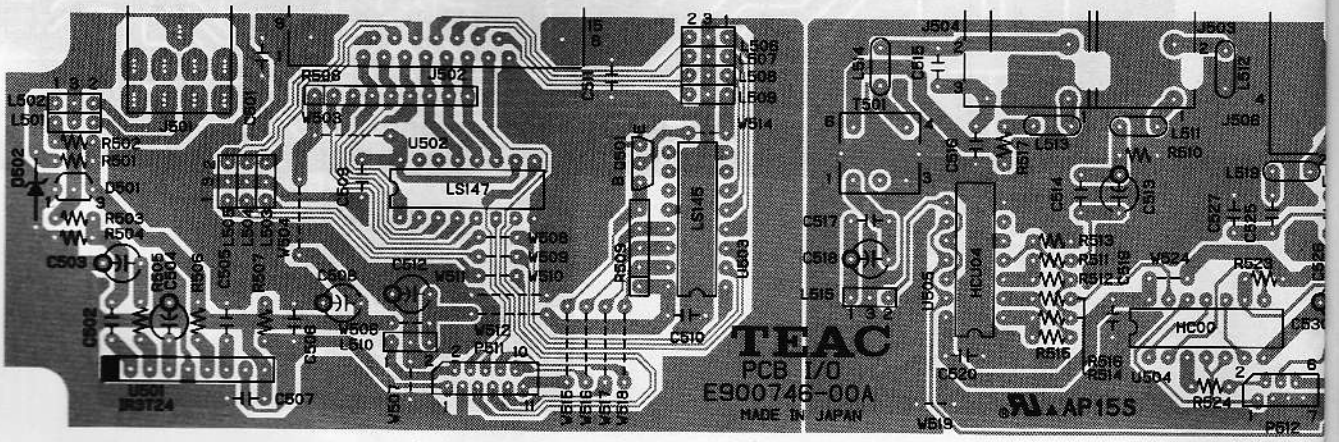
SW AC PCB

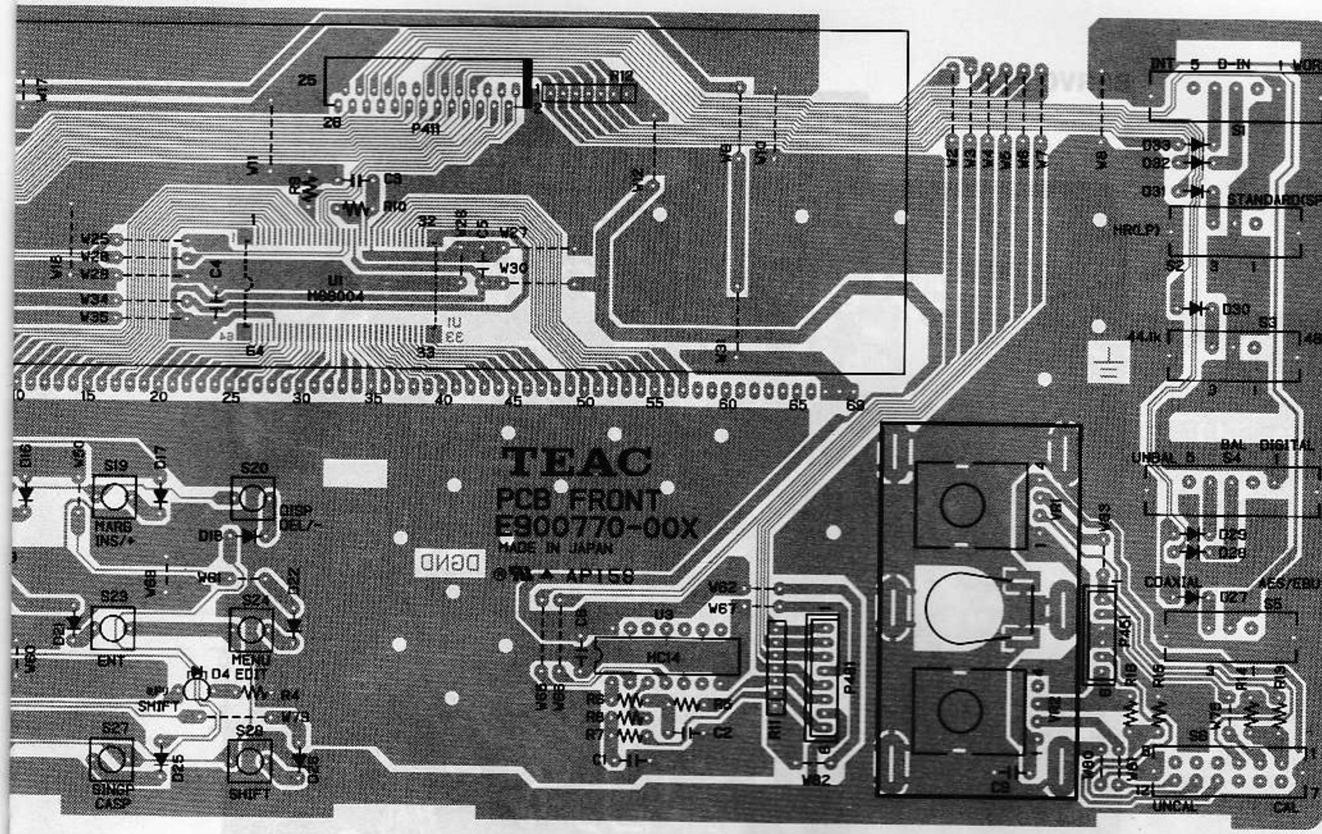


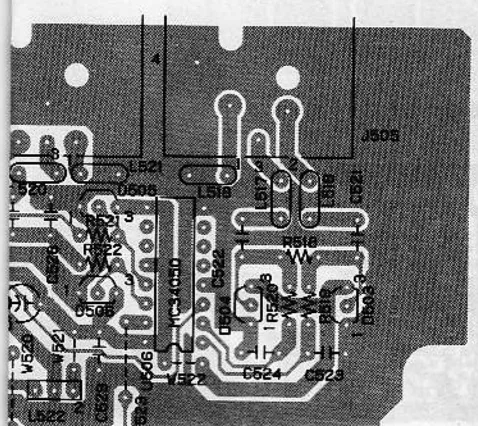
FRONT PCB



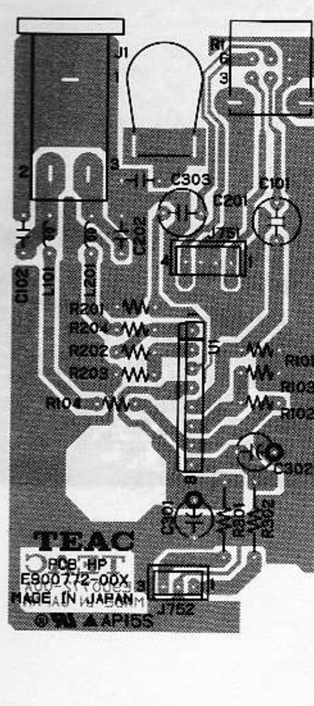
I/O PCB



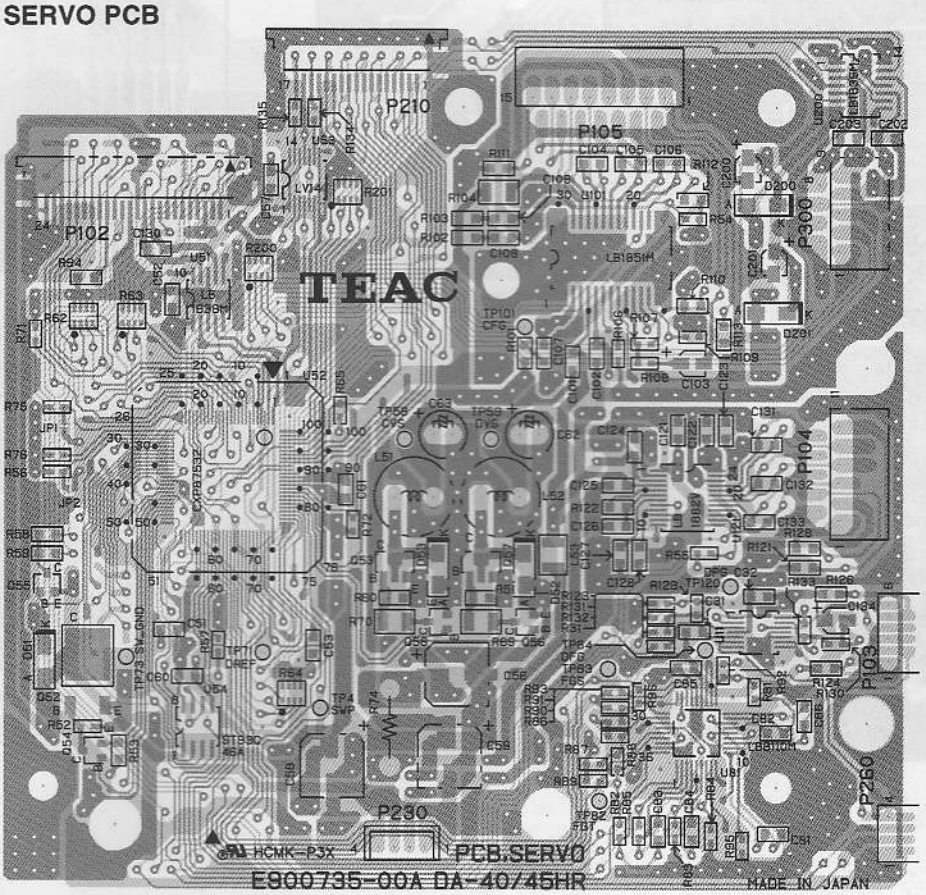

TEAC
PCB FRONT
E900770-00X
MADE IN JAPAN
AP15S
DGND
M66004
HC14
P411
MARG INS/+
DISP DEL/-
ENT
MENU
D4 EDIT
SHIFT
SINGP CASP
INT 5 D-IN 1 WORD
STANDARD(SP)
HR(LP)
44.1K
48K
UNBAL 5 S4 BAL DIGITAL
COAXIAL
AES/EBU
UNCAL
CAL


J505

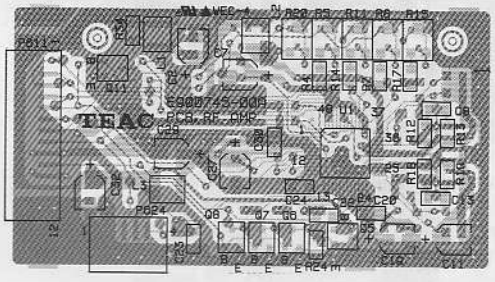
HP PCB


TEAC
PCB HP
E900772-00X
MADE IN JAPAN
AP15S

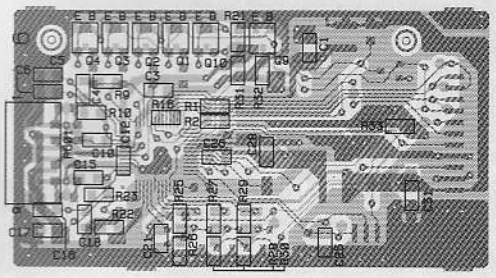
SERVO PCB



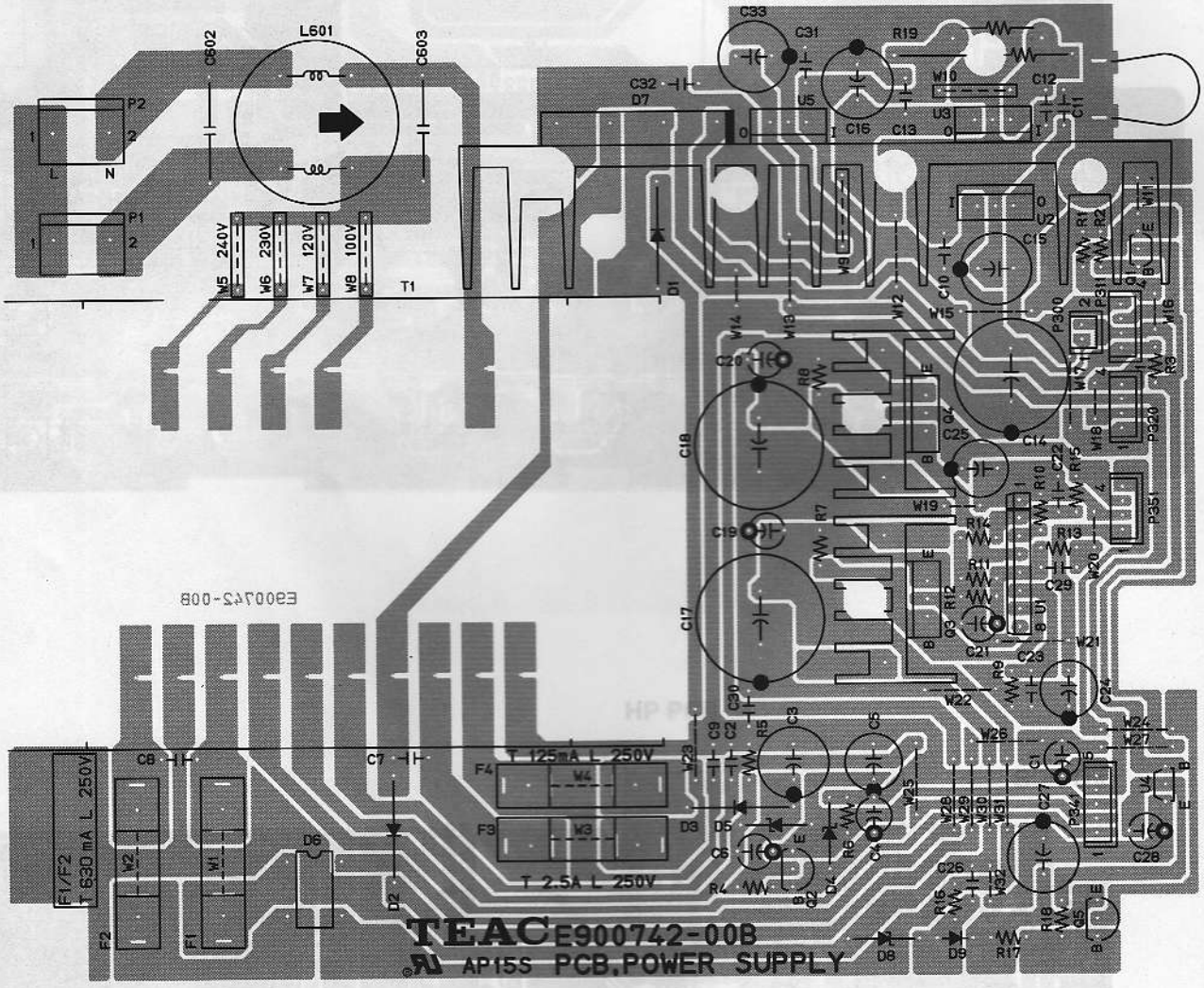
RF AMP PCB SIDE A



RF AMP PCB SIDE B



POWER PCB


L601
C602
C603
P2
P1
W5 240V
W6 230V
W7 120V
W8 100V
T1
C33
C31
R19
C32
D7
U5
C16
C13
W10
C12
U3
C11
U2
C15
C10
W15
P300
C20
R8
C18
C25
C14
C19
R7
W19
R14
R13
R11
C29
C17
C21
C23
W21
W22
C24
W26
W24
W27
C8
C7
F4
T 125mA L 250V
W4
F3
W3
T 2.5A L 250V
F1/F2
T 630 mA L 250V
W2
W1
D6
D2
D3
D5
C6
R6
R4
C26
W32
C28
D8
D9
R17
TEAC E900742-00B
AP15S PCB,POWER SUPPLY

MAIN PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	*E95074400A	PCB ASSY, MAIN
	*E90074400A	PCB, MAIN
	*E00533200A	WIRE, MAIN 40 L=95
D301	5224015020	D, 1SS133T-77 FT
D302	5224015020	D, 1SS133T-77 FT
D303	5224015020	D, 1SS133T-77 FT
D304	5224015020	D, 1SS133T-77 FT
J1	E0013220	JACK, RCA 4P WHT, RED
J2, 3	E0047090	JACK, XLR IN NC3FAH2
J4, 5	E0035610	JACK, NC3MAH(XLR)
K301	5290012700	RELAY, 12V G5A-237PL
L101, 201	5347027620	FERRITE BEAD, FBR07HA850
L102, 202	5347027620	FERRITE BEAD, FBR07HA850
L103, 203	5347027620	FERRITE BEAD, FBR07HA850
L151, 251	5347027620	FERRITE BEAD, FBR07HA850
L152, 252	5347027620	FERRITE BEAD, FBR07HA850
L301-304	5286032720	COIL, CHOKE 1.0UH K(LAP2T)VT
L401	5286032920	COIL, CHOKE 1.5UH K(LAP2T)VT
L402	5286033320	COIL, CHOKE 3.3UH K(LAP2T)VT
L403, 404	5292808620	EMI FILTER, EMC EMT 10000PFT
L405	5286030200	COIL, CHOKE 47UH LAL04NA
P121	E0045770	CONNECTOR, CFF5117
P131	5336255400	PLUG, CONN. B04B-PH-K-K (BLK)
P141	E0045860	CONNECTOR, CFF5126
P151	E0045710	CONNECTOR, CFF5111
P152	E0045670	CONNECTOR, CFF5107
P161	5336250000	PLUG, CONN. B10B-PH-K-S (WHT)
P162	5336249200	PLUG, CONN. B02B-PH-K-S (WHT)
P171	5336249700	PLUG, CONN. B07B-PH-K-S (WHT)
P531	5336251400	PLUG, CONN. B04B-PH-K-R (RED)
P541	5336249600	PLUG, CONN. B06B-PH-K-S (WHT)
Q101, 201	5231762520	TR, 2SD1915TA
R159, 259	R0076210	VAR RES, RK09K1110-20KB
R169, 269	R00330900A	RES ARRAY, EXBF11L668FP
U101, 201	5220431800	IC, NE5532AN
U102, 202	S0000170	IC, NJM2100D
U103, 203	5220431800	IC, NE5532AN
U104, 204	5220431100	IC, NJM5532S
U301	S0029074	IC, ADC AK5351-VF
U302	S0029084	IC, DAC AK4321-VF
U303	5232255920	TR, DTC143XSA
U304	5232255720	TR, DTC124ESA
U305	13447952	IC, NJM7805FA
U306	5232254720	TR, DTA114ESA
U401	S0024023	IC, CXD2607BQ
U402	S0024254	IC, SRAM SRM2B256SLMX70
U403	5220103800	IC, TC74HC157AF-TP2
U404	5220093500	IC, TC74HC04AF-TP2
U405	S0024873	IC, UPD784031GC-8BT
U406	E0046370	SOCKET, IC160-0324-350

MAIN PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
U406	S00332000A	IC, SYSTEM ROM M27C1001-12C1
U407	S0021454	IC, HD74HC573FPEL
U408	S0033414	IC, M93C46-MN6T
U409	5220116300	IC, HD74HC126FP
U410	S00314900A	IC, UPD78054GC-A25 V1.00
U411	5220118700	IC, M51957BFP
X401	E0046350	RESONATOR, 22.5792M
X402	E0046330	RESONATOR, 49.152M
X403	E0046340	RESONATOR, 37.632M
X404	E0036690	RESONATOR, 16.000MHZ
X405	5347012000	OSC, CERAMIC CST4, 19MGW

SHUTTLE PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	*E95077100A	PCB ASSY, SHUTTLE
	*E90077100A	PCB, SHUTTLE
J841	E00446700A	HARNESS ASSY, SHUTTLE
S101	E0000460	ENCODER, SRGPHJ

SW AC PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	*E95074300A	PCB ASSY, SW AC
	*E90074300A	PCB, SW AC
C601	⚠ E0022570	SPK KILLER, 0.0047UF/250V
J1	E00446200A	HARNESS ASSY, SW AC
S1	⚠ 5300060700	SW, PUSH SDDLD1248A

FRONT PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	*E95077001B	PCB ASSY, FRONT
	*E90077000B	PCB, FRONT
	*5555590000	PLATE A, EARTH
	*M00757000A	BRACKET, VOL
	*M00761000B	BRACKET, FL
	*M00823600A	SHEET, ADHESIVE
D1, 4	S0029152	LED, LN38GPX(GRN)
D2	S0030662	LED, LN48YPX(ANV)
D3	S0029141	LED, LN28RPX(RED)
D5-33	5224015020	D, 1SS133T-77 FT
P411	E0046130	CONNECTOR, CFF3326
P431	5336287500	PLUG, CONN. S5B-PH-K-S (WHT)
P451	5336249600	PLUG, CONN. B06B-PH-K-S (WHT)
P481	5336249800	PLUG, CONN. B08B-PH-K-S (WHT)
Q1, 2	5232254720	TR, DTA114ESA

FRONT PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
R11, 12	5242132300	R ARRAY, EXB Z07E223J
S2, 3	5300917300	SW, SLIDE 1-2 N SSSU01
S4	E0052690	SW, SSSU013-P06S1
S5	5300917300	SW, SLIDE 1-2 N SSSU01
S6	E0042960	SW, SSSU042(L=6)
S7-28	E0047272	SW, EVQ21509K
U1	S0018723	IC, M66004FP
U2	E00423800A	IND TUBE, BJ622GK
U3	5220066700	IC, HD74HC14P
VR1, 2	R0085631	VAR RES, RK11K114(20KA)

I/O PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	*E95074600A	PCB ASSY, I/O
	*E90074600A	PCB, I/O
D501	S0028912	D, MC982
D502	5224571801	D, ZENER RD3.0EL2 FR
D503-506	S0028912	D, MC982
J501	5330016100	JACK, 3P
J502	5334079900	SOCKET, CONN. 15P DSUB
J503	E0046180	JACK, YKC21-3627
J504	E0020230	JACK, RCA PIN J(ORG)
J505	E0047090	JACK, XLR IN NC3FAH2
J506	E0035610	JACK, NC3MAH(XLR)
L501	5292807920	EMI FILTER, EMC EMT 47PFT
L502	5292808620	EMI FILTER, EMC EMT 10000PFT
L503-509	5292808020	EMI FILTER, EMC EMT 100PFT
L510	5292808620	EMI FILTER, EMC EMT 10000PFT
L511-514	5347027620	FERRITE BEAD, FBR07HA850
L515	5292807920	EMI FILTER, EMC EMT 47PFT
L516, 517	5347027620	FERRITE BEAD, FBR07HA850
L519, 520	5347027620	FERRITE BEAD, FBR07HA850
L522	5292808620	EMI FILTER, EMC EMT 10000PFT
P511	E0045710	CONNECTOR, CFF5111
P512	E0045670	CONNECTOR, CFF5107
Q501	5232255620	TR, DTC114ESA
R508	5242118900	RES ARRAY, RMLS 8J223
R509	5242118400	RES ARRAY, RMLS 4J103
T501	5320046300	TRANS, PULS TC-1027-04
U501	S0029250	IC, IR3T24
U502	13442774	IC, SN74LS147N
U503	13441784	IC, SN74LS145N
U504	5220051600	IC, TC74HC00AP
U505	5220040900	IC, UPD74HCU04C
U506	S0026710	IC, M5M34050P

HP PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	*E95077200A	PCB ASSY, HP
	*E90077200A	PCB, HP
	*5555590000	PLATE A, EARTH
	*E00447000A	HARNESS ASSY, HP
J1	5330012600	JACK, 3P FJ332DB-M
L101, 201	5286032720	COIL, CHOKE 1.0UH K(LAP2T)VT
R1	R00762000A	VAR RES, RK09L12B0-20KAX2
R301, 302	⚠ R0035141	R, 1/2W 10 OHM J FT
U1	5220427900	IC, M5216L

SERVO PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	*E95073501A	PCB ASSY, SERVO
	*E90073500A	PCB, SERVO
D51-53	S0021344	D, RB160L-40
D200, 201	S0028854	D, RB060L-40TE25
L51, 52	14728449	COIL, 390UH 10%
L53	14728094	COIL, CHIP 22UH 5%
P102	E0032154	CONNECTOR, 52271-2490
P103	13124439	CONNECTOR, ZH 6B-ZR
P104	E0023650	CONNECTOR, 11FE-ST-VK-N
P105	E0023690	CONNECTOR, 15FE-ST-VK-N
P210	E0042184	CONNECTOR, 52271-1790
P230	5336249400	PLUG, CONN. B04B-PH-K-S(WHT)
P260	13124021	CONNECTOR, 4P S4B-ZR
P300	E0023630	CONNECTOR, 09FE-ST-VK-N
Q52	S0017904	TR, 2SD992K-Z-E2
Q53	5230020200	TR, 2SA1314B-TE12L, C
Q54, 55	13428276	TR, DTA114EKAT-146
Q56	13428286	TR, DTC114EKAT-146
Q57	5230020200	TR, 2SA1314B-TE12L, C
Q58	13428286	TR, DTC114EKAT-146
R62-64	R0067464	RES ARRAY, 1/16W 4X47K J
R74	⚠ R0034901	RD, 1/2W 1.0 OHM J FT
R200, 201	R0067464	RES ARRAY, 1/16W 4X47K J
U11	S0000974	IC, NJM3403AV (TE1)
U51	5220451100	IC, LB1638M TP-T2
U52	S0033530	IC, CXP87532-1XXR V1.01
U53	S0028864	IC, SN74LV14APW-EL
U54	S0033414	IC, M93C46-MN6T
U81	5220448800	IC, LB8110M
U101	5220448900	IC, LB1851M
U121	S0024104	IC, LB1882V
U200	5220449000	IC, LB1836M

RF AMP PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	*E95074501A	PCB ASSY, RF AMP
	*E90074500A	PCB, RF AMP
	*M00757100A	SHIELD CASE, A
L1	14728094	COIL, CHIP 22UH 5%
L2	14728102	COIL, CHIP 100UH 5%
L3	14728094	COIL, CHIP 22UH 5%
P601	E0034094	CONNECTOR, S6BZRSM3ATF
P611	E0027734	CONNECTOR, S12BZRSM3ATF
P624	E0034074	CONNECTOR, S4BZRSM3ATF
Q1	13428288	TR, DTC144EKAT-146
Q3	13428288	TR, DTC144EKAT-146
Q5	13427337	TR, 2SC2412K
Q11	13428288	TR, DTC144EKAT-146
R5, 8	R0066284	VAR RES, EVM3VSX50B53
U1	S0024084	IC, CXA1364R

POWER PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	*E95074201A	PCB ASSY, POWER [J]
	*E95074211A	PCB ASSY, POWER [US/C]
	*E95074241A	PCB ASSY, POWER [E, K, UK]
	*E95074261A	PCB ASSY, POWER [A]
	*E90074200B	PCB, POWER SUPPLY
	*5800501502	HEATSINK
	*5780003008	SCREW, BIND M3X8
	*5786700400	EARTH LUG, B-4 3.2φ [US/C]
	*5555590000	PLATE A, EARTH
	*E0034560	CLIP, FUSE H0446 [E, K, UK, A]
	*M00869500A	SHIELD COVER [E, K, UK, A]
	*M00869600A	WASHER [E, K, UK, A]
C3	⚠ 5260424910	C, ELEC. 220UF 50V
C5	⚠ 5260424320	C, ELEC. 100UF 50V
C7-10	⚠ 12908842	C, CC 0.1UF 50V
C12	⚠ 12908842	C, CC 0.1UF 50V
C14	⚠ 5260428110	C, ELEC. 4700UF 16V
C15	⚠ 5260426410	C, ELEC. 1000UF 16V
C17, 18	⚠ 5260476910	C, ELEC. 3300UF 25V
C24, 25	⚠ 5260473420	C, ELEC. 100UF 25V
C27	⚠ 5260423420	C, ELEC. 47UF 16V
C31	⚠ 12908842	C, CC 0.1UF 50V
C602, 603	⚠ E0022570	SPK KILLER, 0.0047UF 250V
D1-3	⚠ 5224013200	D, DS135 D FR
D4	5224579401	D, ZENER RD33EL1 FR
D5	5224573801	D, ZENER RD6.2EL2 FR
D6	⚠ 5228010700	SILICON STAC, S1WB(A)20
D7	⚠ 5228013400	SILICON STAC, D3SBA20
D8	⚠ 5224573001	D, ZENER RD4.7EL3 FR
D9	⚠ 5224015020	D, 1SS133T-77 FT

POWER PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
F1, 2	⚠ 5142185000	FUSE, MINI T-LAG 630MA 250V [E, K, UK, A]
F3	⚠ 5142190000	FUSE, MINI T-LAG 2.5A 250V [E, K, UK, A]
F4	⚠ 5142180000	FUSE, MINI T-LAG 125MA 250V [E, K, UK, A]
L601	⚠ 5292806300	FILTER, NOISE FKOB16MH13
P1	5336376200	PLUG, CONN. B2P3-VH
P2	E0046660	CONNECTOR, MPSS156-3-C
P311	5336255400	PLUG, CONN. B04B-PH-K-K(BLK)
P320	5336249400	PLUG, CONN. B04B-PH-K-S
P341	5336249500	PLUG, CONN. B05B-PH-K-S(BLK)
P351	5336251400	PLUG, CONN. B04B-PH-K-R(RED)
Q1	S0028932	TR, 2SC5395F
Q2	⚠ 5145085000	TR, 2SA934 R
Q3	⚠ S0017100	TR, 2SB1565E
Q4	⚠ S0017110	TR, 2SD2394E
Q3, 4	5730039200	HEATSINK, OSH-2425-SPL
Q5	5145085000	TR, 2SA934 R
R19	⚠ R0085621	RW, 3W 3.3 OHM J
U1	⚠ 5220425800	IC, M5230LA
U2	⚠ S0000180	IC, LM2940T-9.0
U3	⚠ 13447952	IC, NJM7805FA
U4	S0030861	TR, DTC144TSA TP
U5	⚠ 13447952	IC, NJM7805FA

DA-40

TASCAM
TEAC Professional Division

ティアック株式会社 電子機器事業部 タスカムディビジョン ☎ (0422) 52-5072 〒180－8550 東京都武蔵野市中町3－7－3

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サービスに関するお問合わせは、最寄りの営業所等へご連絡ください。営業所にはサービス・センターが併設されています。	札幌営業所	☎ (011) 521-4101(代)	〒064－0807 札幌市中央区南7条西2－2	くぼたビル
	仙台営業所	☎ (022) 227-1501(代)	〒980－0811 仙台市青葉区1番町2－5－5	中央ビル
	新潟サービス	☎ (025) 245-0103	〒950－0865 新潟県新潟市本馬越1－4－11	黒井ハイツ
	大宮サービス	☎ (048) 642-4551	〒331－0052 大宮市三橋2－8－46	
	サービス2課	☎ (0422) 52-5107	〒180－8550 東京都武蔵野市中町3－7－3	
	タスカム東京営業所	☎ (03) 3592-2051(代)	〒100－0014 東京都千代田区永田町2－10－7	星ガ岡会館
	千葉サービス	☎ (043) 255-1281	〒260－0042 千葉市中央区椿森1－21－13	清水ビル
	神奈川サービス	☎ (042) 746-6850	〒228－0803 相模原市相模大野7－14－9	グリーンシティビル
	静岡サービス	☎ (054) 238-2431	〒422－8034 静岡市高松1－12－1	寿通ハイツ105号
	名古屋営業所	☎ (052) 702-3100(代)	〒465－0025 名古屋市名東区上社5－406	
	京都サービス	☎ (075) 871-8730	〒616－8224 京都市右京区常盤窪町19	西垣ビル
	大阪営業所	☎ (06) 6384-5201(代)	〒564－0062 吹田市垂水町3－34－10	
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	岡山サービス	☎ (0862) 25-8601	〒700－0945 岡山市新保1142－6	
	広島営業所	☎ (082) 294-4751(代)	〒730－0846 広島市中区西川口町13－19	
	福岡営業所	☎ (092) 431-5781(代)	〒812－0008 福岡市博多区東光2－2－24	
	福岡サービス	☎ (092) 936-5672	〒811－2202 福岡県粕屋郡志免町志免1041	

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TEAC DEUTSCHLAND GmbH	Bahnstrasse 12, 65205 Wiesbaden-Erbenheim, Germany	Phone:0611-71580
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TEAC AUSTRALIA PTY., LTD. A.C.N. 005 408 462	106 Bay Street, Port Melborne, Victoria 3207, Australia	Phone:(03)9644-2442
TEAC ITALIANA S.p.A.	Via C. Cantù 11, 20092 Cinisello Balsamo, Milano, Italy	Phone:02-66010500

PRINTED IN JAPAN 0399U 0.43 M-1490A

DA-45HR Remote Control Code MODEL: RC-D45

KEY No.	Function	DATA	KEY No.	Function	DATA
K1		0	K33		40
K2		1	K34	AUTO ID	41
K3		2	K35	MENU	42
K4	OPEN/CLOSE	3	K36		43
K5		4	K37	MARGIN RESET	44
K6		5	K38	DISPLAY	45
K7		6	K39	SINGLE PLAY	46
K8		7	K40	REPEAT	47
K9	CAPS	8	K41	SP-1	48
K10	CHECK	9	K42	CURSOR ←	49
K11	POSITION	A	K43	CURSOR →	4A
K12	ID SELECT	B	K44		4B
K13	INS / +	C	K45		4C
K14	DEL / -	D	K46		4D
K15	EDIT	E	K47		4E
K16	ENTER	F	K48		4F
K17		10	K49	SKIP <<	50
K18		11	K50	SKIP >>	51
K19		12	K51	MEMO 1	52
K20		13	K52	MEMO 2	53
K21	1 / ABC	14	K53	REW	54
K22	2 / DEF	15	K54	F FWD	55
K23	3 / GHI	16	K55	LOC 1	56
K24	COUNTER MODE	17	K56	LOC 2	57
K25	4 / JKL	18	K57	STOP	58
K26	5 / MNO	19	K58	PLAY	59
K27	6 / PQR	1A	K59	PAUSE	5A
K28	CHAR	1B	K60	RECORD	5B
K29	7 / STU	1C	K61		5C
K30	8 / VWX	1D	K62	SAMPLING MONITOR	5D
K31	9 / YZ&	1E	K63	REC MUTE	5E
K32	SKIP PLAY	1F	K64		5F

NEC format Custom code = 8371 h

JACK: 3.5 STEREO PHONE JACK
TIP :3V power supply for remote controller
RING :control signal

TECHNICAL INFORMATION

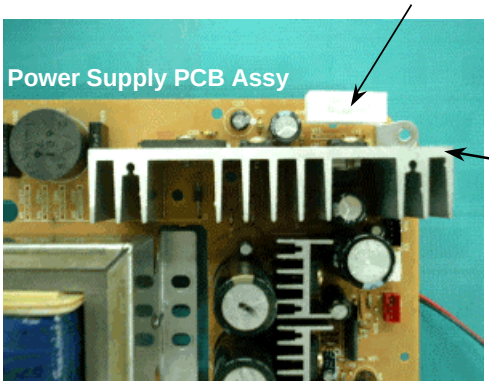
TASCAM DA-45HR, Heat Sink

No. **0010**
DATE 26th April 2000

Symptom: Small jitter components will be added on the digital output momentarily at the beginning of PLAY, REC/PLAY, EJECT or tape loading. Some machines receiving this digital output may get out of synchronization.
Example:
* TM-D8000's Fs STATUS will show "UNLOCKED" momentarily.
* Sonic Solution will take about 10 seconds to re-lock.

Cause: The power supply fluctuates slightly at the beginning of the drum motor rotation.

Solution: On the Power Supply PCB, short R19 (3.3 Ω) and replace the heat sink with enlarged one.



There is no production which have the new heat sink as of 20/Apr/2000.

TEAC **TECHNICAL INFORMATION**

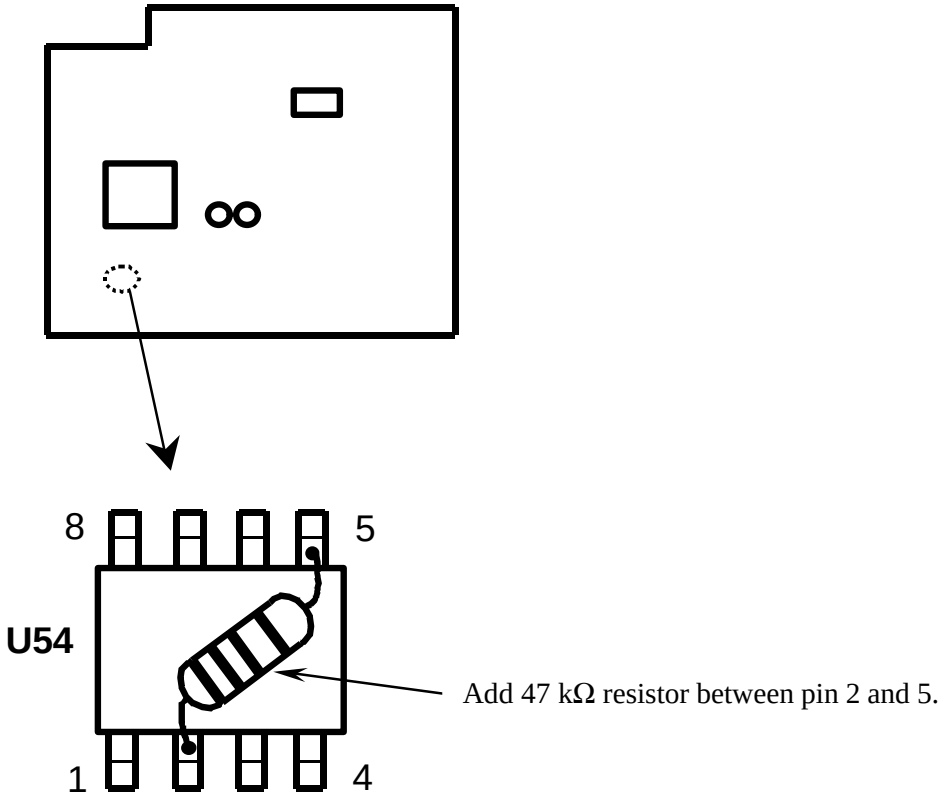
TASCAM DA-40, DPG (Delay PG) Misread

No. **9928**
DATE 22nd October 1999

Phenomenon: No output or noise can be heard with self-recording/playback. No problem on playback with tapes recorded by other machines.
Cause: In very rare occasion, DPG (delay PG) value stored in the EEPROM (U54 on Servo PCB Assy) is misread causing faulty recording position.
Solution: 47 kΩ pull-down resistor has been added to U54-2 and 5 on the Servo PCB Assy on the products with S/No. 0040171 and higher.
Note: DA-45HR does not concern this phenomenon.

47 kΩ resistor, **P/No. 52400322-20**

Servo PCB Assy
Components Side



TECHNICAL INFORMATION

TASCAM DA-40, ROM Upgrade (SYS V1.10)

No. **9927**
DATE 22nd October 1999

System ROM, U406 on the Main PCB Assy has been upgraded from V1.00 to V1.10 on the products with S/No. 0060001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.10	**S003320-00B**	**S0001133** (M27C1001-12C1)

* Use the PLCC 3232-11 (Advantech) ROM adapter to program the M27C1001-12C1. This ROM Adapter is the one being used for RC-898 (CONT) ROM.

Problem Corrected by V1.10

1) Ready to write the START ID. Start audio recording. Press ENTER immediately then the unit will freeze.
2) Renumbering during LP mode. The first START ID is renumbered correctly (300 frames). However, other START ID's are recorded wrongly (600 frames).
3) LOC2 does not work during REPEAT A-B mode.
4) LOC1 and LOC2 do not work during FFWD, REW, CUE and REVIEW.
5) When locating, mechanism mode transits to capstan driving mode near the locating point. In that case, pressing PLAY cannot reserve PLAY mode but stops at the locate point.
6) When the unit cannot find target program number due to that the program number is discontinuous, the unit goes to PLAY mode on adjacent program. This behavior has been changed that the unit stops when the target is not found.

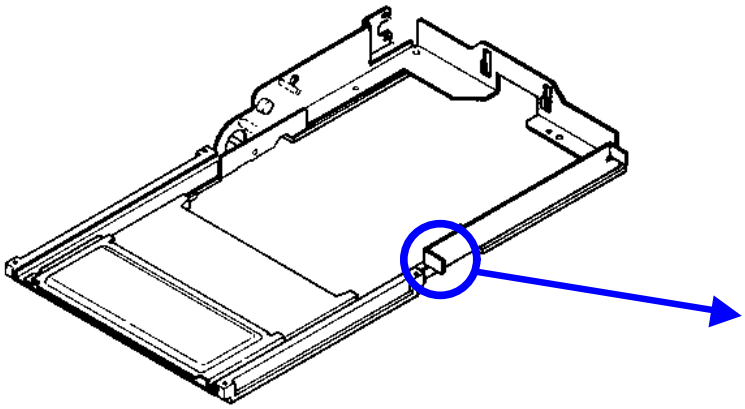
TEAC **TECHNICAL INFORMATION**

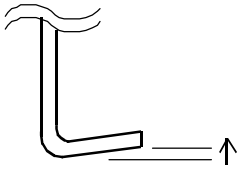
R-9/10/, DA-30/30MK2/40/45HR, False Cassette Loading

No. **9920**
DATE 3rd September 1999

Symptom: When a tape is loaded, a machine does not accept it and ejects a cassette automatically.
Cause: Total length of (cassette shell + opened lid) is slightly longer than usual. When such cassette is loaded, Cassette IN Switch cannot be activated.
Solution: Slightly bend a lever for the Cassette IN Switch as shown below.

Note:
1) Cassette IN Switch is located at No.73-22-04, Fig. 3-17, page 14, DA-30MK2 service manual.
2) This symptom has been confirmed in Japan with following tapes.
maxell R-120DM / TDK R-120 / 3M R-120 / KAO





Bend the lever slightly.

TEAC TECHNICAL INFORMATION

TASCAM DA-45HR, ROM Upgrade (SYS V1.30)

No. **9909**
DATE 9th April 1999

System ROM, U102 on the Main PCB Assy has been upgraded from V1.10 to V1.30 on the products with S/No. 0090001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.30	**S003157-00D**	**S0001133** (M27C1001-12C1)

* Use the PLCC 3232-11 (Advantech) ROM adapter to program the M27C1001-12C1. This ROM Adapter is the one being used for RC-898 (CONT) ROM.

Problem Corrected by V1.30

1) Ready to write the START ID. Start audio recording. Press ENTER immediately then the unit will freeze.
2) Set dd mode. The DA-45HR is now recording AES/EBU signal. Digital out of the CD player is also fed to COAX input. START ID is recorded erroneously when the program number of the CD is incremented.
3) When SKIP is pressed many times rapidly, some SKIP commands may be missed.
4) LOC2 does not work during REPEAT A-B mode.
5) LOC1 and LOC2 do not work during FFWD, REW, CUE and REVIEW.
6) When locating, mechanism mode transits to capstan driving mode near the locating point. In that case, pressing PLAY cannot reserve PLAY mode but stops at the locate point.
7) When the unit cannot find target program number due to that the program number is discontinuous, the unit goes to PLAY mode on adjacent program. This behavior has been changed that the unit stops when the target is not found.
8) Originally, STANDARD and HR mode cannot be mixed on one tape. Warning message will appear if the operator attempts that. However, following procedure will mix them illegally causing half or double speed sound.
    1. Load a tape stripped with standard mode.
    2. Enter Rec/Pause mode.
    3. Change the Rec mode switch to HR(24BIT).
    4. Start recording. No warning appears.
    5. Rewind and reproduce the recorded portion. Mechanism runs at the standard speed and the half speed sound can be heard.

    * By the same manner, standard mode recording can be mixed on the tape stripped with HR mode. In this case double speed sound can be heard on playback.

TEAC **TECHNICAL INFORMATION**

TASCAM DA-45HR, Fan Noise Suppression

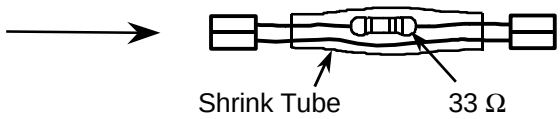
No. **9905**
DATE 5th March 1999

In case the customer requests to lower the fan noise, applying Bracket Kit, Fan DA-45HR is suggested.

Bracket Kit, Fan DA-45HR P/No. V000866-00A

This kit consists of following parts:

Description	Q'ty
Harness Assy, Fan Kit	1
Bracket, FAN A	1
Bind M3×6	2
Bracket, FAN B	1
Pin, Step	4
Damper	4



Changes made with this kit are:

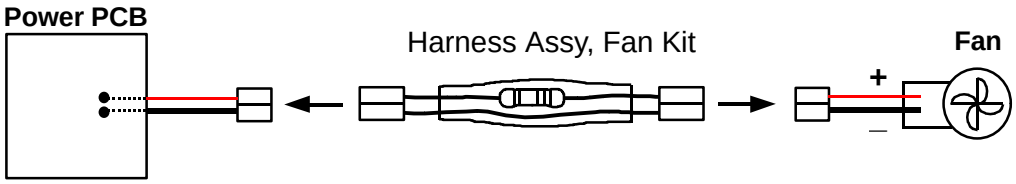
1. Insert series 33 Ω resistor to reduce the driving voltage of the fan.
   ⇒ See page 2 for the details.
2. The fan is mounted horizontally and isolated from the chassis by dampers.
   ⇒ See page 3 for the details.

Reducing the Driving Voltage

According to Tech-Info No. 9904, wiring between the Power PCB Assy and the cooling fan have been changed on the products S/No. 0070001 and higher. Therefore, procedure to insert 33 Ω resistor differs depending on the products serial number as following.

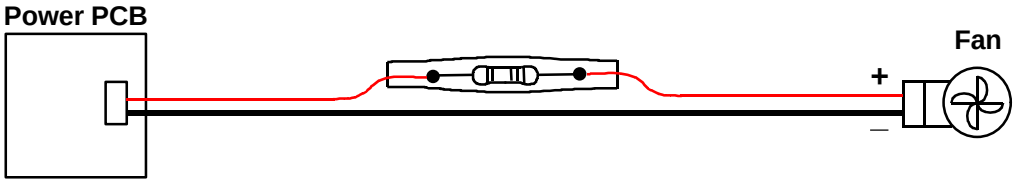
DA-45HR S/No. up to 0069999

Insert the Harness Assy, Fan Kit between the Power PCB Assy and the fan.



DA-45HR S/No. 0070001 to 0089999.

Take out 33 Ω resistor from the Harness Assy, Fan Kit. Or, use an equivalent 33 Ω (1/4W) resistor such as P/No. 51814460-00.
Cut the original red wire and solder 33Ω resistor there. Cover them with shrink tube.

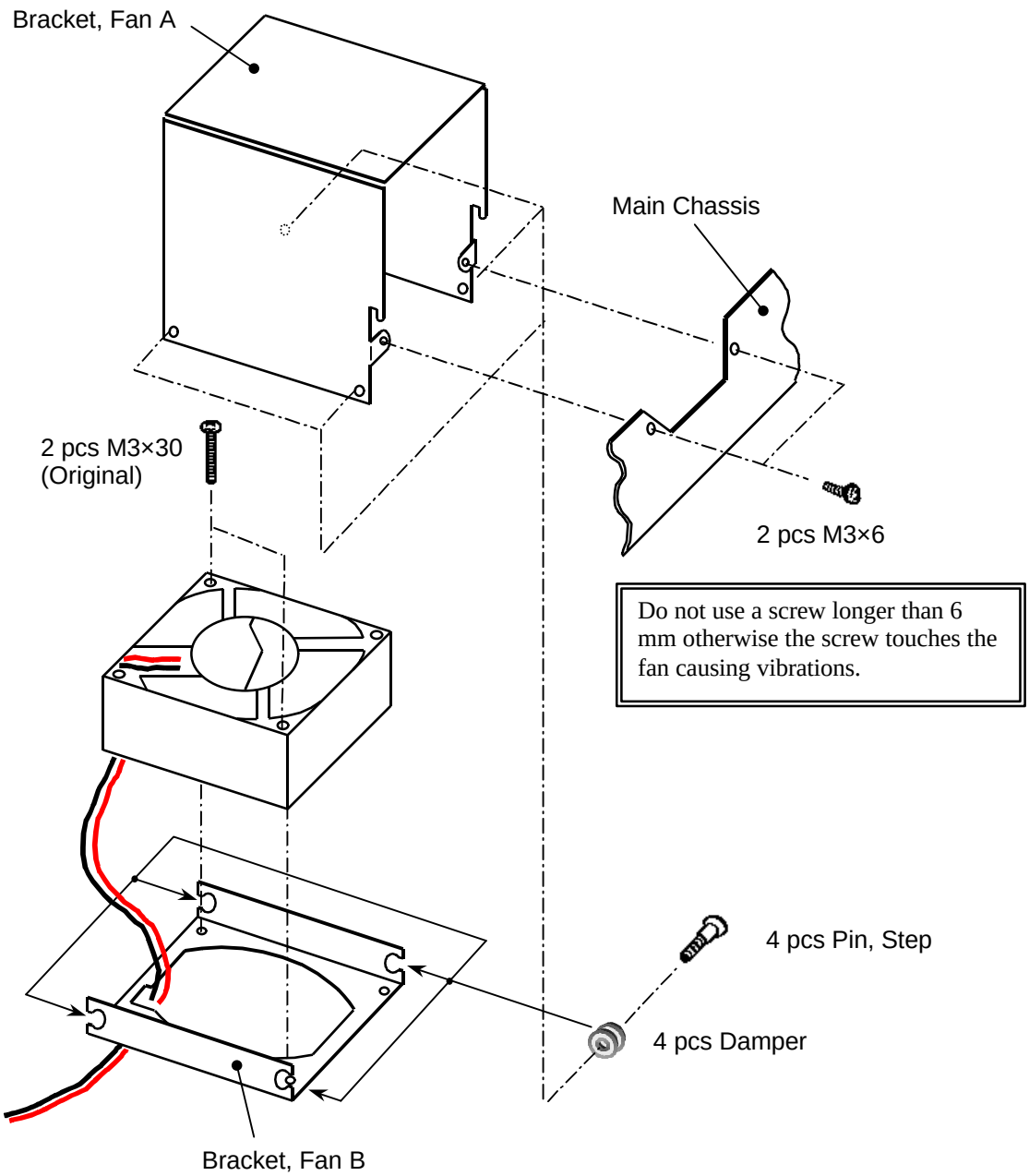


DA-45HR S/No. 0090001 and higher.

Bracket Kit, Fan DA-45HR has been mounted.
The 33 Ω resistor is mounted across a cut foil on the Power PCB Assy.
The resistor will be regularly mounted on the PCB in the future production.

Isolating the cooling fan from the chassis

Note:
Originally the cooling fan is fixed by 4 pcs of M3 × 30 screws. On the procedure below, abandon 2 pcs of them and use 2 pcs of M3 × 6 included in the kit.



TEAC **TECHNICAL INFORMATION**

TASCAM DA-45HR, Change of Cooling Fan

No. **9904**
DATE 5th March 1999

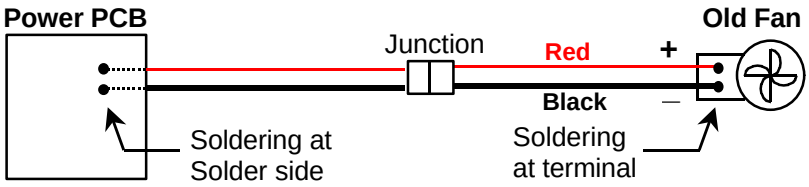
To improve the productivity, cooling fan and Power PCB Assy have been changed on the products S/No. 0070001 and higher.

	Old	New
Cooling fan	E005067-00A	E0051380
Power PCB Assy	E950742-00A [J] E950742-10A [US/C] E950742-40A [E, K, UK] E950742-60A [A]	E950742-00B [J] E950742-10B [US/C] E950742-40B [E, K, UK] E950742-60B [A]

Note: Old and new fan are completely same except that the old fan has lead wires soldered on the PCB and the new one has a plug-in connector.

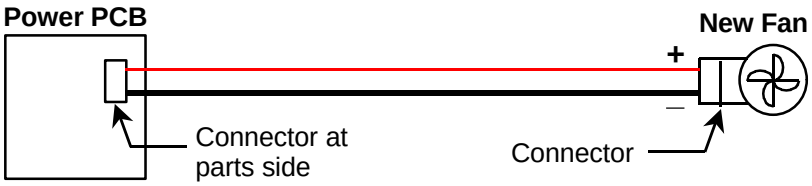
Old style

Power PCB Assy and cooling fan are connected with a junction connector.



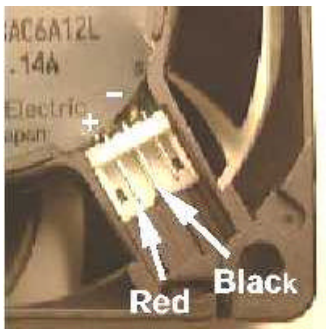
New style

Power PCB Assy and cooling fan are connected with connectors.



Note:

Only the new cooling fan is available for the spare part. When the new cooling fan is fitted to the old unit, remove the original wires from the old cooling fan and then solder these wires to the terminal of the new cooling fan as shown.



TEAC

TECHNICAL INFORMATION

TASCAM DA-45HR, Service Manual Correction

No. **9851**
DATE 18th December 1998

Corrections are required on the service manual (P/No. D004642-00A) as shown below.

	×	○
Page 36	EXPLODED VIEW-3	EXPLODED VIEW-4
Page 38	EXPLODED VIEW-4	EXPLODED VIEW-3

TEAC **TECHNICAL INFORMATION**

TASCAM DA-45HR, ROM Upgrade (SYS V1.10)

No. **9844**
DATE 20th November 1998

System ROM, U102 on the Main PCB Assy has been upgraded from V1.00 to V1.10 on the products with S/No. 0070001 and higher. New feature has been added.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.10	**S003157-00B**	**S0001133** (M27C1001-12C1)

*Use the PLCC 3232-11 (Advantech) ROM adapter to program the M27C1001-12C1. This ROM Adapter is the one being used for RC-898 (CONT) ROM.

Additional Feature

1) “DD” mode has been added in the menu of Auto ID level newly.

This allows the automatic recording of Start IDs based on the digital data from digital audio devices like CD or DAT machine through digital input coaxial connector.

Refer to supplement owner's manual P/No. **D004600-00A** attached.

A new setting has been added to the Auto ID level menu (3.2, “Auto ID level”).
This allows the automatic recording of START IDs based on the digital data received from digital audio devices connected through the DIGITAL INPUT COAXIAL [34] connector.

The menu options are now: -48dB, -54dB, -57dB, -60dB and dd. The dd setting detects the start of a track, as determined by the digital subcode, as opposed to the start of the audio material (the two may not be identical).
If a DAT deck is connected to the DA-45HR through the COAXIAL interface, the START IDs and SKIP IDs on the source deck are transferred over the coaxial connection and recorded on the DA-45HR.

If a CD player is connected, when the start of a track is read, a START ID is written on the DA-45HR with the same program number as the track number on the CD player.

Note that if an analog connection is made between the DA-45HR and a CD or DAT recorder, and recording is carried out through the analog connections, even if dd has been selected, the Auto ID level is automatically set to -54dB. This is also the case if a digital device other than a DAT recorder or a CD player is attached to the DA-45HR.

NOTE

- When recording in HR mode from a DAT recorded in standard (non-HR) mode, the start ID (normally 9 seconds in length) will be recorded at double speed (i.e. 4.5 seconds). Skip IDs (normally 1 second) will likewise be at double speed (0.5 seconds).

- CD tracks of less than 18 seconds may not have their corresponding START IDs recorded properly. In order to ensure accurate program searching, a gap of at least 9 seconds should be left between the end of one START ID and the beginning of the next.

TEAC **TECHNICAL INFORMATION**

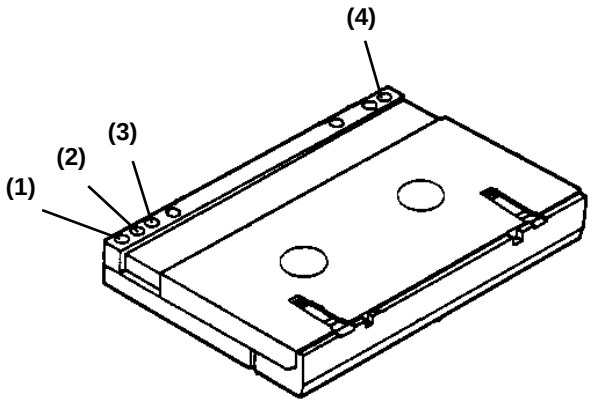
TASCAM DA-45HR / DA-40, Clearing Drum Time

No. **9840**
DATE 29th September 1998

Strictly Confidential

Drum time can be cleared by the following procedure.

1 Turn the power on.
2 Press MENU several times then "Drum T" "xxxx H" appears.
3 Insert a cassette of which a hole (3) is opened.
4 Wind a tape to EOT (End Of Tape).
5 Hold STOP then press MARGIN RESET and MENU simultaneously. Then "DrumT 0000H" appears on the display and starts counting.



TECHNICAL INFORMATION

TASCAM DA-40, ROM Upgrade (MAIN V1.11)

No. **0020**
DATE 12th July 2000

System ROM, U406 on the Main PCB Assy has been upgraded from V1.10 to V1.11 on the products with S/No. 0190001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.11	**S003320-00C**	**S0001133** (M27C1001-12C1)

* Use the PLCC 3232-11 (Advantech) ROM adapter to program the M27C1001-12C1.
This ROM Adapter is the one being used for RC-898 (CONT) ROM.

Problem Corrected by V1.10

Make analog recording with a consumer DAT.
Reproduce it with DA-40.
Consumer products such as DAT or MD cannot record the SPDIF out of the DA-40 and shows "recording prohibited". (According to the SPDIF regulation, they should record.)

Cause of problem is that the DA-40 outputs wrong category code in the C-bit.

AK5351

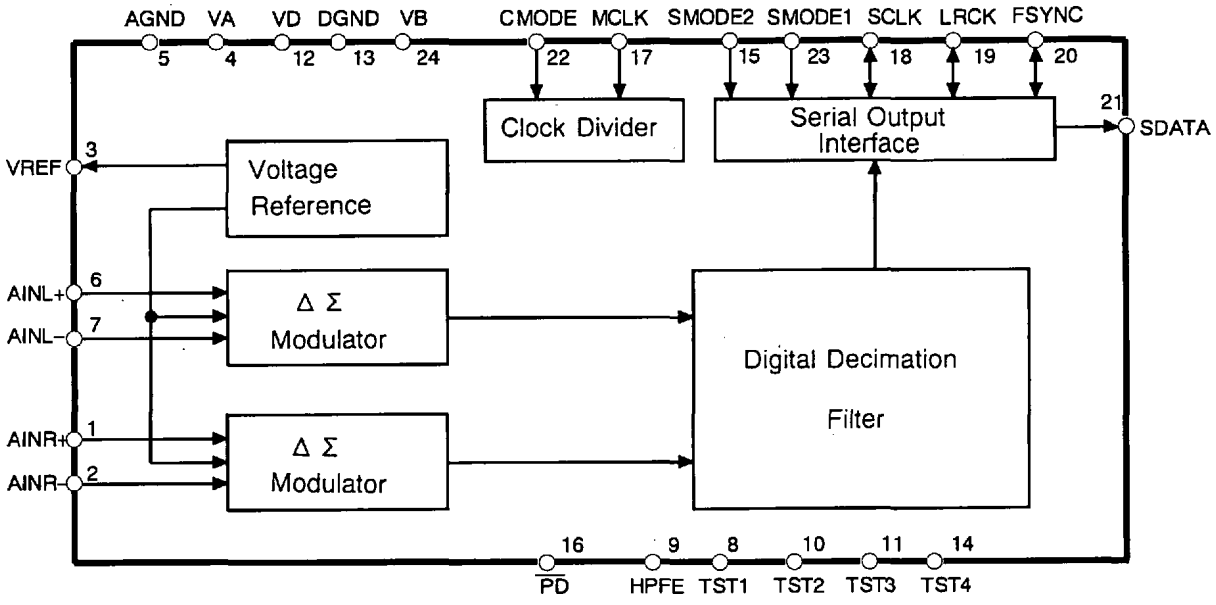
Enhanced Dual bit ΔΣ 20bit ADC

GENERAL DESCRIPTION

The AK5351 is a 20-bit, 64x oversampling rate(64fs), 2-channel A/D converter for stereo digital systems. The ΔΣ modulator in the AK5351 uses the new developed Enhanced Dual bit architecture. This new architecture achieves the wider dynamic range, while keeping much the same superior distortion characteristics as the conventional Single bit way. The AK5351 is suitable for digital surround and Hi-Fi audio application such as Car-audio, MD, etc. Analog inputs of the AK5351 are normally Full-differential inputs, while they are also acceptable Single-ended inputs.
The AK5351 is available in a small 24pin VSOP package which will reduce your system space.

FEATURES

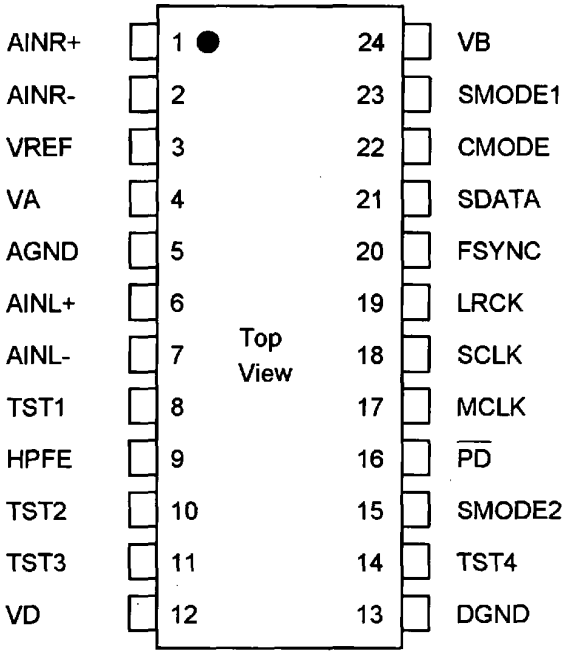
- ☐ Full-differential / Single-ended inputs
- ☐ S/(N+D): 97dB
- ☐ DR, S/N: 103dB
- ☐ Linear phase digital filter
  - Pass band: 0~22kHz(@fs=48kHz)
  - Pass band ripple: ±0.005dB
  - Stop band attenuation: 80dB
- ☐ Digital HPF for DC-offset cancel
- ☐ Master clock: 256fs/384fs
- ☐ Power supply: 5V±10%
- ☐ Small package: 24pinVSOP



■ Ordering Guide

AK5351-VF	-40~85°C	24pin VSOP
AKD5351/2	Evaluation Board	

■ Pin Layout



■ Replacement from AK5350 to AK5351

	AK5350	AK5351
Package	28VSOP	24VSOP *)Interchangeable with AK5350
Analog Inputs Voltage	±3.47Vp-p	±2.10Vp-p *)Acceptable Single-ended
fc of HPF(@fs=48kHz)	7Hz	1Hz
SCLK	~64fs	~128fs

PIN/FUNCTION

No.	Pin Name	I/O	FUNCTION
1	AINR+	I	Right channel analog positive input pin
2	AINR-	I	Right channel analog negative input pin
3	VREF	O	Voltage Reference output pin (VA-2.6V) Normally connected to VA with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic capacitor.
4	VA	-	Analog section Analog Power Supply, +5V
5	AGND	-	Analog section Analog Ground
6	AINL+	I	Left channel analog positive input pin
7	AINL-	I	Left channel analog negative input pin
8 10 11 14	TST1 TST2 TST3 TST4		Test pin (Pull-down pin) Should be left floating.
9	HPFE	I	High Pass Filter Enable pin (Pull-up pin) "H": ON "L": OFF
12	VD	-	Digital section Digital Power Supply pin, +5V
13	DGND	-	Digital section Digital Ground pin
16	$\overline{PD}$	I	Power Down pin "L" brings the device into power-down mode. Must be done once after power-on.
17	MCLK	I	Master Clock input pin CMODE="H":384fs CMODE="L":256fs
18	SCLK	I/O	Serial Data Clock pin Data is clocked out at the falling edge of SCLK. Slave mode: 64fs clock is input usually. Master mode: SCLK outputs a 64fs clock. SCLK stays low during the power-down mode($\overline{PD}$="L").
19	LRCK	I/O	L/R Channel Clock Select pin Slave mode: An fs clock is fed to this LRCK pin. Master mode: LRCK output an fs clock. LRCK goes "H" at SMODE2="L" and "L" at SMODE2="H" during reset when SMODE1 "H".
20	FSYNC	I/O	Frame Synchronization Signal pin Slave mode: When "H", data bits are clocked out on SDATA. As I^2S slave mode ignores FSYNC, it should hold "L" or "H". Master mode: FSYNC outputs 2fs clock. Stay low during the power-down mode($\overline{PD}$="L").

21	SDATA	O	Serial Data Output pin Data are output with MSB first, in 2's complement format. After 20 bits are output it turns to "L". It also remains "L" at a power-down mode($\overline{PD}$="L").
22	CMODE	I	Master Clock Selection pin "L": MCLK=256fs "H": MCLK=384fs
23 15	SMODE1 SMODE2	I I	Serial Interface Mode Select pin Defines the directions of LRCK, SCLK and FSYNC pins and Output Data Format. SMODE2 is pull-down pin. SMODE1 SMODE2 MODE LRCK L L Slave mode: MSB justified : H/L H L Master mode: Similar to I^2S : H/L L H Slave mode: I^2S : L/H H H Master mode: I^2S : L/H
24	VB	-	Substrate Power Supply, +5V

ABSOLUTE MAXIMUM RATINGS

(AGND,DGND=0V; Note 1)

Parameter	Symbol	min	max	Units
DC Power Supply:Analog Power(VA pin)	VA	-0.3	6.0	V
Digital Power(VD pin) (Note 2)	VD	-0.3	6.0/VB+0.3	V
Substrate Power(VB pin)	VB	-0.3	6.0	
Input Current (Any pin except supplies)	IIN	-	±10	mA
Analog Input Voltage AINL+,AINL-,AINR+,AINR-pins (Note 2)	VINA	-0.3	6.0/VA+0.3	V
Digital Input Voltage (Note 2)	VIND	-0.3	6.0/VB+0.3	V
Ambient Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1 : All voltage with respect to ground.

Note 2 : Absolute maximum value is the highest voltage in 6.0V, VA+0.3V and VB+0.3V.

WARNING: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND,DGND=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
DC Power Supplies: Analog Power	VA	4.50	5.0	5.50	V
Digital Power(VD pin)	VD	4.50	5.0	VB	V
(VB pin) (Note 3)	VB	4.50	5.0	5.50	V

Note 1 : All voltages with respect to ground.

Note 3 : The VA and VB are connected together through the chip substrate and have several ohms resistance. The VA and VB should be powered at the same time or earlier than VD.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA,VD,VB=5.0V; fs=48kHz; 20bit; Input signal frequency=1kHz,
Measurement Bandwidth=10Hz~20kHz; unless otherwise specified.)

Parameter	min	typ	max	Units
Resolution		20		Bits
Analog Input Characteristics (Analog source impedance: 330Ω)				
S/(N+D) (Note 4)	88	97		dB
Dynamic Range (A-weighted) (Note 5)	97	103		dB
S/N (A-weighted) (Note 6)	97	103		dB
Interchannel Isolation (f=1kHz)	100	120		dB
Interchannel Gain Mismatch		0.1	0.3	dB
Gain drift		±200		ppm/°C
Input Voltage Range	±1.97	±2.10	±2.23	Vp-p
Input Impedance	30	50		kΩ
Power Supplies				
Power Supply Current (Note 7)				
Normal Operation ($\overline{PD}$="H")				
VA+VB		15	25	mA
VD		6	9	mA
Power-Down mode ($\overline{PD}$="L")				
VA+VB		20		uA
VD		10		uA
Power Consumption (Note 7)				
Normal Operation		105	170	mW
Power-Down mode		150		uW
Power Supply Rejection Ratio		50		dB

Note 4 : The ratio of the rms value of the signal to the sum of all other spectral components up to 20kHz except for the signal (included harmonic component, excluded DC component, analog input signal is -0.5dB). Inversed of THD+N.

Note 5 : S/(N+D) with an input signal of 60dB below full-scale.

Note 6 : When using only 20kHzLPF, S/N and DR are 99dB(typ.). When using CCIR-ARM filter, S/N is 99dB(typ.)

Note 7 : Almost no current is supplied from VB pin.

DIGITAL FILTER CHARACTERISTICS

(Ta=25°C; VA,VD,VB=5.0V±10%; fs=48kHz)

Low Pass Filter characteristics	Symbol	min	typ	max	Units
Passband -0.005dB (Note 8)	PB	0		21.5	kHz
-0.02dB				21.768	
-0.06dB				22.0	
Stopband (Note 9)	SB	26.5			kHz
Passband Ripple (Note 10)	PR			±0.005	dB
Stopband Attenuation (Note 9 ,Note 11)	SR	80			dB
Group Delay Distortion	Δ GD			0	us
Group Delay (Note 12)	GD		29.3		1/fs
High Pass Filter characteristics					
Frequency Response -3dB(Note 8)	FR		1.0		Hz
-0.5dB			2.9		Hz
-0.1dB			6.5		Hz

Note 8 : These frequencies scale with the sampling frequency(fs).

Note 9 : Stopband is 26.5kHz to 3.0455MHz at fs=48kHz.

Note 10 : Passband is DC to 21.5kHz at fs=48kHz.

Note 11 : The analog modulator samples the input at 3.072MHz for a system sampling rate of fs=48kHz. These is no rejection of input signals at those bandwidths which are multiples of the sampling frequency (n x 3.072MHz ±22kHz ;n=0,1,2,3…).

Note 12 : The calculation delay time occurred by digital filtering. This is the time from the input of analog signal to setting the 20bit data of both channels to the output registers. GD=29.3/fs.

ELECTRICAL CHARACTERISTICS

■ Digital Characteristics

(Ta=25°C; VA,VD,VB=5.0V±10%)

Parameter	Symbol	min	typ	max	Units
High-Level Input voltage	V_{IH}	70%VD	-	-	V
Low-Level Input voltage	V_{IL}	-	-	30%VD	V
High-Level Output voltage Iout=-20uA	V_{OH}	VD-0.1	-	-	V
Low-Level Output voltage Iout=20uA	V_{OL}	-	-	0.1	V
Input Leakage Current (Note 13)	Iin	-	-	±10	uA

Note 13 : Except for pull-down and pull-up pins. TST1, TST2, TST3, TST4, SMODE2 pins have internal pull-down device, HPFE pin has internal pull-up devive(Typ. 50kΩ)

■ **SWITCHING CHARACTERISTICS**

(Ta=25°C; VA,VD,VB=5.0V±10%; C_L=20pF)

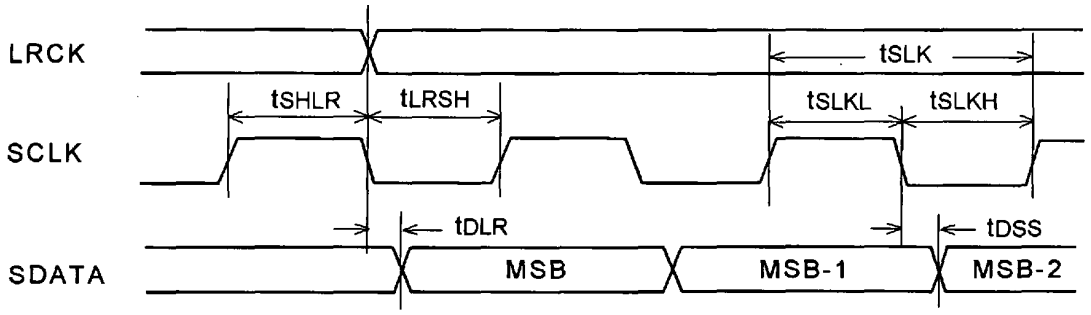
Parameter	Symbol	min	typ	max	Unit
Control Clock Frequency					
Master Clock 256fs:	f_{CLK}	2.048	12.288	13.824	MHz
Pulse width Low	t_{CLKL}	30.0			ns
Pulse width High	t_{CLKH}	30.0			ns
384fs:	f_{CLK}	3.072	18.432	20.736	MHz
Pulse width Low	t_{CLKL}	20.0			ns
Pulse width High	t_{CLKH}	20.0			ns
Serial Data Output Clock	f_{SLK}		3.072	6.912	MHz
Channel Select Clock(Sampling Frequency)	fs	8	48	54	kHz
Duty Cycle		25		75	%
Serial Interface Timing (Note 14)					
Slave Mode(SMODE1="L")					
SCLK Period	t_{SLK}	144.7			ns
SCLK Pulse width Low	t_{SLKL}	65			ns
Pulse width High	t_{SLKH}	65			ns
SCLK Rising to LRCK Edge (Note 15)	t_{SHLR}	30			ns
LRCK Edge to SCLK Rising (Note 15)	t_{LRSH}	30			ns
LRCK Edge to SDATA MSB Valid	t_{DLR}			50	ns
SCLK Falling to SDATA Valid	t_{DSS}			50	ns
SCLK Rising to FSYNC Edge(Note 15)	t_{SHF}	30			ns
FSYNC Edge to SCLK Rising(Note 15)	t_{FSH}	30			ns
Master Mode(SMODE1="H")					
SCLK Frequency	f_{SLK}		64fs		Hz
Duty Cycle			50		%
FSYNC Frequency	f_{FSYNC}		2fs		Hz
Duty Cycle			50		%
SCLK Falling to LRCK Edge	t_{SLR}	-20		20	ns
LRCK Edge to FSYNC Rising	t_{LRF}		1		tslk
SCLK Falling to SDATA Valid	t_{DSS}			50	ns
SCLK Falling to FSYNC Edge	t_{SF}	-20		20	ns
Power down timing					
$\overline{PD}$ Pulse width	t_{PDW}	150			ns
$\overline{PD}$ Rising to SDATA Valid (Note 16)	t_{PDV}		516		1/fs

Note 14 : Refer to Serial Data Interface.

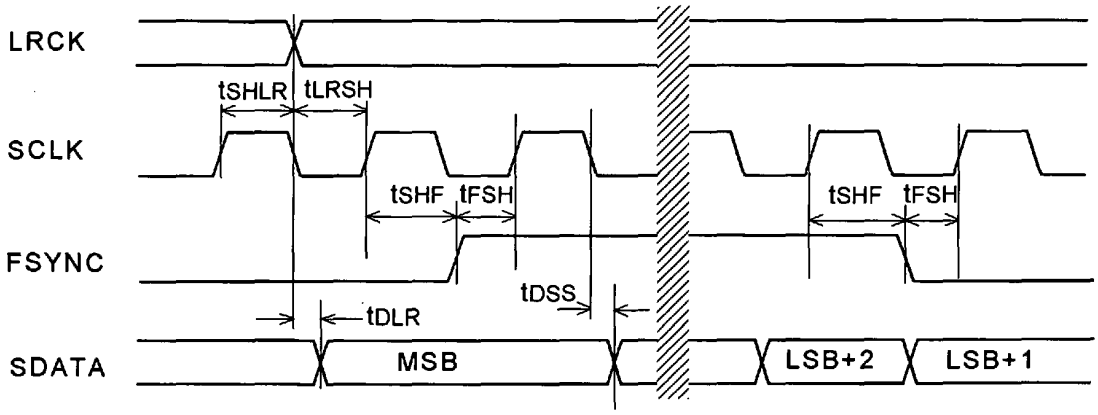
Note 15 : Specified LRCK and FSYNC edges not to coincide with the rising edges of SCLK.

Note 16 : The number of LRCK rising edges after $\overline{PD}$ brought high. The value is in master mode.
In slave mode it becomes one LRCK clock(1/fs) longer.

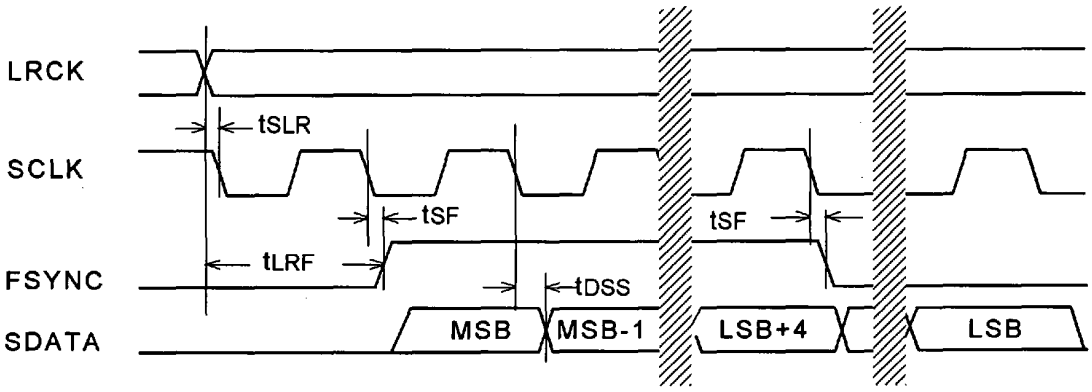
■ **Timing Chart**



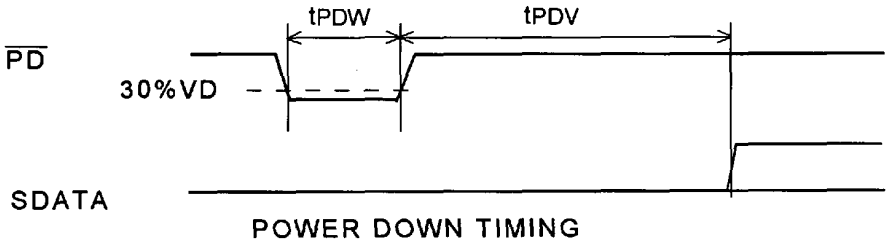
SERIAL DATA TIMING (SLAVE MODE, FSYNC = "H")



SERIAL DATA TIMING (SLAVE MODE)



SERIAL DATA TIMING (MASTER MODE)



POWER DOWN TIMING

OPERATION OVERVIEW

■ System clock

In slave mode, MCLK(256fs/384fs), LRCK(fs) and SCLK(64fs) are required for AK5351. Use a signal divided from the MCLK for LRCK. In master mode, only MCLK is needed. A LRCK clock rate meets standard audio rates (32kHz, 44.1kHz, 48kHz). In slave mode, the MCLK should be synchronized with LRCK but the phase is free of care.

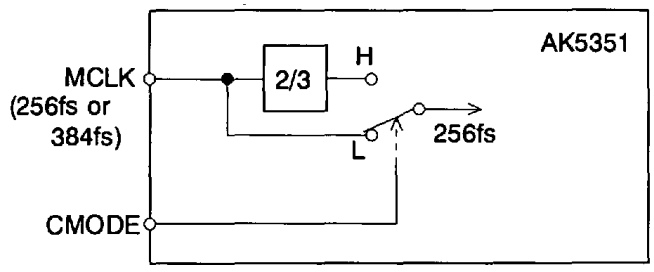
The AK5351 includes the phase detect circuit for LRCK clock, the AK5351 is reset automatically when the synchronization is out of phase by changing the clock frequencies. (Please refer to the "Asynchronization - reset."). When changing sampling frequency(fs) after power-up, AK5351 should be reset.

During the operation ($\overline{PD}$="H") following external clocks should never be stopped : CLK in master mode and MCLK, SCLK and LRCK in slave mode. When the clocks stop there is a possibility that the device comes into a malfunction because of over currents in the dynamic logic. If the external clocks are not present, the AK5351 should be in the power-down mode. ($\overline{PD}$="L")

fs	Master Clock (MCLK)		SCLK(64fs)
	256fs	384fs	
32.0kHz	8.1920MHz	12.2880MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	3.0720MHz

Table 1 . System Clock

■ Clock Circuit



CMODE	MCLK
L	256fs
H	384fs

AK5351 has an internal divider as shown in the above figure. The device can interface either or an external MCLK(256fs or 384fs) by controlling CMODE pin.

■ **Serial Data Interface**

Audio Serial Interface has four kinds of mode, it can be changed by SMODE1 and SMODE2 pins. Data format is MSB first, 2's complement.

Figure	SMODE1	SMODE2	Mode	L/R polarity
Figure 1	L	L	Slave Mode: 20bit, MSB justified	Lch=H, Rch=L
Figure 2	H	L	Master Mode: Similar to I^2S	Lch=H, Rch=L
Figure 3	L	H	Slave Mode: I^2S	Lch=L, Rch=H
Figure 4	H	H	Master Mode: I^2S	Lch=L, Rch=H

Table 2 . Serial Interface

1) SLAVE mode

An output channel is defined by LRCK. Both channel data are output in sequence, in order of the Lch first then Rch at the rate of fs. Data bits are clocked out via the SDATA pin at SCLK rate. Figure 1 and Figure 3 shows data output timing at SCLK=64fs. FSYNC enables SCLK to start clocking out data. The MSB is clocked out by the LRCK edge. SCLK causes the ADC to output succeeding bits when FSYNC is high. However, as I^2S slave mode ignores FSYNC, it should hold "L" or "H".

2) MASTER mode

In MASTER mode, the A/D converter is driven from a master clock(MCLK:256fs/384fs) and outputs all other clocks(LRCK, SCLK). The falling edge of SCLK causes the ADC to output each bit. Figure 2 and Figure 4 shows the output timing. 2x fs clock of 50% duty is output via the FSYNC pin. FSYNC rises one SCLK cycle after the transition of LRCK edges and stays high during 16 serial clocks(16*t_{SLK}). Upper 16 bit data is output during FSYNC "H", lower 4 bit is output after FSYNC "L" transition.

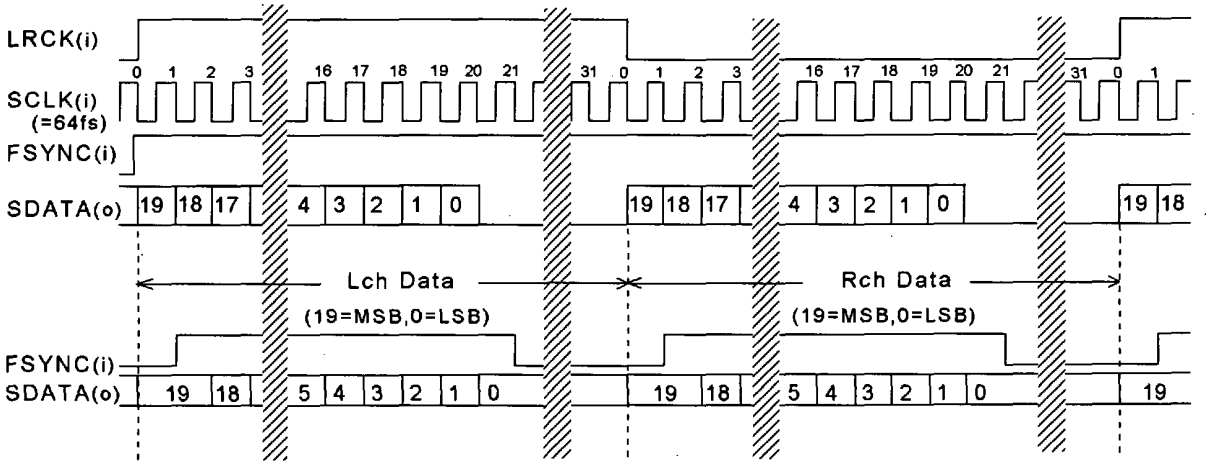


Figure 1 . Data Output Timing (Slave mode)

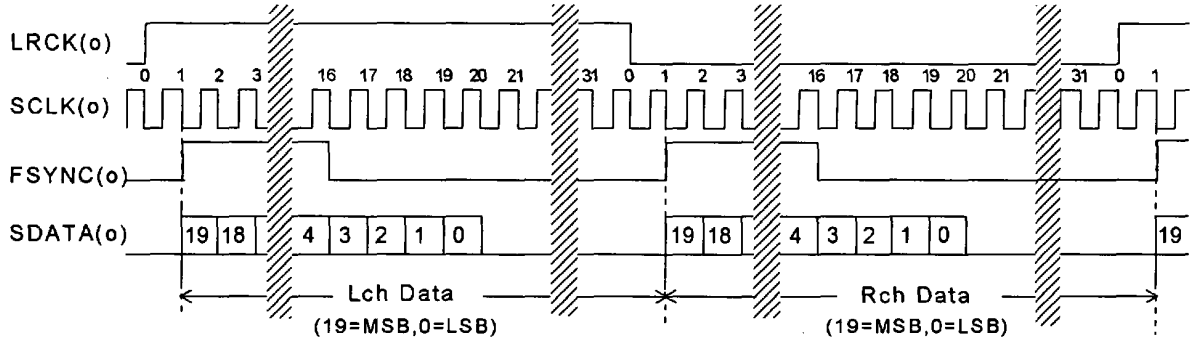


Figure 2. Data Output Timing(Master mode)

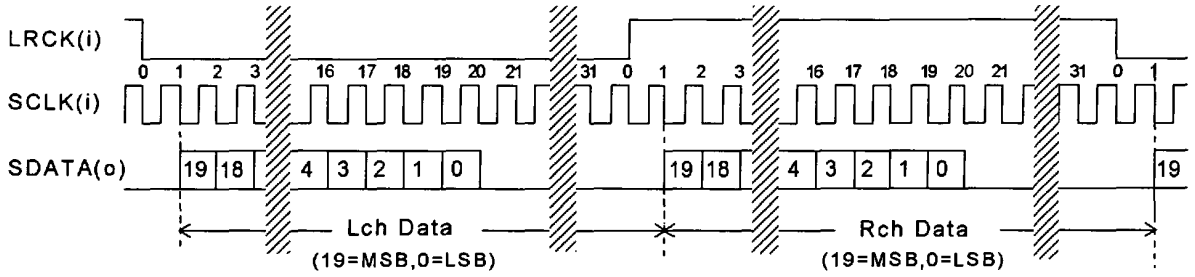


Figure 3. Data Output Timing(I ² S Slave mode)

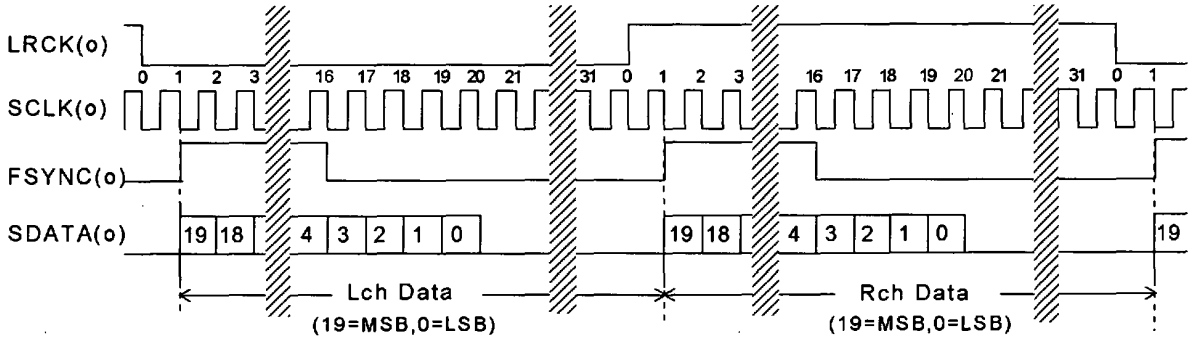


Figure 4. Data Output Timing (I ² S Master mode)

■ **Power-down mode**

The AK5351 has to be reset once by bringing $\overline{PD}$ "L" upon power-up. All internal registers of the digital filter and so on in the AK5351 are reset by this operation. When exiting the power-down mode($\overline{PD}$="H"), the internal timing starts clocking by first MCLK "↑"(rising edge). In master mode internal counter starts at once, in slave mode internal counter starts after synchronizing with the first rising edge of LRCK. The serial output data is available after 516 counting clock of LRCK cycle.

■ **Asynchronization-reset**

In slave mode, if the phase difference between LRCK and internal control signals is larger than +1/16~-1/16 of word period(1/fs), the synchronization of internal control signals with LRCK is done automatically at the first rising edge of LRCK.

■ **High Pass Filter(HPFE pin)**

The AK5351 has a Digital High Pass Filter(HPF) for DC-offset cancel. When HPFE pin goes "H", HPF is enabled. The cut-off frequency of the HPF is 1Hz(@fs=48kHz). It also scales with the sampling frequency(fs). The HPF can be disabled by bringing HPFE pin "L". In this case, the AK5351 has the DC-offset of a few mV.

SYSTEM DESIGN

Figure 5 shows the system connection diagram. Figure 6 and Figure 7 shows the input buffer circuit. An evaluation board[AKD5351/2] is available which demonstrates the optimum layout, power supply arrangement and measurement results.

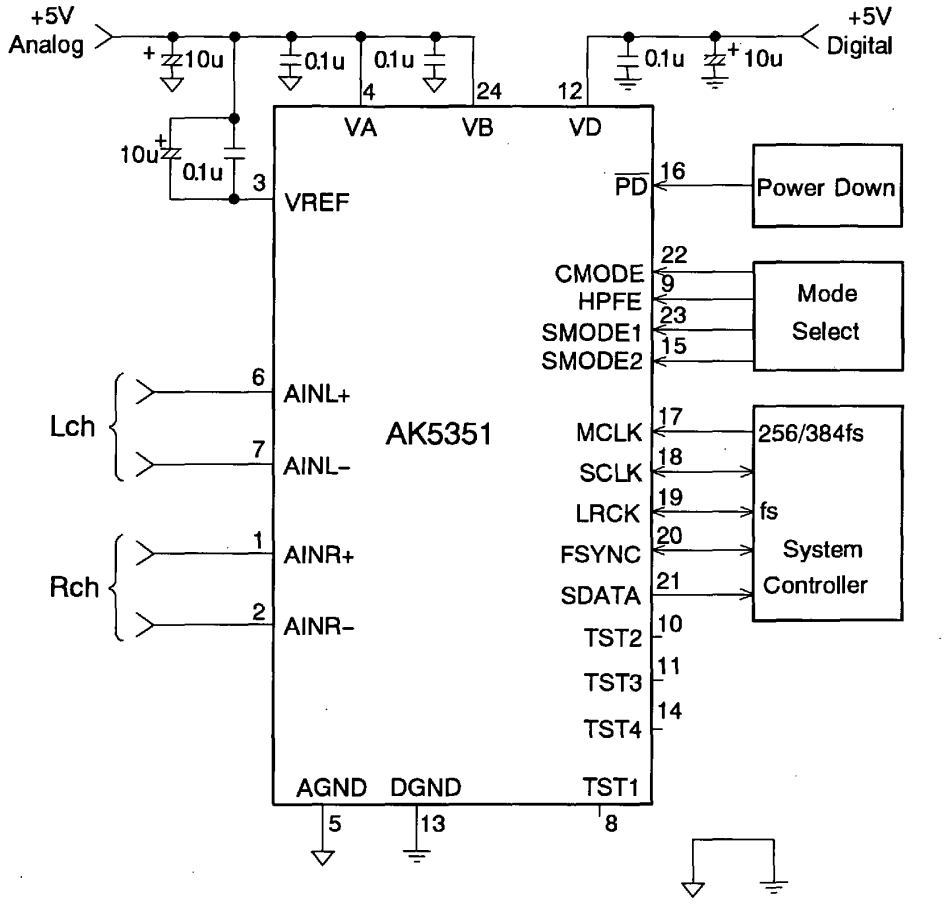


Figure 5 . System Connection Diagram Example

NOTE: +5V Analog should be powered the same time or earlier than +5V Digital.

■ Grounding and Power Supply Decoupling

The AK5351 requires careful attention to power supply and grounding arrangements. The VA and VB are connected together through the chip substrate and have several ohm resistance. The power to VB should come up at the same time or faster than the power to VD, when they are fed separately to the device (Figure 5). As to the connections of decoupling capacitors, refer to Figure 5 . The 0.1uF of decoupling capacitors connected power supply pins should be as near as possible to the power supply pin.

As AIN± pins is near VD pin, ground pattern should be inserted between VD line and AINL± lines to avoid digital noise coupling. Refer to evaluation board manual of AKD5352/1 Rev.B about board layout.

■ Analog connections

Analog signal is differentially input into the modulator via the AIN+ and the AIN- pins. The input voltage is the difference between AIN+ and AIN- pins. The full-scale of each pin is ±2.10Vp-p on its reference voltage(VREF). In case that the positive input is more than its full-scale, the AK5351 outputs positive 7FFFFH(Hex, Full-scale). In case that the negative input is more than its full-scale, the AK5351 outputs negative 80000H(Hex, Full-scale). Analog inputs of the AK5351 are normally Full-differential inputs, while they are also acceptable Single-ended inputs. In case of Single-ended inputs, analog signal is input from either positive or negative input and the other side inputs bias voltage. Figure 7 is a circuit example which analog input signal is input 4.20Vp-p into AIN- pin and bias voltage into AIN+ pin. The DC offset is removed by the internal HPF.

AK5351 samples the analog inputs at 3.072MHz with fs=48kHz. The digital filter rejects all noise between 26.5kHz and 3.0455MHz. However, the filter will not reject frequencies right around 3.072MHz (and multiples of 3.072MHz). Most audio signals do not have significant noise energy at 3.072MHz. Hence, a simple RC filter is sufficient to attenuate any noise energy at 3.072MHz.

The reference voltage for A/D converter is supplied from the VREF pin at VA reference. In order to eliminate the effects of high frequency noise on the VREF pin, a 10uF or less electrolytic capacitor and a 0.1uF ceramic capacitor should be connected parallel between the VREF and the VA pins. No current should be driven from the VREF pin.

The AK5351 accepts +5V supply voltage. Any voltage which exceeds the upper limit of (VA+)+0.3V and lower limit of AGND-0.3V and any current beyond 10mA for the analog input pins(AINL±, AINR±) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits.
Use caution specially in case of using ±15V in surrounding analog circuit.

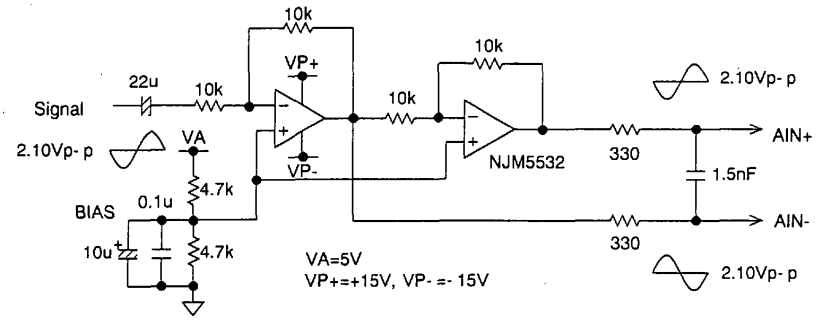


Figure 6 . Full-differential Input Buffer Circuit Example

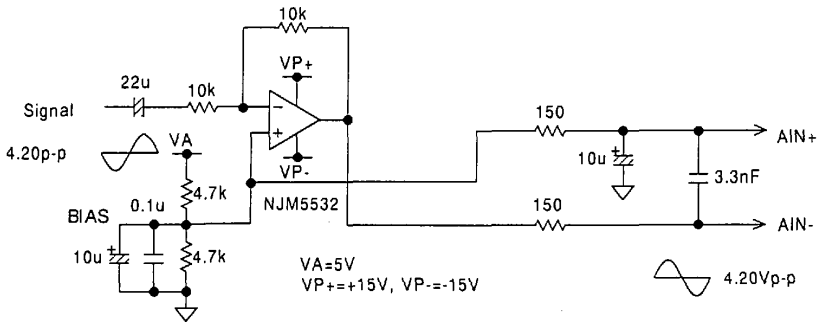


Figure 7 . Single-ended Input Buffer Circuit Example

■ **Digital Connections**

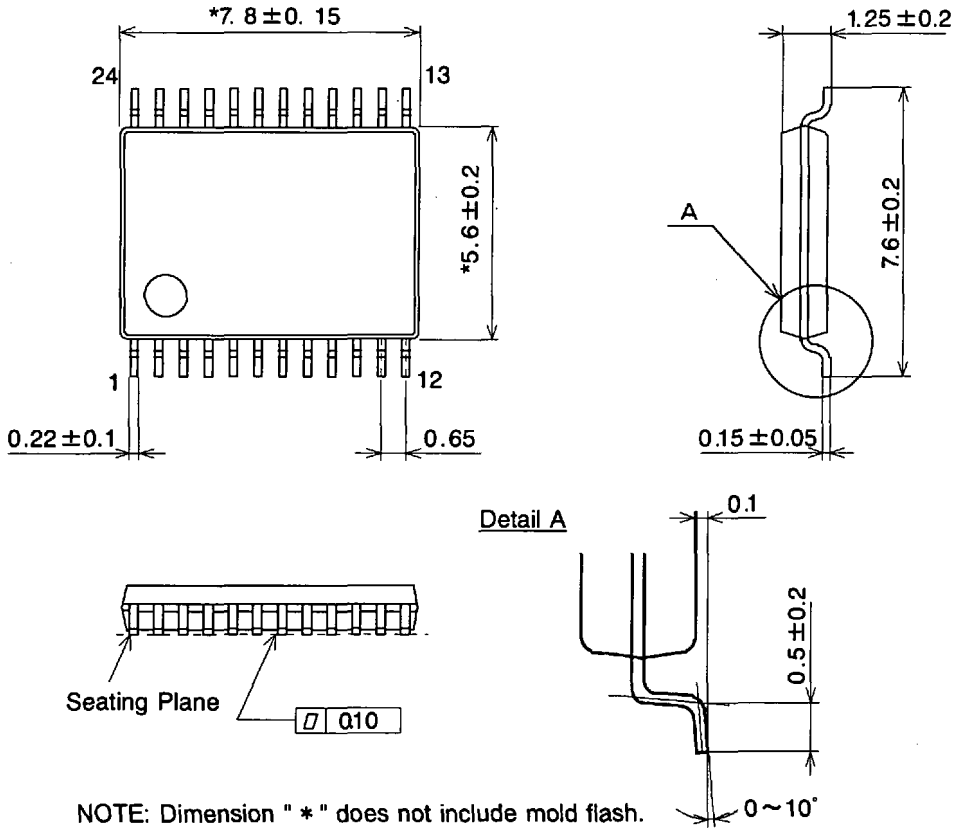
To minimize digital originated noise, connect the ADC digital outputs only to CMOS inputs. Logic families of 4000B, 74HC, 74AC, 74ACT and 74HCT series are suitable.

■ **Multiple AK5351**

In systems where multiple ADC's are required, care must be taken to insure the internal clocks are synchronized between converters to make simultaneous sampling. In slave mode, synchronous sampling is achieved by supplying the same MCLK and LRCK to all converters. In master mode, the same $\overline{PD}$ signal is supplied to each ADC. The $\overline{PD}$ state is released at the first rising edge of MCLK after bringing $\overline{PD}$ into high. Hence, if the rising edge of $\overline{PD}$ and rising edge of MCLK coincides together the sampling difference among the ADC's modulator would occur. The difference could be 1/256fs in the sampling clock(64fs) of the modulator, typically 81ns at fs=48kHz.

PACKAGE

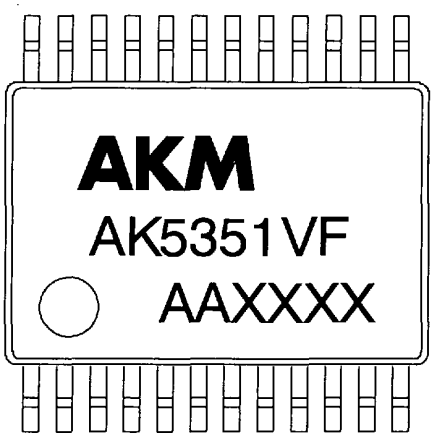
● **24pin VSOP (Unit: mm)**



■ **Material & Lead finish**

Package: Epoxy
Lead-frame: Copper
Lead-finish: Soldering plate

MARKING



Contents of AAXXXX

AA: Lot#

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NIPPON PRECISION CIRCUITS INC.

SM5843A×1

Audio Multi-function Digital Filter

OVERVIEW

The SM5843A×1 is a multi-function digital filter IC, fabricated using NPC's Molybdenum-gate CMOS process, for digital audio reproduction equipment. It features 8-times oversampling (interpolation), digital deemphasis and soft muting functions. It accepts 16, 18, or 20-bit input data, and outputs data in 18 or 20-bit format. It operates using either a 384fs or 256fs system clock.

FEATURES

- Filter configuration (2-channel processing)
  - 8-times oversampling (interpolation)
    - 3-stage FIR configuration
  - Deemphasis filter
    - IIR filter configuration for correct gain and phase characteristics
    - 2-channel independent ON/OFF control
    - 32/44.1/48 kHz sampling frequency (fs)
  - 21 × 22-bit parallel multiplier/25-bit accumulator for high precision
  - Overflow limiter
- 2 oversampling filter characteristics
  - Sharp roll-off characteristic (response 1)
    - ≤ ±0.00005 dB passband ripple (0 to 0.4535fs)
    - ≥ 110 dB stopband attenuation (0.5465fs to 7.4535fs)
  - Slow roll-off characteristic (response 2)
    - ≤ ±0.00003 dB passband ripple (0 to 0.235fs)
    - ≥ 77 dB stopband attenuation (0.745fs to 7.255fs)
- Soft muting
- Digital attenuator
- Input data format
  - 2s complement, MSB first
    - LR alternating, 16/18/20-bit serial, trailing data
    - LR alternating, 20-bit serial, leading data
    - LR simultaneous, 20-bit serial, leading data
- Output data format
  - 2s complement, MSB first, LR simultaneous
  - 18/20-bit serial
  - BCKO burst (NPC format)
- Dither processing ON/OFF control
- Jitter-free/Sync mode selectable
- 256fs/384fs system clock selectable
  - 21.2/14.2MHz maximum frequency (384fs/256fs)
- 5 V supply
- Crystal oscillator circuit built-in
- TTL-compatible input/outputs
- 28-pin plastic DIP and SOP
- Molybdenum-gate CMOS

APPLICATIONS

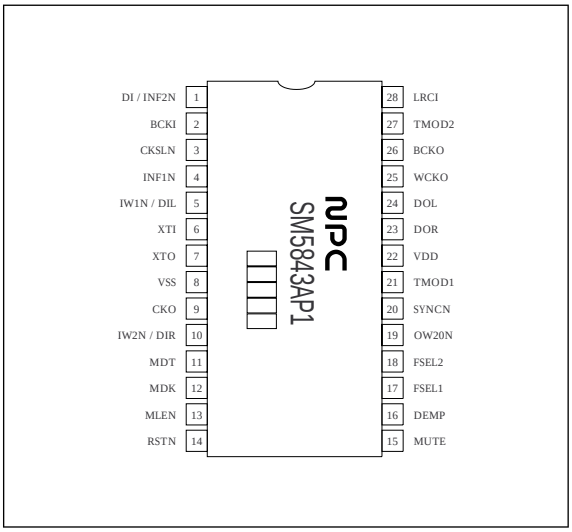
- CD players
- DAT players
- PCM systems

ORDERING INFOMATION

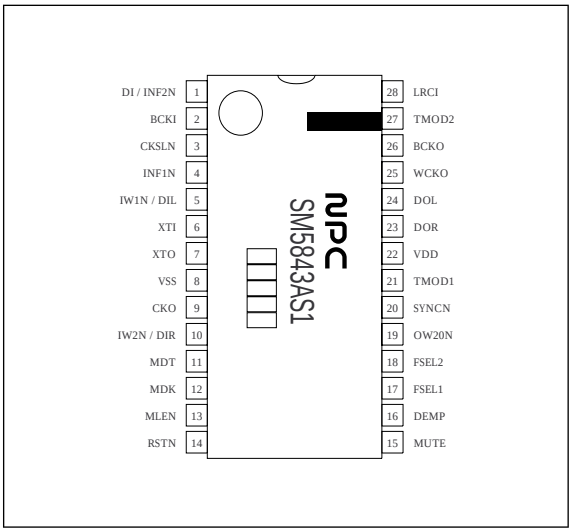
Device	Package
SM5843AP1	28pin DIP
SM5843AS1	28pin SOP

PINOUT(TOP VIEW)

28-pin DIP

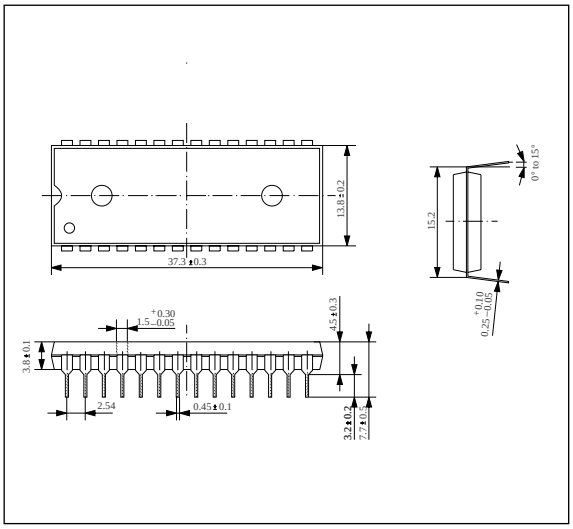


28-pin SOP

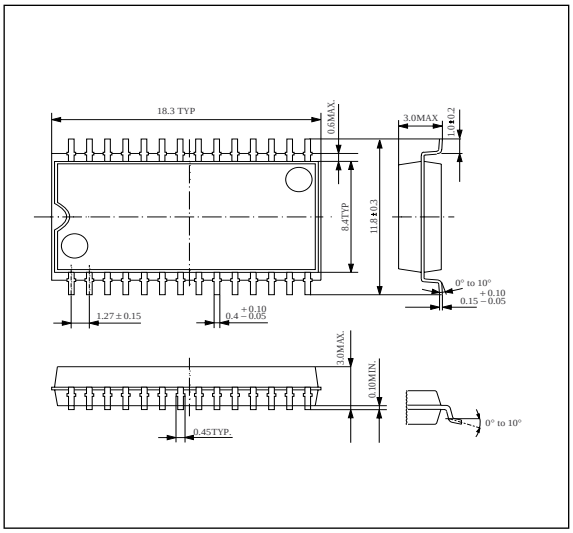


PACKAGE DIMENSIONS(Unit: mm)

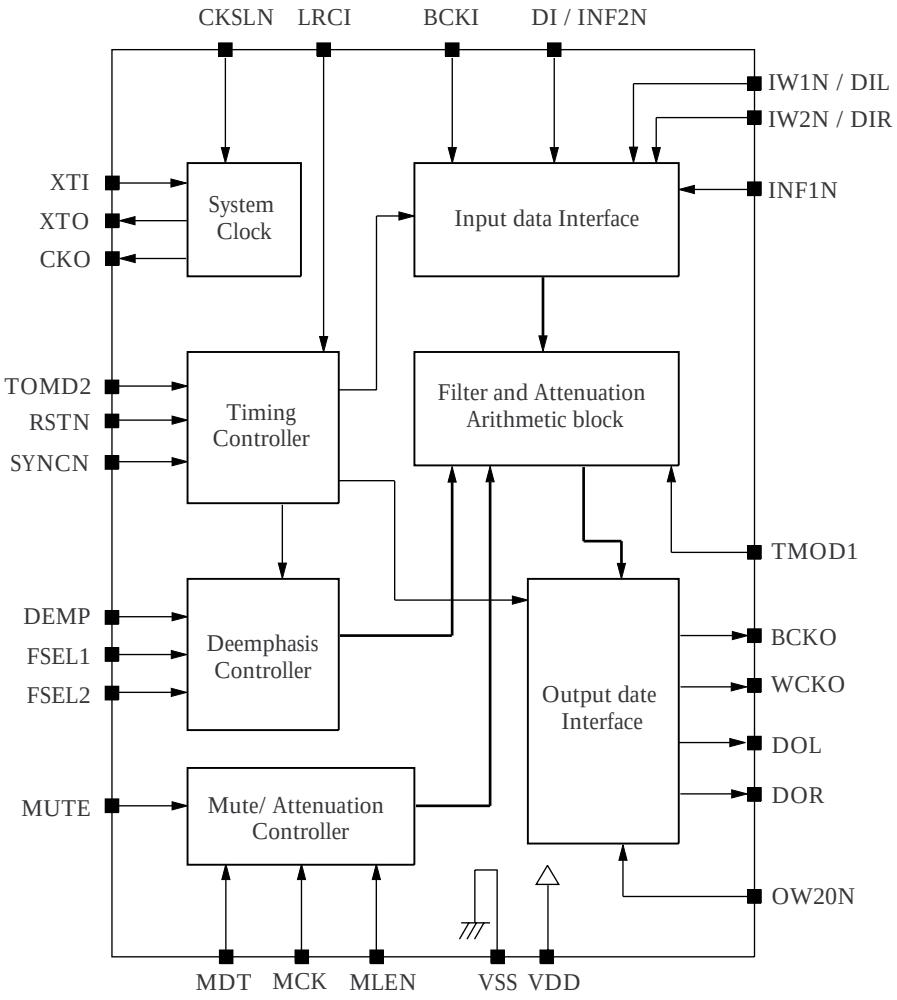
28-pin DIP



28-pin SOP



BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Number</th><th>Name</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>1</td><td>DI/INF2N</td><td>Ip</td><td>Data input when INF1N is LOW, and input format select pin when INF1N is HIGH.</td></tr>
<tr><td>2</td><td>BCKI</td><td>Ip</td><td>Input bit clock</td></tr>
<tr><td>3</td><td>CKSLN</td><td>Ip</td><td>Oscillator and system clock select input. 384fs when HIGH, and 256fs when LOW.</td></tr>
<tr><td>4</td><td>INF1N</td><td>Ip</td><td>Input format select pin. INF1N and INF2N select the pin functions below.
<table>
<tr><th rowspan="2">INF1N</th><th rowspan="2">DI/INF2N</th><th rowspan="2">Input format</th><th colspan="3">Pin function selection</th></tr>
<tr><th>DI/INF2N</th><th>IW1N/DIL</th><th>IW2N/DIR</th></tr>
<tr><td>LOW</td><td>LOW</td><td rowspan="2">LR alternating, trailing data</td><td rowspan="2">DI</td><td rowspan="2">IW1N</td><td rowspan="2">IW2N</td></tr>
<tr><td>LOW</td><td>HIGH</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>LR alternating, leading data</td><td rowspan="2">INF2N</td><td rowspan="2">DIL</td><td rowspan="2">DIR</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>LR simultaneous, leading data</td></tr>
</table></td></tr>
<tr><td>5</td><td>IW1N/DIL</td><td>Ip</td><td>Input bit length select pin when INF1N is LOW, and left-channel data input when INF1N is HIGH. IW1N and IW2N select the input data length.
<table>
<tr><th>INF1N</th><th>IW2N/DIL</th><th>IW1N/DIR</th><th>Input bit length</th></tr>
<tr><td rowspan="4">LOW</td><td>LOW</td><td>LOW</td><td>20 bits</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>20 bits</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>18 bits</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>16 bits</td></tr>
<tr><td>HIGH</td><td>×</td><td>×</td><td>20 bits</td></tr>
</table></td></tr>
<tr><td>6</td><td>XTI</td><td>I</td><td>Oscillator input connection</td></tr>
<tr><td>7</td><td>XTO</td><td>O</td><td>Oscillator output connection</td></tr>
<tr><td>8</td><td>VSS</td><td>–</td><td>Ground</td></tr>
<tr><td>9</td><td>CKO</td><td>O</td><td>Oscillator output clock. Same frequency as XTI.</td></tr>
<tr><td>10</td><td>IW2N/DIR</td><td>Ip</td><td>Input bit length select pin when INF2N is LOW, and right-channel data input when INF2N is HIGH. IW1N and IW2N select the input data length as shown in the table for pin 5.</td></tr>
<tr><td>11</td><td>MDT</td><td>Ip</td><td>Attenuator serial data input</td></tr>
<tr><td>12</td><td>MCK</td><td>Ip</td><td>Attenuator bit clock input</td></tr>
<tr><td>13</td><td>MLEN</td><td>Ip</td><td>Attenuator latch enable input</td></tr>
<tr><td>14</td><td>RSTN</td><td>Ip</td><td>System reset. Reset operation when LOW, and normal operation when HIGH.</td></tr>
<tr><td>15</td><td>MUTE</td><td>Ip</td><td>Mute control signal. Muting when HIGH, and normal operation when LOW.</td></tr>
<tr><td>16</td><td>DEMP</td><td>Ip</td><td>Deemphasis control signal. OFF when LOW, and ON when HIGH.</td></tr>
<tr><td>17</td><td>FSEL1</td><td>Ip</td><td rowspan="2">Deemphasis filter select inputs
<table>
<tr><th>FSEL1</th><th>FSEL2</th><th>Sampling frequency (fs)</th></tr>
<tr><td>LOW</td><td>LOW</td><td>44.1 kHz</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>48 kHz</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>Test mode</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>32 kHz</td></tr>
</table></td></tr>
<tr><td>18</td><td>FSEL2</td><td>Ip</td></tr>
<tr><td>19</td><td>OW20N</td><td>Ip</td><td>Output bit length select pin. 20-bit output when LOW, and 18-bit output when HIGH.</td></tr>
<tr><td>20</td><td>SYNCN</td><td>Ip</td><td>Sync mode select pin. Normal sync mode when LOW, and jitter-free mode when HIGH.</td></tr>
<tr><td>21</td><td>TMOD1</td><td>Ip</td><td>Dither processing control. ON when LOW, and OFF when HIGH.</td></tr>
<tr><td>22</td><td>VDD</td><td>–</td><td>5 V supply</td></tr>
</table>

Number	Name	I/O[1]	Description
23	DOR	O	Right-channel data output
24	DOL	O	Left-channel data output
25	WCKO	O	Output word clock
26	BCKO	O	Output bit clock
27	TMOD2	Ip	Filter characteristic select pin. Sharp roll-off (response 1) when HIGH, and slow roll-off (response 2) when LOW.
28	LRCI	Ip	Input data sample rate (fs) clock

1. I = input, Ip = Input with pull-up resistor, O = output

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	550 (DIP)	mW
		390 (SOP)	
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

fs = 384fs (CKSLN = HIGH): V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.5 to 5.5	V
Operating temperature range	T_{opr}	–20 to 80	°C

fs = 256fs (CKSLN = LOW): V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.75 to 5.25	V
Operating temperature range	T_{opr}	–20 to 70	°C

DC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 5.0 V[1]	–	50	65	mA
XTI HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
XTI AC-coupled input voltage	V_{INAC}		0.3V_{DD}	–	–	V_{p-p}
HIGH-level input voltage[2]	V_{IH2}		2.4	–	–	V
LOW-level input voltage[2]	V_{IL2}		–	–	0.5	V
HIGH-level output voltage[3]	V_{OH}	I_{OH} = –0.4 mA	2.5	–	–	V
LOW-level output voltage[3]	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH}	V_{IN} = V_{DD}	–	10	20	µA
XTI LOW-level input current	I_{IL1}	V_{IN} = 0 V	–	10	20	µA
LOW-level input current[2]	I_{IL2}	V_{IN} = 0 V	–	10	20	µA
Input leakage current[2]	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA

1. f_{SYS} = 256fs = 14.2 MHz (CKSLN = LOW), no output load
2. Pins DI/INF2N, BCKI, CKSLN, INF1N, IW1N/DIL, IW2N/DIR, MDT, MCK, MLEN, RSTN, MUTE, DEMP, FSEL1, FSEL2, OW20N, SYNCN, LRCI, TMOD1, TMOD2
3. Pins CKO, DOL, DOR, BCKO, WCKO

AC Electrical Characteristics

Input Clock (XTI)

Crystal oscillator

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	2.0	–	21.2	MHz

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	1.0	–	14.2	MHz

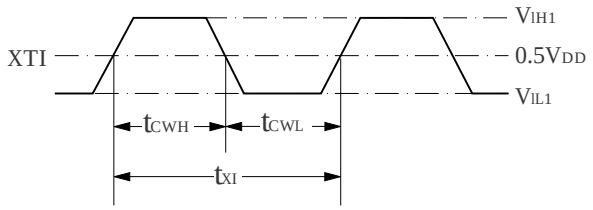
External clock input

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	20	–	250	ns
Clock LOW-level pulsewidth	t_{CWL}	20	–	250	ns
Clock pulse cycle time	t_{XI}	47	–	500	ns

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 70 °C

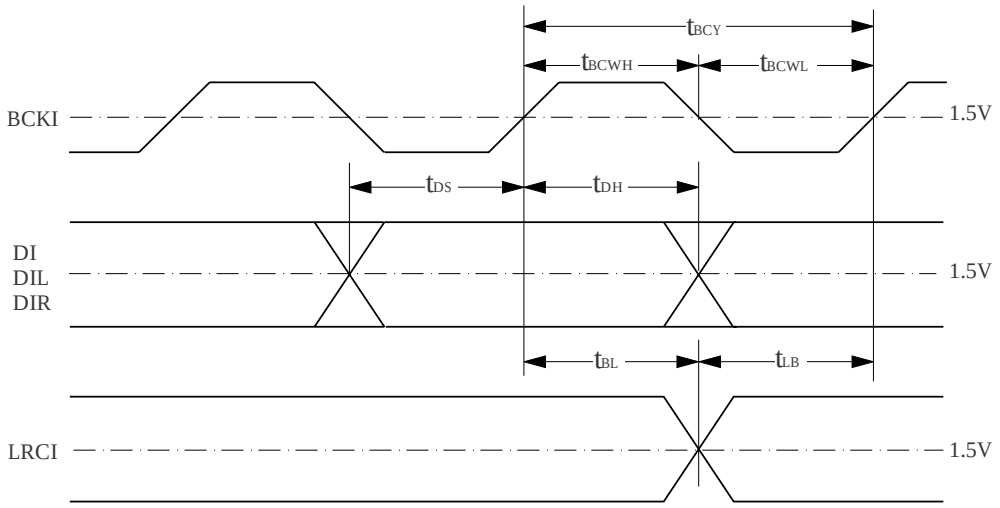
Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	30	–	500	ns
Clock LOW-level pulsewidth	t_{CWL}	30	–	500	ns
Clock pulse cycle time	t_{XI}	70	–	1000	ns



Serial input timing (BCKI, DI, DIL, DIR, LRCI)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI pulse cycle	t_{BCY}	100	–	–	ns
DIN setup time	t_{DS}	50	–	–	ns
DIN hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns



Reset timing (RSTN)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

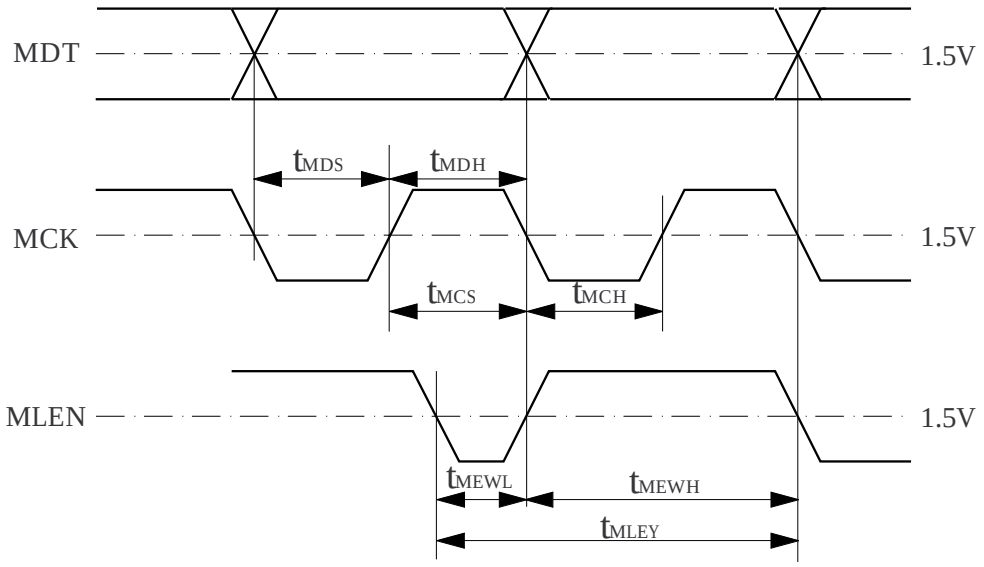
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{RST}$ LOW-level reset pulsewidth	t_{RST}	At power-ON	1	–	–	µs
		At all other times	50	–	–	ns

Attenuator timing (MDT, MCK, MLEN)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
MDT setup time	t_{MDS}	20	–	–	ns
MDT hold time	t_{MDH}	20	–	–	ns
MLEN setup time	t_{MCS}	40	–	–	ns
MLEN hold time	t_{MCH}	20	–	–	ns
MLEN LOW-level pulsewidth	t_{MEWL}	20	–	–	ns
MLEN HIGH-level pulsewidth	t_{MEWH}	20	–	–	ns
MLEN pulse cycle time	t_{MLEY}	6	–	–	t_{SYS}[1]

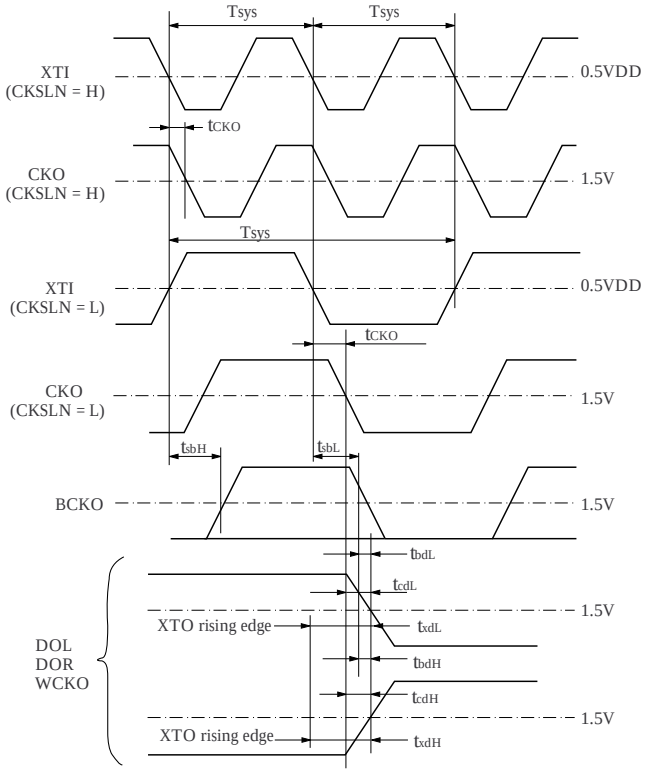
1. t_{SYS} = 1/384fs when CKSLN is HIGH, and 1/256fs when CKSLN is LOW.



Output timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C, C_L = 15 pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI to XTO delay	t_{XTO}	XTI fall to XTO rise	3	–	15	ns
XTI to CKO delay	t_{CKO}	XTI fall to CKO fall	10	–	35	ns
XTI to BCKO delay (CKSLN = HIGH)	t_{sbH}	XTI fall to BCKO rise	20	–	60	ns
	t_{sbL}	XTI fall to BCKO fall	20	–	60	
XTI to BCKO delay (CKSLN = LOW)	t_{sbH}	XTI fall to BCKO rise	20	–	60	ns
	t_{sbL}	XTI fall to BCKO fall	20	–	60	
BCKO to DOL, DOR, WCKO delay	t_{bdH}	BCKO fall to output rise	–5	–	10	ns
	t_{bdL}	BCKO fall to output fall	–5	–	10	
CKO TODOL, DOR, WCKO delay	t_{cdH}	CKO fall to output rise	5	–	25	ns
	t_{cdL}	CKO fall to output fall	5	–	25	
XTO TODOL, DOR, WCKO delay	t_{xdH}	XTO rise to output rise	15	–	50	ns
	t_{xdL}	XTO rise to output fall	15	–	50	



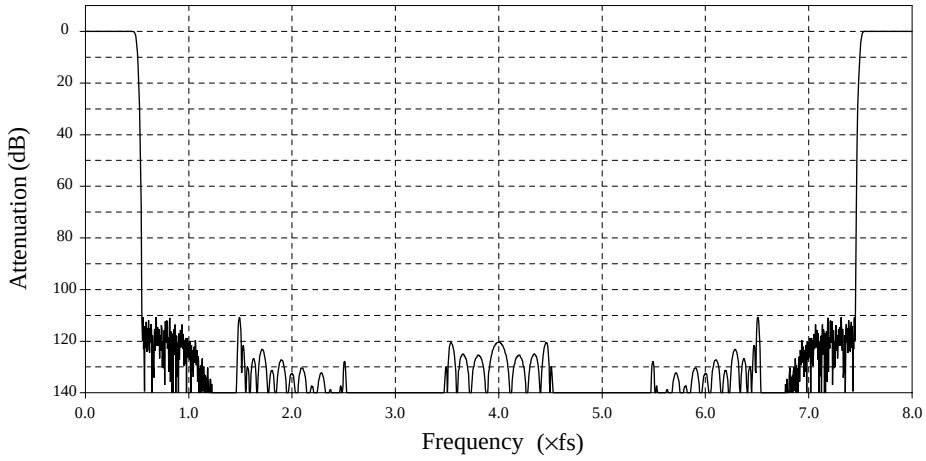
Filter Characteristics

8-times interpolation filter (sharp roll-off: response 1)

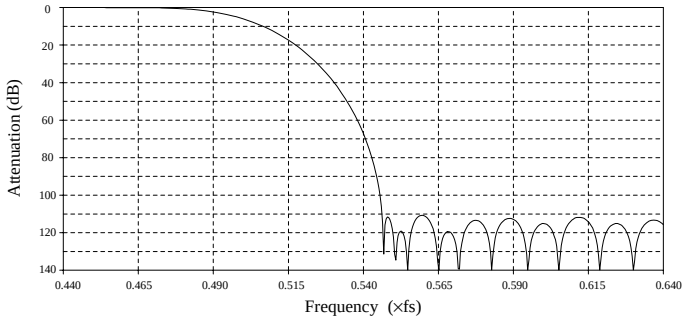
Parameter	Condition	Rating @ 256fs
Passband		0 to 0.4535fs
Stopband		0.5465fs to 7.4535fs
Passband ripple		≤ ±0.00005 dB
Stopband attenuation		≥ 110 dB
Group delay[1]	SYNCN = LOW	44.625/fs
	SYNCN = HIGH	44.25/fs to 45.0/fs

1. The digital filter arithmetic computation time from when the completion of data input at rate fs to the start of data output at rate 8fs.

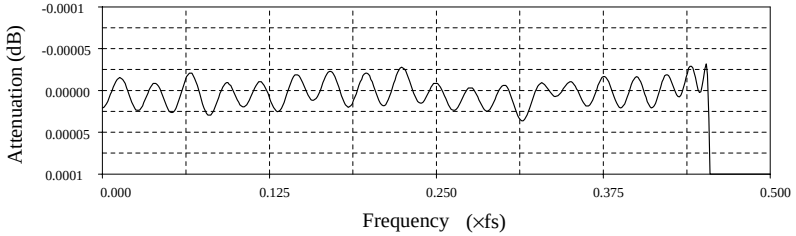
8fs filter response with deemphasis OFF



8fs filter band transition response with deemphasis OFF



8fs filter passband response with deemphasis OFF

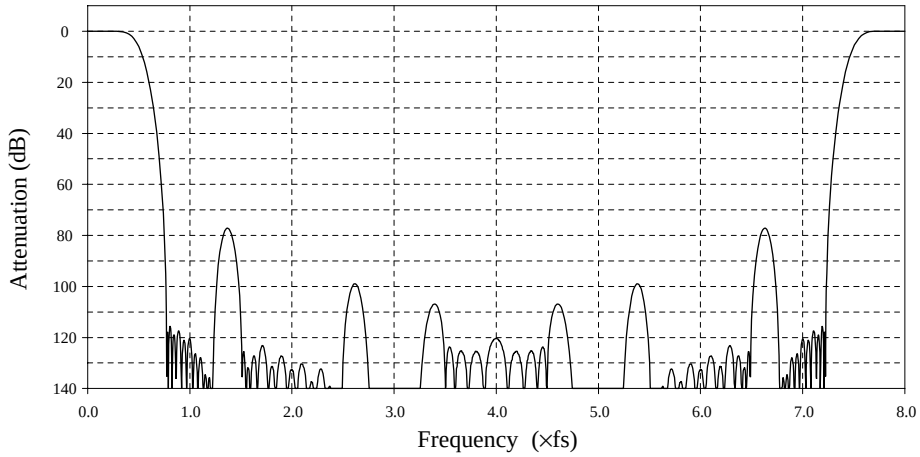


8-times interpolation filter (slow roll-off: response 2)

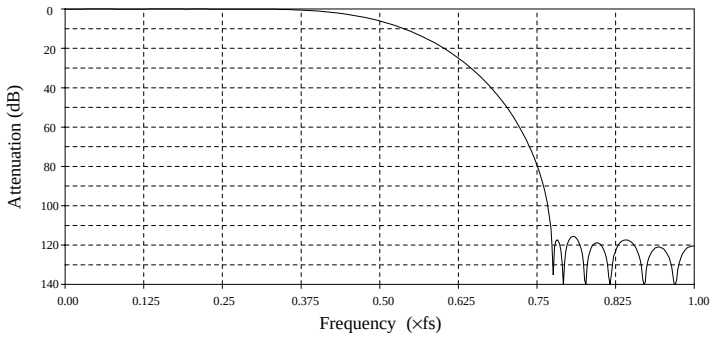
Parameter	Condition	Rating @ 256fs
Passband	< 3 dB attenuation	0 to 0.455fs
Stopband	> 77 dB attenuation	0.745fs to 7.255fs
Passband ripple	0 to 0.235fs	≤ ±0.00003 dB
Stopband attenuation		≥ 77 dB
Group delay[1]	SYNCN = LOW	25.625/fs
	SYNCN = HIGH	25.25/fs to 26.0/fs

1. The digital filter arithmetic computation time from when the completion of data input at rate fs to the start of data output at rate 8fs.

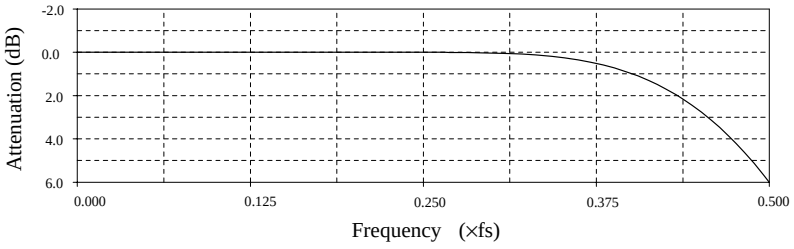
8fs filter response with deemphasis OFF



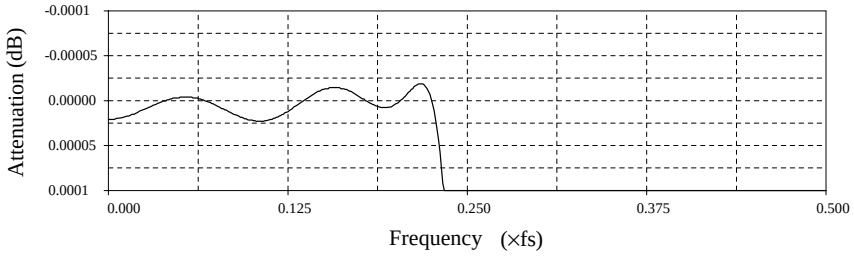
8fs filter band transition response with deemphasis OFF



8fs filter passband response with deemphasis OFF



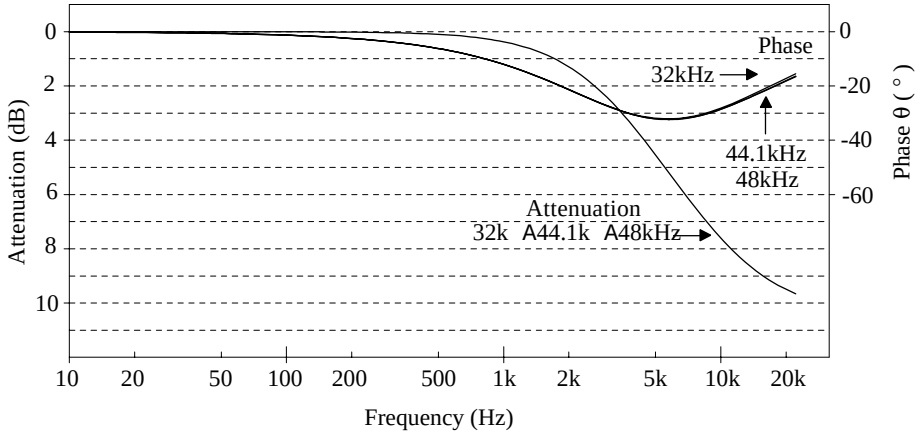
8fs filter passband response [amplitude gain enlarged]



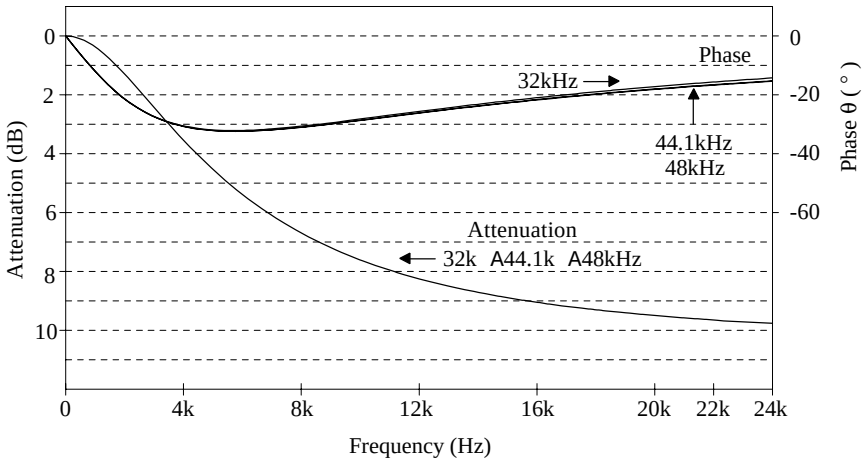
Deemphasis filter

Parameter		Sampling frequency (fs)		
		32 kHz	44.1 kHz	48 kHz
Passband bandwidth (kHz)		0 to 14.5	0 to 20.0	0 to 21.7
Deviation from ideal characteristic	Attenuation	≤ ±0.001 dB		
	Phase, θ	0 to 1.5°		

Passband response with deemphasis ON (logarithmic frequency axis)



Passband response with deemphasis ON (linear frequency axis)



FUNCTIONAL DESCRIPTION

The basic arithmetic block is shown in figure 1, and the function of each block is described in the following sections.

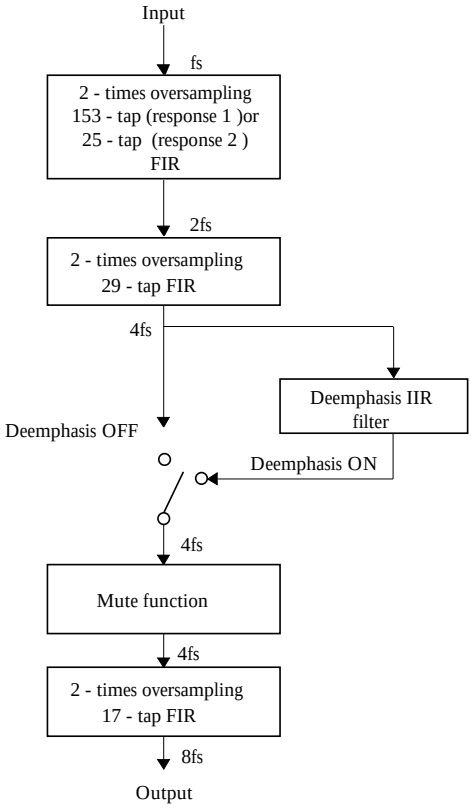


Figure 1. Arithmetic block diagram

8-times Oversampling (Interpolation)

The interpolation arithmetic block is comprised of 3 cascaded, 2-times FIR interpolation filters, as shown in figure 1.

The input signal is sampled at rate fs, and then 8-times oversampling data is output. Sampling noise in the 0.5465fs to 7.4535fs stopband for the sharp roll-off (response 1) characteristic, 0.745fs to 7.255fs for the slow roll-off (response 2) characteristic, is removed by the interpolation filter.

Digital Deemphasis

The digital deemphasis filter has the same construction as analog filters. It is implemented as an IIR filter to faithfully reproduce the gain and phase characteristics of standard analog deemphasis filters. The three sets of filter coefficients for the three fs = 32.0/44.1/48.0 kHz sampling frequencies are selected by FSEL1 and FSEL2 when the sampling frequency is specified, as shown in the following table. Deemphasis is ON when DEMP is HIGH, and OFF when DEMP is LOW.

FSEL1	FSEL2	Sampling frequency (fs)
LOW	LOW	44.1 kHz
LOW	HIGH	48 kHz
HIGH	LOW	Test mode
HIGH	HIGH	32 kHz

Note that test mode is not available for operation.

Soft Muting

The muting function controls the muting of both left and right channels simultaneously. Muting is ON when MUTE is HIGH, muting is OFF when MUTE is LOW.

When MUTE goes HIGH, the attenuation changes smoothly from 0 to −∞ dB in 512/fs, or approximately 11.6 ms when fs = 44.1 kHz. When MUTE goes LOW, muting is released and the attenuation changes smoothly from −∞ to 0 dB, again taking approximately 11.6 ms.

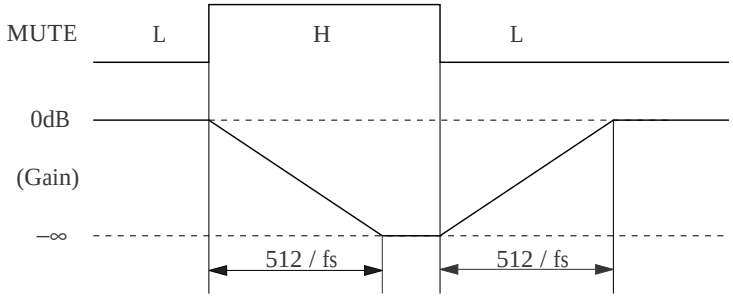


Figure 2. Mute timing

When RSTN goes LOW, the DOL and DOR outputs go LOW, immediately muting the output signal. Muting is released and timing is synchronized immediately after RSTN goes HIGH.

Digital Attenuator (MDT, MCK, MLEN)

The attenuation function is controlled by MDT, MCK and MLEN. MDT data, in 11-bit serial MSB first format, is shifted into an internal shift register on the rising edge of the serial data clock MCK. The contents of the shift register are transferred to the internal processing circuits on the rising edge of the MLEN gate pulse. The attenuation data format is shown in figure 3.

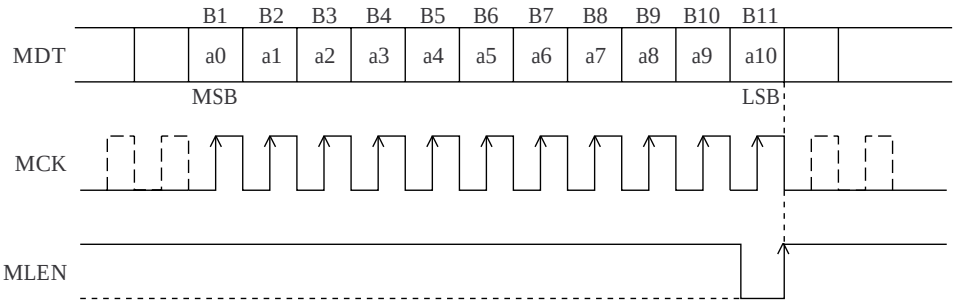


Figure 3. Attenuation data format

The attenuation register data DATT can take on any value between 0 and 1024 (400_H). The attenuation is given by the following equation for both left and right channels simultaneously.

Attenuation = $20 \times \log_{10}(DATT/1024)$ [dB]

Thus, the attenuation level is −∞ when DATT is 0, and attenuation is 0 dB when DATT is 1024. DATT is set to 1024 (400_H) after system reset initialization. The attenuation data and attenuation level for sample DATT values are shown in the following table.

Attenuation data DATT	Attenuation level (dB)
000_H	−∞
001_H to $3FF_H$	−60.206 to −0.0085
400_H	0

Attenuation operation

When an attenuation value DATT is set, the attenuation changes smoothly from the current attenuation level to the new level. The new attenuation data is stored in the attenuation register while the current attenuation data is stored in a temporary register. The attenuation then changes smoothly by ramping between the two register values, updating the temporary register with each step. If a new attenuation value for DATT is set before the previous target attenuation level is reached, the attenuation then ramps toward the new attenuation level.

When MUTE is HIGH, the attenuation level is −∞. When MUTE goes LOW (muting OFF), the attenuation level returns to that of the original value of DATT.

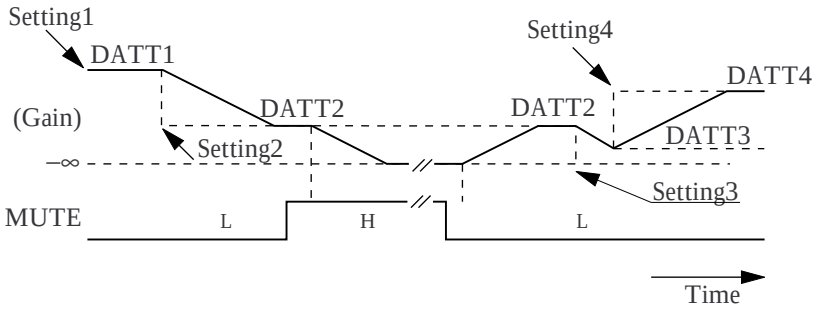


Figure 4. Attenuation and mute timing

System Clock (XTI, XTO, CKO, CKSLN)

Two system clock frequencies, 384fs and 256fs, can be used. An external clock source can be input on XTI, or a crystal oscillator can be constructed by connecting a crystal between XTI and XTO. The system clock is also buffered and then output on CKO. The system clock frequency selection and the internal clock frequency are shown in the following table.

Parameter	CKSL	
	HIGH	LOW
XTI input clock frequency ($f_{XI} = 1/t_{XI}$)	384fs	256fs
CKO clock frequency	384fs	256fs
Internal clock frequency (t_{SYS})	$2 \times t_{XI}$	t_{XI}

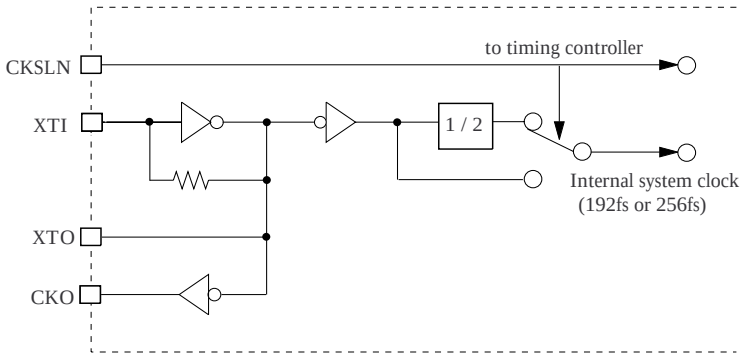


Figure 5. Clock generator circuit

Audio Data Input (INF1N, INF2N, IW1N, IW2N, DI, DIL, DIR, BCKI, LRCI)

The input data format and several input pin functions are selected by the state of INF1N and INF2N.

INF1N	DI/INF2N	Input format	Pin function selection		
			DI/INF2N	IW1N/DIL	IW2N/DIR
LOW	LOW	LR alternating[1], trailing data	DI	IW1N	IW2N
LOW	HIGH				
HIGH	LOW	LR alternating, leading data	INF2N	DIL	DIR
HIGH	HIGH	LR simultaneous[2], leading data			

1. Alternating left-channel and right-channel data input on a single input DI.
2. Simultaneous left-channel and right-channel data input on two inputs, DIL and DIR, respectively.

The input data word length is selected by the state of IW1N and IW2N when INF1N is LOW. 20-bit is selected when INF1N is HIGH.

INF1N	IW2N/DIL	IW1N/DIR	Input bit length
LOW	LOW	LOW	20 bits
	LOW	HIGH	20 bits
	HIGH	LOW	18 bits
	HIGH	HIGH	16 bits
HIGH	×	×	20 bits

Jitter-free Function (SYNCN)

The arithmetic circuit and output control timing is derived from the system clock, and is therefore independent of the input LRCI and BCKI clocks. Accordingly, any jitter in the data input clock (LRCI and BCKI) does not cause jitter in the output.

Generally, the internal timing is synchronized to the LRCI input timing after a system reset release, when RSTN goes from LOW to HIGH, on the first LRCI clock start edge. If the input timing and LRCI start edge timing subsequently drift, the input timing is automatically resynchronized when the timing error exceeds a certain value. There are 2 timing error values at which resynchronization occurs, selected by the state of SYNCN.

Jitter-free mode (SYNCN = HIGH)

When SYNCN is HIGH, the timing error value is ±3/8 × (LRCI clock period). When the difference between the input timing and LRCI start edge position do not exceed this value, internal timing is not resynchronized and all functions continue to operate normally.

Sync mode (SYNCN = LOW)

When SYNCN is LOW, the timing error value is ±1 × (system clock period), which is a much smaller timing error tolerance than in jitter-free mode. In this mode, the internal timing is guaranteed to follow the LRCI clock timing within this tolerance, making this mode useful for systems constructed from a multiple number of SM5843A×1 devices.

Note that resynchronization affects the internal operation and can generate a momentary click noise output.

Audio Data Output (DOL, DOR, BCKO, WCKO, OW20N)

The output data is in serial, simultaneous left and right-channel, 2s complement, MSB first, BCKO burst (NPC format) format. The output data word length is selected by the state of OW20N. 18-bit output is selected when OW20N is HIGH, and 20-bit output when OW20N is LOW.

8fs serial data is output in sync with the falling edge of the internal system clock and BCKO clock. The number of BCKO bit clock pulses per word changes depending on the output bit length selected (18/20 bits). Consequently, output data is latched into the internal output register on the falling of the edge of an output word clock WCKO, which has timing independent of the number of output bits as specified in the following table.

Parameter	Symbol	CKSLN = HIGH	CKSLN = LOW
Bit clock rate	T_B	1/192fs	1/256fs
Data word length	T_{DW}	$24t_{SYS}$	$32t_{SYS}$

System Reset (RSTN)

The SM5843A×1 must be reset under the following conditions.

- At power-ON.
- When the LRCI clock and internal operation timing need to be resynchronized.
- When switching the CKSLN clock select input.
- When switching between filter characteristics using TMOD2.
- When either or both of the LRCI and XTI clocks stop or are interrupted.

The system is reset by applying a LOW-level pulse on RSTN.

The arithmetic and output timing counters are reset on the first LRCI start edge after reset is released, as long as the XTI clock has already stabilized. The LRCI start edge is determined by the state of INF1N and INF2N. When INF1N is LOW or when both INF1N and INF2N are HIGH, the start edge is the rising edge. When INF1N is HIGH and INF2N is LOW, the start edge is the falling edge.

When RSTN is LOW, the DOL and DOR outputs are LOW, muting the output signal to an attenuation level of −∞.

The power-ON reset pulse can be applied by a microcontroller or, for systems where XTI and LRCI are stable at power-ON, by connecting a capacitor of several hundred pF between RSTN and VSS. For systems that do not use a microcontroller, the capacitor must be chosen such that the XTI and LRCI clocks fully stabilize before RSTN goes from LOW to HIGH.

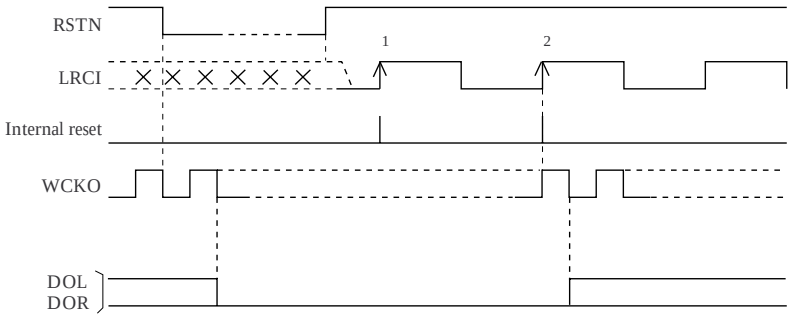


Figure 6. System reset timing and output muting

Filter Characteristic Selection (TMOD2)

There are 2 digital filter frequency response characteristics incorporated into the SM5843A×1, selected by the state of TMOD2. A sharp roll-off characteristic (response 1) is selected when TMOD2 is HIGH, and a slow roll-off characteristic (response 2) when TMOD2 is LOW. The response is modified by changing the number of taps in the 1st FIR filter stage, as shown in figure 1.

- Filter response 1
  - 153-tap 1st FIR
  - 29-tap 2nd FIR
  - 17-tap 3rd FIR
- Filter response 2
  - 25-tap 1st FIR
  - 29-tap 2nd FIR
  - 17-tap 3rd FIR

Note that the device should be reset when changing TMOD2 during normal operation.

Dither Rounding-off Processing (TMOD1)

Dither rounding-off processing of output data is ON when TMOD1 is LOW. Dither is OFF and normal processing mode is selected when TMOD1 is HIGH.

TIMING DIAGRAMS

Input Timing Examples (DIN, BCKI, LRCI)

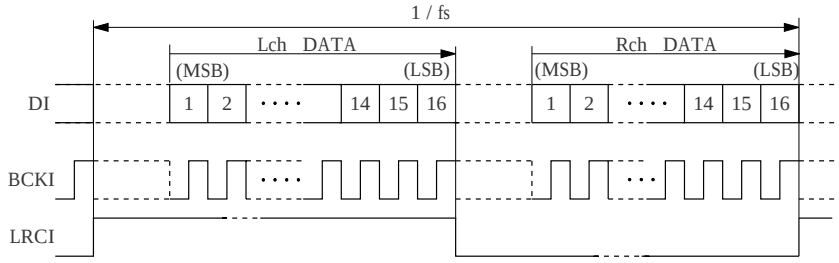
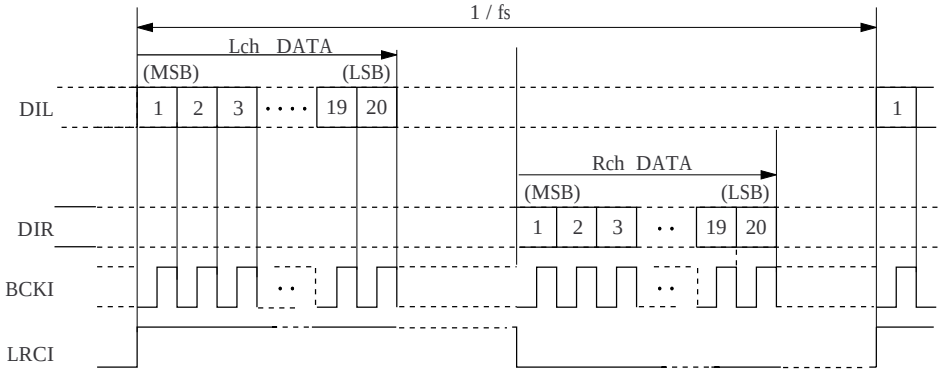
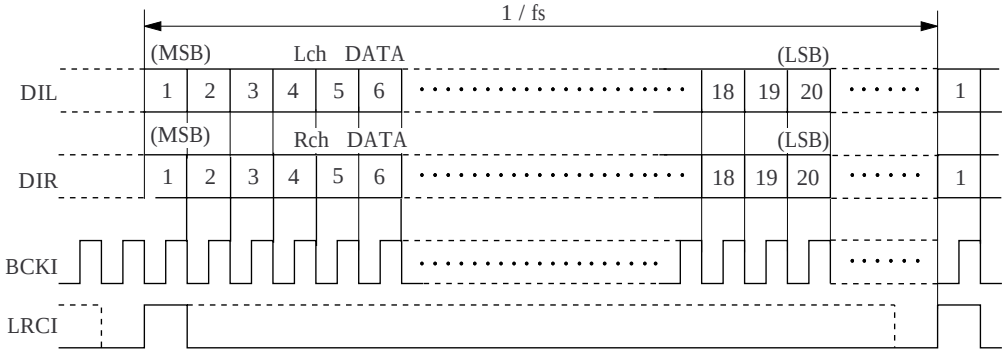


Figure 7. LR alternating, trailing data, 16-bit input



Data after lsb (bit 20) is ignored. After bit 20, BCKI clock input is not needed.

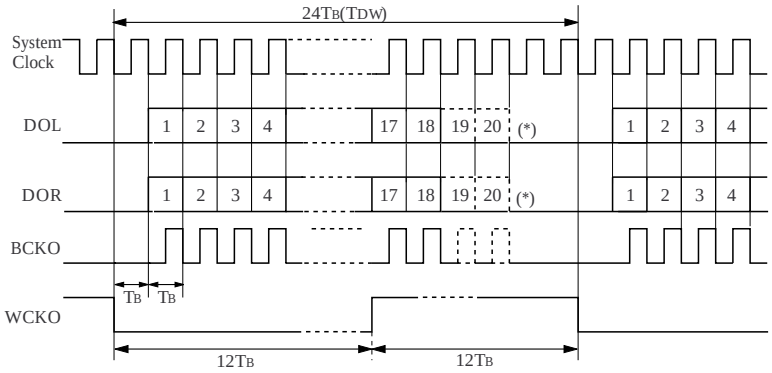
Figure 8. LR alternating, leading data, 20-bit input



Data after lsb (bit20) is ignored. After bit 20, BCKI clock input is not needed.

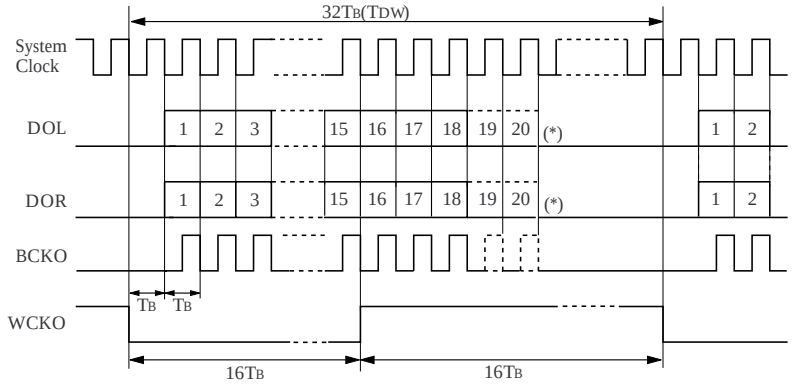
Figure 9. LR simultaneous, leading data, 20-bit input

Output Timing Examples (DOL, DOR, BCKO, WCKO)



The number of output bits is determined by the output bit length selected.

Figure 10. 18/20-bit output ($\overline{CKSL}$ = HIGH)



The number of output bits is determined by the output bit length selected.

Figure 11. 18/20-bit output ($\overline{CKSL}$ = LOW)

Data Input to Output Delay Timing

This is the digital filter arithmetic computation time from the completion of data input at rate fs (t_{INPUT}) on the rising edge of LRCI to the start of data output at rate 8fs (t_{OUTPUT}) on the falling edge of WCKO.

Filter response	CKSLN	SYNCN	Mode	$t_{OUTPUT} - t_{INPUT}$
Filter response 1	LOW (256fs)	LOW	After reset + sync mode	44.625/fs
		HIGH	Jitter-free mode	44.25/fs – 45.0/fs
	HIGH (384fs)	LOW	After reset + sync mode	44.75/fs
		HIGH	Jitter-free mode	44.375/fs – 45.125/fs
Filter response 2	LOW (256fs)	LOW	After reset + sync mode	25.625/fs
		HIGH	Jitter-free mode	25.25/fs – 26.0/fs
	HIGH (384fs)	LOW	After reset + sync mode	25.75/fs
		HIGH	Jitter-free mode	25.375/fs – 26.125/fs

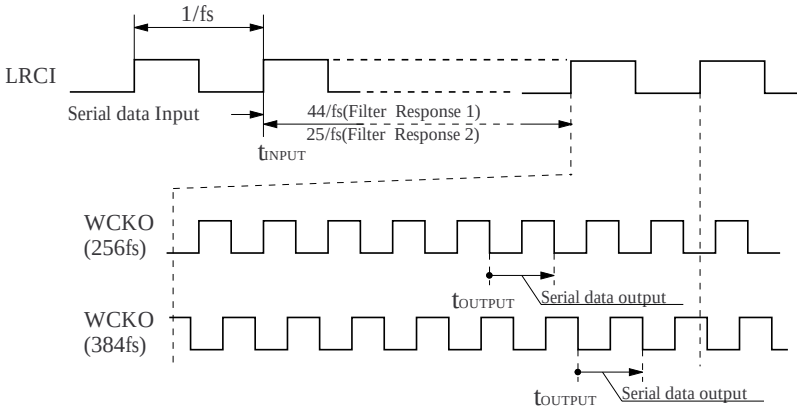


Figure 12. Delay timing (SYNCN = LOW)

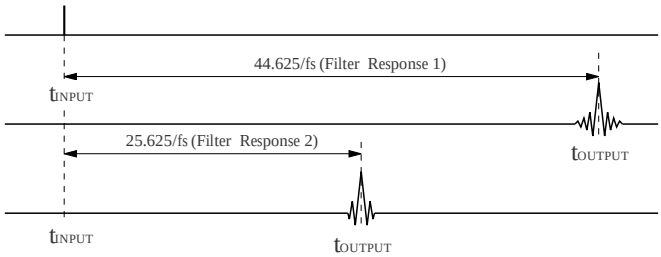
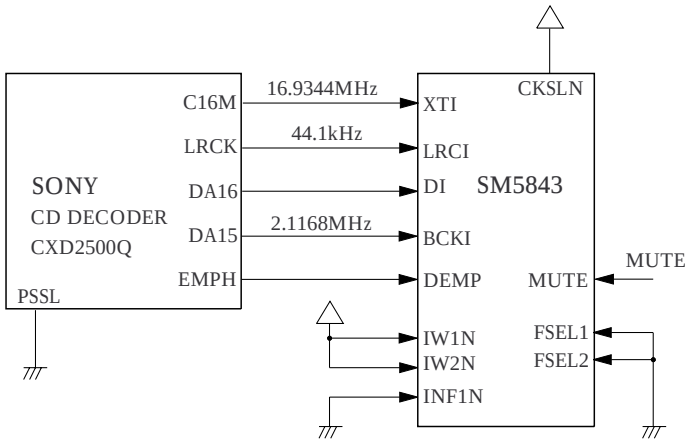


Figure 13. Delay timing (SYNCN = CKSLN = LOW)

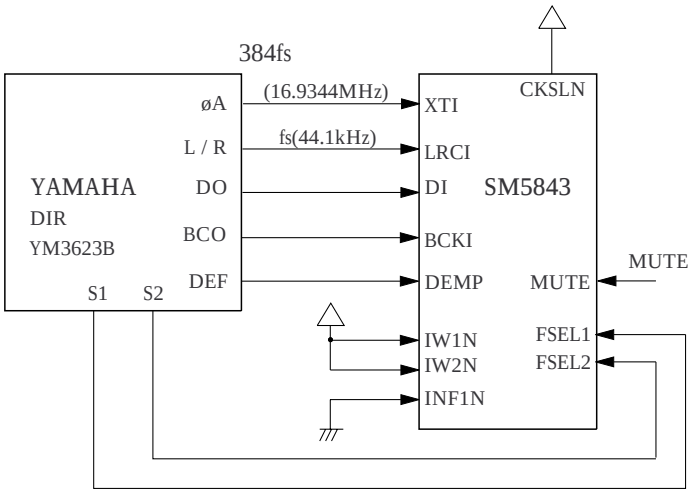
APPLICATION CIRCUITS

Input Interface Circuits

CD decoder (CXD2500Q) connection

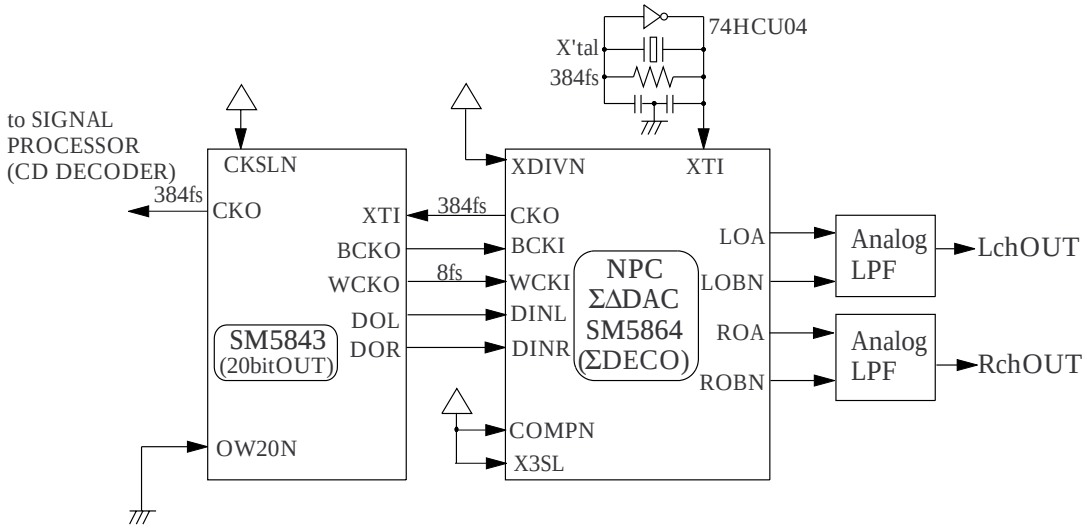


Digital audio interface receiver (YM3623B) connection



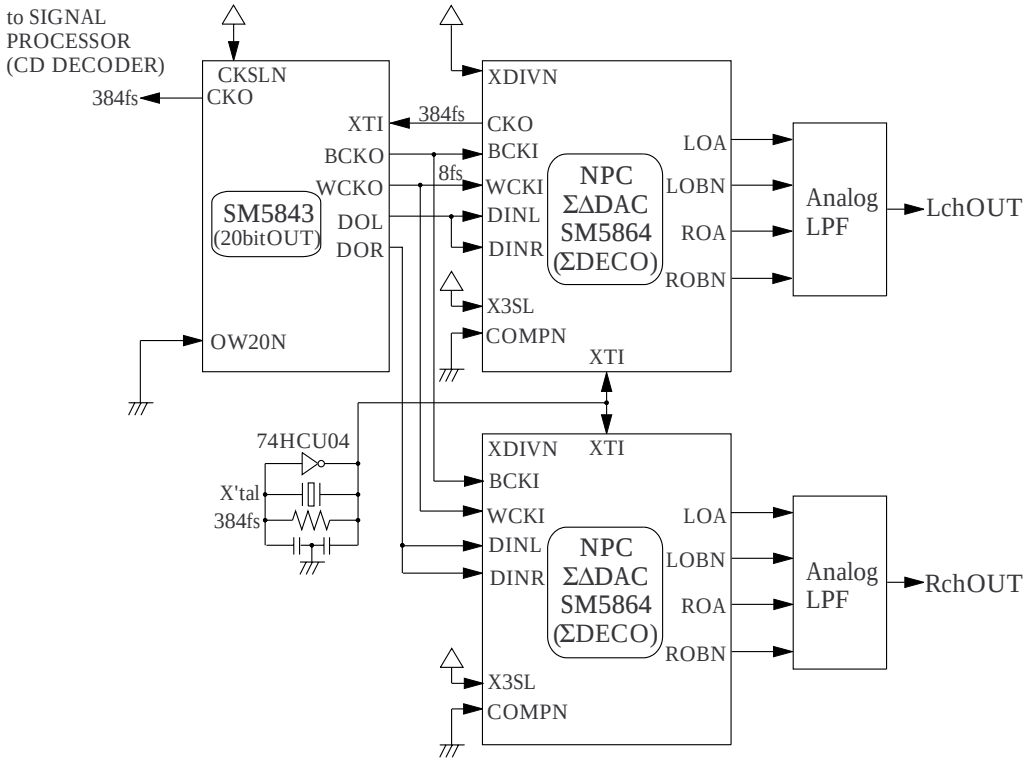
Output Interface Circuits

20-bit input ΣΔ DAC (SM5864AP) connection 1



20-bit input ΣΔ DAC (SM5864AP) connection 2

L/R-channel independent complementary PWM output



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NC9626AE 1997.03

A DIVISION OF CIRRUS LOGIC

CS5396
CS5397

120 dB, 96 kHz Audio A/D Converter

Features

- 24-Bit Conversion
- 120 dB Dynamic Range (A-Weighted)
- Low Noise and Distortion
  >105 dB THD + N
- Complete CMOS Stereo A/D System
  Delta-Sigma A/D Converters
  Digital Anti-Alias Filtering
  S/H Circuitry and Voltage Reference
- CS5396 - digital filter optimized for audio
- CS5397 - non-aliasing digital filter
- Adjustable System Sampling Rates including 32, 44.1, 48 & 96 kHz
- Differential Analog Architecture
- Linear Phase Digital Anti-Alias Filtering
- 10 Tap Programmable Psychoacoustic Noise Shaping Filter
- Single +5 V Power Supply

General Description

The CS5396 and CS5397 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form at sample rates up to 100 kHz per channel.

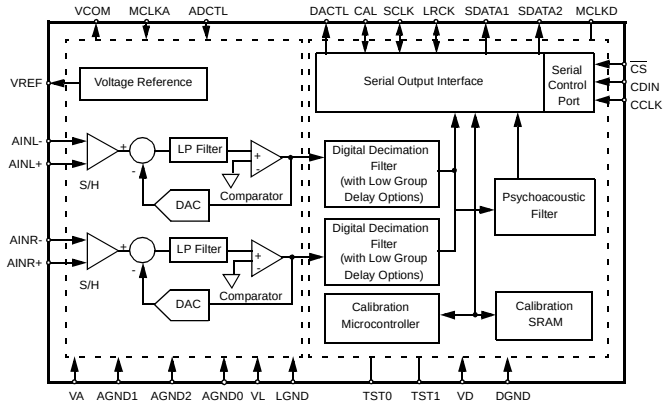
The CS5396/97 use a patented 7th-order, tri-level delta-sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADCs use a differential architecture which provides excellent noise rejection.

The CS5396 has a linear phase filter optimized for audio applications with ±0.005 dB passband ripple and >117 dB stopband rejection. The CS5397 has a non-aliasing filter response with ±0.005 passband ripple and >117 dB stopband attenuation. Other features available in both the CS5396 and CS5397 are an optional low group delay filter and a unique psychoacoustic noise shaping filter which subjectively truncates the output to 16, 18 or 20 bits while 24-bit sound quality is preserved.

The CS5396/97 are targeted for the highest performance professional audio systems requiring wide dynamic range, negligible distortion and low noise.

ORDERING INFORMATION

CS5396-KS	-10° to 50° C	28-pin SOIC
CS5397-KS	-10° to 50° C	28-pin SOIC
CDB5396/97		Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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TABLE OF CONTENTS

ANALOG CHARACTERISTICS (T_A = 25°C; VA, VL,VD = 5V; Full-scale Input Sinewave, 997 Hz; Analog connections as shown in Figure 1; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Logic 0 = 0V, Logic 1 = VD;

Parameter		Symbol	Min	Typ	Max	Units
Dynamic Performance						
Dynamic Range	MCLK equal to 24.576 MHz		TBD			
Fs = 48 kHz in 128x Oversampling Mode	(A-weighted)		TBD	120	-	dB
Fs = 48 kHz in 128x mode			TBD	117	-	dB
Fs = 96 kHz in 64x mode	(A-weighted)		TBD	120	-	dB
Fs = 96 kHz in 64x mode	(40 kHz Bandwidth)			114	-	dB
	MCLK equal to 12.288 MHz		TBD			
Fs = 48 kHz in 64x mode	(A-weighted)		TBD	117	-	dB
Fs = 48 kHz in 64x mode				114	-	dB
Total Harmonic Distortion + Noise		THD+N				
Fs = 48 kHz in 128x mode	-1 dB (Note 1)		TBD	105	-	dB
	-20 dB (Note 1)		TBD	97	-	dB
	-60 dB (Note 1)		TBD	57	-	dB
Fs = 96 kHz in 64x mode	-1 dB (Note 1)		TBD	105	-	dB
(40 kHz bandwidth)	-20 dB (Note 1)		TBD	97	-	dB
	-60 dB (Note 1)		TBD	57	-	dB
Fs = 48 kHz in 64x mode	-1 dB (Note 1)		TBD	105	-	dB
	-20 dB (Note 1)		TBD	97	-	dB
	-60 dB (Note 1)		TBD	57	-	dB
Total Harmonic Distortion	-1 dB (Note 1)	THD	TBD	0.00056	-	%
Interchannel Phase Deviation			-	0.0001	-	deg
Interchannel Isolation			-	120	-	dB
Dynamic Range Performance Drift	(following calibration)		-	0.05	-	dB/°C
dc Accuracy						
Interchannel Gain Mismatch			-	0.05	-	dB
Gain Error			-	±5	TBD	%
Gain Drift			-	±100	-	ppm/°C
Offset Error (With high pass filter enabled)			-	0	-	LSB
Analog Input						
Full-scale Differential Input Voltage	(Note 2)	V_{IN}	TBD	4	TBD	V_{pp}
Input Impedance	Differential	Z_{IN}	-	4.5	-	kΩ
	Common-mode		-	TBD	-	kΩ
Common-Mode Rejection Ratio		CMRR	-	82	-	dB

Notes: 1. Referenced to typical full-scale differential input voltage (4.0 Vpp).

2. Specified for a fully differential input ±{(AINR+)-(AINR-)}.The ADC accepts input voltages up to the analog supplies (VA and AGND). Full-scale outputs will be produced for differential inputs beyond VIN.

* Refer to Parameter Definitions at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS (T_A = 25 °C; VA, VL,VD = 5V±5%; Fs = 48 kHz)

Parameter	Symbol	CS5396 Min	CS5396 Typ	CS5396 Max	CS5397 Min	CS5397 Typ	CS5397 Max	Unit
High-Performance Filter								
Passband(-0.01 dB)		0	-	0.4604	0	-	0.3958	Fs
Passband Ripple		-	-	±0.005	-	-	±0.005	dB
Stopband		0.5542	-	63.45	0.4979	-	63.50	Fs
Stopband Attenuation		117	-	-	117	-	-	dB
Group Delay (Fs = Output Sample Rate)	t_{gd}							
128x Oversampling Mode		-	34/Fs	-	-	34/Fs	-	µs
64x Oversampling Mode		-	34/Fs	-	-	34/Fs	-	µs
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	-	-	0.0	µs
Low Group Delay Filter								
Passband(-0.01 dB)		0	-	0.375	0	-	0.375	Fs
128x Oversampling Mode		0	-	0.188	0	-	0.188	Fs
64x Oversampling Mode								
Passband Ripple		-	-	0.015	-	-	0.015	dB
Stopband		0.646	-	127.35	0.646	-	127.35	Fs
128x Oversampling Mode		0.323	-	63.68	0.323	-	63.68	Fs
64x Oversampling Mode								
Stopband Attenuation		86	-		86	-		dB
Group Delay (Fs = Output Sample Rate)	t_{gd}	-	10/Fs	-	-	10/Fs	-	µs
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	-	-	0.0	µs
High Pass Filter Characteristics								
Frequency Response-3.0 dB (Note 3)		-	1.8	-	-	1.8	-	Hz
-0.036 dB (Note 3)			20	-		20	-	Hz
Phase Deviation@ 20Hz (Note 3)		-	5.3	-	-	5.3	-	Deg
Passband Ripple		-	-	0	-	-	0	dB

Notes: 3. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

POWER AND THERMAL CHARACTERISTICS

(T_A = 25 °C; VA, VL,VD = 5V±5%; Fs = 48 kHz; Master Mode)

Parameter		Symbol	64X oversampling MCLK=12.288 MHz Min	Typ	Max	128X oversampling MCLK=24.576 MHz Min	Typ	Max	Unit
Power Supply Current (Normal Operation)	VA+VL	I_A	-	150	TBD	-	160	TBD	mA
	VD	I_D	-	65	TBD	-	125	TBD	mA
Power Supply Current (Power-Down Mode)	VA+VL	I_A	-	2	-	-	3	-	mA
	VD	I_D	-	2	-	-	3.5	-	mA
Power Consumption(Normal Operation)			-	1075	TBD	-	1425	TBD	mW
(Power-Down Mode)			-	20	-	-	33	-	mW
Power Supply Rejection Ratio (1 kHz)		PSRR	-	65	-	-	65	-	dB
Allowable Junction Temperature			-	-	135	-	-	135	°C
Junction to Ambient Thermal Impedance		T_{JA}	-	45	-	-	45	-	°C/W

DIGITAL CHARACTERISTICS (T_A = 25 °C; VA, VL,VD = 5V±5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.4	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage at I_o = -20 µA	V_{OH}	VD - 1.0	-	-	V
Low-Level Output Voltage at I_o = 20 µA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	±10	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Logic	VL	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
	|VA - VD|		-	-	0.4	V
	(Note 6)		-	-	0.4	V
	|VA - VL|		-	-	0.4	V
	(Note 6)					
	|VD - VL|					
	(Note 6)					
Input Current	(Note 4)	I_{in}	-	-	±10	mA
Analog Input Voltage	(Note 5)	V_{IN}	AGND-0.7	-	VA+0.7	V
Digital Input Voltage	(Note 5)	V_{IND}	-0.3	-	VD+0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-55	-	+50	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 4. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

5. The maximum over/under voltage is limited by the input current.

6. Applies to normal operation. Greater differences during power up/down will not cause SCR latch-up.
WARNING: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

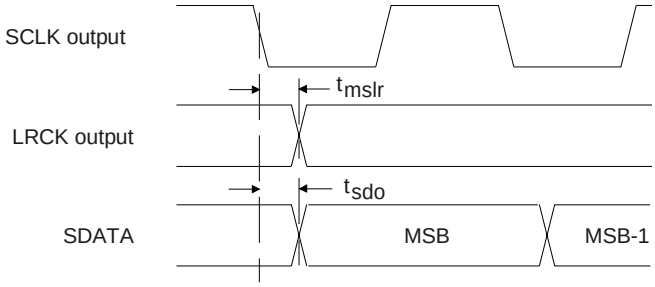
RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD	4.75	5.0	5.25	V
	Positive Logic	VL	4.75	5.0	5.25	V
	Positive Analog	VA	4.75	5.0	5.25	V
	|VA - VD| (Note 6)		-	-	0.4	V
Ambient Operating Temperature (Power Applied)		T_A	-10	-	+50	°C

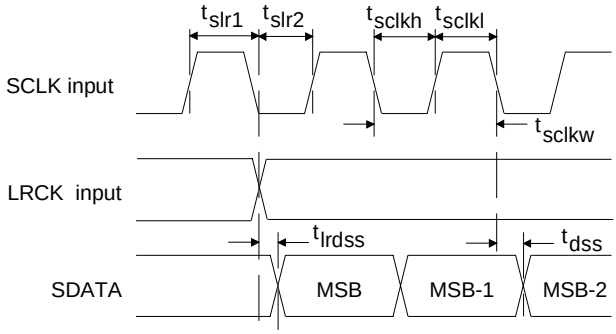
Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A = 25 °C; VA = 5V±5%; Inputs: Logic 0 = 0V, Logic 1 = VA = VD; C_L = 20 pF)

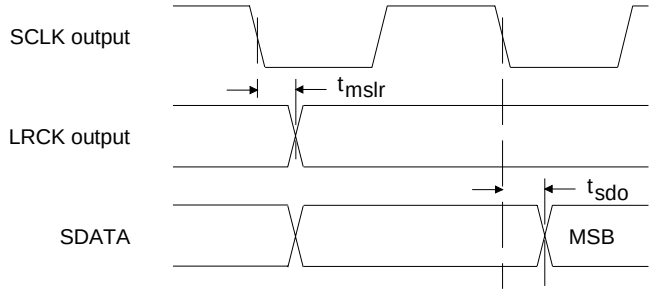
Parameter	Symbol	Min	Typ	Max	Units
Output Sample Rate	Fs	2	-	100	kHz
MCLK Period	t_{clkw}	39.06	-	1950	ns
MCLK Low	t_{clkl}	26	-	-	ns
MCLK High	t_{clkh}	26	-	-	ns
MCLK Fall Time	t_{clkft}	-	-	8	ns
Master Mode					
SCLK falling to LRCK	t_{mslr}	-20	-	+20	ns
SCLK falling to SDATA valid	t_{sdo}	-	-	20	ns
SCLK duty cycle		-	50	-	%
Slave Mode					
LRCK Period	1/Fs	10	-	500	µs
LRCK duty cycle		-	50	-	%
SCLK Period	t_{sclkw}	4 x t_{clw}	-	-	ns
SCLK Pulse Width Low	t_{sclkl}	2 x t_{clw}	-	-	ns
SCLK Pulse Width High	t_{clkh}	60	-	-	ns
SCLK falling to SDATA valid	t_{dss}	-	-	t_{clw} + 20 ns	ns
LRCK edge to MSB valid	t_{lrdss}	-	-	t_{clw} + 20 ns	ns
SCLK rising to LRCK edge delay	t_{slr1}	t_{clw} + 20 ns	-	-	ns
LRCK edge to rising SCLK setup time	t_{slr2}	t_{clw} + 20 ns	-	-	ns



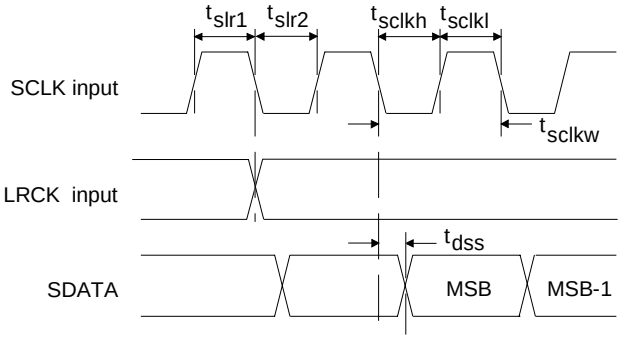
SCLK to SDATA & LRCK - MASTER mode
Serial Data Format, Left Justified



SCLK to LRCK & SDATA - SLAVE mode
Serial Data Format, Left Justified



SCLK to SDATA & LRCK - MASTER mode
Serial Data Format, I^2S compatible



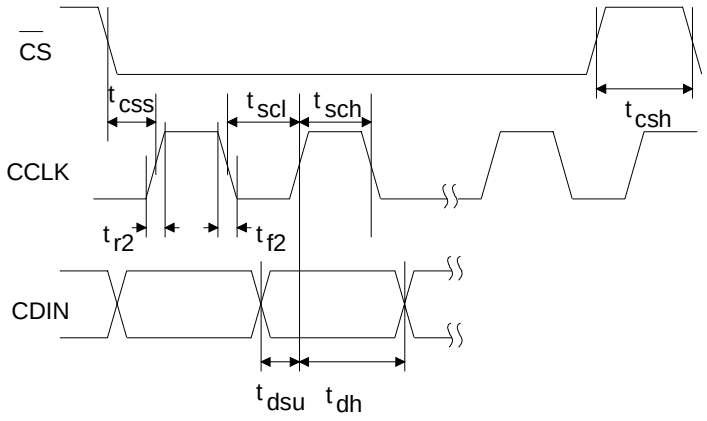
SCLK to LRCK & SDATA - SLAVE mode
Serial Data Format, I^2S compatible

SPI CONTROL PORT SWITCHING CHARACTERISTICS (T_A = 25 °C; VD, VA = 5V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD; C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sck}	-	6	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 7)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 8)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 8)	t_{f2}	-	100	ns

Notes: 7. Data must be held for sufficient time to bridge the transition time of CCLK.

8. For F_{SCK} < 1 MHz.

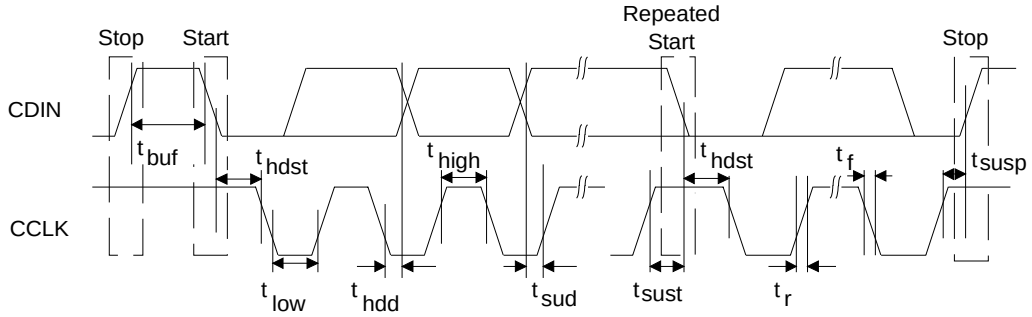


I²C CONTROL PORT SWITCHING CHARACTERISTICS (T_A = 25 °C; VD, VA = 5V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD; C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
I²C® Mode	***(Note 9)***				
CCLK Clock Frequency		f_{scl}	-	100	kHz
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low Time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
CDIN Hold Time from CCLK Falling	(Note 10)	t_{hdd}	0	-	µs
CDIN Setup Time to CCLK Rising		t_{sud}	250	-	ns
Rise Time of Both CDIN and CCLK Lines		t_r	-	1	µs
Fall Time of Both CDIN and CCLK Lines		t_f	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs

Notes: 9. Use of the I²C® bus interface requires a license from Philips.

10. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.



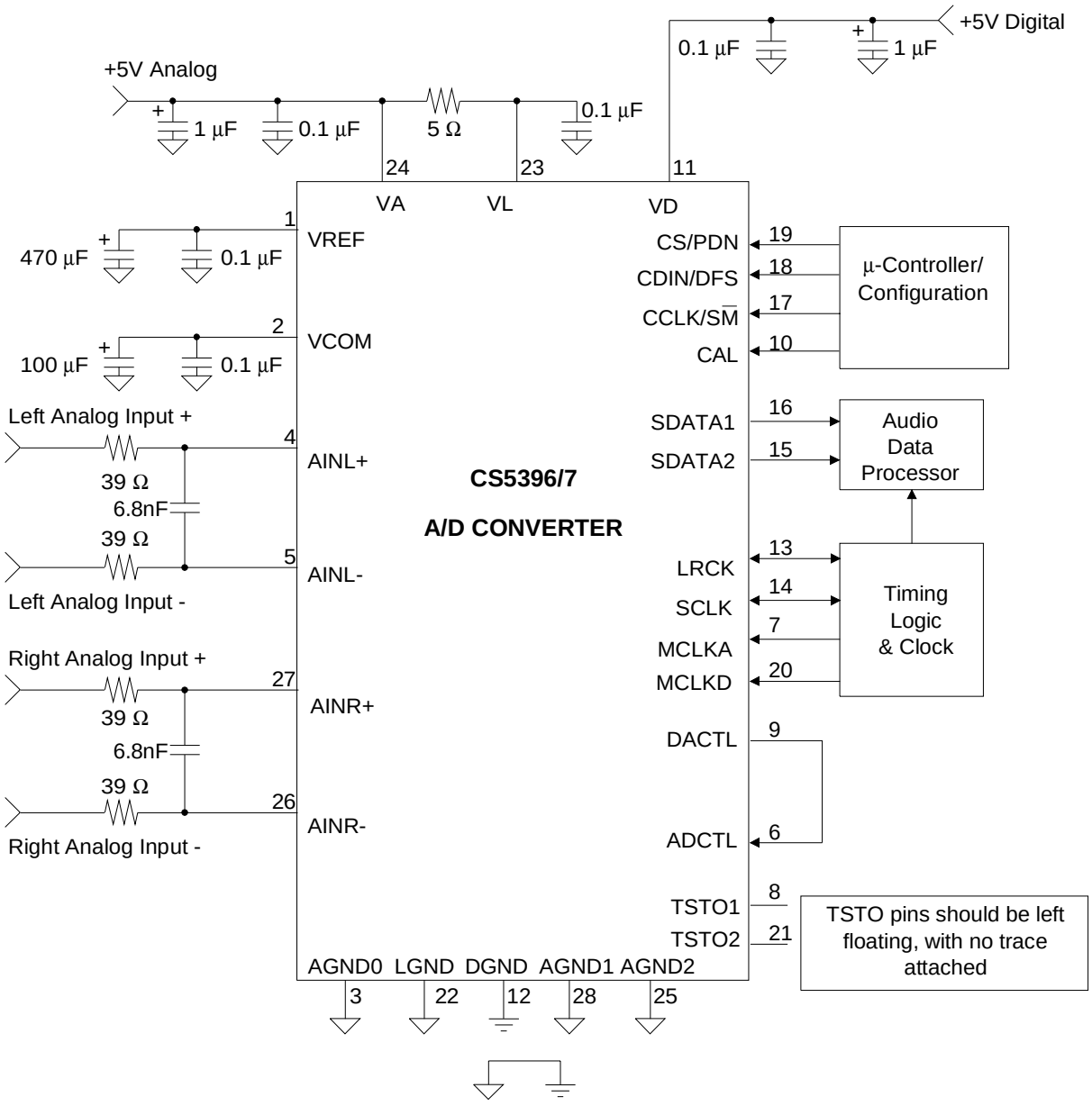


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5396/97 is a 24-bit, stereo A/D converter designed for stereo digital audio applications. The analog input channels are simultaneously sampled by separate, patented, 7th-order tri-level delta-sigma modulators at either 128 or 64 times the output sample rate (64× Fs or 128× Fs) of the device. The resulting serial bit streams are digitally filtered, yielding pairs of 24-bit values at output sample rates (Fs) of up to 100 kHz. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters, and it does not require external sample-and-hold amplifiers or voltage references. Only normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are required, as shown in Figure 1. An on-chip voltage reference provides for a differential input signal range of 4.0 Vpp. The device also contains a high pass filter, implemented digitally after the decimation filter, to completely eliminate any internal offsets in the converter or any offsets present at the input circuitry to the device. Output data is available in serial form, coded as 2's complement 24-bit numbers. For more information on delta-sigma modulation techniques see the references at the end of this data sheet.

Stand-Alone vs. Control Port Mode

The CS5396/97 can operate in either Stand-Alone or Control Port Mode. The functionality of pins 17, 18 and 19 is established upon entering either the Stand-Alone or Control Port mode, as described in the Pin Description section.

The Control Port Mode requires a micro-controller and allows access to many additional features, which include:

- 128× Oversampling Mode
- Reduction of 24-bit data to 20, 18 or 16-bit data with psychoacoustically optimized dither
- Programmability of psychoacoustic filter coefficients
- Peak Input Signal Level Monitor with either High Resolution or Bar Graph mode selection
- Signal inversion
- High pass filter defeat
- Mute
- Access to the digital filter to allow the input of external digital audio data to produce a two-to-one decimated output and/or psychoacoustic bit reduction.

STAND-ALONE MODE

Master Clock - Stand-Alone Mode

The master clock is the clock source for the delta-sigma modulator sampling (MCLKA) and digital filters (MCLKD). The required MCLKA/D frequency is determined by the desired Fs and must be 256× Fs. Table 1 shows some common master clock frequencies.

LRCK (kHz)	MCLKA/D (MHz)	SCLK (MHz)
32	8.192	2.048
44.1	11.2896	2.822
48	12.288	3.072
64	16.384	4.096
88.2	22.5792	5.6448
96	24.576	6.144

Table 1. Common Clock Frequencies for Stand-Alone Mode

Serial Data Interface - Stand-Alone Mode

The CS5396/97 supports two serial data formats which are selected via the digital format select pin, DFS. The digital output format determines the relationship between the serial data, left/right clock and serial clock. Figures 2 and 3 detail the interface for-

mats. The serial data interface is accomplished via the serial data outputs; SDATA1 and SDATA2; serial data clock, SCLK, and the left/right clock, LRCK. The serial nature of the output data results in the left and right data words being read at different times. However, the samples within an LRCK cycle represent simultaneously sampled analog inputs.

Serial Data- Stand-Alone Mode

The serial data block consists of 24 bits of audio data presented in 2's-complement format with the MSB-first. The data is clocked from SDATA1 and SDATA2 by the serial clock and the channel is determined by the Left/Right clock. The full precision 24-bit data is available on SDATA1 and the output from the low group delay filter is available on SDATA2.

Serial Clock - Stand-Alone Mode

The serial clock shifts the digitized audio data from the internal data registers via the SDATA1 and SDATA2 pins. SCLK is an output in Master Mode where internal dividers will divide the master clock by 4 to generate a serial clock which is 64× Fs. In Slave Mode, SCLK is an input with a serial clock typically between 48× and 128× Fs. However, it is recommended that SCLK be equal to 64×, though other frequencies are possible, to avoid potential interference effects which may degrade system performance.

Left/Right Clock - Stand-Alone Mode

The Left/Right clock, LRCK, determines which channel, left or right, is to be output on SDATA1 and SDATA2. In Master Mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs and synchronous to MCLKA/D.

Master Mode - Stand-Alone Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from the master clock. Internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 64× Fs and by 256 to generate a LRCK which is equal to Fs. The CS5396/97 is placed in the Master mode with the slave/master pin, S/$\overline{M}$, low.

Slave Mode - Stand-Alone Mode

LRCK and SCLK become inputs in SLAVE mode. LRCK must be externally derived from MCLKA/D and be equal to Fs. It is recommended that SCLK be equal to 64×. Other frequencies between 48× and 128× Fs are possible but may degrade system performance due to interference effects. The master clock frequency must be 256× Fs. The CS5396/97 is placed in the Slave mode with the slave/master pin, S/$\overline{M}$, high.

High Pass Filter - Stand-Alone Mode

The CS5396/97 includes a high pass filter after the decimator to remove the DC offsets introduced by the analog buffer stage and the CS5396/97 analog modulator. The characteristics of this first-order high pass filter are outlined below, for Fs equal to 48 kHz. This filter response scales linearly with sample rate.

Frequency response:	-3 dB @ 1.8 Hz
	-0.036 dB @ 20 Hz
Phase deviation:	5.3 degrees @ 20 Hz
Passband ripple:	None

Power-up and Calibration - Stand-Alone Mode

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by exiting the power-down mode. However, the voltage reference will take a much longer time to reach a final value due to the presence of external capacitance on the VREF pin. A time delay of approximately 10ms/µF is required after applying power to the device or after exiting a power down state.

A calibration of the tri-level delta-sigma modulator should always be initiated following power-up and after allowing sufficient time for the voltage on the external VREF capacitor to settle. This is required to minimize noise and distortion. It is also advised that the CS5396/97 be calibrated after the device has reached thermal equilibrium, approximately 10 seconds, to maximize performance.

Synchronization of Multiple Devices - Stand Alone Mode

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. It is recommended that the rising edge of the CAL signal be timed with a falling edge of MCLK to ensure that all devices will initiate a calibration and synchronization sequence on the same rising edge of MCLK. The absence of re-timing of the CAL signal can result in a sampling difference of one MCLK period.

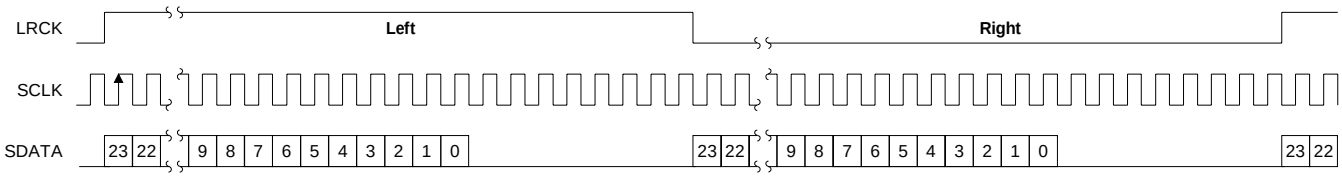
CONTROL PORT MODE

Access to Control Port Mode

The mode selection between Stand-Alone and Control Port Mode is determined by the state of the SDATA1 pin 250 MCLK cycles following the internal power-on reset. A 47 kΩ pull-up resistor on SDATA1 will select the Control Port Mode. However, the control port will not respond to CCLK and CDIN until the pull-up on the SDATA1 pin is released.

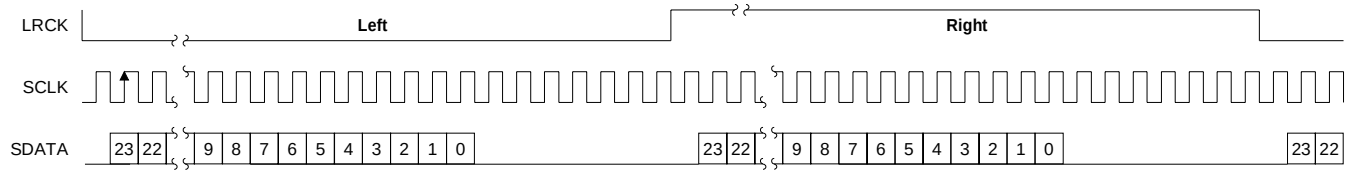
Internal Power-On Reset

The timing required to determine Control port mode and I^2S/SPI mode is based on an internal power-on reset. The internal power-on reset requires the power supply to exceed a threshold voltage. However, there is no external indication of when the internal reset is activated. If precise timing of the Control port and I^2S/SPI decisions is required, MCLK should not be applied until the power supply has stabilized.



MASTER	SLAVE
24-Bit Left Justified Data	24-Bit Left Justified Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x Fs	MCLK equal to 256x Fs

Figure 2. Serial Data Format 0, Stand-Alone Mode, DFS low. Left Justified.



MASTER	SLAVE
I^2S 24-Bit Data	I^2S 24-Bit Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x Fs	MCLK equal to 256x Fs

Figure 3. Serial Data Format 1, Stand-Alone Mode, DFS High. I^2S compatible

Master Clock - Control Port Mode

The master clock is the clock source for the delta-sigma modulator sampling (MCLKA) and digital filters (MCLKD). The required MCLKA/D frequency is determined by the desired Fs and the chosen Oversampling Mode. Table 2 shows some common master clock frequencies.

64× vs. 128× Oversampling Modes

The CS5396/97 can operate in a 64× Oversampling Mode with a 256× master clock (MCLKA/D) at a maximum sample rate of 100 kHz. The device can also operate in a 128× Oversampling Mode with a 512× master clock (MCLKA/D) where the maximum Fs is 50 kHz. Notice that the required master clock is 24.576 MHz for Fs equal to either 48 kHz in the 128× Oversampling Mode or 96 kHz in the 64× Oversampling Mode. The sampling mode is set via the control register which alters the decimation ratio of the digital filter. The 64× Oversampling Mode is the default mode. Table 2 shows some common clock frequencies for both modes. Refer to Appendix A for additional discussion of 64× vs. 128× Oversampling Modes.

LRCK (kHz)	Over-sampling	MCLKA/D (MHz)	SCLK (MHz)
32	64	8.192	2.048
44.1	64	11.2896	2.822
48	64	12.288	3.072
32	128	16.384	4.096
44.1	128	22.5792	5.6448
48	128	24.576	6.144
64	64	16.384	4.096
88.2	64	22.5792	5.6448
96	64	24.576	6.144

Table 2. Common Clock Frequencies

Serial Data Interface - Control Port Mode

The CS5396/97 supports two serial data formats which are selected via the control register. The digital output format determines the relationship between the serial data, left/right clock and serial clock. Figures 4 - 7 detail the interface formats. The serial data interface is accomplished via the serial data outputs; SDATA1 and SDATA2, serial data clock, SCLK, and the left/right clock, LRCK. The serial nature of the output data results in the left and right data words being read at different times. However, the samples within an LRCK cycle represent simultaneously sampled analog inputs.

Serial Data - Control Port Mode

The serial data block is presented in 2's-complement format with the MSB-first. The data is clocked from SDATA1 and SDATA2 by the serial clock and the channel is determined by the Left/Right clock. The full precision 24 bit data is available on SDATA1 and the output from the low group delay is available on SDATA2.

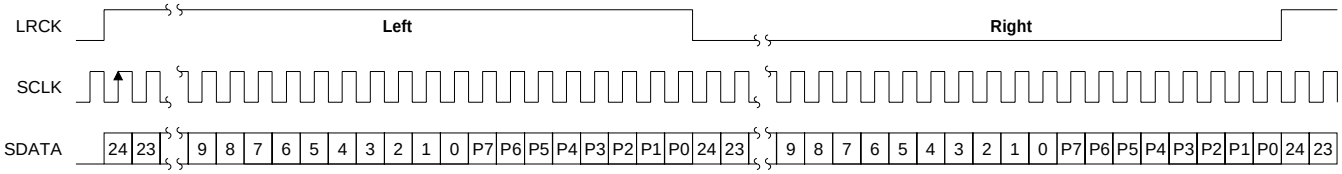
The serial data can be followed by 8 Peak Signal Level, PSL, bits as shown in Figures 4 - 7 if the PKEN bit is set. Refer to the Dual Audio Output section of this data sheet for further discussion of SDATA1 and SDATA2 options.

Serial Clock - Control Port Mode

The serial clock shifts the digitized audio data from the internal data registers via SDATA1 and SDATA2. SCLK is an output in Master Mode where internal dividers will divide the master clock by 4 to generate a serial clock which is 64× Fs in the 64× Oversampling Mode. In the 128× Oversampling Mode, internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 128× Fs. In Slave Mode, SCLK is an input with a serial clock typically between 48× and 128× Fs. It is recommended that SCLK be equal to 64× in the 64× Oversampling Mode and equal to 128× in the 128× Oversampling Mode to avoid possible system performance degradation due to interference effects.

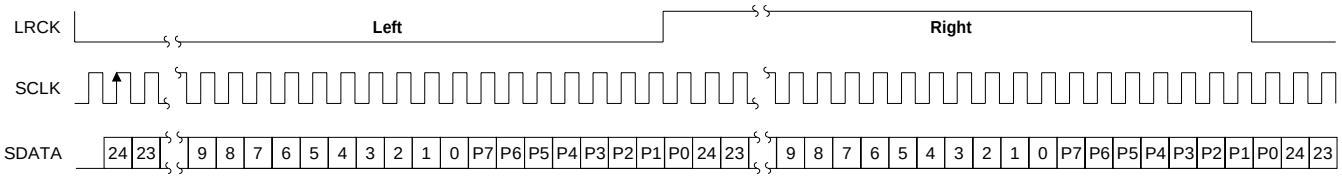
Left/Right Clock -Control Port Mode

The Left/Right clock, LRCK, determines which channel, left or right, is to be output on SDATA1



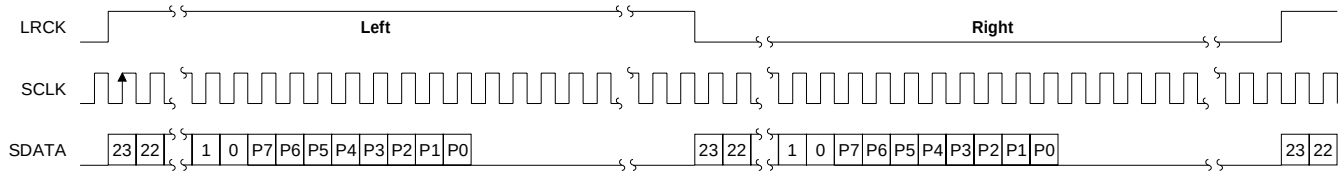
MASTER	SLAVE
24-Bit Left Justified Data	24-Bit Left Justified Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x Fs	MCLK equal to 256x Fs

Figure 4. Control Port Mode, Serial Data. Left Justified. 64x Oversampling Mode
The peak signal level bits are available only if Bit 6 of Byte 7 is set.



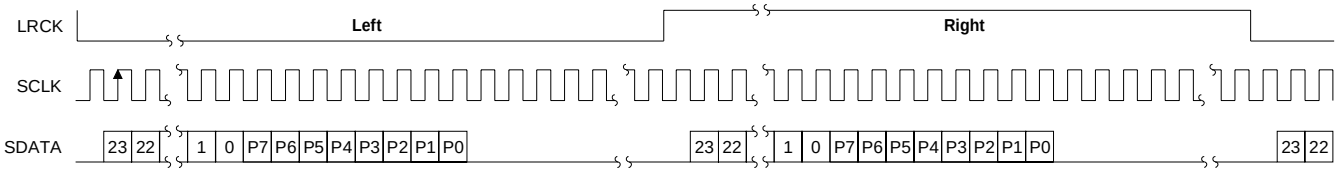
MASTER	SLAVE
I^2S 24-Bit Data	I^2S 24-Bit Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x Fs	MCLK equal to 256x Fs

Figure 5. Control Port Mode, Serial Data. I^2S Compatible. 64x Oversampling Mode.
The peak signal level bits are available only if Bit 6 of Byte 7 is set.



MASTER	SLAVE
24-Bit Left Justified Data	24-Bit Left Justified Data
Data Valid on Rising Edge of 128x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 512x Fs	MCLK equal to 512x Fs

Figure 6. Control Port Mode, Serial Data. Left Justified. 128x Oversampling Mode
The peak signal level bits are available only if Bit 6 of Byte 7 is set.



MASTER	SLAVE
I^2S 24-Bit Data	I^2S 24-Bit Data
Data Valid on Rising Edge of 128x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 512x Fs	MCLK equal to 512x Fs

Figure 7. Control Port Mode, Serial Data. I^2S Compatible. 128x Oversampling Mode.
The peak signal level bits are available only if Bit 6 of Byte 7 is set.

and SDATA2. In Master Mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs and synchronous to MCLKA/D.

Master Mode- Control Port Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from the master clock. In the 64× Oversampling Mode, internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 64× Fs and by 256 to generate a LRCK which is equal to Fs. In the 128× Oversampling Mode, internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 128× Fs and by 512 to generate a LRCK which is equal to Fs. The CS5396/97 is placed in the Master mode via the control register.

Slave Mode - Control Port Mode

LRCK and SCLK become inputs in SLAVE mode. LRCK must be externally derived from MCLKA/D and be equal to Fs. It is recommended that SCLK be equal to 64× in the 64× Oversampling Mode and equal to 128× in the 128× Oversampling Mode. Other frequencies are possible but may degrade system performance due to interference effects. The CS5396/97 is placed in the Slave mode via the control register.

Synchronization of Multiple Devices - Control Port Mode

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. The FSTART bit in register 1 controls the synchronization of the internal clocks and sampling process between the analog modulator and the digital filter. Multiple ADCs can be synchronized if the FSTART command is initiated on the same edge of MCLK. This can be accomplished by re-timing the CCLK clock with the falling edge of MCLK. This is a relatively simple matter if the ADCs have the same address. However, if the system requires the devices to have individual addresses, synchronization can be accomplished by;

1) Disable the address enable bit (ADDREN) in register 7

2) Issue a system broadcast FSTART command synchronized with CCLK.

3) Reset the ADDREN bit.

Power-up and Calibration - Control Port Mode

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by exiting the power-down mode. However, the voltage reference will take a much longer time to reach a final value due to the presence of external capacitance on the VREF pin. A time delay of approximately 10ms/µF is required after applying power to the device or after exiting a power down state.

A calibration of the tri-level delta-sigma modulator should always be initiated following power-up and after allowing sufficient time for the voltage on the external VREF capacitor to settle. This is required to minimize noise and distortion. It is also advised that the CS5396/97 be calibrated after the device has reached thermal equilibrium to maximize performance. A calibration sequence requires the following commands;

1) set the FSTART bit

2) set the GND CAL bit

3) set the CAL bit

4) Wait a minimum of 2050 LRCK periods in the 128x mode or 4100 LRCK periods in the 64x mode.

5) Remove GND CAL

High Pass Filter -Control Port Mode

The CS5396/97 includes a high pass filter after the decimator to remove the DC offsets introduced by

the analog buffer stage and the CS5396/97 analog modulator. The high pass filter can be defeated with the control register. It is also possible to write to the left/right offset registers to establish a predetermined offset.

The characteristics of this first-order high pass filter are outlined below for Fs equal to 48 kHz. The filter response scales linearly with sample rate.

Frequency response:	-3 dB @ 1.8 Hz
	-0.036 dB @ 20 Hz
Phase deviation:	5.3 degrees @ 20 Hz
Passband ripple:	None

Input Level Monitoring - Control Port Mode

The CS5396/97 includes independent Peak Input Level Monitoring for each channel. The analog-to-digital converter continually monitors the peak digital signal for both channels and records these values in the Active registers. This information can be transferred to the Output registers by writing the PU (Peak Update) bit which will also reset the Active register. The Active register contains the peak signal level since the previous peak update request. The 8-bit contents of the output registers are available in both interface modes. The peak signal level information is available in two formats - High Resolution Mode and Bar Graph Mode. The output format is controlled via the control register.

High Resolution Mode

Bits P7-P0 indicate the Peak Signal Level (PSL) since the previous peak update (or previous write of the PU bit). If the ADC input level is less than full-scale, bits P5-P0 represent the peak value from -60 dB to 0 dB of full scale in 1 dB steps. The PSL outputs are accurate to within 0.25 dB. Bit P6 provides a coarse means of determining an ADC input idle condition. Bit P7 indicates an ADC overflow condition if the ADC input level is greater than full-scale.

P7 - Overrange
0 - Analog input less than full-scale level
1 - Analog input greater than full-scale

P6 - Idle channel
0 - Analog input >-60 dB from full-scale
1 - Analog input <-60 dB from full-scale

P5 to P0 - Input Level Bits (1 dB steps)

Inputs <0 dB	P5 - P0
0 dB	000000
-1 dB	000001
-2 dB	000010
-60 dB	111100

Bar Graph Mode

This mode provides a decoded output format which indicates the peak input signal level in a “Bar Graph” format which can be used to drive front panel LEDs. This decoded output can be used to drive front panel LEDs.

Input Level	T7 - T0
Overflow	11111111
0 dB to -3 dB	01111111
-3 dB to -6 dB	00111111
-6 dB to -10 dB	00011111
-10 dB to -20 dB	00001111
-20 dB to -30 dB	00000111
-30 dB to -40 dB	00000011
-40 dB to -60 dB	00000001
< - 60 dB	00000000

Dual Digital Audio Outputs

The CS5396/97 contains two stereo digital audio output channels - SDATA1 and SDATA2. These audio output channels are completely independent, as SDATA1 can contain 24-bit audio data simultaneous with psychoacoustic audio data on SDATA2. Another example of this independence is 24-bit audio data output on SDATA1 simultaneously with a low group delay output on SDATA2.

The audio output formats are completely programmable through the I^2C/SPI µC interface. The output

formats include: inverted output, psychoacoustic output (16-bit, 18-bit, 20-bit), and low group delay output.

Psychoacoustic Filter

The CS5396/97 includes a programmable 10 tap digital filter which can be used to perform psychoacoustic noise-shaping of the audio spectrum if desired. The filter can implement a variety of 16-bit, 18-bit, or 20-bit noise-shaped responses by setting the digital filter coefficients. Further discussion of the psychoacoustic filter can be found in Appendix C.

Appendix B discusses an application using the psychoacoustic filter independently of the A/D converter function. In this mode, SDATA2 becomes an input to the psychoacoustic filter stage and SDATA1 is the digital audio output.

Low Group Delay Filter

The characteristics of the low group delay filter are shown in Figures 17 - 24.

µC Interface Formats

The device supports either SPI or I^2C interface formats. The CS5396/97 monitors the state of $\overline{CS}$ during power-up and will configure to an SPI interface if the pin is held low. Conversely, if the pin is held high, the port will configure to a I^2C interface.

SPI Mode

In SPI mode, $\overline{CS}$ is the chip select signal, CCLK is the µC bit clock and CDIN is the input data line from the microcontroller. Notice that it is not possible to read the CS5396/97 registers in SPI mode due to the lack of a data output pin.

To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN are the chip address, and must be zero. The eighth bit is a read/write indicator (R/$\overline{W}$) which must be low.

The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into the register designated by the MAP.

The CS5396/97 has a MAP auto increment, which will increment the MAP after each byte is written, allowing block writes of successive registers.

I^2C Mode

In I^2C mode, CDIN is a bidirectional data line. Data is clocked into and out of the part by CCLK.

The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. Use of the I^2C bus compatible interface requires a license from Philips. I^2C bus in a registered trademark of Philips Semiconductors.

Establishing the Chip Address in I^2C Mode

Connecting SDATA1 pin and $\overline{CS}$ to 5 volts during power-up will set the device to the Control Port and I^2C mode. However, the control port will not respond to CCLK and CDATA until the hold on the SDATA1 pin is released. The chip address can be set by:

1) Release the hold on the SDATA1 pin of the device to be addressed.
2) Program the chip address and set the Address Enable bit, addren, which will prevent further communication to this device without the correct address.
3) Repeat steps 1 and 2 for the remaining devices on the bus.

ANALOG CONNECTIONS - ALL MODES

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the

modulators via the AINR+/- and AINL+/- pins. Each analog input will accept a maximum of 2.0 Vpp. The + and - input signals are 180° out of phase resulting in a differential input voltage of 4.0 Vpp. Figure 8 shows the input signal levels for full scale.

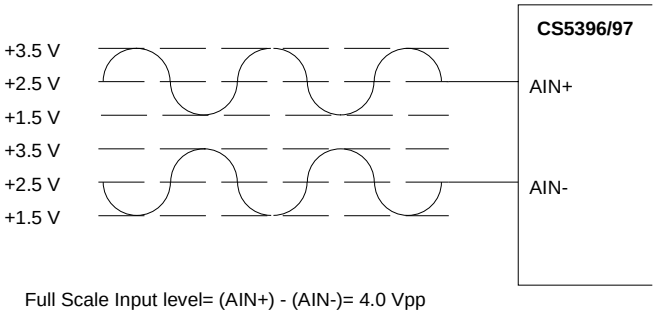


Figure 8. Full scale input voltage

The analog modulator samples the input at 6.144 MHz (MCLK=24.576 MHz) corresponding to Fs equal to 48 kHz in the 128× Oversampling Mode and Fs equal to 96 kHz in the 64× Oversampling Mode. The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are ($n \times 6.144$ MHz) ± the digital passband frequency, where n=0,1,2,...A 39 Ω resistor in series with the analog input and a 6.8 nF COG capacitor between the inputs will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output sample rate.

The on-chip voltage reference and the common mode voltage are available at VREF and VCOM for the purpose of decoupling only. However, due to the sensitivity of this node, the circuit traces attached to these pins must be minimal in length and no load current may be taken from VREF. It is possible to use VCOM as a reference voltage to bias the input buffer circuits, if the circuit trace is very short and VCOM is buffered at the converter (refer to the CDB53965/97). The recommended decoupling scheme for VREF, Figure 1, is a 470 µF electrolytic capacitor and a 0.1 µF ceramic capacitor connected from VREF to AGND. The recommended decoupling scheme for VCOM, Figure 1, is a 100 µF electrolytic capacitor and a 0.1 µF ceramic capacitor connected from VCOM to AGND.

GROUNDING AND POWER SUPPLY DECOUPLING - ALL MODES

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA and VL connected to a clean +5 V supply. VD, which powers the digital filter, should be run from the system +5 V logic supply, provided that it is not excessively noisy (< ±50 mV pk-to-pk). Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. The VREF decoupling capacitors, particularly the 0.01 µF, must be positioned to minimize the electrical path from VREF and pin 3, AGND. The CDB5396/97 evaluation board demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

DIGITAL FILTER PLOTS

Figures 9-24 show the performance of the digital filters included in the ADC. All plots are normalized to Fs. Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with Fs.

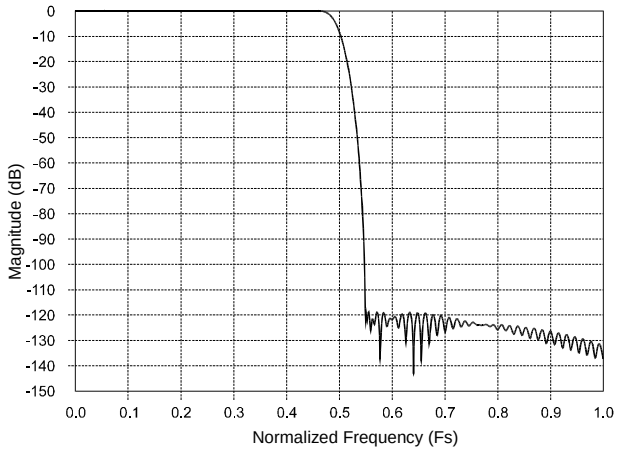


Figure 9. CS5396 Stop Band Attenuation

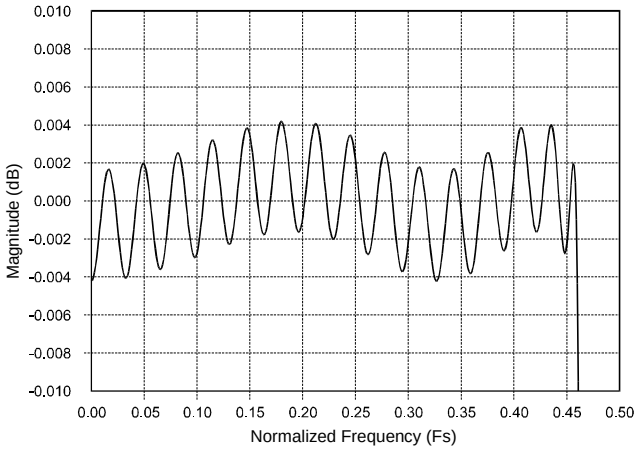


Figure 10. CS5396 Passband Ripple

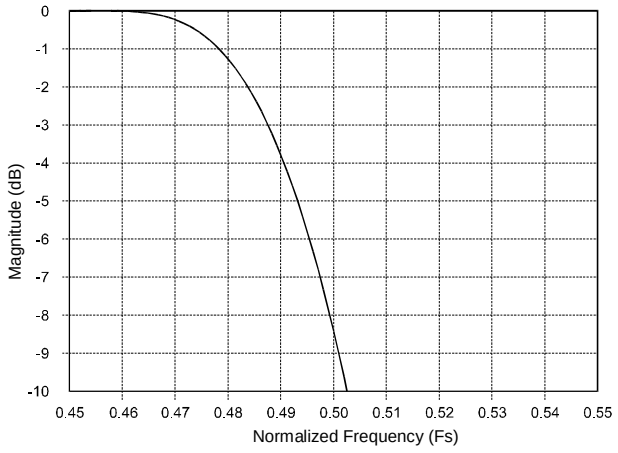


Figure 11. CS5396 Transition Band

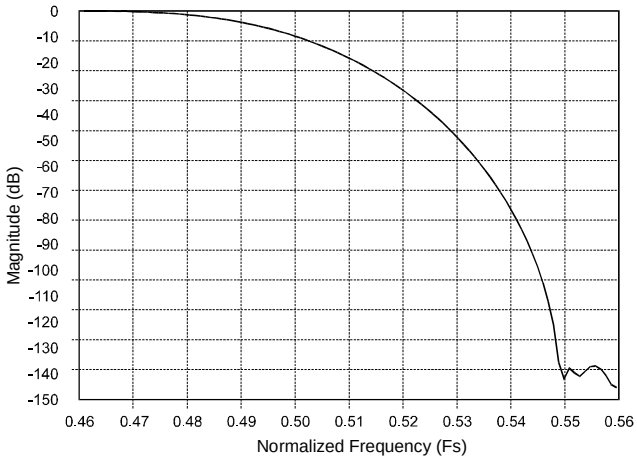


Figure 12. CS5396 Transition Band

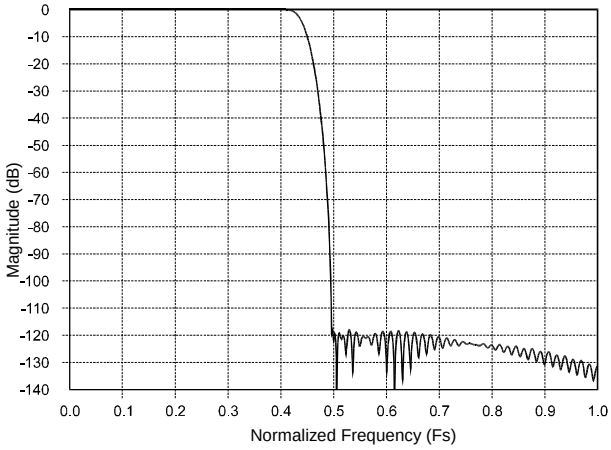


Figure 13. CS5397 Stop Band Attenuation

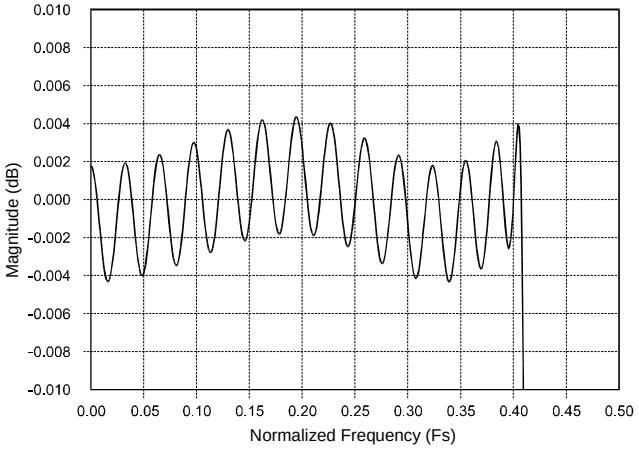


Figure 14. CS5397 Passband Ripple

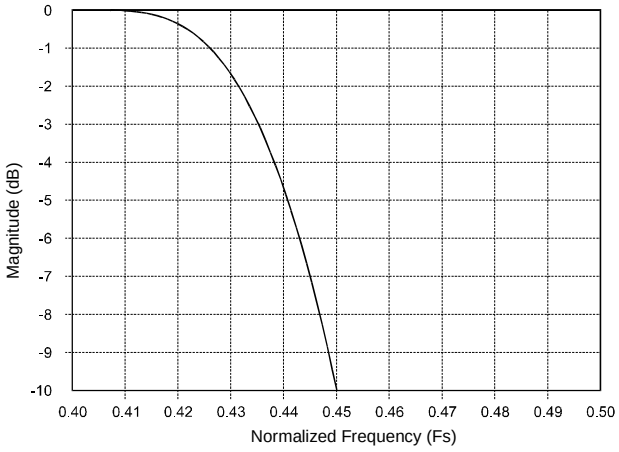


Figure 15. CS5397 Transition Band

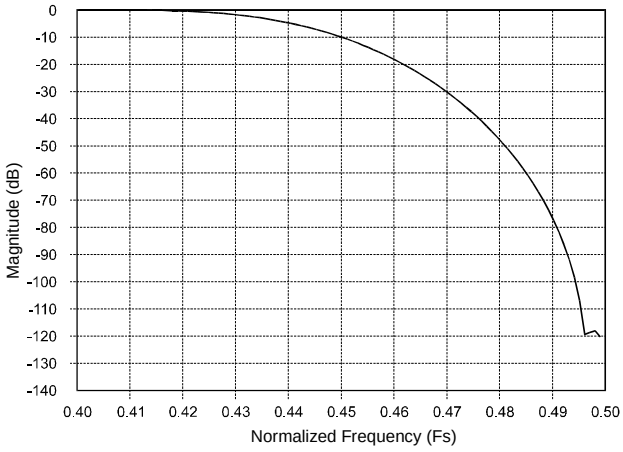


Figure 16. CS5397 Transition Band

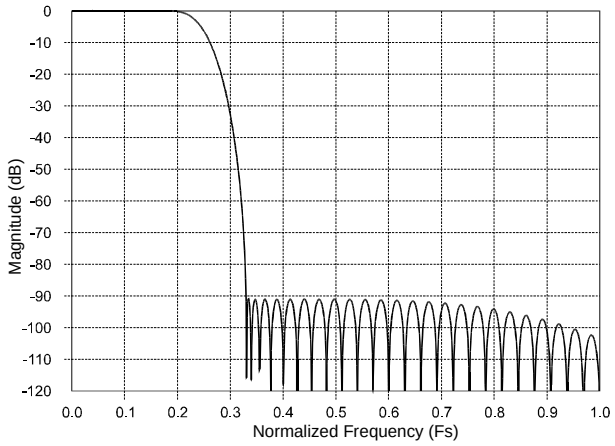


Figure 17. Low Group Delay Filter Stop Band Attenuation 64x Oversampling Mode

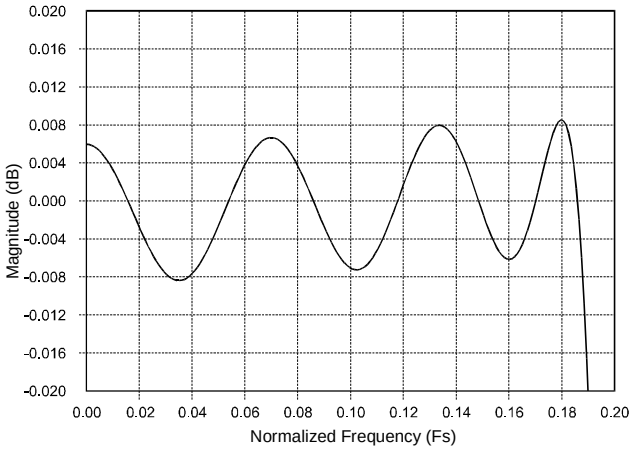


Figure 18. Low Group Delay Filter Passband Ripple 64x Oversampling Mode

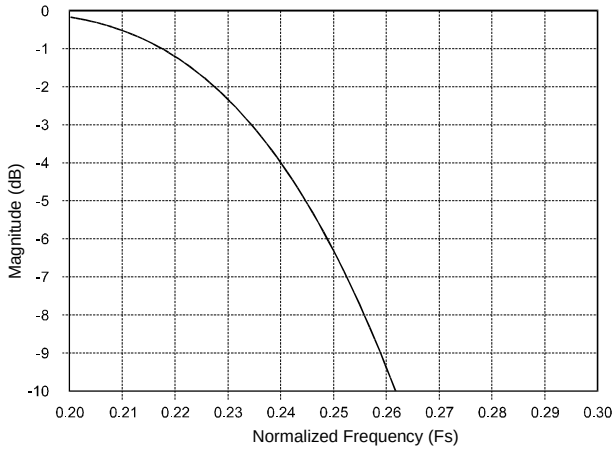


Figure 19. Low Group Delay Filter Transition Band 64x Oversampling Mode

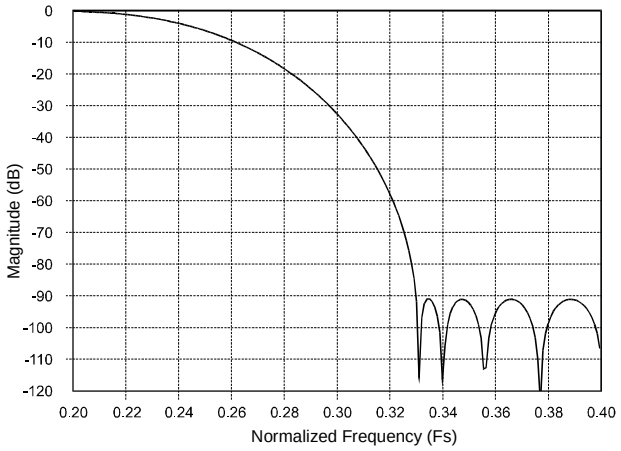


Figure 20. Low Group Delay Filter Transition Band 64x Oversampling Mode

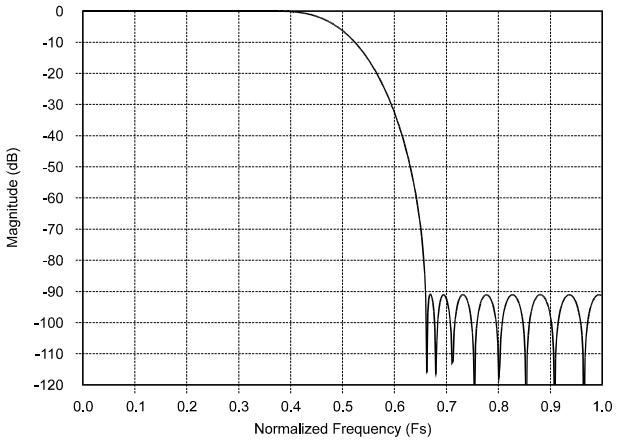


Figure 21. Low Group Delay Filter Stop Band Attenuation 128x Oversampling Mode

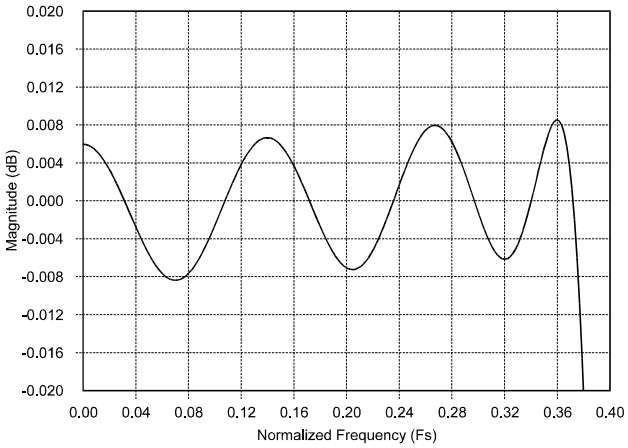


Figure 22. Low Group Delay Filter Passband Ripple 128x Oversampling Mode

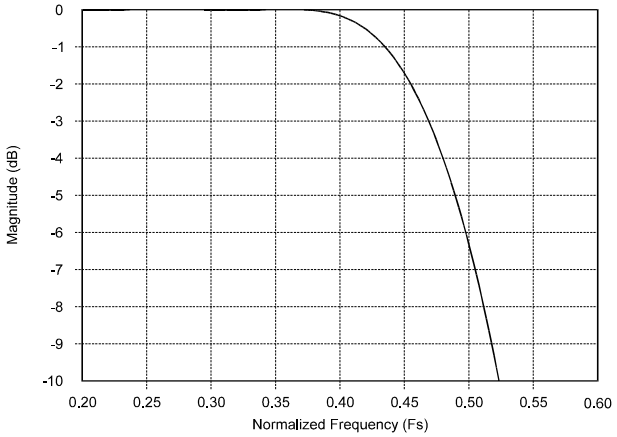


Figure 23. Low Group Delay Filter Transition Band 128x Oversampling Mode

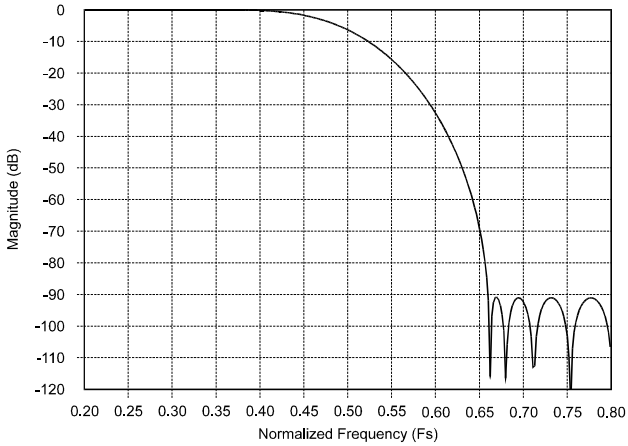


Figure 24. Low Group Delay Filter Transition Band 128x Oversampling Mode

REGISTER DESCRIPTION

** “default” ==> bit status after power-up-sequence

Analog control (address 00000001)

7	6	5	4	3	2	1	0
fstart	gndcal	aapd	adpd	1bit			
0	0	0	0	0			

FSTART (Frame start)Default = ‘0’.

This bit must be set to ‘1’ to synchronize the modulator output and the decimation filter input and is automatically reset to ‘0’ after a “fstart” pulse is sent to the analog and digital block.

GNDCAL (Ground calibration enable)

Default = ‘0’.

Modulator input is tied to internal “Vcom” when this bit is ‘1’.

AAPD (Analog Section of modulator in power down)

Default = ‘0’.

The analog section of the modulator is in power down mode when aapd = ‘1’.

ADPD (Digital Section of modulator in power down)

Default = ‘0’.

The digital section on the modulator is in power down mode when adpd = ‘1’.

TEST BIT Default =’0’.

Must remain at 0.

Mode (address 00000010)

7	6	5	4	3	2	1	0
128x/$\overline{64x}$	cal	change_sign	_LR/LL	_hpen	s/_m	DFS	mute
0	0	0	0	0	0	0	0

128x/$\overline{64x}$ Default = ‘0’.

Oversampling ratio is 128 when this bit is ‘1’ and 64 when this bit is ‘0’.

CAL (System calibration enable)

Default = ‘0’.

Setting this bit to ‘1’ will initiate calibration.

This bit is automatically reset to ‘0’ following calibration.

Change_sign (Change Sign enable)

Default = ‘0’.

A ‘1’ will interchange the analog input paths within each channel resulting in a phase inversion of the analog signal. This bit applies to both channels.

_LR/LL (Left-Right output disable) Default = ‘0’.

If this bit is ‘0’, SDATA1 will output the Left and Right channel data from the sdata1 source and SDATA2 will output the Left and Right channel data from the sdata2 source as described elsewhere in the data sheet.

If this bit is set to ‘1’, the Left channel data from sdata1 source and sdata2 source (stored in Audio port register) will be sent out in SDATA1. SDATA2 will output all the Right channel data.

HPEN (HP enable) Default = '0'.
The highpass filter will be disabled when _HPEN = '1'. The highpass filter will be automatically enabled following calibration.

S/_M (Slave / Master mode) Default = '0'.
In master mode, LRCK, and SCLK are outputs. In slave mode, LRCK and SCLK are inputs. This bit is ignored when sdata1 is used as input port in "fir2in" or "psychoin" mode (refer to Digital control & Tag register and Appendix B).

DFS (Digital Format Select)Default = '0'.
Output of serial data complies with I^2S standard when DFS is 1. Output of serial data is Left Justified when DFS is 0.

MUTE Default = '0'.
Data at SDATA1 and SDATA2 is always '0' when this set to '1'.

Audio port (address 00000011)

7	6	5	4	3	2	1	0
24bit (sdata1)	24bit (sdata2)	psycho (sdata1)	psycho (sdata2)	psel18/_16	psel20/_16	lgd (sdata1)	lgd (sdata2)
1	0	0	0	0	0	0	1

24bit(SDATA1) Default = '1'.
A '1' enables the serial audio port 1 to transmit the 24-bit high precision output.
This bit must be set to '0' to enable other SDATA1 output options.

24bit(SDATA2) Default = '0'.
A '1' enables the serial audio port 2 to transmit 24-bit high precision output. This bit must be set to '0' to enable other SDATA2 output options.

psycho(SDATA1) Default = '0'.
psychoacoustic output will be the data at the serial audio port 1 if this bit is '1' and all other bits of the port are set to '0'.

psycho(SDATA2) Default = '0'.
psychoacoustic output will be the data at the serial audio port 2 if this bit is '1' and all other bits of the port are set to '0'.

psel18/_16(Psycho 18bit or 16bit)
Default = '0'.
This bit indicates the number of output bit if the psychoacoustic filter is chosen as output. A '0' here allows 16 bits output whereas a '1' allows 18 bits output as long as "psel20/_16" is '0'.

psel20/_16(Psycho 20bit)
Default = '0'.
This bit has the highest priority when setting the number of output bit of psychoacoustic filter. If this bit is '1', the output is set to 20-bit regardless of the status of "psel18/_16".

LGD(sdata1) Default = '0'.
24-bit low-group-delay filter output will go through a highpass filter if "_hpen" bit in the Mode register is '0'. The LGD output will be the data at the serial audio port 1 if this bit is '1' and all other bits of the port set to '0'.

LGD(sdata2) Default = '1'.

24-bit low-group-delay filter output will go through a high passfilter if "_hpen" bit in the Mode register is '0'. If "_hpen" is '1', data at the serial audio port will derive directly from the LGD filter output.
If more than 1 bit is set for sdata2, low-group-delay filter output will be selected for output at the port.

Test Mode 0(address 00000100)

7	6	5	4	3	2	1	0
aoverflow	doverflow	fir1_en	fir1(LRCK)	_psydither	dstart1	dstart0	
0	0	0	0	0	0	0	

aoverflow — A '1' indicates an overflow condition occurs in the modulator. This bit is reset by reading the register.

doverflow — A '1' indicates an overflow condition occurs in the decimation filter. This bit is reset by reading the register.

fir1_en(sdata) — Default = '0'.
Test purpose only.

fir1L_R(fir1 L channel enable)
Default = '0'.
Test purpose only.

_psydither(psychoacoustic filter dither disable)
Default = '0'.
A '0' means adding dither in the psychoacoustic filter.

dstart1, dstart2(dstart control bits)
Default = '00'.
Test purpose only.

Test Mode 1(add 00000101)

7	6	5	4	3	2	1	0
test mode. reserved for factory use only							

FOR FACTORY USE ONLY

Chip Address (address 00000110)

7	6	5	4	3	2	1	0
	caddr6	caddr5	caddr4	caddr3	caddr2	caddr1	caddr0
	0	0	0	0	0	0	0

caddr(6-0) (chip address (bit6 to bit0))
Default = '0000000'.
This is used to store the programmable chip address for I^2C and SPI mode.
When more than 1 device are connected to the I^2C or SPI buses and using chip address is necessary, chip address set up is done by:
1) Hold the SDATA1 pin of every chip to '1' during power up.

2) Release the SDATA1 pin of the chip that is going to be programmed with chip address.
3) Send chip address and “addren”=’1’ (in Register 7) through the serial control port. (The remaining devices will not repond to this request.)
4) Repeat step 2) and step 3) for to other chips one-by-one. (SDATA1 output is tri-stated until it is released from pull up.)

Digital Control & Peak Signal Level (address 00000111)

7	6	5	4	3	2	1	0
ADDREN	pken	pkupdate	hr/_bg		ddpd	fir2in	psychoin
0	0	0	0		0	0	0

addren(chip address enable)
Default = ‘0’.
When this bit is ‘0’, no chip address comparison is done. The chip will response to all the request from Control Port.
When this bit is ‘1’, the chip responds to the µC only if the chip address from the µC matches the chip address stored in “caddr(6-0)”.

pken(PEAK enable) Default = ‘0’.
PSL bits calculation is based on the high precision 24-bit output.
PSL bits output follows the serial audio port that sends out 24-bit data.
If this bit is disabled, the PSL bits location on the output stream will be replaced by zeros.

pkupdate(PEAK update)
Default = ‘0’.
A ‘0’ to ‘1’ transition will load the peak value (since the last update) to the appropriate serial audio port. The internal peak register will then reset to ‘0’.

hr/_bg(PEAK display format)
Default = ‘0’.
High resolution tag format (hr/_bg=’1’) converts the 24-bit decimation filter output into 1 dB step.
Bar Graph tag format (hr/_bg=’0’) allows LCD display format of the 24-bit output with 8 discrete values.

ddpd(digital filter power down enable)
Default = ‘0’.
The digital filter and serial audio port is in power down mode when ddpd = ‘1’.

fir2in(external fir2 input enable)
Default = ‘0’.
Input of 2nd stage decimation filter is taken from the sdata2 port. The input data will be decimated by 2 and then output to sdata1 of serial audio port.

psychoin (external psychoacoustic filter input enable)
Default = ‘0’.
Input of psychoacoustic filter is taken from the sdata2 port. The 24-bit input data will be truncated in psychoacoustic filter to the chosen output word length and then output to sdata1 of serial audio port.

R_cal_coeff (address 00001000 - 00001010)

7	6	5	4	3	2	1	0
ralpha (bit7)	ralpha (bit6)	ralpha (bit5)	ralpha (bit4)	ralpha (bit3)	ralpha (bit2)	ralpha (bit1)	ralpha (bit0)
0	0	0	0	0	0	0	0
ralpha (bit15)	ralpha (bit14)	ralpha (bit13)	ralpha (bit12)	ralpha (bit11)	ralpha (bit10)	ralpha (bit9)	ralpha (bit8)
0	0	0	0	0	0	0	0
ralpha (bit23)	ralpha (bit22)	ralpha (bit21)	ralpha (bit20)	ralpha (bit19)	ralpha (bit18)	ralpha (bit17)	ralpha (bit16)
0	1	0	0	0	0	0	0

Default = '0000 0000 0000 0000 0100 0000'. (represents 1)
The right channel calibration factor is stored in these registers with MSB in bit 7 of register address 00001010.
This value is updated after every calibration cycle.
User can read from or write to this calibration factor through the serial control port.

L_cal_coeff (address 00001011 - 00001101)

7	6	5	4	3	2	1	0
lalpha (bit7)	lalpha (bit6)	lalpha (bit5)	lalpha (bit4)	lalpha (bit3)	lalpha (bit2)	lalpha (bit1)	lalpha (bit0)
0	0	0	0	0	0	0	0
lalpha (bit15)	lalpha (bit14)	lalpha (bit13)	lalpha (bit12)	lalpha (bit11)	lalpha (bit10)	lalpha (bit9)	lalpha (bit8)
0	0	0	0	0	0	0	0
lalpha (bit23)	lalpha (bit22)	lalpha (bit21)	lalpha (bit20)	lalpha (bit19)	lalpha (bit18)	lalpha (bit17)	lalpha (bit16)
0	1	0	0	0	0	0	0

Default = '0000 0000 0000 0000 0100 0000'. (represents 1)
The left channel calibration factor is stored in these registers with MSB in bit 7 of register address 00001101.
This value is updated after every calibration cycle.
User can read from or write to this calibration factor through the serial control port.

L_offset (address 00001110)

7	6	5	4	3	2	1	0
los(bit13)	los(bit12)	los(bit11)	los(bit10)	los(bit9)	los(bit8)	los(bit7)	los(bit6)
0	0	0	0	0	0	0	0

Default = '0000 0000'.
User can read or write this offset through the serial control port.

R_offset (address 00001111)

7	6	5	4	3	2	1	0
ros(bit13)	ros(bit12)	ros(bit11)	ros(bit10)	ros(bit9)	ros(bit8)	ros(bit7)	ros(bit6)
0	0	0	0	0	0	0	0

Default = '0000 0000'.
User can read or write this offset through the serial control port.

Psycho coeff (address 00010000 - 00011000)

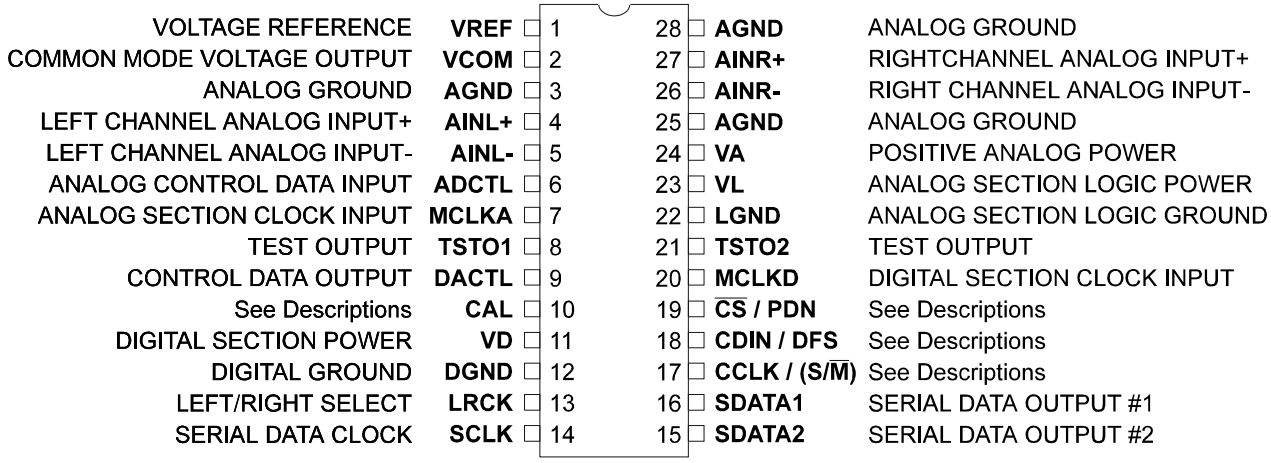
7	6	5	4	3	2	1	0
pc8(bit8)	pc8(bit7)	pc0(bit5)	pc8(bit4)	pc8(bit3)	pc8(bit2)	pc8(bit1)	pc8(bit0)
1	1	0	1	1	0	1	0
pc7(bit8)	pc7(bit7)	pc1(bit5)	pc7(bit4)	pc7(bit3)	pc7(bit2)	pc7(bit1)	pc7(bit0)
0	0	1	1	0	1	0	1
pc6(bit8)	pc6(bit7)	pc2(bit5)	pc6(bit4)	pc6(bit3)	pc6(bit2)	pc6(bit1)	pc6(bit0)
1	1	0	0	0	0	1	0
pc5(bit8)	pc5(bit7)	pc3(bit5)	pc5(bit4)	pc5(bit3)	pc5(bit2)	pc5(bit1)	pc5(bit0)
0	1	0	0	0	0	1	1
pc4(bit8)	pc4(bit7)	pc4(bit5)	pc4(bit4)	pc4(bit3)	pc4(bit2)	pc4(bit1)	pc4(bit0)
1	1	0	0	1	0	1	1
pc3(bit8)	pc3(bit7)	pc5(bit5)	pc3(bit4)	pc3(bit3)	pc3(bit2)	pc3(bit1)	pc3(bit0)
0	0	1	0	0	0	1	1
pc2(bit8)	pc2(bit7)	pc6(bit5)	pc2(bit4)	pc2(bit3)	pc2(bit2)	pc2(bit1)	pc2(bit0)
1	1	1	0	1	1	0	0
pc1(bit8)	pc1(bit7)	pc7(bit5)	pc1(bit4)	pc1(bit3)	pc1(bit2)	pc1(bit1)	pc1(bit0)
0	0	0	0	1	0	0	1
pc0(bit8)	pc0(bit7)	pc8(bit5)	pc0(bit4)	pc0(bit3)	pc0(bit2)	pc0(bit1)	pc0(bit0)
1	1	1	1	1	1	1	1

H1 Default = ‘1101 1010’.
H2 Default = ‘0011 0101’.
H3 Default = ‘1100 0010’.
H4 Default = ‘0100 0011’.
H5 Default = ‘1100 1011’.

Please see Appendix C at the end of this document

of binary point. User can read or write one or all of the coefficients through the serial control port.

PIN DESCRIPTIONS



Power Supply Connections

VA - Positive Analog Power, Pin 24.

Positive analog supply. Nominally +5 volts.

VL - Positive Logic Power, Pin 23.

Positive logic supply for the analog section. Nominally +5 volts.

AGND - Analog Ground, Pin 3, 25 and 28.

Analog ground reference.

LGND - Logic Ground, Pin 22

Ground for the logic portions of the analog section.

VD - Positive Digital Power, Pin 11.

Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, Pin 12.

Digital ground for the digital section.

Analog Inputs

AINR-, AINR+ - Differential Right Channel Analog Inputs, Pin 26, 27.

Analog input connections for the right channel differential inputs. Nominally 4.0 Vpp differential for full-scale digital output.

AINL-, AINL+ - Differential Left Channel Analog Inputs, Pin 4,5.

Analog input connections for the left channel differential inputs. Nominally 4.0 Vpp differential for full-scale digital output.

Analog Outputs

VCOM - Common Mode Voltage Output, Pin 2.

Nominally +2.5 volts. Requires a 100 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor for decoupling to AGND. Caution is required if this output is to be used to bias the analog input buffer circuits. Refer to text.

VREF - Voltage Reference Output, Pin 1.

Nominally +4.0 volts. Requires a 470 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor for decoupling to AGND.

Digital Inputs

ADCTL - Analog Control Input, Pin 6.

Must be connected to DACTL. This signal enables communication between the analog and digital circuits.

MCLKA - Analog Section Input Clock, Pin 7.

This clock is internally divided and controls the delta-sigma modulators. The required MCLKA frequency is determined by the desired output sample rate (Fs). MCLKA of 24.576 MHz corresponds to an Fs of 96 kHz in 64x Oversampling Mode and 48 kHz in 128x Oversampling Mode.

MCLKD - Digital Section Input Clock, Pin 20.

MCLKD clocks the digital filter and must be connected to MCLKA. The required MCLKD frequency is determined by the desired output sample rate (Fs). MCLKD of 24.576 MHz corresponds to an Fs of 96 kHz in 64x Oversampling Mode and 48 kHz in 128x Oversampling Mode.

Digital Input Pin Definitions for Stand-Alone MODE

DFS - Digital Format Select, Pin 18.

The relationship between LRCK, SCLK and SDATA is controlled by the DFS pin. When high, the serial output data format is I^2S compatible. The serial data format is left-justified when low.

PDN - Power-Down, Pin 19.

When high, the device enters power-down. Upon returning low, the device enters normal operation. Calibration of the device is required following release of power-down.

S/$\overline{M}$ - Slave or Master Mode, Pin 17.

When high, the device is configured for Slave mode where LRCK and SCLK are inputs. The device is configured for Master mode where LRCK and SCLK are outputs when S/$\overline{M}$ is low.

CAL - Calibration, Pin 10.

Activates the calibration of the tri-level delta-sigma modulator.

Digital Pin Definitions for CONTROL-PORT MODE

CDIN - Control Port Data Input, Pin 18.

Control port data input for SPI mode.
Control port data input and output for I^2C mode.

CS - Chip Select Input, Pin 19.

Control port chip select for SPI mode. The CS5396/97 monitors the state of $\overline{CS}$ during power-up and will configure to an SPI interface if this pin is held low. Conversely, if held high, the port will configure to a I^2C interface.

CCLK - Control Port Clock Input, Pin 17.

Control port clock input pin for both I^2C and SPI modes.

CAL - Calibration, Pin 10.

CAL pin is not functional in Control Port Mode and should be connected to ground.

Digital Outputs

DACTL- Digital to Analog Control Output, Pin 9.

Must be connected to ADCTL. This signal enables communication from the digital circuits to the analog circuits.

SDATA1 - Digital Audio Data Output #1, Pin 16.

Stand-Alone Mode - The 24-bit audio data is presented MSB first, in 2's complement format.
Control Port Mode - The 24 audio data bits are presented MSB first, in 2's complement format. The audio data can be followed by 8 Peak Signal Level bits which indicate the peak signal level. The additional audio data options include; 16, 18, or 20-bit data with or without psychoacoustically optimized dither; or the output of the Low Group Delay filter. The SDATA1 output is completely independent from SDATA2. The mode selection between Stand-Alone and Control Port mode is determined by the state of the SDATA1 pin during power-up. A 47 kΩ pull-up resistor on SDATA1 will select the Control Port mode. However, the control port will not response to CCLK and CDIN until the pull-up on the SDATA1 pin is released.

SDATA2 - Digital Audio Data Output #2, Pin 15.

Stand-Alone Mode - The 24-bit low group delay audio data is presented MSB first, in 2's complement format.

Control Port Mode - The 24-bit low group delay audio data is presented MSB first, in 2's complement format. The audio data can be followed by 8 peak detect bits which indicate the peak signal level. The additional audio data options include; the standard 24-bit word; 16, 18, or 20-bit data with or without psychoacoustically optimized dither. The SDATA2 output is completely independent from SDATA1.

Digital Inputs or Outputs

LRCK - Left/Right Clock, Pin 13.

LRCK determines which channel, left or right, is to be output on SDATA1 and SDATA2. In master mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs.

Stand-Alone Mode - The relationship between LRCK, SCLK and SDATA is controlled by the Digital Format Select (DFS) pin.

Control Port Mode - The relationship between LRCK, SCLK and SDATA is controlled by the control register.

SCLK - Serial Data Clock, Pin 14.

Stand-Alone Mode- Clocks the individual bits of the serial data from SDATA1 and SDATA2. In master mode, SCLK is an output clock at 64x Fs. In slave mode, SCLK is an input which requires a continuously supplied clock at any frequency from 48x to 128x Fs (64x is recommended). The relationship between LRCK, SCLK and SDATA is controlled by the Digital Format Select (DFS) pin.

Control Port Mode - Clocks the individual bits of the serial data from SDATA1 and SDATA2. In master mode, SCLK is an output clock at 128x the output sample rate in the 128x Oversampling Mode and 64x the output sample rate in the 64x Oversampling Mode.

In slave mode, SCLK is an input, which requires a continuously supplied clock at any frequency from 32x to 128x the output sample rate. A 128x SCLK is preferred in the 128x Oversampling Mode and 64x SCLK is preferred in the 64x Oversampling Mode. The relationship between LRCK, SCLK and SDATA is controlled by the control register.

Miscellaneous

TSTO1, TSTO2 - Test Outputs, Pins 8 and 21.

These pins are intended for factory test outputs. They must not be connected to any external component or any length of circuit trace.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

ADDITIONAL INFORMATION

1) "Techniques to Measure and Maximize the Performance of a 120 dB, 24-bit, 96 kHz A/D Integrated Circuit" by Steven Harris, Steven Green and Ka Leung. Paper presented at the 103rd Convention of the Audio Engineering Society, September 1997.

2) "A 120 dB Dynamic Range, 96 kHz, 24-bit Analog-to-Digital Converter" by Kafai Leung, Sarah Zhu, Ka Leung and Eric Swanson. Paper presented at the 102nd Convention of the Audio Engineering Society, March 1997.

3) A 5 V, 118 dB Delta Sigma Analog-to-Digital Converter for Wideband Digital Audio by Ka Y. Leung, Eric J. Swanson, Kafai Leung, Sarah S. Zhu. Presented at ISSCC February, 1997, paper FP 13.6

4) "How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters" by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.

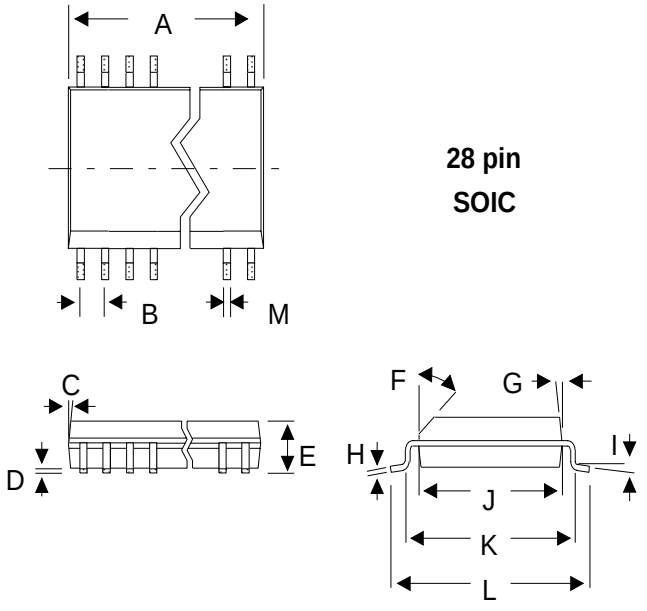
5) "The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADCs" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

6) "A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range" by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

7) "An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

8) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

PACKAGE DIMENSIONS



28 pin
SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.53	18.03	0.690	0.710
B	1.27 BSC		0.050 BSC	
C	7° NOM		7° NOM	
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

APPENDIX C: PSYCHOACOUSTIC FILTER

The psychoacoustic filter in the CS5396 is based on the paper: "Robert A. Wannamaker, Psychoacoustically Optimal Noise Shaping, Journal of the Audio Engineering Society, Vol 40, No 7/8, 1992 July/August." The default coefficients in the CS5396 are the FIR 9-tap filter coefficients described in Table 3 of the paper. Since the effective noise shaping function is (1-H), the CS5396 registers save the (1-H) function coefficients. Therefore, the negative of each filter coefficient is stored in the registers. Each coefficient is represented as a binary 2's complement number where the 4 MSB's represent the whole number of the coefficient and the 4 LSB's represent the fractional portion truncated to 4 binary bits.

Default Coefficients as listed in "Robert A. Wannamaker, Psychoacoustically Optimal Noise Shaping"

a1 = 2.412
a2 = -3.370
a3 = 3.937
a4 = -4.174
a5 = 3.353
a6 = -2.205
a7 = 1.281
a8 = -0.569
a9 = 0.0847

Coefficient conversion example 1:

a1 = 2.412

a1 = (0010.0110) binary repesentation with the fractional portion truncated to 4 bits.

-a1 = -(0010.0110) binary representation

-a1 = 1101.1010 in two's complement

this value is stored in register 10h.

Coefficient conversion example 2:

a2 = -3.370

-a2 = 3.370

-a2 = 0011.0101 binary repesentation with the fractional portion truncated to 4 bits.

-a2 = 0011.0101 in 2's complement

this value is stored in register 11h.

PSYCHO-ACOUSTIC FILTER COEFFICIENTS

7	6	5	4	3	2	1	0
MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB

Access:

R/W in I2C and write only in SPI

Filter coefficient a1 (address 10h)

Filter coefficient a2 (address 11h)

Filter coefficient a3 (address 12h)

Filter coefficient a4 (address 13h)

Filter coefficient a5 (address 14h)

Filter coefficient a6 (address 15h)

Filter coefficient a7 (address 16h)

Filter coefficient a8 (address 17h)

Filter coefficient a9 (address 18h)

Default:

a1 - 1101 1010
a2 - 0011 0101
a3 - 1100 0010
a4 - 0100 0011
a5 - 1100 1011
a6 - 0010 0011
a7 - 1110 1100
a8 - 0000 1001
a9 - 1111 1111

BURR - BROWN®

PCM1702P
PCM1702U

BiCMOS Advanced Sign Magnitude 20-Bit DIGITAL-TO-ANALOG CONVERTER

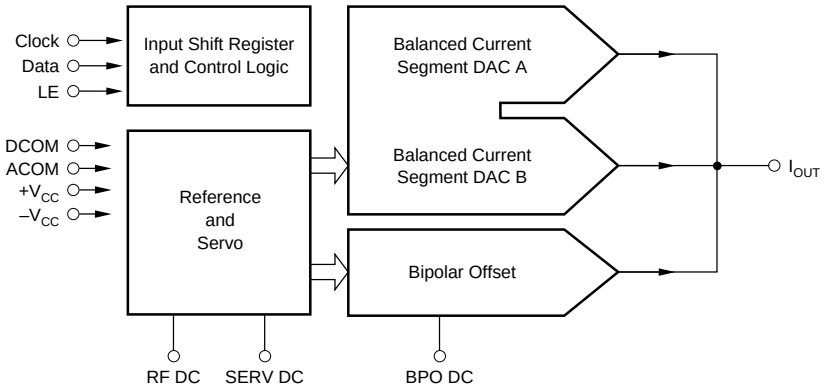
FEATURES

- **ULTRA LOW –96dB max THD+N (No External Adjustment Required)**
- **NEAR-IDEAL LOW LEVEL OPERATION**
- **GLITCH-FREE OUTPUT**
- **120dB SNR TYP (A-Weight Method)**
- **INDUSTRY STD SERIAL INPUT FORMAT**
- **FAST (200ns) CURRENT OUTPUT (±1.2mA)**
- **CAPABLE OF 16X OVERSAMPLING**
- **COMPLETE WITH REFERENCE**
- **LOW POWER (150mW typ)**

DESCRIPTION

The PCM1702 is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB typ with a full scale output). Incorporated into the PCM1702 is an advanced sign magnitude architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM1702 also features a very low noise (120dB typ SNR: A-weighted method) and fast settling current output (200ns typ, 1.2mA step) which is capable of 16X oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1175B
Printed in U.S.A. June, 1995

SPECIFICATIONS

All specifications at 25°C, $\pm V_{CC}$ and $+V_{DD}$ = ±5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM1702P/U, -J, -K MIN	TYP	MAX	UNITS
RESOLUTION		20			Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale, with A-weight			110		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.4		$+V_{DD}$	V
V_{IL}		0		0.8	V
I_{IH}	$V_{IH} = +V_{DD}$			±10	µA
I_{IL}	V_{IL} = 0V			±10	µA
Data Format			Serial, MSB First, BTC[1]		
Input Clock Frequency			12.5	20.0	MHz
TOTAL HARMONIC DISTORTION + N[2]					
P/U V_O = 0dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–92	–88	dB
V_O = –20dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–82	–74	dB
V_O = –60dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–46	–40	dB
P/U, -J V_O = 0dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–96	–92	dB
V_O = –20dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–83	–76	dB
V_O = –60dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–48	–42	dB
P/U, -K V_O = 0dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–100	–96	dB
V_O = –20dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–84	–80	dB
V_O = –60dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–50	–44	dB
ACCURACY					
Level Linearity	At –90dB Signal Level		±0.5		dB
Gain Error			±0.5	±3	%
Bipolar Zero Error[5]			±0.25		%
Gain Drift	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±5		ppm of FSR/°C
Warm-up Time			1		minute
IDLE CHANNEL SNR[6]	Bipolar Zero, A-weighted Filter	110	120		dB
ANALOG OUTPUT					
Output Range			±1.2		mA
Output Impedance			1.0		kΩ
Settling Time	(±0.003% of FSR, 1.2mA Step)		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
Supply Voltage Range: $+V_{CC} = +V_{DD}$		+4.75	+5.00	+5.25	V
$-V_{CC} = -V_{DD}$		–4.75	–5.00	–5.25	V
Combined Supply Current: $+I_{CC}$	$+V_{CC} = +V_{DD} = +5V$		+5.00	+9.0	mA
Combined Supply Current: $-I_{CC}$	$-V_{CC} = -V_{DD} = -5V$		–25.00	–41.0	mA
Power Dissipation	$\pm V_{CC} = \pm V_{DD} = \pm 5V$		150	250	mW
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+125	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (4) D/A converter output frequency (signal level). (5) Offset error at bipolar zero. (6) Measured using an OPA627 and 5kΩ feedback and an A-weighted filter.

ABSOLUTE MAXIMUM RATINGS (DIP Package)

Power Supply Voltage	±6.5VDC
Input Logic Voltage	DGND—0.3V~+V_{DD}+0.3V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Power Dissipation	500mW
Lead Temperature (soldering, 10s)	260°C

ABSOLUTE MAXIMUM RATINGS (SOP Package)

Power Supply Voltage	±6.5VDC
Input Logic Voltage	DGND—0.3V~+V_{DD}+0.3V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Power Dissipation	300mW
Lead Temperature (soldering, 5s)	260°C

PIN ASSIGNMENTS (DIP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	9	+V_{CC}
2	CLOCK	10	BPO DC
3	+V_{DD}	11	I_{OUT}
4	DCOM	12	ACOM
5	–V_{DD}	13	ACOM
6	LE	14	SERV DC
7	NC	15	REF DC
8	NC	16	–V_{CC}

PIN ASSIGNMENTS (SOP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	11	+V_{CC}
2	CLOCK	12	BPO DC
3	NC	13	NC
4	+V_{DD}	14	I_{OUT}
5	DCOM	15	ACOM
6	–V_{DD}	16	ACOM
7	LE	17	SERV DC
8	NC	18	NC
9	NC	19	RFE DC
10	NC	20	–V_{CC}

PACKAGE INFORMATION[1]

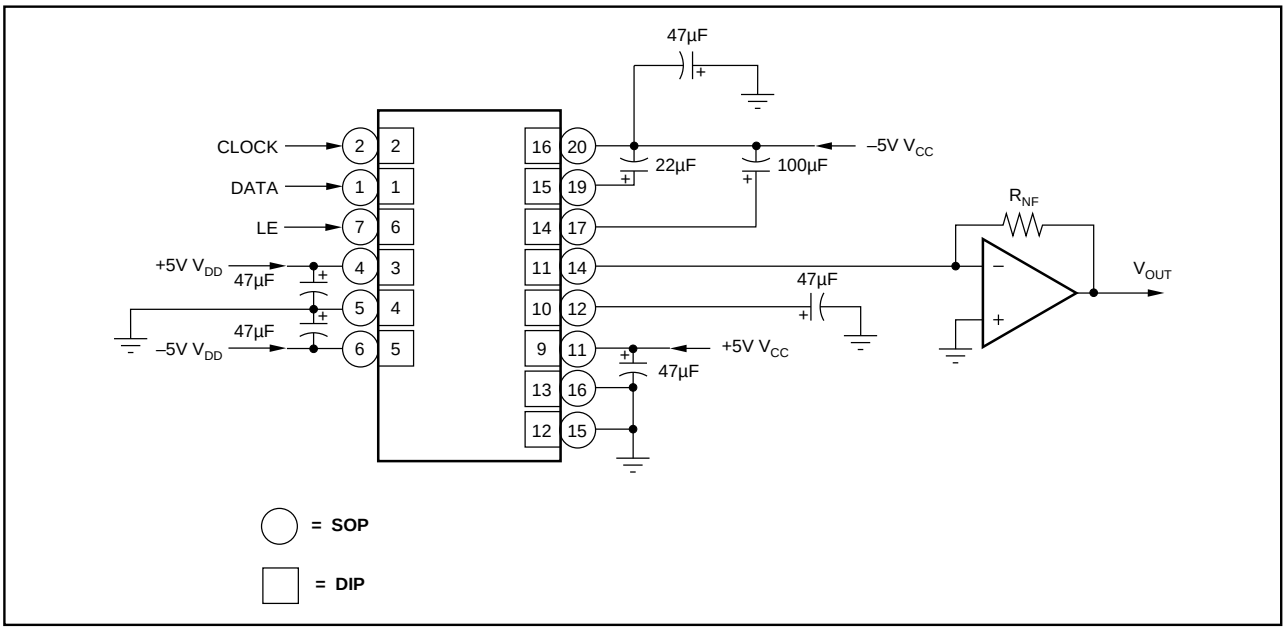
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1702P	16-Pin Plastic DIP	180
PCM1702U	20-Pin Plastic SOP	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

GRADE MARKING (SOP Package)

MODEL	PACKAGE
PCM1702U	Marked PCM1702.
PCM1702U-J	Marked with white dot by pin 10.
PCM1702U-K	Marked with red dot by pin 10.

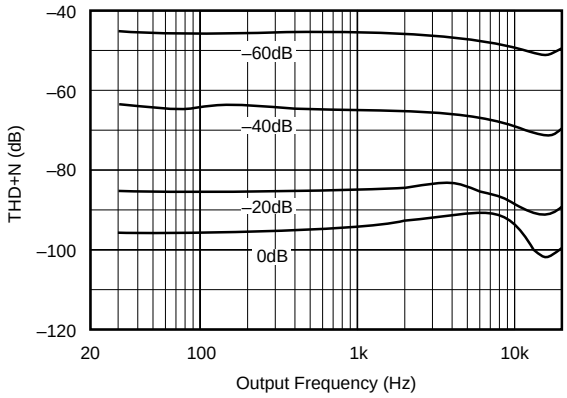
CONNECTION DIAGRAM



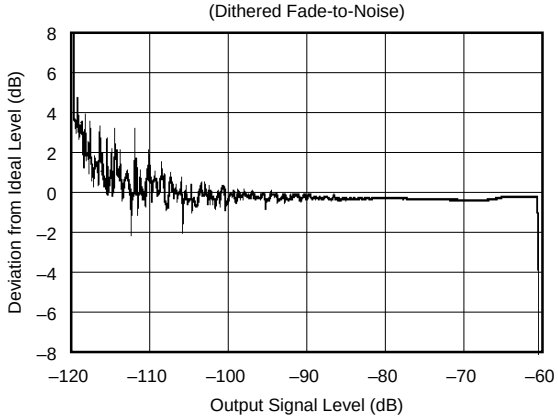
TYPICAL PERFORMANCE CURVES

All specifications at 25°C, $\pm V_A$ and $\pm V_D$ = ±5.0V unless otherwise noted.

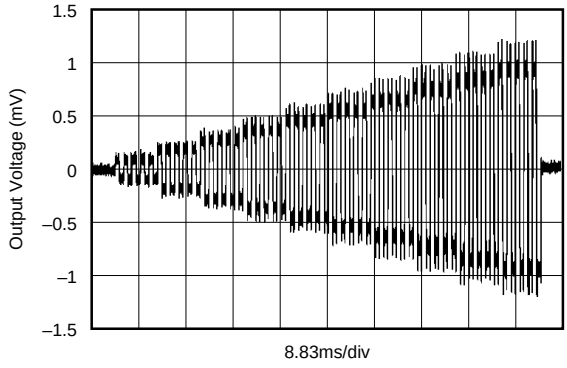
THD+N vs FREQUENCY



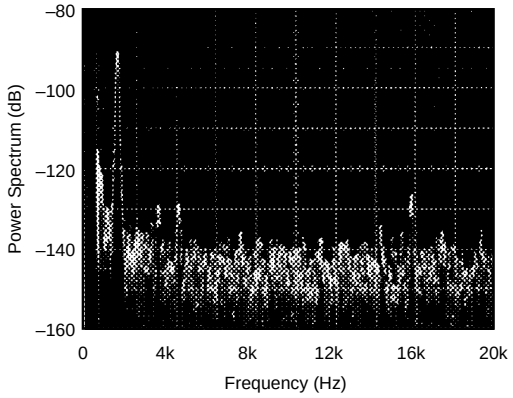
16-BIT LEVEL LINEARITY
(Dithered Fade-to-Noise)



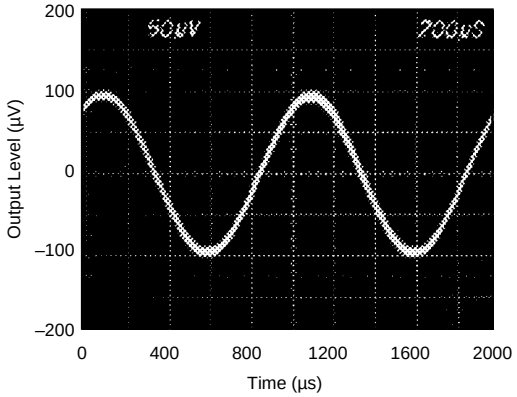
16-BIT MONOTONICITY



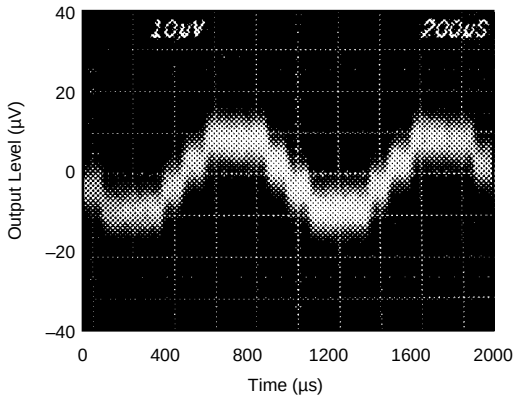
–90dB SIGNAL SPECTRUM
(100Hz Bandwidth)



–90dB SIGNAL
(10Hz to 20kHz Bandwidth)



–110dB SIGNAL
(10Hz to 20kHz Bandwidth)



THEORY OF OPERATION

ADVANCED SIGN MAGNITUDE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However, even the best of these suffer from potential low-level nonlinearity due to errors at the major carry bipolar zero transition. More recently, DACs employing a different architecture which utilizes noise shaping techniques and very high over-sampling frequencies, have been introduced ("Bitstream", "MASH", or 1-bit DAC). These DACs overcome the low level linearity problem, but only at the expense of signal-to-noise performance, and often to the detriment of channel separation and intermodulation distortion if the succeeding circuitry is not carefully designed.

The PCM1702 is a new solution to the problem. It combines all the advantages of a conventional DAC (excellent full scale performance, high signal-to-noise ratio and ease of use) with superior low-level performance. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference, and a common R-2R ladder for bit current sources by dual balanced current segments to ensure perfect tracking under all conditions. By interleaving the individual bits of each DAC and employing precise laser trimming of resistors, the highly accurate match required between DACs is achieved.

This new, complementary linear or advanced sign magnitude approach, which steps away from zero with small steps in both directions, avoids any glitching or "large" linearity errors and provides an absolute current output. The low level performance of the PCM1702 is such that real 20-bit resolution can be realized, especially around the critical bipolar zero point.

Table 1 shows the conversion made by the internal logic of the PCM1702 from binary two's complement (BTC). Also, the resulting internal codes to the upper and lower DACs (see front page block diagram) are listed. Notice that only the LSB portions of either internal DAC are changing around bipolar zero. This accounts for the superlative performance of the PCM1702 in this area of operation.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

The key specifications for the PCM1702 is total harmonic distortion plus noise (THD+N).

Digital data words are read into the PCM1702 at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 1002Hz is realized.

For production testing, the output of the DAC goes to an I to V converter, then through a 40kHz low pass filter, and then to a programmable gain amplifier to provide gain at lower signal output test levels before being fed into an analog-type distortion analyzer. Figure 1 shows a block diagram of the production THD+N test setup.

For the audio bandwidth, THD+N of the PCM1702 is essentially flat for all frequencies. The typical performance curve, "THD+N vs Frequency", shows four different output signal levels: 0dB, –20dB, –40dB, and –60dB. The test signals are derived from a special compact test disk (the CBS CD-1). It is interesting to note that the –20dB signal falls only about 10dB below the full scale signal instead of the expected 20dB. This is primarily due to the superior low level signal performance of the advanced sign magnitude architecture of the PCM1702.

In terms of signal measurement, THD+N is the ratio of $Distortion_{RMS} + Noise_{RMS} / Signal_{RMS}$ expressed in dB. For the PCM1702, THD+N is 100% tested at all three specified output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. All specifications are achieved without the use of external deglitchers.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD+N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The advanced sign magnitude architecture of the PCM1702, with its ideal performance around bipolar zero, provides a more usable dynamic range, even using the strict audio definition, than any previously available D/A converter.

ANALOG OUTPUT	INPUT CODE (20-bit Binary Two's Complement)	LOWER DAC CODE (19-bit Straight Binary)	UPPER DAC CODE (19-bit Straight Binary)
+Full Scale	011...111	111...111+1LSB(1)	111...111
+Full Scale –1LSB	011...110	111...111+1LSB(1)	111...110
Bipolar Zero +2LSB	000...010	111...111+1LSB(1)	000...010
Bipolar Zero +1LSB	000...001	111...111+1LSB(1)	000...001
Bipolar Zero	000...000	111...111+1LSB(1)	000...000
Bipolar Zero –1LSB	111...111	111...111	000...000
Bipolar Zero –2LSB	111...110	111...110	000...000
–Full Scale +LSB	100...001	000...001	000...000
–Full Scale	100...000	000...000	000...000

NOTE: (1) The extra weight of 1LSB is added at this point to make the transfer function symmetrical around bipolar zero.

TABLE I. Binary Two's Complement to Sign Magnitude Conversion Chart.

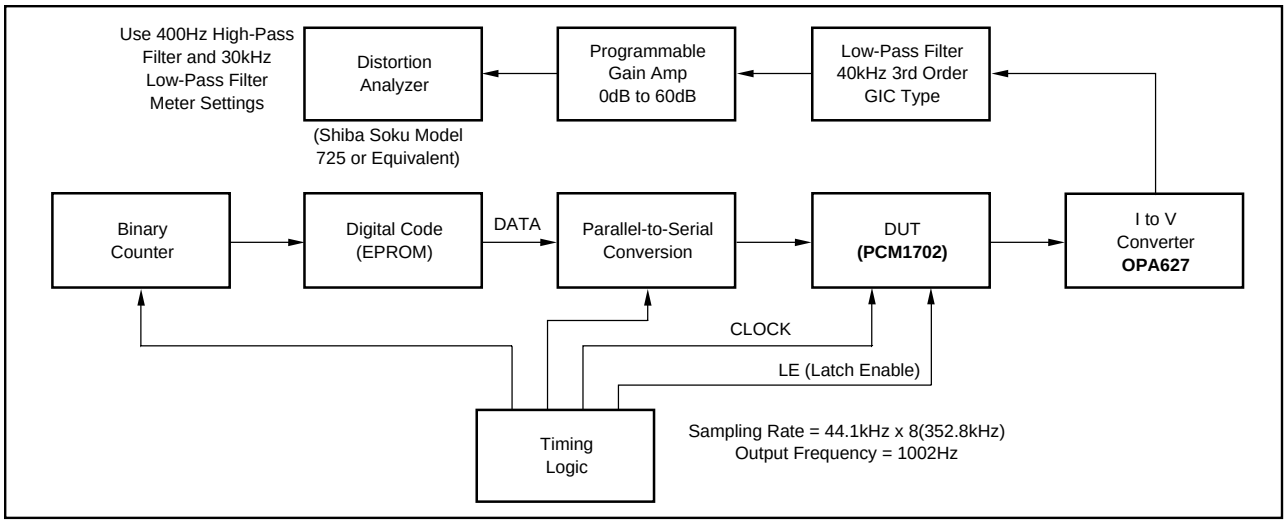


FIGURE 1. Production THD+N Test Setup.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. See the "–90dB Signal Spectrum" plot in the Typical Performance Curves section for the power spectrum of a PCM1702 at a –90dB output level. (The "–90dB Signal" plot shows the actual –90dB output of the DAC). The deviation from ideal for PCM1702 at this signal level is typically less than ±0.3dB. For the "–110dB Signal" plot in the Typical Performance Curves section, true 20-bit digital code is used to generate a –110dB output signal.

This type of performance is possible only with the low-noise, near-theoretical performance around bipolar zero of the PCM1702 advanced sign magnitude.

A commonly tested digital audio parameter is the amount of deviation from ideal of a 1kHz signal when its amplitude is decreased form –60dB to –120dB. A digitally dithered input signal is applied to reach effective output levels of –120dB using only the available 16-bit code from a special compact disk test input. See the "16-bit Level Linearity" plot in the Typical Performance Curves section for the results of a PCM1702 tested using this 16-bit dithered fade-to-noise signal. Note the very small deviation from ideal as the signal goes from –60dB to –100dB.

DC SPECIFICATION

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero, while the output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied. The idle channel SNR for the PCM1702 is typically greater than 120dB, making it ideal for low-noise applications.

Monotonicity

Because of the unique advanced sign magnitude architecture of the PCM1702, increasing values of digital input will always result in increasing values of DAC output as the signal moves away from bipolar zero in one-LSB steps (in either direction). The "16-bit Monotonicity" plot in the Typical Performance Curves section was generated using 16-bit digital code from a test compact disk. The test starts with 10 periods of bipolar zero. Next are 10 periods of alternating 1LSBs above and below zero, and then 10 periods of alternating 2LSBs above and below zero, and so on until 10LSBs above and below zero are reached. The signal pattern then begins again at bipolar zero.

With PCM1702, the low-noise steps are clearly defined and increase in near-perfect proportion. This performance is achieved without any external adjustments. By contrast, sigma-delta ("Bit-stream", "MASH", or 1-bit DAC) architectures are too noisy to even see the first 3 or 4 bits change (at 16 bits), other than by a change in the noise level.

Absolute Linearity

Even though absolute integral and differential linearity specs are not given for the PCM1702, the extremely low THD+N performance is typically indicative of 17-bit integral linearity in the DAC. The relationship between THD+N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

Offset, Gain, and Temperature Drift

Although the PCM1702 is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain and offset drift.

DIGITAL INPUT

Timing Considerations

The PCM1702 accepts TTL compatible logic input levels. The data format of the PCM1702 is binary two's complement (BTC) with the most significant bit (MSB) being first

in the serial input bit stream. Table II describes the exact relationship of input data to voltage output coding. Any number of bits can precede the 20 bits to be loaded, since only the last 20 will be transferred to the parallel DAC register after Latch Enable (Pin6 <PCM1702P>, Pin7 <PCM1702U>, LE) has gone low.

All DAC serial input data (Pin1, DATA) bit transfers are triggered on positive clock (Pin2, CLOCK), edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Latch Enable. The change in the output of the DAC occurs at a rising edge of the 4th clock of the CLOCK after the falling edge of Latch Enable. Refer to Figure 2 for graphical relationships of these signals.

Maximum Clock Rate

A typical clock rate of 16.9MHz for the PCM1702 is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16X over-sampling) the standard audio word bit length of 24 bits (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 20 bits are actually being used. The setup and hold timing relationships are shown in Figure 3.

"Stopped Clock" Operation

The PCM1702 is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 20 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until Latch Enable goes low. Latch Enable must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In any case, the setup and hold times for Data and LE must be observed as shown in Figure 3.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT
1,048,576LSBs	Full Scale Range	2.40000000mA
1LSB	NA	2.28882054nA
$7FFFF_{HEX}$	+Full Scale	–1.19999771mA
00000_{HEX}	Bipolar Zero –1LSB	0.00000000mA
80000_{HEX}	–Full Scale	+1.20000000mA

TABLE II. Digital Input/Output Relationships.

INSTALLATION

POWER SUPPLIES

Refer to CONNECTION DIAGRAM for proper connection of the PCM1702. The PCM1702 only requires a ±5V supply. Both positive supplies should be tied together at a single point. Similarly, both negative supplies should be connected together. No real advantage is gained by using separate analog and digital supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in CONNECTION DIAGRAM regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM1702 as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in CONNECTION DIAGRAM, various size decoupling capacitors can be used, with no special tolerances being required. The size of the offset decoupling capacitor is not critical either, with larger values (up to 100µF) giving slightly better SNR readings. All capacitors should be as close to the appropriate pins of the PCM1702 as possible to reduce noise pickup from surrounding circuitry.

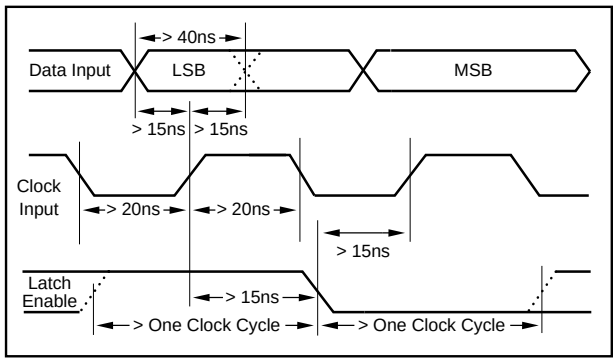
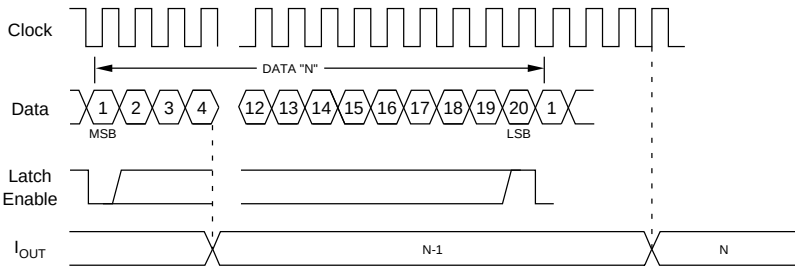


FIGURE 3. Setup and Hold Timing Diagram.



NOTES : (1) If clock is stopped between input of 20-bit data words, "Latch" Enable (LE) must remain low until after the first clock cycle of the next 20-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch Enable (LE) must remain low at least one clock cycle after going negative. (4) Latch Enable (LE) must be high for at least one clock cycle before going negative. (5) I_{OUT} changes on positive going edge of the 4th clock after negative going edge of Latch Enable (LE).

FIGURE 2. Timing Diagram.

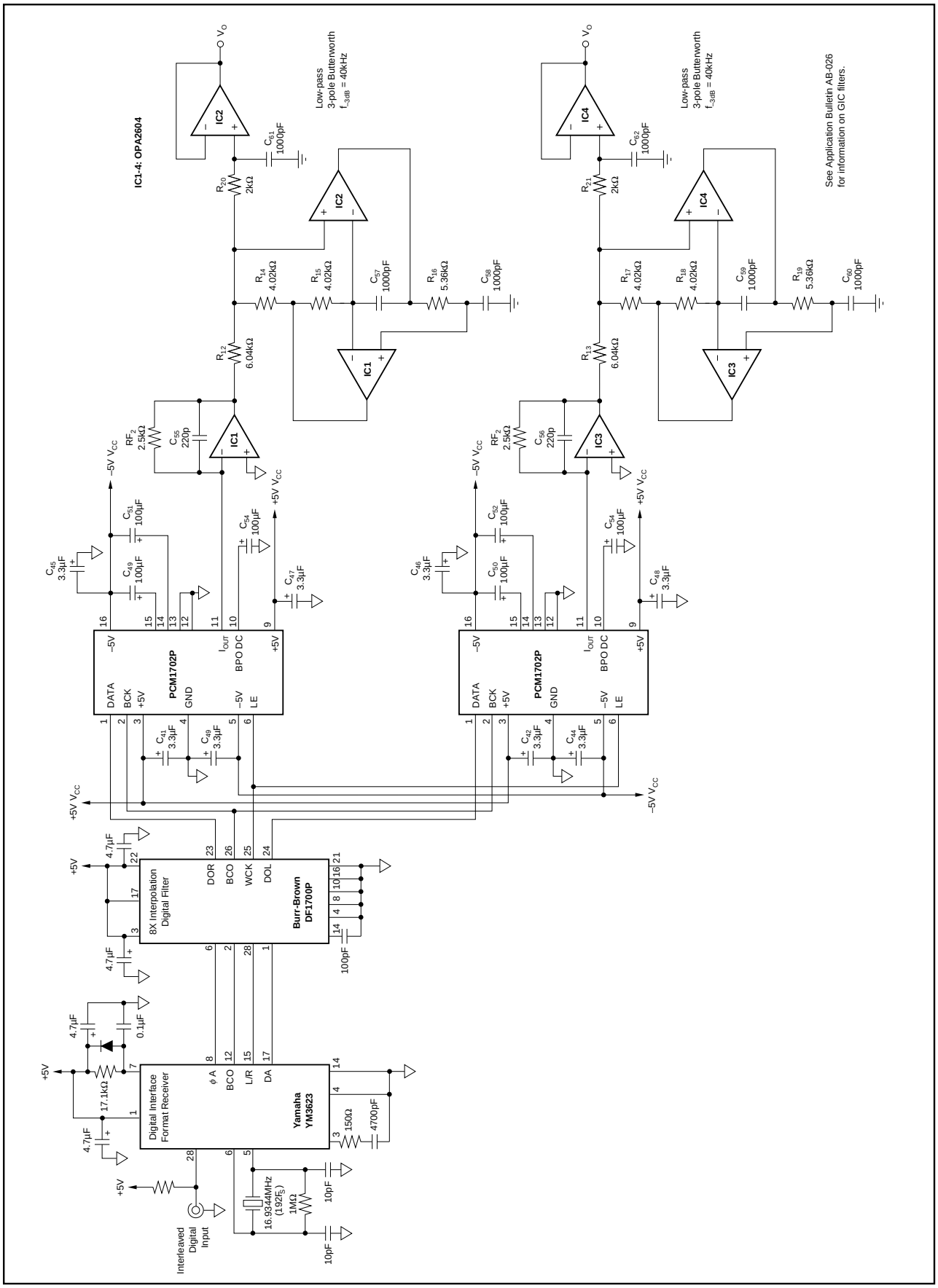


FIGURE 4. Typical Application for Stereo Audio 8X Oversampling system.

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