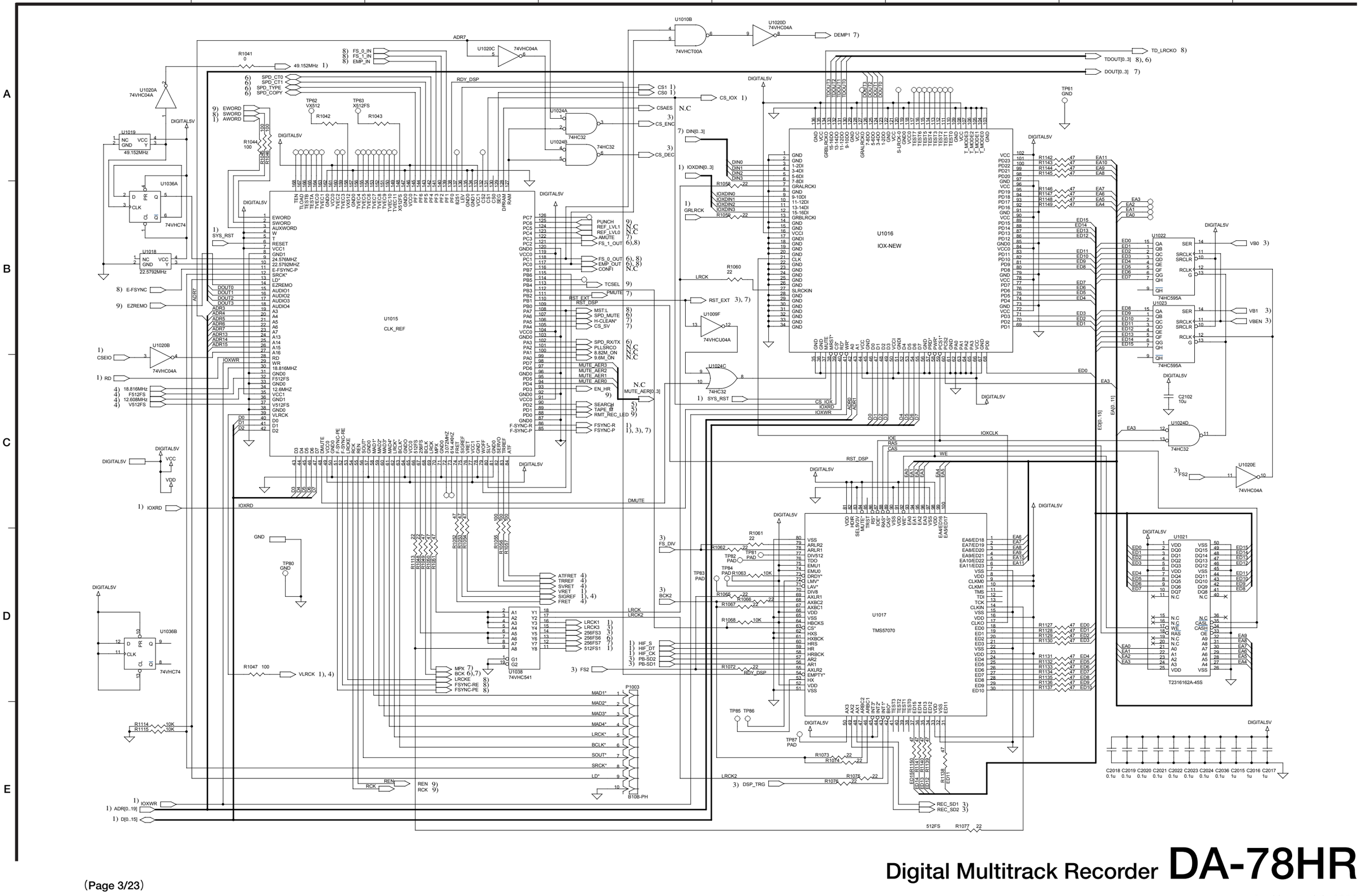
SCHEMATIC DIAGRAM DA-78HR HR-MAIN PCB (2/14)



Digital Multitrack Recorder **DA-78HR**

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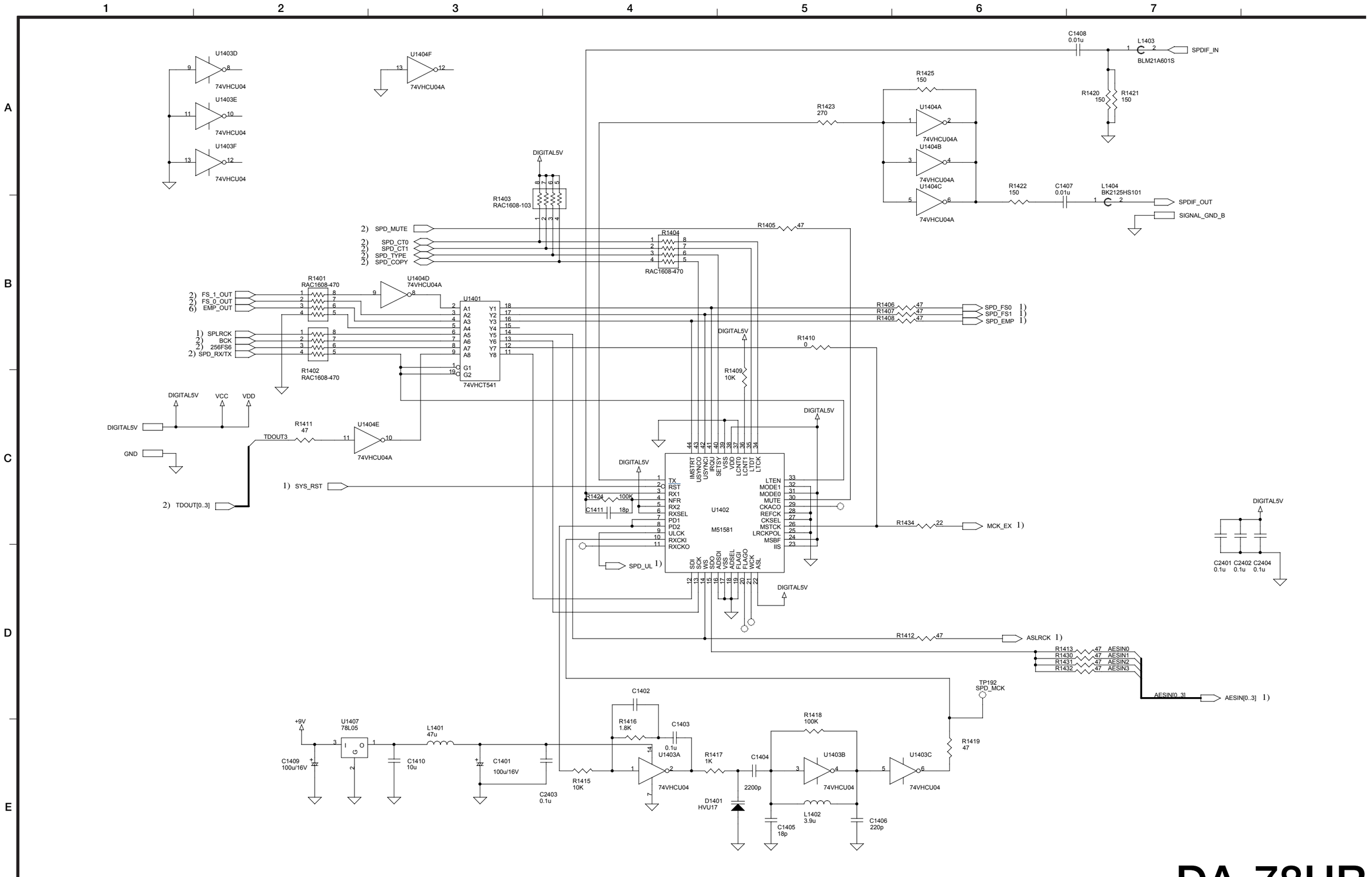
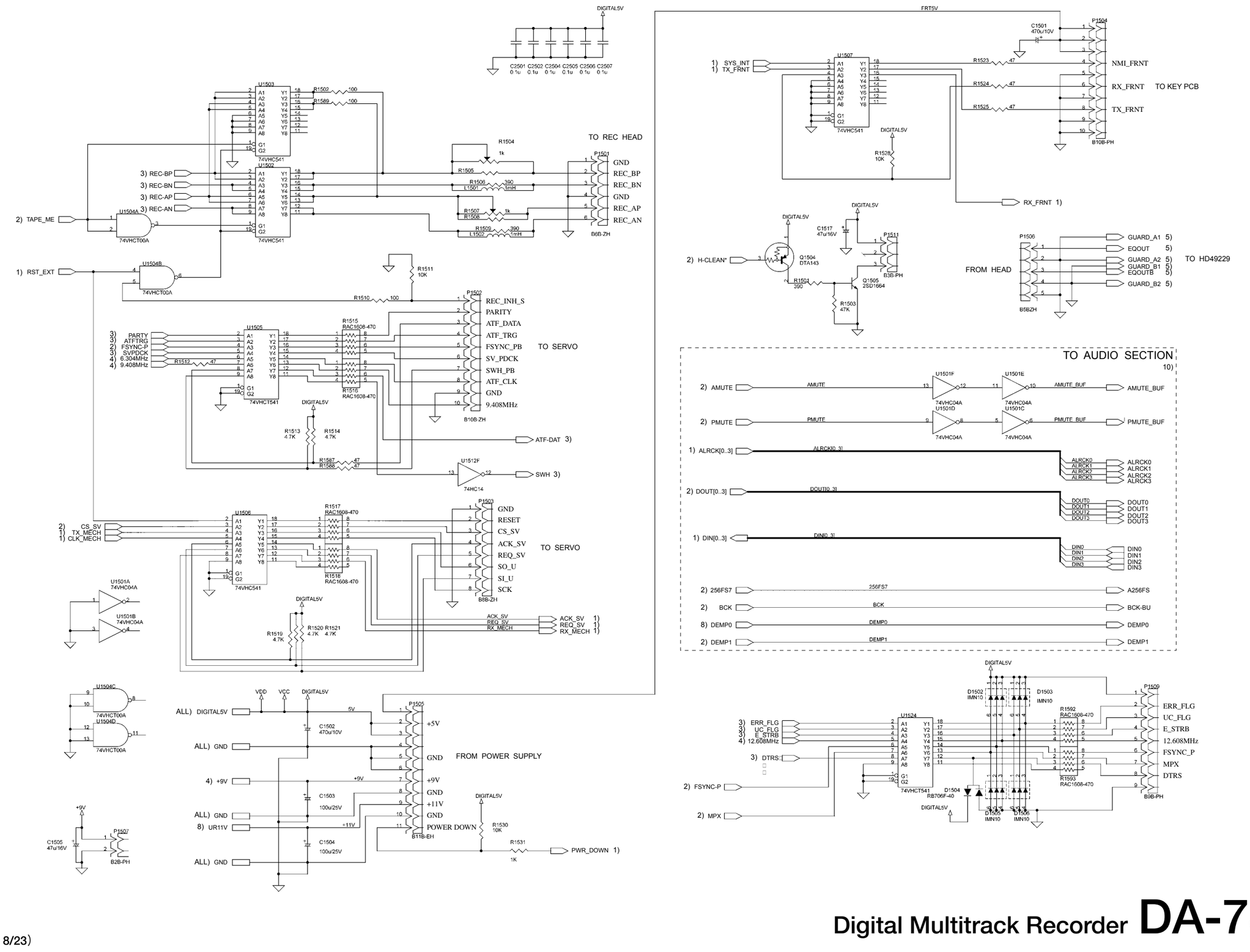

1
2
3
4
5
6
7
A
B
C
D
E
U1403D
74VHCU04
U1403E
74VHCU04
U1403F
74VHCU04
U1404F
74VHCU04A
C1408
0.01u
L1403
BLM21A601S
SPDIF_IN
R1425
150
R1420
150
R1421
150
R1423
270
U1404A
74VHCU04A
U1404B
74VHCU04A
U1404C
74VHCU04A
R1422
150
C1407
0.01u
L1404
BK2125HS101
SPDIF_OUT
SIGNAL_GND_B
DIGITAL5V
R1403
RAC1608-103
2) SPD_MUTE
2) SPD_CT0
2) SPD_CT1
2) SPD_TYPE
2) SPD_COPY
R1404
RAC1608-470
R1405
47
R1401
RAC1608-470
U1404D
74VHCU04A
2) FS_1_OUT
2) FS_0_OUT
6) EMP_OUT
1) SPLRCK
2) BCK
2) 256FS6
2) SPD_RX/TX
R1402
RAC1608-470
U1401
74VHCT541
R1406
R1407
R1408
47
SPD_FS0 1)
SPD_FS1 1)
SPD_EMP 1)
R1410
0
R1409
10K
DIGITAL5V
VCC
VDD
GND
TDOUT3
R1411
47
U1404E
74VHCU04A
2) TDOUT[0..3]
1) SYS_RST
U1402
M51581
R1424
100K
C1411
18p
SPD_UL 1)
R1434
22
MCK_EX 1)
C2401
0.1u
C2402
0.1u
C2404
0.1u
R1412
47
ASLRCK 1)
R1413
R1430
R1431
R1432
AESIN0
AESIN1
AESIN2
AESIN3
AESIN[0..3]
TP192
SPD_MCK
C1402
R1416
1.8K
C1403
0.1u
U1403A
R1418
100K
R1419
47
+9V
U1407
78L05
L1401
47u
C1409
100u/16V
C1410
10u
C1401
100u/16V
C2403
0.1u
R1415
10K
R1417
1K
C1404
2200p
U1403B
U1403C
74VHCU04
D1401
HVU17
L1402
3.9u
C1405
18p
C1406
220p



Digital Multitrack Recorder DA-78HR

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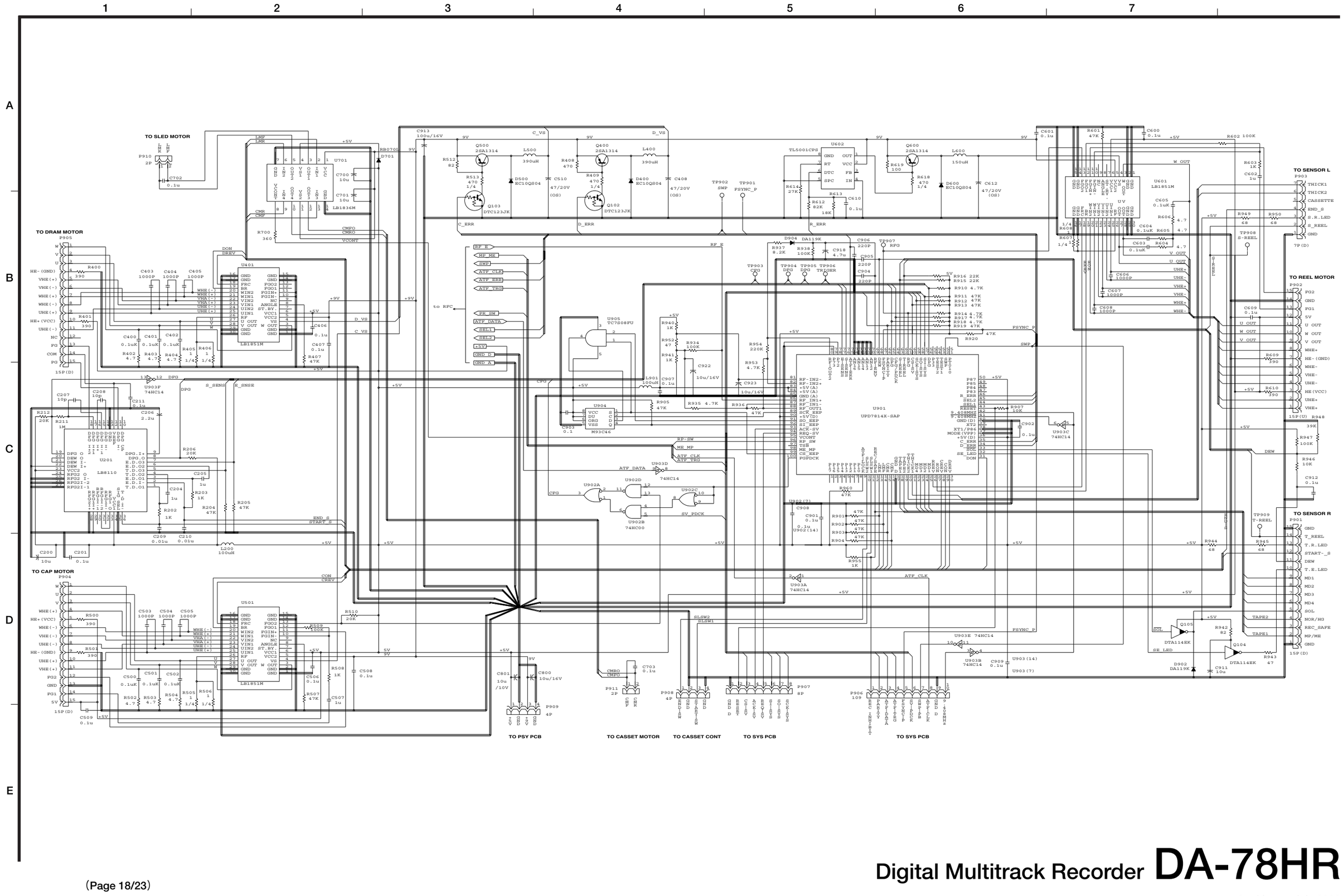
SCHEMATIC DIAGRAM DA-78HR SERVO PCB (1/2)



Digital Multitrack Recorder DA-78HR
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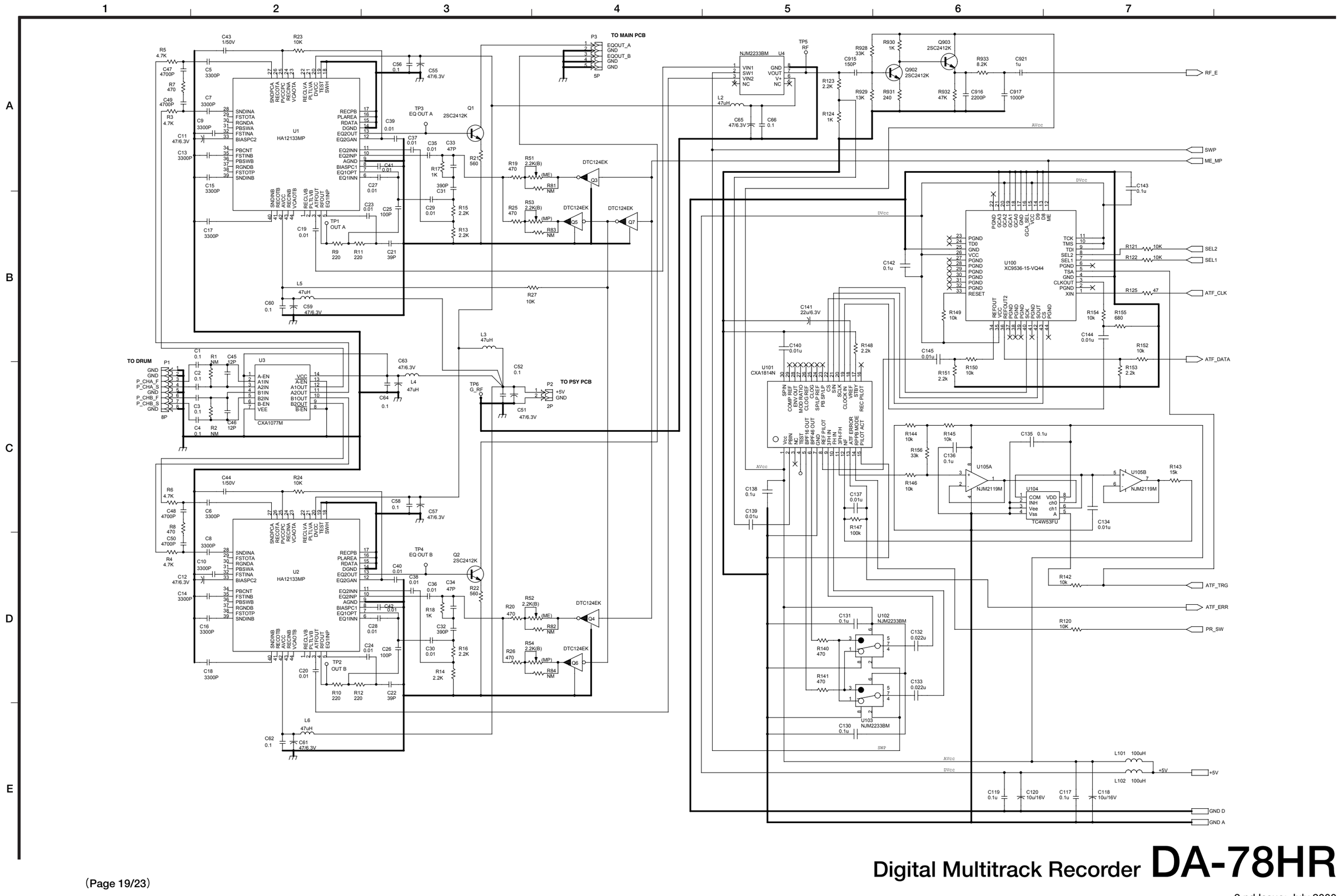
SCHEMATIC DIAGRAM DA-78HR SERVO PCB (2/2)



Digital Multitrack Recorder **DA-78HR**

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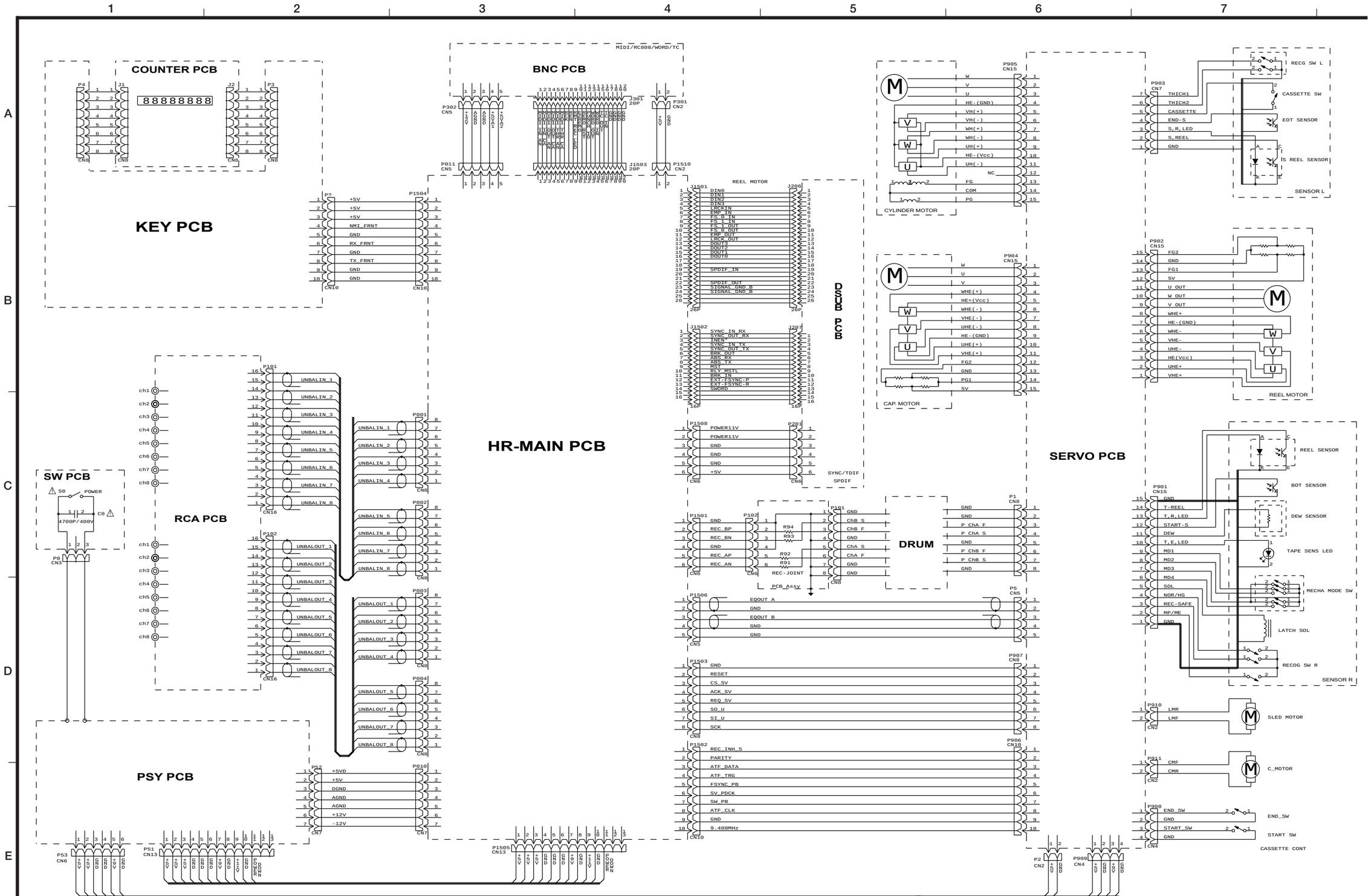
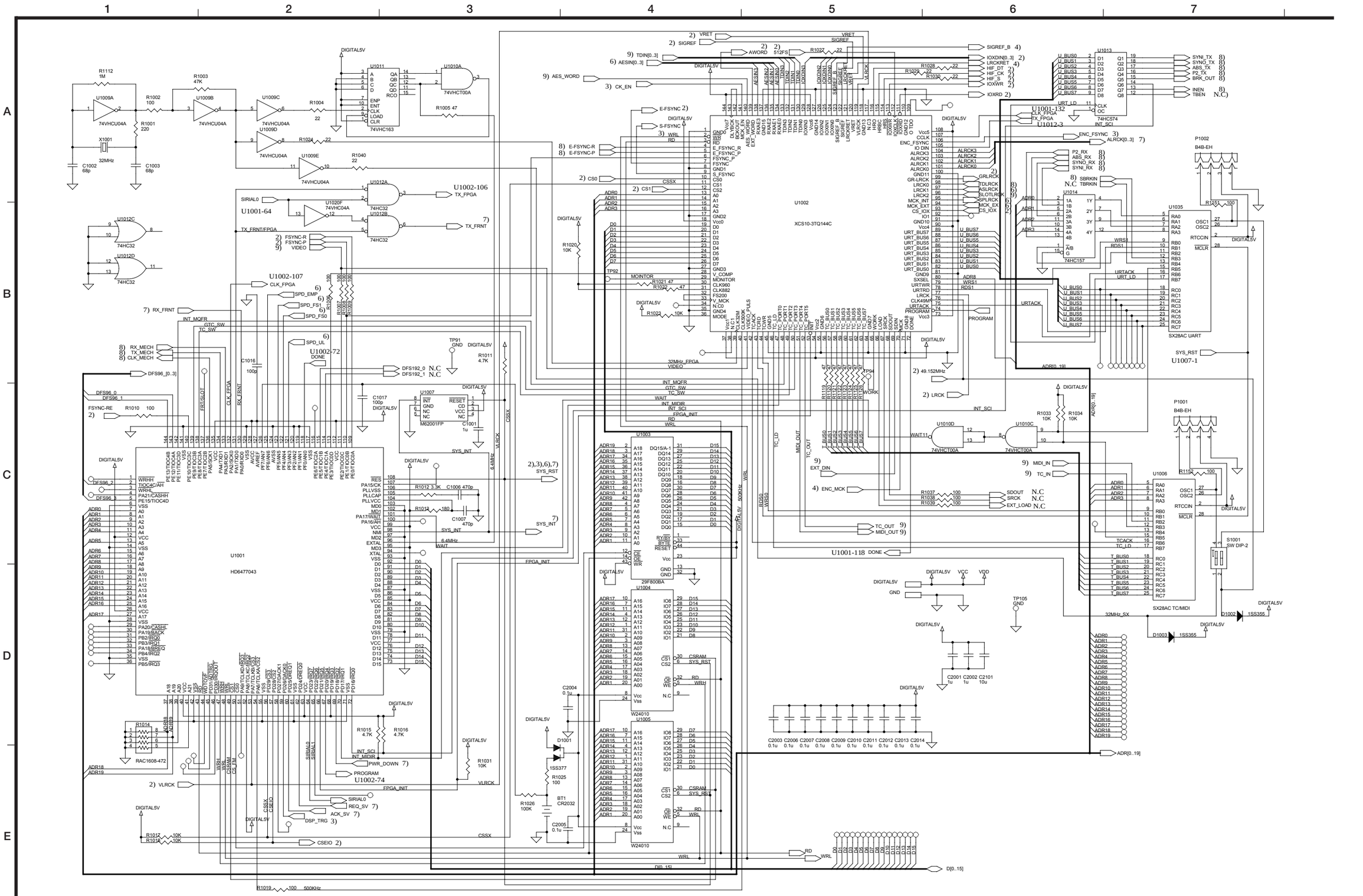
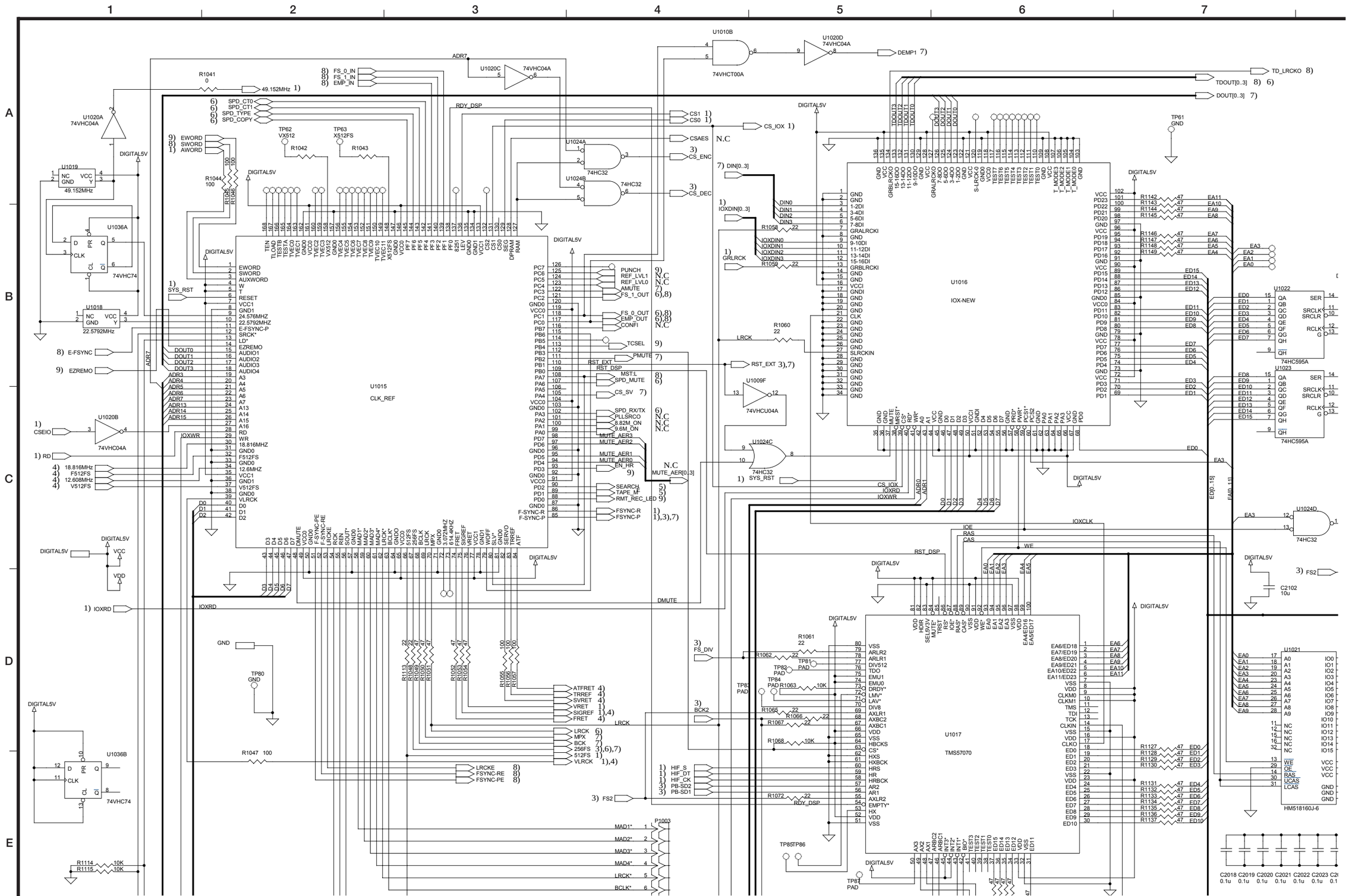

COUNTER PCB
88888888
KEY PCB
BNC PCB
MIDI/RC808/WORD/TC
HR-MAIN PCB
REEL MOTOR
D/SUB PCB
SYNC/TDIF
SPDIF
SW PCB
POWER
4700P/400V
RCA PCB
PSY PCB
DRUM
REC-JOINT
PCB_Assy
CYLINDER MOTOR
CAP. MOTOR
SERVO PCB
RECG SW L
CASSETTE SW
EOT SENSOR
IS REEL SENSOR
SENSOR L
REEL MOTOR
REEL SENSOR
BOT SENSOR
DEW SENSOR
TAPE SENS LED
MECHA MODE SW
LATCH SOL
RECOG SW R
SENSOR R
SLED MOTOR
C_MOTOR
END_SW
START SW
CASSETTE CONT

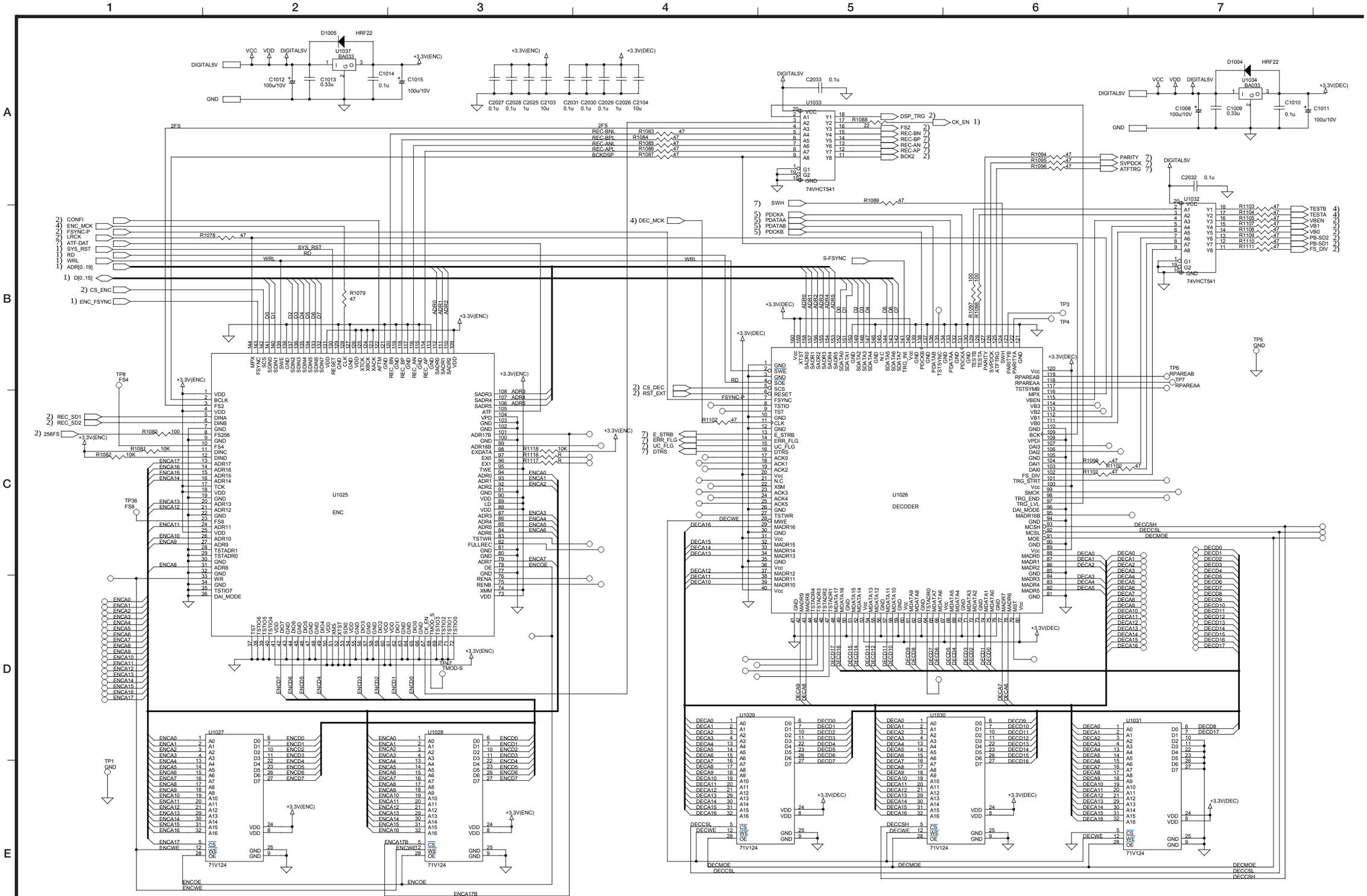
SCHEMATIC DIAGRAM DA-78HR HR-MAIN PCB (1/14)



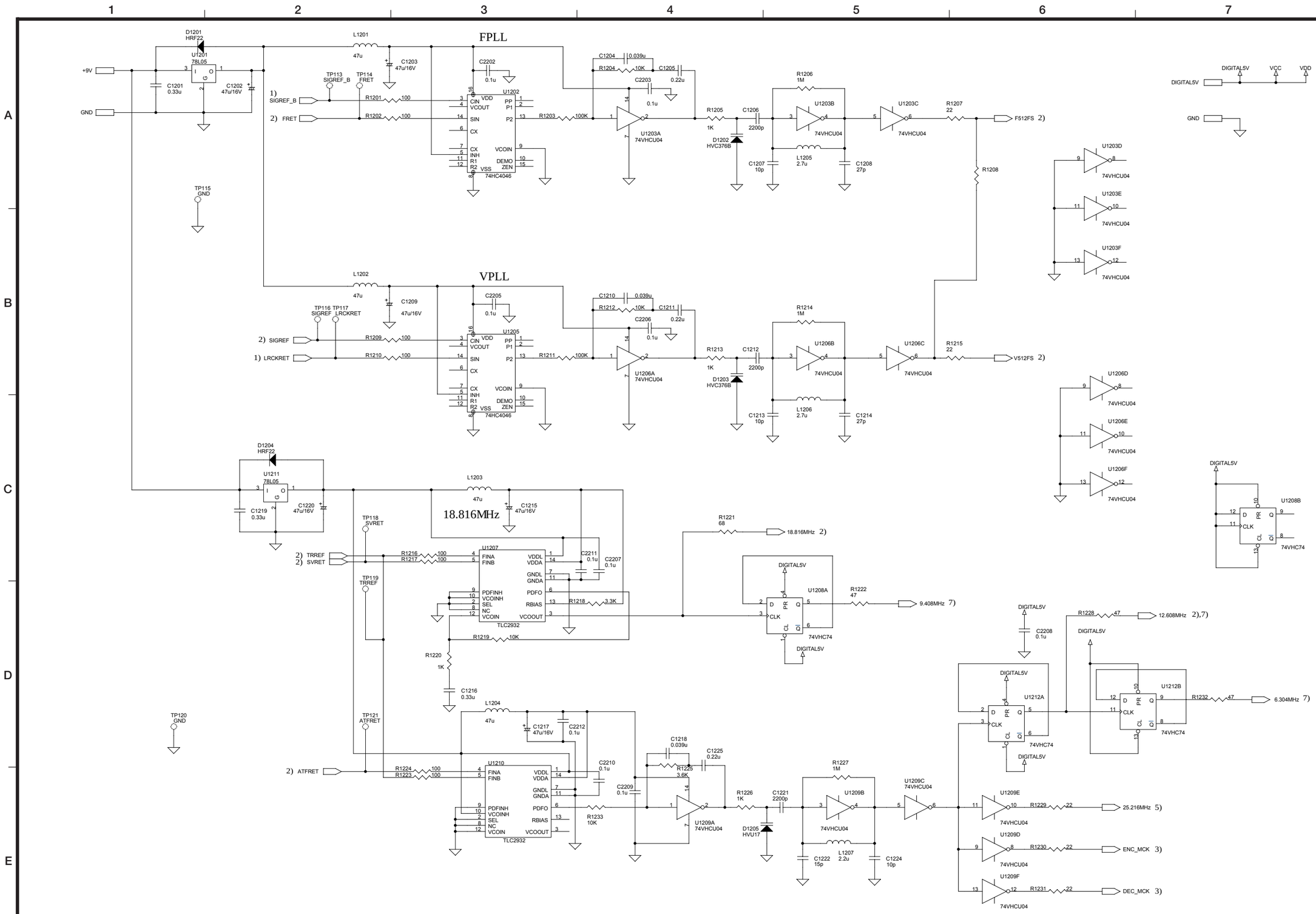
Digital Multitrack Recorder **DA-78HR**


1
2
3
4
5
6
7
A
B
C
D
E
U1010B
74VHCT00A
U1020D
74VHC04A
DEMP1 7)
TD_LRCKO 8)
TDOUT[0..3] 8) 6)
DOUT[0..3] 7)
U1020C
74VHC04A
ADR7
8) FS_0_IN
8) FS_1_IN
8) EMP_IN
R1041
0
49.152MHz 1)
U1020A
74VHC04A
DIGITAL5V
6) SPD_CT0
6) SPD_CT1
6) SPD_TYPE
6) SPD_COPY
RDY_DSP
CS1 1)
CS0 1)
CS_IOX 1)
N.C
CSAES
3) CS_ENC
3) CS_DEC
U1024A
74HC32
U1024B
74HC32
9) EWORD
8) SWORD
1) AWORD
TP62
VX512
TP63
X512FS
R1042
R1043
R1044
100
R1045
100
R1046
100
U1019
49.152MHz
U1036A
74VHC74
U1018
22.5792MHz
8) E-FSYNC
9) EZREMO
1) SYS_RST
U1015
CLK_REF
DOUT0
DOUT1
DOUT2
DOUT3
AUDIO1
AUDIO2
AUDIO3
AUDIO4
ADR3
ADR4
ADR5
ADR6
ADR7
ADR13
ADR14
ADR15
A3
A4
A5
A6
A7
A13
A14
A15
A16
1) CSEIO
1) RD
IOXWR
RD
WR
18.816MHZ
GND0
F512FS
GND0
12.6MHZ
VCC1
GND1
V512FS
GND0
VLRCK
D0
D1
D2
4) 18.816MHz
4) F512FS
4) 12.608MHz
4) V512FS
U1020B
74VHC04A
DIGITAL5V
VCC
VDD
1) IOXRD
IOXRD
DMUTE
GND
TP80
GND
U1036B
74VHC74
R1047 100
R1114 10K
R1115 10K
TEN
TLOAD
TSTB
TEST1A
TEST0
TVEC0
TVEC1
GND0
VCC0
TVEC2
TVEC3
VCC2
GND0
TVEC4
TVEC5
TVEC6
TVEC7
TVEC8
TVEC9
TVEC10
TVEC11
X512FS
GND0
VCC0
PF7
PF6
PF5
PF4
PF3
PF2
PF1
PF0
8251
GND0
GND1
VCC1
CS2
CS0
SEG
DRAM
RAM
PC7
PC6
PC5
PC4
PC3
PC2
GND0
VCC0
PC1
PC0
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
PA7
PA6
PA5
PA4
VCC0
GND0
PA3
PA2
PA1
PA0
PD7
PD6
GND0
PD5
PD4
PD3
GND0
VCC0
PD2
PD1
PD0
GND0
F-SYNC-R
F-SYNC-P
PUNCH
REF_LVL1
REF_LVL0
AMUTE
FS_1_OUT
FS_0_OUT
EMP_OUT
CONFI
TCSEL
PMUTE
RST_EXT
RST_DSP
MST:L
SPD_MUTE
CS_SV 7)
SPD_RX/TX
PLLSRCO
8.62M_ON
9.6M_ON
MUTE_AER3
MUTE_AER2
MUTE_AER1
MUTE_AER0
EN_HR
MUTE_AER[0..3]
SEARCH
TAPE_MF
RMT_REC_LED
FSYNC-R
FSYNC-P
D3
D4
D5
D6
D7
DMUTE
VCC0
GND0
F-SYNC-PE
F-SYNC-RE
LRCKE
RCK
REN
SOUT*
GND0
MAD1*
MAD2*
MAD3*
MAD4*
LRCK*
BCLK*
GND0
VCC0
512FS
256FS
BCLK
LRCK
MPX
GND0
22.5792MHZ
614.4KHZ
FRET
SIGREF
SIGREF
VCC1
GND1
VOFF
SLICE
GND0
SERVO
VREF
ATF
ATFRET 4)
TRREF 4)
SVRET 4)
VRET 1)
SIGREF 1),4)
FRET 4)
LRCK 6)
MPX 7)
BCK 7),6),7)
512FS 1)
VLRCK 1),4)
LRCKE 8)
FSYNC-RE 8)
FSYNC-PE 8)
HIF_S
HIF_DT
HIF_CK
PB-SD2
PB-SD1
3) FS2
P1003
MAD1*
MAD2*
MAD3*
MAD4*
LRCK*
BCLK*
R1113 22
R1048 47
R1049 47
R1050 47
R1051 47
R1052 47
R1053 47
R1054 47
R1055 100
R1056 100
R1057 100
U1016
IOX-NEW
TP61
GND
7) DIN[0..3]
1) IOXDIN[0..3]
1) GRLRCK
R1058 22
R1060 22
LRCK
RST_EXT 3),7)
U1009F
74VHCU04A
U1024C
74HC32
1) SYS_RST
CS_IOX
IOXRD
IOXWR
ADR0
ADR1
IOXCLK
IOE
RAS
CAS
WE
RST_DSP
U1017
TMS57070
3) FS_DIV
3) BCK2
R1061 22
R1062 22
R1063 10K
R1065 22
R1066 22
R1067 22
R1068 10K
R1072 22
RDY_DSP
TP82 PAD
TP84 PAD
TP85 PAD
TP86
TP87 PAD
TP85TP86
R1142 47 EA11
R1143 47 EA10
R1144 47 EA9
R1145 47 EA8
R1146 47 EA7
R1147 47 EA6
R1148 47 EA5
R1149 47 EA4
EA3
EA2
EA1
EA0
ED15
ED14
ED13
ED12
ED11
ED10
ED9
ED8
ED7
ED6
ED5
ED4
ED3
ED2
ED1
ED0
ED[0..15]
EA[0..11]
U1022
U1023
74HC595A
U1024D
74HC32
3) FS2
C2102
10u
U1021
HM518160J-6
R1127 47 ED0
R1128 47 ED1
R1129 47 ED2
R1130 47 ED3
R1131 47 ED4
R1132 47 ED5
R1133 47 ED6
R1134 47 ED7
R1135 47 ED8
R1136 47 ED9
R1137 47 ED10
C2018 0.1u
C2019 0.1u
C2020 0.1u
C2021 0.1u
C2022 0.1u
C2023 0.1u

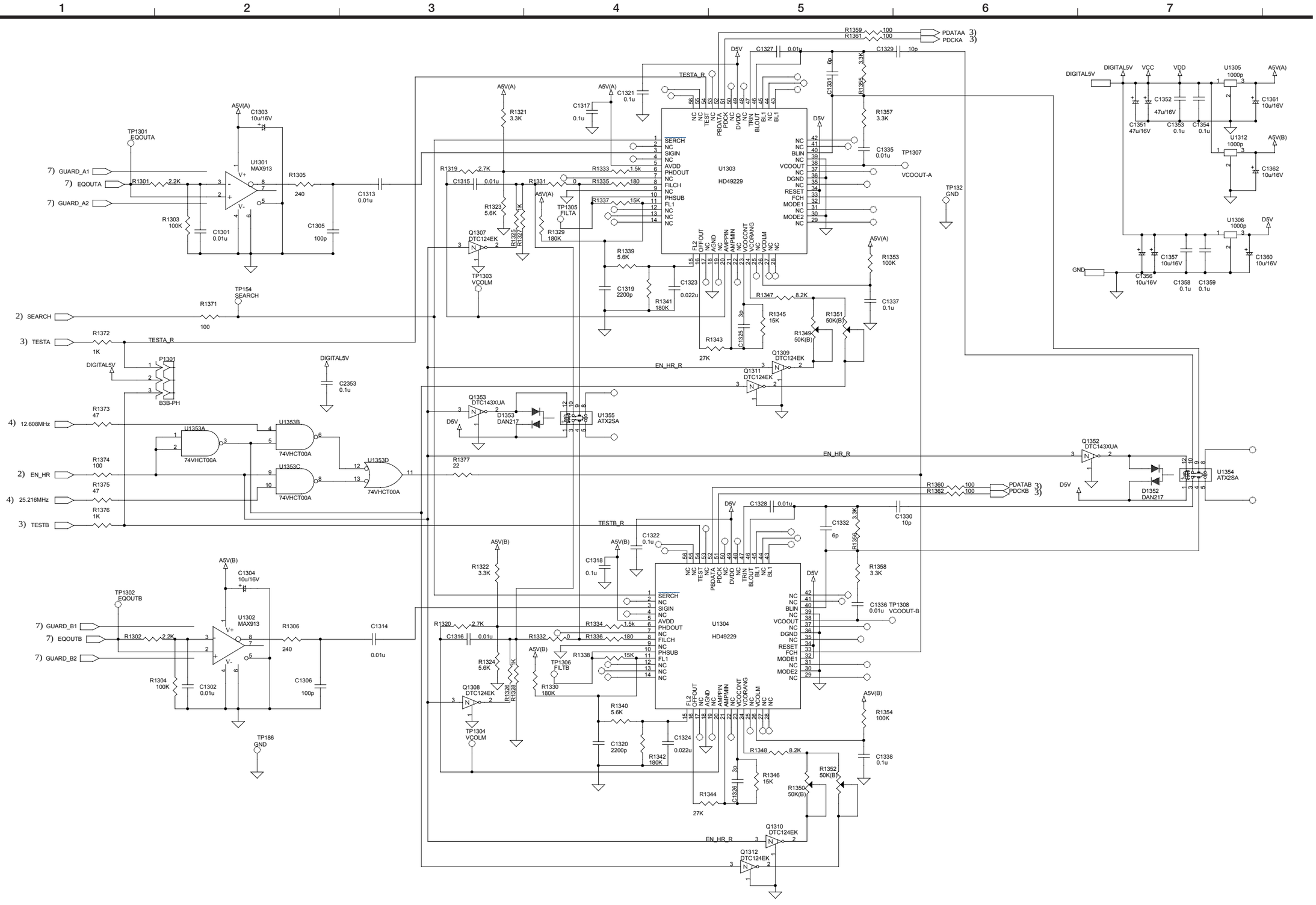
SCHEMATIC DIAGRAM DA-78HR HR-MAIN PCB (3/14)

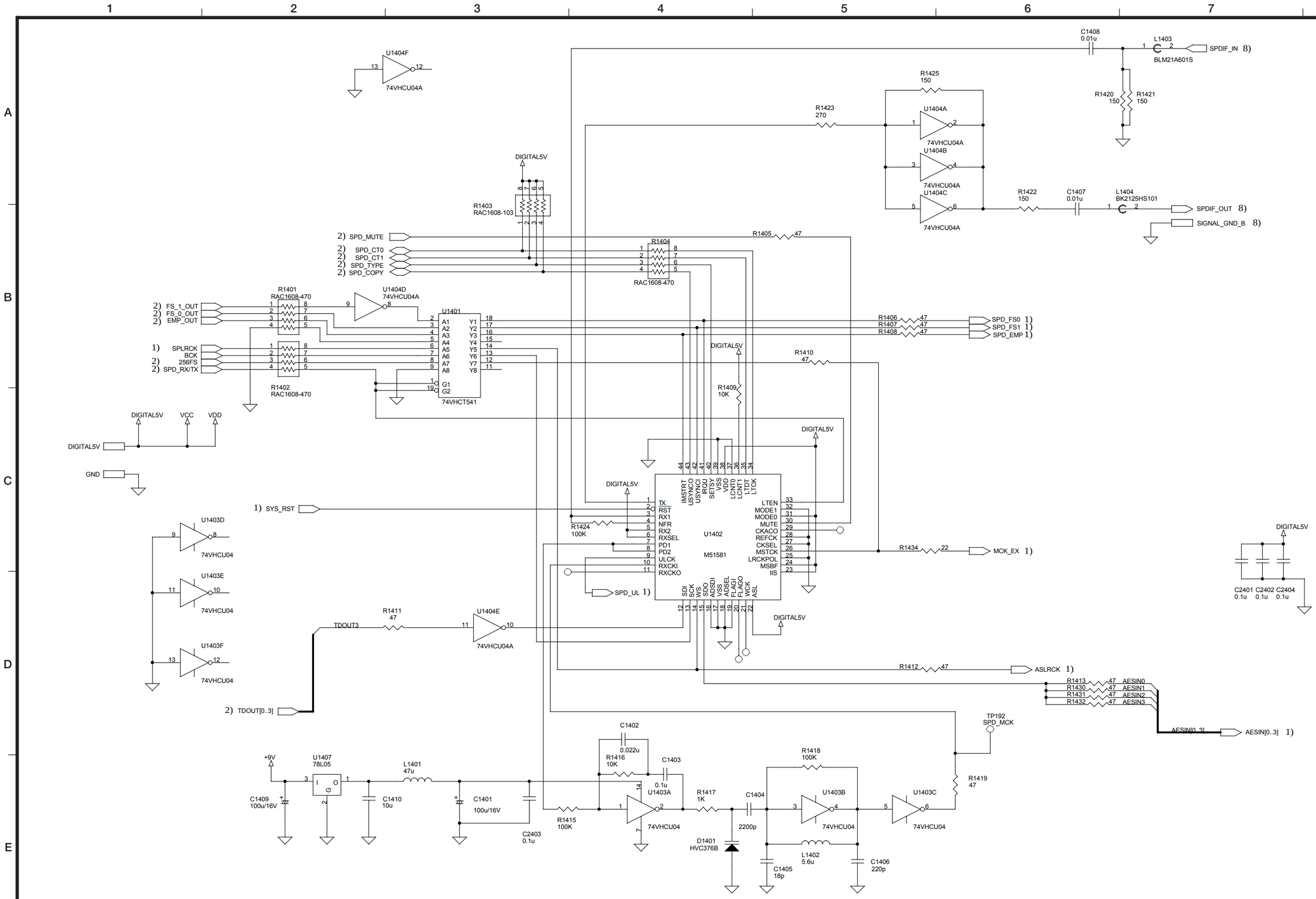


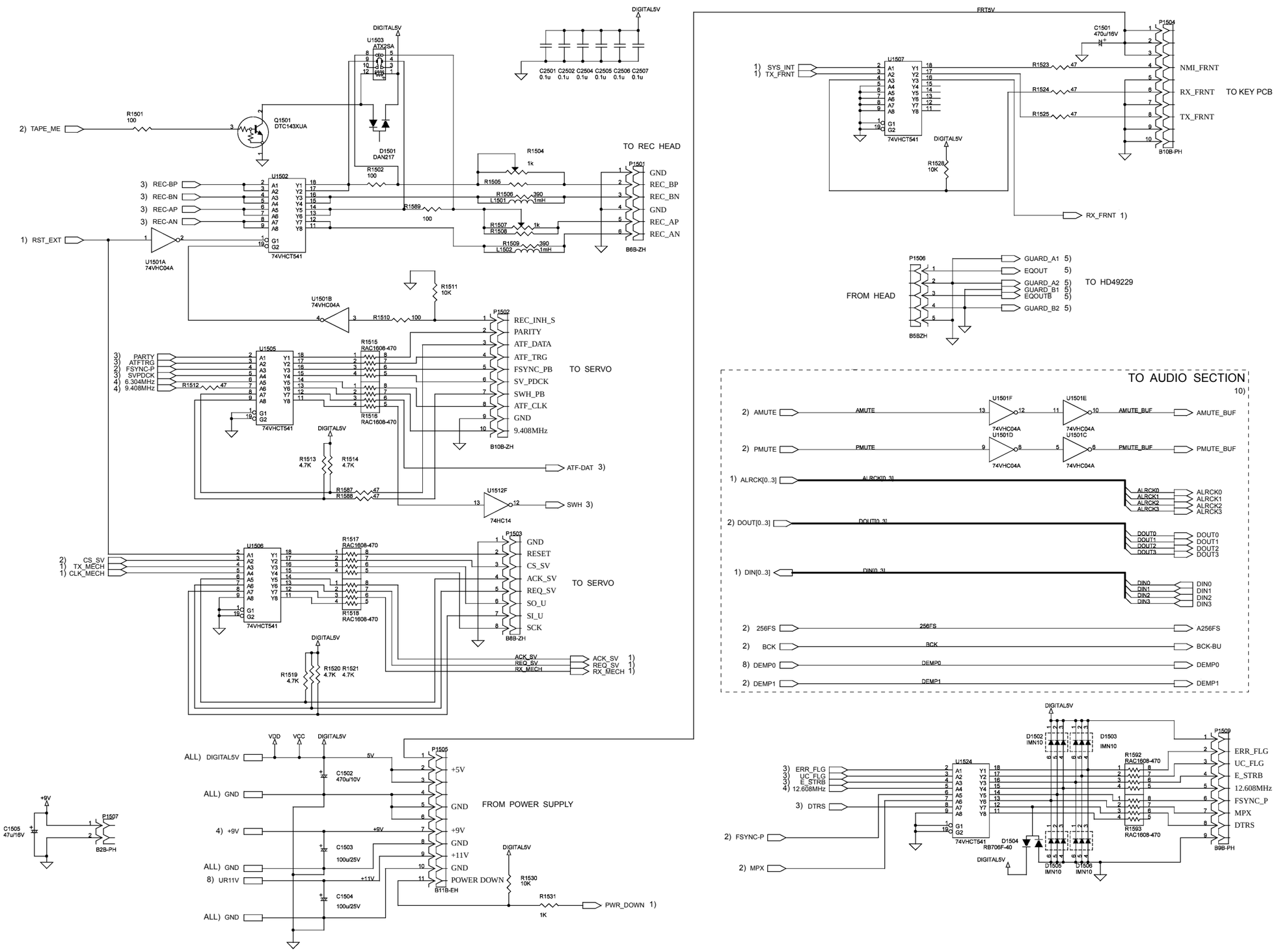
SCHEMATIC DIAGRAM DA-78HR HR-MAIN PCB (4/14)



SCHEMATIC DIAGRAM DA-78HR HR-MAIN PCB (5/14)

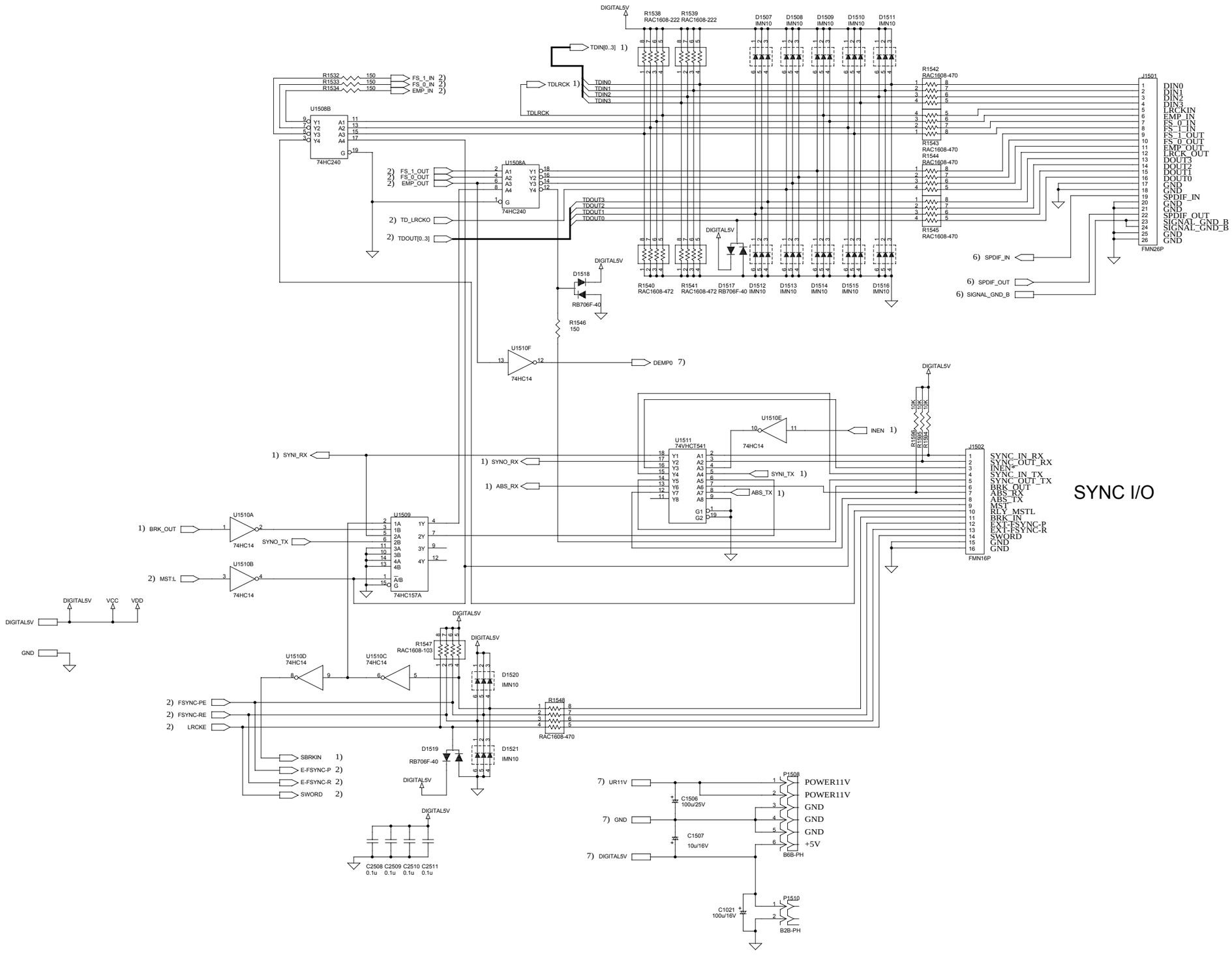



1
2
3
4
5
6
7
A
B
C
D
E
U1404F
74VHCU04A
C1408
0.01u
L1403
BLM21A601S
SPDIF_IN 8)
R1425
150
R1420
150
R1421
150
R1423
270
U1404A
U1404B
U1404C
74VHCU04A
R1422
150
C1407
0.01u
L1404
BK2125HS101
SPDIF_OUT 8)
SIGNAL_GND_B 8)
DIGITAL5V
R1403
RAC1608-103
2) SPD_MUTE
2) SPD_CT0
2) SPD_CT1
2) SPD_TYPE
2) SPD_COPY
R1404
RAC1608-470
R1405
47
R1401
RAC1608-470
U1404D
74VHCU04A
2) FS_1_OUT
2) FS_0_OUT
2) EMP_OUT
U1401
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2
74VHCT541
R1406
R1407
R1408
47
SPD_FS0 1)
SPD_FS1 1)
SPD_EMP 1)
1) SPLRCK
BCK
2) 256FS
2) SPD_RX/TX
R1402
RAC1608-470
R1410
47
R1409
10K
DIGITAL5V
VCC
VDD
GND
U1403D
U1403E
U1403F
74VHCU04
1) SYS_RST
R1424
100K
U1402
M51581
TX RST RX1 NFR RX2 RXSEL PD1 PD2 ULCK RXCKI RXCKO
IMSTRT USYNCO USYNCI IRQU SETSY VSS VDD CNT0 CNT1 LTDT LTCK
LTEN MODE1 MODE0 MUTE CKACO REFCK CKSEL MSTCK LRCKPOL MSBF IIS
SDI SCK WS SDO ADSDI VSS ADSEL FLAGI FLAGO WCK ASL
SPD_UL 1)
R1434
22
MCK_EX 1)
C2401 C2402 C2404
0.1u 0.1u 0.1u
TDOUT3
R1411
47
U1404E
74VHCU04A
2) TDOUT[0..3]
R1412
47
ASLRCK 1)
R1413
R1430
R1431
R1432
47
AESIN0
AESIN1
AESIN2
AESIN3
AESIN[0..3]
AESIN[0..3] 1)
TP192
SPD_MCK
C1402
0.022u
R1416
10K
C1403
0.1u
U1403A
R1418
100K
R1419
47
+9V
U1407
78L05
C1409
100u/16V
C1410
10u
L1401
47u
C1401
100u/16V
C2403
0.1u
R1415
100K
R1417
1K
C1404
2200p
U1403B
U1403C
74VHCU04
D1401
HVC376B
L1402
5.6u
C1405
18p
C1406
220p

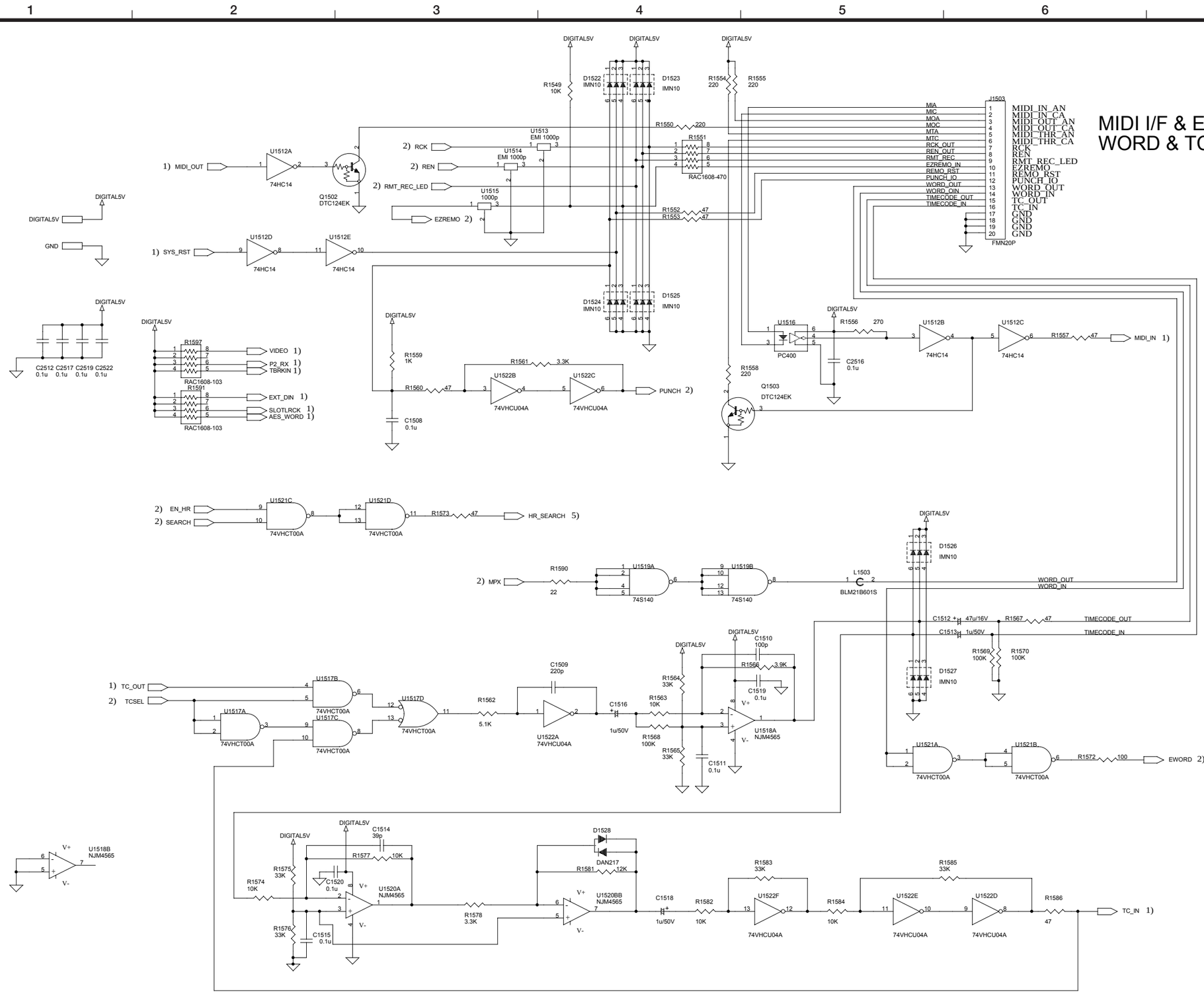

1
2
3
4
5
6
7
A
B
C
D
E
DIGITAL5V
U1503
ATX2SA
C2501 C2502 C2504 C2505 C2506 C2507
0.1u 0.1u 0.1u 0.1u 0.1u 0.1u
2) TAPE_ME
R1501
100
Q1501
DTC143XUA
D1501
DAN217
R1502
100
R1504
1k
R1505
R1508
390
L1501
1mH
R1507
1k
R1508
R1509
390
L1502
1mH
R1589
100
TO REC HEAD
P1501
GND
REC_BP
REC_BN
GND
REC_AP
REC_AN
B6B-ZH
U1502
74VHCT541
3) REC-BP
3) REC-BN
3) REC-AP
3) REC-AN
1) RST_EXT
U1501A
74VHC04A
R1511
10K
U1501B
74VHC04A
R1510
100
P1502
REC_INH_S
PARITY
ATF_DATA
ATF_TRG
FSYNC_PB
SV_PDCK
SWH_PB
ATF_CLK
GND
9.408MHz
B10B-ZH
TO SERVO
U1505
74VHCT541
3) PARITY
3) ATFTRG
2) FSYNC-P
3) SVPDCK
4) 6.304MHz
4) 9.408MHz
R1512
47
R1515
RAC1608-470
R1516
RAC1608-470
R1513
4.7K
R1514
4.7K
R1587
47
R1588
47
U1512F
74HC14
ATF-DAT 3)
SWH 3)
U1506
74VHCT541
2) CS_SV
1) TX_MECH
1) CLK_MECH
R1517
RAC1608-470
R1518
RAC1608-470
P1503
GND
RESET
CS_SV
ACK_SV
REQ_SV
SO_U
SI_U
SCK
B8B-ZH
TO SERVO
R1519
4.7K
R1520
4.7K
R1521
4.7K
ACK_SV
REQ_SV
RX_MECH
ACK_SV 1)
REQ_SV 1)
RX_MECH 1)
FRT5V
C1501
470u/16V
P1504
1) SYS_INT
1) TX_FRNT
U1507
74VHCT541
R1523
47
R1524
47
R1525
47
NMI_FRNT
RX_FRNT
TX_FRNT
TO KEY PCB
B10B-PH
R1526
10K
RX_FRNT 1)
P1506
FROM HEAD
GUARD_A1 5)
EQOUT 5)
GUARD_A2 5)
GUARD_B1 5)
EQOUTB 5)
GUARD_B2 5)
TO HD49229
B5BZH
TO AUDIO SECTION
10)
2) AMUTE
AMUTE
U1501F
74VHC04A
U1501E
74VHC04A
AMUTE_BUF
AMUTE_BUF
2) PMUTE
PMUTE
U1501D
74VHC04A
U1501C
74VHC04A
PMUTE_BUF
PMUTE_BUF
1) ALRCK[0..3]
ALRCK[0..3]
ALRCK0
ALRCK1
ALRCK2
ALRCK3
2) DOUT[0..3]
DOUT[0..3]
DOUT0
DOUT1
DOUT2
DOUT3
1) DIN[0..3]
DIN[0..3]
DIN0
DIN1
DIN2
DIN3
2) 256FS
256FS
A256FS
2) BCK
BCK
BCK-BU
8) DEMP0
DEMP0
DEMP0
2) DEMP1
DEMP1
DEMP1
VDD
VCC
DIGITAL5V
ALL) DIGITAL5V
5V
C1502
470u/10V
P1505
+5V
ALL) GND
GND
FROM POWER SUPPLY
4) +9V
+9V
C1503
100u/25V
+9V
GND
+11V
GND
POWER DOWN
ALL) GND
8) UR11V
+11V
C1504
100u/25V
ALL) GND
B11B-EH
R1530
10K
R1531
1K
PWR_DOWN 1)
+5V
C1505
47u/16V
P1507
B2B-PH
DIGITAL5V
D1502
IMN10
D1503
IMN10
R1592
RAC1608-470
U1524
74VHCT541
3) ERR_FLG
3) UC_FLG
3) E_STRB
4) 12.608MHz
3) DTRS
2) FSYNC-P
2) MPX
D1504
RB706F-40
D1505
IMN10
D1506
IMN10
R1593
RAC1608-470
P1509
ERR_FLG
UC_FLG
E_STRB
12.608MHz
FSYNC_P
MPX
DTRS
B9B-PH

1 2 3 4 5 6 7

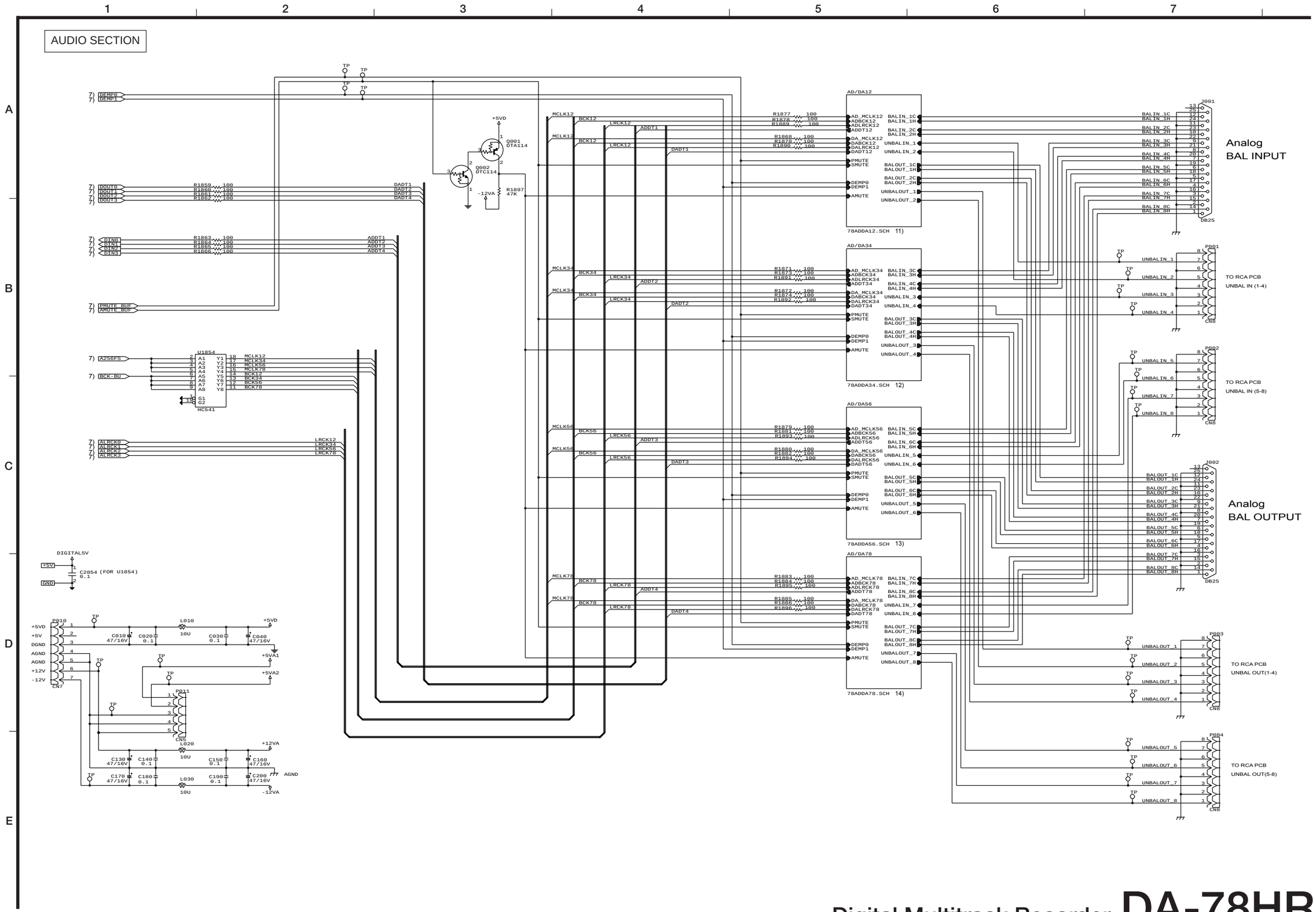
A B C D E



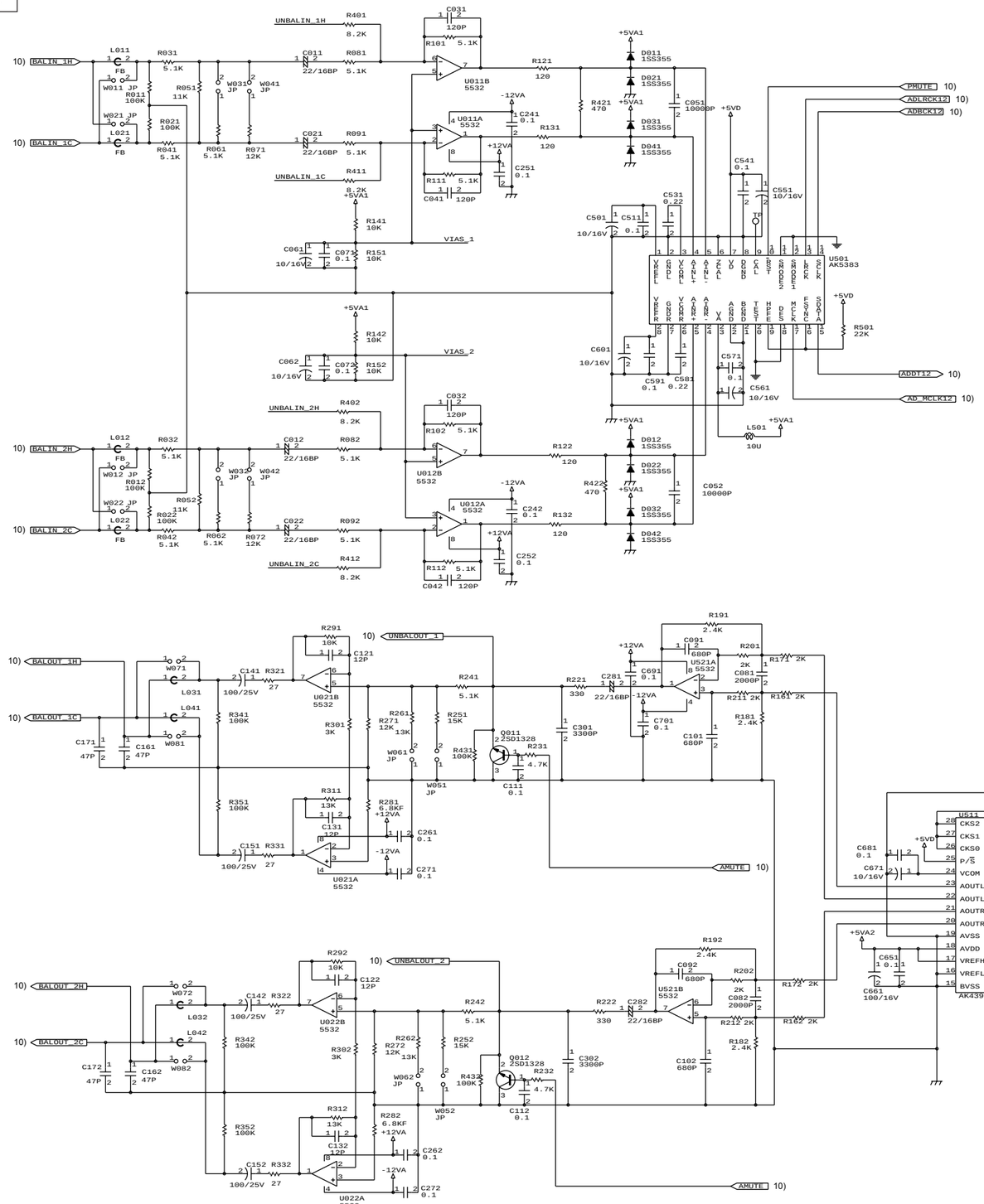
MIDI I/F & EZ-REMOCON WORD & TC I/O

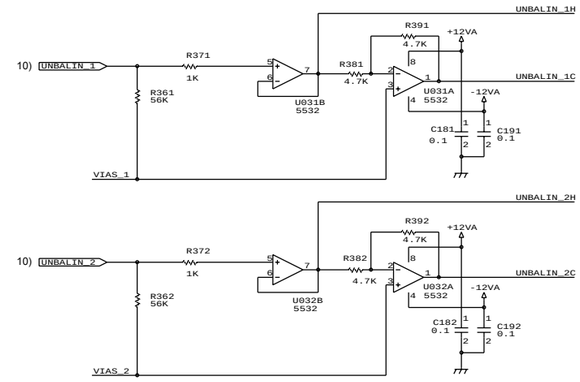


AUDIO SECTION

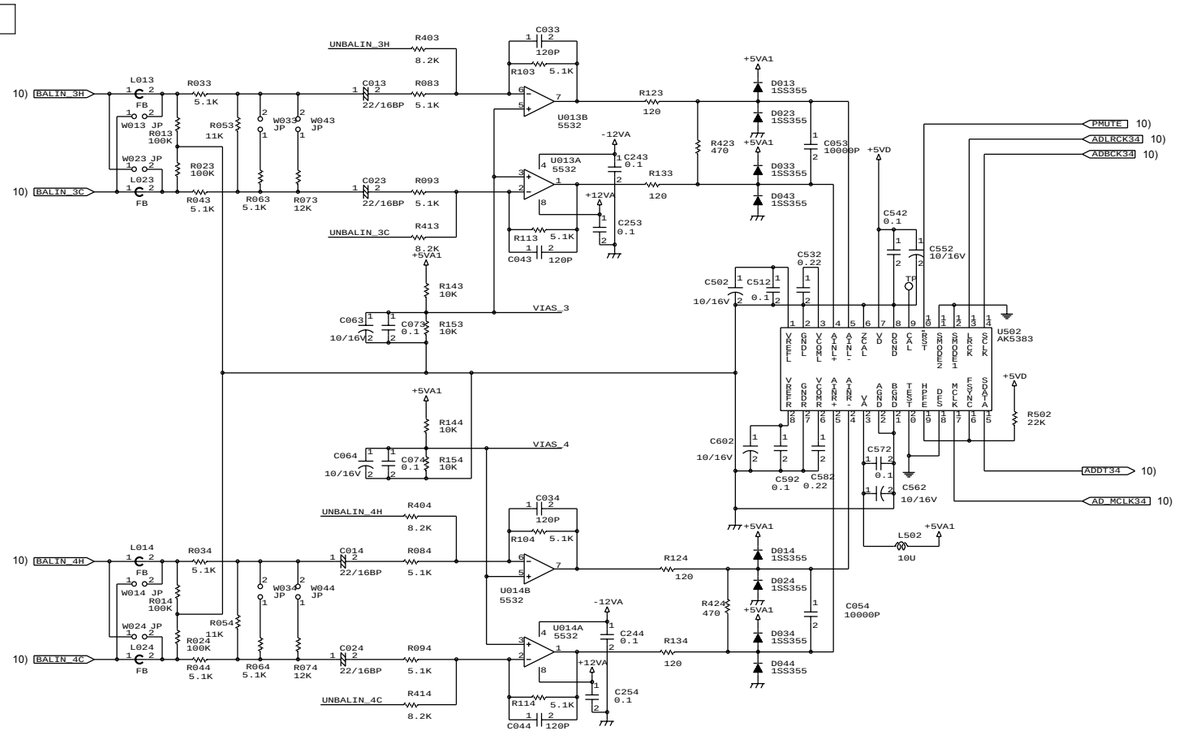


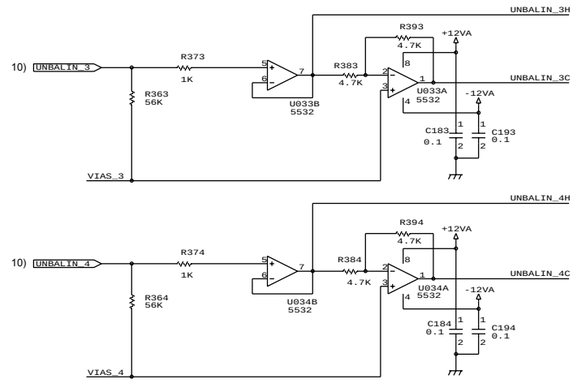
AD/DA 12

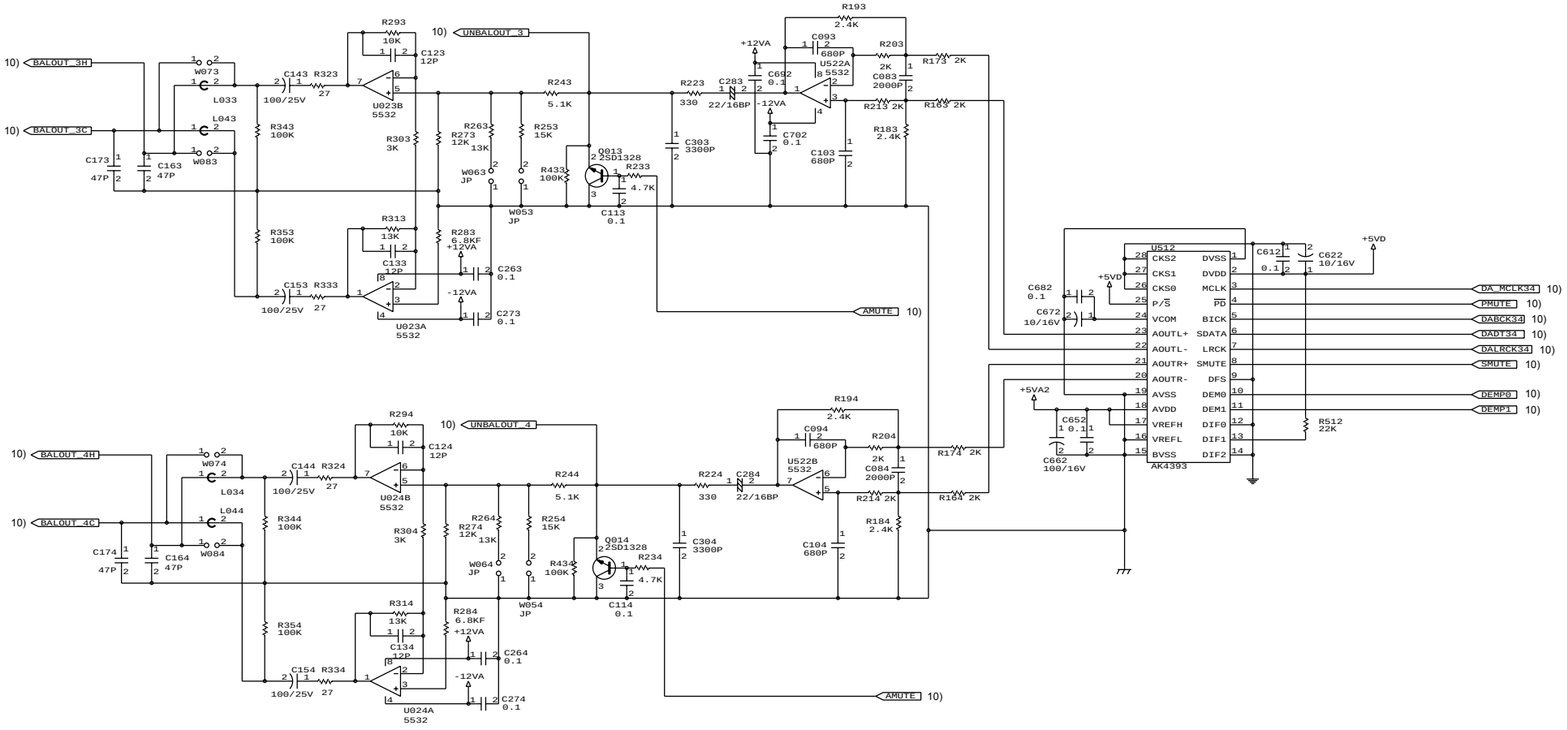

UNBALIN_1H
UNBALIN_1C
UNBALIN_2H
UNBALIN_2C
BALIN_1H
BALIN_1C
BALIN_2H
BALIN_2C
VIAS_1
VIAS_2
+5VA1
-12VA
+12VA
+5VD
U011B 5532
U011A 5532
U012B 5532
U012A 5532
U501 AK5383
PMUTE
ADLRCK12
ADBCK12
ADDT12
AD_MCLK12
UNBALOUT_1
UNBALOUT_2
BALOUT_1H
BALOUT_1C
BALOUT_2H
BALOUT_2C
U021B 5532
U021A 5532
U022B 5532
U022A 5532
AMUTE
U511 AK4393
DA_MCLK12
DABCK12
DADT12
DALRCK12
SMUTE
DEMP0
DEMP1


UNBALIN_1
UNBALIN_1C
VIAS_1
U031B 5532
U031A 5532
UNBALIN_2
UNBALIN_2C
VIAS_2
U032B 5532
U032A 5532

AD/DA 34

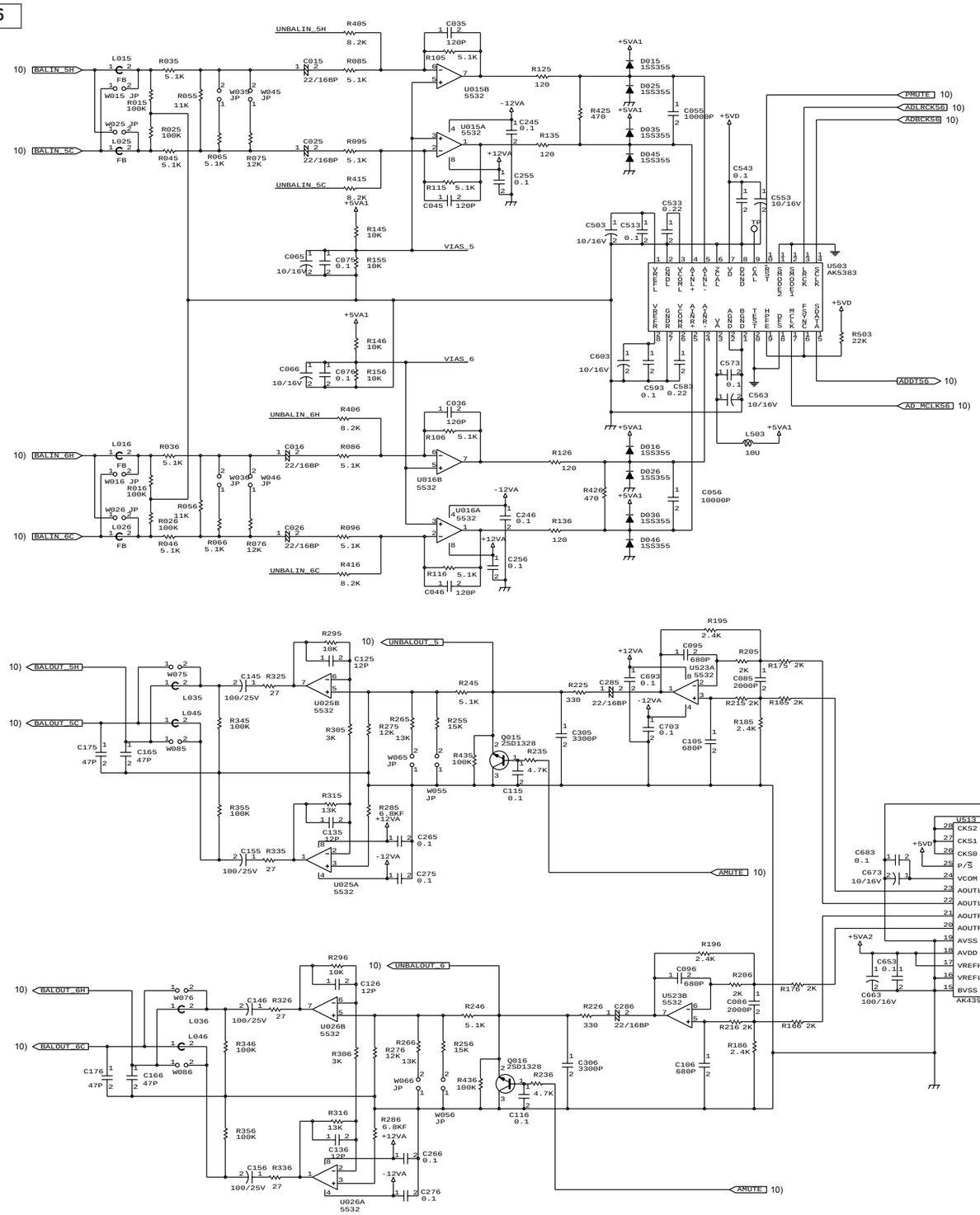

UNBALIN_3H
UNBALIN_3C
UNBALIN_4H
UNBALIN_4C
BALIN_3H
BALIN_3C
BALIN_4H
BALIN_4C
VIAS_3
VIAS_4
U013B 5532
U013A 5532
U014B 5532
U014A 5532
U502 AK5383
+5VA1
-12VA
+12VA
+5VD
PMUTE
ADLRCK34
ADBCK34
ADDT34
AD_MCLK34

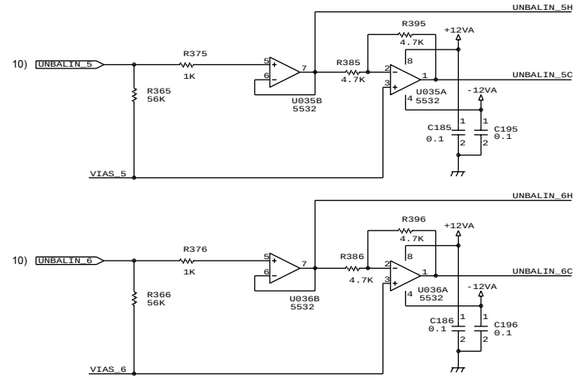

UNBALIN_3
UNBALIN_4
VIAS_3
VIAS_4
U033A 5532
U033B 5532
U034A 5532
U034B 5532
+12VA
-12VA


BALOUT_3H
BALOUT_3C
BALOUT_4H
BALOUT_4C
UNBALOUT_3
UNBALOUT_4
U023B 5532
U023A 5532
U024B 5532
U024A 5532
U522A 5532
U522B 5532
AMUTE
+12VA
-12VA
+5VD
+5VA2

U512
AK4393
DA_MCLK34
PMUTE
DABCK34
DADT34
DALRCK34
SMUTE
DEMP0
DEMP1

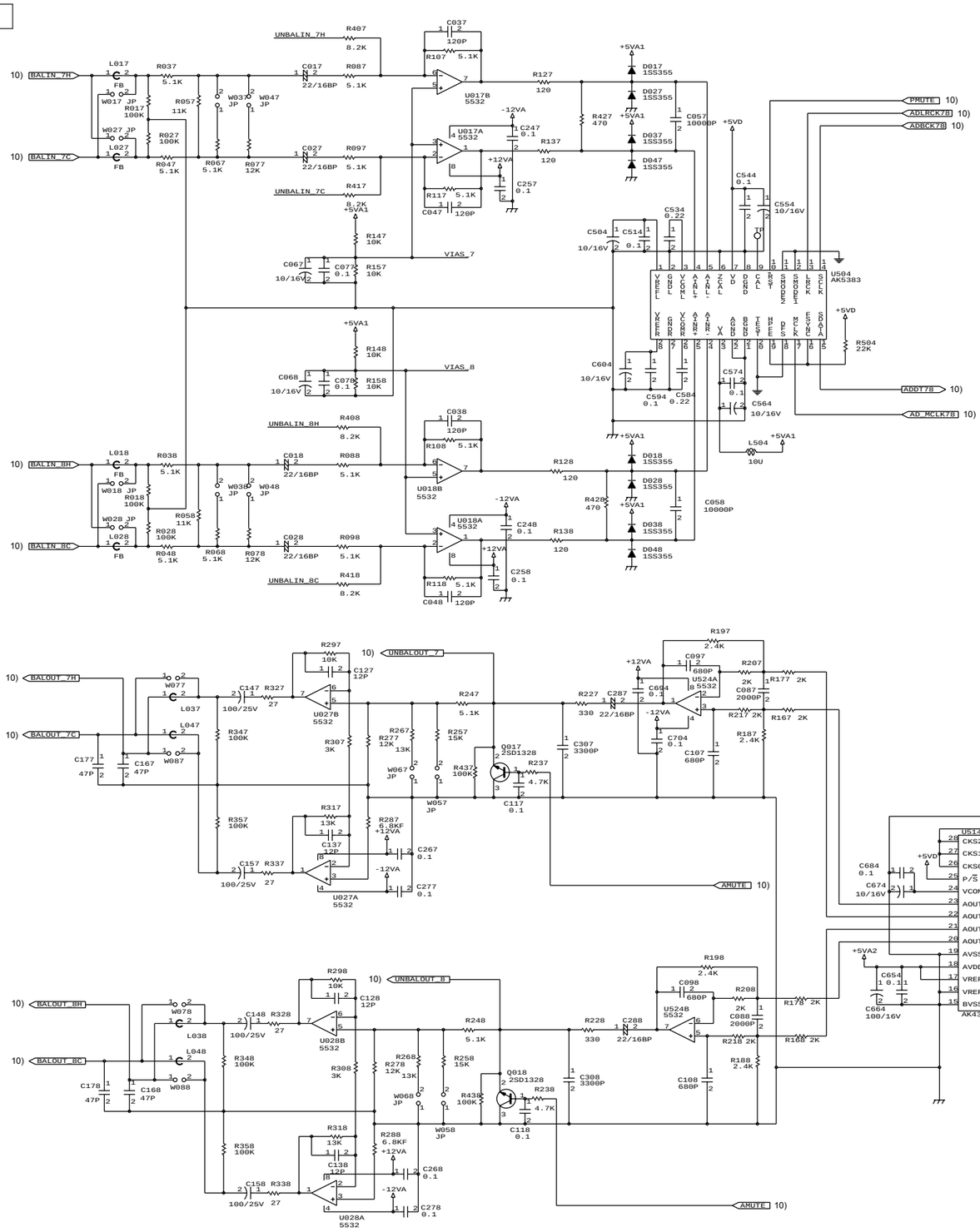
AD/DA 56

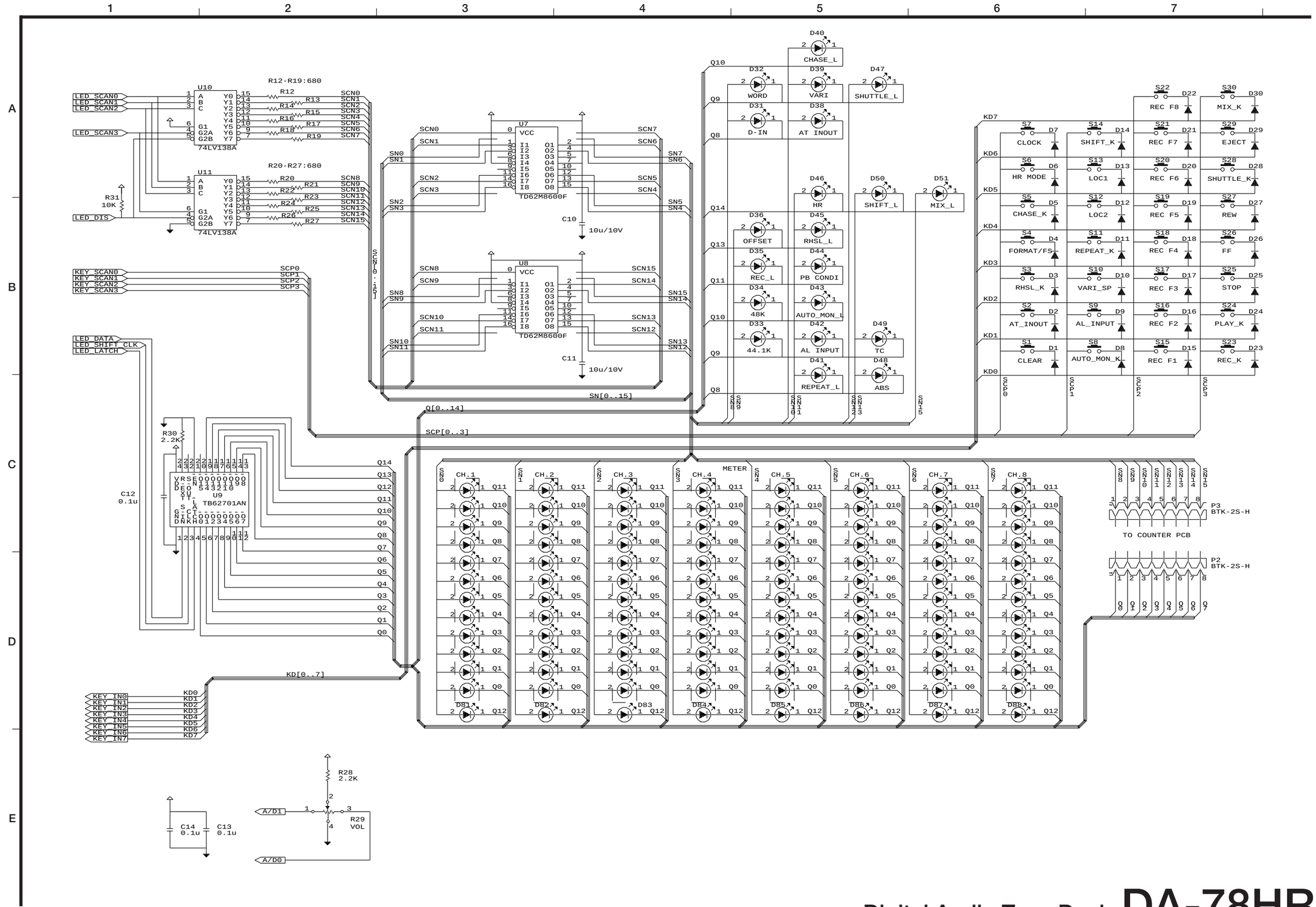

UNBALIN_5H
UNBALIN_5C
UNBALIN_6H
UNBALIN_6C
BALIN_5H
BALIN_5C
BALIN_6H
BALIN_6C
VIAS_5
VIAS_6
+5VA1
-12VA
+12VA
+5VD
PMUTE
ADLRCK56
ADBCK56
ADDT56
AD_MCLK56
U015B 5532
U015A 5532
U016B 5532
U016A 5532
U503 AK5383
C543 0.1
C553 10/16V
C503 10/16V
C513 0.1
C533 0.22
C603 10/16V
C593 0.1
C583 0.22
C573 0.1
C563 10/16V
L503 10U
R503 22K
C056 10000P
C055 10000P
C045 120P
C046 120P
C255 0.1
C256 0.1
C245 0.1
C246 0.1
D015 1SS355
D025 1SS355
D035 1SS355
D045 1SS355
D016 1SS355
D026 1SS355
D036 1SS355
D046 1SS355
R125 120
R135 120
R126 120
R136 120
R425 470
R426 470
R145 10K
R146 10K
R155 10K
R156 10K
R415 8.2K
R416 8.2K
R405 8.2K
R406 8.2K
R105 5.1K
R115 5.1K
R106 5.1K
R116 5.1K
C035 120P
C036 120P
R085 5.1K
R095 5.1K
R086 5.1K
R096 5.1K
C015 22/16BP
C025 22/16BP
C016 22/16BP
C026 22/16BP
R035 5.1K
R045 5.1K
R055 11K
R065 5.1K
R075 12K
R036 5.1K
R046 5.1K
R056 11K
R066 5.1K
R076 12K
W015 JP
W025 JP
W035 JP
W045 JP
W016 JP
W026 JP
W036 JP
W046 JP
R015 100K
R025 100K
R026 100K
R016 100K
L015 FB
L025 FB
L016 FB
L026 FB
C065 10/16V
C075 0.1
C066 10/16V
C076 0.1


UNBALIN_5H
UNBALIN_5C
UNBALIN_6H
UNBALIN_6C
VIAS_5
VIAS_6
U035B 5532
U035A 5532
U036B 5532
U036A 5532
R375 1K
R365 56K
R376 1K
R366 56K
R395 4.7K
R385 4.7K
R396 4.7K
R386 4.7K
C185 0.1
C195 0.1
C186 0.1
C196 0.1
+12VA
-12VA

BALOUT_5H
BALOUT_5C
BALOUT_6H
BALOUT_6C
UNBALOUT_5
UNBALOUT_6
AMUTE
U025B 5532
U025A 5532
U026B 5532
U026A 5532
U523A 5532
U523B 5532
Q015 2SD1328
Q016 2SD1328
R195 2.4K
R196 2.4K
R205 2K
R206 2K
R175 2K
R185 2.4K
R215 2K
R165 2K
R176 2K
R186 2.4K
R216 2K
R166 2K
C095 680P
C085 2000P
C105 680P
C086 2000P
C106 680P
C693 0.1
C703 0.1
C663 100/16V
C653 0.1
C683 0.1
C673 10/16V
C613 0.1
C623 10/16V
R513 22K
U513 AK4393
DA_MCLK56
PMUTE
DABCK56
DADT56
DALRCK56
SMUTE
DEMP0
DEMP1
+5VA2
+5VD

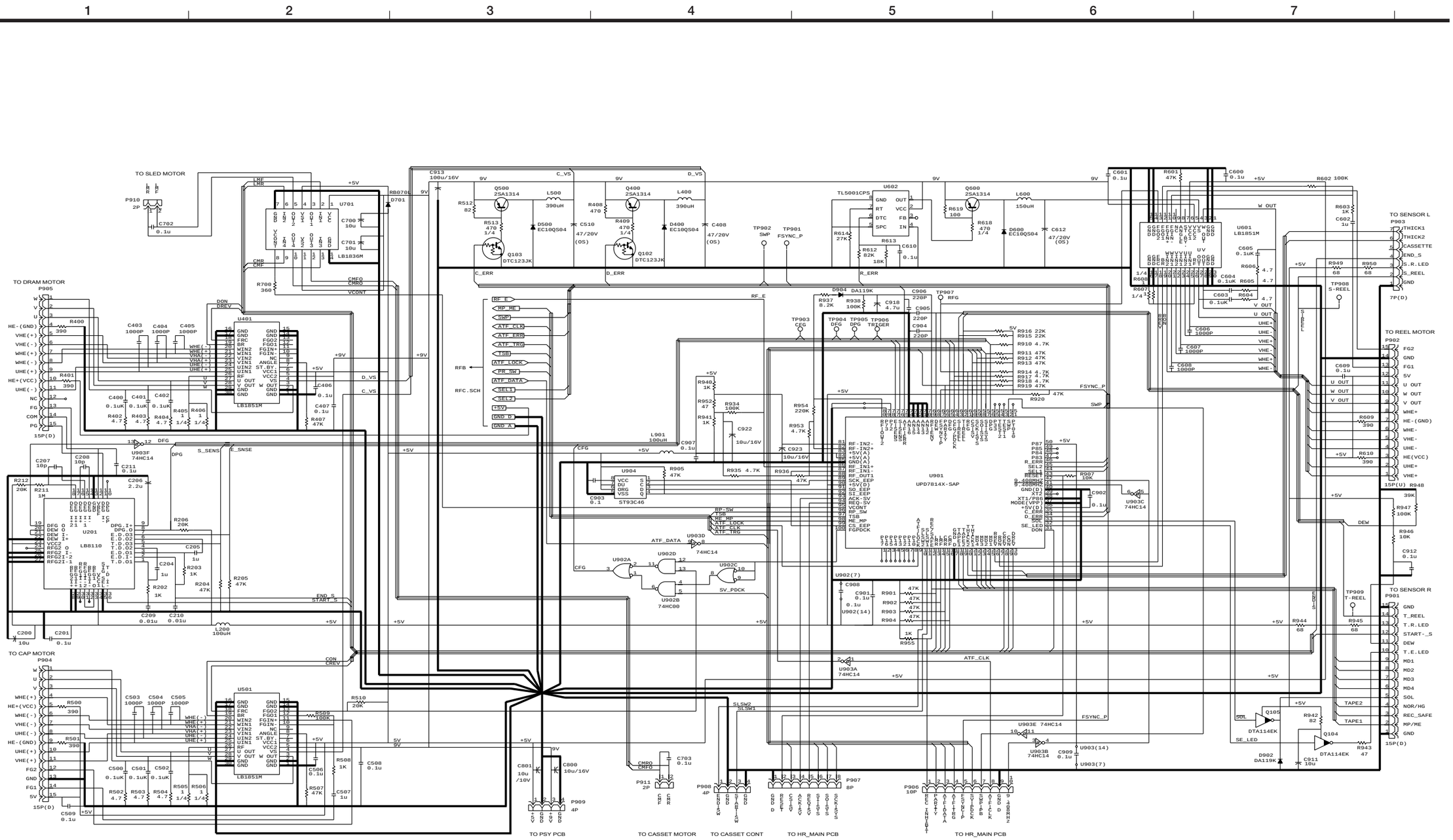
AD/DA 78

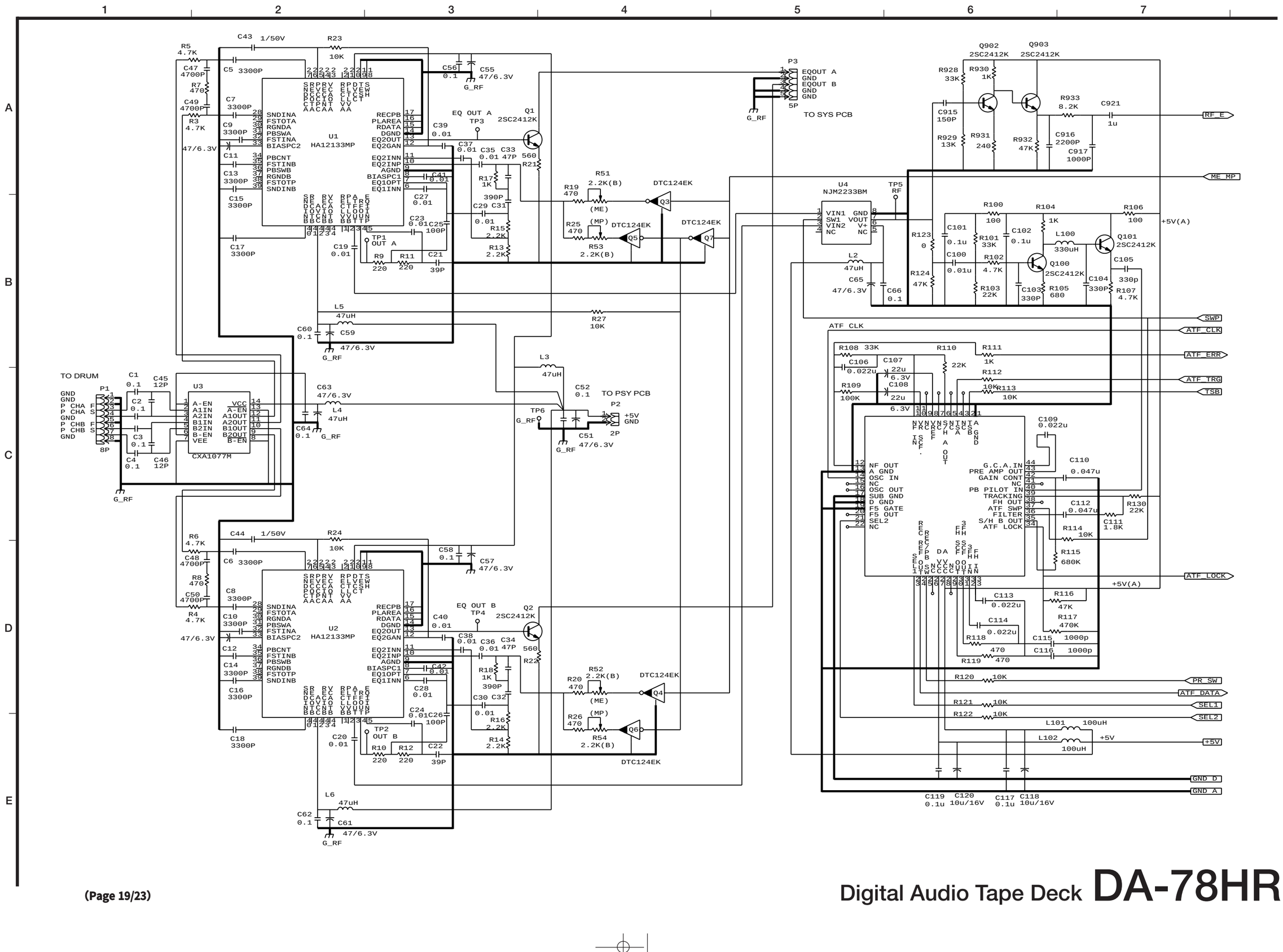

BALIN_7H
BALIN_7C
BALIN_8H
BALIN_8C
UNBALIN_7H
UNBALIN_7C
UNBALIN_8H
UNBALIN_8C
VIAS_7
VIAS_8
U017B 5532
U017A 5532
U018B 5532
U018A 5532
U504 AK5383
PMUTE 10)
ADLRCK78 10)
ADBCK78 10)
ADDT78 10)
AD_MCLK78 10)
BALOUT_7H
BALOUT_7C
BALOUT_8H
BALOUT_8C
UNBALOUT_7
UNBALOUT_8
U027B 5532
U027A 5532
U028B 5532
U028A 5532
AMUTE 10)
U514 AK4393
DA_MCLK78 10)
PMUTE 10)
DABCK78 10)
DADT78 10)
DALRCK78 10)
SMUTE 10)
DEMP0 10)
DEMP1 10)

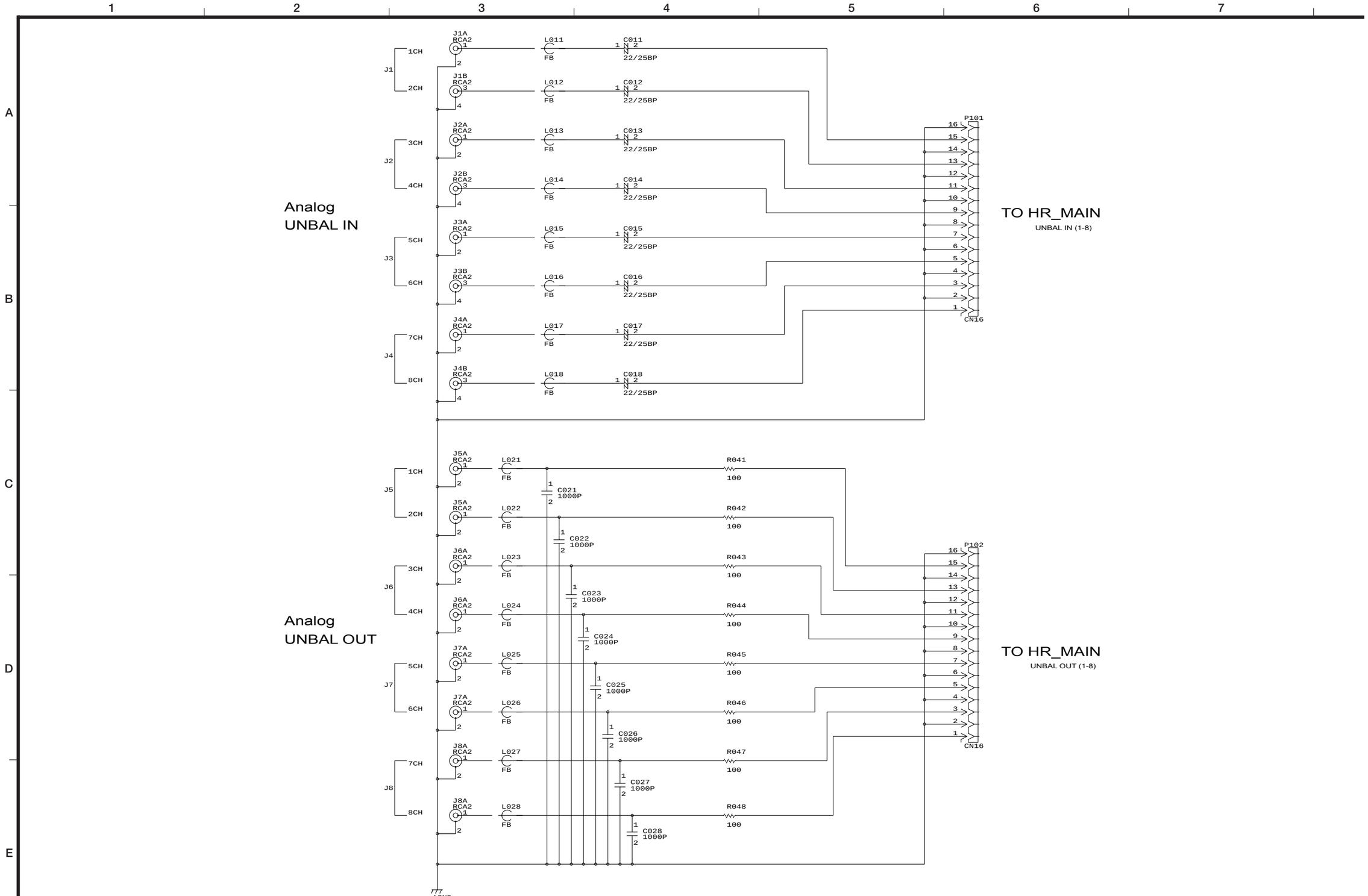

1
2
3
4
5
6
7
A
B
C
D
E
R12-R19:680
R20-R27:680
U10
U11
74LV138A
LED_SCAN0
LED_SCAN1
LED_SCAN2
LED_SCAN3
LED_DIS
R31
10K
SCN0
SCN1
SCN2
SCN3
SCN4
SCN5
SCN6
SCN7
SCN8
SCN9
SCN10
SCN11
SCN12
SCN13
SCN14
SCN15
U7
U8
TD62M8600F
C10
10u/10V
C11
10u/10V
SN0
SN1
SN2
SN3
SN4
SN5
SN6
SN7
SN8
SN9
SN10
SN11
SN12
SN13
SN14
SN15
SCN[0..15]
SCP0
SCP1
SCP2
SCP3
KEY_SCAN0
KEY_SCAN1
KEY_SCAN2
KEY_SCAN3
SCP[0..3]
Q[0..14]
LED_DATA
LED_SHIFT_CLK
LED_LATCH
R30
2.2K
C12
0.1u
U9
TB62701AN
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
KD[0..7]
KD0
KD1
KD2
KD3
KD4
KD5
KD6
KD7
KEY_IN0
KEY_IN1
KEY_IN2
KEY_IN3
KEY_IN4
KEY_IN5
KEY_IN6
KEY_IN7
R28
2.2K
R29
VOL
C13
0.1u
C14
0.1u
A/D1
A/D0
D40
CHASE_L
D32
WORD
D39
VARI
D47
SHUTTLE_L
D31
D-IN
D38
AT INOUT
D46
HR
D50
SHIFT_L
D51
MIX_L
D36
OFFSET
D45
RHSL_L
D35
REC_L
D44
PB CONDI
D34
48K
D43
AUTO_MON_L
D33
44.1K
D42
AL INPUT
D49
TC
D41
REPEAT_L
D48
ABS
S7
CLOCK
S14
SHIFT_K
S21
REC F7
S29
EJECT
S6
HR MODE
S13
LOC1
S20
REC F6
S28
SHUTTLE_K
S5
CHASE_K
S12
LOC2
S19
REC F5
S27
REW
S4
FORMAT/FS
S11
REPEAT_K
S18
REC F4
S26
FF
S3
RHSL_K
S10
VARI_SP
S17
REC F3
S25
STOP
S2
AT_INOUT
S9
AL_INPUT
S16
REC F2
S24
PLAY_K
S1
CLEAR
S8
AUTO_MON_K
S15
REC F1
S23
REC_K
S22
REC F8
S30
MIX_K
KD7
KD6
KD5
KD4
KD3
KD2
KD1
KD0
METER
CH.1
CH.2
CH.3
CH.4
CH.5
CH.6
CH.7
CH.8
D81
D82
D83
D84
D85
D86
D87
D88
P3
BTK-2S-H
TO COUNTER PCB
P2
BTK-2S-H

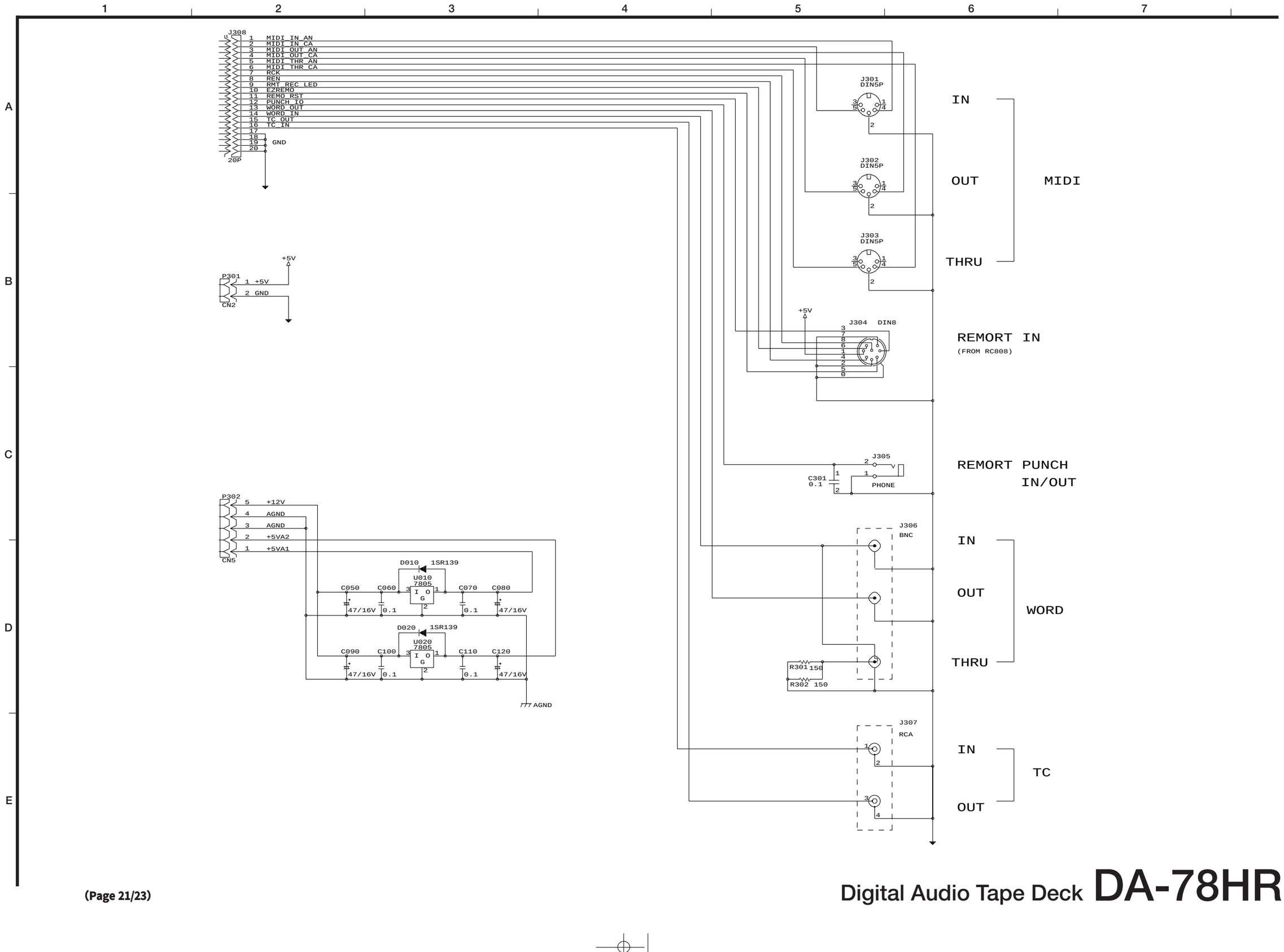
1
2
3
4
5
6
7
A
B
C
D
E
C1 0.1u
C2 0.1u
C3 0.1u
C4 0.1u
C5 0.1u
C6 0.1u
C7 0.1u
TP2 GND
TP3 GND
TP4 GND
TP1 GND
R1 10K
U3 TEST
R2 10K
R3 3.9K
R4 1.5K
U2 M51957
C8 1u\16V
X1 12MHz
U1 UPD784031
U5 74HC573
U6 27C512
D37 PLAY_L
R32 330
R33 330
U12 DTC124EKA
C18 100p
C19 100p
C17 100p
R6 10K
R5 10K
R7 47
C9 100U/10V
R8 47
R9 47
R11 47
R10 47
U4 LVC541
P1
TO HR-MAIN
10P
LED_SHIFT_CLK
LED_DATA
LED_LATCH
LED_DIS
LED_SCAN3
LED_SCAN2
LED_SCAN1
LED_SCAN0
A[8..15]
D[0..D8]
KEY_IN7
KEY_IN6
KEY_IN5
KEY_IN4
KEY_IN3
KEY_IN2
KEY_IN1
KEY_IN0
VER_2
VER_1
KEY_SCAN0
KEY_SCAN1
KEY_SCAN2
KEY_SCAN3
KEY_SCAN4
KEY_SCAN5
KEY_SCAN6
KEY_SCAN7
A/D1
A/D0
KEY PCB (MPU)
P0
S0
SDDLB14000
S2P3-VH
C0
0.0047u
SW PCB
J1
J2
TO KEY PCB
BTK-8S-2S
D52 LB302DF
D53 LB302DF
D54 LB302DF
D55 LB302DF
LED:ANODE_COMMON
COUNTER PCB

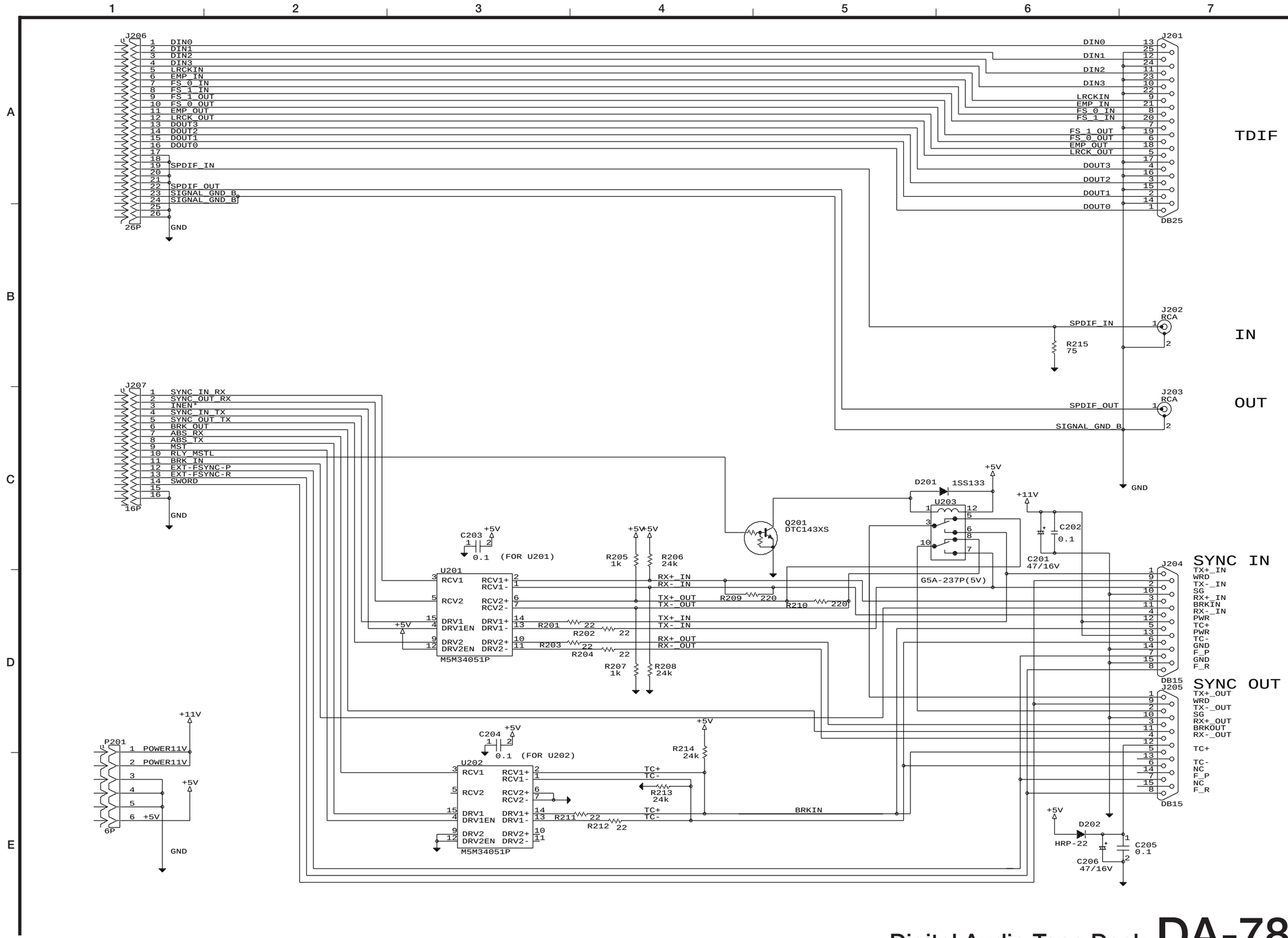
SCHEMATIC DIAGRAM DA-78HR SERVO PCB (1/2)



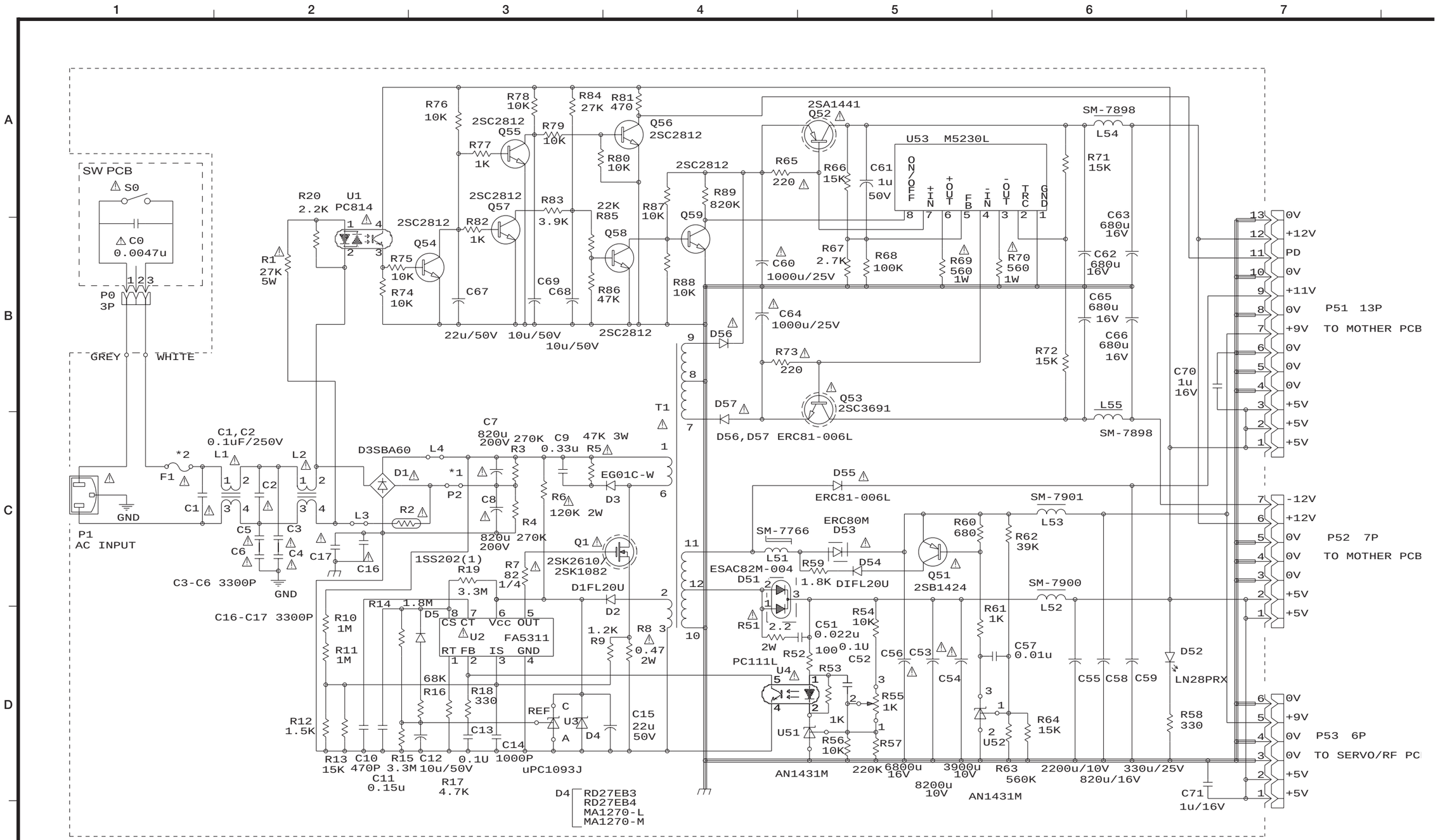

1
2
3
4
5
6
7
A
B
C
D
E
U1
HA12133MP
U2
HA12133MP
U3
CXA1077M
U4
NJM2233BM
Q1
2SC2412K
Q2
2SC2412K
Q3
DTC124EK
Q4
DTC124EK
Q5
DTC124EK
Q6
DTC124EK
Q7
DTC124EK
Q902
2SC2412K
Q903
2SC2412K
Q100
2SC2412K
Q101
2SC2412K
TO DRUM
TO SYS PCB
TO PSY PCB
EQ OUT A
EQ OUT B
TP1 OUT A
TP2 OUT B
TP3
TP4
TP5 RF
TP6
P1
P2
P3
8P
2P
5P
EQOUT A
EQOUT B
GND
+5V
ATF CLK
RF_E
ME_MP
SWP
ATF_CLK
ATF_ERR
ATF_TRG
TSB
ATF_LOCK
+5V(A)
PR_SW
ATF_DATA
SEL1
SEL2
+5V
GND_D
GND_A
G_RF


1
2
3
4
5
6
7
A
B
C
D
E
Analog
UNBAL IN
J1A
RCA2
1CH
2CH
J1
J1B
J2A
3CH
4CH
J2
J2B
J3A
5CH
6CH
J3
J3B
J4A
7CH
8CH
J4
J4B
L011
L012
L013
L014
L015
L016
L017
L018
FB
C011
C012
C013
C014
C015
C016
C017
C018
22/25BP
P101
CN16
TO HR_MAIN
UNBAL IN (1-8)
Analog
UNBAL OUT
J5A
J5
J6A
J6
J7A
J7
J8A
J8
L021
L022
L023
L024
L025
L026
L027
L028
R041
R042
R043
R044
R045
R046
R047
R048
100
C021
C022
C023
C024
C025
C026
C027
C028
1000P
P102
TO HR_MAIN
UNBAL OUT (1-8)
AGND


1
2
3
4
5
6
7
A
B
C
D
E
J308
1 MIDI_IN_AN
2 MIDI_IN_CA
3 MIDI_OUT_AN
4 MIDI_OUT_CA
5 MIDI_THR_AN
6 MIDI_THR_CA
7 RCK
8 REN
9 RMT_REC_LED
10 EZREMO
11 REMO_RST
12 PUNCH_IO
13 WORD_OUT
14 WORD_IN
15 TC_OUT
16 TC_IN
17
18
19 GND
20
20P
J301
DIN5P
IN
J302
DIN5P
OUT
MIDI
J303
DIN5P
THRU
+5V
P301
1 +5V
2 GND
CN2
+5V
J304 DIN8
REMORT IN
(FROM RC808)
J305
PHONE
C301
0.1
REMORT PUNCH
IN/OUT
P302
5 +12V
4 AGND
3 AGND
2 +5VA2
1 +5VA1
CN5
D010 1SR139
U010
7805
C050 C060 C070 C080
47/16V 0.1 0.1 47/16V
D020 1SR139
U020
7805
C090 C100 C110 C120
47/16V 0.1 0.1 47/16V
AGND
J306
BNC
IN
OUT
THRU
WORD
R301 150
R302 150
J307
RCA
IN
OUT
TC

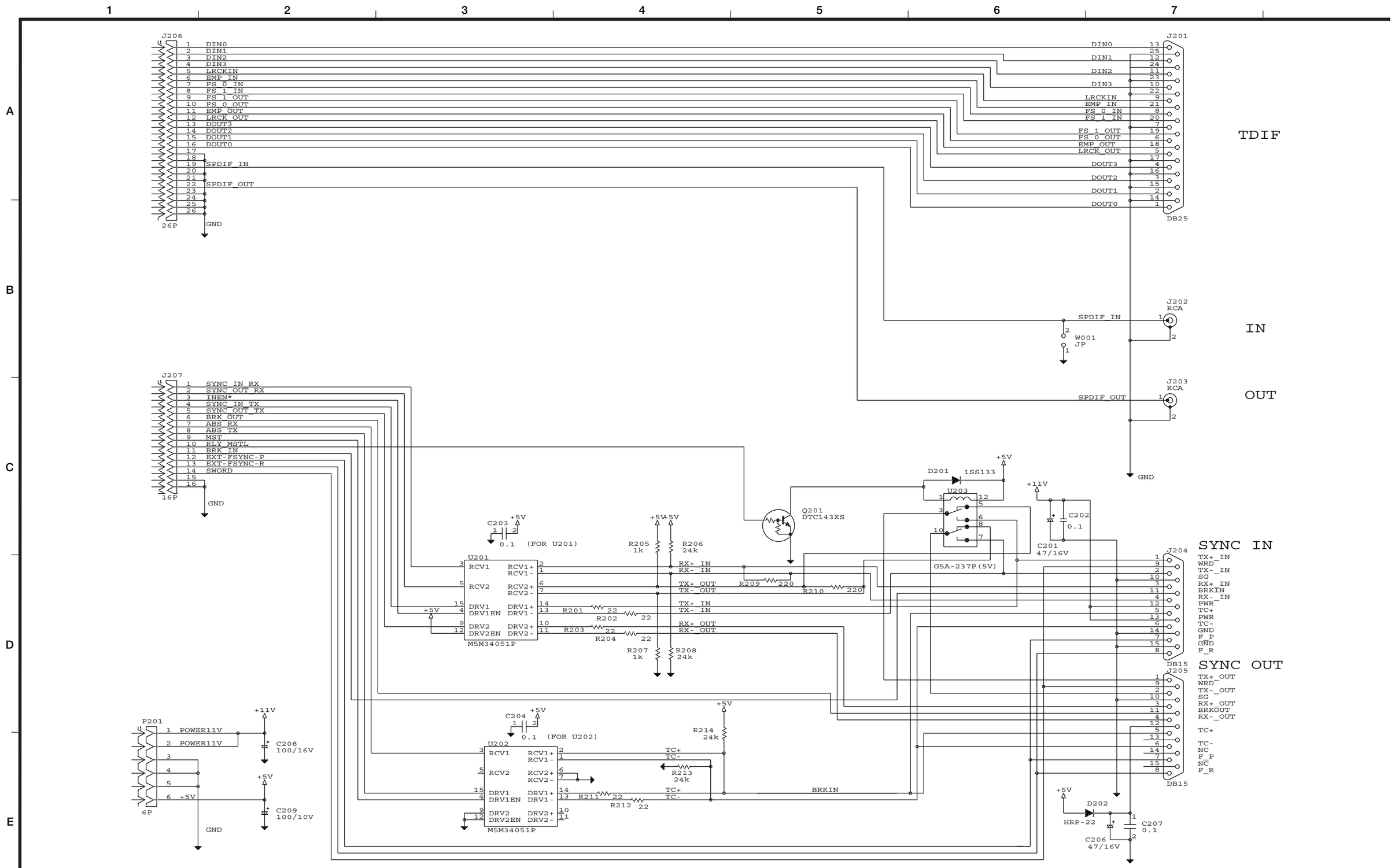

1
2
3
4
5
6
7
A
B
C
D
E
J206
1 DIN0
2 DIN1
3 DIN2
4 DIN3
5 LRCKIN
6 EMP_IN
7 FS_0_IN
8 FS_1_IN
9 FS_1_OUT
10 FS_0_OUT
11 EMP_OUT
12 LRCK_OUT
13 DOUT3
14 DOUT2
15 DOUT1
16 DOUT0
17
18
19 SPDIF_IN
20
21
22 SPDIF_OUT
23 SIGNAL_GND_B
24 SIGNAL_GND_B
25
26
26P
GND
J201
DIN0 13
DIN1 25
DIN2 12
DIN3 24
LRCKIN 11
EMP_IN 23
FS_0_IN 10
FS_1_IN 22
FS_1_OUT 9
FS_0_OUT 21
EMP_OUT 8
LRCK_OUT 20
DOUT3 7
DOUT2 19
DOUT1 6
DOUT0 18
5
17
4
16
3
15
2
14
1
DB25
TDIF
J202
RCA
SPDIF_IN 1
2
R215
75
IN
J203
RCA
SPDIF_OUT 1
SIGNAL_GND_B 2
OUT
GND
J207
1 SYNC_IN_RX
2 SYNC_OUT_RX
3 INEN*
4 SYNC_IN_TX
5 SYNC_OUT_TX
6 BRK_OUT
7 ABS_RX
8 ABS_TX
9 MST
10 RLY_MSTL
11 BRK_IN
12 EXT-FSYNC-P
13 EXT-FSYNC-R
14 SWORD
15
16
16P
GND
+5V
D201 1SS133
U203
G5A-237P(5V)
+11V
C202 0.1
C201 47/16V
Q201 DTC143XS
C203 0.1 (FOR U201)
R205 1k
R206 24k
U201
RCV1 RCV1+ RCV1-
RCV2 RCV2+ RCV2-
DRV1 DRV1+ DRV1-
DRV1EN
DRV2 DRV2+ DRV2-
DRV2EN
M5M34051P
RX+_IN
RX-_IN
TX+_OUT
TX-_OUT
TX+_IN
TX-_IN
RX+_OUT
RX-_OUT
R209 220
R210 220
R201 22
R202 22
R203 22
R204 22
R207 1k
R208 24k
J204
SYNC IN
TX+_IN
WRD
TX-_IN
SG
RX+_IN
BRKIN
RX-_IN
PWR
TC+
PWR
TC-
GND
F_P
GND
F_R
DB15
J205
SYNC OUT
TX+_OUT
WRD
TX-_OUT
SG
RX+_OUT
BRKOUT
RX-_OUT
TC+
TC-
NC
F_P
NC
F_R
DB15
P201
1 POWER11V
2 POWER11V
3
4
5
6 +5V
6P
+11V
+5V
GND
C204 0.1 (FOR U202)
R214 24k
U202
R213 24k
R211 22
R212 22
BRKIN
D202 HRP-22
C205 0.1
C206 47/16V

SCHEMATIC DIAGRAM DA-78HR POWER SUPPLY SECTION



*1 *2

	*1		*2
DM TCA/CND	SHORT	100V-120V	T4A L 125V
EUR KOR UK AUS	OPEN	230V-240V	T3.15A L 250V



Digital Multitrack Recorder **DA-78HR**

2 nd Issue; August 2000

TASCAM DA-78HR Version 1.13

These notes refer to changes and additions in the system version 1.13 of the DA-78HR DTRS recorder. Please keep this sheet together with the original documentation for the DA-78HR.

TC Rec once mode (TC menu group)

Previously, the TC Record enable parameter was automatically switched off when recording was completed. This has been changed, so that the timecode record enable parameter can now be left on following recording.

The three options now available using the tcrEcEn (**TCRECEN**) submenu from the **TC** menu are:

rEc. oFF **OFF**	Timecode recording is disabled
rEc. oncE **ONCE**	Timecode recording is enabled, but will automatically be disabled when recording is complete.
rEc. on **ON**	Timecode recording is enabled, and will remain enabled after recording is complete.

There is an alternative way of turning this function on and off, without using the menu system:

Pressing and holding the **SHIFT** key, and pressing the **CLOCK** key will turn the function on if it is oFF, or oFF if it is currently set to oncE or on.

It is not possible to make the oncE setting in this way.

If the DA-78HR is operated using a remote control unit, the oncE setting cannot be made.

Sampling frequency message

If a tape recorded on the DA-98HR with a track format different from the "standard" 8 x base-frequency tracks is loaded in the DA-78HR, the following message is displayed:

Err. HiFS (**ERR HIFS**).

NOTE

It is possible to record on a tape, even when this message appears, but the HR mode used will be that of the machine's current setting, and will overwrite that on tape. Even if the tape is then replayed on a DA-98HR, the original format cannot be re-used.

Play TC Out (TC menu group)

This new feature allows the setting of when LTC will be output by the DA-78HR, which may be found useful when using the DA-78HR with some timecode slave units.

There are two options for this LocYtc (**LOCK TC**) submenu from the **TC** menu:

0	which outputs LTC as soon as the DA-78HR starts to play back, even before the servo is locked.
1	outputs LTC when the unit servo is locked (in the same way that audio data is only output when the unit is servo-locked).

Error message

The DA-98HR can record at base, dual or quad sampling frequency, and this Track Fs information is now included as part of the TDIF data. The "E bit" portion of the TDIF data, previously unused, contains this Track Fs information.

Since the DA-78HR unit can only record using the base Fs, if it receives TDIF data with mismatched Track Fs information (that is, the E bit shows quad- or dual-frequency mode), the following message is displayed:

E. dio (**E.DIO**)

IMPORTANT NOTE

If this message is displayed, you should not record on the tape. Even if it appears that you have recorded on the tape, correct playback will be impossible, even if it is played back on a DA-98HR with its Fs settings set to the original settings.

TDIF E Bit (Audio 1 menu group)

This new menu item allows you to ignore E bit data embedded in the incoming TDIF data, which under certain circumstances may be falsely interpreted by the DA-78HR as being errors (for example, when non-HR TDIF data is received from certain units). If such units output E bit data, the message described above will appear, even if the audio data is correctly formatted.

This Ed iF. E (**TDIF.E**) submenu item in the Audio 1 menu group allows any such spurious data to be ignored and the error message suppressed:

There are two options:

0	(default) the error message is shown.
1	the error message is suppressed.

IMPORTANT NOTE

If you are suppressing the error message, you must be certain that the incoming TDIF data Track Fs setting is eight base-frequency tracks. If you attempt recording when there is a data mismatch, even if it appears that you have recorded on the tape, correct playback will be impossible, even if it is played back on a DA-98HR with its Fs settings set to the original settings.

TEAC **TECHNICAL INFORMATION**

TASCAM DA-78HR, ROM Upgrade (Main V1.17)

No. **0402**
DATE 17th March 2004

Main ROM, U1003 on the HR Main PCB Assy has been upgraded from V1.15 to V1.17 on the products with S/No. 0300001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
MAIN V1.17	S003653-00J	S0035153, IC,MBM29F800BA-70PF

Problem corrected by V1.17

1. Incorrect IN and OUT point

This symptom occurs only when the unit is running Auto Punch/Rehearsal mode.

A. During Rehearsal mode, unit turns to input monitor approx 30 msec earlier than IN point.
B. During Auto Punch, unit turns to Punch OUT approx 10-60 msec earlier than OUT point.

• Note for A: Recording works at IN point correctly.
• Note for B: Rehearsal works at OUT point correctly.

2. Incorrect time information of timecode output

When TC Offset is set from –5h through –12h, unit outputs “plus 1h” timecode while the tape is running at correct position.

Example:
VCR (TC master) is now at 00h00m00s00f.
On DTRS (TC slave), set TC offset to –05h00m00s00f.
Start master VCR.
DTRS (tape) runs at 19hXXmXXsXXf correctly, however, TC from TC out terminal shows 20hXXmXXsXXf.

TECHNICAL INFORMATION

TASCAM DA-78HR, ROM Upgrade (Main V1.15)

No. **0335**
DATE 09th October 2003

Main ROM, U1003 on the HR Main PCB Assy has been upgraded from V1.14 to V1.15 on the products with S/No. 0300001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
MAIN V1.15	**S003653-00H**	**S0035153**, IC,MBM29F800BA-70PF

Problem corrected by V1.15

On rare occasions, locating does not reach locate point. At this time the transport (time counter) goes back and forth around the locate point. Same thing occurs when chasing external timecode.

- This symptom occurs with only V1.14.

TECHNICAL INFORMATION

TASCAM DA-78HR, ROM Upgrade (Main V1.14)

No. **0315**
DATE 20th June 2003

Main ROM, U1003 on the HR Main PCB Assy, has been upgraded from V1.13 to V1.14 on the products of S/N 0280001 and up.

	Version	P/N (PGMed ROM)	P/N (Blank ROM)
Former	V1.13	S003653-00E	S0035153, IC, MBM29F800BA-70PF
New	**V1.14**	**S003653-00F**	

Problem Fixed

1. When Play key (DA-78HR's or remote control's) is pressed right after finishing locate, DA-78HR doesn't start to play.

2. Tape TC is not read correctly while tape runs at 20x speeds. Unit runs at 20x speed around following points.

a) Tape reaches to beginning or end in FF or REW mode.
b) Tape reaches to target point in Locate mode.

3. Setting of TC Accuracy or Input TC Timing returns to default automatically after recycling power.

   TC Accuracy: "Normal" (Default) or "Wide"
   Input TC Timing: "Analog" (Default) or "Digital"

4. When tape TC is reproduced under different setting from original recording (*), incorrect time is shown when reproducing TC around across 00h 00m 00s 00f.

* For example: Reproduce 29DF tape TC by a unit that is set to 25F.

TECHNICAL INFORMATION

TASCAM DA-78HR, ROM Upgrade (Front V1.01)

No. **0201**
DATE 1st March 2002

Front ROM, U6 on the Key PCB Assy has been upgraded from V1.00 to V1.01 on the products with S/No. 0230001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
Front V1.01	**S003568-00B**	**S0018093,** IC, M27C512-12C1

Problem Corrected by V1.01

In rare occasions, Front ROM would not receive the initialization signal coming from Main ROM resulting the unit does not boot.

TEAC **TECHNICAL INFORMATION**

TASCAM DA-78HR, Improvement of the Error Rate

No. **0122**
DATE 19th October 2001

Following changes have been made on the products with S/No. 0200001 and higher.
Change 1: Error rate for recording/playback has been improved.
Change 2: Recording current adjustment has been eliminated and become fixed value.

Change 1: Improvement of the error rate

On the Servo PCB Assy

	Old	New
C25, C26	100 pF	82 pF, P/No. 12909879
C31, C32	390 pF	330 pF, P/No. 12911095

On the HR Main PCB Assy

	Old	New
R1506, R1509	390 Ω	470 Ω, P/No. 11985916

Change 2: Eliminating the VR's for recording current adjustment

On the HR Main PCB Assy

	Old	New
R1504, R1507	1 kΩ (VR)	Removed
R1505, R1508	Vacant	0 Ω, P/No. 11986740

On the Rec Joint PCB Assy

	Old	New
R91, R92, R93, R94	120 Ω	150 Ω, P/No. R0022674

By above change, P/No. for each PCB Assy has been changed as follows:

	Old	New
HR Main PCB Assy	E950989-00B	E950989-00C
Servo PCB Assy	E950995-00B	E950995-00B (no change)
Rec Joint PCB Assy	E950996-00A	E950996-00B

* Gather PCB Assy, S DA-78HR (P/No. E950994-00C) consists of Servo PCB Assy (-00B) and Rec Joint PCB Assy (-00B).

Note:

A) To improve the error rate in the servicing level, no need to apply the change 2 above.
B) In case the HR Main PCB Assy is changed from (-00A) or (-00B) to (-00C), Rec Joint PCB Assy should absolutely be replaced with (-00B) simultaneously. Or, just replace 4 resistors on the Rec Joint PCB Assy with 150 Ω.
   * If the HR Main PCB Assy is changed from (-00A) to (-00C), see Tech-Info No. 0024R.
C) On the production, 1% resistors have been used for R1506/R1509 (HR Main PCB Assy) and R91-R94 (Rec Joint PCB Assy) to spread a safety margin but usual carbon resistors can be used as long as the recording current value satisfies the specification.

TECHNICAL INFORMATION

TASCAM DA-78HR, Low Battery

No. **0108R**
DATE 26th September 2001

This is the revised edition of Tech-Info No. 0108.
There is no change from the original No. 0108 except that:
Tokyo stock has been reworked and those units have "1F" mark stamped on the carton box.

"LoW bEry (low battery) " will be displayed earlier than expected.

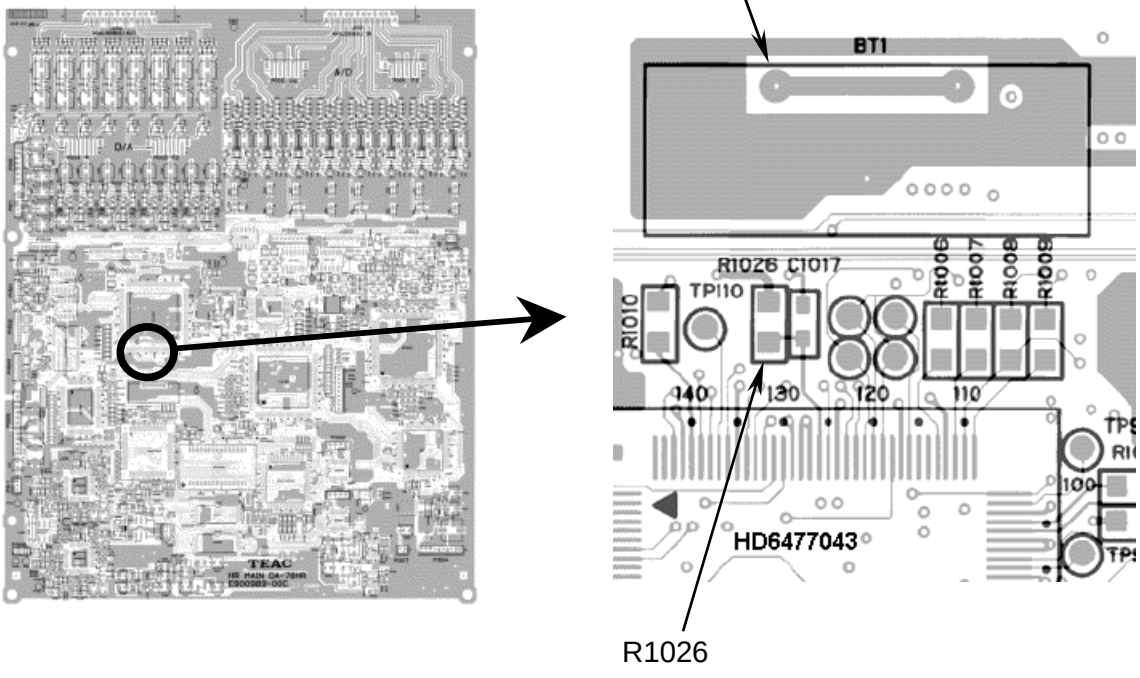
The cause is R1026 on the HR Main PCB Assy. The small resistor value can cause the battery (BT1) to drain prematurely.

To decrease the current, R1026 (100 kΩ) has been changed to 1 MΩ, **P/No. 11152105** on the products with S/No. 0230001 and higher.

After R1026 is replaced, it is suggested to also replace the battery with new one. The type of the battery is CR2032 which is a very common battery available at most electronic parts supply.

Note:
1. The battery is only being used when the unit is powered off, so the longer a DA-78HR or DA-98HR sits in a box waiting to be purchased, the shorter the life of the battery will be.
2. Even if the battery has come to its life, drum hours are not cleared as it is memorized on the Servo PCB Assy. Only standard work settings will be lost. Until the battery is replaced with new one, it is suggested to store and load settings to and from tape. Refer to the owner's manual, 7.14 Saving settings to tape and 7.15 Restoring settings from tape.

HR Main PCB Assy (top side)



TEAC TECHNICAL INFORMATION

TASCAM DA-78HR, Low Battery

No. **0108**
DATE 31st May 2001

"LoW btrY (low battery)" will be displayed earlier than expected.

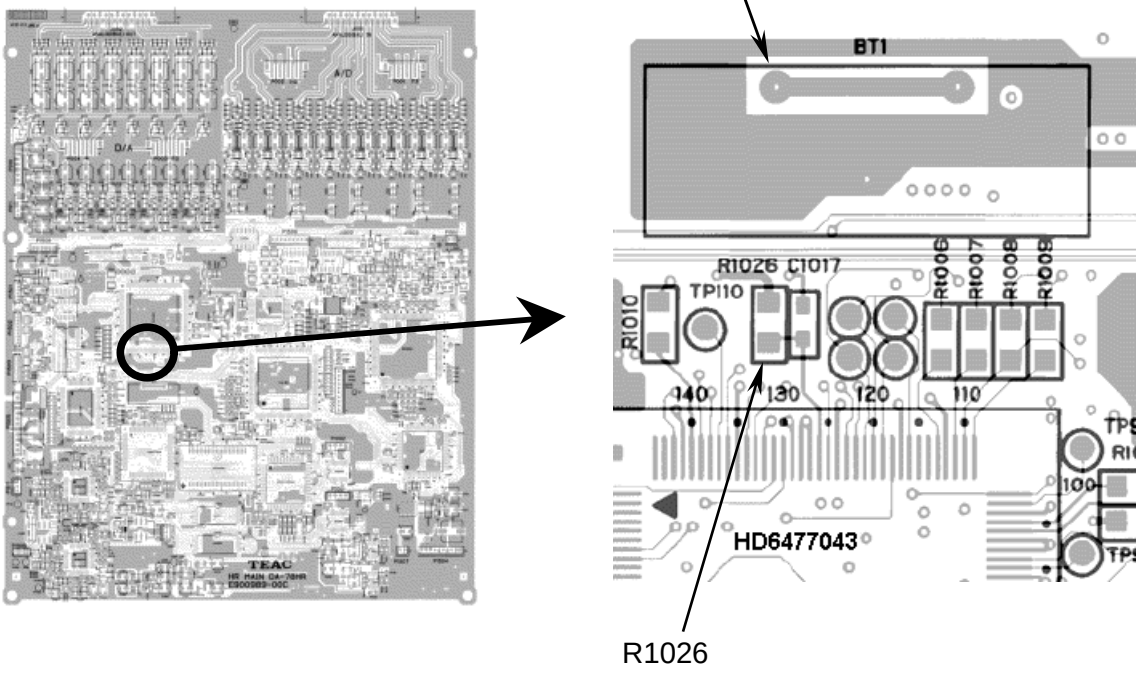
The cause is R1026 on the HR Main PCB Assy. The small resistor value can cause the battery (BT1) to drain prematurely.

To decrease the current, R1026 (100 kΩ) has been changed to 1 MΩ, **P/No. 11152105** on the products with S/No. 0230001 and higher.

After R1026 is replaced, it is suggested to also replace the battery with new one. The type of the battery is CR2032 which is a very common battery available at most electronic parts supply.

Note:
1. The battery is only being used when the unit is powered off, so the longer a DA-78HR or DA-98HR sits in a box waiting to be purchased, the shorter the life of the battery will be.
2. Even if the battery has come to its life, drum hours are not cleared as it is memorized on the Servo PCB Assy. Only standard work settings will be lost. Until the battery is replaced with new one, it is suggested to store and load settings to and from tape. Refer to the owner's manual, 7.14 Saving settings to tape and 7.15 Restoring settings from tape.

HR Main PCB Assy (top side)



TEAC

TECHNICAL INFORMATION

TASCAM DA-78HR, Supplement Service Manual

No. **0025**
DATE 22nd September 2000

Supplement service manual for the DA-78HR has been issued.
This information adds some details for each section.

4-5-5. Linearity check

- This new procedure is applicable to the unit that has the new Servo PCB Assy introduced by Tech-Info No. 0021R.
- For earlier DA-78HR's, use original procedure.
- "VTR MODE" has been supported on all DA-78HR's regardless of the firmware version.

4-5-6. Final checking of each guide

- This new procedure is applicable to all DTRS machines.
- Offers more precise check.

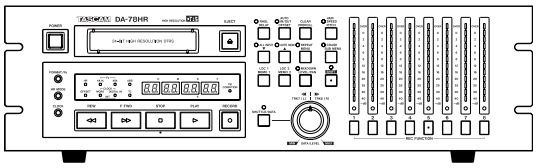
5-4-5/6/7. P.G. (Phase generator) position adjustment

- This new procedure is applicable to all DTRS machines except DA-98HR.
- Former way was to adjust 250 μs at the beginning of the RF waveform. However, there was a difficulty to define the beginning point precisely.

PCB Patterns & Parts Lists

- PCB patterns and parts lists have been updated as introduced by Tech-Info No. 0021R / 0024

TASCAM
TEAC Professional Division



SUPPLEMENT

DA-78HR

Digital Multitrack Recorder

Due to improvement of the DA-78HR, part of the description in the service manual of the DA-78HR is slightly changed. Please note that this supplement describes only changes in the service manual.

製品の改良等により、DA-78HRサービスマニュアルの内容が一部変更になっています。このサプリメントでは、サービスマニュアルの変更部分のみ記載しています。

Effective : August, 2000

S-0028

●Page 22 : The following adjustment procedure has been changed.

4-5. Adjusting the tape travel

5. Linearity check
   1) Set the unit to the VTR mode (see below).
   2) When the unit is in the VTR mode, the level fluctuates spontaneously.
      At this time, check that the shape of the waveform remains consistent while the level is changes.
      If it doesn't, fine-adjust the guide rollers located at the entrance and exit of the drum.
      If the level stops varying, set the unit to the track-off mode so that the level continues to vary. (see below.)

(How to Set the Track-Off Mode)
① Set the unit to the VTR mode.
② Check to see that the VARI SPEED key is not pressed on, then press on the SHIFT key.
③ Press the VARI SPEED key to enter the Track-Off mode.
④ Using the ▼ and ▲ keys, change the pitch display within the limits of from -0.5% to 0.5%.

(How to Set the VTR mode)
① Turn power on while pressing and holding the F FWD + STOP + PLAY keys simultaneously.
The display shows a countdown from 3 → 2 → 1.
② In the period between the start of the countdown to the disappearance of "1", release the keys and press only the PLAY key. (The display shows "VTR MODE".)
③ The VTR mode is released when power is turned off.

●Page 23 : The underlined section has been added.

4-5. Adjusting the tape travel

6. Final checking of each guide
   3) Confirm the lower edge travel regulation for the capstan guide.
   Note) Play an ME tape and make adjustments as described in item 3 on page 22, then check again.

●22ページ　下記の調整方法が変更になりました。

4-5. テープ走行調整

5. 直線性の確認
   1）VTRモードにする。（下記参照）
   2）VTRモードにすると、レベルがかってに大きくなったり小さくなったりします。このときの波形が形を変えずにレベルだけが大小することを確認する。そうでない場合は、ドラム入口、出口の回転ガイドを微調整する。
   もし、レベルが大小を繰り返さないようならば、次の方法でトラックオフさせるとレベルが変化するようになります。

（トラックオフのさせ方）
① VTRモードにする。
② VARI SPEEDキーがOFFであることを確認して、SHIFTキーをONにする。
③ VARI SPEEDキーを押して、Track offモードにする。
④ ▼キーまたは▲キーにより、ピッチ表示を－0.5%～0.5%の範囲で変化させる。

（VTRモードの起動方法）
① F FWDキー＋STOPキー＋PLAYキーを押しながら電源をONにする。
このとき、表示部に 3→2→1というカウントダウンが表示される。
② カウントダウンが始まってから“1”が消えるまでの間に、一旦キーから手を離してからPLAYキーを押す。（VTR MODEと表示）
③ 電源をOFFにすると、VTRモードは解除される。

●23ページ　下線部が追加になりました。

4-5. テープ走行調整

6. 各ガイドの最終チェック
   3）キャプスタン部ガイドの下エッジ走行規制を確認する。
   注）MEテープを走行させ、22ページの3項の調整を再度行って確認をする。

●Page 27 : The underlined section has been changed.

5-4. P.G. (Phase generator) position adjustment

5. Enter the play mode and, using the ▲ and ▼ keys, adjust the lag between the fall of the switching pulse and the begining of the SUB DATA area for 821 µsec, as shown in Fig. 5-2.
6. Press STOP, then switch power off to save the setting.
7. Switch on power again, then enter the play mode to check that the lag of 821 µsec is maintained.

●27ページ　下線部が変更になりました。

5-4. PG（Phase Generator）走行調整

5. PLAYモードにして、スイッチングパルスの立ち下がりからSUB DATAエリアの始まりまでが 821 μ secになるように、▲または▼キーを押して調整する。（図5-2参照）
6. STOP後、一度電源をOFFして値を記憶させる。
7. 再度電源をONにし、PLAYモードにして 821 μ secが変化していないことを確認する。

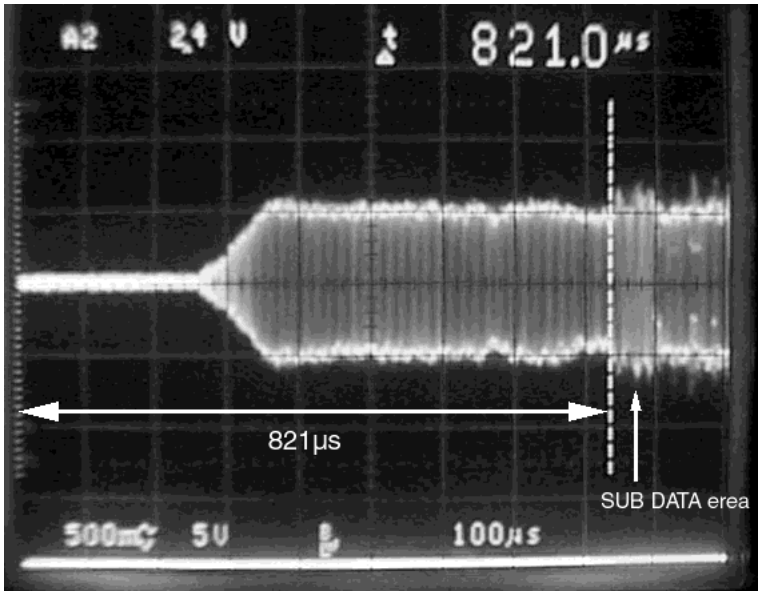


Fig. 5-2

EXPLODED VIEW-3 (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
3- 3	*M00921001A	DRUM ASSY,HR01

SERVO PCB ASSY (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
	*E95099500B	PCB ASSY,SERVO
	*E90099500B	PCB,SERVO
	*M00456800A	SHIELD PLATE,RF
D400	5224019200	D,EC10QS04TE12L
D500	5224019200	D,EC10QS04TE12L
D600	5224019200	D,EC10QS04TE12L
D701	S0021554	DIODE,RB070L-40TE25
D902	13411651	DIODE,DAN202K(SMT)
D904	13411651	DIODE,DAN202K(SMT)
L2-6	14728209	COIL,CHIP 47UH
L101,102	E0022854	COIL,CHIP 100UF
L200	E0022854	COIL,CHIP 100UF
L400	14728449	COIL,390UH 10%
L500	14728449	COIL,390UH 10%
L600	14728444	COIL,150UH 10%
L901	E0022854	COIL,CHIP 100UF
P1	5336379600	CONNECTOR,8P 52271-0890
P2	5336287200	PLUG,CONN. S2B-PH-K-S(WHT)
P3	13124438	CONNECTOR,ZH S 5B-ZR
P901	13153693	CONNECTOR,52271-1590
P902	13153479	CONNECTOR,15P
P903	5336379500	CONNECTOR,7P 52271-0790
P904,905	13153693	CONNECTOR,52271-1590
P906	13124443	CONNECTOR,ZH S10B-ZR
P907	13124025	CONNECTOR,ZN S 8B-ZR
P908	13124021	CONNECTOR,ZN S 4B-ZR
P909	5336287400	PLUG,CONN. S4B-PH-K-S(WHT)
P910,911	13124435	CONNECTOR,ZH S 2B-ZR
Q1,Q2	13427337	TR,2SC2412K
Q3-Q7	S0020404	TR,DTC124EEATL
Q102,Q103	S0000674	TR,DTC123JUA
Q104,Q105	S0019894	TR,DTA114EUA-T106
Q400	5230020200	TR,2SA1314B-TE12L,C
Q500	5230020200	TR,2SA1314B-TE12L,C
Q600	5230020200	TR,2SA1314B-TE12L,C
Q902,903	13427337	TR,2SC2412K
R51-54	R0016700	VAR RES,2.2KB RH0422C
U1,U2	5220449300	IC,HA12133MP
U3	13448164	IC,CXA1077M-T4
U4	S0020414	IC,NJM2233BV-TE1

SERVO PCB ASSY (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
U100	S00381800A	IC,ATF-CTRL
U101	S0038383	IC,CXA1814N
U102	S0020414	IC,NJM2233BV-TE1
U103	S0020414	IC,NJM2233BV-TE1
U104	S0001204	IC,TC4W53FU-TE12L
U105	S0038394	IC NJM2119M
U201	5220448800	IC,LB8110M
U401	5220448900	IC,LB1851M
U501	5220448900	IC,LB1851M
U601	5220448900	IC,LB1851M
U602	5220450800	IC,TL5001CPS-T
U701	5220449000	IC,LB1836M
U901	S00218100A	IC,UPD78146GF-024-3BA
U902	S0033274	IC,SN74LV00APW
U903	S0020454	IC,SN74LV14PW
U904	S0033414	IC,M93C46-MN6T
U905	S0034654	IC,TC7S08FU

D-SUB PCB ASSY (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
	*E95099200C	PCB ASSY,D-SUB
	*E90099200C	PCB,D-SUB
D201	5224015020	DIODE,1SS133T-77 FT
D202	S0038591	DIODE,1GWJ42
J201	E0032220	CONNECTOR,DSUB 25PIN
J202,203	E0046180	JACK,YKC21-3627
J204,205	E0032210	CONNECTOR,DSUB 15PIN
J206	E0019330	CONNECTOR,26FMZ-ST
J207	E0019300	CONNECTOR,16FMZ-ST
P201	5336287600	PLUG,CONN. S6B-PH-K-S(WHT)
Q201	5232255920	TR,DTC143XSA
U201-202	S0026730	IC,M5M34051P
U203	13203497	RELAY,5V (G5A-237P,5V)

RCA PCB ASSY (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
	*E95099100C	PCB ASSY,RCA
	*E90099100C	PCB,RCA
J1-4	E0056130	JACK,YKC21-4141
J5-8	E0056130	JACK,YKC21-4141
L011-018	5347027620	FERRITE BEADS,FBR07HA850
L021-028	5347027620	FERRITE BEADS,FBR07HA850
P101,102	5336244600	PLUG,CONN. S16B-PH-K-S

BNC PCB ASSY (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
	*E95099300C	PCB ASSY,BNC
	*E90099300C	PCB,BNC
	*5780003006	SCREW,BIND M3X6
D010,020	5224017120	DIODE,1SR139-200 T-31
J301-J303	E0022450	CONNECTOR,DIN5 YKF51-5040
J304	5334081000	SOCKET,CONN.DIN8P YKF51-5014
J305	5330014800	JACK,1P YKB21-5014
J306	E0033070	JACK,P2286-A BNC3P(1SW)
J307	E0056130	JACK,YKC21-4141
J308	E0019310	CONNECTOR,20FMZ-ST
P301	5336249200	PLUG,CONN. B02B-PH-K-S(WHT)
P302	5336249500	OLUG,CONN. B05B-PH-K-S(WHT)
U010	13447952	IC,NJM7805FA
U010A	M00922900A	HEATSINK,REG
U020	13447952	IC,NJM7805FA

HR MAIN PCB ASSY (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
	*E95098900B	PCB ASSY,HR MAIN
	*E90098900C	PCB,HR-MAIN
	*M00473900A	SPACER,IOX
	*5780002606	SCREW,BIND M2.6X6
	*M01120800A	HEATSINK,SX
	*M01120900B	TORSION SPRING,SX
	*13152094	CONNECTOR,4P(EHR-4)
BT1	E0055380	BATTERY,CR2032
BT1A	E0055390	HOLDER,BCR20V4
D011-018	13411644	DIODE,CHIP 1SS355 TE-17
D021-028	13411644	DIODE,CHIP 1SS355 TE-17
D031-038	13411644	DIODE,CHIP 1SS355 TE-17
D041-048	13411644	DIODE,CHIP 1SS355 TE-17
D1001	S0035734	DIODE,1SS377(TE85L)
D1002,1003	S0022094	DIODE,1SS355
D1004,1005	13411667	DIODE,HRF22
D1201	13411667	DIODE,HRF22
D1202,1203	S0035214	DIODE,HVC376B-TRF
D1204	13411667	DIODE,HRF22
D1205	5228018100	C,VARI HVU17TR
D1352	S0023224	DIODE,DAN217 T146
D1401	5228018100	C,VARI HVU17TR
D1501	S0023224	DIODE,DAN217 T146
D1502,1503	13411596	DIODE,IMN10
D1504	S0025274	DIODE,RB706F-40
D1505-1516	13411596	DIODE,IMN10
D1517-1519	S0025274	DIODE,RB706F-40
D1520-1527	13411596	DIODE IMN10
D1528	S0023224	DIODE,DAN217 T146
J001,002	5334080000	SOCKET,CONN. 25P DSUB

HR MAIN PCB ASSY (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
J1501	E0032464	CONNECTOR,FMN 26BMT
J1502	E0032364	CONNECTOR,FMN 16BMT
J1503	E0032404	CONNECTOR,FMN 20BMT
L010	E0054724	COIL,LQH3C100K24
L011-018	E0054804	BEAD COIL,BLM21B121SDPT
L020	E0054724	COIL,LQH3C100K24
L021-028	E0054804	BEAD COIL,BLM21B121SDPT
L030	E0054724	COIL,LQH3C100K24
L031-038	E0054804	BEAD COIL,BLM21B121SDPT
L041-048	E0054804	BEAD COIL,BLM21B121SDPT
L501-504	E0054724	COIL,LQH3C100K24
L1201-1204	14728209	COIL,CHIP 47UH
L1205,1206	5286051500	COIL,CHIP 2.7UH K LK2125
L1207	5286051300	COIL,CHIP 2.2UH K LK2125
L1401	14728209	COIL,CHIP 47UH
L1402	5286051900	COIL,CHIP 3.9UH K LK2125
L1403,1404	E0022704	BEAD COIL,BK2125HS
L1501,1502	E0055364	COIL,CHIP 1000UH 5%
L1503	E0031304	BEAD COIL,BLM21A601S
P001-004	E0016854	CONNECTOR,B08B-PH-SM3
P010	5336303700	PLUG,CONN. B7B-EH(WHT)
P011	5336249500	PLUG,CONN. B05B-PH-K-S(WHT)
P1001,1002	5336303400	PLUG,CONN. B4B-EH(WHT)
P1301	5336249300	PLUG,CONN. B03B-PH-K-S(WHT)
P1501	5334083300	PLUG,CONN. B06B-ZR(WHT)
P1502	13124432	CONNECTOR,ZH B 10B-ZR
P1503	5334083500	PLUG,CONN. B08B-ZR ｼﾛ
P1504	5336250000	PLUG,CONN. B10B-PH-K-S(WHT)
P1505	5336304100	PLUG,CONN. B11B-EH(WHT)
P1506	13124427	CONNECTOR ZH B 5B-ZR
P1508	5336249600	PLUG,CONN. B06B-PH-K-S(WHT)
P1509	5336249900	PLUG,CONN. B09B-PH-K-S(WHT)
P1510	5336249200	PLUG,CONN. B02B-PH-K-S(WHT)
Q001	13428276	TR,DTA114EKAT-146
Q002	13428286	TR,DTC114EKAT-146
Q011-018	S0016434	TR,2SD1328T/S
Q1309-1312	13428287	TR,DTC124EKAT-146
Q1352	S0019224	TR,DTC143XUA T106
Q1501	S0019224	TR,DTC143XUA T106
Q1502,1503	13428287	TR,DTC124EKAT-146
R1014	R0067224	RES ARRAY,1/16W 4X4.7K J
R1349-1352	R0066374	VAR RES,EVM3VSX50B54
R1401,1402	R0092704	RES ARRAY,1/16W 4X47 J
R1403	R0067304	RES ARRAY,1/16W 4X10K J
R1404	R0092704	RES ARRAY,1/16W 4X47 J
R1504	R0092754	VAR RES,1KB RH03ADC
R1507	R0092754	VAR RES,1KB RH03ADC
R1515-1518	R0092704	RES ARRAY,1/16W 4X47 J
R1538,1539	R0092714	RES ARRAY,1/16W 4X2.2K J
R1540,1541	R0067224	RES ARRAY,1/16W 4X4.7K J

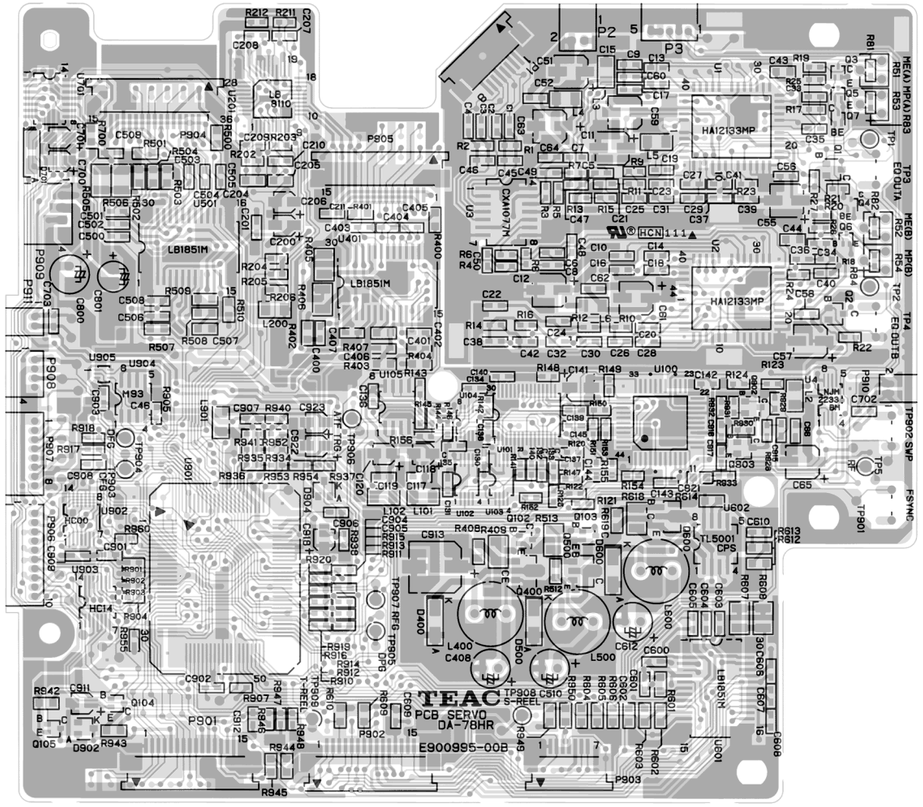
HR MAIN PCB ASSY (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
R1542-1545	R0092704	RES ARRAY,1/16W 4X47 J
R1547	R0067304	RES ARRAY,1/16W 4x10K J
R1548	R0092704	RES ARRAY,1/16W 4X47 J
R1551	R0092704	RES ARRAY,1/16W 4X47 J
R1591	R0067304	RES ARRAY,1/16W 4X10K J
R1592,1593	R0092704	RES ARRAY,1/16W 4X47 J
R1597	R0067304	RES ARRAY,1/16W 4X10K J
S1001	E0031064	SW,SLIDE SW CHS-02TA
U011-018	5220450400	IC,NJM5532M-T2
U021-028	5220450400	IC,NJM5532M-T2
U031-038	5220450400	IC,NJM5532M-T2
U501-504	S0035224	IC,AK5383
U511-514	S0035234	IC,AK4393
U521-524	5220450400	IC,NJM5532M-T2
U1001	S0035133	IC,HD6437043AE00F
U1002	S0035143	IC,XCS10-3TQ144C
U1003	S00365300D	IC,MAIN V1.08 MBM29F800BA-70PF
U1003A	E0033093	SOCKET,44PIN SOP IC179
U1004-1005	S0037443	IC,BS62LV1024TC-70
U1006	S00351700D	IC,SX28AC/SS TC
U1007	S0024464	IC,M62001FP-600D
U1009	S0018944	IC,TC74VHCU04F(EL)
U1010	S0024314	IC,TC74VHCT00F(EL)
U1011	S0025594	IC,TC74VHC163FEL
U1012	5220118000	IC,TC74HC32AF-TP2
U1013	13444685	IC,74HC 574F
U1014	5220103800	IC,TC74HC157AF-TP2
U1015	S00177600A	IC,CLK1
U1016	S00190600A	IC,IOX
U1016A	M00473600A	HEATSINK,IOX
U1017	S0024353	IC,DSP TMS57070FFT
U1018	E0013344	CRYSTAL OSC,22.5792MHZ
U1019	E00546900A	CRYSTAL OSC,49.152MHZ
U1020	S0020334	IC,TC74VHC04
U1021	S0036203	IC,T2316162A-45S
U1022,1023	5220104000	IC,TC74HC595AF-TP2
U1024	5220118000	IC,TC74HC32AF-TP2
U1025	S00335500A	IC,DTRS-HR ENC
U1026	S00335600A	IC,DTRS-HR DEC
U1027-1028	S0035204	IC,71V124SA15PH-T&R
U1029-1031	S0035204	IC,71V124SA15PH-T&R
U1032,1033	S0025614	IC,TC74VHCT541AFEL
U1034	S0035714	IC,BA033FP
U1035	S00351800D	IC,SX28AC/SS UART
U1036	S0020354	IC,TC74VHC74
U1037	S0035714	IC,BA033FP
U1038	S0020344	IC,TC74VHC541
U1201	13447922	IC,NJM78L05UA-TE1
U1202	5220123500	IC,MC74HC4046AF-FR1

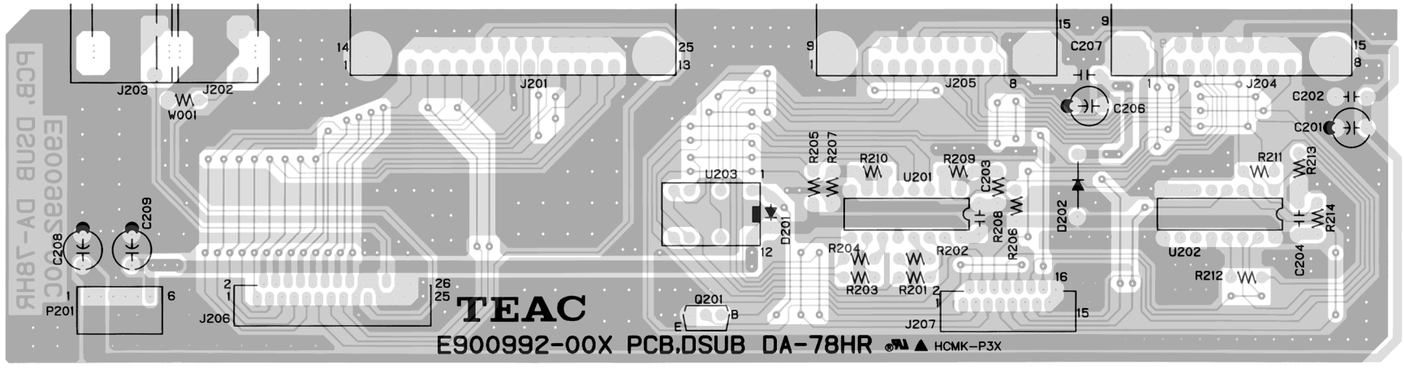
HR MAIN PCB ASSY (NEW)

REF.NO.	PARTS NO.	DESCRIPTION
U1203	S0018944	IC,TC74VHCU04F(EL)
U1205	5220123500	IC,MC74HC4046AF-FR1
U1206	S0018944	IC,TC74VHCU04F(EL)
U1207	S0029674	IC,TLC2932IPWR
U1208	S0020354	IC,TC74VHC74
U1209	S0018944	IC,TC74VHCU04F(EL)
U1210	S0029674	IC,TLC2932IPWR
U1211	13447922	IC,NJM78L05UA-TE1
U1212	S0020354	IC,TC74VHC74
U1301	S0035274	IC,MAX913CSA
U1302	S0035274	IC,MAX913CSA
U1303,1304	5220101800	IC,HD49229
U1305,1306	5292811400	EMI FILTER,CHIP 10000PFT
U1312	5292811400	EMI FILTER,CHIP 10000PFT
U1353	S0024314	IC,TC74VHCT00F(EL)
U1354	E0042034	RELAY,ATX206SA 2C,SMT
U1401	S0020344	IC,TC74VHC541
U1402	5220115600	IC,M51581FP
U1403,1404	S0018944	IC,TC74VHCU04F(EL)
U1407	13447922	IC NJM78L05UA-TE1
U1501	S0020334	IC,TC74VHC04
U1502,1503	S0020344	IC,TC74VHC541
U1504	S0024314	IC,TC74VHCT00F(EL)
U1505	S0025614	IC,TC74VHCT541AFEL
U1506,1507	S0020344	IC,TC74VHC541
U1508	5220116700	IC,HD74HC240FP
U1509	5220103800	IC,TC74HC157AF-TP2
U1510	5220115800	IC,MC74HC14AF
U1511	S0025614	IC,TC74VHCT541AFEL
U1512	5220115800	IC,MC74HC14AF
U1513-1515	5292811200	EMI FILTER,CHIP 1000PFT
U1516	S0024184	PHOTO COUPLER,PC400
U1517	S0024314	IC,TC74VHCT00F(EL)
U1518	S0023994	IC,NJM4565M-T1
U1519	5220102000	IC,SN74S140NS
U1520	S0023994	IC,NJM4565M-T1
U1521	S0024314	IC,TC74VHCT00F(EL)
U1522	S0018944	IC,TC74VHCU04F(EL)
U1524	S0025614	IC,TC74VHCT541AFEL
U1854	S0020344	IC,TC74VHC541
X1001	E00547000A	RESONATOR,SD3 32MHZ

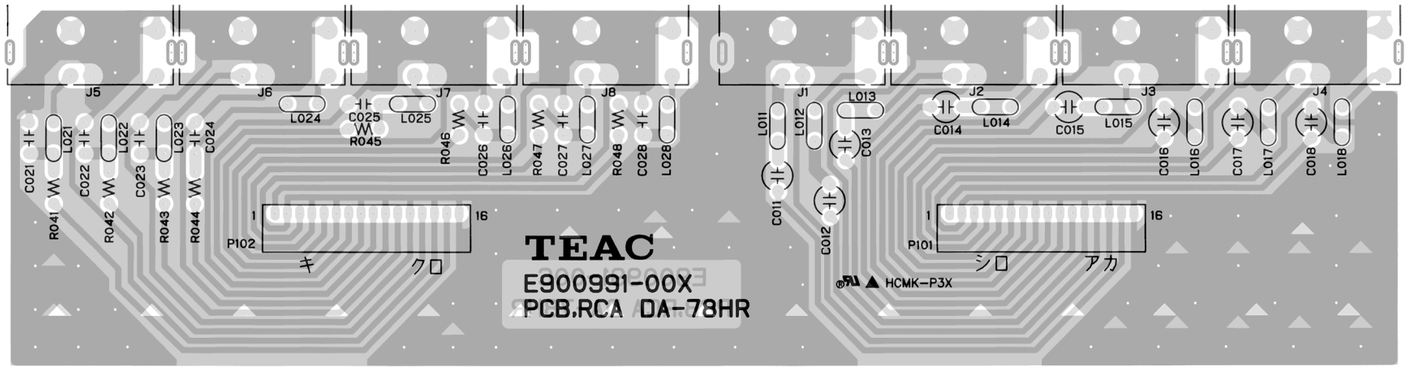
SERVO PCB (NEW)



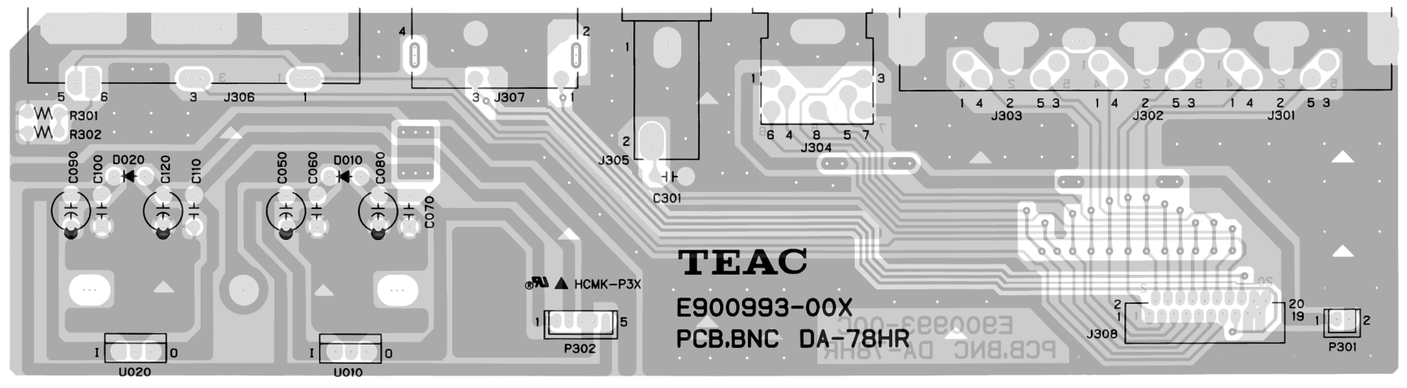
DSUB PCB (NEW)



RCA PCB (NEW)

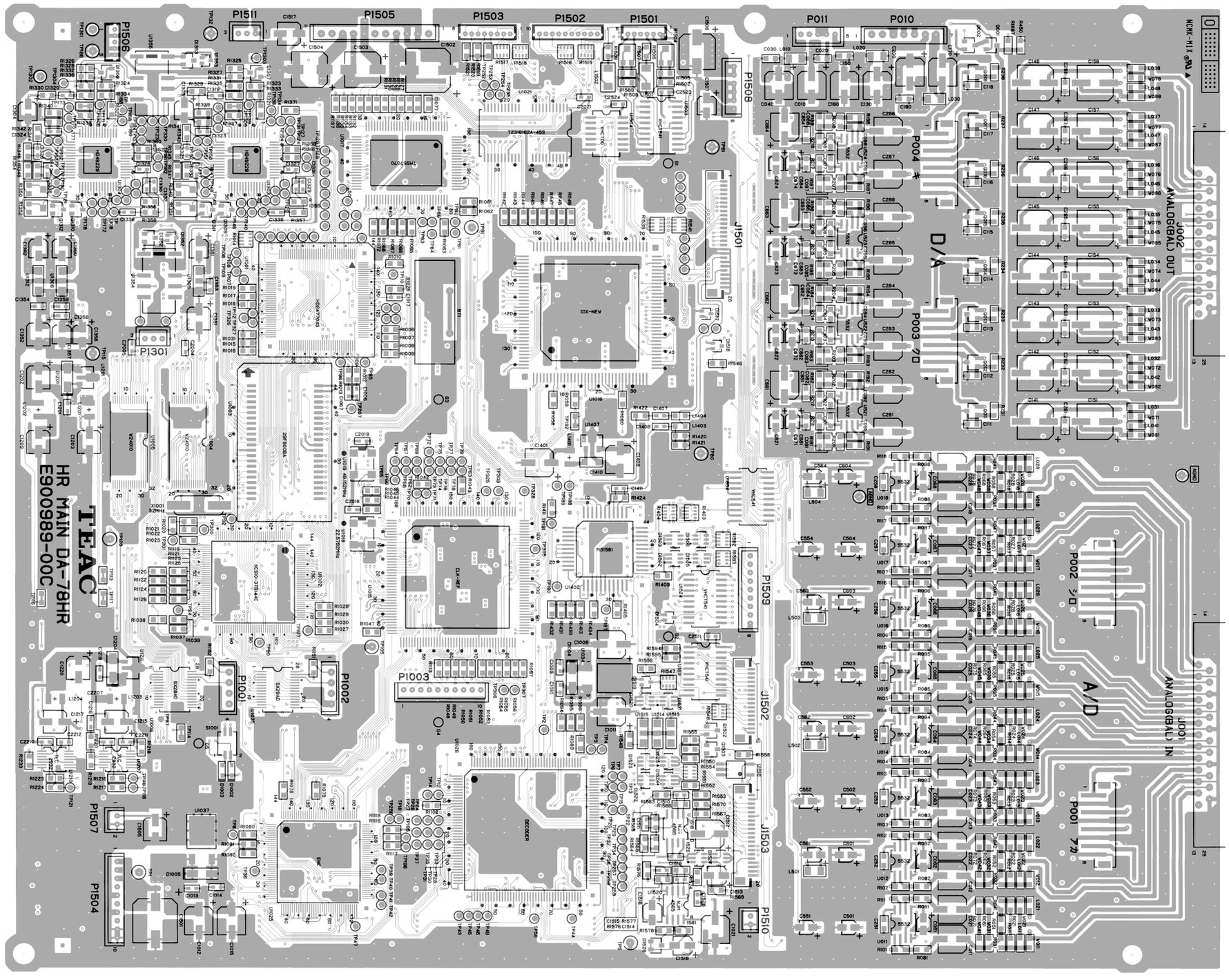


BNC PCB (NEW)



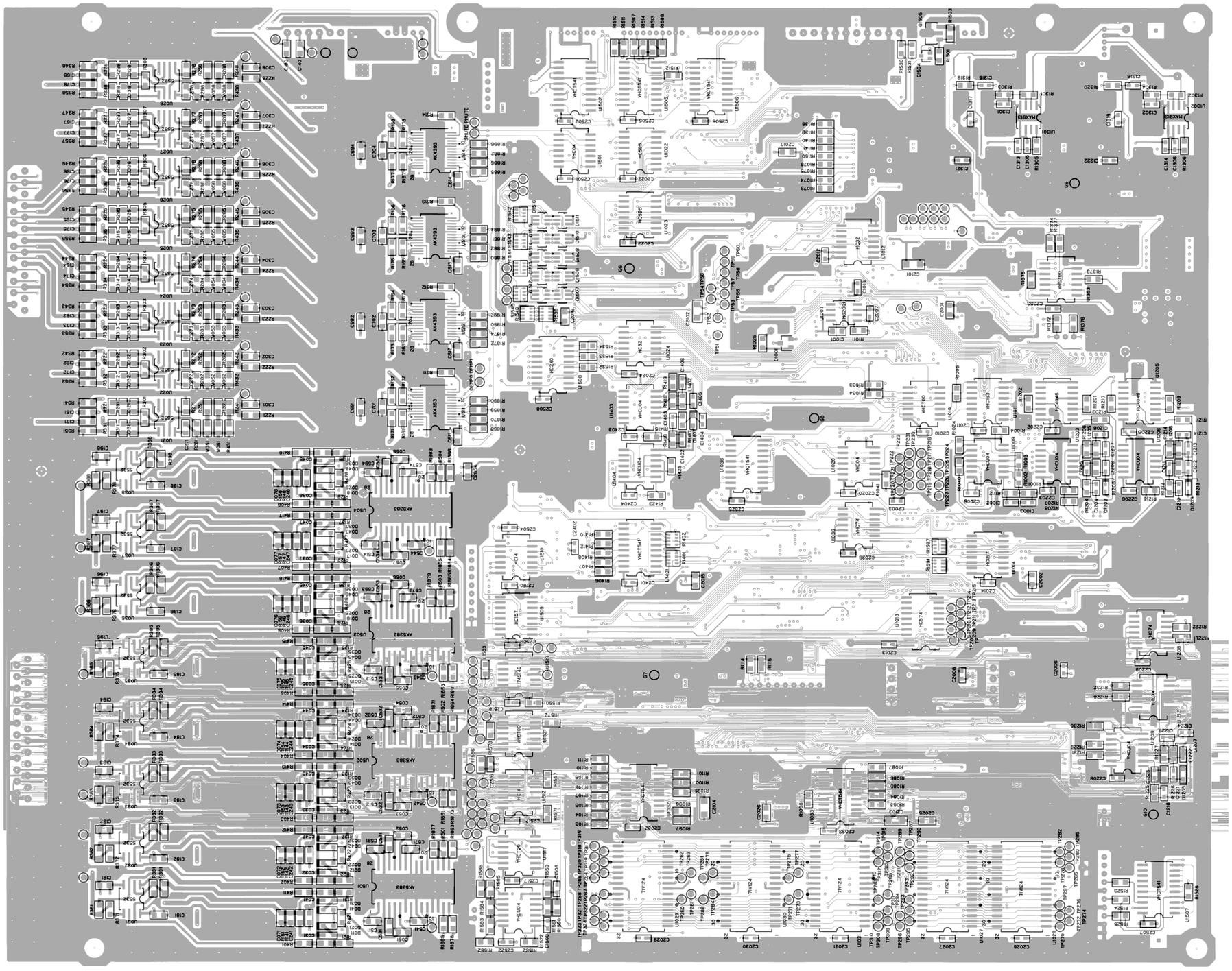
HR MAIN PCB (NEW)

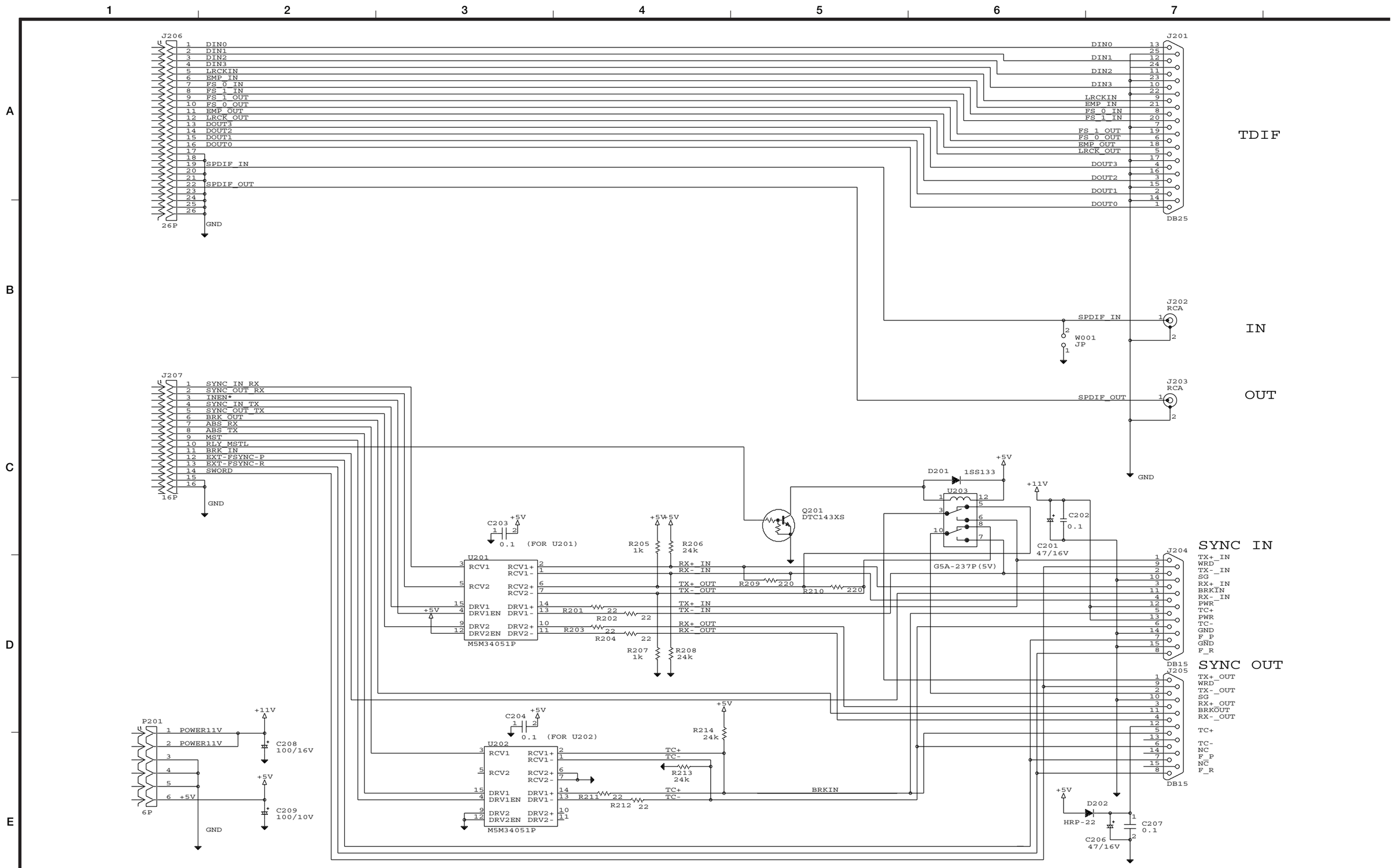
SIDE A



HR MAIN PCB (NEW)

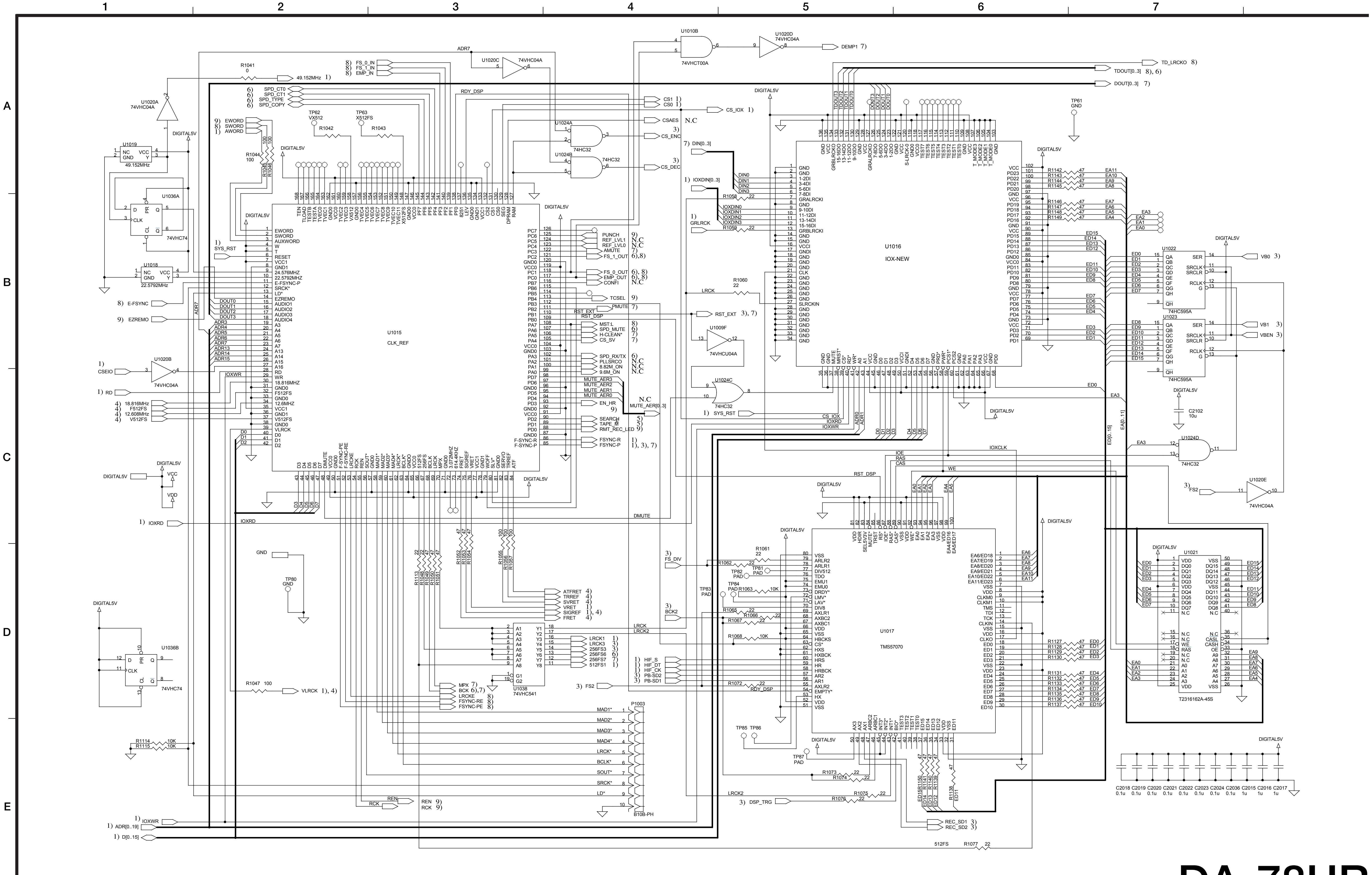
SIDE B





Digital Multitrack Recorder DA-78HR

2 nd Issue; August 2000


U1015
CLK_REF
U1016
IOX-NEW
U1017
TMS57070
U1021
T2316162A-45S
U1022
74HC595A
U1023
74HC595A
U1038
74VHC541
U1019
49.152MHz
U1018
22.5792MHz
U1036A
74VHC74
U1036B
74VHC74
U1010B
74VHCT00A
U1020D
74VHC04A
U1024A
74HC32
U1024B
74HC32
U1024C
74HC32
U1024D
74HC32
U1009F
74VHCU04A
U1020A
74VHC04A
U1020B
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U1020C
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U1020E
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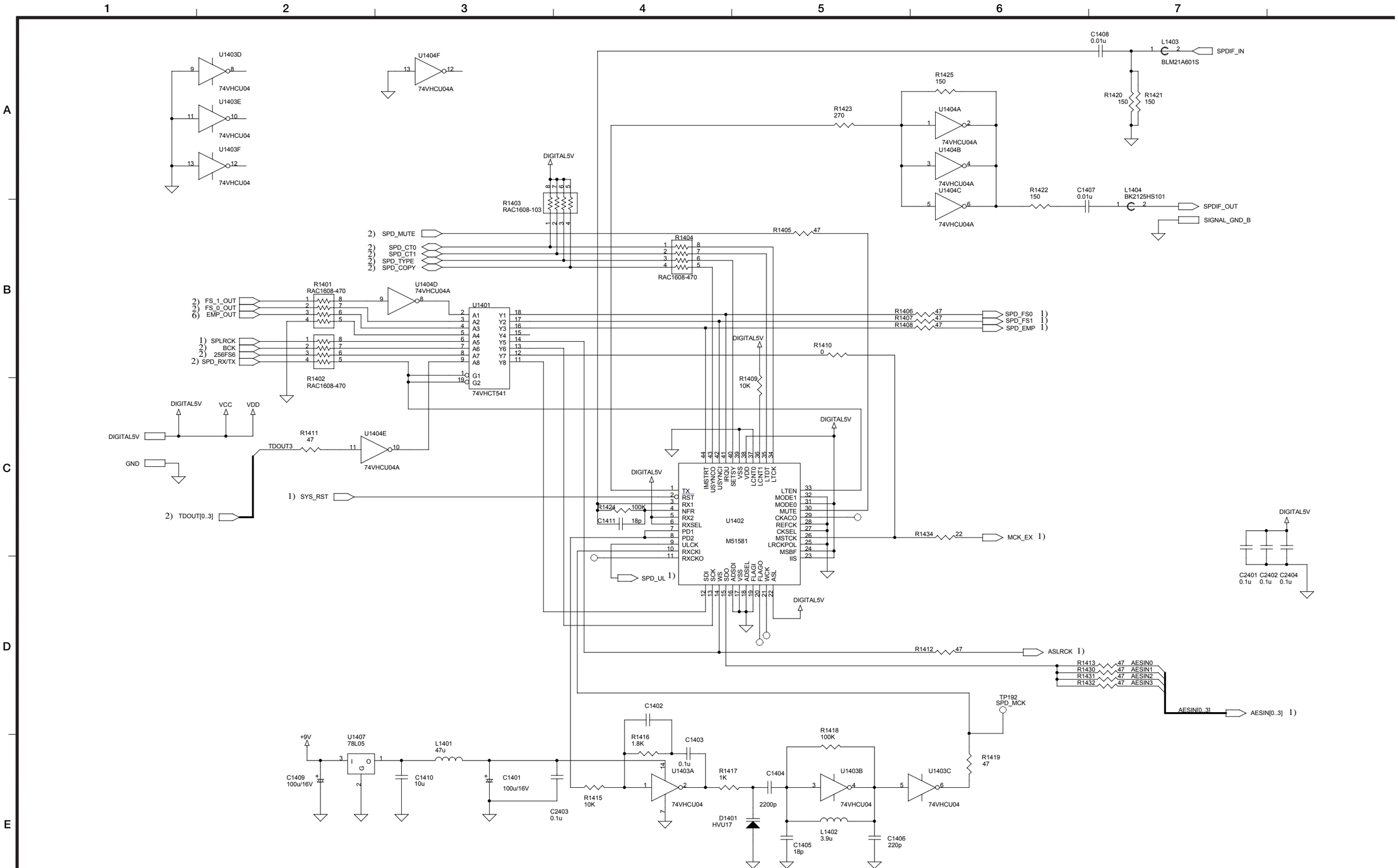
P1003
B10B-PH



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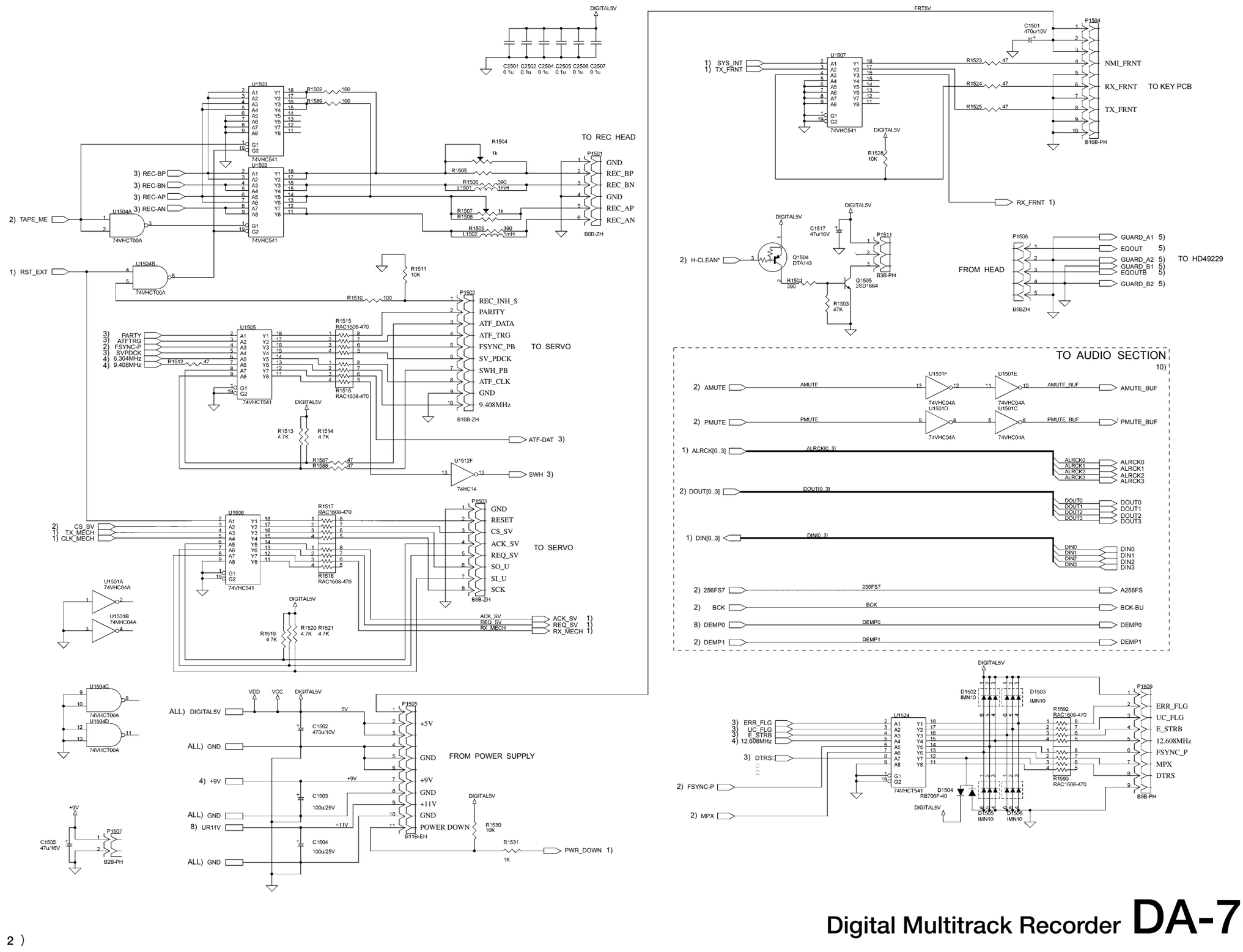

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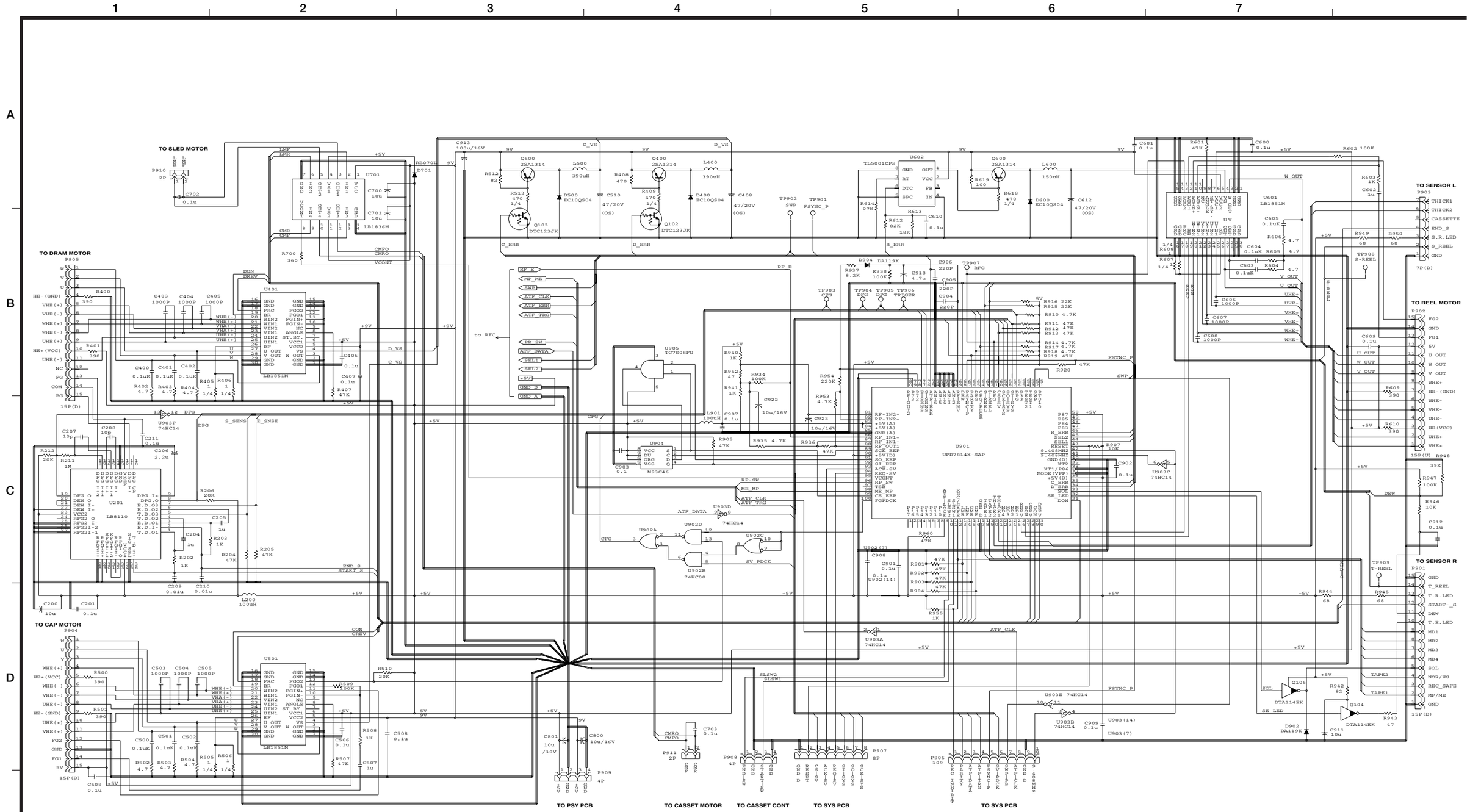
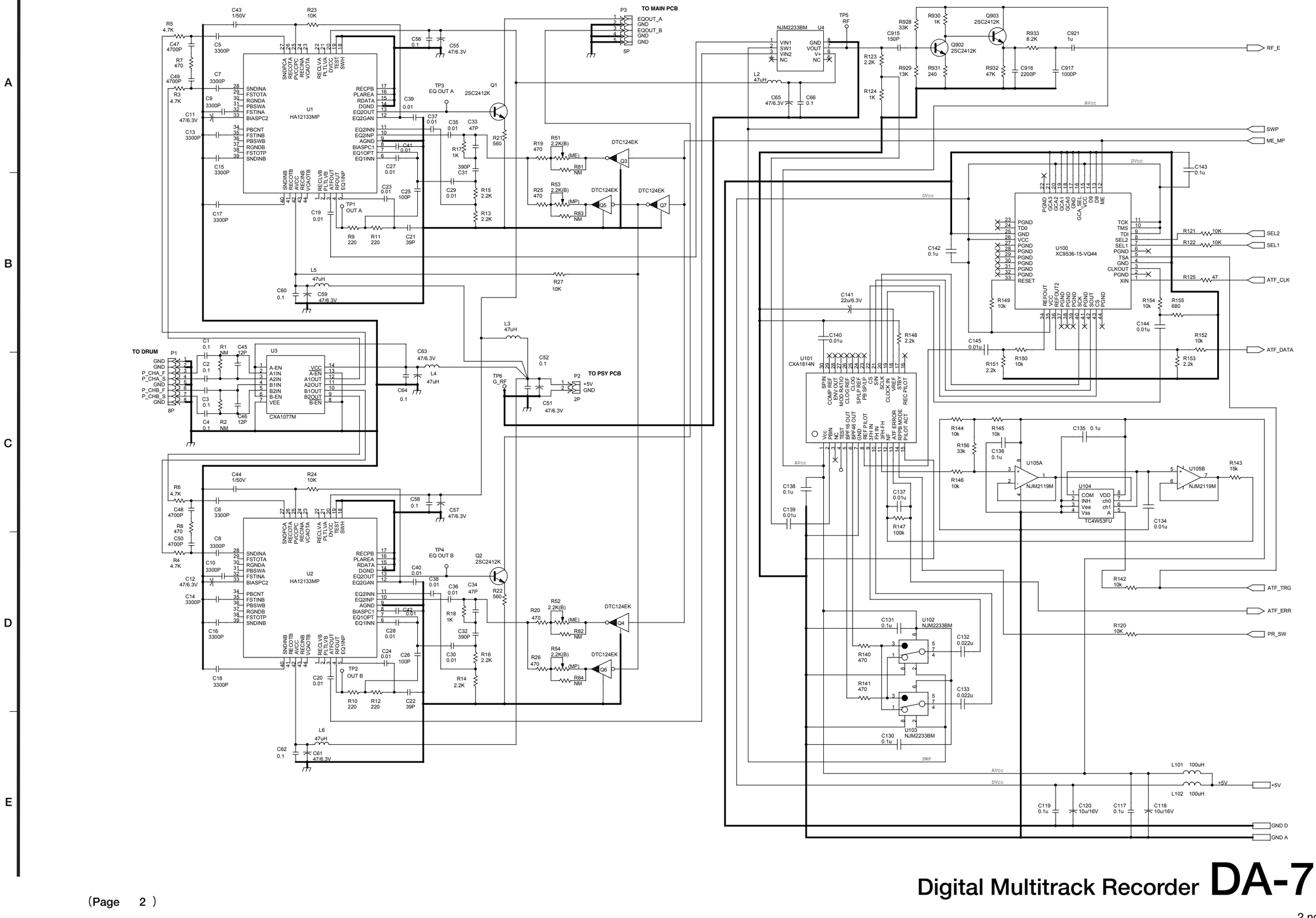
SCHEMATIC DIAGRAM DA-78HR SERVO PCB (1/2)



Digital Multitrack Recorder **DA-78HR**

2 nd Issue; July 2000

SCHEMATIC DIAGRAM DA-78HR SERVO PCB (2/2)



Digital Multitrack Recorder DA-78HR

2 nd Issue; July 2000

TEAC **TECHNICAL INFORMATION**

TASCAM DA-78HR, ROM Upgrade (Main V1.13)

No. **0030**
DATE 19th December 2000

Main ROM, U1003 on the HR Main PCB Assy has been upgraded from V1.08 to V1.13 on the products with S/No. 0190001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
Main V1.13	**S003653-00E**	**S0035153**, IC, MBM29F800BA-70PF

Refer to V 1.13 supplemental owner's manual for newly added features.

Problems corrected by V1.13

1. DTRS master unit always chases SMPTE timecode regardless of time mode. However, time mode should be set to TC when "TC offset" is displayed or edited.
2. There is a little possibility that RC-828 and RC-898 freeze.
3. With the DTRS slave units, LOCATE→PLAY does not work.
4. When saving settings to tape, if REC function keys or TC REC are set ON, recording on those tracks are also performed falsely.
5. Problem on TDIF E bit. Refer to below.

Introduction of TDIF E bit

DA-98HR can record and playback at 2X and 4X sampling frequencies: 88.2 kHz and 176.4 kHz, and 96 kHz and 192 kHz. To declare those track Fs information through TDIF, two bits (originally reserved) are newly defined. These bits are named "E bit".

With Main V1.13, DA-78HR becomes to recognize E bit. In case Fs track information other than "1X Fs/8 track" is received, following message will be displayed.

E. dio

Problem

However, there are some machines in the market that send wrong information in E bit such as DA-88 and YAMAHA O2R. If these machines are connected, the DA-78HR shows "E. dio" message even if the Fs on both are the same.

Solution

With the DA-78HR Main V1.13, new menu has been added. Refer to the supplemental owner's manual for V1.13 for more details.

menu group	Audio 1	
submenu	tdiF.E.	
parameter	0 (default)	DA-78HR looks at E bit
	1	DA-78HR ignores E bit

Notice: As mentioned in the supplemental owner's manual, if tdiF.E. is set "1", DA-78HR can record the TDIF signal that does not suit to the setting of the tape loaded. Take very care of that and warn customers.

TECHNICAL INFORMATION

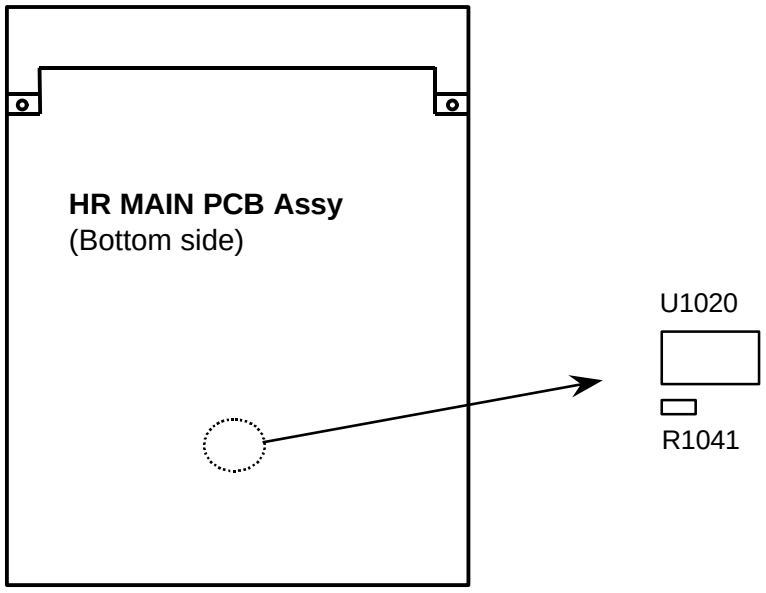
TASCAM DA-78HR, Freeze

No. **0028**
DATE 07th November 2000

Symptom: DA-78HR may freeze after long hours of use or used under high temperature.
Cause: Operation speed of TC74VHC04 (U1020 on the HR Main PCB Assy) becomes insufficient in case IC batch tolerance and ambient temperature are met at the worst state.
Solution: Replace U1020 with HD74LVC04FP. And replace R1041 (0 Ω) with 22 Ω.

This change has been made on the products with S/No. 0160001 and higher.

	Original	New
U1020	TC74VHC04	**P/No. S0037324**, HD74LVC04FP
R1041	0 Ω	**P/No. 11152220**, 22 Ω 1/10W



TEAC **TECHNICAL INFORMATION**

TASCAM DA-78HR, Change of HR MAIN PCB Assy

No. **0024R**
DATE 18th October 2000

This is the revised edition of Tech-Info No. 0024.

HR Main PCB Assy has been changed for following purposes.

1. Incorporating hardware changes made in the past. (Tech-Info No. 0002/0003/0004/005)
2. Change of foil pattern to reinforce the GND line.

Addition
Item 2 above relates to Tech-Info No. 0023 (TC out interruption). Usually, that problem can be solved by Tech-Info No. 0023. However, there may be a possibility that Tech-Info No. 0023 may not be sufficient with the products that have a powerful WORD driving circuit. Therefore GND on HR Main, BNC and D-SUB PCB Assy has been reinforced simultaneously.

	Original P/No.	New P/No.
HR Main PCB Assy (Ref 1-9)	E950989-00A	E950989-00B
BNC PCB Assy (Ref 1-4)	E950993-00A	E950993-00C
D-SUB PCB Assy (Ref 1-5)	E950992-00A	E950992-00C

All 3 PCB Assy's have been changed on the products with S/No. 0170001 and higher.

Notice:
1. Basically above 3 PCB Assy's should be combined in one unit.
~~2. Spares stock for original PCB Assy (-00A) will be maintained.~~
3. BNC PCB Assy (-00A) and (-00C) are interchangeable. However, GND reinforcement will not be effective if BNC PCB Assy (-00C) is mounted on the HR Main PCB Assy (-00A)
4. D-SUB PCB Assy (-00C) can be mounted on HR Main PCB Assy (-00A) in case Tech-Info No. 0002 has been made on HR Main PCB Assy (-00A). However, GND reinforcement will not be effective if do that.
5. This is not listed on the table above but RCA PCB Assy has also been changed to (-00C). Only the part number has been changed so that RCA PCB Assy (-00A) and (-00C) are completely the same. Purpose of the change is to align the version with BNC and D-SUB PCB Assy as all three PCB Assy's are made as one Gather PCB Assy.

2. Original PCB Assy's (-00A) are no longer available.

TEAC **TECHNICAL INFORMATION**

TASCAM DA-78HR, Change of HR MAIN PCB Assy

No. **0024**
DATE 22nd September 2000

HR Main PCB Assy has been changed for following purposes.

1. Incorporating hardware changes made in the past. (Tech-Info No. 0002/0003/0004/005)
2. Change of foil pattern to reinforce the GND line.

Addition
Item 2 above relates to Tech-Info No. 0023 (TC out interruption). Usually, that problem can be solved by Tech-Info No. 0023. However, there may be a possibility that Tech-Info No. 0023 may not be sufficient with the products that have a powerful WORD driving circuit. Therefore GND on HR Main, BNC and D-SUB PCB Assy has been reinforced simultaneously.

	Original P/No.	New P/No.
HR Main PCB Assy (Ref 1-9)	E950989-00A	E950989-00B
BNC PCB Assy (Ref 1-4)	E950993-00A	E950993-00C
D-SUB PCB Assy (Ref 1-5)	E950992-00A	E950992-00C

All 3 PCB Assy's have been changed on the products with S/No. 0170001 and higher.

Notice:
1. Basically above 3 PCB Assy's should be combined in one unit.
2. Spares stock for original PCB Assy (-00A) will be maintained.
3. BNC PCB Assy (-00A) and (-00C) are interchangeable. However, GND reinforcement will not be effective if BNC PCB Assy (-00C) is mounted on the HR Main PCB Assy (-00A)
4. D-SUB PCB Assy (-00C) can be mounted on HR Main PCB Assy (-00A) in case Tech-Info No. 0002 has been made on HR Main PCB Assy (-00A). However, GND reinforcement will not be effective if do that.
5. This is not listed on the table above but RCA PCB Assy has also been changed to (-00C). Only the part number has been changed so that RCA PCB Assy (-00A) and (-00C) are completely the same. Purpose of the change is to align the version with BNC and D-SUB PCB Assy as all three PCB Assy's are made as one Gather PCB Assy.

TECHNICAL INFORMATION

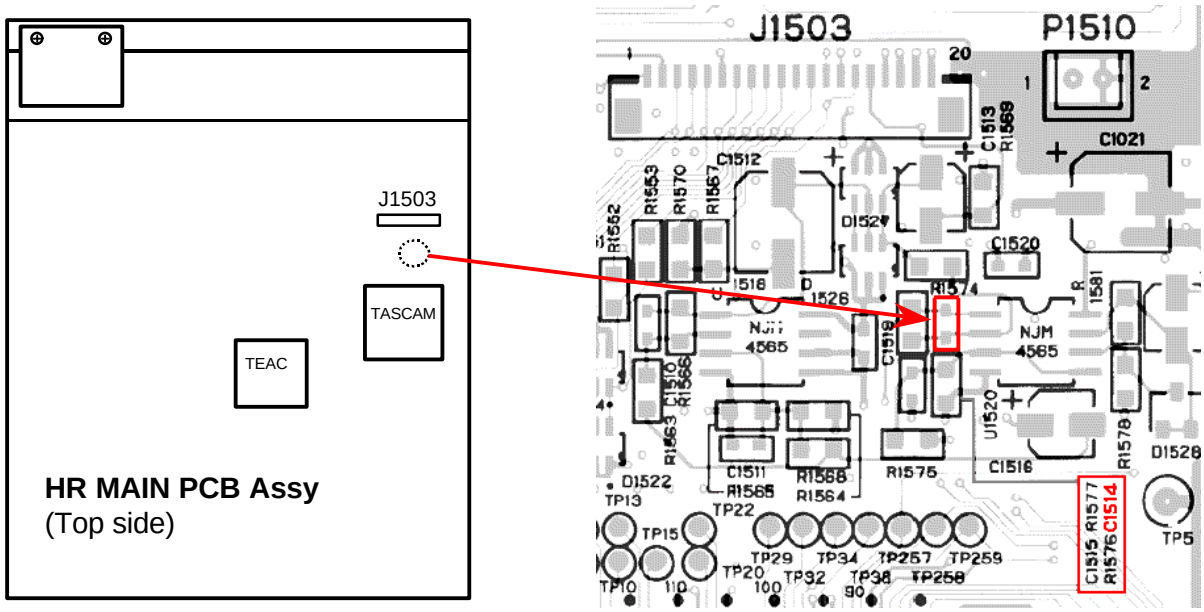
TASCAM DA-78HR, Interruption of timecode output

No. **0023**
DATE 22nd September 2000

Symptom: Timecode output (SMPTE/EBU and MTC) is interrupted in case WORD signal (44.1 kHz) is fed to WORD SYNC IN.
Cause: GND on the BNC PCB Assy is affected by WORD connection causing noise at TC circuit.
Solution: C1514 on the HR Main PCB Assy has been changed from 39 pF to 100 pF on the products with S/No. 0160001 and higher.

* No problem with 48 kHz WORD.
* Clock setting of the DA-78HR does not concern. Symptom occurs with only WORD connection.

Ceramic capacitor, 100 pF 50 V, **P/No. C0001594**



Service Hint

1. For temporal solution, applying double termination with BNC-T plug and 75Ω is suggested.
2. However, there are products in the market that have a powerful WORD driving circuit. In this case, the work of this Tech-Info may not be effective. When such, go to Tech-Info No. 0024.

TEAC TECHNICAL INFORMATION

TASCAM DA-78HR, Change of Drum Assy & Servo PCB Assy

No. **0021**
DATE 23rd August 2000

Production of ATF IC (CXA1204Q, U101 on the Servo PCB Assy) has been discontinued.
As the original and the substitution ATF IC are incompatible, Servo PCB Assy has newly been designed.

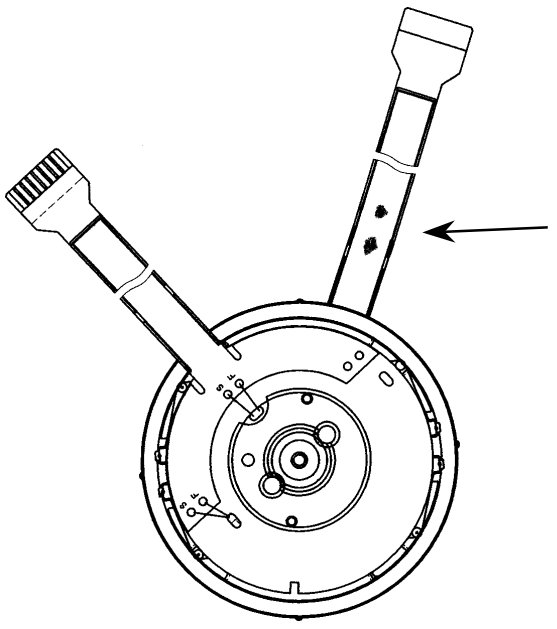
With the new Servo PCB Assy, it is required to change the height difference of Recording and Playback head from original 172 μm to 173 μm. Therefore, Drum Assy, HR01 has also been designed newly.

New Servo PCB Assy and new Drum Assy, HR01 have been mounted on the products with S/No. 0120371 and higher.

	P/No. (Original)	P/No. (New)
Servo PCB Assy	E950994-00A	E950994-00B
Drum Assy	M009210-00A (Drum Assy, HR)	M009210-00B (Drum Assy, HR01)

Notice:

1. The original and the new parts cannot be combined.
   Servo PCB Assy (-00A) and Drum Assy (-00A) should be paired.
   Servo PCB Assy (-00B) and Drum Assy (-00B) should be paired.
2. If the original and the new are combined, error rate at punch-in/out section will become worse.
3. Spares stock for the original Drum Assy will be maintained. No need to use the new parts.
4. Drum Assy, HR01 has two dots marked on the flexible cable as shown below.



Drum Assy, HR01

Two dots here.

TEAC **TECHNICAL INFORMATION**

TASCAM DA-78HR, Rec Current Adjustment

No. **0018**
DATE 26th June 2000

Symptom: On some products, value of recording current adjustment does not reach the specification. It shows 9.5 ~10 mAp-p while the specification is 11.2±0.2 mAp-p.
Cause: Due to batch tolerance of TC74VHCT541 (U1502 on the HR Main PCB Assy), there may be some IC's that output level is lower (approx. +4V).
Solution: Replace with TC74VHC541.

This change has been made on the products with S/No. 0130001 and higher.

	Old	New
U1502	TC74VHCT541	TC74VHC541, **P/No. S0020344**

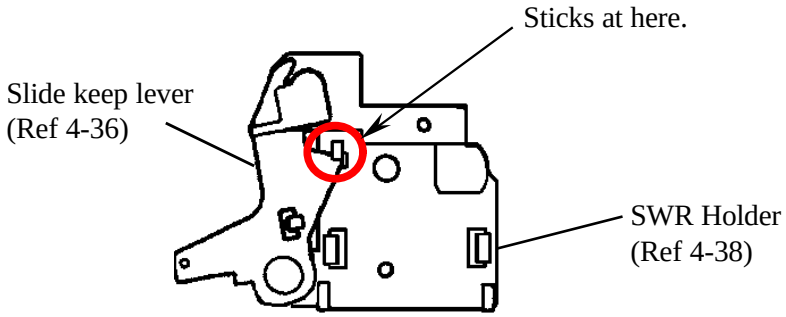
Note: To facilitate the production parts, U1401, U1506 and U1507 have been changed to the same TC74VHC541 simultaneously. However, replacing only U1502 is enough for service purpose.

TEAC **TECHNICAL INFORMATION**

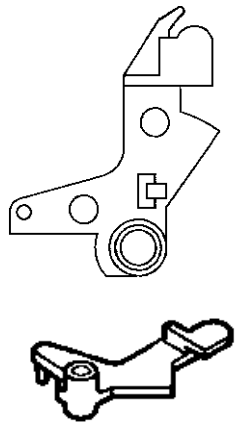
TASCAM DA-78HR, Change of Slide Keep Lever (S-Err 41)

No. **0015**
DATE 12th June 2000

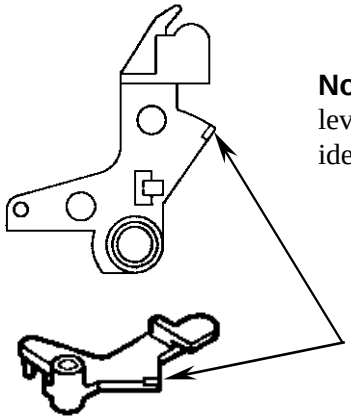
Symptom: Unit does not go to 100 times speed (F.FWD/REW).
S-Err 41 would be displayed then freeze.
Cause: Slide keep lever (Ref 4-36) sticks at a tip of the SWR Holder (Ref 4-38).
Then Solenoid (Ref 4-37) does not latch.
Solution: Change of a shape of the slide keep lever.



Old Slide Keep lever



New Slide Keep lever
P/No. 16788704-02



Note: Color of the new Slide Keep lever has been changed to black for identification.

This change has been made on the DA-78HR S/No. 0130001 and higher.
(DA-38/88/98: No production as of 20/May/2000.)

TECHNICAL INFORMATION

TASCAM DA-78HR, ROM Upgrade (MAIN V1.08)

No. **0014**
DATE 26th May 2000

Main ROM, U1003 on the HR MAIN PCB Assy has been upgraded from V1.03 to V1.08 on the products with S/No. 0130001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
MAIN V1.08	**S003653-00D**	**S0035153**, IC,MBM29F800BA-70PF

Problems corrected by V1.08

1. If TC Track is recorded (or just setting TC Rec Enable=1 and operate PLAY mode), ABS time may be re-wrote erratically (jump, discontinuous).
2. Jogging is not smooth enough through MIDI or remote control.
3. STOP LED blinks but no other LED's lit on RC-828 upon HR mode select.
4. "In TC timing" is selective only on "ANALOG".
5. False Auto Offset data may be registered in case no tape is loaded or tape with no TC recorded is loaded or no master TC is fed.
6. Jog is not effective after Shuttling by RC-828 operation.
7. ALL SAFE entered by RC-848 or RC-898 is released by REC TRACK SEL command through MIDI.
8. Punch out is not possible in slave unit through MIDI when write-protected tape is loaded on master.
9. During Rehearsal/Auto Rec mode, LOC 1/2 keys correspond to in/out points. That goes to Memo 1/2 with RC-808 operation.
10. Rec starts erratically at the mode finally selected when Fs/HR mode was once changed and even the change was cancelled afterward at the format ready mode.
11. Worsened error rate occurs when TDIF dubbing to another DA-78HR is made while tape is stopped.
12. A new feature of DA-98HR, clock select to "slot" is not selective by future RC-898 when DA-98HR is set next to DA-78HR in the DTRS chain.
13. Entry of Rehearsal/Auto rec mode is not possible while TC chase.

Additional Information:

An additional version seal like below has been stuck at both sides on the carton.

M108T105S104

M108: Main Ver 1.08 (U1003 System Control)
T105: TCM Ver 1.05 (U1006 TC, MIDI)
S104: SCI Ver 1.04 (U1035 Remote, Sync i/o serial interface)

TEAC **TECHNICAL INFORMATION**

TASCAM DA-78HR, Clearing the Servo RAM

No. **0009**
DATE 26th April 2000

Strictly confidential

Drum time, times of cleaning, and servo error history[1] can be cleared by the following procedure.

1 Set the DA-78HR to Test Mode[2].
2 Hold SHIFT and press CLEAR.
Display shows **[SVO Init]** for 1 sec then goes to **[rEAdy]** automatically.
3 Hold CLEAR for 2 sec. The servo RAM is cleared and **[CLEAr]** is displayed.

In case drum time or times of head cleaning are needed to be set, proceed to below.

4 Each time pressing MENU or SUB MENU, the display shows following:
[d. 0000]
[d.S. 0000]
[CLEn. 0000]
5 Set the value with using ▼ or ▲.
6 Turn the power off to memorize.

References:
1 See 2-2-5, page 7, service manual.
2 See 2-1, page 6, service manual.

TEAC

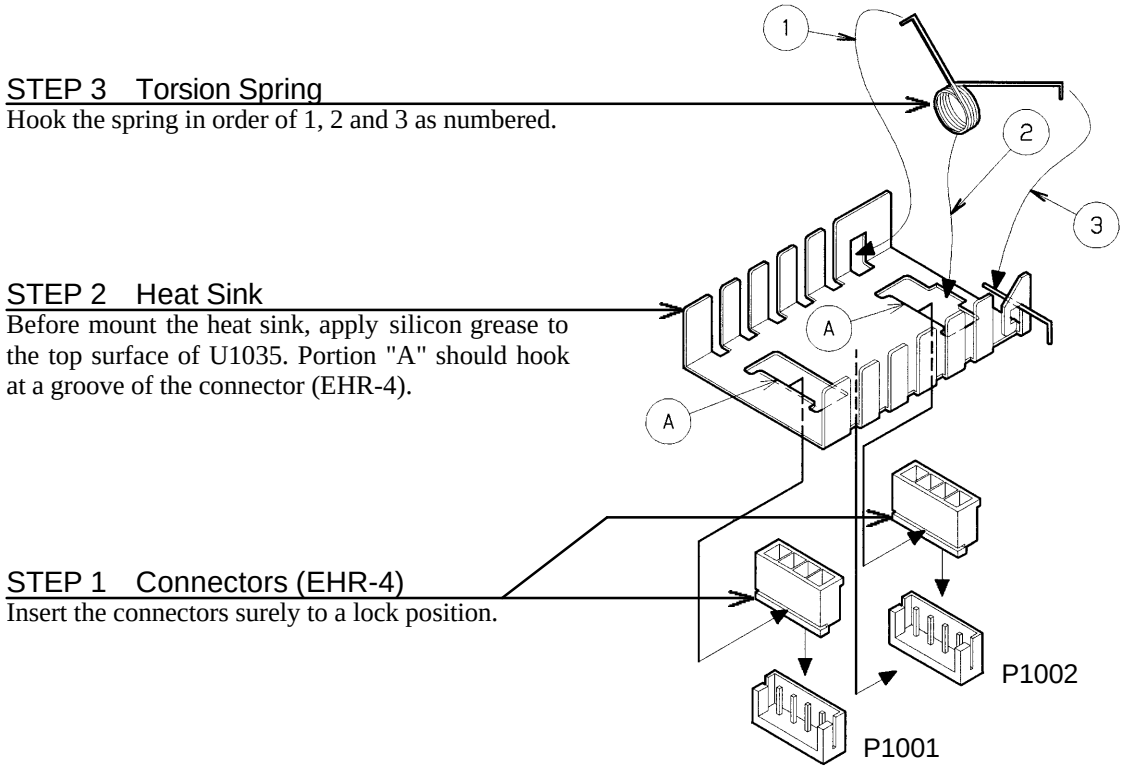
TECHNICAL INFORMATION

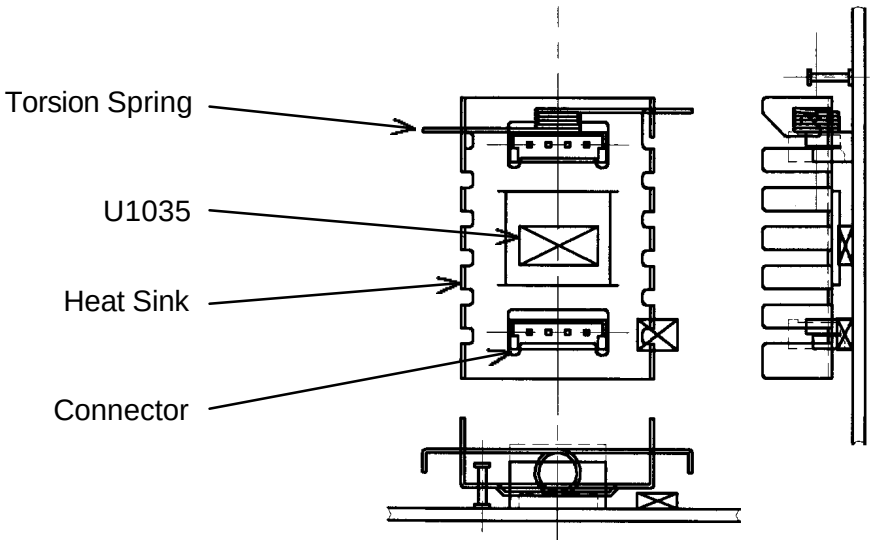
TASCAM DA-78HR, Heat Sink Kit

No. **0008**
DATE 28th March 2000

Heat sink has newly been added on the products with S/No. 0090001 and higher as the unit may become inoperative when the temperature of U1035 on the HR MAIN PCB Assy reaches 45 ºC.

Heat Sink Kit, DA-78HR **P/No. V000893-00A**





TEAC **TECHNICAL INFORMATION**

TASCAM DA-78HR/98, Change of Photo Transistor

No. **0007**
DATE 28th March 2000

Production of the phototransistor for BOT/EOT sensor has been discontinued. Substitution is as follows. Bracket for the phototransistor has also been changed as the shape of the new phototransistor does not match the original bracket.

	Original	New
Ref 3-21	**P/No. 13419661** PHOTO TR, PLT-462T3	**P/No. 13419521** Photo Element, GL450
Ref 3-22	**P/No. 16788721-00** Bracket, LED (white)	**P/No. 16788721-50** Bracket, LED (black)

Note: Original parts are still available as of 28/Mar/2000.
PHOTO TR, PLT-462T3 656 pcs
Bracket, LED (white) 510 pcs

Change has been made on:

DA-98	S/No. 0170001 and higher
DA-78HR	S/No. 0060001 and higher
DA-38/88	No production

TEAC TECHNICAL INFORMATION

TASCAM DA-78HR, ROM Upgrade (MAIN V1.02/V1.03)

No. **0006**
DATE 28th March 2000

Changes have been made on the MAIN ROM, U1003 on the HR MAIN PCB Assy.

MAIN V1.00 → V1.02

Problems corrected by MAIN V1.02
1) No audio is outputted when SHUTTLE PAUSE → PLAY is performed.
(No problem with SHUTTLE PAUSE → STOP → PLAY.)
2) Servo errors (S-Err XX) are not displayed correctly.
3) Cassette is not ejected when a cassette that has a tape cut is loaded.

Products with S/No. up to 0049999 in Tokyo stock have been reworked and "D" mark have been stamped on the carton.
All products with S/No. 0050001 and higher have V1.02.

MAIN V1.02 → V1.03

Problem corrected by MAIN V1.03
The DA-78HR cannot receive the TDIF signal coming from the TM-D8000 correctly. Noise occurs.
Solution is to change the threshold level of TDIF input from TTL to CMOS level.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
MAIN V1.03	**S003653-00C**	**S0035153**, IC,MBM29F800BA-70PF

Products with S/No. up to 0079999 in Tokyo stock have been reworked and "G" mark have been stamped on the carton.
All products with S/No. 0080001 and higher have V1.03 mounted with no mark.

Note: "G" mark includes "D" and "•".

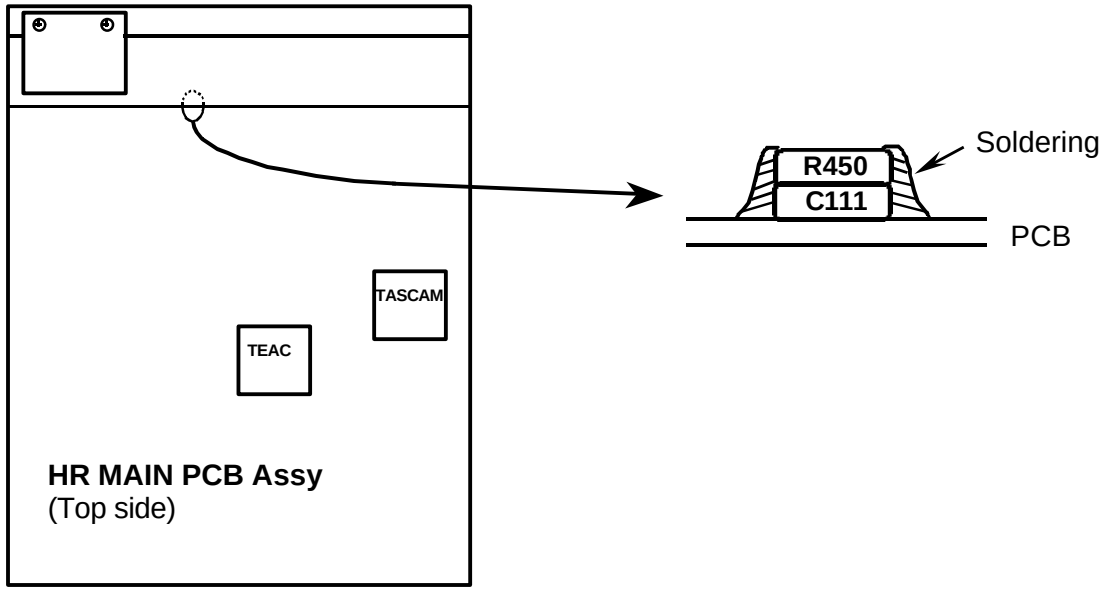
TECHNICAL INFORMATION

TASCAM DA-78HR, Distortion Ratio on Analog Output

No. **0005**
DATE 28th March 2000

Distortion ratio for analog output on some channels may be deteriorated by 0.008 % through a mute transistor while the specification is 0.004 % (DTRS-HR) and 0.005 % (DTRS).

To improve the distortion ratio, one pce of 100 kΩ resistor, R450 (**P/No. 11152104**) has newly been added parallel to C111 on the HR MAIN PCB Assy.



Products with S/No. up to 0079999 in Tokyo stock have been reworked and "G" mark have been stamped on the carton.
All products with S/No. 0080001 and higher have R450.

Note 1) The distortion ratio of each channel has been checked at the production line and the mute transistor has been replaced in case the value exceeds the specification. Therefore basically there should be no problem on all units that have already been released to the market with no "G" mark.

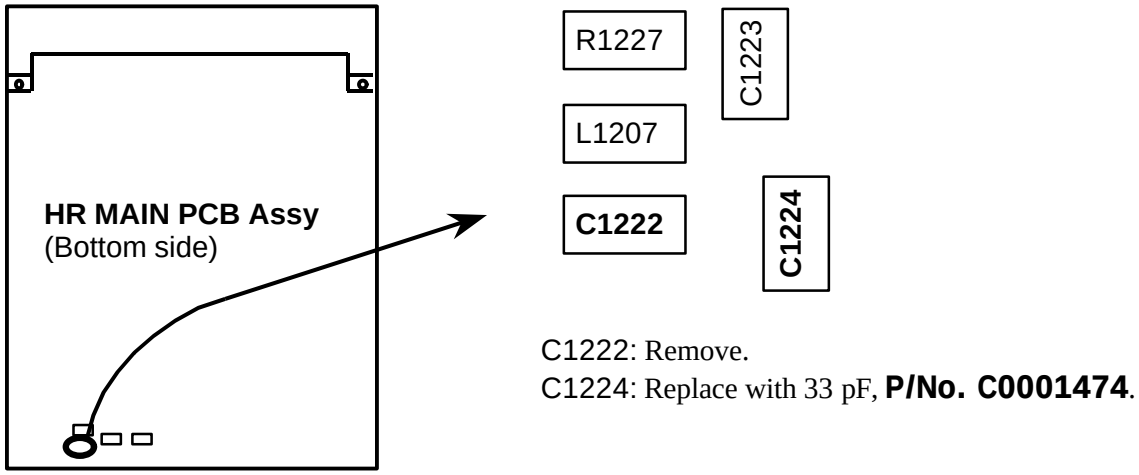
Note 2) "G" mark includes "D" and "•".

TECHNICAL INFORMATION

TASCAM DA-78HR, Error Rate at ± 6 % Vari-Pitch

No. **0004**
DATE 24th March 2000

Error rate is deteriorated when the unit runs at ±6 % vari-pitch, resulting that PB CONDITION LED will light. To stabilize the PLL circuit, following change has been made.



C1222: Remove.
C1224: Replace with 33 pF, **P/No. C0001474**.

Products with S/No. up to 0079999 in Tokyo stock have been reworked and "G" mark have been stamped on the carton.
All products with S/No. 0080001 and higher have been improved with no mark.

Note: "G" mark includes "D" and "•".

TECHNICAL INFORMATION

TASCAM DA-78HR, Clock Stabilizing

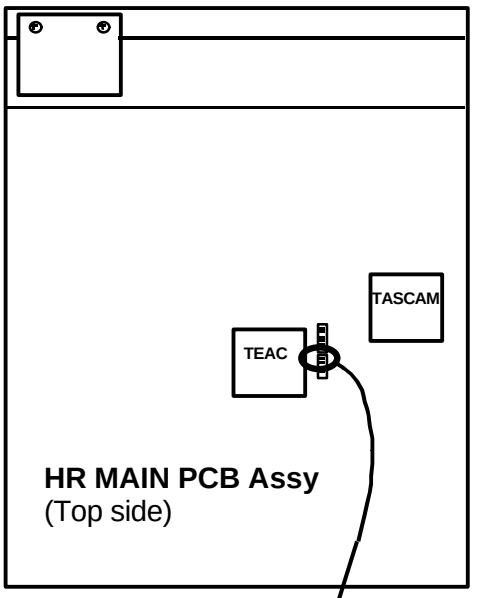
No. **0003**
DATE 28th March 2000

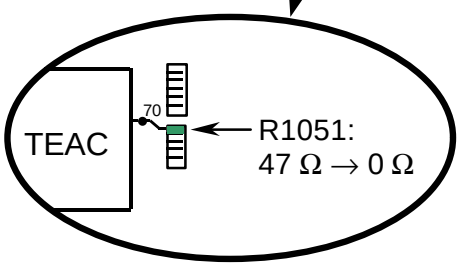
To stabilize the clock circuit, following changes have been made.

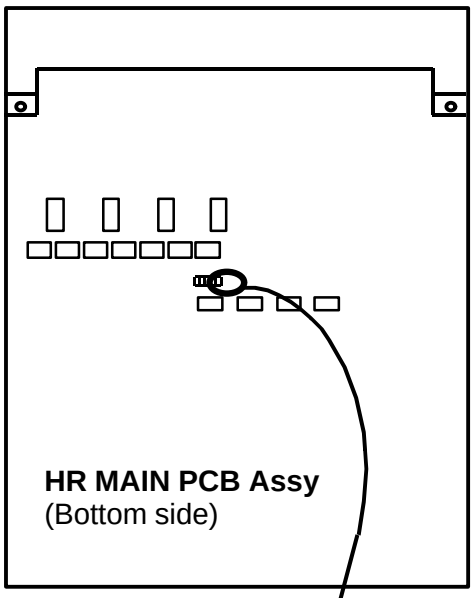
R1051 47 Ω → 0 Ω (jumper), **P/No. 11986740**
R1410 47 Ω → 0 Ω (jumper), **P/No. 11986740**

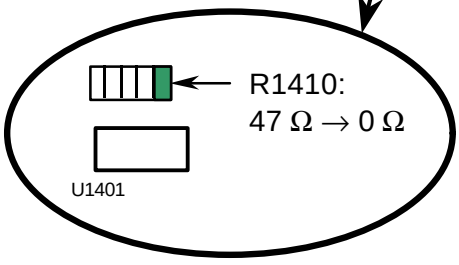
Note:
Change of R1051 solves a noise occurring with Mackie d8b digital console through TDIF out.
Change of R1410 solves that DA-78HR SPDIF out may not be received by other SPDIF machines.

Products with S/No. up to 0049999 in Tokyo stock have been reworked and "D" and " •" mark have been stamped on the carton.
All products with S/No. 0050001 and higher have been improved.









AK4393

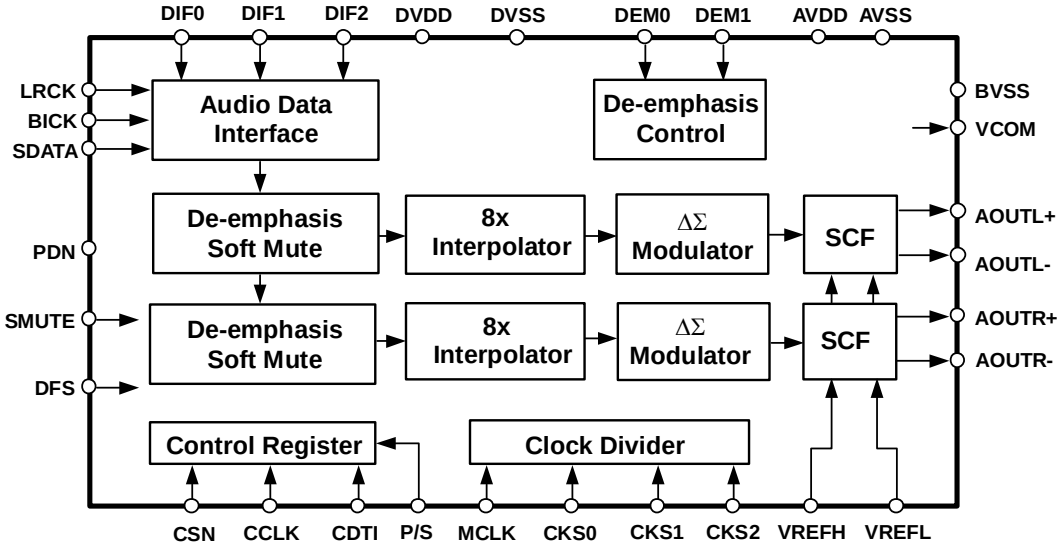
Advanced Multi-Bit 96kHz 24-Bit ΔΣ DAC

GENERAL DESCRIPTION

The AK4393 is a high performance stereo DAC for the 96kHz sampling mode of DAT, DVD including a 24bit digital filter. The AK4393 introduces the advanced multi-bit system for ΔΣ modulator. This new architecture achieves the wider dynamic range, while keeping much the same superior distortion characteristics as conventional Single-Bit way. In the AK4393, the analog outputs are filtered in the analog domain by switched-capacitor filter (SCF) with high tolerance to clock jitter. The analog outputs are full differential output, so the device is suitable for hi-end applications. The operating voltages support analog 5V and digital 3.3V, so it is easy to I/F with 3.3V logic IC.

FEATURES

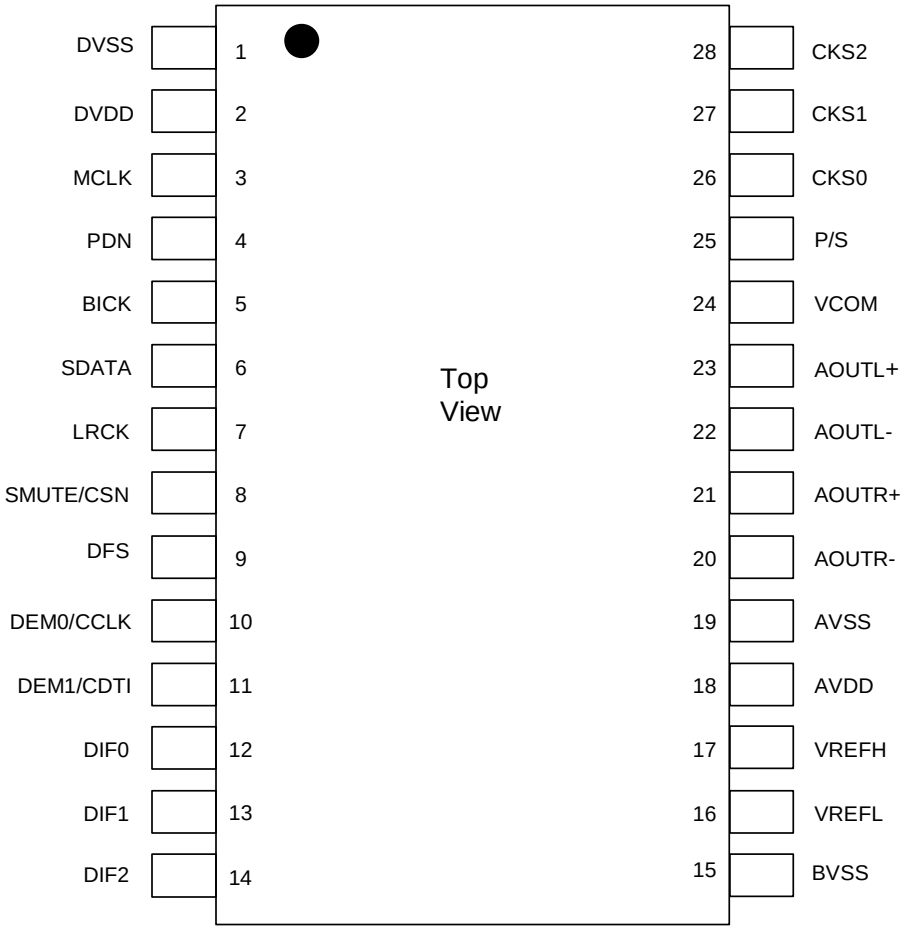
- **128x Oversampling**
- **Sampling Rate up to 108kHz**
- **24Bit 8x Digital Filter**
  Ripple: ±0.005dB, Attenuation: 75dB
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **Digital de-emphasis for 32, 44.1, 48 & 96kHz sampling**
- **Soft Mute**
- **THD+N: -100dB**
- **DR, S/N: 120dB**
- **I/F format : MSB justified, 16/20/24bit LSB justified, I^2S**
- **Master Clock: Normal Speed: 256fs, 384fs, 512fs or 768fs**
  Double Speed: 128fs, 192fs, 256fs or 384fs
- **Power Supply: 4.75 to 5.25V (Analog), 3 to 5.25V (Digital)**
- **Small Package: 28pin VSOP**



■ Ordering Guide

AK4393VF	-40 ~ +85 °C	28pin VSOP (0.65mm pitch)
AKD4393	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVSS	-	Digital Ground Pin
2	DVDD	-	Digital Power Supply Pin, 3.3V or 5.0V
3	MCLK	I	Master Clock Input Pin
4	PDN	I	Power-Down Mode Pin When at "L", the AK4393 is in power-down mode and is held in reset. The AK4393 should always be reset upon power-up.
5	BICK	I	Audio Serial Data Clock Pin The clock of 64fs or more than is recommended to be input on this pin.
6	SDATA	I	Audio Serial Data Input Pin 2's complement MSB-first data is input on this pin.
7	LRCK	I	L/R Clock Pin
8	SMUTE	I	Soft Mute Pin in parallel mode When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CSN	I	Chip Select Pin in serial mode
9	DFS	I	Double Speed Sampling Mode Pin (Internal pull-down pin) "L": Normal Speed , "H": Double Speed
10	DEM0	I	De-emphasis Enable Pin in parallel mode
	CCLK	I	Control Data Clock Pin in serial mode
11	DEM1	I	De-emphasis Enable Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode
12	DIF0	I	Digital Input Format Pin
13	DIF1	I	Digital Input Format Pin
14	DIF2	I	Digital Input Format Pin
15	BVSS	-	Substrate Ground Pin, 0V
16	VREFL	I	Low Level Voltage Reference Input Pin
17	VREFH	I	High Level Voltage Reference Input Pin
18	AVDD	-	Analog Power Supply Pin, 5.0V
19	AVSS	-	Analog Ground Pin, 0V
20	AOUTR-	O	Rch Negative analog output Pin
21	AOUTR+	O	Rch Positive analog output Pin
22	AOUTL-	O	Lch Negative analog output Pin
23	AOUTL+	O	Lch Positive analog output Pin
24	VCOM	O	Common Voltage Output Pin, 2.6V
25	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
26	CKS0	I	Master Clock Select Pin
27	CKS1	I	Master Clock Select Pin
28	CKS2	I	Master Clock Select Pin

Note: All input pins except internal pull-up/down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, BVSS, DVSS = 0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	| BVSS-DVSS | (Note 2)	Δ GND	-	0.3	V
Input Current , Any pin Except Supplies		IIN	-	±10	mA
Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Operating Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Notes: 1. All voltages with respect to ground.
2. AVSS, BVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, BVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog	AVDD	4.75	5.0	5.25	V
(Note 3)	Digital	DVDD	3.0	3.3	5.25	V
Voltage Reference	"H" voltage reference	VREFH	AVDD-0.5	-	AVDD	V
(Note 4)	"L" voltage reference	VREFL	AVSS	-	-	V
	VREFH-VREFL	Δ VREF	3.0	-	AVDD	V

Notes: 3. The power up sequence between AVDD and DVDD is not critical.
4. Analog output voltage scales with the voltage of (VREFH-VREFL).
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = ±2.4Vpp×(VREFH-VREFL)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta = 25°C; AVDD = 5V, DVDD = 3.3V; AVSS, BVSS, DVSS = 0V, VREFH = AVDD, VREFL = AVSS;
fs = 44.1kHz; BICK = 64fs; Signal Frequency = 1kHz; 24bit Input Data; Measurement Bandwidth = 20Hz~20kHz;
$R_L \geq 600\Omega$; External circuit: Figure 11; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					24	Bits
Dynamic Characteristics (Note 5)						
THD+N	fs=44.1kHz	0dBFS		-100	-90	dB
	BW=20kHz	-60dBFS		-53	-	dB
	fs=96kHz	0dBFS		-97	-86	dB
	BW=40kHz	-60dBFS		-51	-	dB
Dynamic Range (-60dBFS with A-weighted)	fs=44.1kHz	(Note 6)	112	117		dB
		(Note 7)	-	120		dB
	fs=96kHz		111	116		dB
		(Note 7)	-	118		dB
S/N (A-weighted	fs=44.1kHz	(Note 8)	112	117		dB
		(Note 7)	-	120		dB
	fs=96kHz		111	116		dB
		(Note 7)	-	118		dB
Interchannel Isolation (1kHz)			100	120		dB
DC Accuracy						
Interchannel Gain Mismatch				0.15	0.3	dB
Gain Drift		(Note 9)		20	-	ppm/°C
Output Voltage		(Note 10)	±2.25	±2.4	±2.55	Vpp
Load Resistance		(Note 11)	600			Ω
Output Current					3.5	mA
Power Supplies						
Power Supply Current						
Normal Operation (PDN = "H")						
AVDD				60	-	mA
DVDD(fs=44.1kHz)				3	-	mA
DVDD(fs=96kHz)				5	-	mA
AVDD + DVDD					90	mA
Power-Down Mode (PDN = "L")						
AVDD + DVDD		(Note 12)		10	50	μA
Power Supply Rejection		(Note 13)		50		dB

Notes: 5. At 44.1kHz, measured by Audio Precision, System Two. Averaging mode.
At 96kHz, measured by ROHDE & SCHWARZ, UPD. Averaging mode.
Refer to the eva board manual.
6. 101dB at 16bit data and 116dB at 20bit data.
7. By Figure12. External LPF Circuit Example 2.
8. S/N does not depend on input bit length.
9. The voltage on (VREFH-VREFL) is held +5V externally.
10. Full-scale voltage (0dB). Output voltage scales with the voltage of (VREFH-VREFL).
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = ±2.4Vpp×(VREFH-VREFL)/5.
11. For AC-load. 1kΩ for DC-load.
12. In the power-down mode. P/S = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.
13. PSR is applied to AVDD, DVDD with 1kHz, 100mVpp. VREFH pin is held +5V.

FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; fs = 44.1kHz; Normal Speed Mode; DEM = OFF)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband ±0.01dB (Note 14)		PB	0		20.0	kHz
-6.0dB			-	22.05	-	kHz
Stopband (Note 14)		SB	24.1			kHz
Passband Ripple		PR			± 0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 15)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response 0 ~ 20.0kHz			-	± 0.2	-	dB

Note: 14. The passband and stopband frequencies scale with fs.
For example, PB = 0.4535×fs (@±0.01dB), SB = 0.546×fs.

15. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

FILTER CHARACTERISTICS (fs = 96kHz)

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; fs = 96kHz; Double Speed Mode; DEM = OFF)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband ±0.01dB (Note 14)		PB	0		43.5	kHz
-6.0dB			-	48.0	-	kHz
Stopband (Note 14)		SB	52.5			kHz
Passband Ripple		PR			± 0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 15)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response 0 ~ 40.0kHz			-	± 0.3	-	dB

DC CHARACTERISTICS

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%DVDD	V
Input Leakage Current	(Note 16)	Iin	-	-	± 10	μA

Note: 16. DFS and P/S pins have internal pull-down or pull-up devices, nominally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; C_L = 20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing (Note 17)					
Normal Speed: 256fs, Double Speed: 128fs	fCLK	7.7		13.824	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
Normal Speed: 384fs, Double Speed: 192fs	fCLK	11.5		20.736	MHz
Pulse Width Low	tCLKL	20			ns
Pulse Width High	tCLKH	20			ns
Normal Speed: 512fs, Double Speed: 256fs	fCLK	15.4		27.648	MHz
Normal Speed: 768fs, Double Speed: 384fs	fCLK	23.0		41.472	MHz
Pulse Width Low	tCLKL	7			ns
Pulse Width High	tCLKH	7			ns
LRCK Frequency (Note 18)					
Normal Speed Mode (DFS = "L")	fsn	30	44.1	54	kHz
Double Speed Mode (DFS = "H")	fsd	60	88.2	108	kHz
Duty Cycle	Duty	45		55	%
Serial Interface Timing					
BICK Period	tBCK	140			ns
BICK Pulse Width Low	tBCKL	60			ns
Pulse Width High	tBCKH	60			ns
BICK "↑" to LRCK Edge (Note 19)	tBLR	20			ns
LRCK Edge to BICK "↑" (Note 19)	tLRB	20			ns
SDATA Hold Time	tSDH	20			ns
SDATA Setup Time	tSDS	20			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Reset Timing					
PDN Pulse Width (Note 20)	tPW	150			ns

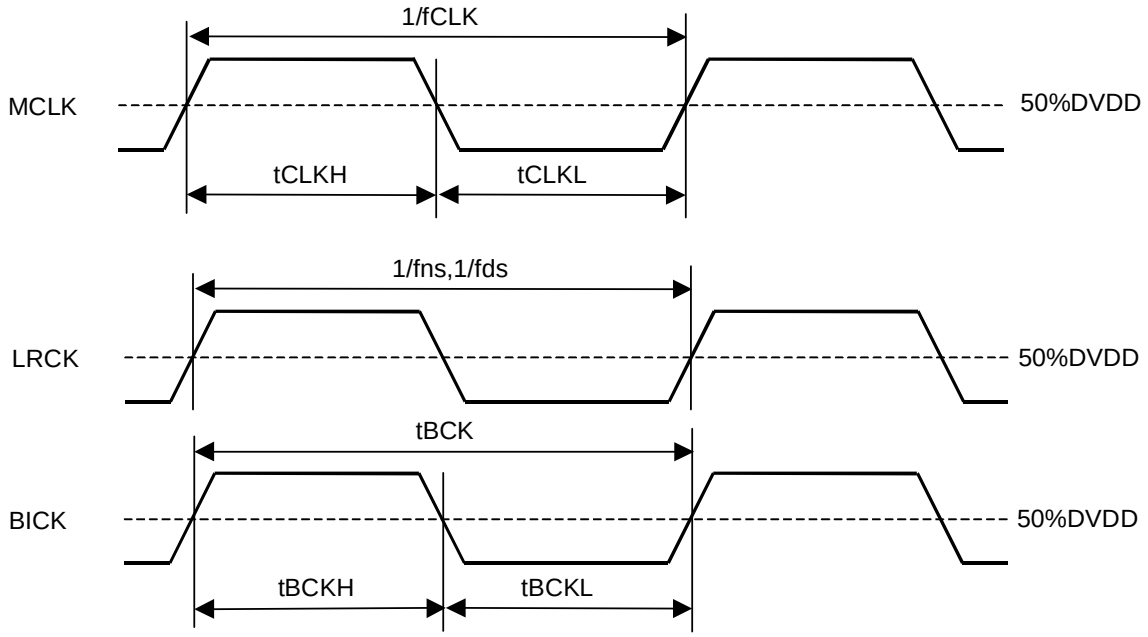
Notes: 17. **For Double Speed mode please see Appendix A for relationship of MCLK and BCLK/LRCK.**

18. When the normal and double speed modes are switched, AK4393 should be reset by PDN pin or RSTN bit.

19. BICK rising edge must not occur at the same time as LRCK edge.

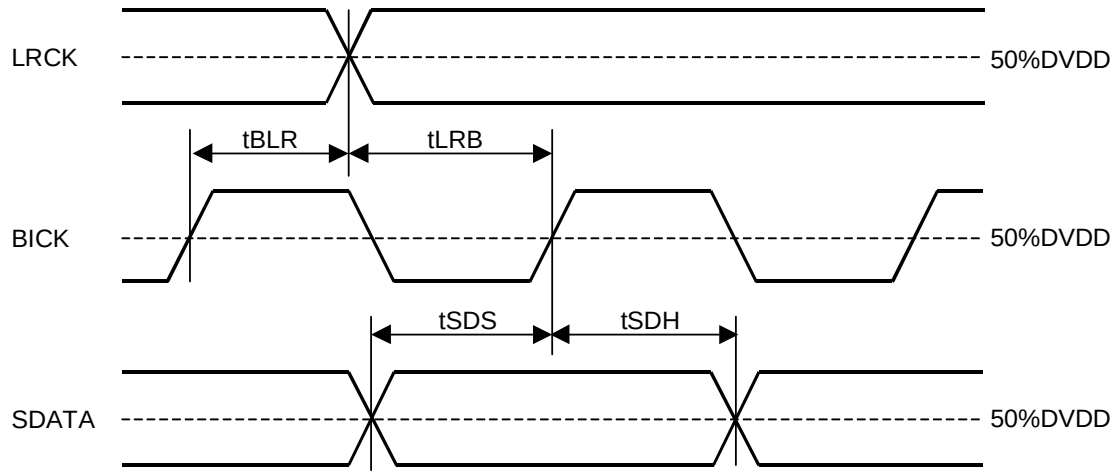
20. The AK4393 can be reset by bringing PDN "L" to "H".
When the states of CKS2-0 or DFS change, the AK4393 should be reset by PDN pin or RSTN bit.

■ **Timing Diagram**

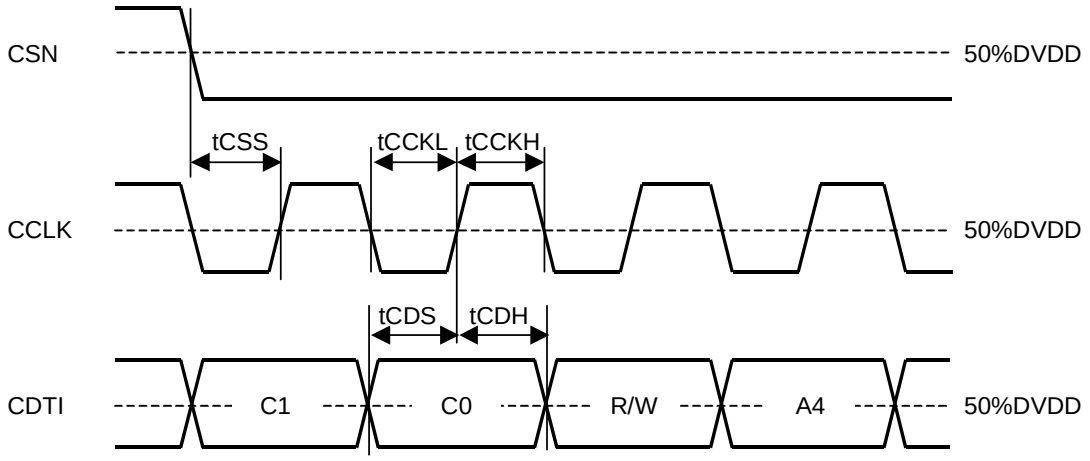


Clock Timing

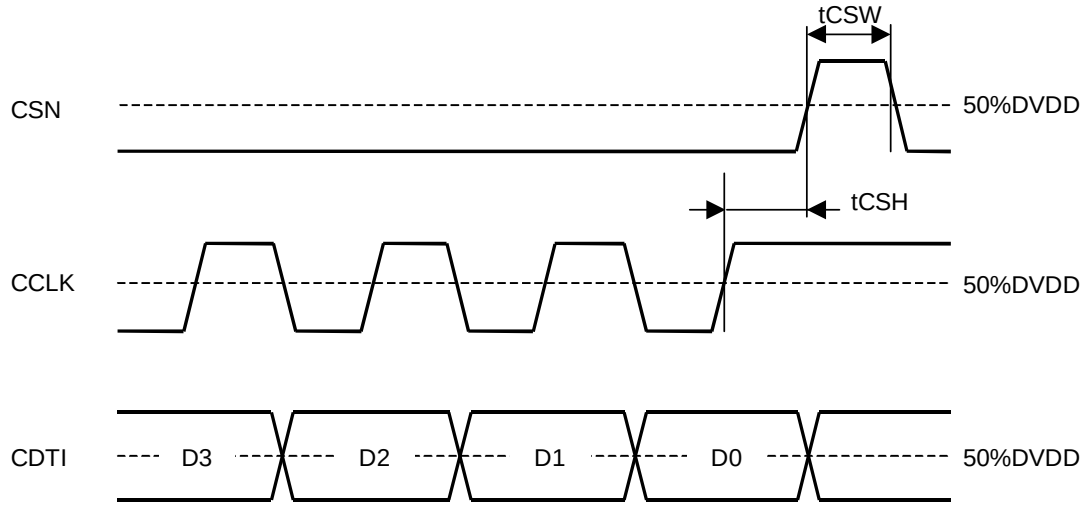
For Double Speed mode timing please see Appendix A for relationship of MCLK and BCLK/LRCK.



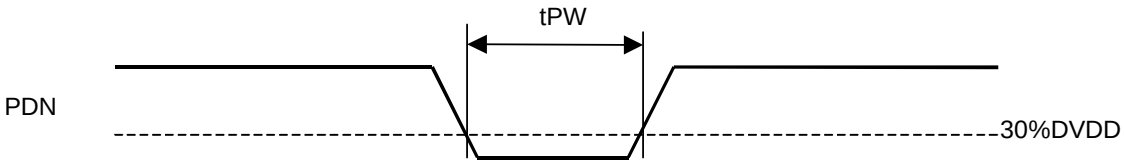
Audio Interface Timing



WRITE Command Input Timing



WRITE Data Input Timing



Power-down Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4393, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. **However, in Double Speed Mode, the phase relationship between MCLK and LRCK/BICK is limited. (Refer to Appendix A).** The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The sampling speed is set by DFS (Table 1). The sampling rate (LRCK), CKS0/1/2 and DFS determine the frequency of MCLK (Table 2).

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4393 is in normal operation mode (PDN = "H"). If these clocks are not provided, the AK4393 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4393 should be in the power-down mode (PDN = "L") or in the reset mode (RSTN = "0"). After exiting reset at power-up etc., the AK4393 is in power-down mode until MCLK and LRCK are input.

DFS	Sampling Rate (fs)		
0	Normal Speed Mode	30kHz~54kHz	Default
1	Double Speed Mode	60kHz~108kHz	

Table 1. Sampling Speed

Mode	CKS2	CKS1	CKS0	Normal	Double	
0	0	0	0	256fs	128fs	Default
1	0	0	1	256fs	256fs	
2	0	1	0	384fs	192fs	
3	0	1	1	384fs	384fs	
4	1	0	0	512fs	256fs	
5	1	0	1	512fs	N/A	
6	1	1	0	768fs	384fs	
7	1	1	1	768fs	N/A	

Table 2. System Clocks

LRCK	MCLK				BICK
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz

Table 3. System clock example (Normal Speed Mode)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 4. System clock example (Double Speed Mode)

■ Audio Serial Interface Format

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Five data formats are supported and selected by the DIF0-2 as shown in Table 5. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	Mode	BICK	Figure
0	0	0	0	0: 16bit LSB Justified	≥32fs	Figure 1
1	0	0	1	1: 20bit LSB Justified	≥40fs	Figure 2
2	0	1	0	2: 24bit MSB Justified	≥48fs	Figure 3
3	0	1	1	3: I^2S Compatible	≥48fs	Figure 4
4	1	0	0	4: 24bit LSB Justified	≥48fs	Figure 2

Table 5. Audio Data Formats

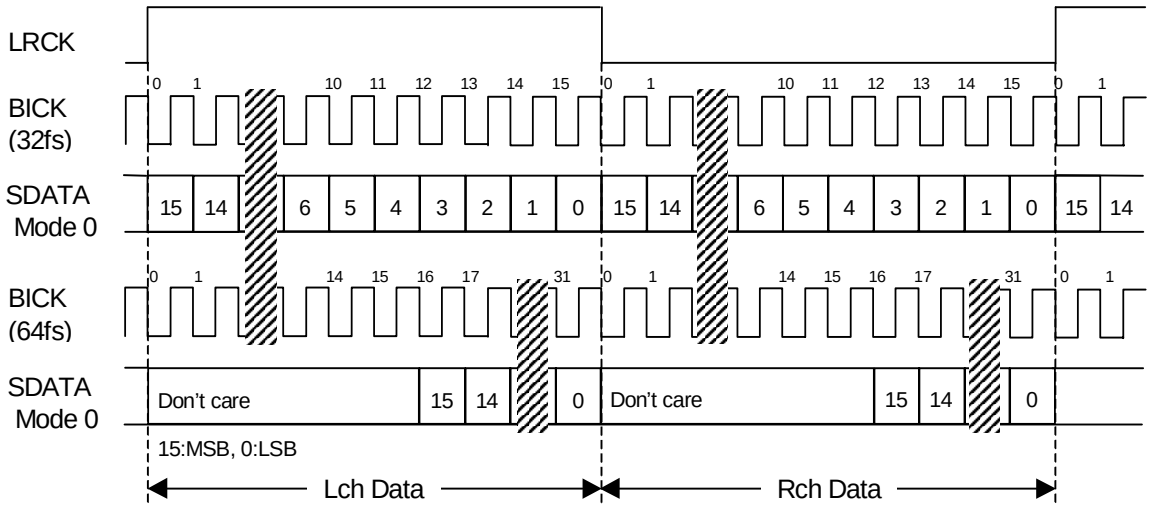


Figure 1. Mode 0 Timing

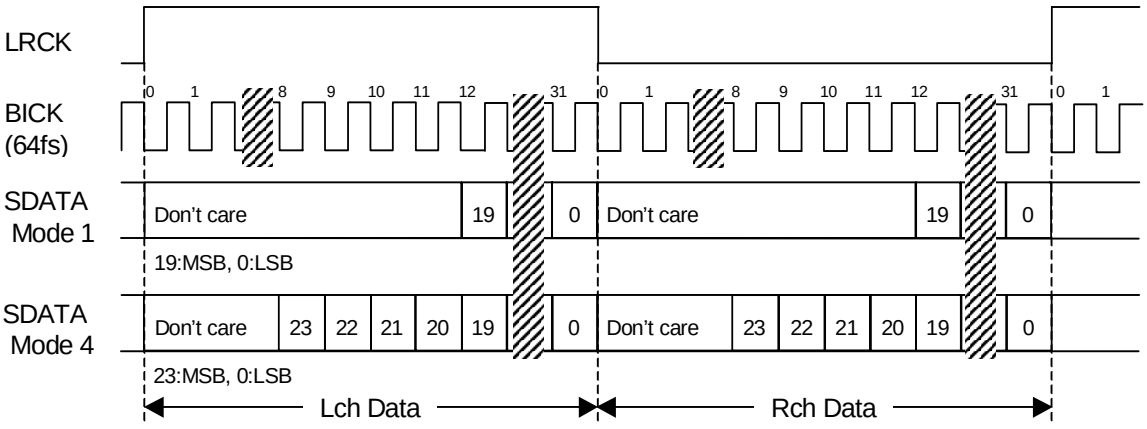


Figure 2. Mode 1,4 Timing

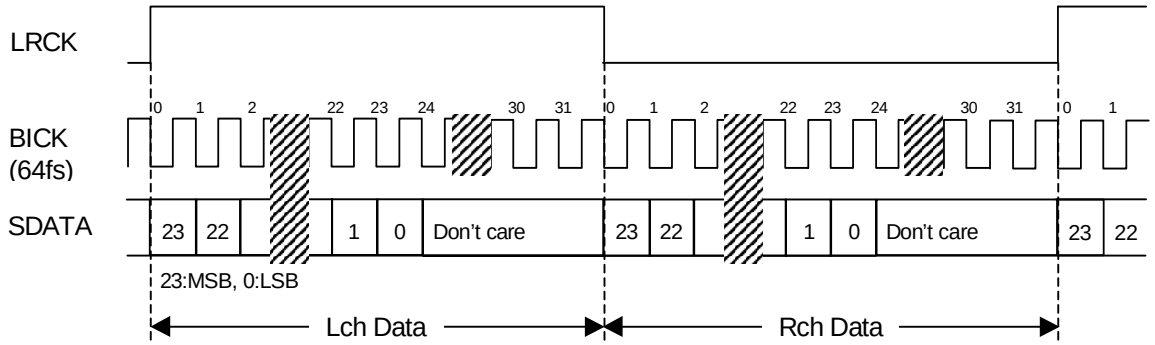


Figure 3. Mode 2 Timing

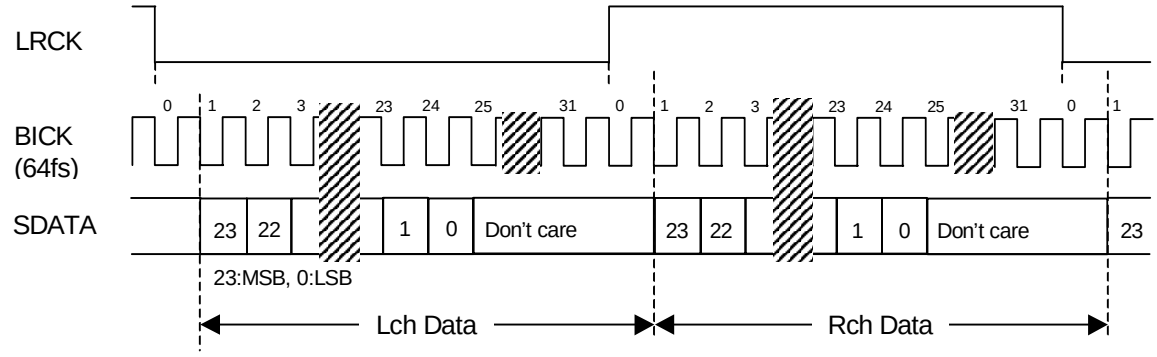


Figure 4. Mode 3 Timing

■ De-emphasis filter

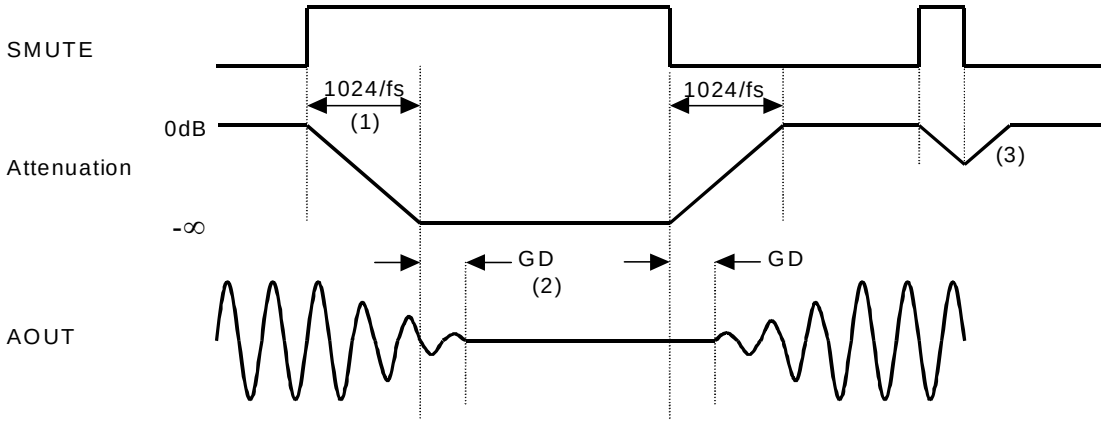
A digital de-emphasis filter is available for 32, 44.1, 48 or 96kHz sampling rates (tc = 50/15μs) and is enabled or disabled with the DEM0, DEM1 and DFS input pins.

DEM1	DEM0	DFS	Mode	
0	0	0	44.1kHz	Default
0	1	0	OFF	
1	0	0	48kHz	
1	1	0	32kHz	
0	0	1	OFF	
0	1	1	OFF	
1	0	1	96kHz	
1	1	1	OFF	

Table 6. De-emphasis filter control

■ Soft mute operation

Soft mute operation is performed at digital domain. When SMUTE goes to "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

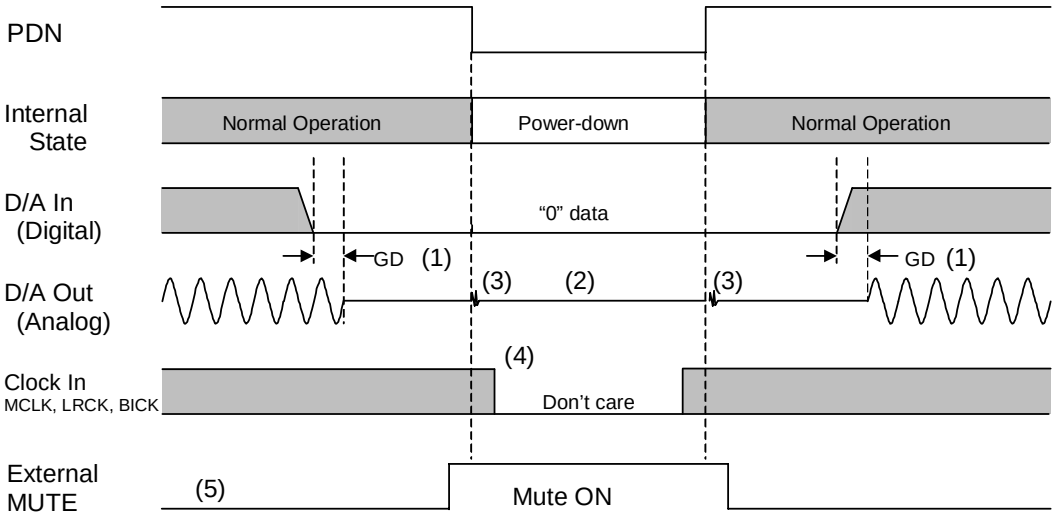
Figure 5. Soft mute operation

■ System Reset

The AK4393 should be reset once by bringing PDN = "L" upon power-up. The AK4393 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4393 is in the power-down mode until MCLK and LRCK are input.

■ Power-Down

The AK4393 is placed in the power-down mode by bringing PDN pin "L" and the anlog outputs are floating (Hi-Z). Figure 6 shows an example of the system timing at the power-down and power-up.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = "L").
(5) Please mute the analog output externally if the click noise (3) influences system application. The timing example is shown in this figure.

Figure 6. Power-down/up sequence example

■ Click Noise from analog output

Click noise occurs from analog output in the following cases.

1) When switching de-emphasis mode by DEM0, DEM1 and DFS pins,
2) When switching serial data mode by DIF0, DIF1 and DIF2 pins,
3) When going and exiting power down mode by PDN pin,
4) When switching normal speed and double speed by DFS pin,

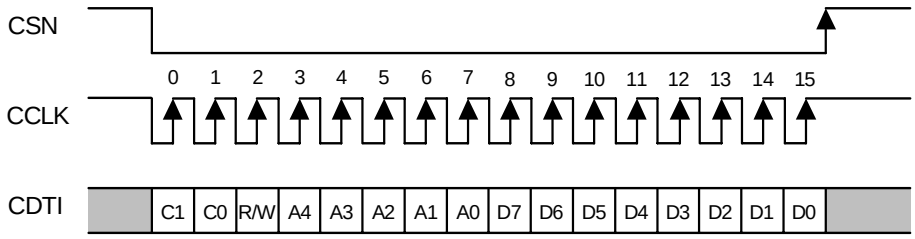
However in case of 1) & 2), If the input data is "0" or the soft mute is enabled (after 1024 LRCK cycles from SMUTE = "H"), no click noise occur except for switching DFS pin.

■ Mode Control Interface

Pins (parallel control mode) or registers (serial control mode) can control each functions of the AK4393. For DIF2-0, CKS2-0 and DFS, the setting of pin and register are "ORed" internally. So, even serial control mode, pin setting can also control these functions.

The serial control interface is enabled by the P/S pin = "L". In this mode, pin setting must be all "L". Internal registers may be written by 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2bits, C1/0; fixed to "01"), Read/Write (1bit; fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). The AK4393 latches the data on the rising edge of CCLK, so data should be clocked in on the falling edge. The writing of data becomes valid by CSN "↑". The clock speed of CCLK is 5MHz(max). The CSN and CCLK must be fixed to "H" when the register does not be accessed.

PDN = "L" resets the registers to their default values. When the state of P/S pin is changed, the AK4393 should be reset by PDN = "L". In serial mode, the internal timing circuit is reset by RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 7. Control I/F Timing

*The AK4393 does not support the read command and chip address. C1/0 and R/W are fixed to "011"
*When the AK4393 is in the power down mode (PDN = "L") or the MCLK is not provided, writing into the control register is inhibited.
*For setting the registers, the following sequence is recommended.

- Control 1 register
  (1) Writing RSTN = "0" and other bits (D6-D1) to the register at the same time.
  (2) Writing RSTN = "1" to the register. The other bits are no change.
- Control 2 register
  This writing sequence has no limitation like control 1 register.

*When RSTN = "0", the click noise is output from AOUT pins.
*If the mode setting is done without setting RSTN = "0", large noise may be output from AOUT pins. (Especially when CKS0/1/2 are changed.)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	CKS2	CKS1	CKS0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	0	0	DFS	DEM1	DEM0	SMUTE
02H	Test	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0

Notes:

For addresses from 03H to 1FH, data must not be written.

When PDN pin goes to "L", the registers are initialized to their default values. When RSTN bit goes to "0", the only internal timing is reset and the registers are not initialized to their default values. DIF2-0, CKS2-0 and DFS bits are ORed with pins respectively.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	CKS2	CKS1	CKS0	DIF2	DIF1	DIF0	RSTN
default		0	0	0	0	0	0	0	1

RSTN: Internal timing reset

0: Reset. All registers are not initialized.

1: Normal Operation

When the states of CKS2-0 or DFS change, the AK4393 should be reset by PDN pin or RSTN bit.

DIF2-0: Audio data interface modes (see Table 5)

Initial: "000", Mode 0

Register bits are ORed with DIF2-0 pins if P/S = "L".

CKS2-0: Master Clock Frequency Select (see Table 2)

Initial: "000", Mode 0

Register bits are ORed with CKS2-0 pins if P/S = "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	0	0	DFS	DEM1	DEM0	SMUTE
default		0	0	0	0	0	0	0	0

SMUTE: Soft Mute Enable

0: Normal operation

1: DAC outputs soft-muted

DEM1-0: De-emphasis response (see Table 6)

Initial: "00", 44.1kHz

DFS: Sampling speed control (see Table 1)

0: Normal speed

1: Double speed

Register bit is ORed with DFS pin if P/S = "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Test	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
default		0	0	0	0	0	0	0	0

TEST7-0: Test mode. Do not write any data to 02H.

SYSTEM DESIGN

Figure 8 and 9 show the system connection diagram. An evaluation board (AKD4393) is available which demonstrates the optimum layout, power supply arrangements and measurement results.

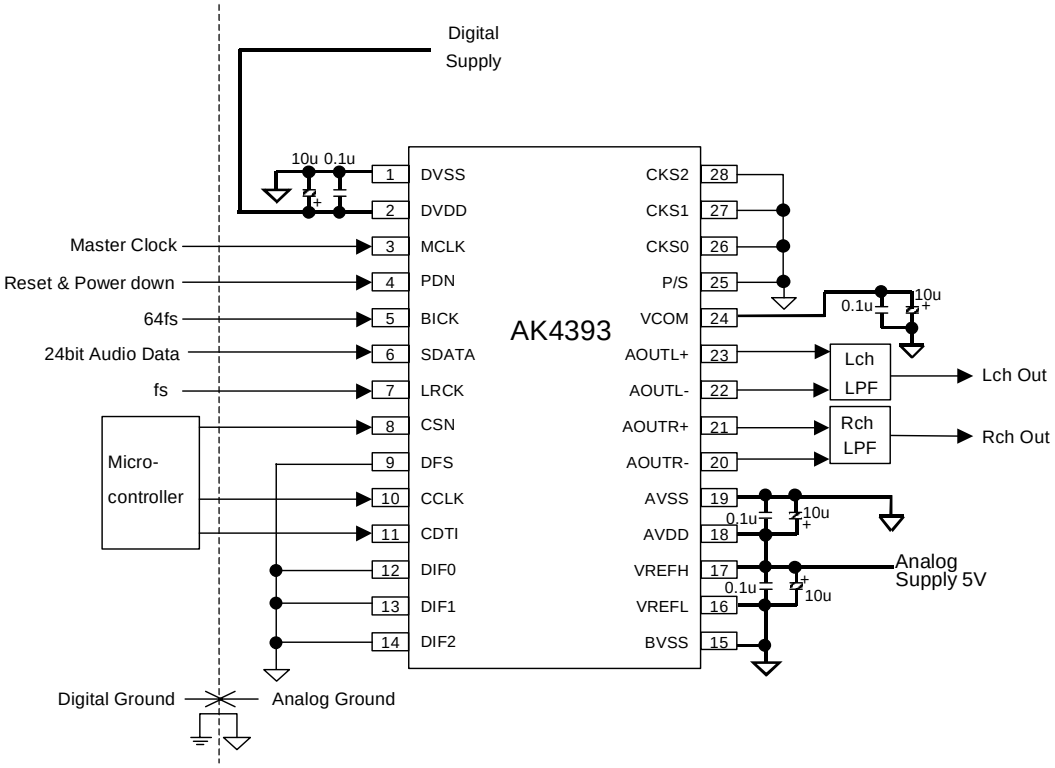


Figure 8. Typical Connection Diagram (Serial mode)

Notes:

- LRCK = fs, BICK = 64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS, BVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

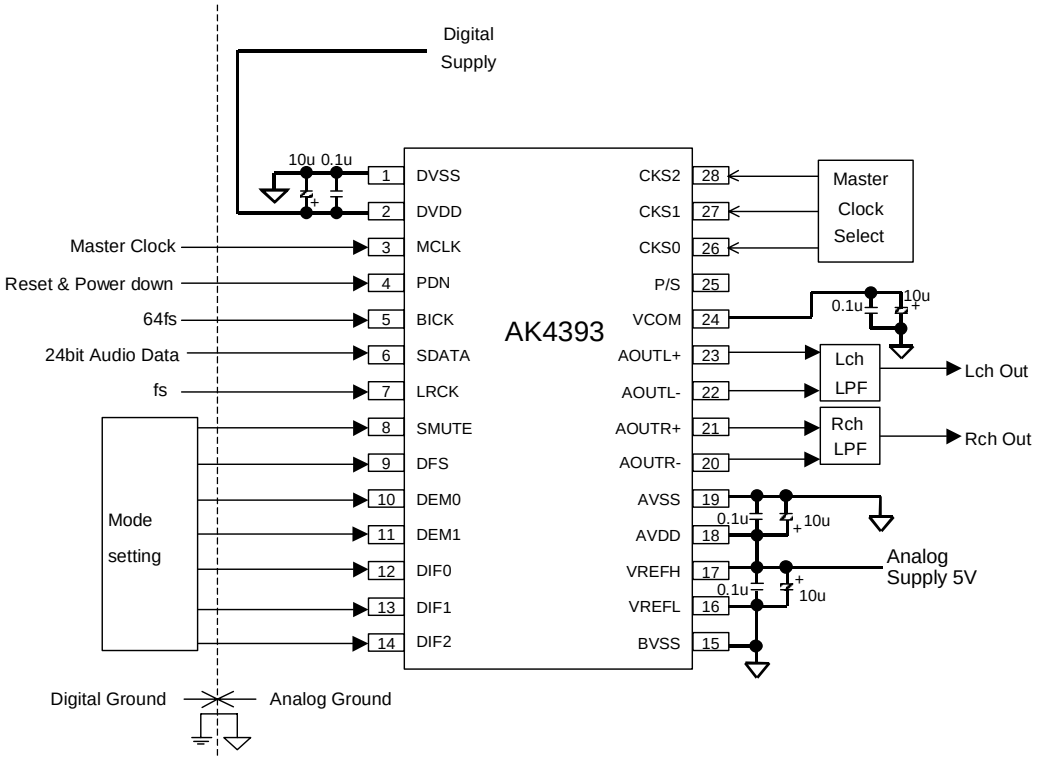


Figure 9. Typical Connection Diagram (Parallel mode)

Notes:

- LRCK = fs, BICK = 64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS, BVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

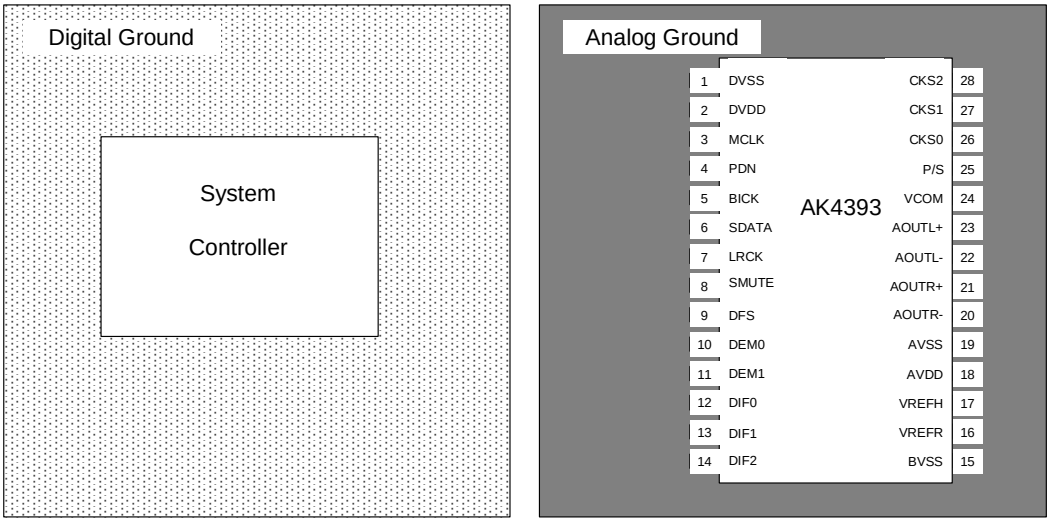


Figure 10. Ground Layout

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from digital supply in system. If AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS, BVSS and DVSS must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible.

2. Voltage Reference

The differential Voltage between VREFH and VREFL set the analog output range. VREFH pin is normally connected to AVDD and VREFL pin is normally connected to AVSS. VREFH and VREFL should be connected with a 0.1µF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH, VREFL and VCOM pins in order to avoid unwanted coupling into the AK4393.

3. Analog Outputs

The analog outputs are full differential outputs and 2.4Vpp (typ@VREF=5V) centered around VCOM. The differential outputs are summed externally, V_{AOUT} = (AOUT+) - (AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 4.8Vpp (typ@VREF=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage (V_{AOUT}) is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal V_{AOUT} is 0V for 000000H(@24bit).

The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

Figure 11 shows an example of external LPF circuit summing the differential outputs by an op-amp.
Figure 12 shows an example of differential outputs and LPF circuit example by three op-amps.

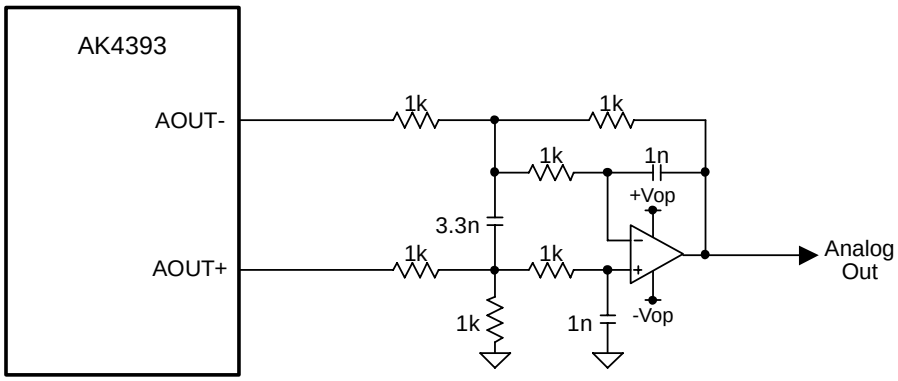


Figure 11. External LPF Circuit Example 1

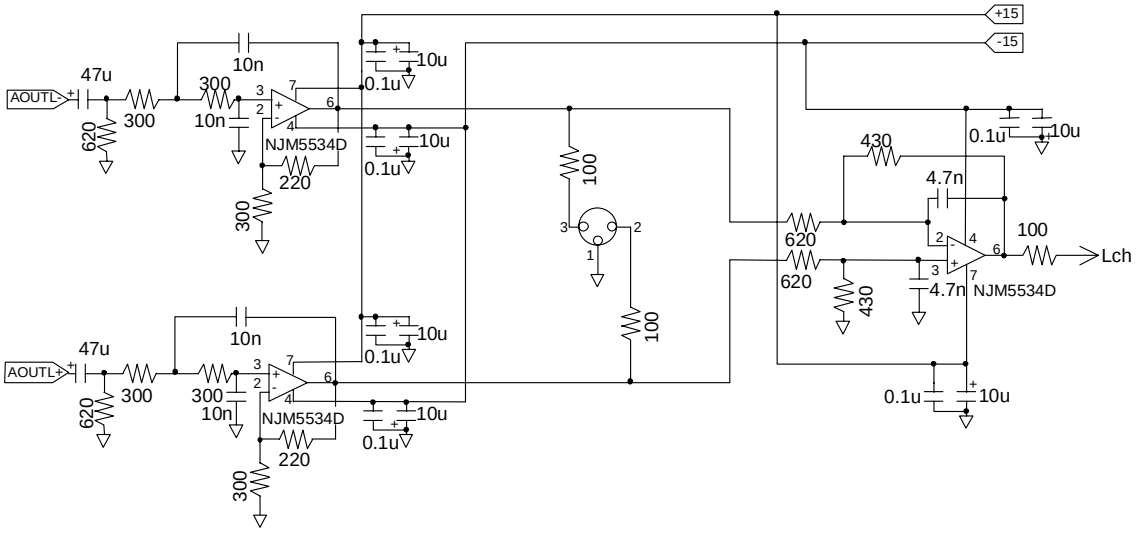
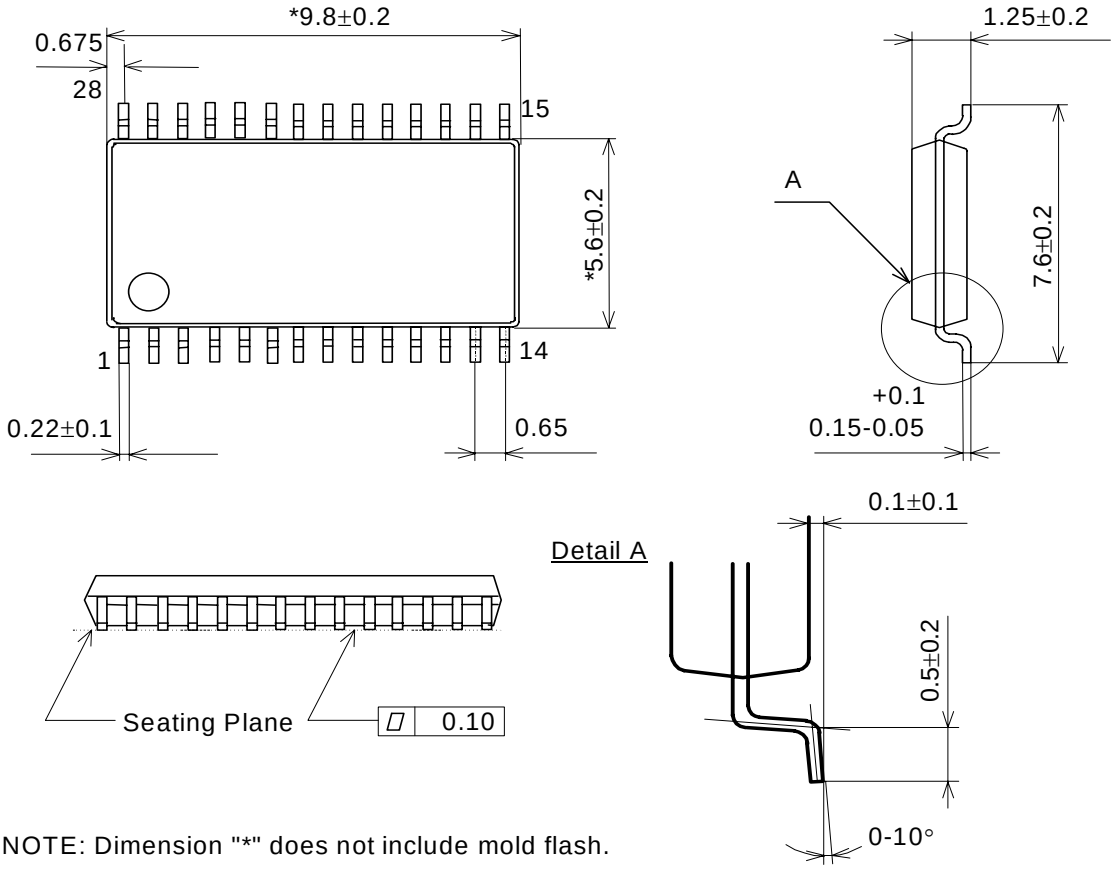


Figure 12. External LPF Circuit Example 2

PACKAGE

28pin VSOP (Unit: mm)

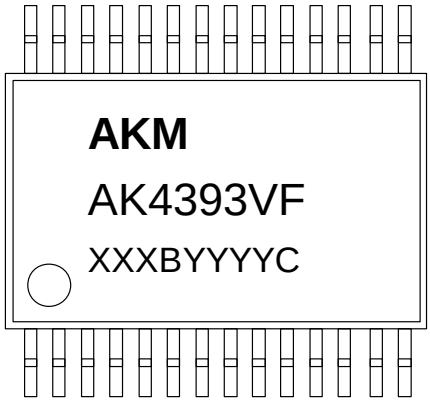


NOTE: Dimension "*" does not include mold flash.

■ **Material & Lead finish**

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

MARKING



XXXXBYYYYC data code identifier

XXXB: Lot number (X : Digit number, B : Alpha character)
YYYYC: Assembly date (Y : Digit number C : Alpha character)

Appendix A

In Double Speed Mode, the phase relationship between MCLK and LRCK/BICK is limited (Table 7). If the phase relationship happens during this prohibited period, it is possible to occur the inverse of output channel. The phase relationship must be set to avoid the prohibited period when the AK4393 operates at Double Speed Mode. The prohibited period is specified by the combination of digital power supply voltage (DVDD), MCLK frequency and audio data format (Table 5). When the audio data formats are 16/20/24bit LSB Justified (Mode 0,1,4) and 24bit MSB Justified (Mode 2), the phase relationship (tLRM: Figure 11) between the rising edge of LRCK and the rising edge of MCLK has the prohibited period of min to max in Table 7. In case of I^2S Compatible (Mode 3), the relationship between the falling edge of BICK and the rising edge of MCLK has the prohibited period (tBCM: Figure 12)

Sampling Mode	Digital Power Supply, DVDD	MCLK Frequency	Mode Setting				Prohibited Period		Units
			CKS2	CKS1	CKS0	DFS	min	max	
Double Speed	3.0 to 5.25V	128fs	0	0	0	1	0.4	1.7	ns
Double Speed	3.0 to 5.25V	192fs	0	1	0	1	-0.5	0.8	ns
Double Speed	3.0 to 5.25V	256fs	0	0	1	1	-0.7	0.7	ns
Double Speed	3.0 to 5.25V	256fs	1	0	0	1	-0.7	0.7	ns
Double Speed	3.0 to 5.25V	384fs	0	1	1	1	-1.7	-0.3	ns
Double Speed	3.0 to 5.25V	384fs	1	1	0	1	-1.7	-0.3	ns
Double Speed	4.75 to 5.25V	128fs	0	0	0	1	0.8	1.5	ns
Double Speed	4.75 to 5.25V	192fs	0	1	0	1	-0.2	0.5	ns
Double Speed	4.75 to 5.25V	256fs	0	0	1	1	-0.3	0.4	ns
Double Speed	4.75 to 5.25V	256fs	1	0	0	1	-0.3	0.4	ns
Double Speed	4.75 to 5.25V	384fs	0	1	1	1	-1.0	-0.3	ns
Double Speed	4.75 to 5.25V	384fs	1	1	0	1	-1.0	-0.3	ns

Table **7**. Prohibited Period

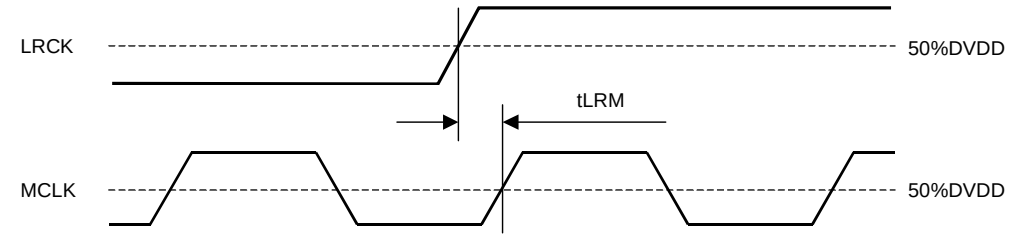


Figure 11. 16/20/24bit LSB Justified, 24bit MSB Justified

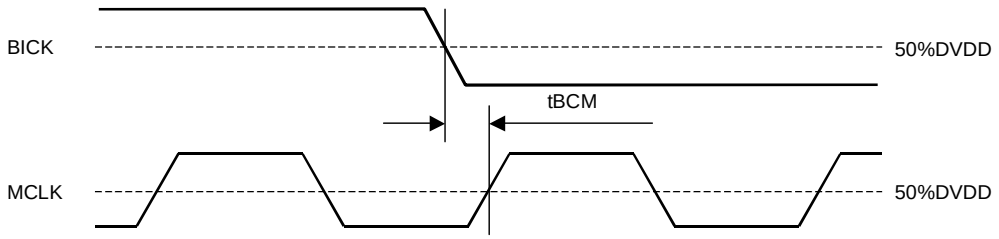
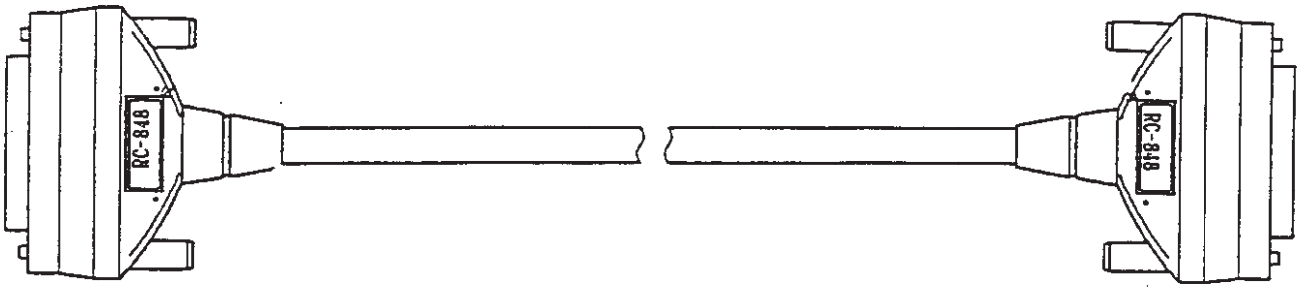


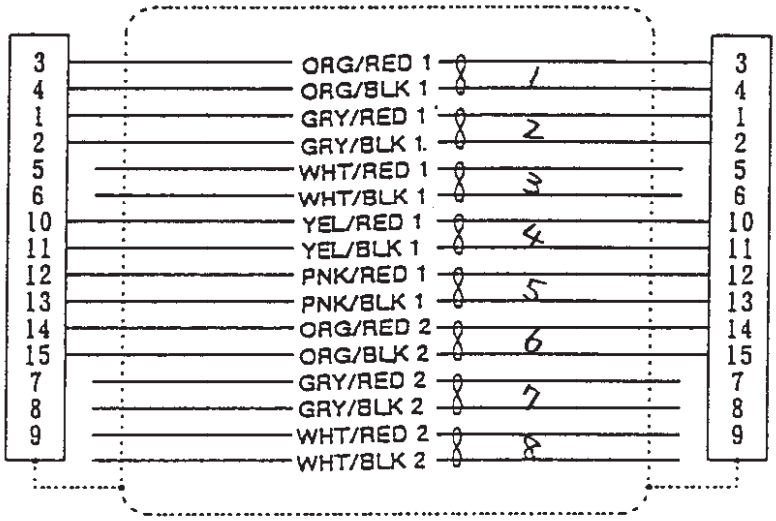
Figure 12. I^2S Compatible

THE CABLES FOR REMOTE

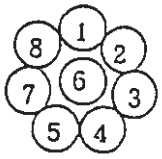


Female

Male

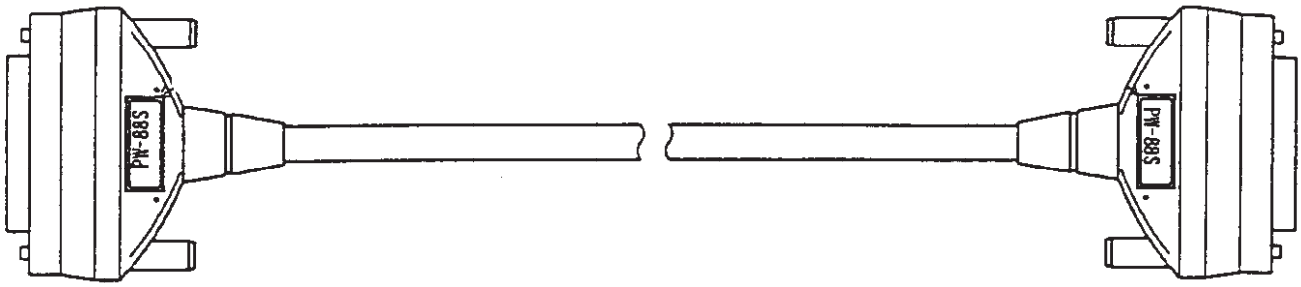


means Twisted wire

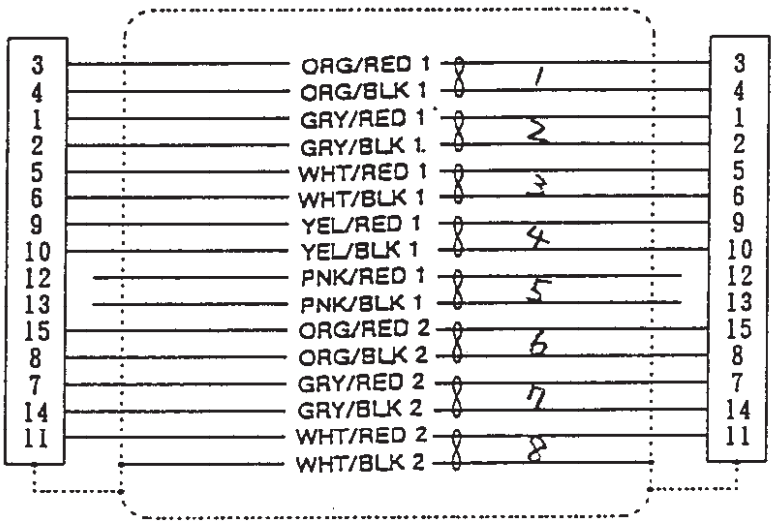


1 pce.	5336 3570-00	Connector Plug, 15 pin D-Sub (Male)
1 pce.	1315 2907-	Connector Socket, 15 pin D-Sub (Female)
2 pcs.	5336 3580-00	Case Assy, 15 pin D-Sub

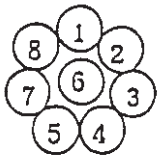
THE CABLES FOR SYNC



Male Male

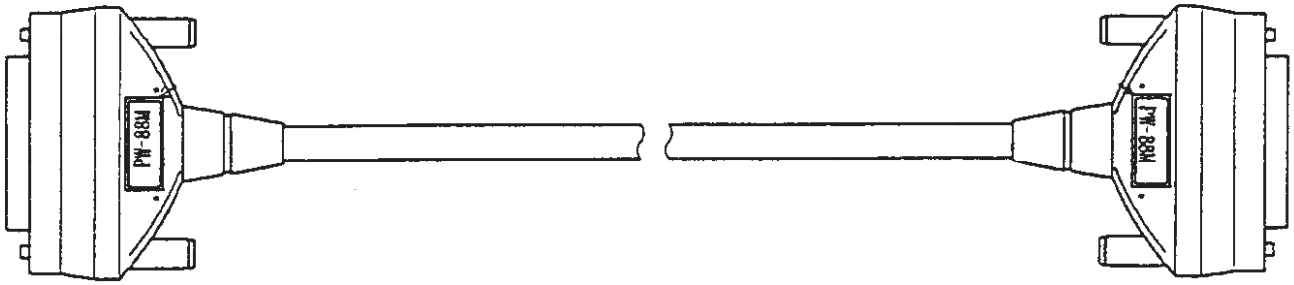


means Twisted wire

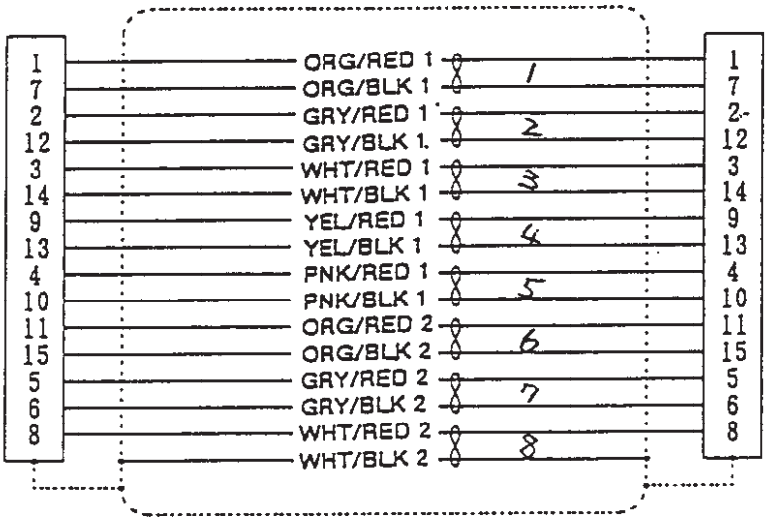


2 pcs.	5336 3570-00	Connector Plug, 15 pin D-Sub (Male)
2 pcs.	5336 3580-00	Case Assy, 15 pin D-Sub

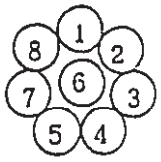
THE CABLES FOR METER



Female Male

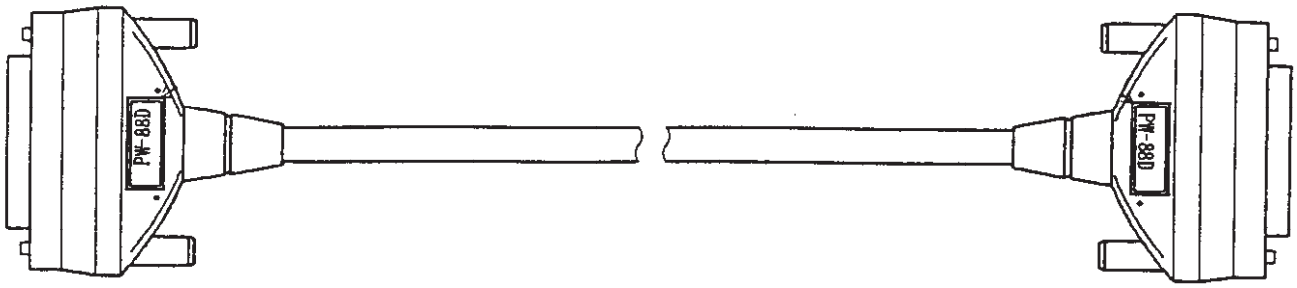


means Twisted wire

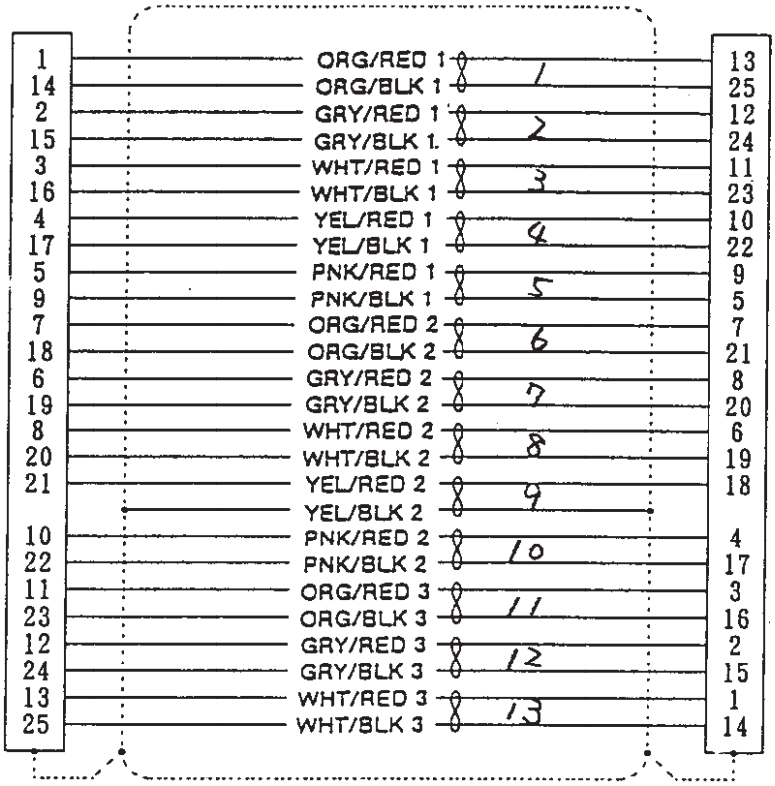


1 pce.	5336 3570-00	Connector Plug, 15 pin D-Sub (Male)
1 pce.	1315 2907-	Connector Socket, 15 pin D-Sub (Female)
2 pcs.	5336 3580-00	Case Assy, 15 pin D-Sub

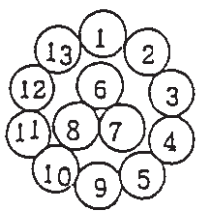
THE CABLES FOR TDIF



Male Male



means Twisted wire



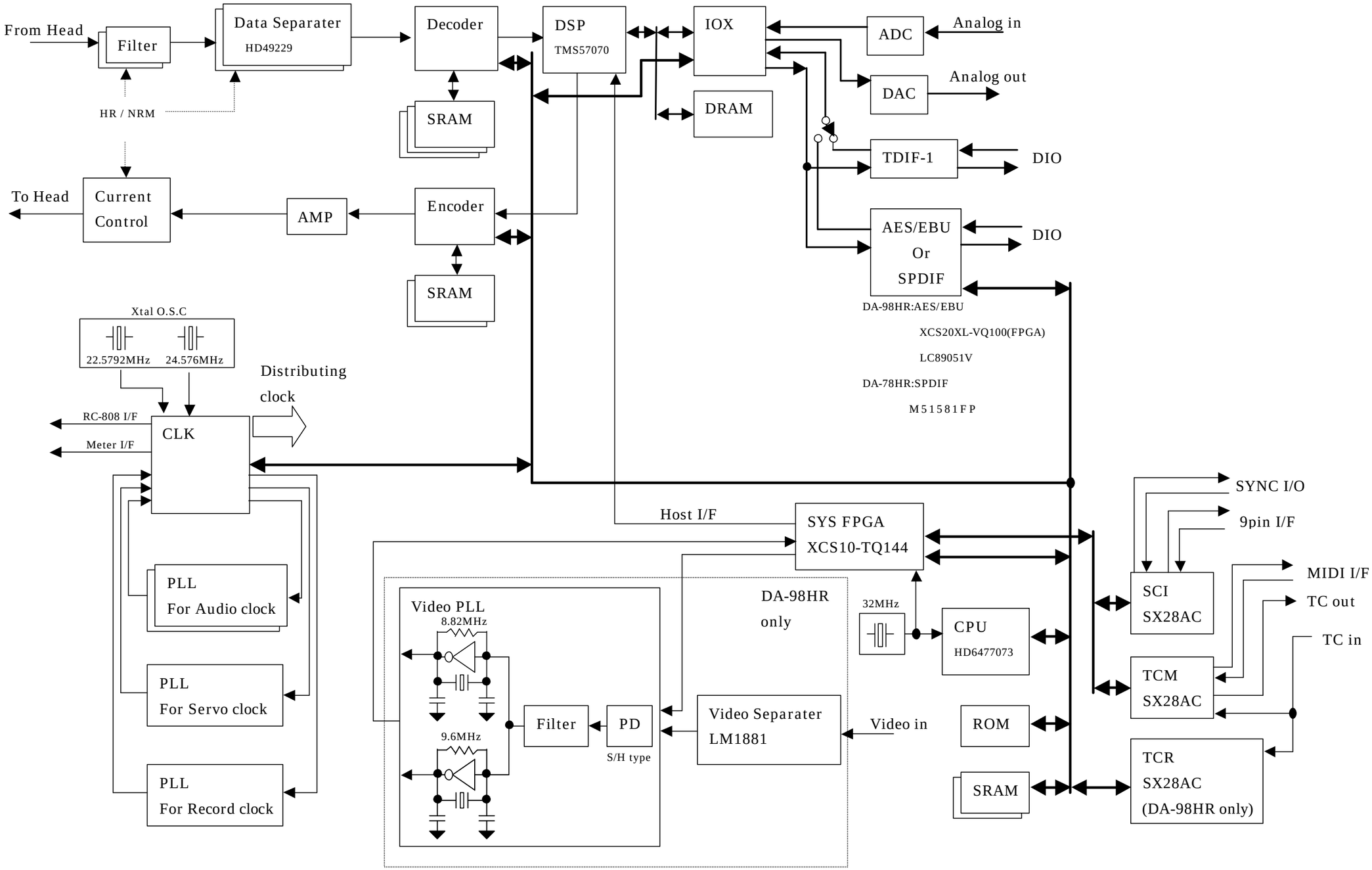
2 pcs.	1315 2908-	Connector Plug, 25 pin D-Sub (Male)
2 pcs.	5336 3581-00	Case Assy, 25 pin D-Sub

DA-78HR, Error Message

Message		Problem	Solution
E CLOC	error : clock	No signal from clock source or different Fs.	Check source unit, Fs setting.
E dio	error : digital I/O	Even if “digital” is selected at “Input Patch bay”, there is no digital input at that track. In case Fs is different, Fs LED will blink.	
E deu	error : deu	Condensation on drum.	Leave the unit for 1-2 hours with powering on.
E EmP	error : emphasys	DA-78HR cannot record the digital audio signal with the emphasis.	
E Hi-8t	error : high eight tape	Tape other than Hi8 is loaded.	Use Hi8 tape.
E no mSt	error : no master	No time data coming from the master.	
E no tC	error : no TC	Tape TC is not present. TC is not recorded in case of “tape TC”=”TC track”. Tape is not formatted or no TC record source in case of “Ttape TC” = conv ABS”. Generator is not running incase of “src”= “generator” External TC is not fed incase of “src”=”EXT”. TC cannot be read incase of “src”=”tape TC” and “Tape TC”=”TC track”. If above error is occurring, TC recording will continue affecting previous TC data.	
E t cut	error : tape cut	Tape is cut.	
E thint	error : thin tape	Thin tape is loaded. Thin tape: Thickness= less than 8.5 um.	
Err dSP	error : DSP	Main CPU cannot communicate with DSP.	
Err Frm	error : TC frame	External timecode and the system frame of the DA-78HR do not match.	Confirm the frame rate of external TC and the system frame of the DA-78HR.
Low btry	low battery	Backup battery is getting lower.	
not Sync	not synchronized	External TC being recorded is not synchronizing to digital audio clock.	

Servo Error xx

S-Err.00	Main CPU cannot communicate with Servo CPU.
S-Err.04	The capstan motor could not work correctly in time.
S-Err.11	Unable to shift mechanism mode within the five seconds of command reception.
S-Err.02	The drum motor could not work correctly in time.
S-Err.08	The reel motor could not work correctly in time
S-Err.59	
S-Err.68	
S-Err.21	Tape is not wound into cassette half even Eject is commanded.
S-Err.41	Unable to latch solenoid on FF/REW winding.
S-Err.31	Occurrence of tape slack during tape runs


From Head
Filter
Data Separater
HD49229
Decoder
DSP
TMS57070
IOX
ADC
Analog in
DAC
Analog out
DRAM
SRAM
HR / NRM
TDIF-1
DIO
To Head
Current
Control
AMP
Encoder
AES/EBU
Or
SPDIF
DIO
SRAM
DA-98HR:AES/EBU
XCS20XL-VQ100(FPGA)
LC89051V
DA-78HR:SPDIF
M51581FP
Xtal O.S.C
22.5792MHz
24.576MHz
Distributing
clock
RC-808 I/F
Meter I/F
CLK
PLL
For Audio clock
PLL
For Servo clock
PLL
For Record clock
Host I/F
SYS FPGA
XCS10-TQ144
SYNC I/O
9pin I/F
MIDI I/F
TC out
TC in
SCI
SX28AC
TCM
SX28AC
TCR
SX28AC
(DA-98HR only)
DA-98HR
only
32MHz
CPU
HD6477073
ROM
SRAM
Video PLL
8.82MHz
9.6MHz
Filter
PD
S/H type
Video Separater
LM1881
Video in

AK5383

24-Bit, 96kHz Analog-to-Digital Converter

Features

- Proprietary dual-bit delta-sigma (ΔΣ) architecture
- Sampling rate from 1kHz to 108kHz
- Full differential inputs
- Dynamic range = 110dB
- Signal-to-noise = 110dB
- Signal-to-(Noise + Distortion) = 103dB
- On-chip linear phase digital anti-alias filter
  - Passband from 0 to 21.768kHz at fs = 48kHz
  - Ripple = 0.001dB
  - Stopband attenuation = 110dB
- Selectable digital HPF or offset calibration
- Power supplies
  - Analog: 5V ± 5%
  - Digital: from 3V to 5.25V
- Low power dissipation: 210mW
- Small 28-pin SOP package
- Pin compatible with the AK5391, AK5392, and AK5393

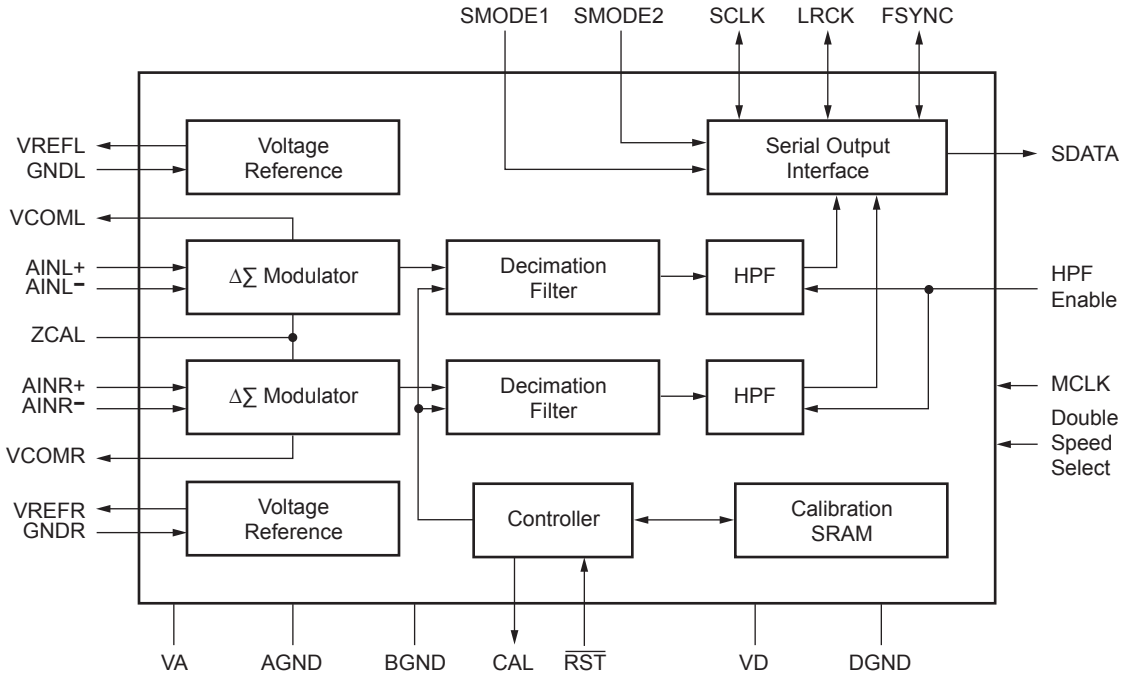
Description

The AK5383 is a 24-bit, 96kHz stereo Analog-to-Digital Converter (ADC) that offers up to 110dB of dynamic range and a 103dB Signal-to-(Noise + Distortion) Ratio. The improved dynamic range and lowered distortion are achieved using an innovative dual-bit ΣΔ architecture that reduces power consumption and improves reliability.

The AK5383 include full differential inputs for maximum signal range and performance. It also includes a reference filter and a digital decimation filter to minimize application requirements for anti-aliasing filtering. The user can select an internal HPF to eliminate DC inputs or offset calibration. The AK5383 outputs data at up to 108kHz, in several selectable formats.

The AK5383 is available in a space-saving 28-pin SOP package, and it operates over the full commercial temperature range: –10˚C to 70˚C.

Block Diagram



ASAHI KASEI MICROSYSTEMS CO., LTD.

Performance Specifications

Analog Characteristics

Ta = 25°C, VA = 5.0V, VD = 3.3V, AGND= SGND = DGND = 0V, fs = 48kHz, Signal Frequency = 1kHz, 24-bit output, and measurement frequency = 10Hz to 20kHz, unless otherwise specified.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Resolution				24	Bits
Analog Input Characteristics					
Dynamic Range	-60dBFS, A-Weighted	105	110		dB
Signal-to-Noise Ratio	A-Weighted	105	110		dB
Signal-to-(Noise + Distortion) Ratio	-1dBFS	96	103		dB
	-20dBFS		87		
	-60dBFS		47		
	-1dBFS, fs = 96kHz[1]	93	100		
	-20dBFS, fs = 96kHz[1]		81		
	-60dBFS, fs = 96kHz[1]		41		
Interchannel Isolation		110	120		dB
Interchannel Gain Mismatch			0.1	0.5	dB
Gain Drift				150	ppm/°C
Offset Error After Calibration	HPF = Off		±200	±1000	LSB[2]
	HPF = On		±1		
Offset Drift	HPF = Off		±10		LSB/°C
Offset Calibration Range	HPF = Off		±50		mV
Input Voltage	(AIN+) - (AIN-)	±2.3	±2.45	±2.6	V
Input Impedance		8	14		kΩ
Power Supplies					
Analog Power Supply Current			38	54	mA
Digital Power Supply Current			6	9	mA
	fs = 96kHz		9	14	
Power Dissipation			210	300	mW
Power Supply Rejection[3]			70		dB

Digital Characteristics

Ta = 25°C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Input					
High-Level Input Voltage		0.7VD			V
Low-Level Input Voltage				0.3VD	V
Input Leakage Current				±10	µA
Output					
High-Level Output Voltage	Iout = -20µA	VD - 0.1			V
Low-Level Output Voltage	Iout = 20µA			0.1	V

Performance Specification (Continued)

Filter Characteristics—fs = 48kHz

fs = 48kHz, Ta = 25˚C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V, DFS = Low.

Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
ADC Digital Filter (Decimation LPF)						
PB	Passband[4]		0		21.768	kHz
SB	Stopband[4]		26.232			kHz
PR	Passband Ripple				±0.001	dB
SA	Stopband Attenuation[5]		110			dB
GD	Group Delay[6]			38.7		1/fs
ΔGD	Group Delay Distortion			0		μs
ADC Digital Filter (HPF)						
FR	Frequency Response[4]	-3dB		1.0		Hz
		-0.5dB		2.9		
		-0.1dB		6.5		

Filter Characteristics—fs = 96kHz

fs = 96kHz, Ta = 25˚C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V, DFS = High.

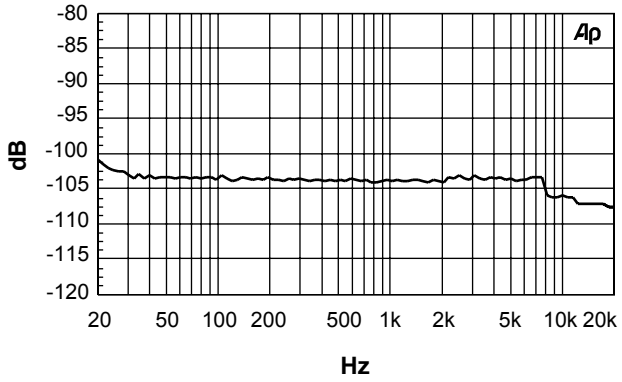
Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
ADC Digital Filter (Decimation LPF)						
PB	Passband[4]		0		43.536	kHz
SB	Stopband[4]		52.464			kHz
PR	Passband Ripple				±0.003	dB
SA	Stopband Attenuation[7]		110			dB
GD	Group Delay[6]			38.8		1/fs
ΔGD	Group Delay Distortion			0		μs
ADC Digital Filter (HPF)						
FR	Frequency Response[4]	-3dB		2.0		Hz
		-0.1dB		13.0		

Notes:

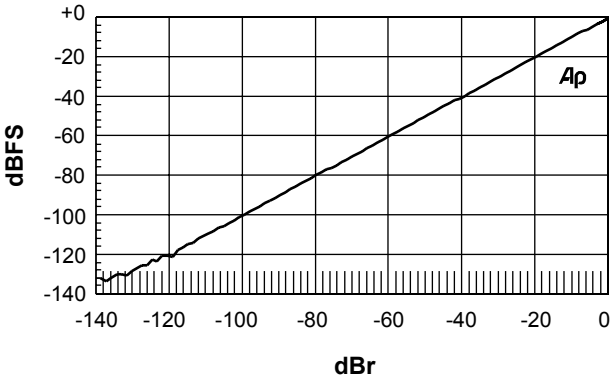
1. When fs = 96kHz, a measurement bandwidth of 40kHz is used.
2. LSB refers to the Least Significant Bit of the 24-bit output data.
3. The Power Supply Rejection ratio is measured with a 1kHz, 20mV_{P-P} input to VA and VD. VREFH is held at a constant voltage.
4. The passband and stopband frequencies are proportional to fs.
5. The analog modulator samples the input at 6.144MHz for 48kHz output. There is no rejection of input signals which are multiples of the sampling frequency. That is, there is no rejection for signals of the following frequencies:
   n x 6.144MHz ± 21.768kHz, where n = 1, 2, 3, 4, ...
6. The Group Delay is the calculated delay time which takes place due to the digital filtering process. This time is taken from when the analog signal is input, to the time of setting the 24-bit data (from both channels) to the output register. When the HPF is on, this time is typically 40.7/fs if the DFS pin is Low, and 40.8/fs if the DFS pin is High.
7. The analog modulator samples the input at 6.144MHz for 96kHz output. There is no rejection of input signals which are multiples of the sampling frequency. That is, there is no rejection for signals of the following frequencies:
   n x 6.144MHz ± 43.536kHz, where n = 1, 2, 3, 4, ...

Typical Performance Curves

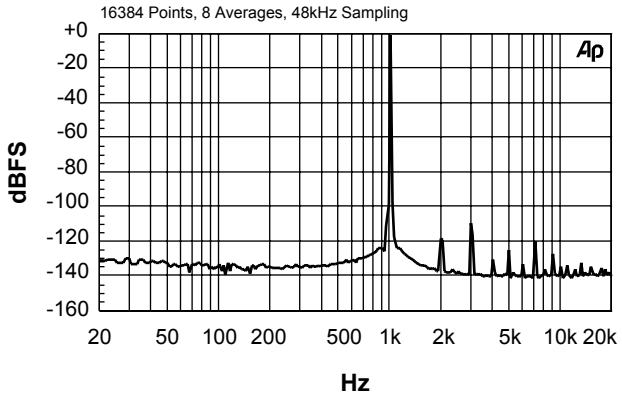
THD + N vs. Frequency



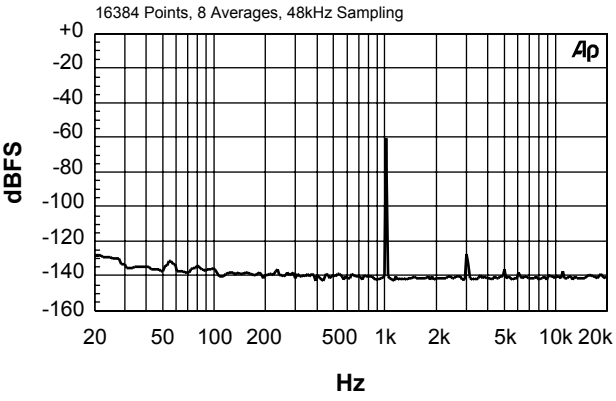
Linearity



0dB FFT



-60dB FFT



Absolute Maximum Ratings

AGND, SGND, and DGND = 0V. All voltages are with respect to ground.

Parameter		Min.	Max.	Units
Power Supplies				
VA	Analog Power Supply	-0.3	6.0	V
VD	Digital Power Supply	-0.3	6.0	V
ΔGND[1]	|SGND - DGND|		0.3	V
IIN	Input Current—All pins except supply pins		±10	mA
VINA	Analog Input Voltage	-0.3	VA + 0.3	V
VIND	Digital Input Voltage	-0.3	VD + 0.3	V
Temperature				
Ta	Ambient Operating Temperature (Power Applied)	-10	70	°C
Tstg	Storage Temperature	-65	150	°C

Note:

1. AGND and SGND must be at the same voltage.

Caution:
Exceeding minimum and maximum ratings may result in damage to the device.

Recommended Operating Conditions

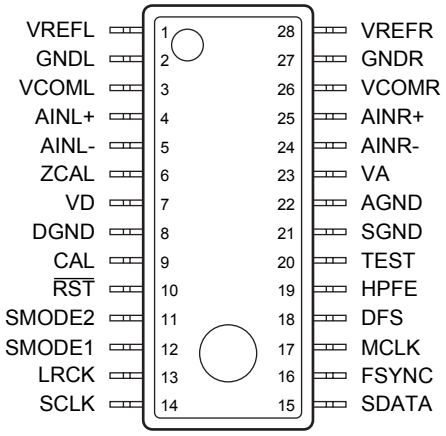
AGND, SGND, and DGND = 0V. All voltages are with respect to ground.

Parameter		Min.	Typ.	Max.	Units
Power Supplies[1]					
VA	Analog Power Supply	4.75	5.0	5.25	V
VD	Digital Power Supply	3.0	3.3	5.25	V

Note:

1. The VA and VD power-up sequences are not critical.

Pin Descriptions



Note:
See Table 1 for compatibility with other AKM devices.

Pin Descriptions

No.	Pin Name	I/O	Pin Function and Description
1	VREFL	O	**Left Channel Reference Voltage.** VREFL = 3.75V. This pin is normally connected to the GNDL pin through a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor in parallel. Refer to the Design Considerations section for additional information.
2	GNDL	-	**Left Channel Reference Ground.** GNDL = 0V.
3	VCOML	O	**Left Common Voltage.** VCOML = 2.75V.
4	AINL+	I	**Left Channel Analog Positive Input.**
5	AINL-	I	**Left Channel Analog Negative Input.**
6	ZCAL	I	**Zero Calibration Control.** This pin controls the calibration reference signal. When ZCAL is Low, the VCOML and VCOMR are selected. When High, the analog inputs (AINL+, AINL-, AINR+, and AINR-) are used for the reference level.
7	VD	-	**Digital Power Supply.** VD = 3.3V.
8	DGND	-	**Digital Ground.** DGND = 0V.
9	CAL	O	**Calibration Active Signal.** When this pin outputs a High signal, it shows that the offset calibration cycle is in progress. The offset calibration cycle starts when the RST pin goes High. The CAL pin goes Low after 8704 clock cycles when DFS is Low or after 17408 cycles when DFS is High.
10	$\overline{\text{RST}}$	I	**Reset.** When this pin is Low, the digital section is powered down. When this pin returns to High, an offset calibration cycle starts. An offset calibration cycle should always be initiated upon powering up the device.
11	SMODE2	I	**Serial Interface Mode Select.** The serial interface mode data should always be MSB first, 2's complement formatted. See Table 3 for these pin definitions.
12	SMODE1	I	
13	LRCK	I/O	**Left Channel and Right Channel Select Clock.** During reset—when the SMODE1 pin is High—the LRCK pin goes High when the SMODE2 pin is Low, and the LRCK pin goes Low when the SMODE2 pin is High.
14	SCLK	I/O	**Serial Data Clock.** Data is clocked on the falling edge of SCLK. In the slave mode, the SCLK pin requires a clock greater than 48fs. In the master mode, this pin outputs a 128fs (when DFS is Low) clock or a 64fs clock. SCLK is Low during reset.
15	SDATA	O	**Serial Data Output.** Serial data output is MSB first and 2's complement formatted. This pin is low during reset.
16	FSYNC	I/O	**Frame Synchronization Signal.** In slave mode, when FSYNC is High, the data bits are clocked on SDATA. In the master mode, FSYNC outputs a 2fs clock and it is Low during reset.

Pin Descriptions (Continued)

No.	Pin Name	I/O	Pin Function and Description
17	MCLK	I	**Master Clock Input.** Set the DFS pin Low for a 256fs input clock. Set the DFS pin High for a 128fs clock.
18	DFS	I	**Double Speed Sampling Mode.** When this pin is Low, the chip is in normal speed mode. When High, the double speed mode is selected.
19	HPFE	I	**High Pass Filter Enable.** When this pin is High, the high pass filter is enabled. When Low, this pin is disabled.
20	TEST	I	**Test.** This pin should be connected to ground.
21	SGND	-	**Substrate Ground.** SGND = 0V.
22	AGND	-	**Analog Ground.** AGND = 0V.
23	VA	-	**Analog Power Supply.** VA = 5V.
24	AINR-	I	**Right Channel Analog Negative Input.**
25	AINR+	I	**Right Channel Analog Positive Input.**
26	VCOMR	O	**Right Common Voltage Pin.** VCOMR = 2.75V.
27	GNDR	-	**Right Channel Reference Ground**. GNDR = 0V.
28	VREFR	O	**Right Channel Reference Voltage.** VREFR = 3.75V. This pin is normally connected to the GNDR pin through a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor in parallel. Refer to the Design Considerations section for additional information.

Note:

1. All input pins, except pull-down pins, should not be left floating.

Table 1. AK5383 Compatibility

	AK5383	AK5393	AK5392	AK5391
Pin 2	GNDL	GNDL	GNDL	VREFL-
Pin 18	DFS	DFS	CMODE	CMODE
Pin 19	HPFE	HPFE	HPFE	SEL24
Pin 27	GNDR	GNDR	GNDR	VREFR-
Maximum fs	108kHz	108kHz	54kHz	54kHz
Master Clock at 48kHz	256fs	256fs	256fs or 384fs	256fs or 384fs
Master Clock at 96kHz	128fs	128fs	N/A	N/A
Dynamic Range	110dB	117dB	116dB	113dB
Signal-to-Noise Ratio	110dB	117dB	116dB	113dB
Signal-to-(Noise + Distortion)	103dB	105dB	105dB	97dB

Swithching Characteristics

Ta = 25˚C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V, C_L = 20pF.

Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
Control Clock Frequency						
fCLK	Master Clock Frequency	256fs	0.256	12.288	13.824	MHz
tCLKL	Clock Pulse Width Low		29			ns
tCLKH	Clock Pulse Width High		29			ns
fSLK	Serial Data Output Clock (SCLK) Frequency			6.144	6.912	MHz
fs	Channel Select Clock (LRCK) Frequency		1	48	108	kHz
Duty Cycle			25		75	%
Serial Interface Timing—Slave Mode[1] (SMODE = Low)						
tSLK	SCLK Period		144.7			ns
tSLKL	SCLK Pulse Width Low		65			ns
tSLKH	SCLK Pulse Width High		65			ns
tSLR	SCLK Falling Edge to LRCK Edge	Note 2	-45		45	ns
tDLR	LRCK Edge to SDATA MSB Valid				45	ns
tDSS	SCLK Falling Edge to SDATA Valid				45	ns
tSF	SCLK Falling Edge to FSYNC Edge		-45		45	ns
Serial Interface Timing—Master Mode (SMODE = High)						
tSCLK	SCLK Frequency	DFS = Low		128fs		Hz
		DFS = High		64fs		
SCLK Frequency Duty Cycle				50		%
fFSYNC	FSYNC Frequency			2fs		Hz
FSYNC Frequency Duty Cycle				50		%
tSLR	SCLK Falling Edge to LRCK Edge		-20		20	ns
tLRF	LRCK Edge to FSYNC Rising Edge			1		tSLK
tDSS	SCLK Falling Edge to SDATA Valid				45	ns
tSF	SCLK Falling Edge to FSYNC Edge		-20		20	ns
Reset and Calibration Timing						
tRTW	$\overline{\text{RST}}$ Pulse Width		150			ns
tRCR	$\overline{\text{RST}}$ Falling to CAL Rising Edge				50	ns
tRCF	$\overline{\text{RST}}$ Rising to CAL Falling Edge	Note 3		8704		1/fs
tRTV	$\overline{\text{RST}}$ Rising Edge to SDATA Valid	Note 3		8960		1/fs

Notes:

1. Refer to the Serial Data Interface section.
2. The specified LRCK edges do not coincide with the rising edges of SCLK.
3. tRCF and tRTV specify the number of LRCK rising edges after $\overline{\text{RST}}$ is brought High. This value is given for when the device is operated in master mode. In slave mode, this value is one LRCK clock (1/fs) longer. When the DFS is High, the number of cycles, 1/fs, is doubled.

Timing Diagrams

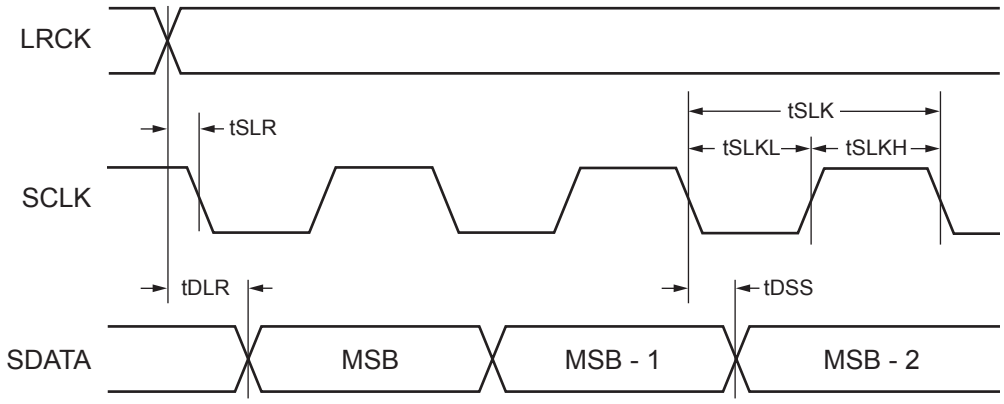


Figure 1. Serial Data Timing (Slave Mode, FSYNC = High)

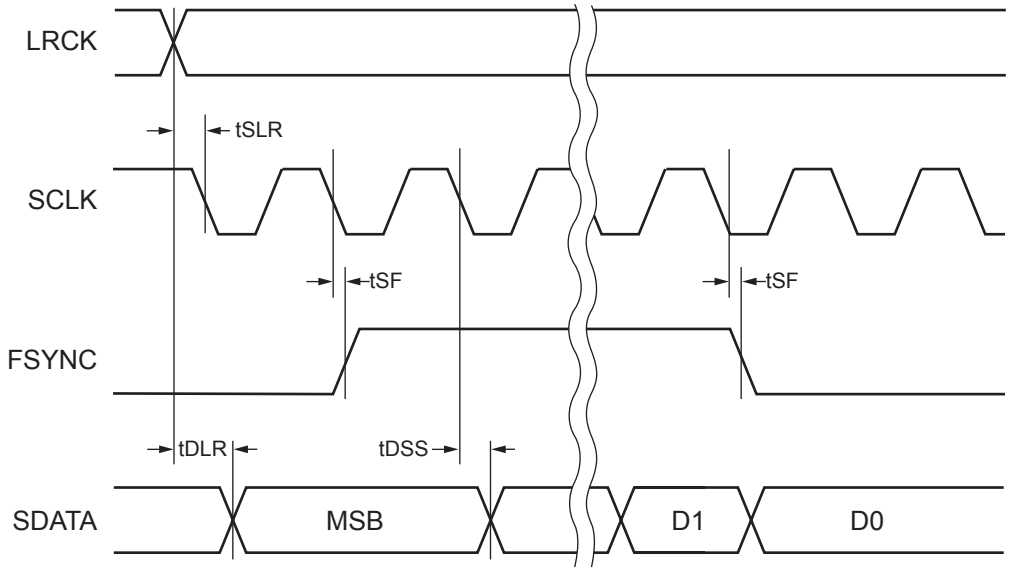


Figure 2. Serial Data Timing (Slave Mode)

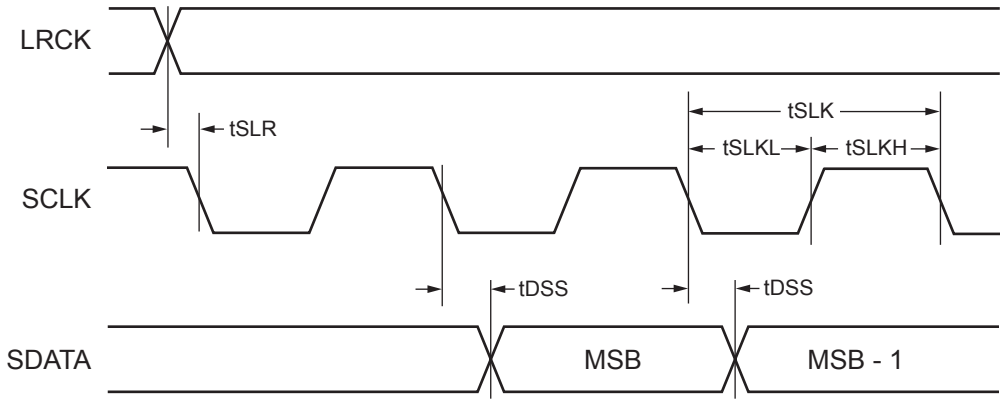


Figure 3. Serial Data Timing (I^2S Slave Mode, FSYNC = Don't Care)

Timing Diagrams (Continued)

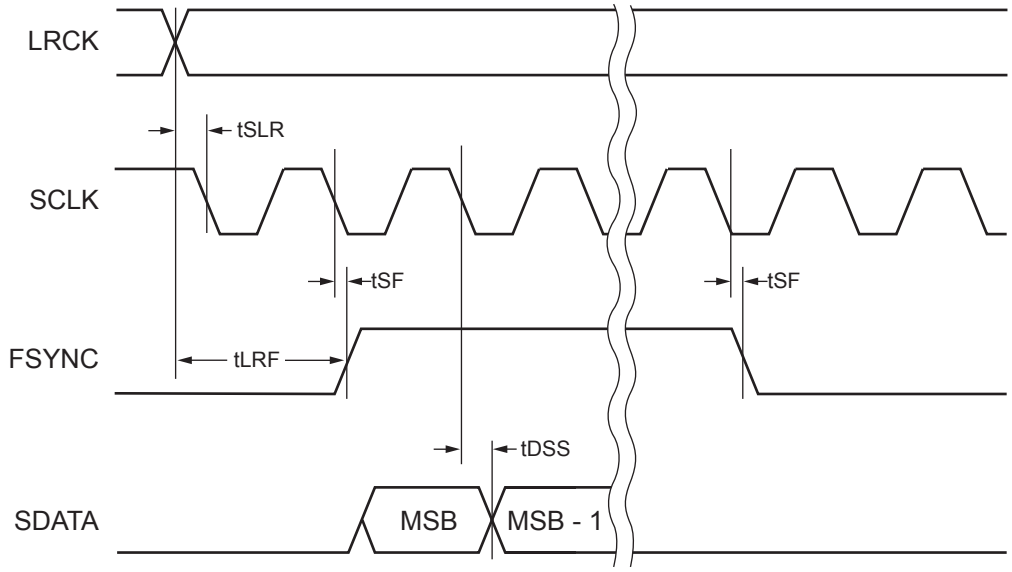


Figure 4. Serial Data Timing (Master Mode and I^2S Master Mode, DFS = Low)

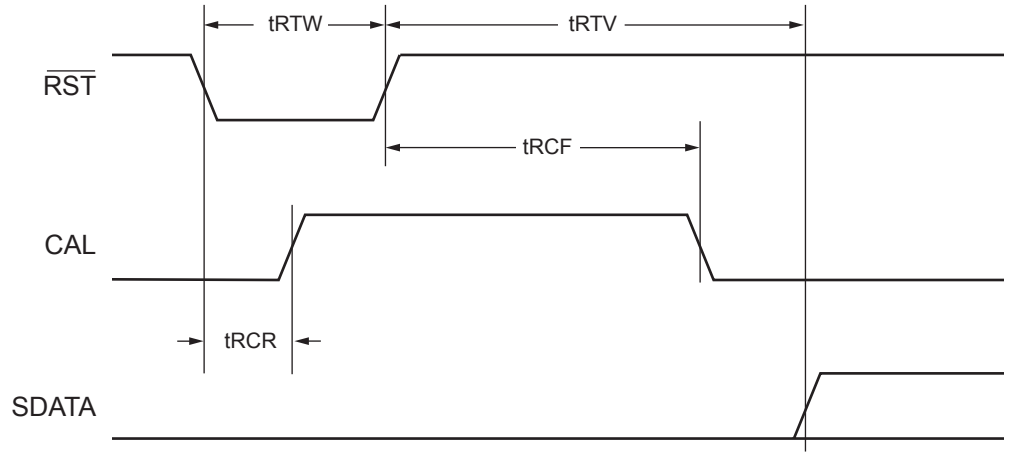


Figure 5. Reset and Calibration Timing

Device Operation

System Clock Input

Three clocks are requiered to operate the AK5383: the Master Clock (MCLK), the Left/Right Channels Select Clock (LRCK), and the Serial Data Clock (SCLK). Refer to Table 1. The MCLK should be synchronized with the LRCK, but the phase is not critical. MCLK should be 256fs when in the normal sampling mode (i.e. DFS = Low), and should be 128fs when in the double sampling mode. Table 2 shows the standard audio word rates and their corresponding frequencies.

Table 1. System Clocks

	Normal Speed (DFS = Low)	Double Speed (DFS = High)
LRCK (maximum)	54kHz	108kHz
BICK	Up to 128fs	Up to 64fs
MCLK	256fs	128fs

Table 2. System Clocks

fs	MCLK	SCLK
32.0kHz	8.1920MHz	4.0960MHz
44.1kHz	11.2896MHz	5.6448MHz
48.0kHz	12.2880MHz	6.1440MHz
96.0kHz	12.2880MHz	6.1440MHz

The AK5383 includes a phase detect circuit for the LRCK; thus, by changing the clock frequencies, the device is reset automatically when synchronization of MCLK on LRCK is not maintained. With this feature, resetting the AK5383 is only needed during power-up.

Ideally, all external clocks—MCLK, BICK, and LRCK—should always be present whenever the AK5383 is in normal operation (that is, when $\overline{RST}$ is High). In real applications, however, one or more of these clocks may not be present for a short amount of time. When this occurs, the AK5383 should be reset by setting the $\overline{RST}$ pin Low, which resets and powers down the device. Once all the clocks have been reinstated, the $\overline{RST}$ pin can again be set High for normal operation, completing the reset procedure.

Caution:
Due to its internal dynamic refresh logic, prolonged periods of time without external clock input may result in damage to the device.

Serial Data Interface

The AK5383 supports four serial data formats which can be selected using the SMODE1 and SMODE2 pins. Refer to Table 3. The data format is MSB first and 2's complement. Figures 6 through 9 show the timing diagrams for the four different types of serial data formats.

Table 3. Serial Interface Formats

Timing Diagram	SMODE2	SMODE1	Mode	LRCK	
				Left Channel	Right Channel
Figure 6	L	L	Slave Mode	H	L
Figure 7	L	H	Master Mode	H	L
Figure 8	H	L	I^2S Slave Mode	L	H
Figure 9	H	H	I^2S Master Mode	L	H

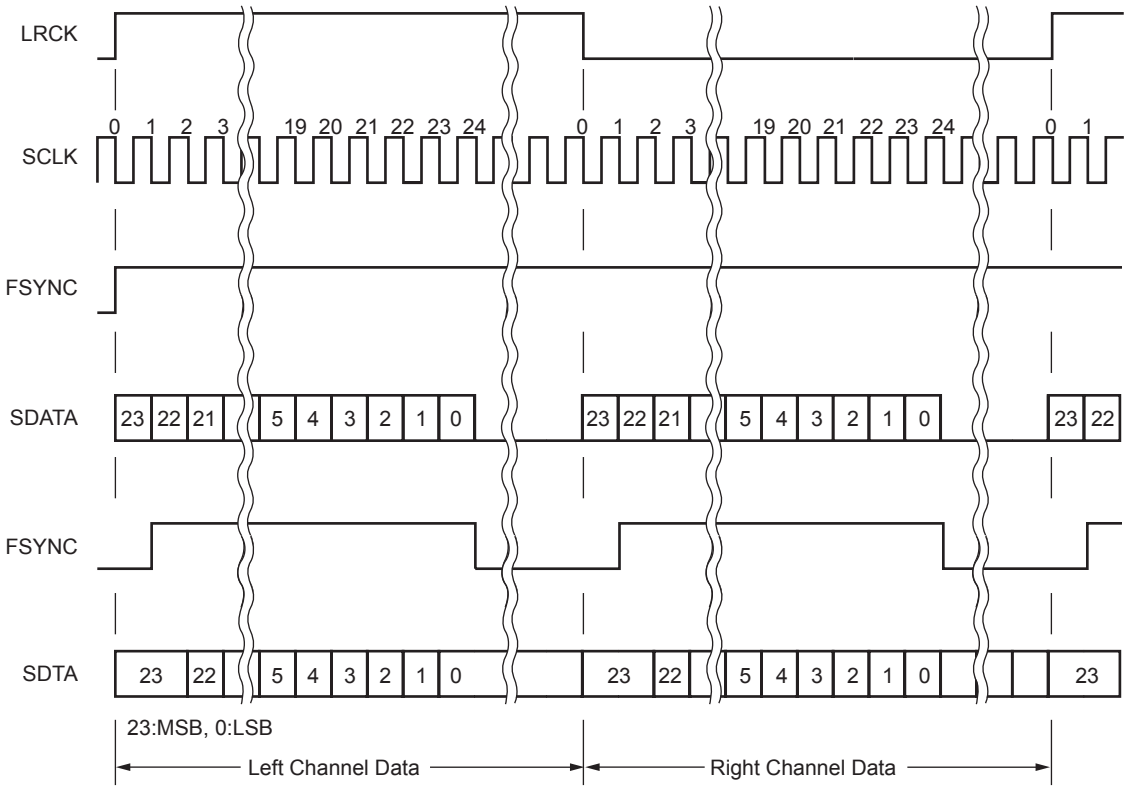


Figure 6. Serial Data Timing—Slave Mode

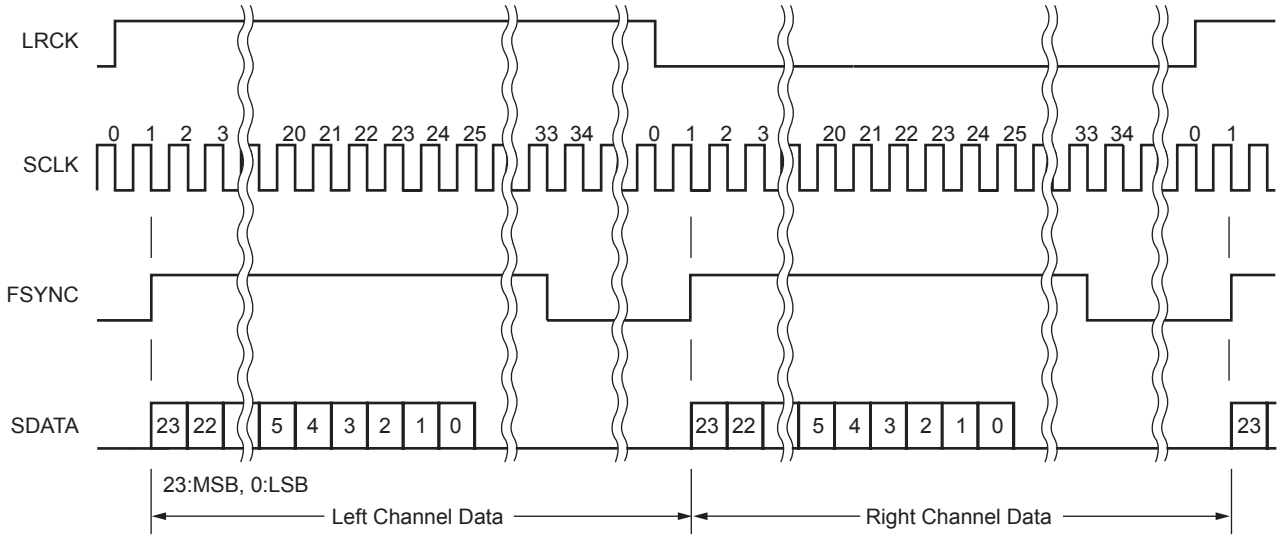


Figure 7. Serial Data Timing—Master Mode (DFS = Low)

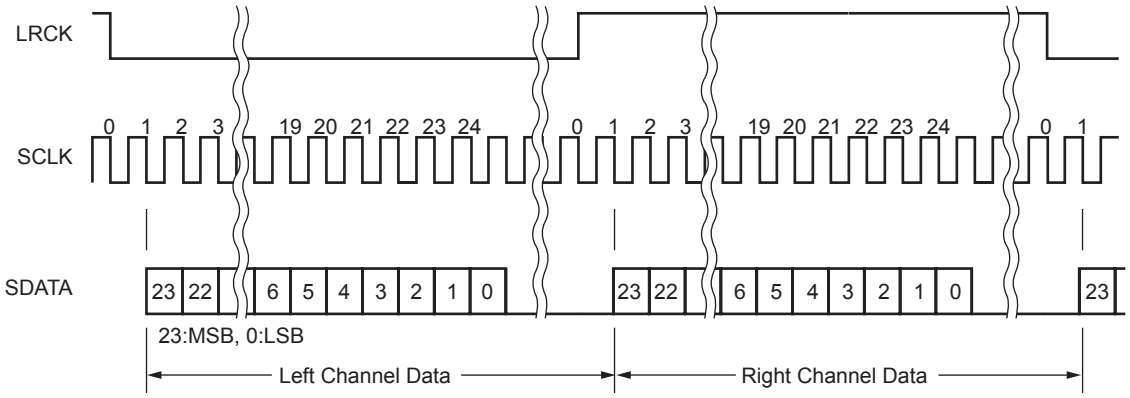


Figure 8. Serial Data Timing—I²S Slave Mode

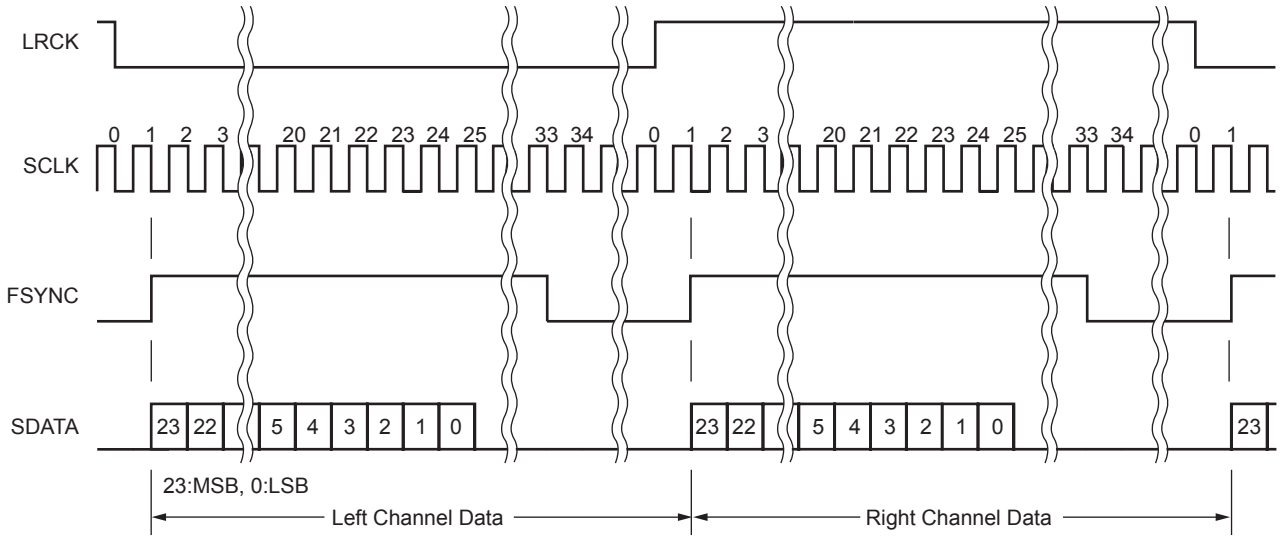


Figure 9. Serial Data Timing—I²S Master Mode (DFS = Low)

Offset Calibration

When the $\overline{\text{RST}}$ pin goes Low, the digital section of the AK5383 is powered down. When this pin returns to High, an offset calibration cycle is started. Such cycle should always be initiated after power-up.

During the offset calibration cycle, the digital section of the AK5383 measures and store the calibration value of each channel into the registers. These calibration values are subtracted from all future outputs. Calibration values may be obtained from the analog input pins (AINL-, AINL+, AINR-, and AINR+) or from the common voltage pins (VCOML and VCOMR) depending on the state of the ZCAL pin. When ZCAL is High, voltages from the analog input pins are measured. When ZCAL is Low, the common voltage pins are measured. The CAL pin is High during calibration.

Digital High Pass Filter

The AK5383 includes a digital High Pass Filter (HPF) used for DC offset cancellation. The cut-off frequency, fc, for the HPF is 1Hz at fs = 48kHz. This frequency also scales with the sampling rate, fs. The cut-off frequency can be calculated by fc = fs/48k.

Design Considerations

Figure 10 shows a system connection diagram. An evaluation board for this device is available, the AKD5383 (see the Ordering Information section). This board demonstrates the applications circuits, an optimum layout, power supply arrangements, and measurement results.

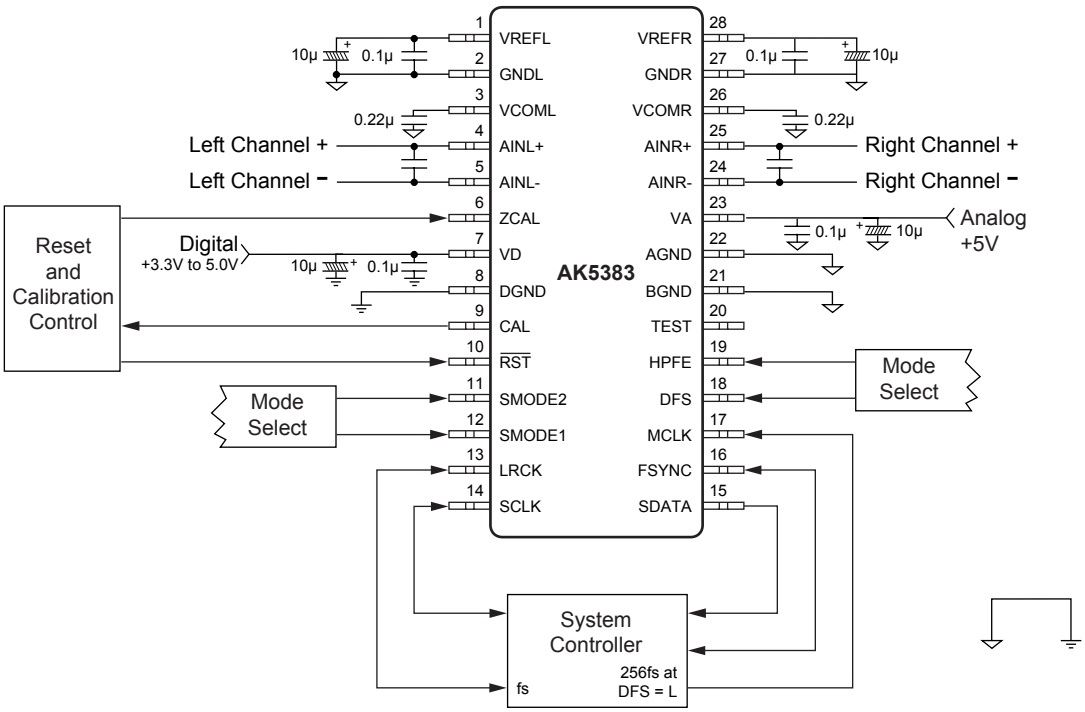


Figure 10. Typical Connection Diagram for Crystal Mode

Grounding and Power Supply Decoupling

Careful attention should be observed for the power supply and grounding of the AK5383. The system's analog and digital grounds are kept separate, but they should be connected together close to where the supplies are brought together into the printed circuit board. The decoupling capacitors should be as close to the AK5383 as possible, with the smaller valued ceramic capacitor being the one nearest to the device.

Voltage Reference and Common Voltage

The AK5383 reference voltage is a differential voltage between the output voltage reference pins (VREFL and VREFR) and the ground pins (GNDL and GNDR). The GNDL and GNDR pins are connected to AGND. In addition, 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor should be connected between the VREFL and GNDL, and between the VREFR and GNDR pins to eliminate the effects of high-frequency noise. It is especially important to place the ceramic capacitors as close to the pins as possible.

All digital signals, especially the clocks, should be kept away from the VREFL and VREFR pins to avoid unwanted coupling with the AK5383. No load current may be drawn from these pins.

The VCOML and VCOMR pins are the common voltages of the analog signals. To eliminate the effects of high-frequency noise, a 0.22µF ceramic capacitor should be connected as close to each of these pins as possible. All signals, especially the clocks, should be kept away from the VCOML and VCOMR pins to avoid unwanted noise coupled into the AK5383. No load current may be drawn from these pins.

Analog Inputs

The AK5383 receives analog signals differentially into the modulator through the analog input pins (AINL-, AINL+, AINR-, and AINR+). Each pin full scale is typically $\pm 2.45V_{P-P}$. The AK5383 can accept input voltages from AGND to VA (that is, from 0V to 5V). The ADC output data is 2's complement. The 24-bit output code is 7FFFFFH for an input signal above a positive full scale, and 800000H for an input signal below a negative full scale. With no input signal, the ideal 24-bit code is 000000H. The DC offset is removed during the offset calibration, or by the HPF in the AK5383.

Internally, the AK5383 samples the analog input signal at 128fs (that is, 6.144MHz at fs = 48kHz when the DFS pin is Low). The digital filter rejects noise above the stop band, except for multiples of 128fs. A simple RC filter may be used to attenuate any noise around 128fs so that most audio signals do not have significant energy at 128fs.

The AK5383 accepts +5V voltage supply. The following conditions should be avoided.

- Any voltage above VA + 0.3V,
- Any voltage below AGND - 0.3V, and
- Any current beyond 10mA for the analog input pins.

Caution:
Excessive currents to the input pins may damage the device. Protect input pins from signals at or beyond the limits stated above, especially if using ±15V in other analog circuits.

Figure 11 shows a fully differential input buffer circuit example with an inverted amplifier (gain = -10dB). The 22nF capacitor between AINL-/AINR- and AINL+/AINR+ decreases the feed through noise of the modulator. The 51Ω resistor has been inserted to stabilize the op-amps before the ADC. This circuit acts also as a LPF with a cut-off frequency of about 140kHz. In this example, the internal offset is removed by self calibration. Refer to the evaluation board data sheet for complete details.

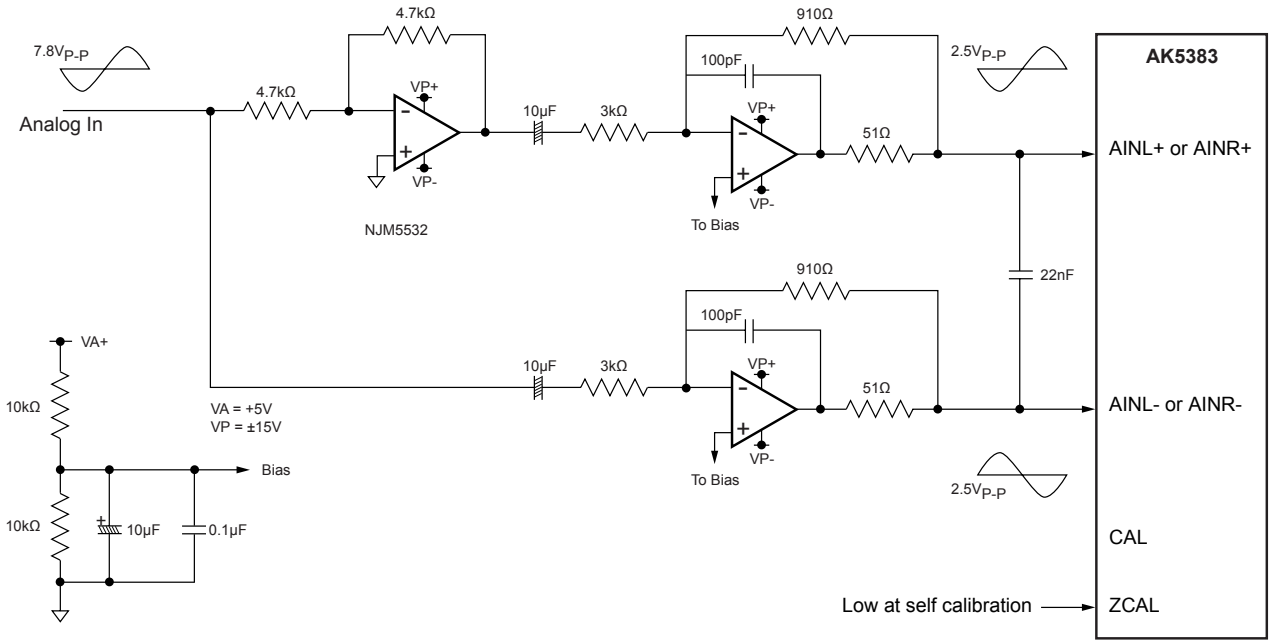


Figure 11. Example of a Differential Input Buffer Circuit

Notes:

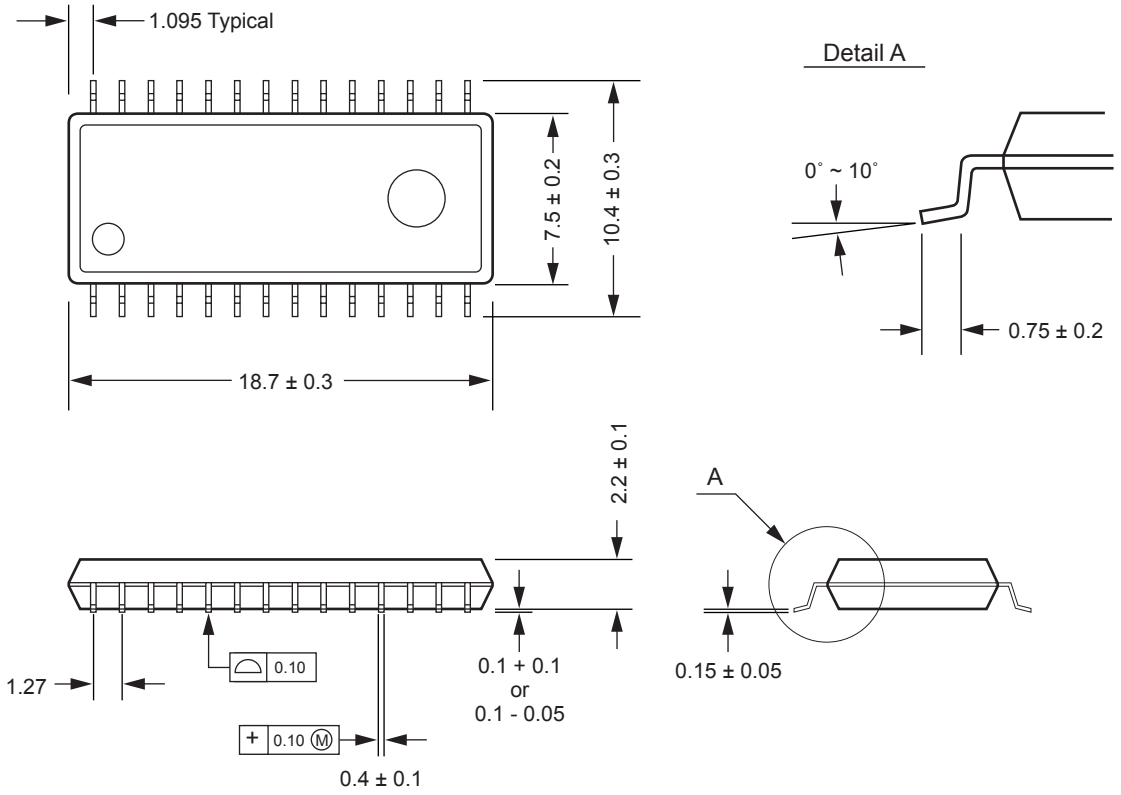
Notes:

Notes:

Package Dimensions

28-Pin SOP

Units: mm



Material and Lead Frame Material:

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder Plate

Package Markings

XXXBYYYYC: Data Code Identifier

XXXB: Lot Number (X: Digit Number, B: Alpha Character)
YYYYC: Assembly Date (YYYY: Digit Number, C: Alpha Character)

Ordering Information

Part Number	Temperature Range	Package
AK5383VS	-10˚C to +70˚C	28-Pin SOP
AKD5383		Evaluation Board