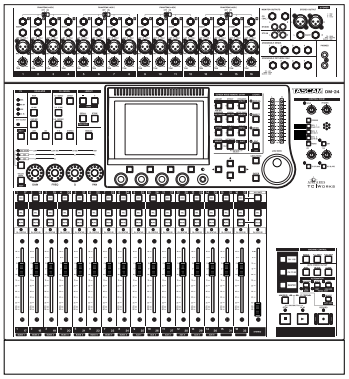


TASCAM
TEAC Professional Division

# SERVICE MANUAL

# DM-24

## Digital Mixing Console

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**INSTRUCTIONS FOR SERVICE PERSONNEL**

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.


Effective : July, 2002

S-0065

# 1. SPECIFICATIONS
仕様

## <Analog audio I/O>

All specifications are given with the factory referencelevel of –16dBFS.

**MIC inputs (channels 1 through 16)**
Balanced XLR-type female connectors
(1=ground, 2=hot, 3=cold)
Adjustable input level: –56dBu (TRIM max) to –2dBu (TRIM min))
Input impedance: 2.2kΩ

**PHANTOM (+48V)**
+48V phantom power. Switchable in blocks of 4 channels (1–4, 5–8, 9–12, 13–16)

**LINE IN (BAL) inputs (channels 1 through 16)**
Balanced 1/4" jacks (sleeve=ground, ring=cold, tip=hot)
Adjustable input level: –42dBu (TRIM max) to +12dBu (TRIM min)
Input impedance: 10kΩ

**INSERT connections (channels 1 through 16)**
1/4" TRS jacks (sleeve=ground, ring=return, tip=send)
Send: nominal output level –2dBu, maximum output level +20dBu, output impedance 100Ω
Return: nominal input level –2dBu, headroom 16dB, input impedance 10kΩ

**ASSIGNABLE RETURNS (BAL) (1 through 4)**
Balanced 1/4" jacks
Nominal input level: –2dBu
Headroom: 16dB
Input impedance: 5kΩ

**ASSIGNABLE SENDS (1 through 4)**
Quasi-balanced 1/4" jacks
Nominal output level: –2dBu
Maximum output level: +14dBu
Output impedance: 100Ω

**2 TR IN (L/R)**
2 x RCA pin jacks
Nominal input level: –10dBV
Headroom: 16dB
Input impedance: 10kΩ

**STEREO OUTPUT (L/R)**
Balanced XLR-type male connectors
Nominal output level: +4dBu
Maximum output level: +20dBu
Output impedance: 100

**STEREO INSERT (L/R) 1/4" TRS jacks**
Send: nominal output level –2dBu, maximum output level +14dBu, impedance 100Ω
Return: nominal input level –2dBu, headroom 22dB, impedance 10kΩ

## <アナログオーディオ入出力>

＊アナログオーディオ出力仕様は基準レベル＝－ 16 dBFS（Full Scale）のとき（標準設定）の仕様を表示しています。サービス対応によって基準レベル＝－ 20 dBFS あるいは－ 9 dBFS に変更した場合、それにともなって最大出力レベル（＝ 0 dBFS 時の出力レベル）が変わります。

MIC 入力（CH1-16）
XLR - 3 - 31 タイプ、バランス
（1 :GND 、2 :HOT 、3 :COLD）
入力インピーダンス : 2.2 k Ω
入力レベル : － 56 dBu ～－ 2 dBu

LINE IN 入力（CH1-16 ）
6 φステレオホンジャック、バランス
（Tip : HOT、Ring : COLD、Sleeve : GND）
入力インピーダンス : 10 k Ω
規定入力レベル : － 42 dBu ～+12 dBu

OL インジケーター（CH1-16）
チャンネル INPUT または MIC/LINE 入力レベルが設定レベルを越えたときに点灯（**SETUP** 画面で設定）
設定レベル : OVER、0、－ 2、－ 4、－ 6、－ 8、－ 10、－ 12、－ 18、－ 30、 － 42（dB）の中から選択

PHANTOM（+48V）
＋ 48V のファントム電源を 4 チャンネル単位（1-4、5-8、9-12、13-16）でオン／オフ可能

INSERT（CH1 - 16）
6φ 3 極（TRS）ホンジャック、アンバランス
（Tip :SEND、Ring :RTN、Sleeve :GND）
SEND（Tip）
出力インピーダンス : 100 Ω
規定出力レベル : － 2 dBu
RETURN （Ring）
入力インピーダンス : 10K Ω
規定入力レベル : － 2 dBu

ASSIGNABLE RETURNS（BAL）（1 ～ 4）
入力インピーダンス : 5 K Ω
規定入力レベル : － 2 dBu

ASSIGNABLE SENDS（1 ～ 4）
出力インピーダンス : 100 Ω
規定出力レベル : － 2 dBu

STEREO OUTPUTS （BALANCED）
XLR-3-32 タイプ、バランス
（1 : GND 、2 : HOT 、3 : COLD ）
出力インピーダンス : 100 Ω
規定出力レベル : ＋ 4 dBu（－ 16 dBFS）

**MONITOR OUTPUTS (CR (BAL))**
Balanced 1/4” jacks
Nominal output level: +4dBu (CR VR max.)
Maximum output level: +20dBu (CR VR max.)
Output impedance: 100Ω
**MONITOR OUTPUTS (STUDIO)**
RCA pin jacks
Nominal output level –10dBV
Maximum output level: +6dBV
Output impedance: 100Ω
**PHONES 2 x 1/4” stereo jacks**
Maximum output level: 120 mW + 120 mW (33Ω load)

## <Digital audio I/O>

**DIGITAL INPUTS (1, 2)**
2 x XLR-type female connectors (input impedance 110Ω)
2 x RCA pin jacks (input impedance 75Ω)
AES3-1992 or IEC60958 data format (automatically detected)
24-bit word length
Switchable sampling frequency conversion available
**DIGITAL OUTPUTS (1, 2)**
2 x XLR-type male connectors (output impedance 110Ω)
2 x RCA pin jacks (output impedance 75Ω)
AES3-1992 or IEC60958 data format (software selectable)
24-bit word length
**TDIF-1(1, 2, 3)**
3 x 25-pin D-sub connectors (metric lock screws)
Conform to TDIF-1 standard
24-bit word length
**ADAT IN/OUT**
2 x “Lightpipe” optical connectors
Conform to ADAT OPTICAL specifications
24-bit word length
**Sampling frequencies**
Internal 44.1kHz/48kHz, 88.2kHz/96kHz (high sampling frequencies)
External ±6.0% ofIs

## <Miscellaneous I/O connections>

**WORD SYNC IN**
BNC connector
Switchable 75Ω termination
TTL level
**WORD SYNC OUT/THRU**
BNC connector
Switchable between through and output
TTL level

STEREO INSERT
6φ 3極（TRS）ホンジャック、アンバランス
（Tip : SEND 、Ring : RTN 、Sleeve : GND）
SEND（Tip）
出力インピーダンス : 100 Ω
規定出力レベル : − 2 dBu
RETURN（Ring）
入力インピーダンス : 10K Ω
規定入力レベル : − 2 dBu

MONITOR OUTPUTS - CR（BAL）
6φホンジャック、バランス
（Tip : HOT 、Ring : COLD 、Sleeve : GND）
出力インピーダンス : 100 Ω
規定出力レベル : +4 dBu（− 16dBFS）/CR VR MAX 時

MONITOR OUTPUTS - STUDIO
6φホンジャック、アンバランス
出力インピーダンス : 100 Ω
規定出力レベル : − 10 dBu（− 16dBFS）

DIM スイッチ
CR 出力を 0 dB 〜−40 dB の範囲（MONITOR 画面で設定）で減衰

PHONES 出力
6φステレオホンジャック
最大出力レベル : 120 mW +120 mW（33 Ω負荷時）

2TR IN
RCA ピンジャック、アンバランス
入力インピーダンス : 10 K Ω
規定入力レベル : − 10 dBV

### <デジタルオーディオ入出力>

TDIF-1（1、2、3）
コネクター : D-sub 25 ピンタイプ
データフォーマット : TDIF-1 規格準拠

ADAT IN/OUT
コネクター : TOSLINK「ライトパイプ」オプティカルタイプ
データフォーマット : ADAT 規格準拠

DIGITAL INPUTS（1、2）
コネクター : XLR-3-31/ RCA ピンジャック
データフォーマット : AES3-1992（AES/EBU）または
IEC-60958（S/PDIF）規格準拠（自動検出）
サンプリング周波数変換機能内蔵

**MIDI IN, OUT, THRU/MTC OUT**
3 x 5-pin DIN connectors—conform to MIDI specifications
**TIME CODE IN**
RCA pin jack
Conforms to SMPTE specifications
**DTRS REMOTE OUT**
15-pin D-sub male (metric lock screws)
Conforms to DTRS SYNC standard
**EXT SW**
1/4" mono jack
**TO METER**
25-pin D-sub connector (non-metric lock screws)
For use with the optional MU-24/DM
**RS-422 (for Sony 9-pin)**
9-pin female D-sub connector (non-metric lock screws) wired to RS-422 standards
**GPI (for Machine start)**
9-pin female D-sub connector (non-metric lock screws) wired for GPI control
Pin 1=GPI1, Pin 2=GPI2, Pin 3=GPI3, Pin 4=GPI4, Pin 5=GPI5, Pin 6=GPI6,
Pin 7=GPI7, Pin 8=GPI8, Pin 9=ground

## <Equalization>

**EQ switch**
On/Off
**HIGH filter**
Gain: ±18dB, 0.5dB resolution
Frequency: 31Hz to 19kHz
Q: 0.27 to 8.65
Type: Hi-shelving, Peak, LPF
**HI MID filter Gain: ±18dB, 0.5dB resolution**
Frequency: 31Hz to 19kHz
Q: 0.27 to 8.65
Type: Peak, Notch
**LO MID filter**
Gain: ±18dB, 0.5dB resolution
Frequency: 31Hz to 19kHz
Q: 0.27 to 8.65
Type: Peak, Notch
**LOW filter**
Gain: ±18dB, 0.5dB resolution
Frequency: 31Hz to 19kHz
Q: 0.27 to 8.65
Type Low-shelving, Peak, HPF

DIGITAL OUTPUT（XLR）

コネクター : XLR-3-32/ RCA ピンジャック

データフォーマット : AES3-1992（AES/EBU）または IEC-60958（S/PDIF）選択可

**サンプリング周波数**

44.1 kHz、48 kHz、88.2 kHz、96 kHz（外部同期時の許容周波数偏差：± 6%）

**＜同期／制御／その他のコネクター＞**

WORD SYNC IN 入力:

コネクター : BNC （アンバランス）

TTL レベル、75 Ω ON/OFF 切替

WORD SYNC THRU/OUT 出力:

コネクター : BNC （アンバランス）

THRU と OUT を選択可

TTL レベル、75 Ω

RS-422:

コネクター : D-sub 9 ピン（メス）

RS-422 準拠、ソニー 9 ピンシリアルプロトコル（P2）によるマシンコントロール用

GPI :

コネクター : D-sub 9 ピン（メス）

TO METER :

コネクター : D-sub 25 ピン（メス）、オプションのメーターユニット（MU-24）接続用

MIDI IN 、OUT 、THRU

コネクター : 5 ピン DIN コネクター

MIDI 規格準拠

EXT SW

6φ、2 極ホンジャック

TC IN 入力:

RCA ピン（アンバランス）

入力インピーダンス : 20K Ω

入力レベル : − 30 dBV

## <System performance>

**THD (nominal level)**
20Hz – 20kHz LINE IN to INSERT SEND: < 0.1%
1kHz LINE IN to STEREO OUTPUT: < 0.013%
**Frequency response (nominal level)**
MIC/LINE IN to INSERT SEND:
20Hz – 25kHz +0.5dB/– 1.5dB
LINE IN to STEREO OUTPUT:
20Hz – 20kHz +0.5dB/– 1.0dB
LINE IN to BUSS/AUX OUTPUT
20Hz – 20kHz +0.5dB/– 1.0dB
2TR IN to MONITOR OUTPUTS
20Hz – 25kHz +0.5dB/– 1.5dB
**Noise level (20Hz – 20kHz, TRIM:max, 150Ω, – 60dB)**
MIC IN to INSERT SEND: < – 128dBu
MIC IN to STEREO OUTPUT (BAL): < – 68dBu
MIC IN to STEREO OUTPUT (UNBAL): < – 74dBu
MIC IN to BUSS/AUX OUTPUT: < – 74dBu
2TR IN to MONITOR OUTPUT: < – 80dBu
**Crosstalk @ 1kHz**
STEREO/BUSS/AUX OUTPUTS: > 80dB
MONITOR OUTPUTS: > 70dB

## <Physical characteristics>

**Displays**
Backlit 320 x 240 LCD with contrast control
2 x 12-segment LED meters
**Faders**
17 x 100mm stroke, motor-driven touch-sensitive faders
**Maximum overall dimensions (w x d x h) including rest**
582 x 657 x 198 (mm) 22.9 x 25.9 x 7.8 (in)
**Weight**
20.5kg (45.1lbs)
**Voltage requirements**
120VAC, 60Hz
230VAC, 50Hz
240VAC, 50Hz
**Power consumption**
82W
**Peak inrush current**
8A
**Applicable electromagnetic environment**
E4

● Specifications and appearance subject to change without notice.

## ＜アナログオーディオ特性＞

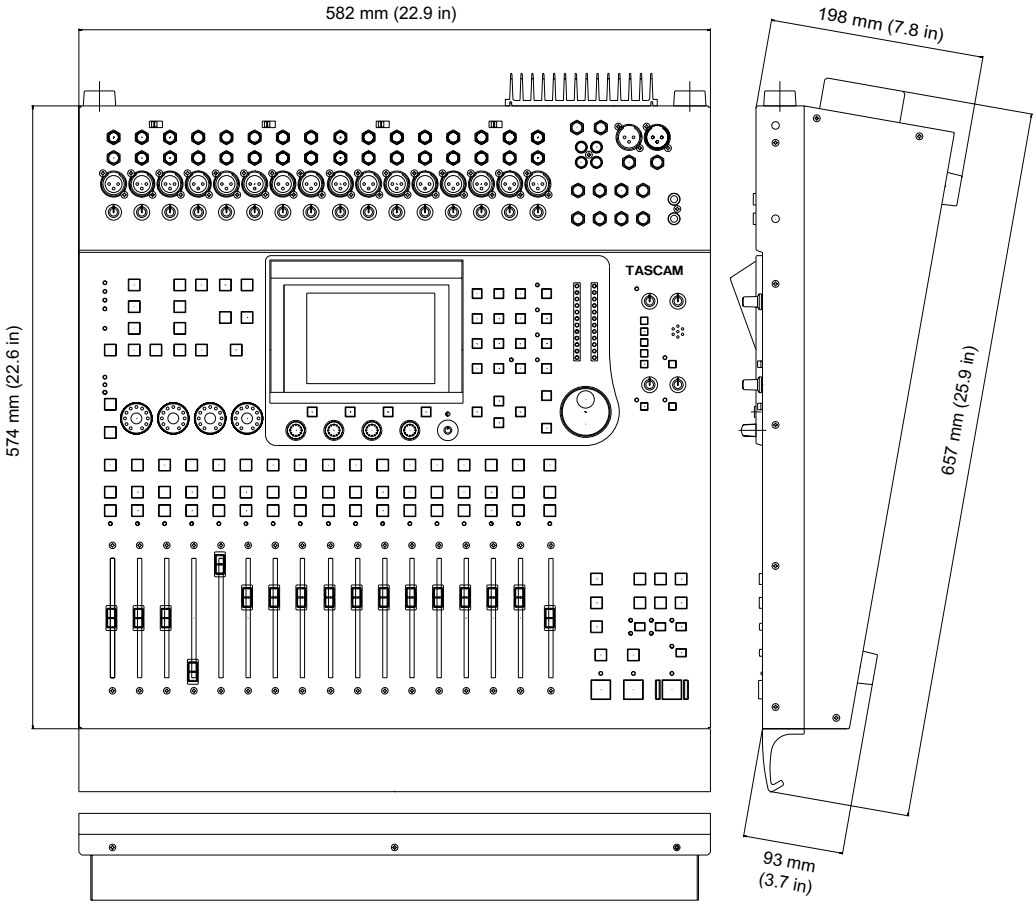
**歪率(THD):**
0.1%以下（20 Hz - 20 kHz 、LINE IN ＋4 dBu 入力 → INSERT SEND）
0.013%以下（1 kHz 、LINE IN ＋4 dBu 入力 → STEREO OUTPUT）
**周波数特性:**
20Hz − 25kHz、＋0.5dB/− 1.5dB（MIC/LINE IN → INSERT SEND）
20Hz − 20kHz、＋0.5dB/− 1.0dB（LINE IN → STEREO OUTPUT）
20Hz − 20kHz、＋0.5dB/− 1.0dB（LINE IN → BUSS/AUX OUTPUT）
20Hz − 25kHz、＋0.5dB/− 1.5dB（2TR IN → MONITOR OUTPUTS）
**ノイズレベル（150 Ω、20Hz − 20kHz、TRIM:最大、−60dB）:**
− 128dBu 以下［MIC IN → INSERT SEND］
− 68dBu 以下［MIC IN → STEREO OUTPUT (BAL)］
− 74dBu 以下［MIC IN → STEREO OUTPUT (UNBAL)］
− 74dBu 以下［MIC IN → BUSS/AUX OUTPUT］
− 80dBu 以下［2TR IN → MONITOR OUTPUT］

## ＜機械的仕様＞

ディスプレイ : バックライト式 320 × 240 LCD（コントラストコントロール可能）
12 セグメント LED メーター（×2）
フェーダー : 100mm ストローク、モータードライブ、タッチセンシティブフェーダー
外形寸法 : 582(W)× 657(D)×198(H)mm
質量 : 20.5 kg
電源 : 100 V 、50/60 Hz AC
消費電力 : 82 W

● 仕様および外観は、改善のため予告なく変更することがあります。

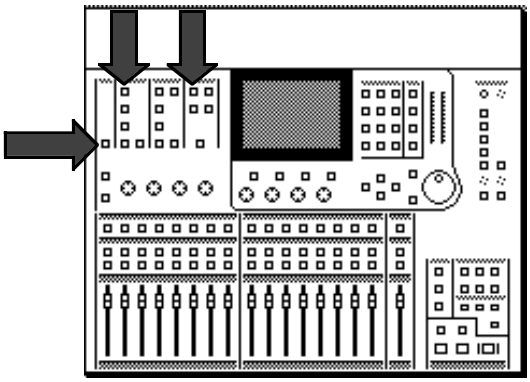
**Dimensional Drawings 寸法図**



# 2. SELF DIAGNOSTIC FUNCTION
## 自己診断機能

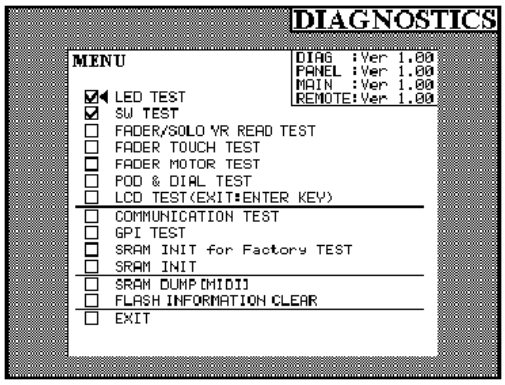
Power to the unit while holding down 2ND F. + EQUALIZER [HIGH] + LIBRARY [-] (until "TASCAM" appears scrolling).

2ND F.キー ＋ EQUALIZER [HIGH]キー＋ LIBRARY [-]キーを押しながら（"TASCAM"の文字がスクロールするまで押したままにしておく）電源投入すると、



Then the DIAG menu screen will appear, as the illustration below shows.
You can move the cursor through the test items by using the cursor keys or JOG/DATA dial. When you press the ENTER key, the unit switches into the selected test mode.

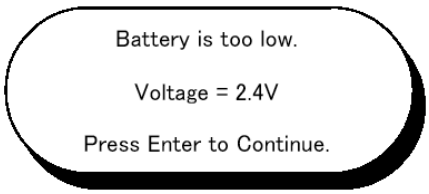
次のようなDIAGメニュー画面が表示される。
カーソルキーまたはJOG/DATAダイヤルで各テスト項目にカーソルを合わせ、ENTERキーを押すと、それぞれのテストモードに移る。



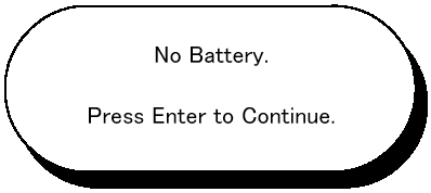

In addition, upon launch of DIAG, the DM-24 checks the voltage of the battery for SRAM and displays a pop-up warning message if the voltage lies in the range of error (below 2.5 V or more than 3.9 V).

また、DIAG起動時、SRAM用の電池の電圧チェックを行い、エラー値（2.5V未満あるいは3.9V以上）であればPop-upで警告する。

In case the voltage is below 2.5 V :
2.5V未満のとき：



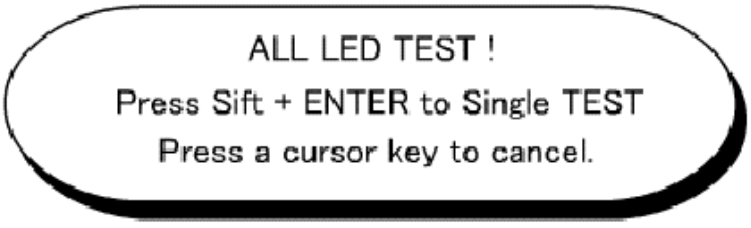

In case the voltage is more than 3.9 V :
V:2.5V未満のとき：



■ LED TEST

This test checks if each of the LEDs illuminates.

1. When the DM-24 switches into the LED TEST mode, a pop-up message, as shown below, appears and all the LEDs should illuminate.
   ※ They illuminate at the same time if the meter bridge (MU-24) is connected.




2. Press a cursor key to return to the DIAG menu screen. If all the LEDs are in order, the LED TEST item is check marked.

※ You can press SHIFT + ENTER during ALL LED TEST. Then the next pop-up message will appear and the LEDs will illuminate one at a time in sequence. Pressing a cursor key brings you back to the DIAG menu screen.
(This test does not run on the meter bridge.)

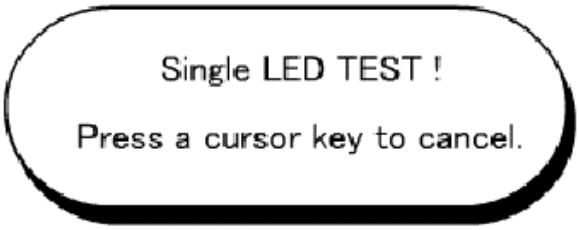
■ LED TEST

各 LED の点灯チェックを行う。

1. LED TEST モードに入ると次の Pop-up メッセージが表示され、LED が全点灯する。
   ※メーターブリッジ（MU-24）が接続されていれば、同時に点灯する。

2. カーソルキーを押すと DIAG メニュー画面に戻る。
   全ての LED が正常ならば LED TEST 項目にチェックマークが付く。

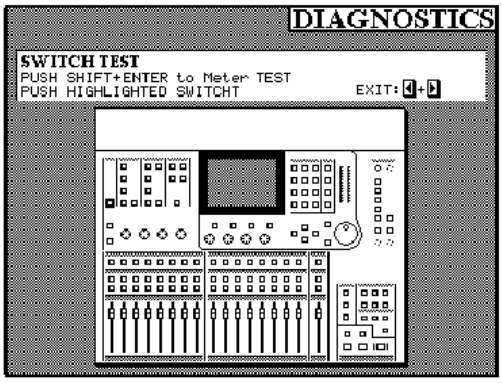
※ ALL LED TEST 中に、SHIFT キー＋ ENTER キーを押すと、次の Pop-up メッセージが表示され、各 LED が順番に点灯する。カーソルキーを押すと DIAG メニュー画面に戻る。
（メータブリッジは、このテストは行わない。）



■ SW TEST

This test checks if each of the switches toggles on/off properly. When you run this test, the DM-24 is automatically set to CH-16 for LAYER STATUS.

1. When the DM-24 switches into the SW TEST mode, the following screen will appear.




2. Press the switches in sequence, the on-screen images of which are blinking. Each time you press a switch, the corresponding on-screen image goes out.
   Pressing a switch associated with an LED causes the LED to illuminate to indicate the switch is activated. The LED turns off when the switch is deactivated.
3. Upon completion of the check of all the switches, the DIAG menu screen reappears with the SW TEST item check marked.

※ To abort the switch test, press the left (◄) and right (►) cursor keys at the same time.
※ When the switch test is being conducted on the DM-24 and you press SHIFT + ENTER, the switch test shifts to the meter bridge (MU-24). Pressing ENTER brings you back to the DIAG menu screen.
   The switches on the meter bridge are tested in the same way the switches on the DM-24 are.

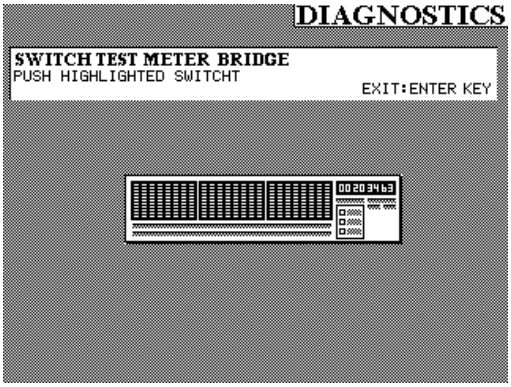
■ SW TEST

各スイッチの ON/OFF チェックを行う。
このとき、LAYER STATUS は自動的に CH1-16 にセットされる。

1. SW TEST モードに入ると、次の画面を表示する。

2. 画面上で点滅しているスイッチを順に押してゆくと、押されたスイッチの表示は消えてゆく。
   このとき、押されたスイッチに連動する LED があれば、スイッチが ON のとき点灯し、OFF のとき消灯する。
3. すべての SW チェックが終了すると、DIAG メニュー画面に戻り、SW TEST 項目にチェックマークが付く。

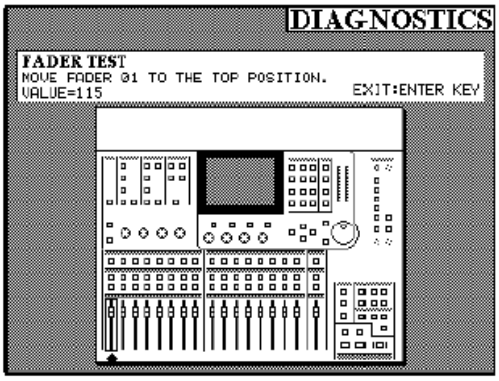
※ 途中で強制終了する場合は、カーソルキー［◄］と［►］を同時に押す。
※ 本体のＳＷテスト中に SHIFT キー + ENTER キーを押すと、メーターブリッジ（MU-24）の SW テストに入る。
ENTER キーを押すと、DIAG メニュー画面に戻る。
テストの方法は本体と同様。



■ FADER/SOLO VR READ TEST

This test checks if the reading provided by each fader is correct. The DM-24 is automatically set to CH-16 for LAYER STATUS.

1. When the DM-24 swiches into the FADER/SOLO VR READ TEST mode, the screen should look like this.




2. An arrow mark is displayed below the image of a fader to be moved. Push up and bring down that fader. A frame should be displayed around the fader and the reading and CH number are displayed in the upper part of the screen.
3. If the fader works properly providing the prescribed maximum and minimum values, go on to the next fader. The image of the previous fader, which has been checked, goes out.
4. When all the faders have been checked, an arrow mark is displayed below the SOLO knob image.
5. Turn the SOLO knob all the way up then all the way down, then the DIAG menu screen reappears with the FADER/SOLO VR READ TEST item check marked.

※ If a fader offers the maximum/minimum value when it is not in the uppermost/lowermost position, something goes wrong with FADER/SOLO VR. Remember that this irregularity does not result in a test failure and a check mark is put to the FADER/SOLO VR READ TEST item on the menu.
※ To abort the fader read test, press ENTER.

■ FADER/SOLO VR READ TEST

各フェーダーの読み取り値が正常化どうかをチェックする。このとき、LAYER STATUS は自動的に CH1-16 にセットされる。

1. FADER/SOLO VR READ TEST モードに入ると、次の画面を表示する。

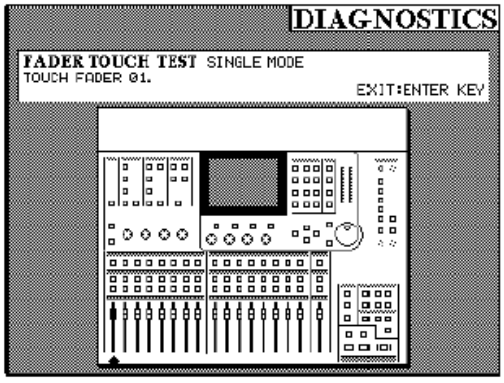
2. 動かすべきフェーダーの下に矢印が表示されるので、そのフェーダーを動かす。このとき、動かしているフェーダーの周りに枠が表示され、また画面の上部に読み取り値と CH が表示される。
3. フェーダーが正常で、最大値と最小値が読めたら次のフェーダーへ移動する。このとき、チェック済みとなったフェーダーの絵は消える。
4. すべてのフェーダーチェックが終了すると、SOLO つまみの下に矢印が表示される。
5. SOLO つまみを最大、最小に回すと、DIAG メニュー画面に戻り、FADER/SOLO VR READ TEST 項目にチェックマークが付く。

※ 最大値／最小値が、一番上／一番下以外の位置で読み取られる場合は、FADER ／ SOLO VR の異常が考えられる。ただしこの場合も、テストは正常とみなされチェックマークは付いてしまうので注意が必要。
※ 途中で強制終了する場合は、ENTER キー押す。

■ FADER TOUCH TEST

This test checks the faders for touch sensitivity. This test also checks if, when a single fader is touched, only that fader senses it or if, when two or more faders are touched, they all sense it.

1. When the DM-24 switches into the FADER TOUCH TEST mode, the following screen will appear.




2. Touch the fader, below the on-screen image of which an arrow mark is displayed.
   The number assigned to a fader to be touched is shown in the upper part of the screen, along with the number assigned to the actually touched fader.
   The on-screen image of the fader knob you touch goes black.
3. If the fader you touched is recognized by the DM-24, go on to the next fader. The on-screen image of the fader having been checked goes out.
4. When all the faders have been successfully checked, the DIAG menu screen reappears with the FADER TOUCH TEST item check marked.

※ If faders are not recognized correctly, try changing the CLOCK setting for FADER SESITIVITY on the SET UP sub-screen under the OPTION screen.
Also, you can set the FADER SENSITIVITY setting to [ON] so that the ON/STATUS LED is available to check the fader sensitivy.

※ To abort the fader sensisvity test, press ENTER.

■ FADER TOUCH TEST

FADER のタッチセンス機能のチェックを行う。触れているフェーダーのみがタッチを認識するかどうかや、複数のフェーダーを同時に触れた時に正しく認識するかをチェックする。

1. FADER TOUCH TEST モードに入ると、以下の画面を表示する。

2. 触れるべきフェーダーの下に矢印が表示されるので、そのフェーダーに触れる。
   このとき、画面の上部に触れるべきフェーダーナンバーと触れているフェーダーナンバーを表示する。
   また、触れているフェーダーノブは黒塗りで表示される。
3. 触れたフェーダーが正しく認識されたなら、次のフェーダーに移動する。このとき、チェック済みとなったフェーダーの絵は消える。
4. すべてのフェーダーチェックが終了すると、DIAG メニュー画面に戻り、FADER TOUCH TEST 項目にチェックマークが付く。

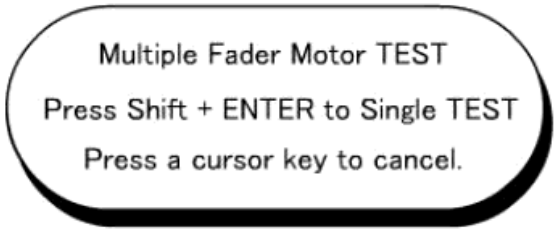
※ 正しく認識されない場合は、OPTION 画面の SET UP サブ画面で、FADER SENSITIVITY の CLOCK 周波数の設定を変えてみる。
また、FADER SENSITIVITY を [ON] にすると、ON/STATUS LED でタッチセンスのチェックが可能。

※ 途中で強制終了する場合は、ENTER キー押す。

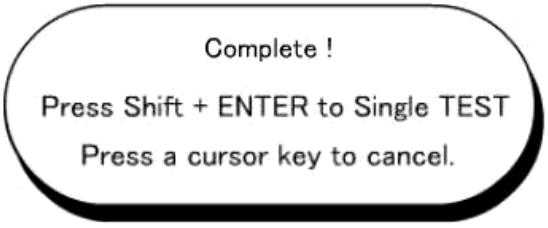
■ FADER MOTOR TEST

This test checks if the fader motors work properly either one by one or all at a time.

1. When the DM-24 switches into the FADER MOTOR TEST mode, the following pop-up message will appear and the Multiple Fader Moter TEST will start.
   All the faders move from MIN value → MAX value → MIN value → 15 dB (or 25 dB with the STEREO fader).

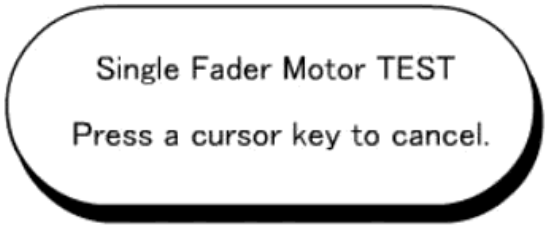



2. When all the faders have moved through the positions indicated above, the next pop-up message would appear.




3. When you press a cursor key, the pop-up message goes out and the DIAG menu screen reappears with the FADER MOTOR TEST item check marked.

※ Pressing SHIFT + ENTER at the Multiple Fader Motor TEST time, the next pop-up message appears and the Single Fader Motor TEST starts.
The faders move from MIN value → MAX value → MIN value in 1 frame steps sequentially, starting with the fader on CH 1. To abort the process, press a cursor key.




■ FADER MOTOR TEST

１つまたは複数のフェーダーのモーターが正常に動作するかをチェックする。

1. FADER MOTOR TEST モードに入ると、次の Pop-up メッセージが表示され、Multiple Fader Motor TEST が開始される。
   このとき、全フェーダーが MIN 値→ MAX 値→ MIN 値→ 15dB（STEREO フェーダーは 25dB）と移動する。

2. フェーダーが移動し終わると、次の Pop-up メッセージが表示される。

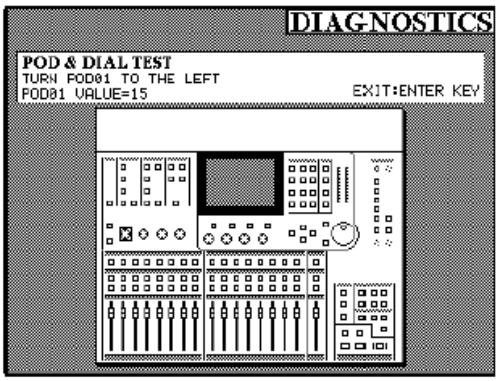
3. カーソルキー押すと Pop-up は消え、DIAG メニュー画面に戻り、FADER MOTOR TEST 項目にチェックマークが付く。

※ Multiple Fader TEST のときに SHIFT キー＋ ENTER キーを押すと、次の Pop-up メッセージが表示され、Single Fader Motor TEST が開始される。
このとき、フェーダーは CH1 から順番に、1 ステップ 1 フレームで MIN 値→ MAX 値→ MIN 値と移動する。
途中で強制終了する場合は、カーソルキーを押す。

■ POD & DIAL TEST

This test checks if each POD recognizes the rotational direction when rotated.

1. When the DM-24 switches into the POD & DIAL TEST mode, the following screen appears.




2. A POD to be rotated is indicated by a bliking frame. Rotate that POD. (First, the JOG/DATA dial will be indicated.)
3. Rotate the POD all the way down (to the left) then all the way up (to the right), and go on to the next POD.
4. When all the PODs have been checked, the DIAG menu screen reappears with the POD & DIAL TEST item check marked.

※ PTo abort the process, press ENTER.

■ POD & DIAL TEST

各 POD を回したときに左右の方向の認識が正しいかをチェックする。

1. POD & DIAL TEST モードに入ると、以下の画面を表示する。

2. 回すべき POD がブリンク枠で表示されるので、それを回す。（最初に JOG/DATA ダイヤルが表示される）
3. 最小値（左回し）に回してから最大値（右回し）に回すと、次の POD に移動する。
4. すべての POD チェックが終了すると、DIAG メニュー画面に戻り、POD & DIAL TEST 項目にチェックマークが付く。

※ 途中で強制終了する場合は、ENTER キー押す。

■ LCD TEST

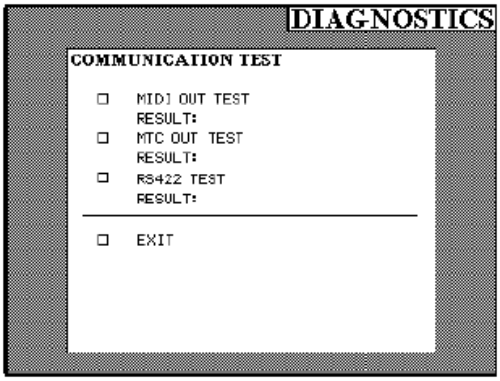
This test checks each of the LCD screens for irregularity.

1. When the DM-24 switches into the LCD TEST mode, the screen sequences through All Turned Off (about 1 second) → All Turned On (about 1 second) → DIAG menu (about 1 second).
2. Pressing ENTER brings you back to the DIAG menu screen with the LCD TEST item check marked.

■ COMMUNICATION TEST

This test checks the MIDI I/O and RS422 for irregularity.
This test is conducted largely by letting data be looped, as internally directed, and checking if the same data returns back.

1. When the DM-24 switches into the COMMUNICATION TEST mode, the following screen will appear.




2. To run the following tests, make the indicated connections.

   MIDI OUT TEST:
   Connect a MIDI cable from MIDI OUT to MIDI IN.

   MTC OUT TEST:
   Connect a MIDI cable from THRU/MTC OUT to MIDI IN.

   RS-422 TEST:
   Get a 9-pin D-sub connector ready, and short-circuit pins 2-8 and 3-7, then connect this connector to the RS-422.

3. Move the cursor to a test item and press ENTER to run the corresponding test.

■ LCD TEST

各液晶画面の不具合がないかをチェックする。

1. LCD TEST モードに入ると、画面は全消灯（約 1 秒）→ 全点灯（約 1 秒）→ DIAG メニュー（約 1 秒）を繰り返す。
2. ENTER キーを押すと、DIAG メニュー画面に戻り、LCD TEST 項目にチェックマークが付く。

■ COMMUNICATION TEST

MIDI I/O と RS422 に不具合がないかをチェックする。
基本的に内部でデータをループさせ同じデータが帰ってくることをチェックする。

1. COMMUNICATION TEST モードに入ると、以下の画面を表示する。

2. 各テストを行うために、各接続を行う。

   MIDI OUT TEST:
   MIDI OUT と MIDI IN を MIDI ケーブルで接続する。

   MTC OUT TEST:
   THRU/MTC OUT と MIDI IN を MIDI ケーブルで接続する。

   RS-422 TEST:
   9-Pin D-sub コネクタを用意し、2-8, 3-7 を短絡したコネクタを作成し、RS-422 端子に接続する。

3. カーソルを各テスト項目に移動させ ENTER キーを押すとテストが開始される。

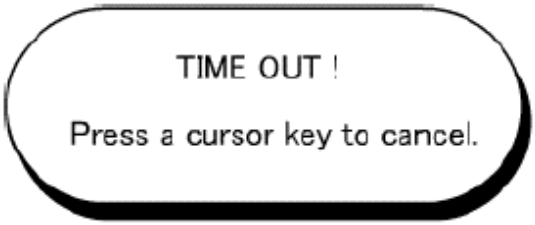
4. When the test was successful, the next pop-up message appears. This pop-up message automatically goes out and brings you back to the COMMUNICATION TEST screen with a check mark placed in the corresponding check box.

4. テスト結果が正常ならば、次の Pop-up メッセージが表示される。この Pop-up メッセージは自動的に消え、COMMUNICATION TEST 画面に戻り、チェックボックスにチェックマークが付く。




5. When a time-out occurs, the next pop-up message will appear.
This pop-up message goes out when you press a cursor key. No check mark is placed in the check box and the RESULT reads NG.

5. タイムアウトが発生した場合は、次の Pop-up メッセージが表示される。
カーソルキーで、この Pop-up メッセージは消え、チェックボックスには、チェックマークは付かない。
また、RESULT に NG が表示される。



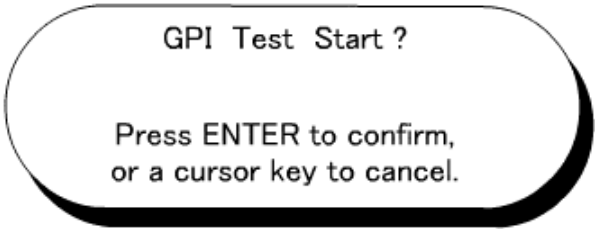

6. Move the cursor to EXIT in the COMMUNICATION TEST screen and press ENTER to return to the DIAG menu screen. If all the three test items are successfully checked on the COMMUNICATION TEST screen, the COMMUNICATION TEST item on the DIAG menu screen is check marked.

6. COMMUNICATION TEST 画面の EXIT にカーソルを移動し ENTER キーを押すと、DIAG メニュー画面に戻る。このとき、COMMUNICATION TEST 画面の 3 つのテスト項目すべてにチェックマークが付いている場合は、DIAG メニューの COMMUNICATION TEST 項目にチェックマークが付く。

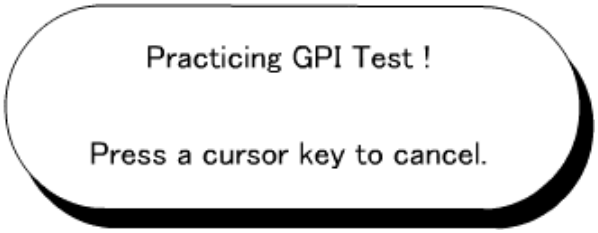
■ GPI TEST

This test check if the GPI pulse signal is sent out correctly.

1. When the DM-24 switches into the GPI TEST mode, the following pop-up message will appear.




2. Upon pressing ENTER, the GPI pulse signal is sent out and the next pop-up message will appear.
※ Pressing a cursor key stops sending out the GPI pulse signal.




3. Pressing a cursor key stops the GPI pulse signal, bringing you back to the DIAG menu screen.
The GPI TEST item is check marked if there is no problem in sending out the GPI pulse signal.

■ GPI TEST

GPI パルスが正しく送出されるかのテスト。

1. GPI TEST モードに入ると、次の Pop-up メッセージが表示される。

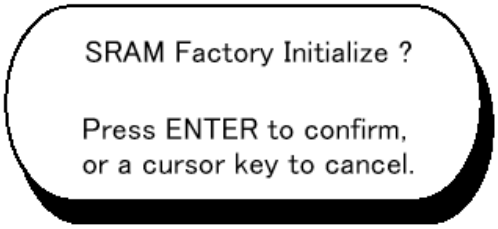
2. ENTER を押すと GPI パルスが送出され、次の Pop-up メッセージが表示される。
※ カーソルキーを押すと、GPI パルスは送出されない。

3. カーソルキーを押すと GPI パルスの送出が止まり、DIAG メニュー画面に戻る。
このとき、GPI パルスが正しく送出されたならば、GPI TEST 項目にチェックマークが付く。

■ SRAM INIT for Factory TEST

This procedure makes the SRAM available for use on a production line.
When you do this, it is absolutely necessary to run the SRAM INIT procedure before shipment. (Refer to the next item.)

1. When the DM-24 switches into the SRAM INIT for Factory TEST, the next pop-up message will appear.



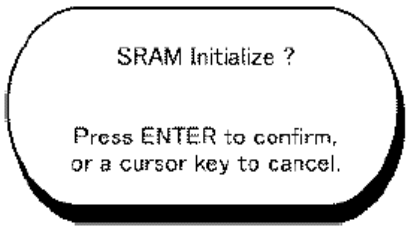

2. Press ENTER and the SRAM is initialized to values for use on a production line. Upon completion of the initialization, the pop-up message will go out, bringing you back to the DIAG menu screen with a check mark placed in the corresponding check box.
※ Pressing a cursor key aborts the initialization.

■ SRAM INIT

This procedure initializes the SRAM to factory defaults.

CAUTION:
When initializing the SRAM, all setting data except for the LIBRARY data are cleared. If necessary, make a backup of the SRAM data, as discussed on page 21.
The LIBRARY data is not cleared because it is on the Flash ROM.

1. When the DM-24 switches into the SRAM INIT mode, the following pop-up message will appear.




2. Press ENTER and the SRAM starts being initialized.
Upon completion of the initialization, the pop-up message will go out, bringing you back to the DIAG menu screen with a check mark put in the corresponding check box.
※ Pressing a cursor key cancels the initialization.

■ SRAM INIT for Factory TEST

SRAM の状態を工場ラインでのチェック用に変更する。
この処理を行った場合、出荷時には必ず SRAM INIT する必要がある。（次項参照）

1. SRAM INIT for Factory TEST モードに入ると、次の Pop-up メッセージが表示される。

2. ENTER キーを押すとライン用の SRAM 値に初期化が行われる。初期化が完了したら Pop-up が消え、DIAG メニュー画面に戻り、チェックボックスにチェックマークが付く。
※ カーソルキーを押すと初期化は行わない。

■ SRAM INIT

SRAM を工場出荷時の値に初期化する。

**注意）**
SRAM を初期化すると、LIBRARY データ以外の各種設定データはクリアされるので、必要であれば 21 ページの手順に従って、SRAM データのバックアップを行うこと。
LIBRARY データは Flash ROM に保存されているのでクリアされない。

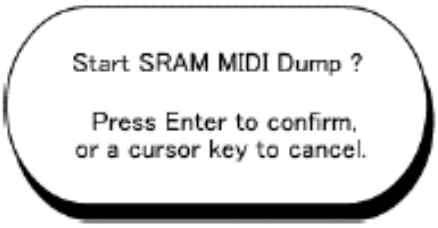
1. SRAM INIT モードに入ると、次の Pop-up メッセージが表示される。

2. ENTER キーを押すと SRAM の初期化が行われる。
初期化が完了したら Pop-up が消え、DIAG メニュー画面に戻り、チェックボックスにチェックマークが付く。
※ カーソルキーを押すと初期化は行わない。

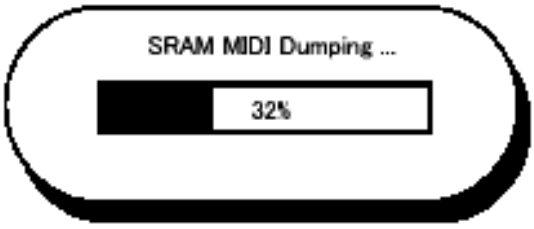
■ SRAM DUMP [MIDI]

This proceudre dumps the content of the SRAM in the SMF (Standard Midi File) format. (Refer to page 21.)

1. When the DM-24 switches into the SRAM DUMP mode, the following message will appear.




2. Upon pressing ENTER, the dump process starts.
   ※ Pressing a cursor key cancels the dump and brings you back to the DIAG menu screen.
   The next pop-up message is displayed during the dump process.
   ※ Once the process starts, there is no way to abort it.




3. Upon completion of the dump, the pop-up message automatically goes out, bringing you back to the DIAG menu screen with a check mark placed in the corresponding check box.

■ SRAM DUMP [MIDI]

SRAM の内容を SMF（Standard Midi File）形式でダンプする。（21 ページ参照）

1. SRAM DUMP モードに入ると、次の Pop-up メッセージが表示される。




2. ENTER キーを押すと、ダンプを開始する。
   ※ カーソルキーを押すとダンプは行わず、DIAG メニュー画面に戻る。
   ダンプ中は次の Pop-up メッセージ（プログレスバー）が表示される。
   ※ ダンプ中のキャンセルはできない。




3. ダンプ終了後、Pop-up は自動的に消え DIAG メニュー画面に戻り、チェックボックスにチェックマークが付く。

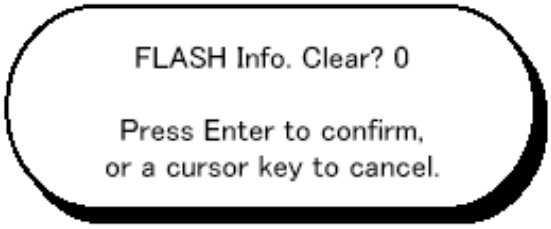
■ FLASH INFORMATION CLEAR

This procedure clears the area of SRAM where is recorded the number of times the FLASH ROM has been written on.

**CAUTION:**
The FLASH ROM life is rated to 100,000 of write times, so the information on how many times the FLASH ROM has been written on is essential to being aware of its precise remaining useable life.
This information is visible on the PREFERENCE sub-screen under the OPTION screen.
Beware: Running the following procedure clears the information about the number of times the FLASH ROM has been written on. Also beware: The number of times you repeat the following procedure is recorded on the SRAM. This record, however, is NOT erased by SRAM INIT.

**BE SURE TO RUN THIS PROCEDURE WHEN THE FLASH ROM IS REPLACED, AND NEVER RUN THIS PROCEDURE EXCEPT IN THE CASE WHERE THE FLASH ROM IS REPLACED.**

1. When the DM-24 switches into the FLASH INROMATION CLEAR mode, the following pop-up message will appear.




2. Press ENTER and the area of the SRAM where the number of times the FLASH ROM has been written on is cleared and the screen is switched to show the DIAG menu screen with a check mark placed in the corrresponding box unless the procedure failed.
   ※ Pressing a cursor key cancels the procedure, bringing you back to the DIAG menu screen.
   ※ The number shown next to the question mark ("?") indicates how many times you have repeated this procedure so far.

■ EXIT

This menu item is used to terminate the DIAG mode.
Upon terminating the DIAG mode, the DM-24 automatically restarts and switches itself into normal mode.

■ FLASH INFORMATION CLEAR

FLASH ROM の書き込み回数情報を記録してある SRAM のエリアをクリアする。

**注意）**
この書き込み回数情報は、FLASH ROM の寿命を正しく把握するために必要な情報である。FLASH ROM は書き込み 10 万回が寿命であるので、何回書き込んだかをメモリする必要がある。
尚、この書き込み情報は OPTION 画面の PREFERENCES サブ画面でみることができる。
この処理では、書き込み回数情報をクリアしてしまうので注意が必要である。
さらにこの処理を実行すると SRAM にこの処理を行った回数を記録するが、SRAM INIT を行ってもこの情報は消せないため注意が必要である。

FLASH ROM を新品に交換したときは必ず行うこと。また、それ以外は絶対に行わないこと。

1. FLASH INFORMATION CLEAR モードに入ると、次の Pop-up メッセージが表示される。

2. ENTER キーを押すと、FLASH ROM の書き込み回数を記録してある SRAM のエリアがクリアされ、DIAG メニュー画面に戻る。
   このとき、正常にクリアされた場合は、チェックボックスにチェックマークが付く。
   ※ カーソルキーを押すとクリアは行わず、DIAG メニュー画面に戻る。
   ※ ” ？” マークの後の数字はこの処理を実行した回数である。

■ EXIT

DIAG モードを終了する。
自動的に再起動し、通常モードとなる。

# 3. HOW TO CHECK THE MAIN PCB VERSION

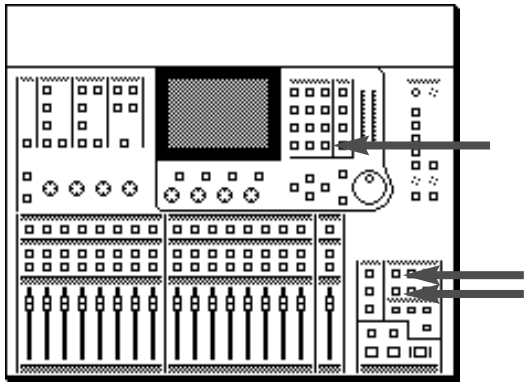
## MAIN PCB Version の確認方法

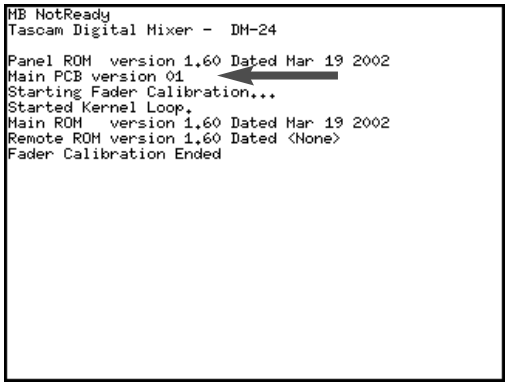
1. Switch on power to the DM-24.

2. Press SHIFT + REPEAT + RHSL as many times as necessary to get to the following screen.
"XX" in "Main PCB version XX" in the forth line is the MAIN PCB version number.

1. 電源を投入する。

2. SHIFT キー＋ REPEAT キー＋ RHSL キーを何回か押して、次の画面を表示させる。
4 行目に表示される "Main PCB version XX" の "XX" が、MAIN PCB の version 番号である。






3. Press SHIFT + REPEAT + RHSL once to go back to the normal screen.

3. SHIFT キー＋ REPEAT キー＋ RHSL キーを 1 回押すと、通常の画面に戻る。

# 4. DOWNLOADING & BACKING-UP THE SRAM DATA

## SRAMデータのバックアップとダウンロード

You need to run the following procedure when the SRAM is cleared, the MAIN PCB is replaced, or the SRAM backup battery is replaced.

The SRAM keeps data about the current various settings except the LIBRARY data.

**CAUTION:**
Do NOT stop the download or the backup procedure in the process. Otherwise, there are occasions where the system data is lost.

この作業は、SRAMクリア時、MAIN PCBの交換時、SRAMのバックアップバッテリーの交換時に必要。

SRAMには、LIBRARYデータ以外の現在の各種設定データが保存されている。

**注意）**
ダウンロードまたはバックアップの作業は途中で止めないこと。システムデータが破壊される可能性がある。

### Required Equipment

- MIDI cable
- Either a computer program that is capable of recording/playing back the MIDI system exclusive data, or a MIDI sequencer (or MIDI Data Filer) equipped with a floppy disk drive

### 使用機器

- MIDIケーブル
- MIDIシステムエクスクルーシブデータを録音／再生することができるコンピューターのプログラムまたは、フロッピーディスクドライブ付きのMIDIシーケンサー（またはMIDI Data Filer）

### Backing up the SRAM data

1. Connect MIDI IN on the sequencer to MIDI OUT on the DA-24 via a MIDI cable.
2. Place the MIDI sequencer in the record mode.
3. Place the DM-24 in the Self Diagnostics mode.
4. Run "SRAM DUMP [MIDI]" in the DIAG menu. (Refer to page 18.)

### SRAMデータのバックアップ方法

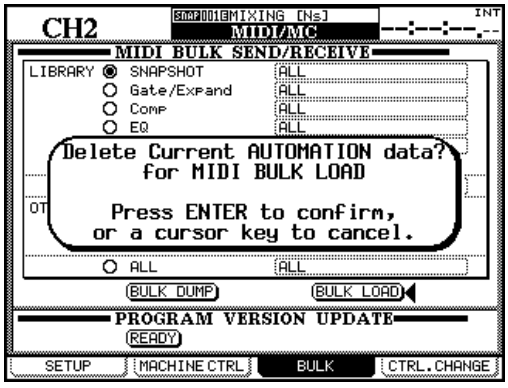
1. シーケンサーのMIDI INとDM-24のMIDI OUTをMIDIケーブルで接続する。
2. MIDIシーケンサーを録音モードにする。
3. 自己診断モードにする。
4. DIAGメニューの“SRAM DUMP [MIDI]”を実行する。（☞ 18ページ）

### Downloading the SRAM data

1. Get to the BULK sub-screen under the MIDI/MC screen, move the cursor to the [BULK LOAD] button, then press ENTER.
2. When the following pop-up message appears, press ENTER.

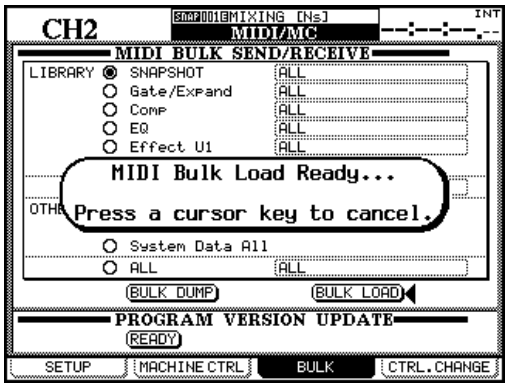
### SRAMデータのダウンロード

1. MIDI/MC画面のBULKサブ画面を表示させ、カーソルを[BULK LOAD]ボタンに合わせてからENTERキーを押す。
2. 次のPop-upメッセージが表示されたら、ENTERキーを押す。



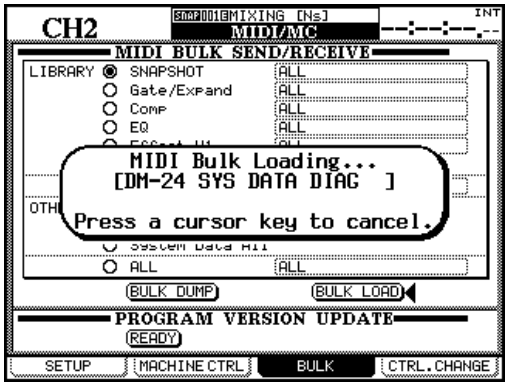
3. When the next pop-up message appears, operate the MIDI sequencer to play the MIDI file containing the SRAM data.

3. 次の Pop-up メッセージが表示されたら、MIDI シーケンサーで SRAM データの MIDI ファイルを再生する。



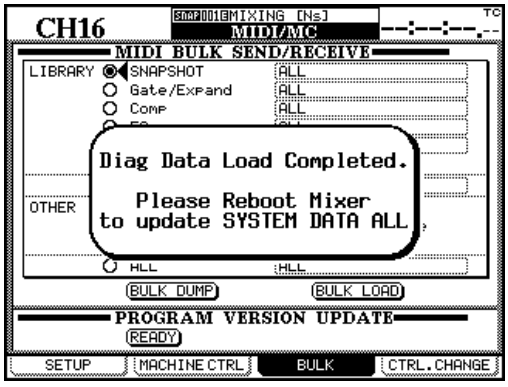

4. When playing the SRAM data, the next pop-up message will appear.

4. データを再生すると次の Pop-up メッセージが表示される。




5. Upon completion of the load, the next pop-up message will appear. When it does, turn the DM-24 off then back on to complete the procedure.

5. Load が完了すると次の Pop-up メッセージが表示されるので、DM-24 の電源を一度切ってから再投入すると完了。



# 5. UPDATING THE PROGRAM
プログラムアップデート

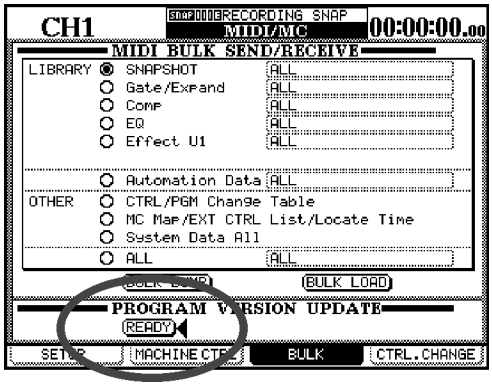
To update the program data, you need to play the following MIDI data in the order indicated using your MIDI Data Filer.

1. flash.mid (Program data about Program Update)
2. remote.mid (Remote Program Data)
3. main.mid (Program Data about Main CPU normal operation)
4. preset.mid (Preset Library Data )
5. diag.mid (Diagnostics Program Data )
6. start.mid (Main CPU StartUp Program Data)
7. panel.mid (Panel CPU Program Data)

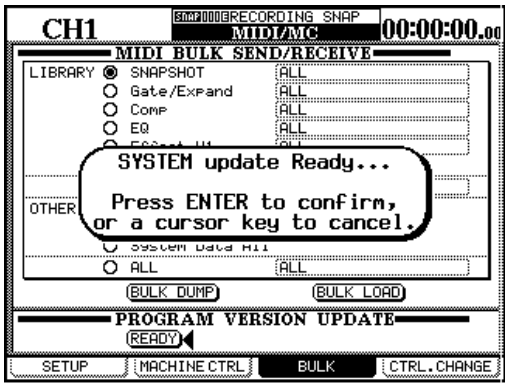
※ Depending on the version, the above MIDI data should be played in a different order. If necessary, follow the instructions for a specific version.

### [Procedure for Program Update]

1. Connect MIDI IN on the DM-24 to MIDI OUT on the MIDI Data Filer.
2. Get to the BULK sub-screen under the MIDI/MC screen, move the cursor to the [READY] button, then press ENTER.




3. Upon appearance of a pop-up stating: "SYSTEM update Ready....", as shown below, press ENTER.




※ There are unusual occasions where the pop-up is not followed by the one that is shown in step 4. If this is the case, turn the DM-24 off then back on and repeat steps 2 and 3.

下記のプログラムアップデート用 MIDI データを、MIDI Data Filer で下記の順番でひとつずつ再生しアップデートする。

1. flash.mid（Program Update の Program Data）
2. remote.mid（Remote Program Data）
3. main.mid（Main CPU 通常動作 Program Data）
4. preset.mid（Preset Library Data）
5. diag.mid（Diagnostics Program Data）
6. start.mid（Main CPU StartUp Program Data）
7. panel.mid（Panel CPU Program Data）

※ Version によっては上記順番と違う場合もある。
この場合は、その Version の手順書に従うこと。

### [Program Update の手順]

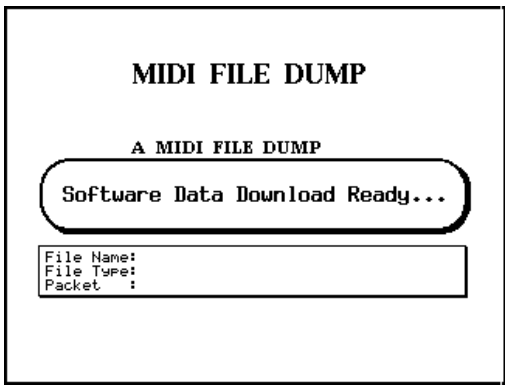
1. DM-24 の MIDI IN 端子と MIDI Data Filer の MIDI OUT 端子を接続する。
2. MIDI/MC 画面の BULK サブ画面を表示させ、カーソルを[READY]ボタンに合わせてから ENTER キーを押す。

3. 下図のように "SYSTEM update Ready..." と Pop-up が出たら、ENTER キーを押す。

※ まれにこの状態から 4 の状態に移行しない場合があるが、その場合は電源を再投入して 2 ～ 3 をやり直す。

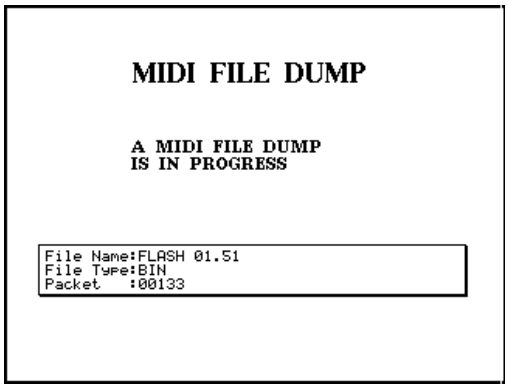
4. The screen changes to show the following pop-up stating: "Software Data Download Ready...".

4. 次の画面に切り替わり、"Software Data Download Ready..."という Pop-up が表示される。



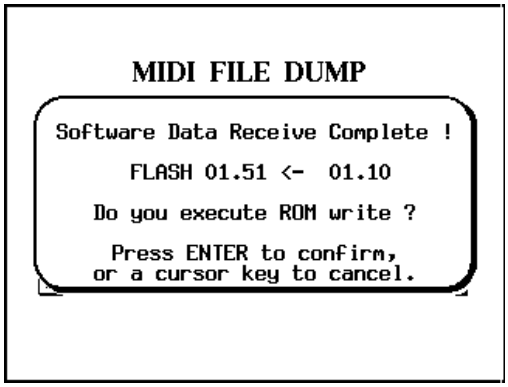

5. Upon appearance of the above pop-up, play the MIDI Data Filer having a .mid file you need to dump before any other one.
6. As shown below, the "File Name" field on the screen reads the file name and version number, the "File Type" field reads "BIN", and the number in the "Packet" field increments to show the data reception process.

5. 4 の状態になったら、指定された.mid ファイルを読み込んだ MIDI Data Filer を再生する。
6. 下図のように、画面の "File Name" 欄にファイル名と Verion 番号、"File Type" 欄に "BIN"と表示され、"Packet" 欄の数字がデータ受信に伴ってインクリメントされる。




7. When the MIDI Data Filer plays the file all the way to the end and the next pop-up message appears, confirm the version number and press ENTER.

7. MIDI Data Filer の再生が終わり、次の Pop-up メッセージが表示されたら、Version 番号を確認し ENTER キーを押す。



8. The screen changes to show one of those shown below.

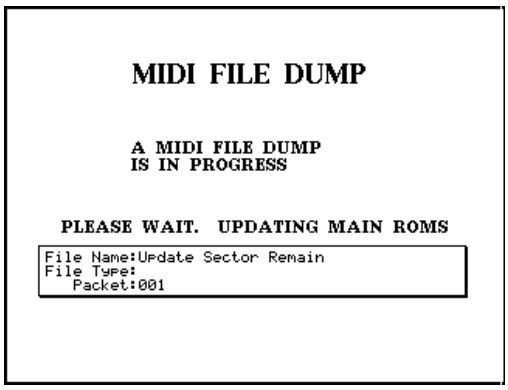
● After having played other files than the panel.mid:

You may get the message "PLEASE WAIT. UPDATING MAIN ROMS" blinking on the screen and upon completion of the ROM update, the DM-24 automatically restarts.

8. 以下の表示に切り換わる。

● panel.mid 以外の再生後

下図のように、"PLEASE WAIT. UPDATING MAIN ROMS"と画面に点滅表示され、ROM アップデートが完了すると自動的に再起動する。




● After having played the panel.mid file.

"Sector xx.download..erase..write..verify..done." is displayed over than 10 times, followed by "ROM update finished, restarting Mixer", and then the DM-24 automatically restarts.

● panel.mid の再生後

下図のように、"Sector xx.download..erase..write..verify..done."と 10 数回表示された後、"ROM update finisied, restarting Mixer"と言う表示が出てしばらくすると自動的に再起動する。




※ Repeat steps 1-8 seven times to dump all the necessary seven files from the flash.mid to the panel.mid.

Remember that we have not checked the ROM Data for legality when the .mid files are dumped in an arbitray order.

Nothing is written on the ROM until you press ENTER in step 7, so if you made a mistake in selecting a .mid file before you reach step 7, you can abort the procedure and redo from the beginning after turning the DM-24 off then back on.

※上記手順 1 ～ 8 を flash.mid ～ panel.mid の順番通り、7 回繰り返す。

順番を変えて実行した場合での ROM Data の正当性確認はしていないので注意すること。

但し、7 の状態で ENTER キーを押すまでは ROM 書き込みを実行しないので、7 以前ならば順番を間違えても電源再投入してやり直しが可能。

**CAUTION:**

NEVER switch off the power when the screen reads any of the messages shown in step 8. If you did so, run the following procedure because, even if the unit seemingly works dependably, the correct operation is not guaranteed.

[If you switched off the power after having played the flash.mid/panel.mid file and when a specific message is shown in step 8]:

Recycling the power would result in a totally white or black screen, the unit not working properly. To get around the problem, run the following procedure.

a) Remove the ROMs (U6, U7, and U31) on the MAIN PCB and use the ROM WRITER to run the Program Update.
b) Install the ROMs removed in step a) and switch on power to the DM-24. Powered up, it shows the screen you were at in step 4.
c) For the flash.mid file, repeat steps 5-8 corrrectly.
d) When the DM-24 automtically restarts after you have performed step 8, if nothing goes wrong with the restart, you can think that the Program Update was successfull.

[If you switched off the power after having played any other than the flash.mid/panel.mid file and when a specific message is shown in step 8]:

a) Switch on power to the DM-24 and it starts showing the screen you were at in step 4.
b) For the .mid file during the play of which you switched off the power, repeat steps 5-8.
c) The DM-24 automtically restarts after you have performed step 8, then perform steps 1-8 correctly for the remaining .mid files.
d) When you have done with all the .mid files, the Program Update is complet.

**注意）**

手順 8 の表示が出ている間は、絶対に電源を切らないこと。もし電源を切ってしまった場合、その後動作している様に見えても正常動作を保証出来なくなるので、下記の手順を実行する。

**[flash.mid/panel.mid 再生後、手順８の表示が出ている間に電源を切ってしまった場合]:**

この場合、電源を再投入しても真っ白または真っ黒な画面が表示され正常に動作しないので、下記の手順を実行する。

a）MAIN PCB の ROM（U6, U7, U31）を外し、ROM WRITER で Program Update を実行する。
b）a の ROM を装着し電源を投入すると、手順 4 の画面で起動する。
c）flash.mid ファイルについて手順 5 ～ 8 までを正しくやり直す。
d）手順 8 後、自動的に再起動したとき、正常に起動したら Program Update 終了。

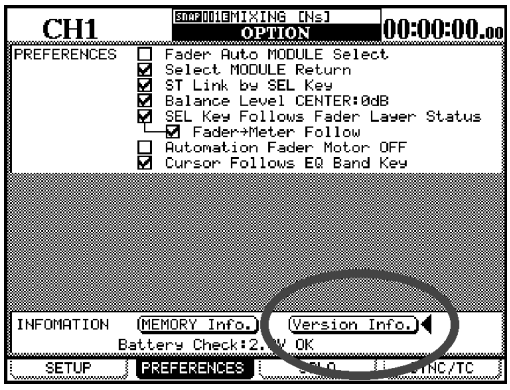
**[flash.mid/panel.mid 以外を再生後、手順８の表示が出ている間に電源を切ってしまった場合]:**

a）電源を投入すると、手順 4 の画面で起動する。
b）電源を切ってしまったときの mid ファイルを、手順 5 ～ 8 までやり直す。
c）手順 8 後、自動的に再起動するので、残りの mid ファイルについて手順 1 ～ 8 までを正しく実行する。
d）全てのファイルにおいて正しく実行したら、Program Update 終了。

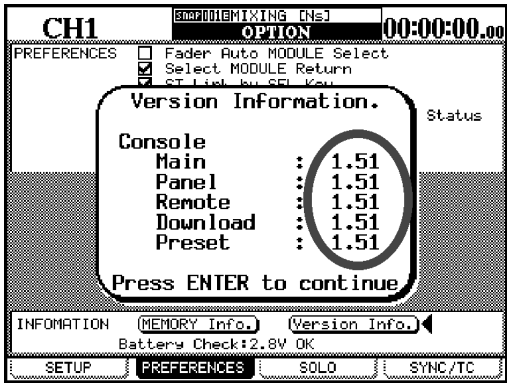
## [Procedures for Checking the Version Number and Initializing the SRAM]

Upon completion of the Program Update, check the Version Number and initialize the SRAM, as follows.

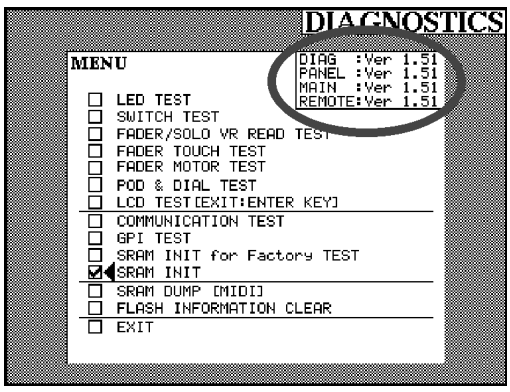
1. Get to the PREFERENCES sub-screen under the OPTION screen, move the curosr to the [Version Info.] button, and press ENTER.




2. Check the pop-ups for the same version number both for the Console and for the Effector.




3. Switch off the power, then, while holding down 2ND F. + EQUALIZER [HIGH] + LIBRARY [-], switch the power back on to let the DIAGNOSTICS screen appear.
The update was successful if the updated version number is shown in the upper right corner of the screen.

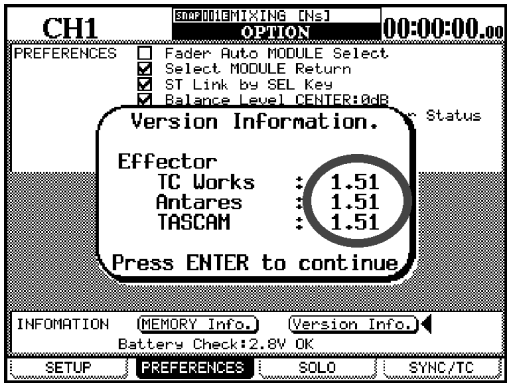



## [Version 番号確認と SRAM 初期化の手順]

Program Update が完了したら、下記の手順で Version 番号を確認し、SRAM 初期化を実行する。

1. OPTION 画面の PREFERENCES サブ画面を表示させ、カーソルを [Version Info.]ボタンに合わせてから ENTER キーを押す。

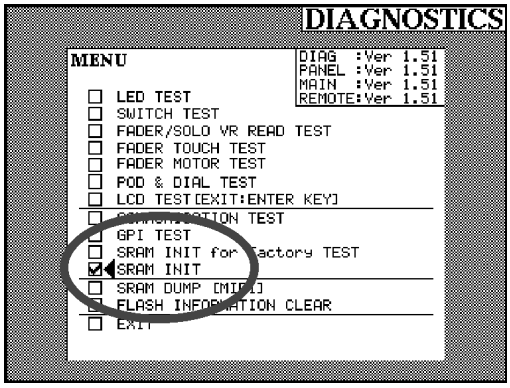
2. Pop-up の内容を確認し、Console/Effector とも全てが Version Up した番号で表示されたら OK。




3. 一旦電源を切ってから、2ND F.キー＋ EQUALIZER [HIGH]キー＋ LIBRARY [-]キーを押しながら電源を投入し、DIAGNOSTICS を起動させる。
このとき、画面右上に Version Up した番号が表示されたら OK.。

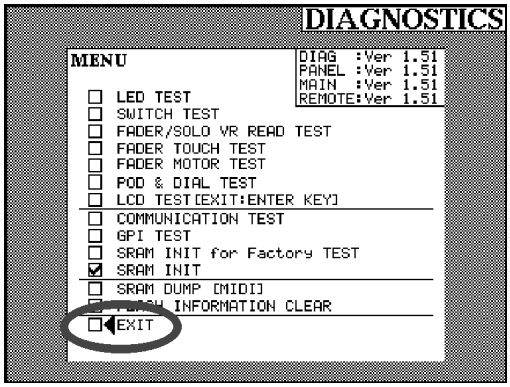
4. Move the cursor to the SRAM INIT option and press ENTER to run SRAM INIT.

4. SRAM INIT にカーソルを合わせて ENTER キーを押し、SRAM INIT を実行する。




5. Move the cursor to the EXIT option and press ENTER to leave the DIAGNOSTICS screen.

5. EXIT にカーソルを合わせて ENTER キーを押し、DIAGNOSTICS を終了させる。



# 6. ERROR MESSAGES
エラーメッセージ

**OS ERROR [***-*****XXX-**]**

| XXX<br>(ERROR CODE) | MEANING<br>意味 | REMEDY<br>対策 |
|---|---|---|
| 1A7 | The polling failed, causing an illegal interruption to occur.<br><br>ポーリング失敗で、割り込みが異常発生した。 | Disconnect all the devices. If this fixed the problem, chances are some of the disconnected devices are factors in the trouble.<br><br>接続されている機器を全て外す。改善した場合、外した機器のいずれかに原因がある可能性がある。 |
| 4B7 | The cueing caused overflow and an illegal interruption occured.<br><br>キューイングオーバーフローで、割り込みが異常発生した。 | Disconnect all the devices. If this fixed the problem, chances are some of the disconnected devices are factors in the trouble.<br><br>接続されている機器を全て外す。改善した場合、外した機器のいずれかに原因がある可能性がある。 |
| 8DE | The address was illegal.<br><br>アドレスが不正であった。 | Check the U6 and U7 on the MAIN PCB and its peripheral circuits for signs of poor contact or bad soldering. If these mesures are of no avail, replace the ROM at U6 and U7.<br><br>MAIN PCB の U6、U7 および周辺回路に接触不良や半田不良がないかどうか確認。改善しない場合、U6、U7 の ROM 交換。 |
| 2AA | The program operates irregularly or some hardware that are relevant to the program operation are at fault (error conditions in/poor contact at ICs, bad soldering, etc.)<br><br>プログラムが異常、またはプログラムの動作に関係するハードウェアの不良 (IC 不良、IC の接触不良、半田不良)。 | Run the SRAM Initialization. If this is of no avail, replace the ROM at U6 and U7 on the MAIN PCB. If this also is of no avail, write down all error messages and check with the Tokyo Service.<br><br>SRAM Initialize を行なう。解決しない場合、MAIN PCB U6、U7 の ROM 交換。それでも解決しない場合、エラーメッセージ全てをメモし、CP 国内サービスに問い合わせる。 |
| 2AB | | |
| 5BB | | |
| 7C2 | | |
| 7C5 | | |
| 7C8 | | |
| 7CA | | |
| 7CB | | |
| 7CC | | |
| 7CD | | |
| 7CF | | |
| 8D5 | | |
| 8D7 | | |
| 8D9 | | |
| 8DA | | |
| 8DD | | |
| 8DF | | |
| 9E9 | | |
| 9EC | | |
| 9ED | | |

**CPU ERROR [00-00000XXX-**]**

| XXX<br>(ERROR CODE) | MEANING<br>意味 | REMEDY<br>対策 |
|---|---|---|
| 000 | The power-on reset was not conducted correctly.<br><br>パワーオンリセットが正常に行なわれなかった。 | Check if the reset signal ( ⌐└┘ ) is issued from pin no.1 of U3 on the MAIN PCB at power-up. If no problem is found, check U2, U6, U7, U8 and U10 on the MAIN PCB as well as their peripehral circuits for signs of poor contact or bad soldering.<br><br>電源投入後、MAIN PCB のU3 1番ピンより、リセット信号 ( ⌐└┘ ) が出力されているかどうか確認。正常な場合、MAIN PCB のU2、U6、U7、U8、U10 および周辺回路に接触不良または半田不良がないかどうか確認。 |
| 001 | The stack pointer was illegal.<br><br>スタックポインターが不正であった。 | Check U10 on the MAIN PCB and its peripehral circuits for signs of poor contact or bad soldering.<br><br>MAIN PCB のU10 および周辺回路に接触不良または半田不良がないかどうか確認。 |
| 004 | An illegal command was issued.<br>命令が不正であった。 | Check U6 and U7 on the MAIN PCB and its peripehral circuits for signs of poor contact or bad soldering.<br><br>MAIN PCB のU6, U7 および周辺回路に接触不良または半田不良がないかどうか確認。 |
| 009 | A CPU address error occured.<br>CPUアドレスエラーが発生した。 | |
| 011 | An illeggal interruption signal was issued.<br><br>割り込み信号が不正であった。 | Check that pin no.76 of U11 on the MAIN PCB is at 5V.<br><br>MAIN PCB のU11 76番ピンが5V になっているかどうか確認。 |
| 002 | The program operates irregularly or some hardware that are relevant to the program operation are at fault (error conditions in/poor contact at ICs, bad soldering, etc.)<br><br>プルグラムが異常、またはプログラムの動作に関係するハードウェアの不良（IC 不良、IC の接触不良、半田不良)。 | Run the SRAM Initialization. If this is of no avail, replace the ROM at U6 and U7 on the MAIN PCB. If this also is of no avail, write down all error messages and check with the Tokyo Service.<br><br>SRAM Initialize を行なう。解決しない場合、MAIN PCB U6、U7 のROM 交換。それでも解決しない場合、エラーメッセージ全てをメモし、CP 国内サービスに問い合わせる。 |
| 003 | | |
| 005 | | |
| 006 | | |
| 007 | | |
| 008 | | |
| 010 | | |
| 012 | | |
| 013-031 | | |
| 032-063 | | |
| 064 | | |
| 065 | | |
| 066 | | |
| 067 | | |
| 068 | | |
| 069 | | |
| 070 | | |
| 071 | | |
| 072-255 | | |

**PANEL ERROR [PP-XXXXXXXX-YY]**

| XXXXXXXX<br>(ERROR CODE) | YY<br>(ERROR CODE) | MEANING<br>意味 | REMEDY<br>対策 |
|---|---|---|---|
| 11111111 | 05 | Commands sent into the panel CPU overflowed.<br><br>パネル CPU に入力されるコマンドがオーバーフローした。 | Disconnect all the devices. If this fixed the problem, chances are some of the disconnected devices are factors in the trouble.<br><br>接続されている機器を全て外す。改善した場合、外した機器のいずれかに原因がある可能性がある。 |
| B5xxxxxx | 06 | An illegal Flash ROM update command is issued.<br><br>異常な Flash ROM アップデートコマンドが発生した。 | Recycle the power and redo the MIDI download. If this is of no avail, write down all error messages and check with the Tokyo Service.<br><br>電源再投入し、MIDI ダウンロードをやり直す。<br>それでも解決しない場合、エラーメッセージ全てをメモし、CP 国内サービスに問い合わせる。 |

**PANEL ERROR [PP-********-YY]**

| YY<br>(ERROR CODE) | MEANING<br>意味 | REMEDY<br>対策 |
|---|---|---|
| 07 | A pop-up message tried to produce more than 64 characters in a single line.<br><br>ポップアップメッセージに、1 行 64 文字以上出そうとした。 | Write down all error messages and check with the Tokyo Service.<br><br>エラーメッセージ全てをメモし、CP 国内サービスに問い合わせる。 |
| 99 | An undefined interruption occured.<br><br>未定義の割込が発生した。 | Run the SRAM Initialization. If this is of no avail, replace the ROM at U31 on the MAIN PCB. If this also is of no avail, write down all error messages and check with the Tokyo Service.<br><br>SRAM Initialize を行なう。解決しない場合、MAIN PCB U31 の ROM 交換。それでも解決しない場合、エラーメッセージ全てをメモし、CP 国内サービスに問い合わせる。 |

**PANEL ERROR [PP-*****XXX-99]**

| XXX<br>(ERROR CODE) | MEANING<br>意味 | REMEDY<br>対策 |
|---|---|---|
| 002<br>003<br>005<br>006<br>007<br>008<br>010<br>012<br>013-031<br>032-063<br>064<br>065<br>066<br>067<br>068<br>069<br>070<br>071<br>072-255 | The program operates irregularly or some hardware that are relevant to the program operation are at fault (error conditions in/poor contact at ICs, bad soldering, etc.)<br><br>プログラムが異常、またはプログラムの動作に関係するハードウェアの不良（IC 不良、IC の接触不良、半田不良）。 | Run the SRAM Initialization. If this is of no avail, replace the ROM at U31 on the MAIN PCB. If this also is of no avail, write down all error messages and check with the Tokyo Service.<br><br>SRAM Initialize を行なう。解決しない場合、MAIN PCB U31 の ROM 交換。それでも解決しない場合、エラーメッセージ全てをメモし、CP 国内サービスに問い合わせる。 |

**PANEL ERROR [PP-XX******-00]**

| XX<br>(ERROR CODE) | MEANING<br>意味 | REMEDY<br>対策 |
|---|---|---|
| 01 | Commands sent out of the panel CPU overflowed.<br>The program operates irregularily or some hardware that are relevant to the program operation are at fault, preventing the Main CPU to operate.<br><br>パネル CPU が出力するコマンドがオーバーフローした。<br>プログラムが異常、またはプログラム動作に関係するハードウェアの不良により Main CPU が動作していない。 | Check if any SEL switches are held down.<br><br>SEL スイッチのいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |
| 02 | | Check if any SOLO switches are held down.<br><br>SOLO スイッチのいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |
| 03 | | Check if any MUTE switches are held down.<br><br>MUTE のいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |
| 04 | | Check if any switches are held down in the Module Control and Layer Control Sections.<br><br>Module Control Section または Layer Control Section のいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |
| 05 | | Check if any switches are held down in the Machine Control Section.<br><br>Machine Control Section のいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |
| 06 | | Check if any switches are held down in the Automation Section.<br><br>Automation Section のいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |
| 07 | | Check if any switches are held down in the Monitoring Section.<br><br>Monitoring Section のいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |
| 08 | | Check if any switches are held down in the Parameter Control Section.<br><br>Parameter Control Section のいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |
| 09 | | Check if any switches are held down in the Library Section.<br><br>Library Section のいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |
| 0A | | Check if any switches are held down in the Meter Bridge Control Section.<br><br>Meter Bridge Control Section のいずれかのスイッチが、押されっ放しになっていないかどうか確認。 |

**PANEL ERROR [PP-XX******-00]**

| XX<br>(ERROR CODE) | 意味 | 対策 |
|---|---|---|
| 31 | Commands sent out of the panel CPU overflowed.<br>The program operates irregularily or some hardware that are relevant to the program operation are at fault, preventing the Main CPU to operate.<br><br>パネル CPU が出力するコマンドがオーバーフローした。<br>プログラムが異常、またはプログラム動作に関係するハードウェアの不良により Main CPU が動作していない。 | Run the SRAM Initialization. If this is of no avail, replace the ROM at U6 and U7 on the MAIN PCB. If this also is of no avail, check if the pulse signal from the encoder/Dial (at pins 1 and 3 of SW35-43 on the PANEL PCB) does not burst off while nothing is operated. If it does, check each operating element and ICs on the signal path going to the input at U31 on the MAIN PCB for signs of bad soldering. If nothing wrong is found, write down all error messages and check with the Tokyo Service.<br><br>SRAM Initialize を行なう。解決しない場合、MAIN PCB U6, U7 の ROM 交換。それでも解決しない場合は、エンコーダ/Dial のパルス信号（PANEL PCB SW35-43 の 1, 3 番ピン）が、操作していないのに暴れていないかの確認をする。信号が暴れている場合は、各操作子本体や MAIN PCB U31 入力までの信号上の IC 等の半田付けをチェックする。信号に問題が無い場合は、エラーメッセージ全てをメモし、CP 国内サービスに問い合わせる。 |
| 41 | | Run the SRAM Initialization. If this is of no avail, replace the ROM at U6 and U7 on the MAIN PCB. If this also is of no avail, check if the read-off signal indicating the Fader/SOLO VR positions (at pin 2 of MFxxx - fader itseld - on the FADER PCB and pin 2 of VR1 on the C.ROOM PCB) does not busrt off while nothing is operated. If it does, check each operating element and ICs on the signal path going to the input at U31 on the MAIN PCB for signs of bad soldering. If nothing wrong is found, write down all error messages and check with the Tokyo Service.<br><br>SRAM Initialize を行なう。解決しない場合、MAIN PCB U6, U7 の ROM 交換。それでも解決しない場合は、Fader/Solo VR 位置の読み取り信号（FADER PCB MFxxx（フェーダー本体）の２番ピン／C.ROOM PCB VR1 の２番ピン）が、操作していないのに暴れていないかの確認をする。信号が暴れている場合は、各操作子本体や MAIN PCB U31 入力までの信号上の IC 等の半田付けをチェックする。信号に問題が無い場合は、エラーメッセージ全てをメモし、CP 国内サービスに問い合わせる。 |
| 43 | | Run the SRAM Initialization. If this is of no avail, replace the ROM at U6 and U7 on the MAIN PCB. If this also is of no avail, check if the read-off fader touch sense signal (at pins 2-9 of U13/pin 2 of U15 on the FADER PCB) does not burst off while nothing is operated. If it does, check each operating element and ICs on the signal path going to the input at U31 on the MAIN PCB for signs of bad soldering. If nothing wrong is found, write down all error messages and check with the Tokyo Service.<br><br>SRAM Initialize を行なう。解決しない場合、MAIN PCB U6, U7 の ROM 交換。それでも解決しない場合は、Fader の Touch Sense の読み取り信号（FADER PCB U13 の 2-9 番ピン／U15 の２番ピン）が、操作していないのに暴れていないかの確認をする。信号が暴れている場合は、各操作子本体や MAIN PCB U31 入力までの信号上の IC 等の半田付けをチェックする。信号に問題が無い場合は、エラーメッセージ全てをメモし、CP 国内サービスに問い合わせる。 |

**Other Error Messages　その他のエラー**

| |
|---|
| Fatal Error:<br>Unexpected Interrupt<br>PP-xxxxxxxx-xx<br><br>Please note for reference |

● Meaning: An illegal interruption signal is sent to the Panel CPU.
● Remedy: Restart the DM-24. If this does not fix the problem, write down all error messages and check with the Tokyo Service.

● 意味：異常な割り込み信号が、Panel CPU に送られた。
● 対策：再起動する。解決しない場合はエラーメッセージを全てメモし、CP 国内サービスに問い合わせる。

| |
|---|
| Fatal : Address Error<br>PC=xxxxxxxx SP=xxxxxxxx Stack=xxxxxxxx<br><br>xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx<br>xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx<br><br>Please note for reference |

● Meaning: The Panel CPU runs wild.
● Remdy: Restart the DM-24. If this does not fix the problem, write down all error messages and check with the Tokyo Service.

● 意味： Panel CPU が暴走している。
● 対策：再起動する。解決しない場合はエラーメッセージを全てメモし、CP 国内サービスに問い合わせる。

| |
|---|
| Init Flag never went to 0.<br>Very Bad.<br>Abandoning plug in |

● Meaning: Error occurred when Main CPU sent data to Effect DSP while starting.
● Remedy: Check Main PCB U106 (DSP), U105 (PLD), and their peripheral circuits for sings of bad soldering. If this does not fix the problem, replace U105.

● 意味：起動時、メイン CPU がエフェクト DSP にデータを送るときにエラーが発生した。
● 対策： MAIN PCB U106（DSP）または U105（PLD）、および周辺回路の半田不良等をチェックする。解決しない場合、U105 を交換する。

Power Supply Voltage (+5V) is too Low
for stable operation.

Please Restart DM-24.

● Meaning: The voltage drops on the +5V line or it has ever dropped.
● Remedy: Restart the DM-24. If this does not fix the problem, check if the power supply provides the prescribed voltage. If it does, chances are the AC voltage momentarily dropped. It is U3 on the MAIN PCB that controls the +5V line and, when something goes wrong on this line, check pin 8 of U3, R3, R52 and pin 76 of U33 which generate an interruption to pin 76 of the CPU (U33) for signs of bad soldering.

● 意味：+5V ラインの電圧が低下している、または、したことがある。
● 対策：再起動する。解決しない場合は、仕様どおりの電源電圧が供給されているか確認。電源電圧 が正常であれば、瞬低（AC が一瞬、低下した）の可能性あり。＋ 5V を監視しているのは MAIN PCB の U3 であり、異常があった場合は CPU（U33）の 76 ピンに割り込みをかけている、U3-8pin、R3、 R52、U33-76pin の半田付けをチェックする。

Out of Sram Range !
Initialize Sram Data?
xxch(xxx) xxxxxxxxxxxxx

Press ENTER to confirm,
or a cursor key to cancel.

● Meaning: The SRAM data is out of the way.
● Remedy: Run the SRAM Initialization. If this does not fix the problem, write down all error messages and check with the Tokyo Service.

● 意味： SRAM データが異常。
● 対策： SRAM Initialize を行なう。解決しない場合、エラーメッセージを全てメモし CP 国内サービスに問い合わせる。

Wait for ready read XX timeouts.

● Meaning: Something goes wrong in hardware having efffects on the Effector functions.
● Remedy: Check U106 on the MAIN PCB and its peripheral circuits for signs of bad soldering.

● 意味： Effecter 機能に関係するハード的な不良が発生した。
● 対策： MAIN PCB の U106 およびその周辺回路の半田不良等をチェックする。

Wait for ready write xx timeouts.

● Meaning: Something goes wrong in hardware having efffects on the Effector functions.
● Remedy: Check U106 on the MAIN PCB and its peripheral circuits for signs of bad soldering.

● 意味： Effecter 機能に関係するハード的な不良が発生した。
● 対策： MAIN PCB の U106 およびその周辺回路の半田不良等をチェックする。

No Battery

Can't save DM-24 system data.
Please contact TASCAM service.
Please ENTER to continue.

● Meaning: The voltage of the backup battery drops.
● Remedy: Get to the PREFERENCES sub-screen under the OPTION screen, and check if the Battery Check reads OK. If the message "Can't Save DM-24 System Date" is blinking, replace the battery.

● 意味：バックアップバッテリーの電圧が低下している。
● 対策： OPTION － PREFERENCE 画面中にある Battery Check が OK を表示しているかどうか確認。 Can't Save DM-24 System Data が点滅している場合は、Battery を交換する。

NaN occurred on the DSP

● Meaning: Aberrant data is detected in the audio signal in the DSP.
● Remedy: Run the SRAM Initialization. If this does not fix the problem, check U6 on the MAIN PCB for signs of poor contact and if necessary replace U6 or further check U71-U93 for signs of bad soldering.

● 意味： DSP 内のオーディオ信号に、異常なデータが検地された。
● 対策： SRAM Initialize を行なう。解決しない場合、MAIN PCB U6 の接触不良のチェックおよび交換、または MAIN PCB U71 ～ U73 の半田不良等をチェックする。

Invalid DSP ID at dsp_execute. (ID:x)

● Meaning: An illegal DPS ID was issued when commands were sent from the Main CPU to the DSP.
● Remedy: Run the SRAM Initialization. If this does not fix the problem, check U6 on the MAIN PCB for signs of poor contact and if necessary replace U6.

● 意味： Main CPU から DSP へのコマンド送信時、異常な DSP ID が送信された。
● 対策： SRAM Initialize を行なう。解決しない場合、MAIN PCB U6 の接触不良のチェックおよび交換を行なう。

Too many pkts at dsp_execute. (#:x)

● Meaning: Too may packets were specified when commands are sent from the Main CPU to the DSP.
● Remedy: Run the SRAM Initialization. If this does not fix the problem, check U6 on the MAIN PCB for signs of bad contact and if necessary replace U6.

● 意味： Main CPU から DSP へのコマンド送信時、指定パケット数が多すぎた。
● 対策： SRAM Initialize を行なう。解決しない場合、MAIN PCB U6 の接触不良のチェックおよび交換を行なう。

Invalid DSP ID at dsp_packetset. (ID:x)

● Meaning: An illegal DSP ID was specified when generating packets.
● Remedy: Run the SRAM Initialization. If this does not fix the problem, check U6 on the MAIN PCB for signs of poor contact and replace U6 as required.

● 意味： コマンドパケット作成時、指定 DSP ID が異常であった。
● 対策： SRAM Initialize を行なう。解決しない場合、MAIN PCB U6 の接触不良のチェックおよび交換を行なう。

Illegal ch number at srnd_bar [x]

● Meaning: The wrong CH number was specified when requesting that the bar display data for the SURROUND screen should be generated.
● Remedy: Run the SRAM Initialization. If this does not fix the problem, check U6 on the MAIN PCB for signs of poor contact and replace U6 as required.

● 意味： SURROUND 画面用 bar 表示データ作成要求で、CH 番号が異常であった。
● 対策： SRAM Initialize を行なう。解決しない場合、Main PCB U6 の接触不良のチェックおよび交換を行なう。

Effect Plug-in Load Incompleted.
TC Works : OK
Antares : Error
TASCAM : OK

Check Version Information.

Press ENTER to continue

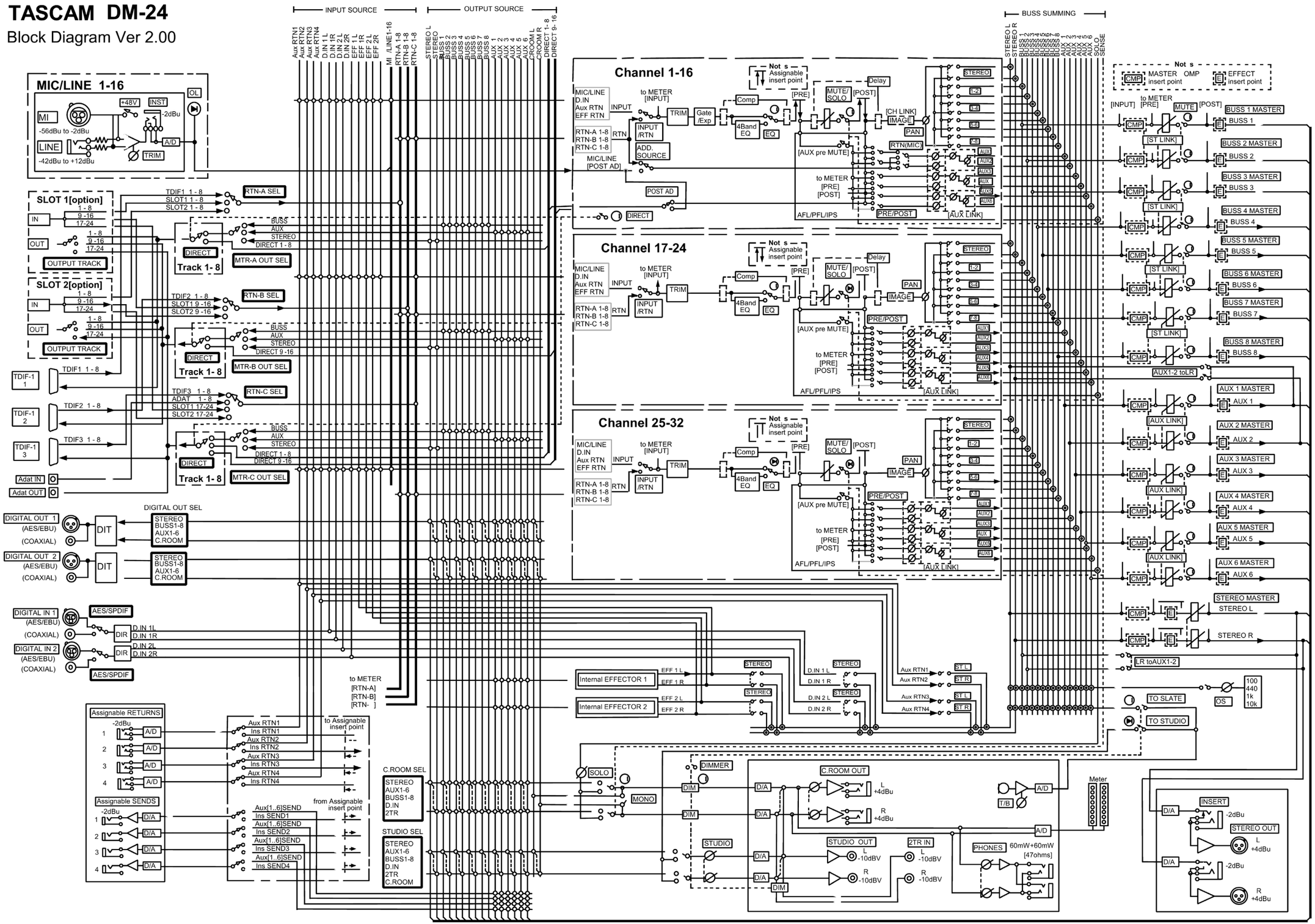
● Meaning: The softwear versions don't meet between the Panel CPU version and the Main CPU. Or erro occured in the Load process.
● Remedy: Make U31 (Panel) on the MAIN PCB consistent with U6 and U7 (Main) on the MAIN PCB in point of version. If their versions are originally met, restart the DM-24. If many times of restart do not fix the problem, try redoing the program update.

● 意味： パネル CPU とメイン CPU のソフトウェアーのバージョンが合っていない。または、Load 処理のエラー。
● 対策： MAIN PCB U31（パネル）と MAIN PCB U6、U7（メイン）のバージョンを合わせる。元々、バージョンが合っていた場合は再起動してみる。何度、再起動しても解決しない場合は、プログラムアップデートをやり直してみる。

# 7. BLOCK DIAGRAMS

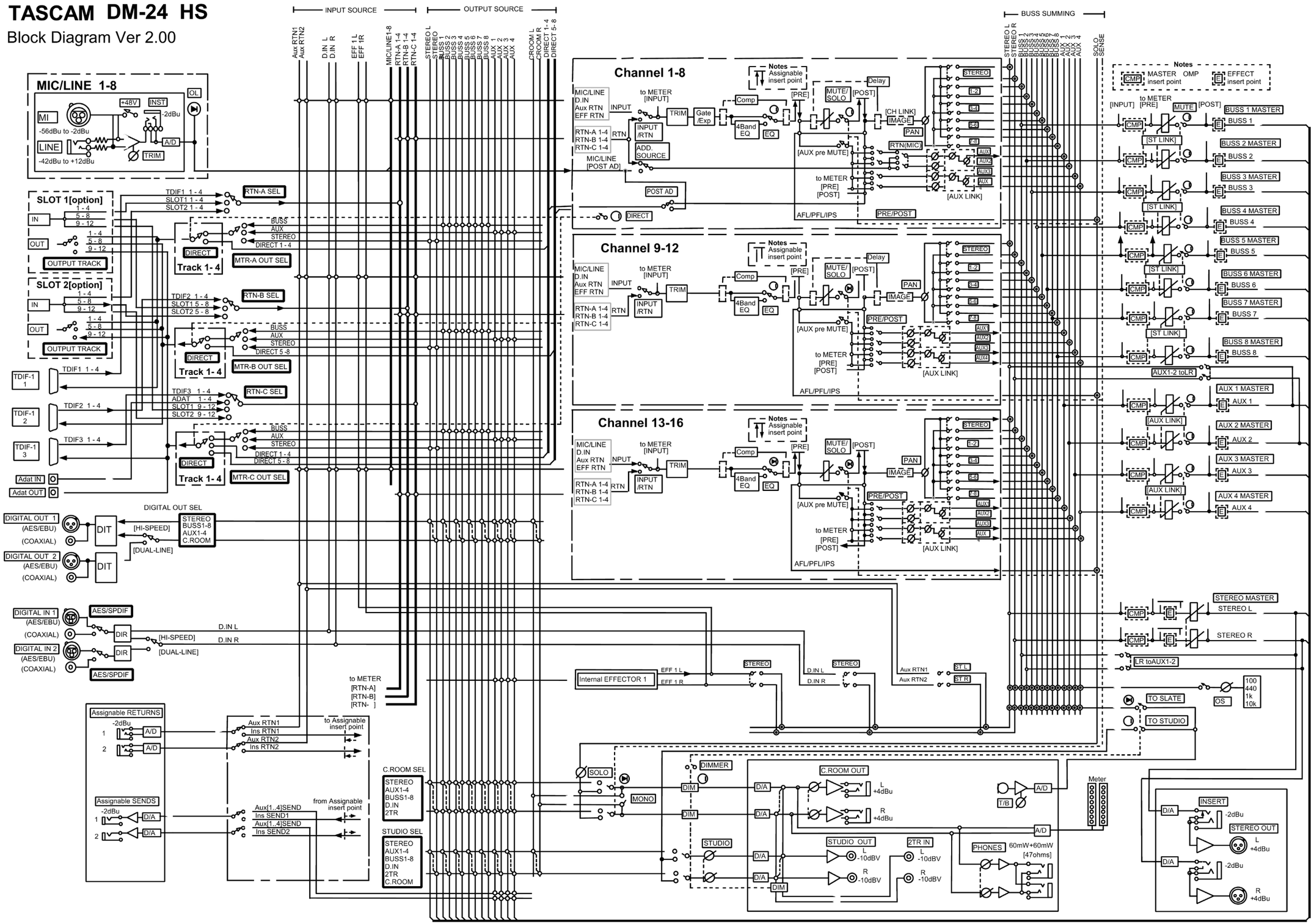
## TASCAM DM-24

Block Diagram Ver 2.00



# TASCAM DM-24 HS

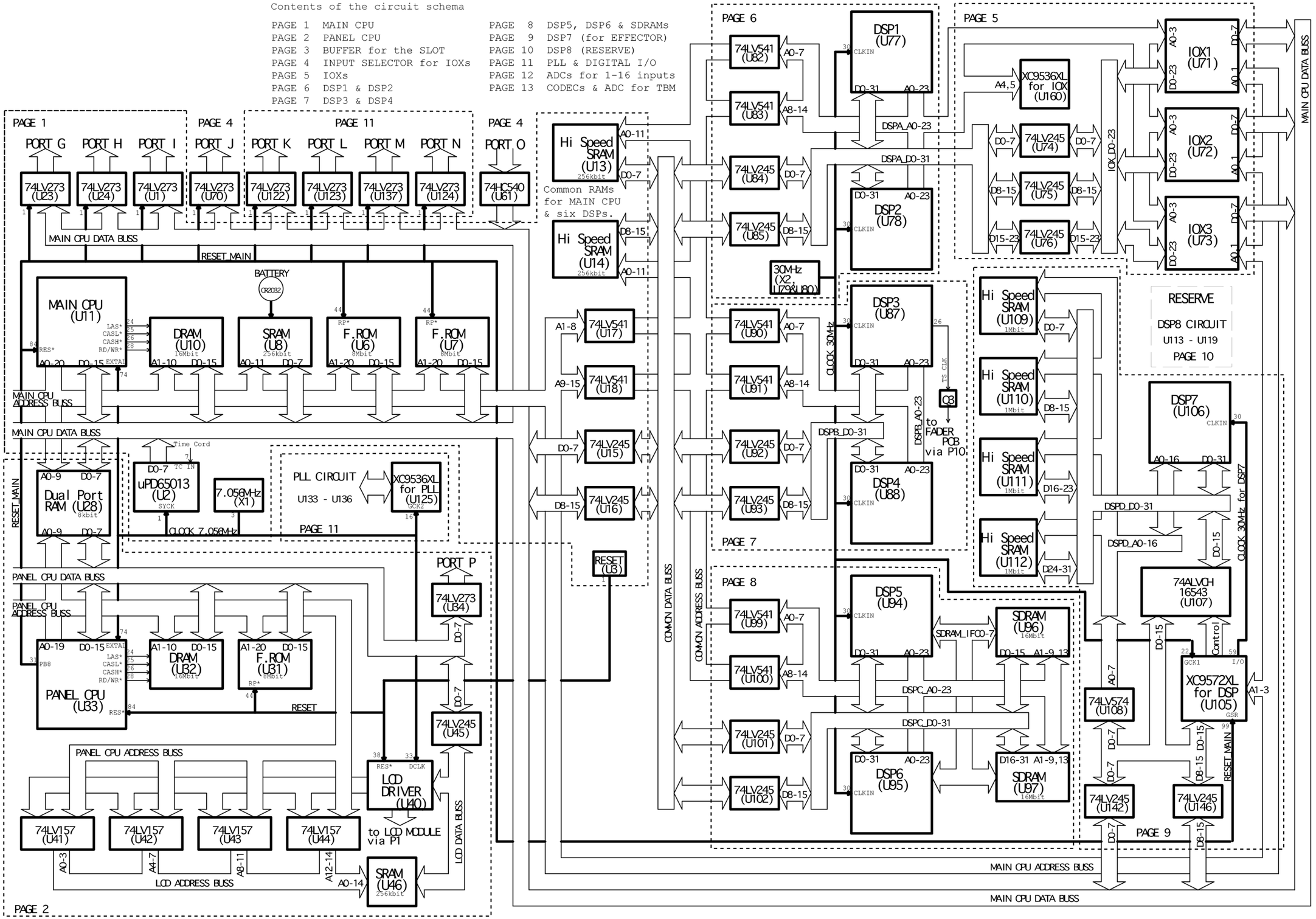
Block Diagram Ver 2.00



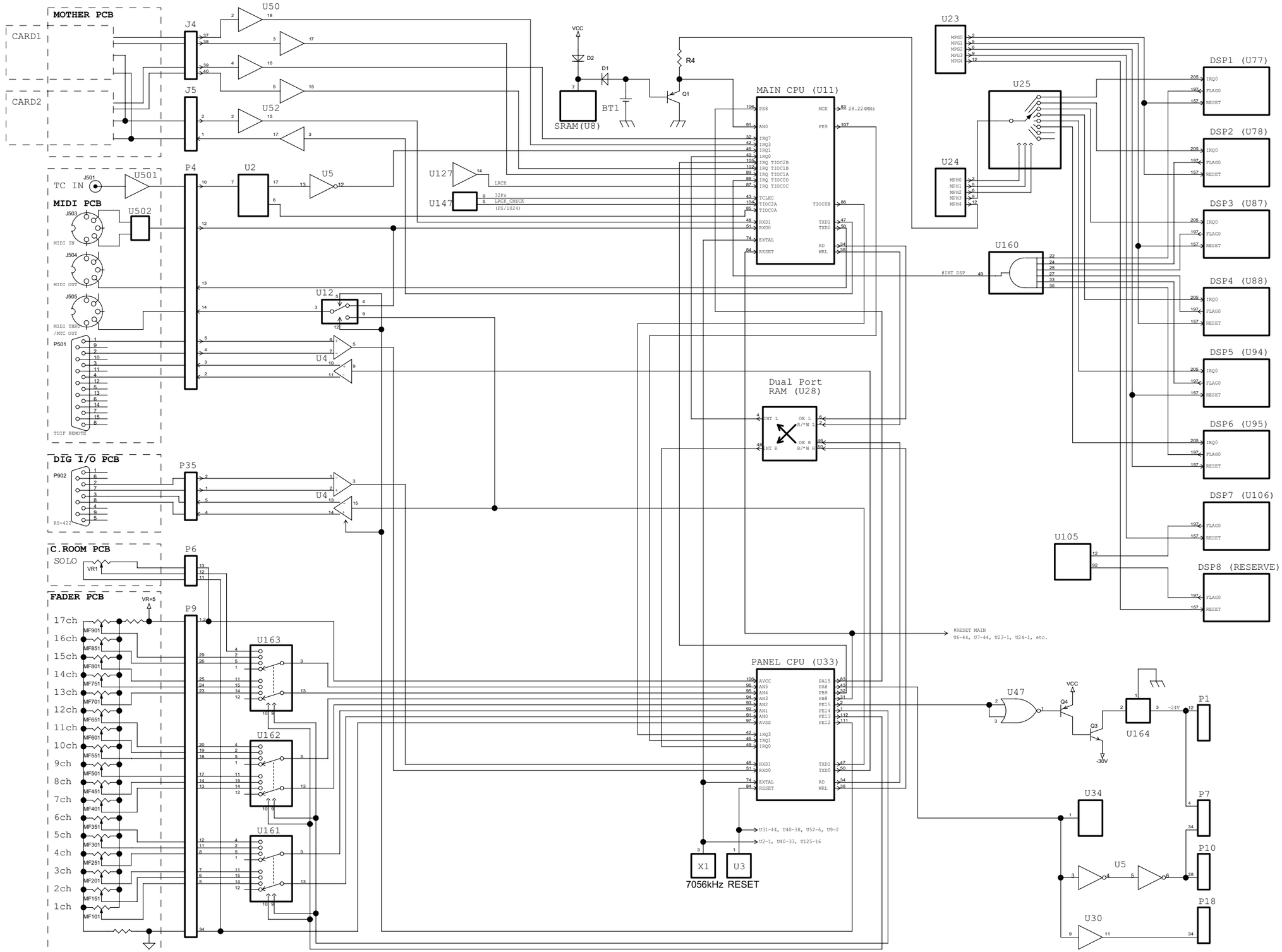
## MAIN PCB CPU BLOCK DIAGRAM (part 1)

Contents of the circuit schema


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PAGE 2 PANEL CPU
PAGE 3 BUFFER for the SLOT
PAGE 4 INPUT SELECTOR for IOXs
PAGE 5 IOXs
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PAGE 9 DSP7 (for EFFECTOR)
PAGE 10 DSP8 (RESERVE)
PAGE 11 PLL & DIGITAL I/O
PAGE 12 ADCs for 1-16 inputs
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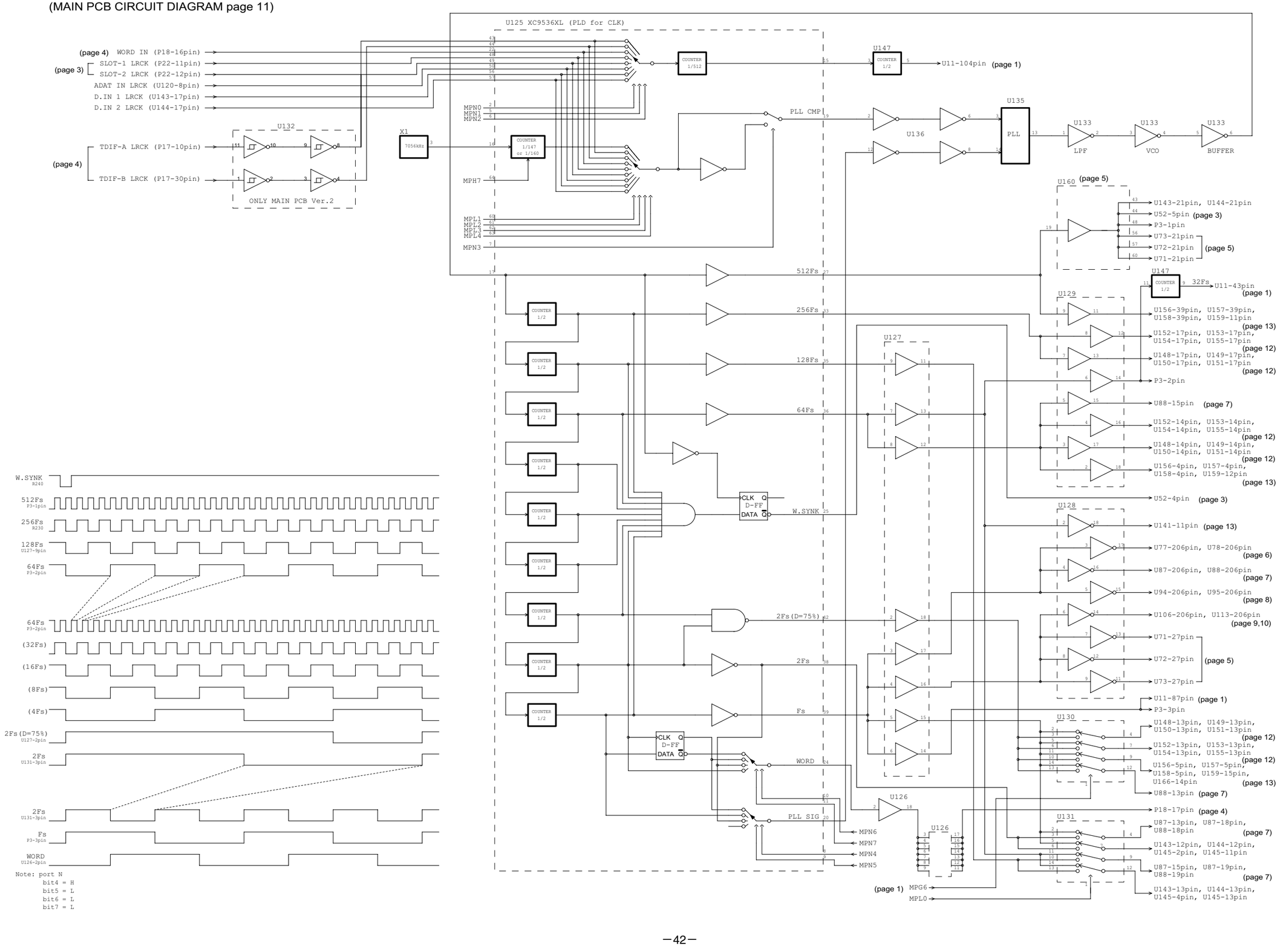



# MAIN PCB CPU BLOCK DIAGRAM (part 2)



# MAIN PCB CLOCK CIRCUIT BLOCK DIAGRAM

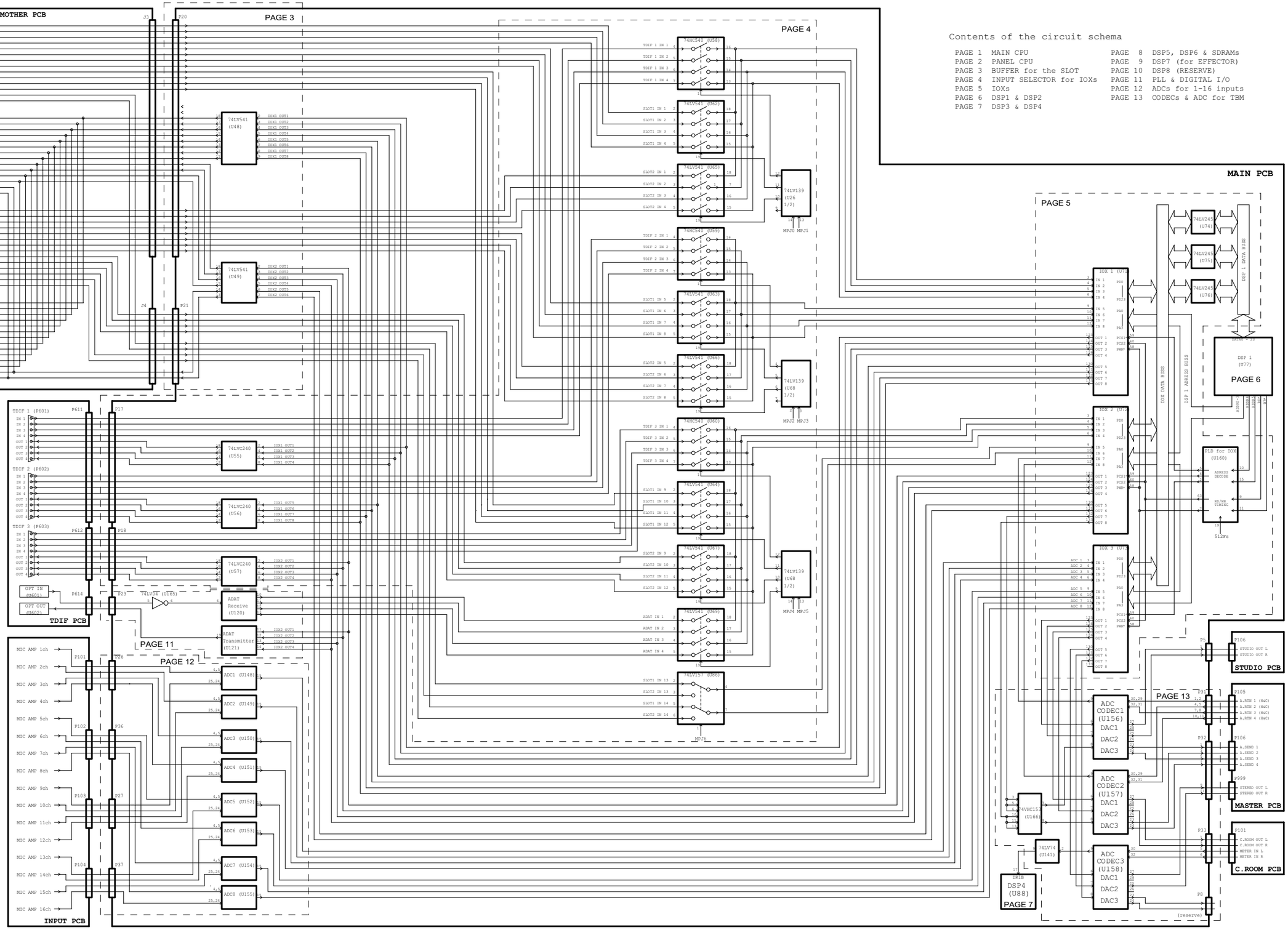
(MAIN PCB CIRCUIT DIAGRAM page 11)



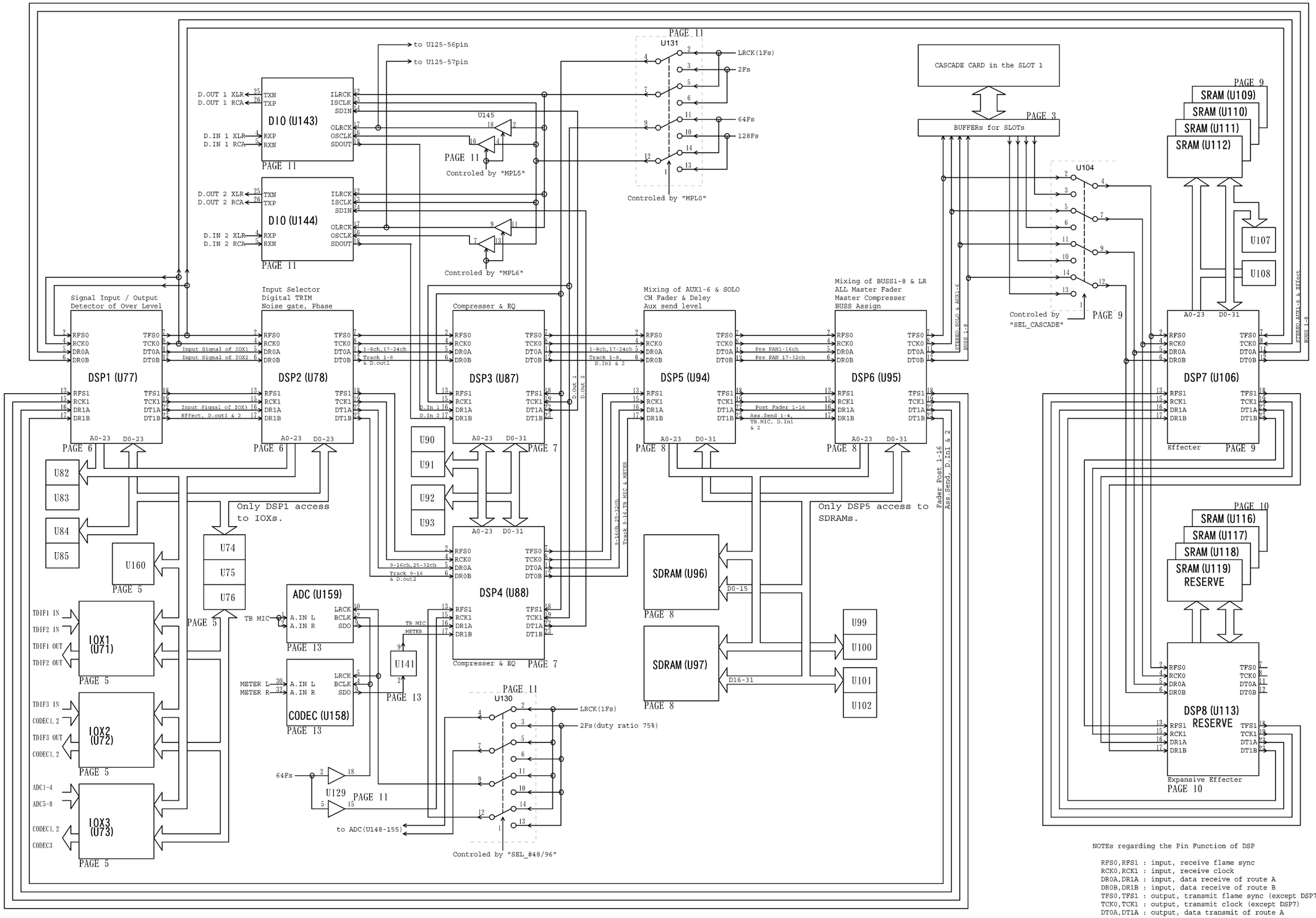
# MAIN PCB IOX BLOCK DIAGRAM

Contents of the circuit schema


| | | | |
|---|---|---|---|
| PAGE 1 | MAIN CPU | PAGE 8 | DSP5, DSP6 & SDRAMs |
| PAGE 2 | PANEL CPU | PAGE 9 | DSP7 (for EFFECTOR) |
| PAGE 3 | BUFFER for the SLOT | PAGE 10 | DSP8 (RESERVE) |
| PAGE 4 | INPUT SELECTOR for IOXs | PAGE 11 | PLL & DIGITAL I/O |
| PAGE 5 | IOXs | PAGE 12 | ADCs for 1-16 inputs |
| PAGE 6 | DSP1 & DSP2 | PAGE 13 | CODECs & ADC for TBM |
| PAGE 7 | DSP3 & DSP4 | | |

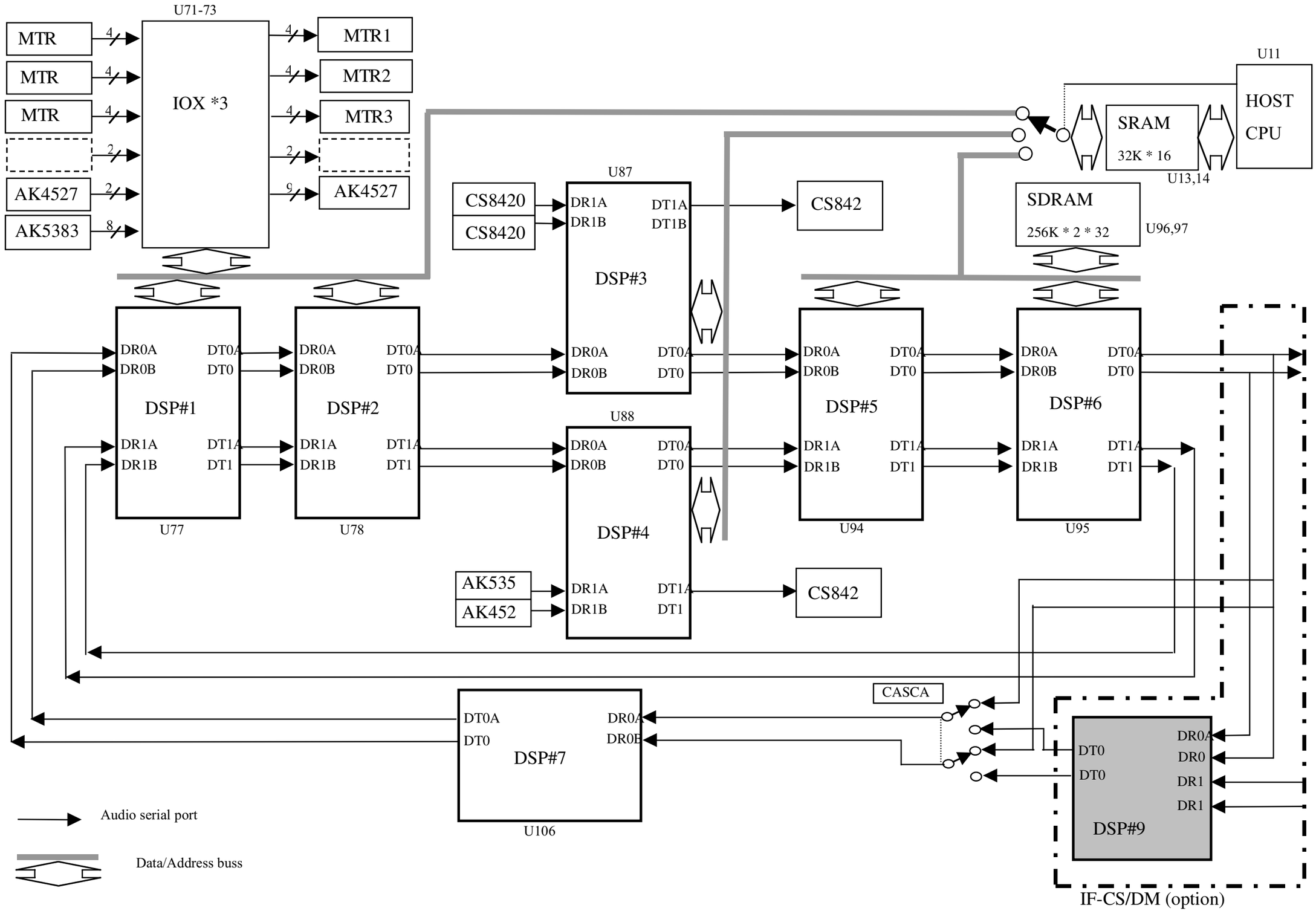
# MAIN PCB DSP BLOCK DIAGRAM



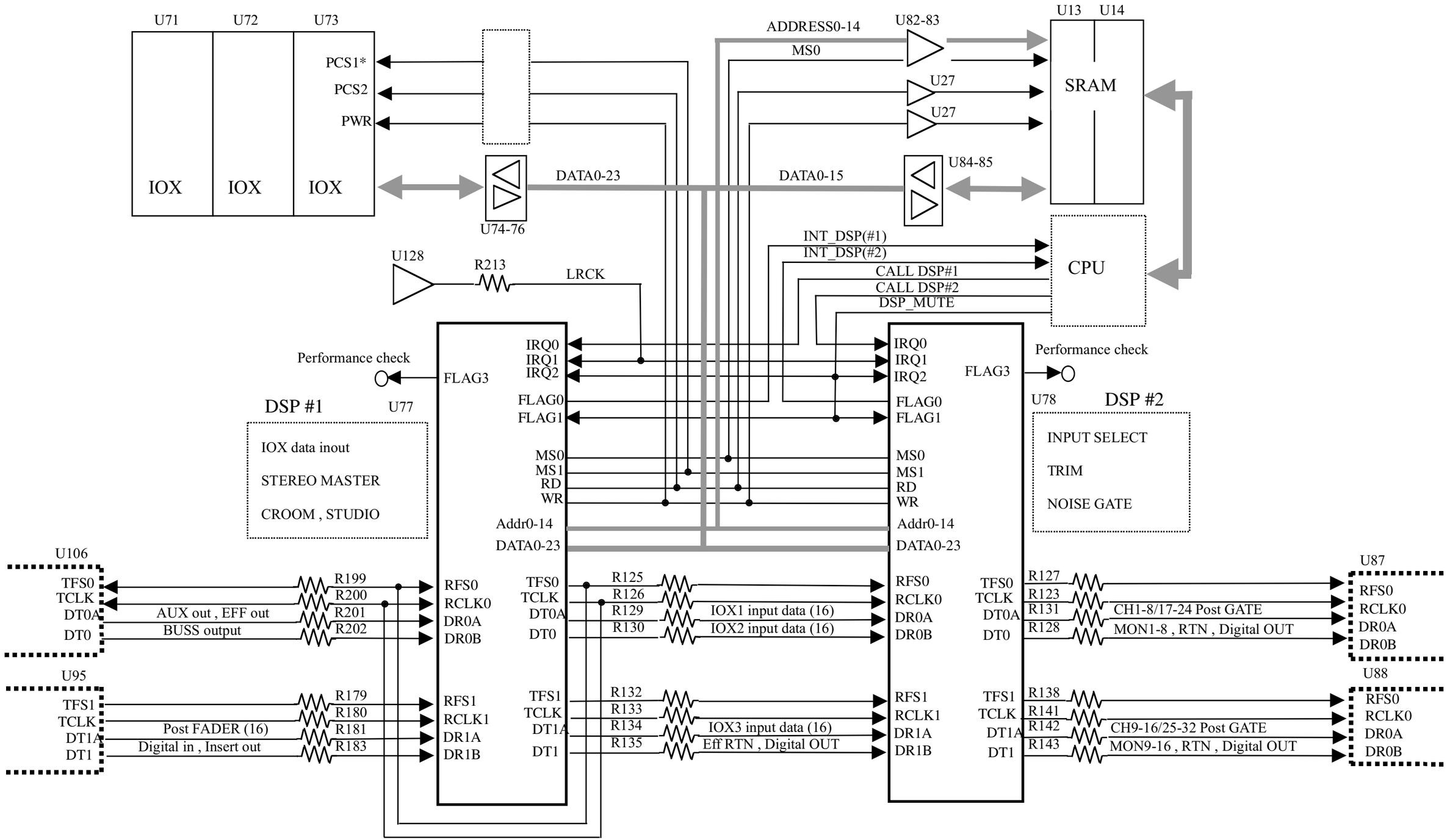

NOTEs regarding the Pin Function of DSP

RFS0,RFS1 : input, receive flame sync
RCK0,RCK1 : input, receive clock
DR0A,DR1A : input, data receive of route A
DR0B,DR1B : input, data receive of route B
TFS0,TFS1 : output, transmit flame sync (except DSP7)
TCK0,TCK1 : output, transmit clock (except DSP7)
DT0A,DT1A : output, data transmit of route A
DT0B,DT1B : output, data transmit of route B

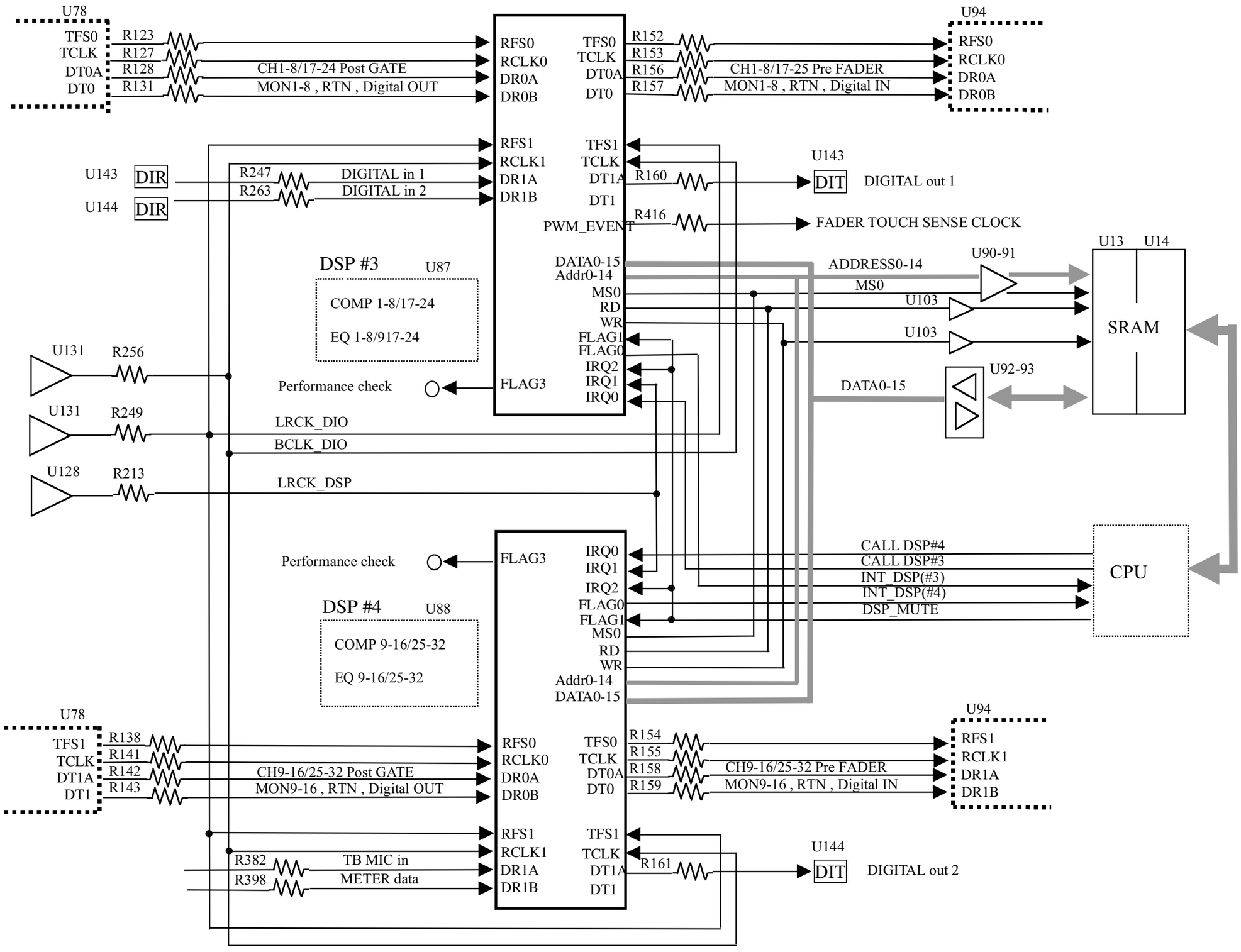
**MAIN PCB DSP Architecture 1/6 (Overview)**



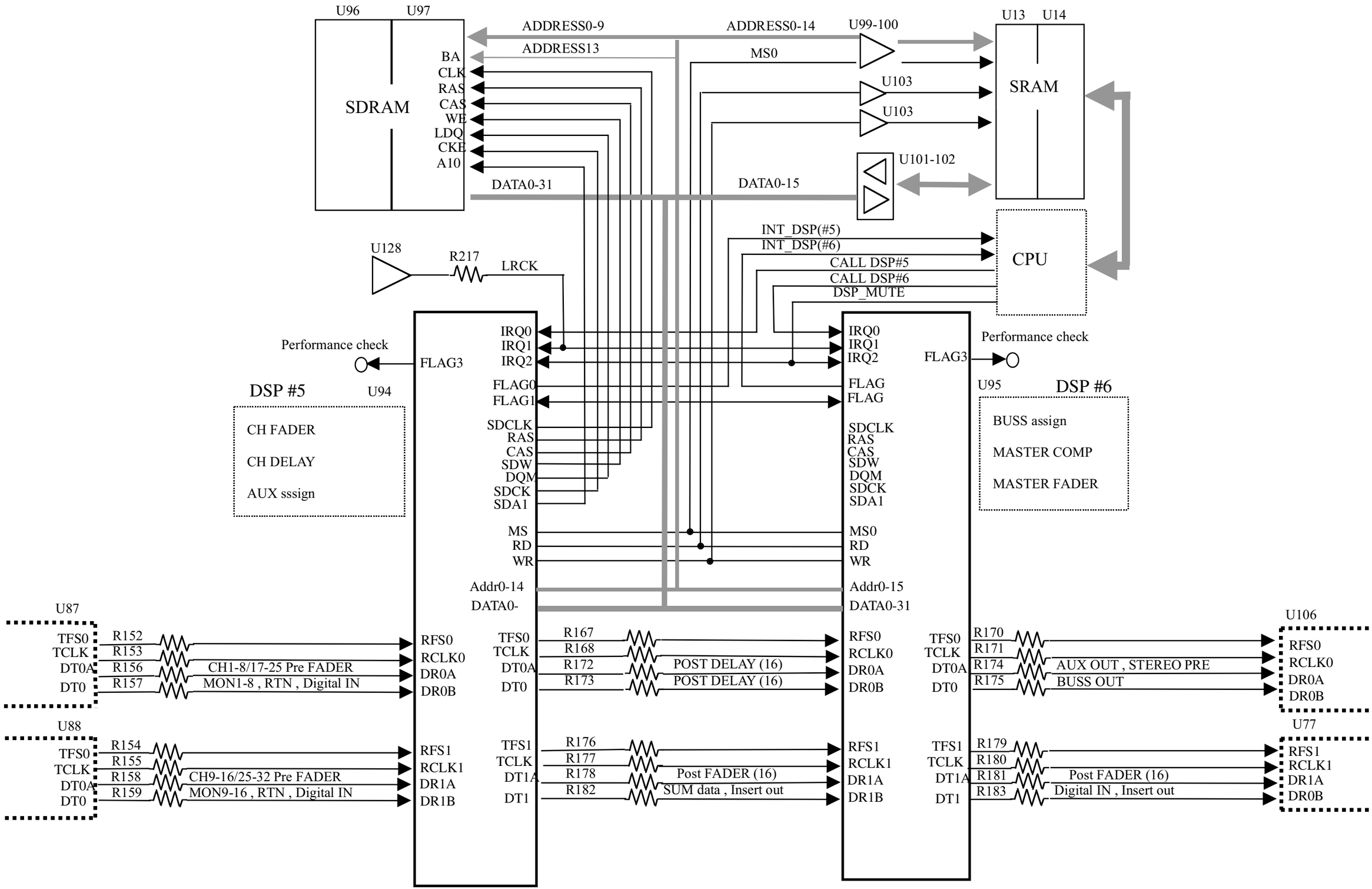
**MAIN PCB DSP Architecture 2/6 (DSP #1 & 2)**



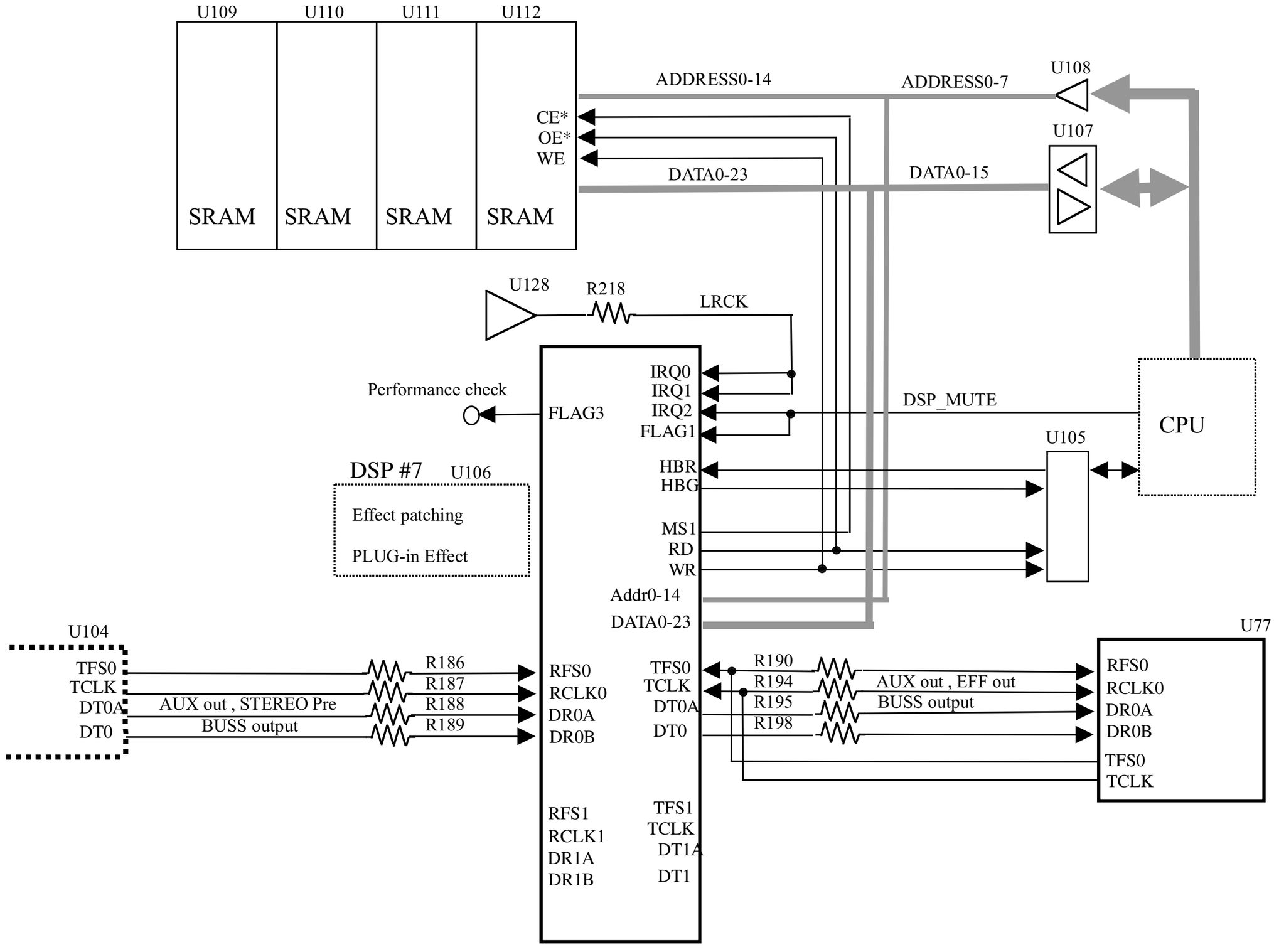
**MAIN PCB DSP Architecture 3/6 (DSP #3 & 4)**



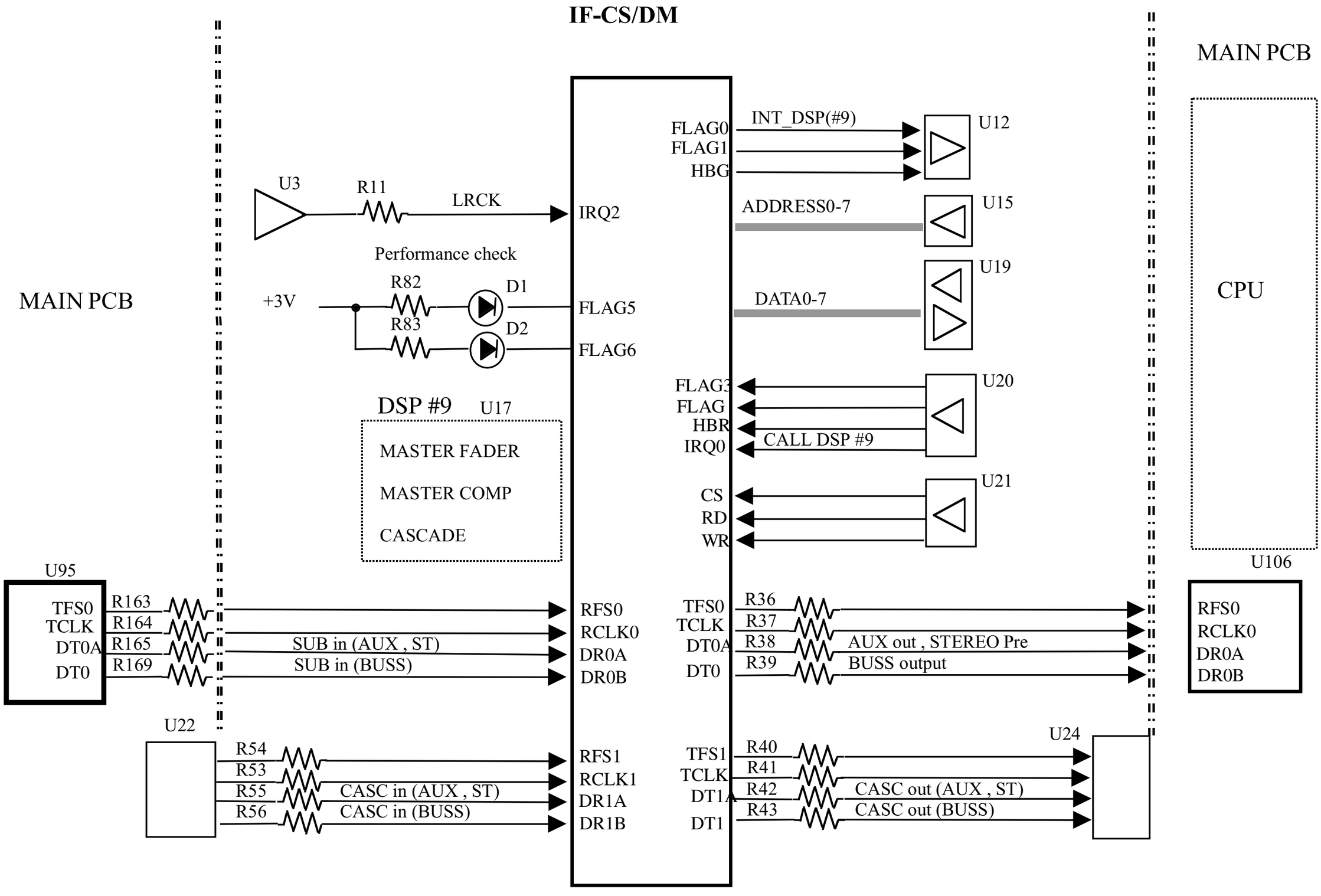
**MAIN PCB DSP Architecture 4/6 (DSP #5 & 6)**



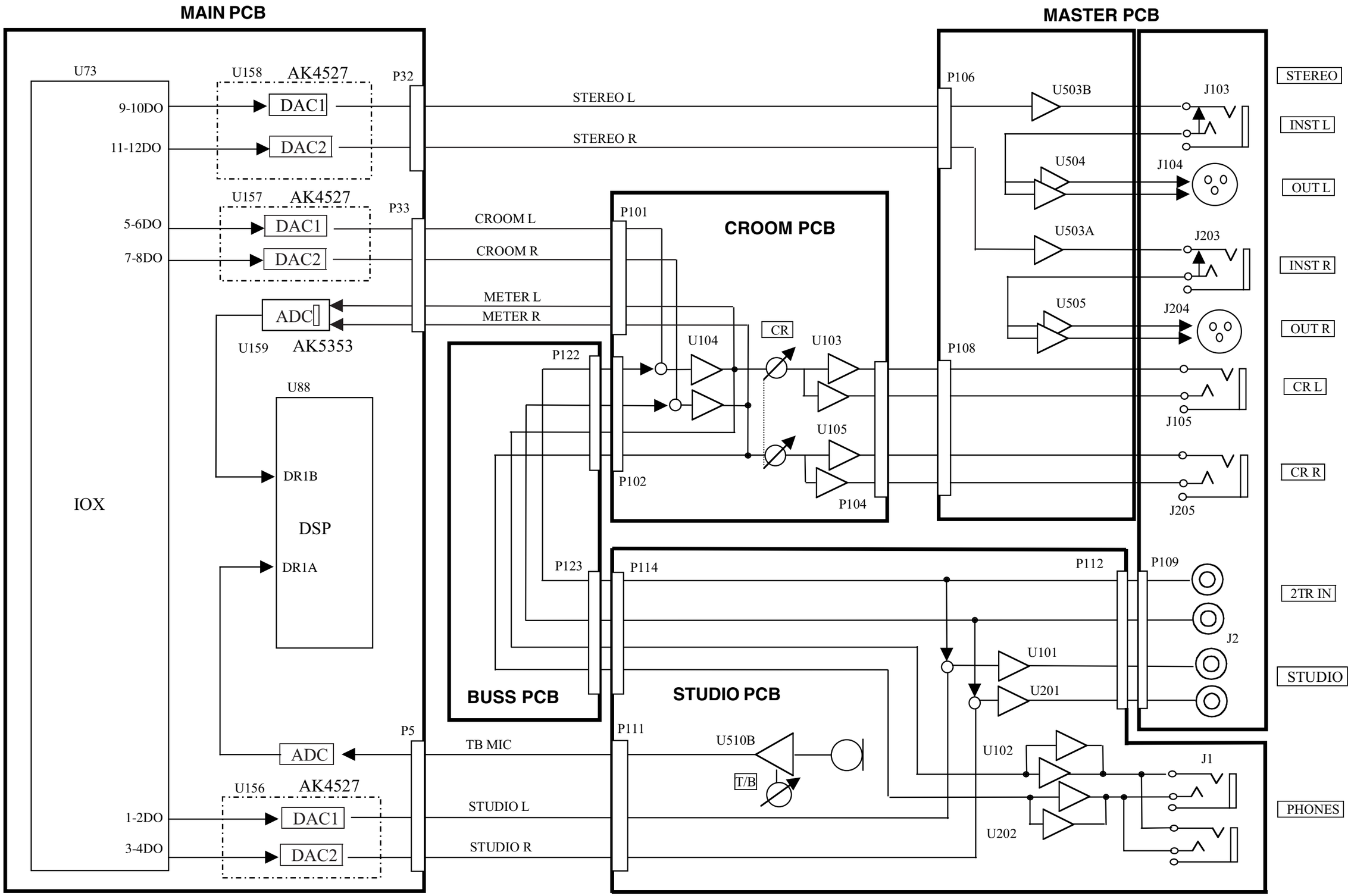
**MAIN PCB DSP Architecture 5/6 (DSP #7)**



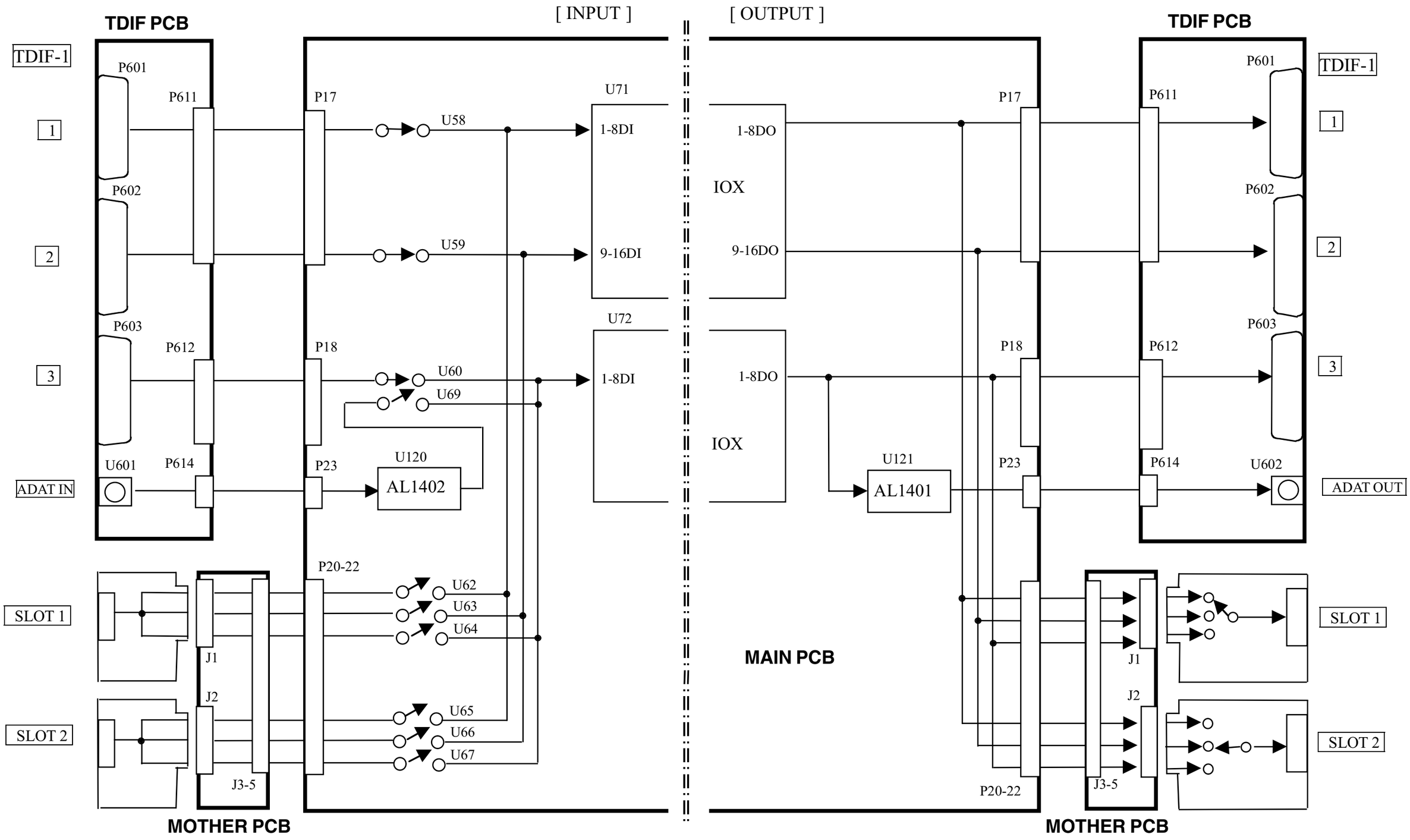
**MAIN PCB DSP Architecture 6/6 (DSP #9 IF-CS/DM)**



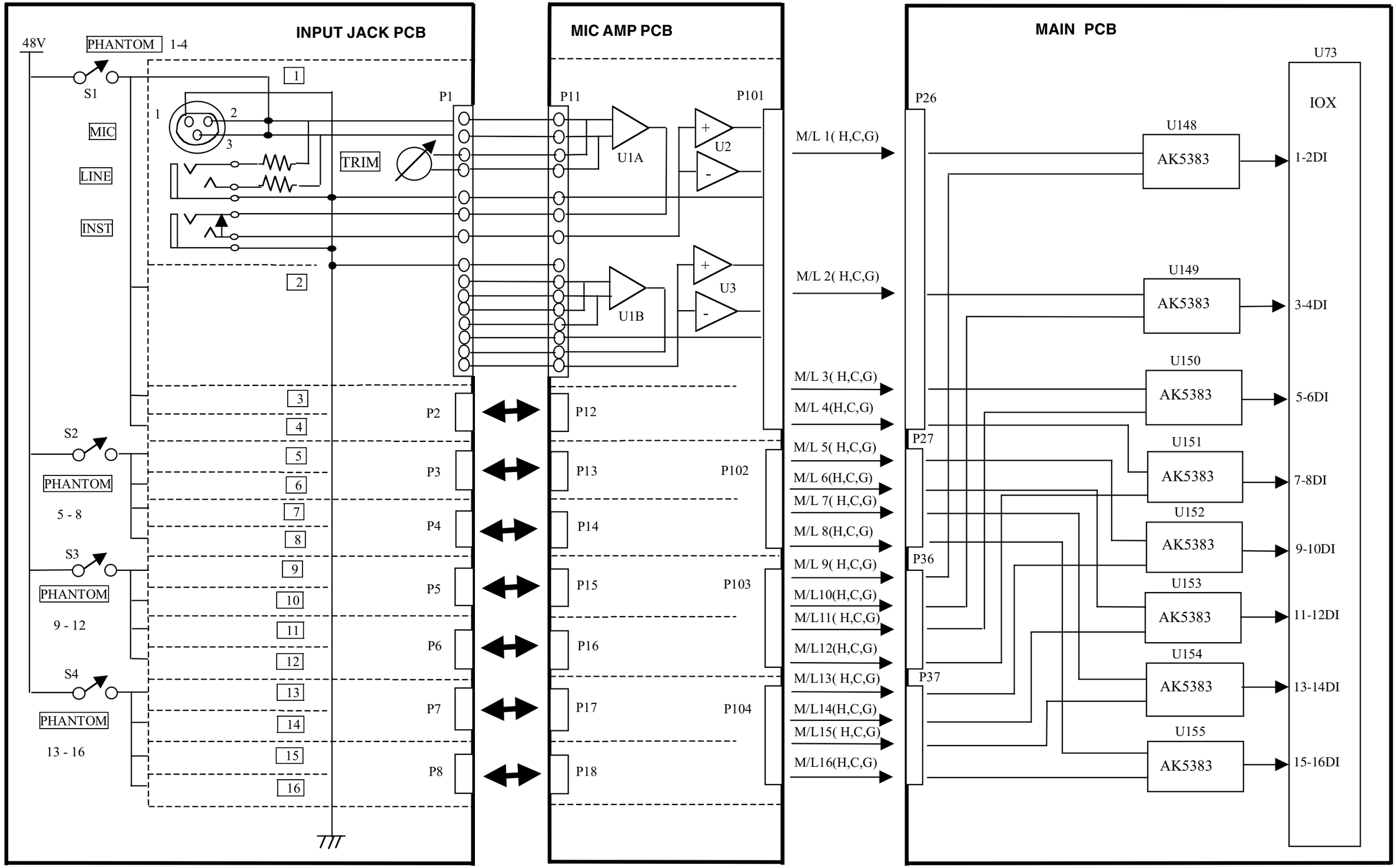
## MASTER SECTION



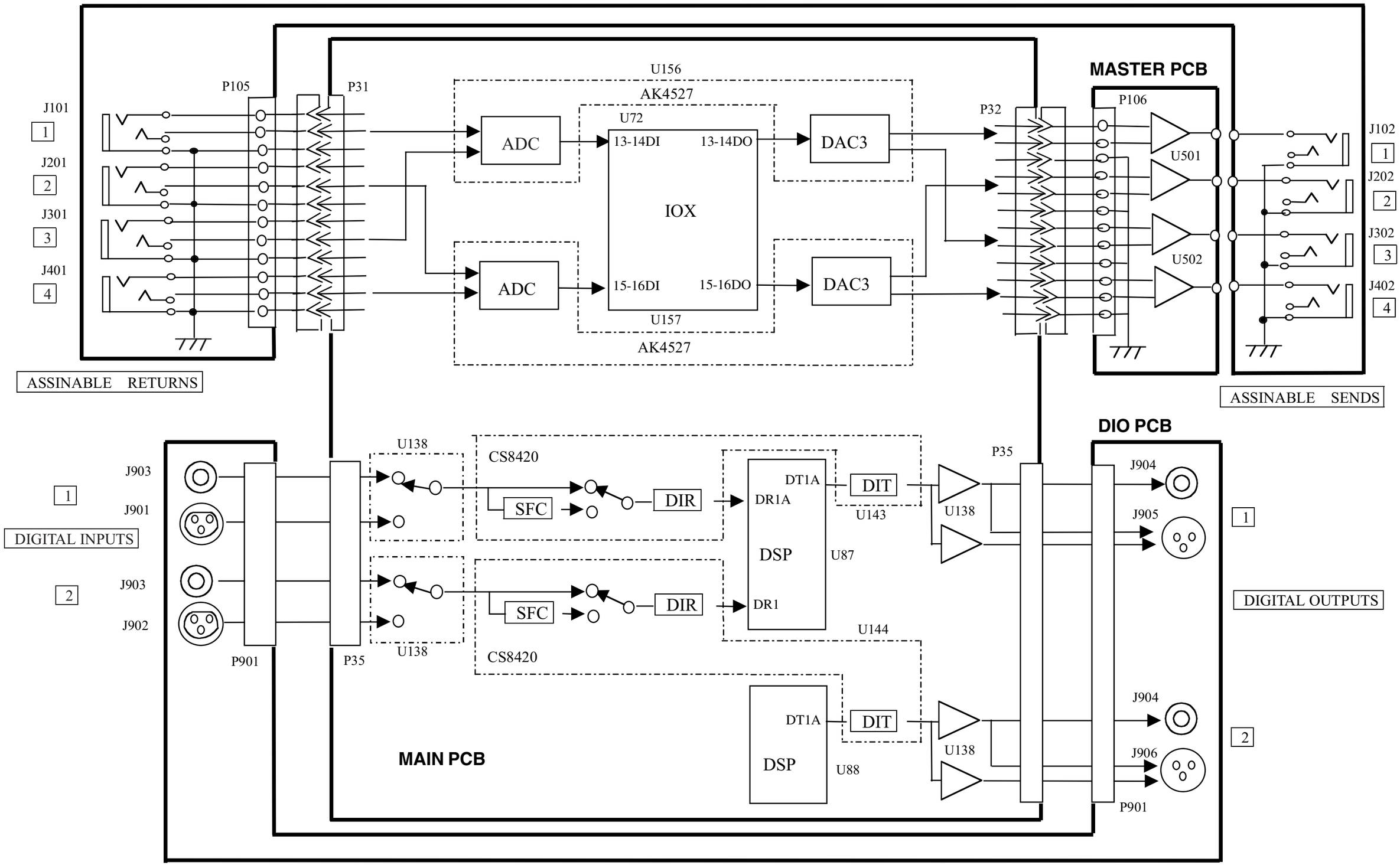
## MTR IN/OUT SECTION (TDIF/ADAT/SLOT)



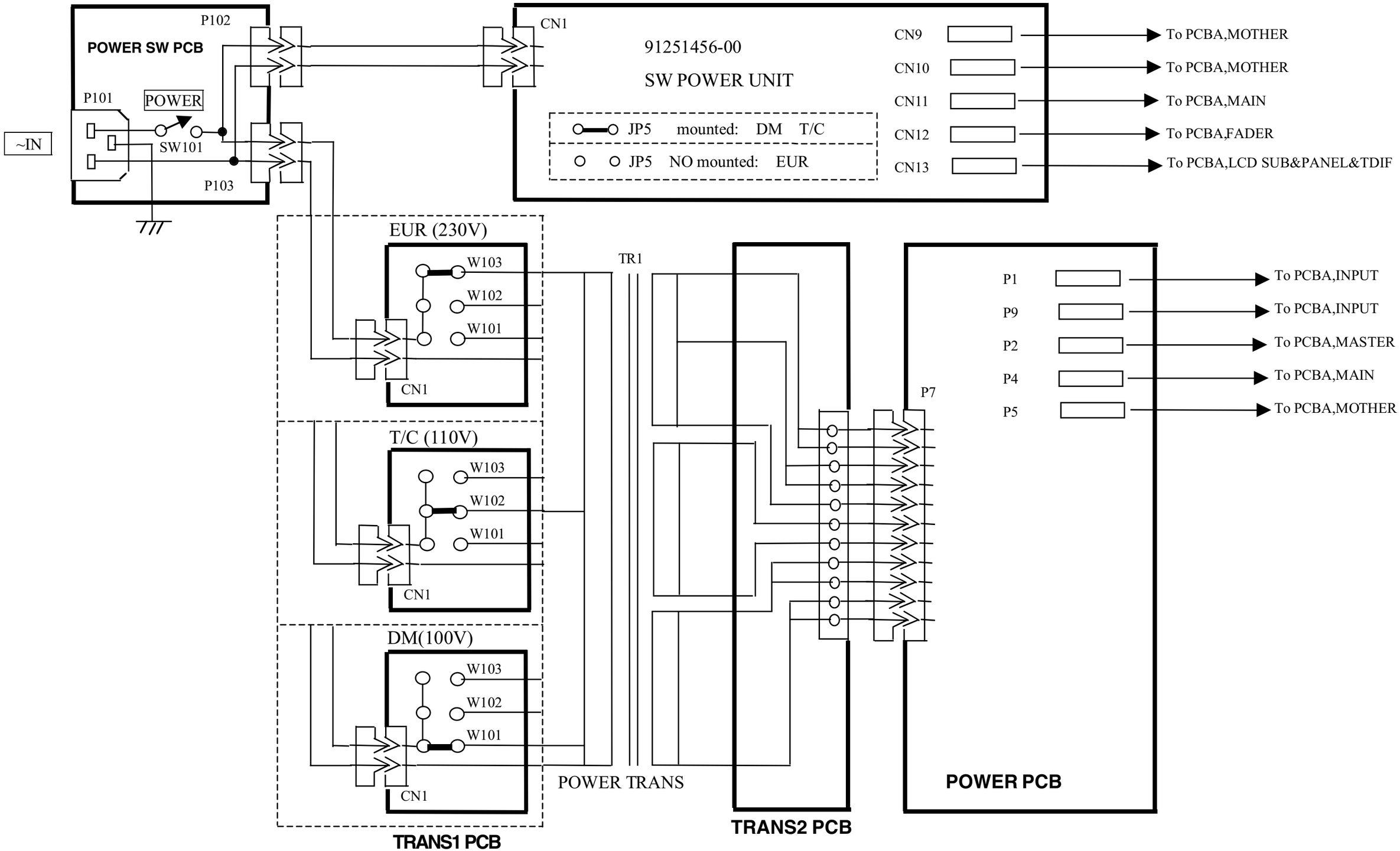
## MIC SECTION


INPUT JACK PCB
MIC AMP PCB
MAIN PCB
48V
PHANTOM
1-4
S1
MIC
LINE
INST
TRIM
P1
P11
P101
U1A
U1B
U2
U3
P2
P12
P3
P13
P102
P4
P14
P5
P15
P103
P6
P16
P7
P17
P104
P8
P18
S2
PHANTOM
5 - 8
S3
PHANTOM
9 - 12
S4
PHANTOM
13 - 16
M/L 1( H,C,G)
M/L 2( H,C,G)
M/L 3( H,C,G)
M/L 4(H,C,G)
M/L 5( H,C,G)
M/L 6(H,C,G)
M/L 7( H,C,G)
M/L 8(H,C,G)
M/L 9( H,C,G)
M/L10(H,C,G)
M/L11( H,C,G)
M/L12(H,C,G)
M/L13( H,C,G)
M/L14(H,C,G)
M/L15( H,C,G)
M/L16(H,C,G)
P26
P27
P36
P37
U73
IOX
U148
AK5383
1-2DI
U149
3-4DI
U150
5-6DI
U151
7-8DI
U152
9-10DI
U153
11-12DI
U154
13-14DI
U155
15-16DI

## ASSIGNABLE SEND/RETURN & DIGITAL IN/OUT SECTION



## POWER SUPPLY SECTION



# PARTS LIST SECTION

**NOTES**

- PC boards shown are viewed from parts side.
- Parts marked with ∗ require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in the manual.
- ⚠Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J]: JAPAN [K]: KOREA [A]: AUSTRALIA [US/C]: U.S.A./CANADA
  [E]: EUROPE [UK]: U.K.

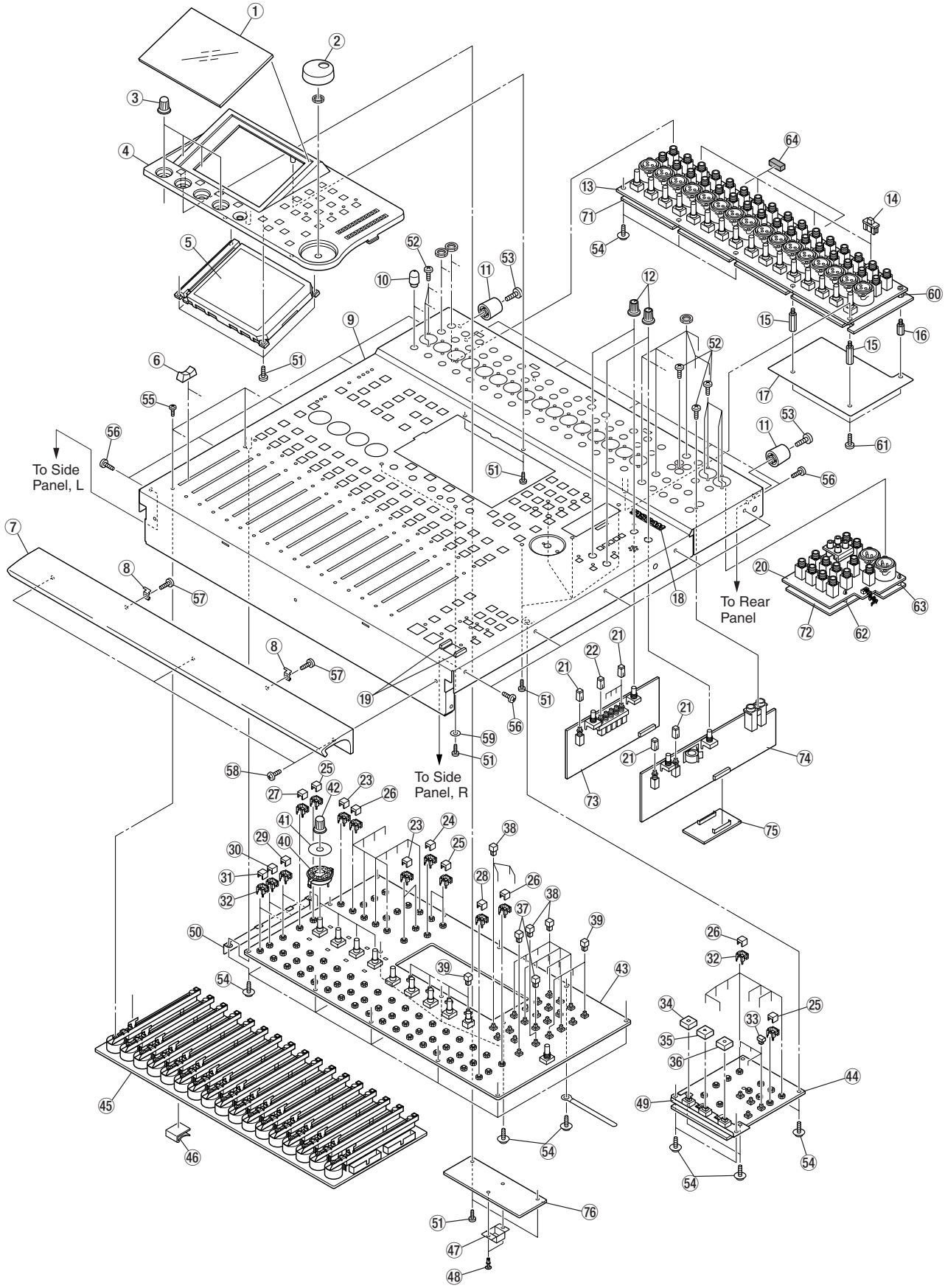
**注 意**

- プリント基板は部品面が示されています。
- ∗印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品及び品番のない部品は供給しません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠は安全重要部品です。
  交換する時は必ずティアック指定の部品を使用してください。
- 仕向先
  [J]: JAPAN [K]: KOREA [A]: AUSTRALIA [US/C]: U.S.A./CANADA
  [E]: EUROPE [UK]: U.K.

# 8. EXPLODED VIEWS AND PARTS LIST

分解図とパーツリスト

**EXPLODED VIEW-1**



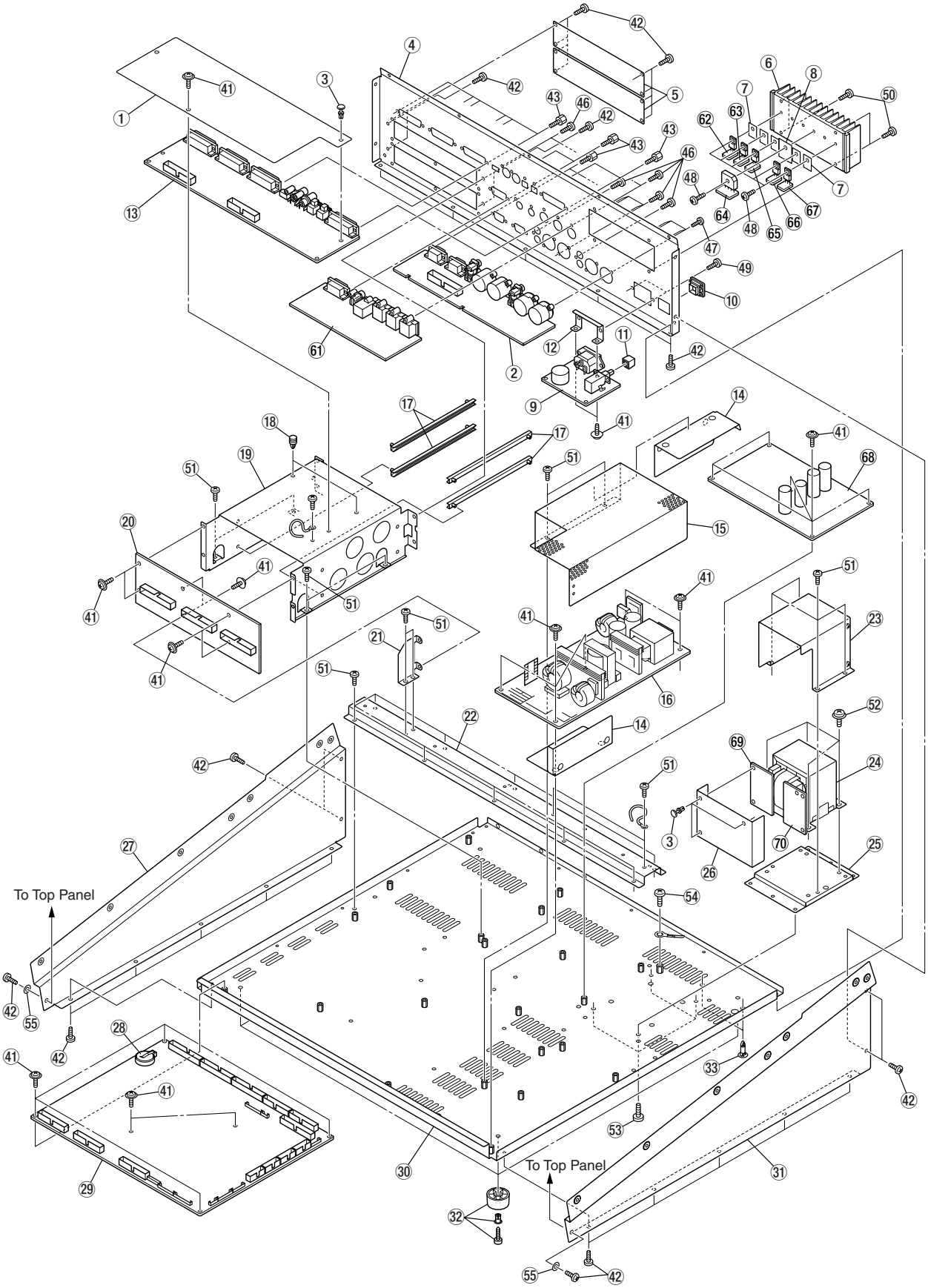
## EXPLODED VIEW-1

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| 1- 1 | 9260363101 | WINDOW,LCD | |
| 1- 2 | 9260385100 | KNOB,JOG N63 | |
| 1- 3 | M00630600C | KNOB,POD N61 | |
| 1- 4 | 9260361701 | ESCUTCHEON,LCD | |
| 1- 5 | 9174027100 | LCD,MG3224C3-SBF | |
| 1- 6 | 9260357800 | KNOB,S-VR NICKEL | |
| 1- 7 | 9260363201 | PAD,582 | |
| 1- 8 | *9260299600 | BRACKET,PAD | |
| 1- 9 | *9260364904 | TOP PANEL ASSY | |
| 1-10 | 9260368000 | KNOB,TRIM N61/N64 | |
| 1-11 | 9260354800 | FOOT,FFT-4 | |
| 1-12 | 5801631800 | KNOB,R-VR N61/N66 | |
| 1-13 | | INPUT JACK PCB ASSY ····· | GATHER PCB ASSY,INPUT (Refer to page 66) |
| 1-14 | M00006100A | KNOB,SLIDE GY | |
| 1-15 | *9783803025 | LOCK SCREW,M3X25X6 | |
| 1-16 | *9783803015 | LOCK SCREW,M3X15X6 | |
| 1-17 | *9260388600 | SHIELD COVER,INPUT | |
| 1-18 | 9260268802 | TASCAM BADGE | |
| 1-19 | M00207800A | ESCUTCHEON,GUARD | |
| 1-20 | | MASTER JACK PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 68) |
| 1-21 | 5801632501 | PUSH BUTTON COVER,WHT/N63 | |
| 1-22 | 9260306400 | PUSH BUTTON COVER,WHT/N61 | |
| 1-23 | 9260362701 | BUTTON,BLT-IN (WHT) | |
| 1-24 | 9260362601 | BUTTON,BLT-IN (R23) | |
| 1-25 | 9260362801 | BUTTON,BLT-IN (N64) | |
| 1-26 | 9260299302 | BUTTON,BLT-IN LED | |
| 1-27 | 9260362901 | BUTTON,BLT-IN (266C) | |
| 1-28 | 9260324702 | BUTTON,BLT-IN LED(SOLO) | |
| 1-29 | 9260351901 | BUTTON,BLT-IN LED(REC) | |
| 1-30 | 9260351701 | BUTTON,BLT-IN LED(SEL) | |
| 1-31 | 9260324502 | BUTTON,BLT-IN LED (MUTE) | |
| 1-32 | 9260299400 | BASE,BLT-IN LED | |
| 1-33 | M00630703A | BUTTON,6.4X8.4 266C | |
| 1-34 | 9260351300 | BUTTON,STOP | |
| 1-35 | 9260351400 | BUTTON,PLAY | |
| 1-36 | 9260351500 | BUTTON,REC | |
| 1-37 | 9260362000 | BUTTON,8X8 WHT | |
| 1-38 | 9260362100 | BUTTON,8X8 N62 | |
| 1-39 | 9260362200 | BUTTON,8X8 N64 | |
| 1-40 | 9260363300 | ESCUTCHEON RING | |
| 1-41 | 9260362301 | PLATE RING | |
| 1-42 | M00630601C | KNOB,POD N63 | |
| 1-43 | | PANEL PCB ASSY ····· | GATHER PCB ASSY,PANEL (Refer to page 68) |
| 1-44 | | TRANSPORT PCB ASSY ····· | GATHER PCB ASSY,TRANSPORT (Refer to page 69) |
| 1-45 | | FADER PCB ASSY ····· | GATHER PCB ASSY,FADER (Refer to page 67) |
| 1-46 | 9260367300 | WIRE CLAMP,FCC-20 | |
| 1-47 | 9260384700 | SHIELD COVER,LCD | |
| 1-48 | 9260385200 | PUSH RIVET,P3045 | |
| 1-49 | *9260363400 | BRACKET,TRANSPORT | |
| 1-50 | *9260388700 | BRACKET,PANEL | |

## EXPLODED VIEW-1

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| 1-51 | *9783602606 | SCREW,BTT-P M2.6X6 | |
| 1-52 | *9783613008 | SCREW,BTT-P M3X8 (BLK) | |
| 1-53 | *9780504010 | SCREW,BH M4X10 (BLK) | |
| 1-54 | *9783103006 | SCREW,CAP-S M3X6 | |
| 1-55 | *9783573004 | SCREW,WHIS BIND M3X4 (BLK) | |
| 1-56 | *9780503006 | SCREW,BH M3X6 (BLK) | |
| 1-57 | *9783213006 | SCREW,BTT-B M3X6 | |
| 1-58 | *9780503008 | SCREW,BH M3X8 (BLK) | |
| 1-59 | Vacant | | |
| 1-60 | *9260389100 | PCB SUPPORT,HP-8 | |
| 1-61 | *9780403006 | SCREW,BH M3X6 | |
| 1-62 | *9260356300 | SPACER SUPPORT,LCC-8 | |
| 1-63 | *9260355700 | SPACER SUPPORT,MC-8 | |
| 1-64 | *9260366700 | CUSHION,10X20X9 | |
| 1-71 | | MIC AMP PCB ····· | GATHER PCB ASSY,INPUT (Refer to page 66) |
| 1-72 | | MASTER AMP PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 68) |
| 1-73 | | C.ROOM PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 68) |
| 1-74 | | STUDIO PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 68) |
| 1-75 | | BUSS PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 68) |
| 1-76 | | LCD SUB PCB ASSY ····· | GATHER PCB ASSY,TRANSPORT (Refer to page 69) |

## EXPLODED VIEW-2



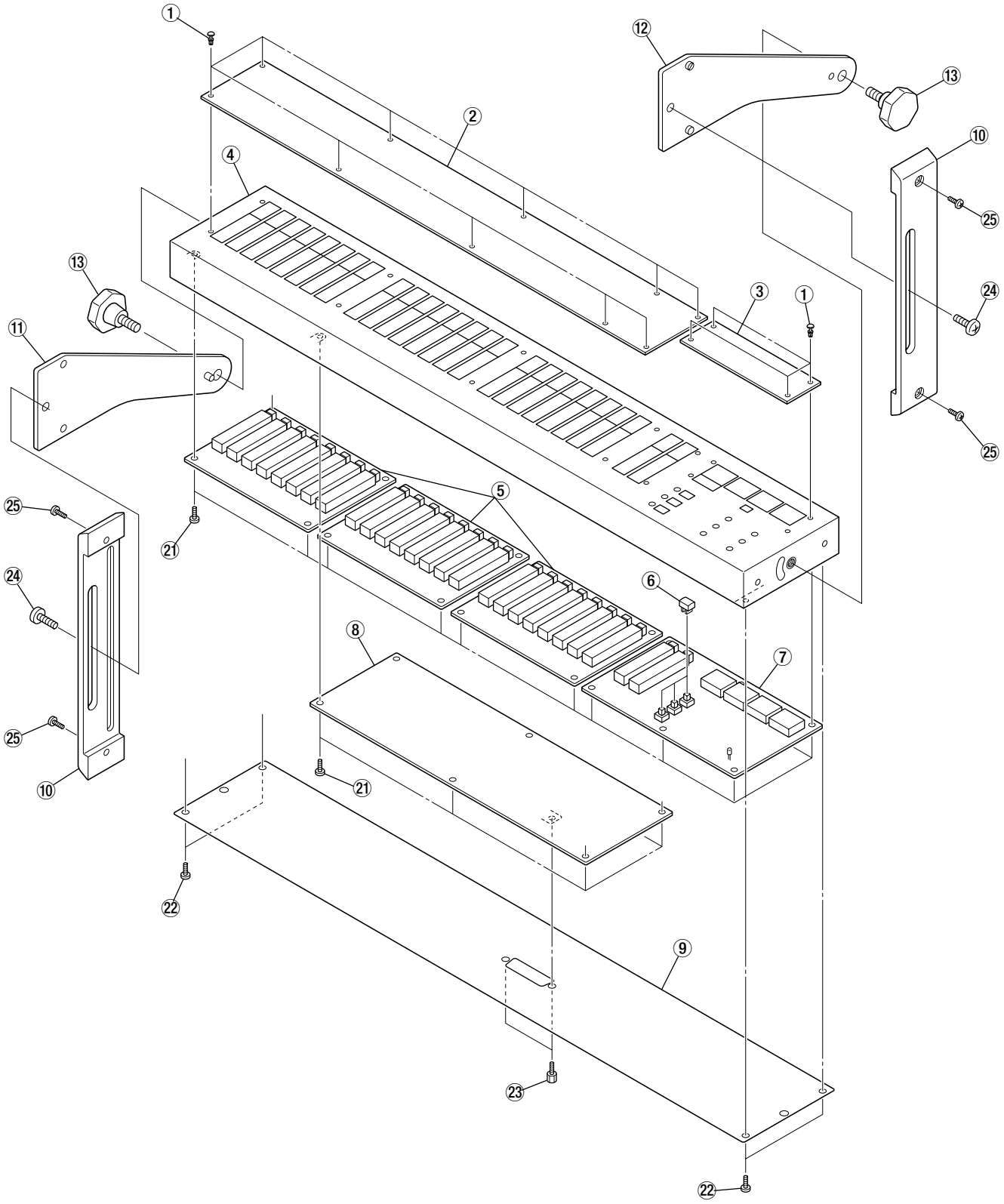
## EXPLODED VIEW-2

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| 2- 1 | *9260384901 | SHIELD SHEET,TDIF | |
| 2- 2 | | DIGITAL I/O PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 68) |
| 2- 3 | 9260361500 | PUSH RIVET,SR3-5.5 | |
| 2- 4 | *9260364401 | REAR PANEL | |
| 2- 5 | *9260359300 | PANEL,SLOT | |
| 2- 6 | *9260364502 | HEAT SINK | |
| 2- 7 | 9260317800 | SI-INSULATOR,T-220 | |
| 2- 8 | *9260232900 | SHEET,RADIATOR D | |
| 2- 9 | | POWER SW PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |
| 2-10 | 5801486601 | ESCUTCHEON D,P-N15-A | |
| 2-11 | 5801503800 | BUTTON,EJECT P-N15-A | |
| 2-12 | 9260320701 | BRACKET,PWRSW | |
| 2-13 | | TDIF PCB ASSY ····· | GATHER PCB ASSY,TRANSPORT (Refer to page 69) |
| 2-14 | *9260383300 | SHEET,SW REG | |
| 2-15 | 9260364801 | COVER,SW REG | |
| 2-16 | 9125146300 | SW-PWR,UPS220-1061-L [J,US/C] | |
| | 9125146400 | SW-PWR,UPS220-1061-H [K,A,E,UK] | |
| 2-17 | 9260356700 | CARD GUIDE,CG-600 | |
| 2-18 | *9260364000 | PCB SUPPORT,DCB-5 | |
| 2-19 | *9260363901 | BRACKET,SLOT | |
| 2-20 | | MOTHER PCB ASSY ····· | GATHER PCB ASSY,MOTHER (Refer to page 70) |
| 2-21 | *9260364301 | BRACKET,MOTHER PCB | |
| 2-22 | 9260363701 | FRAME,BOTTOM | |
| 2-23 | *9260384800 | SHIELD COVER,TRANS | |
| 2-24 | ⚠ 9125145202 | POWER TRANSFORMER | |
| 2-25 | *9260364101 | BRACKET,TRANS | |
| 2-26 | *9260364201 | COVER,TRANS PCB | |
| 2-27 | 9260364601 | SIDE PANEL,L | |
| 2-28 | 9151003000 | BATTERY,CR2032 | |
| 2-29 | | MAIN PCB ASSY ····· | GATHER PCB ASSY,MAIN (Refer to page 65) |
| 2-30 | *9260363601 | CHASSIS,BOTTOM | |
| 2-31 | 9260364701 | SIDE PANEL,R | |
| 2-32 | 9260233100 | FOOT,FF015 | |
| 2-33 | *9260366800 | PCB SUPPORT,RCC-12 | |
| 2-41 | *9783103006 | SCREW,CAP-S M3X6 | |
| 2-42 | 9780503006 | SCREW,BH M3X6 (BLK) | |
| 2-43 | *9260330700 | D-SUB SCREW,HW-H118MN02 | |
| 2-44 | Vacant | | |
| 2-45 | Vacant | | |
| 2-46 | *9783613008 | SCREW,BTT-P M3X8 (BLK) | |
| 2-47 | *9783242608 | SCREW,BTT-B M2.6X8 (BLK) | |
| 2-48 | *9783243012 | SCREW,BTT-B M3X12 (BLK) | |
| 2-49 | *9783243008 | SCREW,BTT-B M3X8 (BLK) | |
| 2-50 | *9780503010 | SCREW,BH M3X10 (BLK) | |
| 2-51 | *9780403006 | SCREW,BH M3X6 | |
| 2-52 | *9783294008 | SCREW,BTT-SSB M4X8 | |
| 2-53 | *9780404008 | SCREW,BH M4X8 | |
| 2-54 | *9780504008 | SCREW,BH M4X8 (BLK) | |

## EXPLODED VIEW-2

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| 2-61 | | MIDI PCB ASSY ····· | GATHER PCB ASSY,TRANSPORT (Refer to page 69) |
| 2-62 | | TR4 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |
| 2-63 | | TR3 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |
| 2-64 | | BD PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |
| 2-65 | | TR2 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |
| 2-66 | | TR1 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |
| 2-67 | | TR5 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |
| 2-68 | | POWER PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |
| 2-69 | | TRANS 2 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |
| 2-70 | | TRANS 1 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 70) |

**EXPLODED VIEW-3 (MU-24)**



## EXPLODED VIEW-3 (MU-24)

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| 3- 1 | 9260388300 | PUSH RIVETS,SR2.6-4.2 | |
| 3- 2 | 9260368800 | WINDOW,L | |
| 3- 3 | 9260368700 | WINDOW,S | |
| 3- 4 | 9260368100 | PANEL ASSY,METER | |
| 3- 5 | | PCB ASSY,INPUT METER ····· | GATHER PCB ASSY,METER BRIDGE (Refer to page 71) |
| 3- 6 | M00630701A | BUTTON,6.4X8.4 N63 | |
| 3- 7 | | PCB ASSY,MASTER METER ····· | GATHER PCB ASSY,METER BRIDGE (Refer to page 71) |
| 3- 8 | | PCB ASSY,METER DRIVER ····· | GATHER PCB ASSY,METER DRIVER (Refer to page 71) |
| 3- 9 | *9260368900 | REAR PANEL,METER | |
| 3-10 | *9260369000 | BASE,METER | |
| 3-11 | *9260369100 | ANGLE,SIDE L | |
| 3-12 | *9260369200 | ANGLE,SIDE R | |
| 3-13 | 9260388401 | HAND SCREW,40-M8-L=16(NI) | |
| 3-21 | *9780403006 | SCREW,BH M3X6 | |
| 3-22 | *9780503006 | SCREW,BH M3X6(BLK) | |
| 3-23 | 9260330800 | D-SUB SCREW,HW-H118EN00 | |
| 3-24 | *9780208010 | SCREW,PH M8X10 (BLK) | |
| 3-25 | *9780503012 | SCREW,BH M3X12 (BLK) | |

## INCLUDED ACCESSORIES (MU-24)

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| | 9101440700 | OWNER'S MANUAL,MU-24 | |
| | 9109032010 | MU-24 METER CABLE | |

# 9. PC BOARDS AND PARTS LIST

基板図とパーツリスト

## GATHER PCB ASSY, MAIN

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145316000 | GATHER PCB ASSY,MAIN |
| | | MAIN PCB |
| BT1 | 9260303900 | BATTERY HOLDER,SN-2032-1 |
| BT1 | 9151003000 | BATTERY,CR2032 |
| D1,2 | 9165025030 | DIODE,BR751V-40/TE17 |
| D4-7 | 9165023530 | DIODE,1SS355 TE17 |
| D8 | 9165028930 | DIODE,HVC376B |
| D9-12 | 9165023530 | DIODE,1SS355 TE17 |
| D13-16 | 9174027431 | LED,KPK-3020NC(ORG)12MAV |
| L1 | 5286051500 | COIL,CHIP 2.7UH LK2125 |
| L2-5 | 9173020830 | COIL,MLF2012E100MT |
| P1 | 9144521900 | CONNECTOR,14FE-BT-VK-N |
| P2 | 9143180000 | CONNECTOR PLUG,12P |
| P3 | 9144513000 | HEADER,2556P03UA00 |
| P4 | 9143242000 | PLUG,14P B14B-PH-K |
| P5 | 9143242000 | PLUG,14P B14B-PH-K |
| P6 | 9143241000 | PLUG,13P(B13B-PH-K) |
| P7 | 9144521000 | CONNECTOR,3675P 34VUA0 |
| P8 | 9143232000 | PLUG,B4B-PH 4P |
| P9,10 | 9144521000 | CONNECTOR,3675P 34VUA0 |
| P11 | 9143174000 | PLUG,6P B6B-EH-A |
| P17,18 | 9144521000 | CONNECTOR,3675P 34VUA0 |
| P20-22 | 9144510000 | CONNECTOR,3675P 40VUA0 |
| P23 | 9143232000 | PLUG,B4B-PH 4P |
| P26,27 | 9144523700 | CONNECTOR,3675P 16VUA0 |
| P29,30 | 9143174000 | PLUG,6P B6B-EH-A |
| P31 | 9143240000 | CONNECTOR PLUG,B12B-PH-K |
| P32 | 9143240020 | CONNECTOR,B12B-PH-K-R |
| P33 | 9143234000 | PLUG,B6B-PH 6P |
| P34 | 9143174000 | PLUG,6P B6B-EH-A |
| P35 | 9144510000 | CONNECTOR,3675P 40VUA0 |
| P36,37 | 9144523700 | CONNECTOR,3675P 16VUA0 |
| Q1 | 9163018030 | TR,2SA1586Y |
| Q2,4 | 9163018530 | DTR,DTA124EU |
| Q3,5 | 9163018630 | DTR,DTC124EU |
| RA1-4 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA5,9 | 9111287030 | R,ARRAY FCA340 103J |
| RA6-8 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA10-13 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA14,17 | 9111287030 | R,ARRAY FCA340 103J |
| RA15,16 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA18,22 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA23,29 | 9111287030 | R,ARRAY FCA340 103J |
| RA24-28 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA30,31 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA32,63 | 9111287030 | R,ARRAY FCA340 103J |
| RA33,34 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA35-37 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |
| RA38,39 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA40,41 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |
| RA42,43 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA44,45 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |
| RA46-49 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |

## GATHER PCB ASSY, MAIN

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| RA50-53 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |
| RA60,61 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |
| RA62 | 9111287030 | R,ARRAY FCA340 103J |
| U1 | S0044474 | IC,HD74LV273AFPEL |
| U2 | 5220049400 | IC,UPD65013 |
| U3 | 9167039930 | IC,M62006FP |
| U4 | S0044614 | IC,HD29051FP |
| U5 | S0044584 | IC,HD74LV04AFPEL |
| U6 | 9167080803 | ROM ASSY,PANEL MBM29F800BA-70PF |
| U7 | 9167080903 | ROM ASSY,PANEL MBM29F800BA-70PF |
| U6,7 | E0033093 | SOCKET,44PIN SOP IC179 |
| U8 | 9167073230 | IC,BS62LV256TC-70 |
| U9 | 9167041730 | IC,TC74VHC00F (14P) |
| U10 | 9167074630 | IC,T2316162A-60S |
| U11 | S0044444 | IC,CPU HD6417014R |
| U12 | S0044574 | IC,HD74LV00AFPEL |
| U13,14 | 9167074730 | IC,T14L256A-15P |
| U15,16 | S0044554 | IC,HD74LV244AFPEL |
| U17,18 | S0044484 | IC,HD74LV541AFPEL |
| U19-21 | S0044524 | IC,HD74LV139AFPEL |
| U22,25 | S0044534 | IC,HD74LV138AFPEL |
| U23,24 | S0044474 | IC,HD74LV273AFPEL |
| U26 | S0044524 | IC,HD74LV139AFPEL |
| U27 | S0044564 | IC,HD74LV125AFPEL |
| U28 | S0039254 | IC,IDT7130SA55J |
| U29 | S0044554 | IC,HD74LV244AFPEL |
| U30 | S0044484 | IC,HD74LV541AFPEL |
| U31 | 9167080703 | ROM ASSY,MBM29F800BA-70PF |
| U31 | E0033093 | SOCKET,44PIN SOP IC179 |
| U32 | 9167074630 | IC,T2316162A-60S |
| U33 | S0044444 | IC,CPU HD6417014R |
| U34 | S0044474 | IC,HD74LV273AFPEL |
| U35 | S0044524 | IC,HD74LV139AFPEL |
| U36 | 9167066330 | IC,HD74LV32AFPEL |
| U37 | S0044554 | IC,HD74LV244AFPEL |
| U38,39 | 9167066330 | IC,HD74LV32AFPEL |
| U40 | S0004183 | IC,HD64646FS |
| U41-44 | S0044604 | IC,HD74LV157AFPEL(16P) |
| U45 | S0044554 | IC,HD74LV244AFPEL |
| U46 | 9167073230 | IC,BS62LV256TC-70 |
| U47 | 9167048730 | IC,HD74LV02FPEL |
| U48-53 | S0044484 | IC,HD74LV541AFPEL |
| U54 | S0044554 | IC,HD74LV244AFPEL |
| U55-57 | 9167065130 | IC,HD74LV240AFPEL |
| U58-61 | 5220121000 | IC,HD74HC540FPEL(20P) |
| U62-67 | S0044484 | IC,HD74LV541AFPEL |
| U68 | S0044524 | IC,HD74LV139AFPEL |
| U69 | S0044484 | IC,HD74LV541AFPEL |
| U70 | S0044474 | IC,HD74LV273AFPEL |
| U71-73 | S00190600A | IC,IOX |
| U74-76 | S0044554 | IC,HD74LV244AFPEL |
| U77,78 | S0038953 | IC,ADSP-21065L |
| U79 | 9167041630 | IC,TC74VHCU04F (14P) |

## GATHER PCB ASSY, MAIN

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| U80 | S0044504 | IC,HD74LVC541AFPEL |
| U81 | S0044574 | IC,HD74LV00AFPEL |
| U82,83 | S0044484 | IC,HD74LV541AFPEL |
| U84,85 | S0044554 | IC,HD74LV244AFPEL |
| U86 | S0044604 | IC,HD74LV157AFPEL(16P) |
| U87,88 | S0038953 | IC,ADSP-21065L |
| U89,98 | S0044574 | IC,HD74LV00AFPEL |
| U90,91 | S0044484 | IC,HD74LV541AFPEL |
| U92,93 | S0044554 | IC,HD74LV244AFPEL |
| U94,95 | S0038953 | IC,ADSP-21065L |
| U96,97 | 9167074030 | IC,T431616A-8S |
| U99,100 | S0044484 | IC,HD74LV541AFPEL |
| U101,102 | S0044554 | IC,HD74LV244AFPEL |
| U103 | S0044564 | IC,HD74LV125AFPEL |
| U104 | S0044604 | IC,HD74LV157AFPEL(16P) |
| U105 | 9167079730 | IC,XC9572XL-10 TQ100 |
| U106 | S0038953 | IC,ADSP-21065L |
| U107 | S0044454 | IC,HD74ALVCH16543 |
| U108 | S0044514 | IC,HD74LV574AFPEL |
| U109-112 | 9167068630 | IC,T14L102N-12J(32P) |
| U120 | 9167066730 | IC,AL1402 |
| U121 | 9167066630 | IC,AL1401A |
| U122-124 | S0044474 | IC,HD74LV273AFPEL |
| U125 | 9167079630 | IC,XC9536XL 100UQ 64-C |
| U126,127 | S0044484 | IC,HD74LV541AFPEL |
| U128 | S0044494 | IC,HD74LV540AFPEL |
| U129 | S0044484 | IC,HD74LV541AFPEL |
| U130,131 | S0044604 | IC,HD74LV157AFPEL(16P) |
| U132 | 9167081230 | IC,HD74LV14AFPEL |
| U133 | 9167041630 | IC,TC74VHCU04F (14P) |
| U134 | 13447922 | IC,NJM78L05UA-TE1(3P) |
| U135 | 9167068030 | IC,MC74HC4046ADR2(16P) |
| U136 | 9167070630 | IC,TC74VHCT00AF |
| U137 | S0044474 | IC,HD74LV273AFPEL |
| U138 | S0044614 | IC,HD29051FP |
| U139 | 9167041630 | IC,TC74VHCU04F (14P) |
| U140 | 9167048730 | IC,HD74LV02FPEL |
| U141 | S0044594 | IC,HD74LV74AFPEL |
| U142 | S0044554 | IC,HD74LV244AFPEL |
| U143,144 | S0042533 | IC,CS8420 |
| U145 | S0044554 | IC,HD74LV244AFPEL |
| U146 | S0044554 | IC,HD74LV244AFPEL |
| U147 | S0044594 | IC,HD74LV74AFPEL |
| U148-155 | S0035224 | IC,AK5383VS-E2 |
| U156-158 | S0044624 | IC,AK4527VQ |
| U159 | S0044634 | IC,AK5353VT-E2 |
| U160 | 9167079630 | IC,XC9536XL 100UQ 64-C |
| U161-163 | 13443492 | IC,HD74HC4052FPEL |
| U164 | S0044434 | IC,NJM79L24UA-TE1 |
| U165 | S0044584 | IC,HD74LV04AFPEL |
| U166 | 9167041530 | IC,TC74VHC153F (16P) |
| X1 | 9173016430 | OSC,MIN95A-T 7.056MHZ |
| X2 | 9173019730 | XTAL,LIM-C 30MHZ |

## GATHER PCB ASSY, INPUT

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145313000 | GATHER PCB ASSY,INPUT |
| | | PCB,INPUT JACK |
| | | PCB,MIC AMP |
| D13,14 | 9165022150 | DIODE,TP 1SS133T |
| D23,24 | 9165022150 | DIODE,TP 1SS133T |
| D33,34 | 9165022150 | DIODE,TP 1SS133T |
| D43,44 | 9165022150 | DIODE,TP 1SS133T |
| D53,54 | 9165022150 | DIODE,TP 1SS133T |
| D63,64 | 9165022150 | DIODE,TP 1SS133T |
| D73,74 | 9165022150 | DIODE,TP 1SS133T |
| D83,84 | 9165022150 | DIODE,TP 1SS133T |
| D93,94 | 9165022150 | DIODE,TP 1SS133T |
| D103,104 | 9165022150 | DIODE,TP 1SS133T |
| D113,114 | 9165022150 | DIODE,TP 1SS133T |
| D123,124 | 9165022150 | DIODE,TP 1SS133T |
| D133,134 | 9165022150 | DIODE,TP 1SS133T |
| D143,144 | 9165022150 | DIODE,TP 1SS133T |
| D153,154 | 9165022150 | DIODE,TP 1SS133T |
| D163,164 | 9165022150 | DIODE,TP 1SS133T |
| J1-15 | 9144277001 | MIC JACK,NC3FAV-0 |
| J16 | 9144526900 | MIC JACK,NC3FAV1-0-Y |
| J101-116 | 9144271001 | PHONE JACK,JY-6353-02-030 |
| J201-216 | 9144272001 | PHONE JACK,JY-6353-02-040 |
| P1-8 | 9144523800 | CABLE BOTTON,51048-1510 |
| P11-18 | 9144523800 | CABLE BOTTON,51048-1510 |
| P101-104 | 9144523700 | CONNECTOR,3675P 16VUA0 |
| P901,903 | 9143181000 | PLUG,13P B13B-EH-A |
| P905 | 9143170000 | CONNECTOR PLUG,2P |
| P906,907 | 9107148600 | 2P POWER WIRES |
| Q11,12 | 9163021320 | TR,2SA1048GR |
| Q13,14 | S0039452 | TR,2SA1084E |
| Q15,16 | S0028932 | TR,2SC5395-T12-F |
| Q21,22 | 9163021320 | TR,2SA1048GR |
| Q23,24 | S0039452 | TR,2SA1084E |
| Q25,26 | S0028932 | TR,2SC5395-T12-F |
| Q31,32 | 9163021320 | TR,2SA1048GR |
| Q33,34 | S0039452 | TR,2SA1084E |
| Q35,36 | S0028932 | TR,2SC5395-T12-F |
| Q41,42 | 9163021320 | TR,2SA1048GR |
| Q43,44 | S0039452 | TR,2SA1084E |
| Q45,46 | S0028932 | TR,2SC5395-T12-F |
| Q51,52 | 9163021320 | TR,2SA1048GR |
| Q53,54 | S0039452 | TR,2SA1084E |
| Q55,56 | S0028932 | TR,2SC5395-T12-F |
| Q61,62 | 9163021320 | TR,2SA1048GR |
| Q63,64 | S0039452 | TR,2SA1084E |
| Q65,66 | S0028932 | TR,2SC5395-T12-F |
| Q71,72 | 9163021320 | TR,2SA1048GR |
| Q73,74 | S0039452 | TR,2SA1084E |
| Q75,76 | S0028932 | TR,2SC5395-T12-F |
| Q81,82 | 9163021320 | TR,2SA1048GR |
| Q83,84 | S0039452 | TR,2SA1084E |
| Q85,86 | S0028932 | TR,2SC5395-T12-F |

## GATHER PCB ASSY, INPUT

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| Q91,92 | | 9163021320 | TR,2SA1048GR |
| Q93,94 | | S0039452 | TR,2SA1084E |
| Q95,96 | | S0028932 | TR,2SC5395-T12-F |
| Q101,102 | | 9163021320 | TR,2SA1048GR |
| Q103,104 | | S0039452 | TR,2SA1084E |
| Q105,106 | | S0028932 | TR,2SC5395-T12-F |
| Q111,112 | | 9163021320 | TR,2SA1048GR |
| Q113,114 | | S0039452 | TR,2SA1084E |
| Q115,116 | | S0028932 | TR,2SC5395-T12-F |
| Q121,122 | | 9163021320 | TR,2SA1048GR |
| Q123,124 | | S0039452 | TR,2SA1084E |
| Q125,126 | | S0028932 | TR,2SC5395-T12-F |
| Q131,132 | | 9163021320 | TR,2SA1048GR |
| Q133,134 | | S0039452 | TR,2SA1084E |
| Q135,136 | | S0028932 | TR,2SC5395-T12-F |
| Q141,142 | | 9163021320 | TR,2SA1048GR |
| Q143,144 | | S0039452 | TR,2SA1084E |
| Q145,146 | | S0028932 | TR,2SC5395-T12-F |
| Q151,152 | | 9163021320 | TR,2SA1048GR |
| Q153,154 | | S0039452 | TR,2SA1084E |
| Q155,156 | | S0028932 | TR,2SC5395-T12-F |
| Q161,162 | | 9163021320 | TR,2SA1048GR |
| Q163,164 | | S0039452 | TR,2SA1084E |
| Q165,166 | | S0028932 | TR,2SC5395-T12-F |
| R21,71 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R121,171 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R221,271 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R321,371 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R421,471 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R521,571 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R621,671 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R721,771 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| S1-4 | | 9135036300 | SLIDE SW,SSSU042NA2-TK |
| U1-32 | | 9167025200 | IC,BA15532N |
| VR1-16 | | 9172038900 | VR,20KZD EVUF2LFL3 24D |

## GATHER PCB ASSY, FADER

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145314000 | GATHER PCBA,FADER |
| | | PCB,FADER |
| D101-103 | 9165023530 | DIODE,1SS355 TE17 |
| D151-153 | 9165023530 | DIODE,1SS355 TE17 |
| D201-203 | 9165023530 | DIODE,1SS355 TE17 |
| D251-253 | 9165023530 | DIODE,1SS355 TE17 |
| D301-303 | 9165023530 | DIODE,1SS355 TE17 |
| D351-353 | 9165023530 | DIODE,1SS355 TE17 |
| D401-403 | 9165023530 | DIODE,1SS355 TE17 |
| D451-453 | 9165023530 | DIODE,1SS355 TE17 |
| D501-503 | 9165023530 | DIODE,1SS355 TE17 |
| D551-553 | 9165023530 | DIODE,1SS355 TE17 |

## GATHER PCB ASSY, FADER

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| D601-603 | 9165023530 | DIODE,1SS355 TE17 |
| D651-653 | 9165023530 | DIODE,1SS355 TE17 |
| D701-703 | 9165023530 | DIODE,1SS355 TE17 |
| D751-753 | 9165023530 | DIODE,1SS355 TE17 |
| D801-803 | 9165023530 | DIODE,1SS355 TE17 |
| D851-853 | 9165023530 | DIODE,1SS355 TE17 |
| D901-903 | 9165023530 | DIODE,1SS355 TE17 |
| L1,2 | 9173020730 | COIL,BLM41P750SPT |
| MF101-901 | R00979400A | VAR RES,5KB T-SENSE |
| MF151-851 | R00979400A | VAR RES,5KB T-SENSE |
| P1 | 9144521000 | CONNECTOR,3675P 34VUA0 |
| P2 | 9144521000 | CONNECTOR,3675P 34VUA0 |
| P3 | 9143179000 | CONNECTOR PLUG,B11B-EH-A |
| R3 | 9111297030 | R,ARRAY 10KX8 YC-15J |
| R4 | 9111300030 | RA,GUS-QS009-01-1002-G |
| U1 | 13447922 | IC,NJM78L05UA-TE1(3P) |
| U2 | S0028474 | IC,NJM79L05UA-TE1 |
| U3 | 13447982 | IC,NJM78L06UA-TE1 |
| U4 | 9167045830 | IC,HD74HC541FPV |
| U5,6 | 13444452 | IC,HD74HC138FP-TR |
| U7,8 | S0044474 | IC,HD74LV273AFPEL |
| U9 | S0044514 | IC,HD74LV574AFPEL |
| U10 | S0044474 | IC,HD74LV273AFPEL |
| U11,12 | S0044474 | IC,HD74LV273AFPEL |
| U13-15 | 9167045830 | IC,HD74HC541FPV |
| U16-18 | S0034834 | IC,TC74HC4051AF |
| U101,201 | S0023994 | IC NJM4565M(8P)-TE1 |
| U102,402 | 13444414 | IC,HD74HC14FP-TR |
| U103,303 | 9167071230 | IC,TC74HC86AF |
| U104,154 | S0031454 | IC,M56783FP |
| U204,254 | S0031454 | IC,M56783FP |
| U301,401 | S0023994 | IC NJM4565M(8P)-TE1 |
| U304,354 | S0031454 | IC,M56783FP |
| U404,454 | S0031454 | IC,M56783FP |
| U501,601 | S0023994 | IC NJM4565M(8P)-TE1 |
| U503,703 | 9167071230 | IC,TC74HC86AF |
| U504,554 | S0031454 | IC,M56783FP |
| U604,654 | S0031454 | IC,M56783FP |
| U701,801 | S0023994 | IC NJM4565M(8P)-TE1 |
| U702 | 13444414 | IC,HD74HC14FP-TR |
| U704,754 | S0031454 | IC,M56783FP |
| U804,854 | S0031454 | IC,M56783FP |
| U901 | S0023994 | IC NJM4565M(8P)-TE1 |
| U903 | 9167071230 | IC,TC74HC86AF |
| U904 | S0031454 | IC,M56783FP |

## GATHER PCB ASSY, PANEL

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145315000 | GATHER PCBA,PANEL |
| | | PANEL PCB |
| | 9260363300 | ESCUTCHEON RING |
| CN1 | 9107142100 | FLAT CABLE ASSY A |
| CN3 | 9107140600 | CABLE ASSY H |
| CN4 | 9107140700 | CABLE ASSY I |
| CN5 | 9107140800 | CABLE ASSY J |
| D1-11 | 9174028520 | LED,LA12540/TBF-4(ORG) |
| D12,28 | 9174028620 | LED,LI12540/TBF-4(RED) |
| D13-27 | 9174028520 | LED,LA12540/TBF-4(ORG) |
| D29 | 9174028520 | LED,LA12540/TBF-4(ORG) |
| D30,31 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D32 | 9174027520 | LED,SLR-332VR T32(RED) |
| D33 -36 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D37 | 9174027720 | LED,SLR-332MG T32(GRN) |
| D38-40 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D41-48 | 9174028720 | LED,LA12540/TBF-2(ORG) |
| D101-108 | 9165022150 | DIODE,TP 1SS133T |
| D111-118 | 9165022150 | DIODE,TP 1SS133T |
| D121-128 | 9165022150 | DIODE,TP 1SS133T |
| D131-138 | 9165022150 | DIODE,TP 1SS133T |
| D141-148 | 9165022150 | DIODE,TP 1SS133T |
| D151-158 | 9165022150 | DIODE,TP 1SS133T |
| D161-168 | 9165022150 | DIODE,TP 1SS133T |
| D171-172 | 9165022150 | DIODE,TP 1SS133T |
| D175-178 | 9165022150 | DIODE,TP 1SS133T |
| D221-229 | 9174028820 | LED,LI12540/TBF-2(RED) |
| 231-238 | 9174028820 | LED,LI12540/TBF-2(RED) |
| D241-248 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D249 | 9174027720 | LED,SLR-332MG T32(GRN) |
| D251-258 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D261-269 | 9174027720 | LED,SLR-332MG T32(GRN) |
| D271-278 | 9174027720 | LED,SLR-332MG T32(GRN) |
| D281-289 | 9174027520 | LED,SLR-332VR T32(RED) |
| D291-298 | 9174027520 | LED,SLR-332VR T32(RED) |
| D301-308 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D311-318 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D321-328 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D331-338 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D346-348 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D356-358 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D366-368 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D376-378 | 9174027620 | LED,SLR-332DU T32(ORG) |
| Q101-116 | 9163018420 | DTR,DTC123ES |
| Q117-125 | 9163019020 | TR,2SB1237R |
| SW1-16 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW17-33 | 9136002000 | TACT SW SKHHDA |
| SW34 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW35-42 | 9172039800 | ENCODER,EC12E24204F25 |
| SW43 | 9172040200 | ENCODER,EC12E2420802 |
| SW101-108 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW111-118 | 9136003020 | TACT SW,EVQ11L H=5 TP |

## GATHER PCB ASSY, PANEL

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| SW121-128 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW131-138 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW141-148 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW151-158 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW161-166 | 9136002000 | TACT SW,SKHHDA |
| SW167 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW168 | 9136002000 | TACT SW,SKHHDA |
| SW171-172 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW175 | 9136002000 | TACT SW,SKHHDA |
| SW176 | 9136002000 | TACT SW,SKHHDA |
| SW177-178 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| U1,2 | 9167026400 | IC,TC74HC138AP |
| U3 | 9167029400 | IC,TC74HC00AP (14P) |
| U4-11 | 9167037200 | IC TC74HC541AP(20P) |
| U12-19 | 9167067500 | IC,HD74LS374P |
| U20 | 5220098700 | IC,HD74HC574P |
| U21 | 9167026400 | IC,TC74HC138AP |
| U22 | 9167067600 | IC,HD74LS138P |
| VR1 | 9172036300 | VR,RK09K113Z401-10KB |

## GATHER PCB ASSY, MASTER

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145318000 | GATHER PCB ASSY,MASTER |
| | | MASTER JACK PCB |
| | | MASTER AMP PCB |
| | | STUDIO PCB |
| | | C.ROOM PCB |
| | | BUSS PCB |
| | | DIGITAL I/O PCB |
| | 9107143900 | CABLE ASSY V |
| | 9260366900 | WIRE CLAMP,WLD-50T |
| D1,4 | 9174020200 | LED,L-341D (RED) |
| D2 | 9174022700 | LED,L-34AD |
| D3 | 9174022700 | LED,L-34AD |
| D901,902 | 9165022150 | DIODE,TP 1SS133T |
| J1 | 9143385010 | CPJ-066-005 |
| J2 | 9144269100 | 4P B402A-B R/W |
| J101,201 | 9144520200 | PHONE JACK,JY-6353-02-250 |
| J102,202 | 9144271001 | PHONE JACK,JY-6353-02-030 |
| J103,203 | 9144272001 | PHONE JACK,JY-6353-02-040 |
| J104,204 | 9144487000 | MIC JACK,NC3MAV |
| J105,205 | 9144271001 | PHONE JACK,JY-6353-02-030 |
| J301,401 | 9144520200 | PHONE JACK,JY-6353-02-250 |
| J302,402 | 9144271001 | PHONE JACK,JY-6353-02-030 |
| J901,902 | 9144438000 | MIC JACK,NC3FAH1-0 (XLR) |
| J903,904 | 9144522100 | 2RCA HSP-242 V2-23 |
| J905,906 | 9144000200 | MIC JACK,NC3MBH(XLR) |
| P101 | 9107140000 | CABLE ASSY A |
| P102 | 9143999000 | CONNECTOR,TUC-P14X-B1 |

## GATHER PCB ASSY, MASTER

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| P103 | | 9107140100 | CABLE ASSY B |
| P104 | | 9107140200 | CABLE ASSY C |
| P105 | | 9107140300 | CABLE ASSY D |
| P106 | | 9107140400 | CABLE ASSY E |
| P107 | | 9143172000 | CONNECTOR PLUG,B4B-EH-A |
| P108 | | 9143178000 | CONNECTOR PLUG,10P |
| P109 | | 9144523900 | CONNECTOR,TWG-P7P-A1 |
| P110 | | 9107141100 | CABLE ASSY M |
| P111 | | 9107140900 | CABLE ASSY K |
| P112 | | 9144524000 | CONNECTOR,TWG-P7X-A1 |
| P113 | | 9143170000 | CONNECTOR PLUG, 2P |
| P114 | | 9143999000 | CONNECTOR,TUC-P14X-B1 |
| P115 | | 9107141200 | CABLE ASSY N |
| P122,123 | | 9144043000 | CONNECTOR,TUC-P14P-B1 |
| P901 | | 9144510000 | CONNECTOR,3675P 40VUA0 |
| P902,903 | | 9144484000 | D-SUB,DE-09SLURL2 |
| Q101,201 | | 9163310620 | TR,TP 2SC-2878A |
| Q102,202 | | 9163310620 | TR,TP 2SC-2878A |
| Q104,204 | | 9164005420 | FET,2SJ498D |
| Q106,206 | | 9163310620 | TR,TP 2SC-2878A |
| Q151,251 | | 9163310620 | TR,TP 2SC-2878A |
| Q152,252 | | 9163310620 | TR,TP 2SC-2878A |
| Q153,253 | | 9163310620 | TR,TP 2SC-2878A |
| Q154,254 | | 9163310620 | TR,TP 2SC-2878A |
| Q155,255 | | 9163310620 | TR,TP 2SC-2878A |
| Q156,256 | | 9163310620 | TR,TP 2SC-2878A |
| Q351,451 | | 9163310620 | TR,TP 2SC-2878A |
| Q903 | | 9163310420 | DTR,DTC 124ES TP |
| R136,137 | ⚠ | 9114409000 | R,NON-F 1/4W 100 FH-15 |
| R236,237 | ⚠ | 9114409000 | R,NON-F 1/4W 100 FH-15 |
| SW1-5 | | 9135041100 | PUSH SW,SPUJ50H803-TK |
| SW6 | | 9135041000 | PUSH SW,SPUJ19A602-TK |
| SW7,8 | | 9135041000 | PUSH SW,SPUJ19A602-TK |
| T901-904 | | 9173021100 | TRANS,PULSE 400UH |
| U1 | | 9179000200 | MIC CONDENSER,U-620-A |
| U101,201 | | 9167025200 | IC,BA15532N |
| U102,202 | | 9167056000 | IC,NJM4580L (8P) |
| U103-105 | | 9167040700 | IC,NE5532N |
| U501,502 | | 9167025200 | IC,BA15532N |
| U503-505 | | 9167040700 | IC,NE5532N |
| U510 | | 9167056000 | IC,NJM4580L (8P) |
| U901-910 | | 9122020620 | FILTER,EXCEMT103BT TP |
| U911-914 | | 9173014020 | FILTER,EXCEMT101BT (100PF) |
| U915-922 | | 9173014020 | FILTER,EXCEMT101BT (100PF) |
| VR1 | | 9172039000 | 5K(B) EVUE2JFK3 B53 |
| VR2 | | 9172023100 | 1S2UVR,14 10K(A)X2 |
| VR3 | | 9172023200 | 1S1UVR,11 50K(W) |
| VR4 | | 9172023100 | 1S2UVR,14 10K(A)X2 |

## GATHER PCB ASSY, TRANSPORT

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| | | *9145319020 | GATHER PCB ASSY,TRANSPORT [J,US/C] |
| | | *9145319050 | GATHER PCB ASSY,TRANSPORT [K,A,E,UK] |
| | | | TRANSPORT PCB |
| | | | LCD SUB PCB |
| | | | MIDI PCB |
| | | | TDIF PCB |
| | | 9260363400 | BRACKET TRANSPORT |
| CN1 | | 9143198000 | CONNECTOR,S9B-EH |
| CN2 | | 9173199000 | PLUG,10P S10B-EH-A |
| D181-186 | | 9165022150 | DIODE,TP 1SS133T |
| D191-196 | | 9165022150 | DIODE,TP 1SS133T |
| D201-206 | | 9165022150 | DIODE,TP 1SS133T |
| D341,344 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D342 | | 9174027720 | LED,SLR-332MG T32(GRN) |
| D343 | | 9174027520 | LED,SLR-332VR T32(RED) |
| D345,353 | | 9174028720 | LED,LA12540/TBF-2(ORG) |
| D351,352 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D354 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D355,365 | | 9174028920 | LED,LG12540/TBF-2(GRN) |
| D361,362 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D363,375 | | 9174028820 | LED,LI12540/TBF-2(RED) |
| D364 | | 9174028720 | LED,LA12540/TBF-2(ORG) |
| D371 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D373,374 | | 9174028720 | LED,LA12540/TBF-2(ORG) |
| D511-513 | | 9165022150 | DIODE,TP 1SS133T |
| D514,515 | | 9165022150 | DIODE,TP 1SS133T |
| D601-685 | | 9165022150 | DIODE,TP 1SS133T |
| F601 | ⚠ | 9150062400 | FUSE,5A 250V 51S050H [J,US/C] |
| | ⚠ | 9150062500 | FUSE,5A 250V 50T050H [K,A,E,UK] |
| F601 | | 9150062100 | FUSE HOLDER,CQ-203B |
| J501 | | 9144462000 | PIN JACK,1P HSP-241V1B |
| J502 | | 9144520300 | PHONE JACK,069-2 |
| J503-505 | | 9144481000 | DIN JACK,HDC-052A-13 |
| J601,602 | | 9144488000 | BNC,COH2201-A |
| L1 | | 9173019900 | COIL,RCH875-151K |
| L601,602 | | 9173019850 | COIL,47UH-EC24-470KT5 |
| P1 | | 9143170000 | CONNECTOR PLUG,2P |
| P2 | | 9143172000 | CONNECTOR PLUG,B4B-EH-A |
| P501 | | 9144489000 | D-SUB,DA-15PLURL2 |
| P502 | | 9107140500 | CABLE ASSY G |
| P601-604 | | 9144445001 | D-SUB,205A-25FSTBBB3 |
| P611,612 | | 9144521000 | CONNECTOR,3675P 34VUA0 |
| P613 | | 9143174000 | PLUG,6P B6B-EH-A |
| P614 | | 9107143200 | FLAT CABLE ASSY L |
| Q1,2 | | 9163461020 | TR,2SC2236-0 TP |
| Q501 | | 9163310420 | DTR,DTC 124ES TP |
| RA1,3,5 | | 9111304000 | R,ARRAY 2.2K*8 P=2.54 |
| RA2,4,6 | | 9111305000 | R,ARRAY 4.7K*8 P=2.54 |
| SW201-203 | | 9135041400 | PUSH SW,SKBMFA000A-TK |

## GATHER PCB ASSY, TRANSPORT

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| SW211,212 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW213,221 | | 9136002000 | TACT SW,SKHHDA |
| SW222,223 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW231,241 | | 9136002000 | TACT SW,SKHHDA |
| SW232,233 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW242,243 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW251-253 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW601 | | 9135041200 | SLIDER SW,SSSF123NA1-TK |
| T1 | | 9125145000 | TRANS,EW-12H/TW |
| U501 | | 9167026900 | IC,TC4069UBP |
| U502 | | 9167051100 | PHOTO COUPLER,PC-900 |
| U504,506 | | 9122020620 | FILTER,EXCEMT103BT TP |
| U509,510 | | 9122020620 | FILTER,EXCEMT103BT TP |
| U601 | | E0062040 | GP1FA550RZ |
| U602 | | E0062920 | GP1FA550TZ |
| U604 | | 9173014020 | FILTER,EXCEMT101BT (100PF) |
| U701 | | 9167070630 | IC,TC74VHCT00AF |

## GATHER PCB ASSY, MOTHER

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| | | *9145317000 | GATHER PCBA,MOTHER<br>MOTHER PCB |
| J1,2 | | 9144520400 | CARD EDGE,4024S120F0B |
| J3-5 | | 9144510000 | CONNECTOR,3675P 40VUA0 |
| P1 | | 9143199000 | PLUG,10P(S10B-EH-A) |
| P2 | | 9143198000 | CONNECTOR,S9B-EH |
| P3 | | 9144332000 | PULG,S4B-EH |

## GATHER PCB ASSY, POWER

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| | | *9145342020 | GATHER PCB ASSY,POWER<br>[J,US/C] |
| | | *9145342050 | GATHER PCB ASSY,POWER<br>[K,A,E,UK] |
| | | | PCB,POWER |
| | | | PCB,POWER SW |
| | | | PCB,TRANS 1 |
| | | | PCB,TRANS 2 |
| | | | PCB,TR1 |
| | | | PCB,TR2 |
| | | | PCB,TR3 |
| | | | PCB,TR4 |
| | | | PCB,TR5 |
| | | | PCB,BD |
| CN1 | | 9144491000 | CONNECTOR,B2P3-VH |
| C1,2 | ⚠ | 9117304100 | C,ELEC 4700U 35V |
| C3,4 | ⚠ | 9117200020 | C,ELEC TP 100M 35V |
| C101-103 | ⚠ | 9120000101 | SPARK KILLER,0.0047M 250V |
| D1 | ⚠ | 9165026900 | BRIDGE DIODE,RS403L |

## GATHER PCB ASSY, POWER

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| D3 | | 9165027000 | BRIDGE DIODE,KBU6D |
| D4,5 | | 9165020550 | DIODE,LT 1N4003 TP 0.6MM |
| D6 | | 9166055551 | Z-DIODE,MTZJ39B |
| D7 | | 9166054651 | Z-DIODE,MTZ J 16 B |
| D8,9 | | 9165022150 | DIODE,TP 1SS133T |
| D10-13 | | 9165020550 | DIODE,LT 1N4003 TP 0.6MM |
| D14,15 | | 9165020550 | DIODE,LT 1N4003 TP 0.6MM |
| D16 | ⚠ | 9165027000 | BRIDGE DIODE,KBU6D |
| EP1 | | 9229088000 | EARTH PLATE B (GND-8) |
| F1,2 | ⚠ | 9150036000 | T-LAG FUSE,4A 250V T<br>[J,US/C] |
| F1,2 | ⚠ | 9150047000 | T-LAG FUSE,4A 250V T<br>[K,A,E,UK] |
| F3 | ⚠ | 9150028000 | T-LAG FUSE,1.6A 250V T<br>[K,A,E,UK] |
| F3 | ⚠ | 9150037000 | T-LAG FUSE,1.6A 250V T<br>[J,US/C] |
| F4 | ⚠ | 9150036000 | T-LAG FUSE,4A 250V T<br>[J,US/C] |
| F4 | ⚠ | 9150047000 | T-LAG FUSE,4A 250V T<br>[K,A,E,UK] |
| F1-4 | | 9150062100 | FUSE HOLDER CQ-203B |
| L101 | ⚠ | 5292806300 | FILTER,FKOB16MH13 |
| P1 | | 9143182000 | PLUG,14P B14B-EH-A |
| P2 | | 9143176000 | PLUG,8P B8B-EH-A |
| P3 | | 9143180000 | CONNECTOR PLUG,12P |
| P4 | | 9143174000 | PLUG,6P B6B-EH-A |
| P5 | | 9143178000 | CONNECTOR PLUG,10P |
| P6 | | 9143170000 | CONNECTOR PLUG,2P |
| P7 | | 9143180000 | CONNECTOR PLUG,12P |
| P8 | | 9143172000 | CONNECTOR PLUG,B4B-EH-A |
| P9 | | 9143180000 | CONNECTOR PLUG,12P |
| P101 | ⚠ | 9144493000 | AC INLET,M1908-B |
| P102,103 | | 9144491000 | CONNECTOR,B2P3-VH |
| Q1 | ⚠ | 9163202900 | TR,2SB1274R |
| Q2 | ⚠ | 9163202900 | TR,2SB1274R |
| Q3 | ⚠ | 9163610300 | TR,2SD1913R |
| Q4 | ⚠ | 9163205000 | TR,2SB1018A-O |
| Q5 | | 9163019120 | TR,2SD1858R |
| Q6 | | 9163013320 | DTR,DTA115ES |
| Q9 | ⚠ | 9163202900 | TR,2SB1274R |
| R1,2 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| SW101 | ⚠ | 9135037200 | POWER SW,SFDLB11M7U TK |
| U101 | ⚠ | 5220425800 | IC,M5230LA (8P) |
| U102,103 | ⚠ | 5220446100 | IC,M5237L (3P) |

## GATHER PCB ASSY,METER BRIDGE (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | 9145336000 | GATHER PCBA,METER BRIDGE<br>PCB,INPUT METER<br>PCB,MASTER METER |
| D101,102 | 9174028300 | LED,L-1043SRD |
| D103,104 | 9174028201 | LBD1013-20/A |
| D105-108 | 9174029400 | LED,DA0411YWA(YELLOW) |
| D109-114 | 9174024820 | LED,L-3XAD-TNB5/4.7-90 |
| D115-117 | 9174028400 | LED,L-1043YD |
| D118-120 | 9174024820 | LED,L-3XAD-TNB5/4.7-90 |
| D121-123 | 9165022150 | DIODE,TP 1SS133T |
| D124,125 | 9174028201 | LBD1013-20/A |
| D201-208 | 9174028201 | LBD1013-20/A |
| D209-216 | 9174028300 | LED,L-1043SRD |
| D217-224 | 9174028201 | LBD1013-20/A |
| J101 | 9144519720 | PLUG,B16B-PH-K (RED) |
| J102 | 9144519700 | PLUG,B16B-PH-K |
| J103 | 9144356000 | CONNECTOR,B13B-ZR |
| J201 | 9144330020 | PLUG,SI6B-PH-K-S (RED) |
| J202 | 9144330000 | PLUG,S16B-PH-K-S |
| SW101-103 | 9136002000 | TACT SW,SKHHDA |

## GATHER PCB ASSY,METER DRIVER (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | 9145335000 | GATHER PCBA,METER DRIVER<br>PCB,METER DRIVER |
| J1 | 9144524500 | D-SUB DB-25PIUCT2 |
| J2,4 | 9144330020 | PLUG SI6B-PH-K-S (RED) |
| J3,5 | 9144330000 | PLUG,S16B-PH-K-S |
| J6,8 | 9144330020 | PLUG SI6B-PH-K-S (RED) |
| J7,9 | 9144330000 | PLUG,S16B-PH-K-S |
| J10 | 9144356000 | CONNECTOR B13B-ZR |
| L1 | 9173017430 | COIL,SLF12565T-470M2R4 |
| Q1-96 | 9163461430 | DTR,DTC123EKA |
| R33-36 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| U1 | 9167067730 | IC,HD74LV245AFPEL |
| U2,7 | 9167065430 | IC,HD74LV244AFPEL |
| U3,4 | 9167075230 | IC,HD74LV138AFPEL |
| U5,8 | 9167075230 | IC,HD74LV138AFPEL |
| U6 | 9167066430 | IC,HD74LV374AFPEL |
| U9 | 9167075230 | IC,HD74LV138AFPEL |
| U10 | 9167065430 | IC,HD74LV244AFPEL |
| U11 | 9167075030 | IC,HD74LV04AFPEL |
| U12-15 | 9167051630 | IC,TD62M8600F(18P) |
| U16-27 | 9167066430 | IC,HD74LV374AFPEL |

## IF-TD/DM (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9260365700 | PANEL,TD/DM CARD |
| | *9260366200 | LEVER SLOT |
| | *9260330700 | D-SUB SCREW,HW-H118MN02 |
| | *9145329000 | GATHER PCB ASSY,IF-TD/DM |
| | | PCB,IF-TD/DM |
| D1 | 9165023530 | DIODE,1SS355 TE17 |
| D2-17 | 9165024730 | DA,IMN10 T108 CHIP |
| P1 | 9144522200 | HEADER6,2556P6UA00 |
| P2 | 9144482000 | D-SUB DB-25SLURL2 |
| P3 | 9144489000 | D-SUB DA-15PLURL2 |
| Q1 | 9163459030 | DTR,DTC363EK T146 |
| R17,32 | 9111297030 | R,ARRAY 10KX8 YC-15J |
| R50,62 | 9111297030 | R,ARRAY 10KX8 YC-15J |
| R63 | 9111282030 | R,ARRAY 2.2KX8 MNR35 CHIP |
| R88 | 9111283030 | R,ARRAY 4.7KX8 MNR35 CHIP |
| U1-3 | 9167055830 | IC,HD74LV541AFPEL |
| U5,6 | 9167055830 | IC,HD74LV541AFPEL |
| U7 | 9167067730 | IC,HD74LV245AFPEL |
| U8 | 9167045830 | IC,HD74HC541FPV |
| U9 | 9167050730 | IC,SN74HCT541NSR(20P) |
| U10 | 9167064330 | IC,HD74LVC541AFPEL(20P) |
| U11,12 | 9173016230 | EMI,EXC CET 471U |
| U13 | 9167040030 | IC,M66230FP |
| U14 | 9173016230 | EMI,EXC CET 471U |
| U15 | 9167050230 | IC,M5M34051FP |
| X1 | 9173013930 | CRYSTAL,SK3 16MHZ |

## IF-AE/DM (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9260365900 | PANEL,AE/DM CARD |
| | *9260366200 | LEVER SLOT |
| | *9260330600 | D-SUB WASHER,HW-C050MN00 |
| | *9260330700 | D-SUB SCREW,HW-H118MN02 |
| | *9145331000 | GATHER PCB ASSY,IF-AE/DM |
| | | PCB,IF-AE/DM |
| D1 | 9165023530 | DIODE 1SS355 TE17 |
| D2,3 | 9165024730 | DA,IMN10 T108 CHIP |
| D4,5 | 9165024730 | DA,IMN10 T108 CHIP |
| D6,7 | 9165024730 | DA,IMN10 T108 CHIP |
| D8,9 | 9165024730 | DA,IMN10 T108 CHIP |
| D10,11 | 9165024730 | DA,IMN10 T108 CHIP |
| D12,13 | 9165024730 | DA,IMN10 T108 CHIP |
| J1 | 9144482000 | D-SUB DB-25SLURL2 |
| J2 | 9143174000 | PLUG 6P B6B-EH-A |
| L1,2 | 9122022230 | EMI FILTER,NFM51R00P506 |
| L3,4 | 9122022230 | EMI FILTER,NFM51R00P506 |
| L5,6 | 9122022230 | EMI FILTER,NFM51R00P506 |
| L7,8 | 9122022230 | EMI FILTER,NFM51R00P506 |
| R39,43 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R46 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| T1-8 | E00595800A | TRANS,PULSE 400UH |
| U1,4 | 9167055830 | IC,HD74LV541AFPEL |
| U2 | S0043574 | IC,CS8415A-CZ |
| U3 | 9167051030 | IC,NJM78L05UA-TE1(3P) |
| U5,7 | 9167055830 | IC,HD74LV541AFPEL |
| U6 | S0042443 | IC,XCS40XL-4PQ208C |
| U8,12 | 9167055830 | IC,HD74LV541AFPEL |
| U9 | 9167074930 | IC,HD74LV00AFPEL |
| U10 | 9167067730 | IC,HD74LV245AFPEL |
| U11 | 9167075030 | IC,HD74LV04AFPEL |
| U13,14 | 9167055830 | IC,HD74LV541AFPEL |
| U15 | 9167076230 | IC,DS26C31TM |
| U16 | 9167055830 | IC,HD74LV541AFPEL |
| U17 | 9167076330 | IC,DS26C32ATM |

## IF-AD/DM (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9260365800 | PANEL,AD/DM CARD |
| | *9260366200 | LEVER SLOT |
| | *9260330600 | D-SUB WASHER,HW-C050MN00 |
| | *9260330800 | D-SUB SCREW,HW-H118EN00 |
| | *9145330000 | GATHER PCBA,IF-AD/DM |
| | | PCB,IF-AD/DM |
| D1 | 9165023530 | DIODE,1SS355 TE17 |
| J1 | 9167073700 | GP1FA550TZ |
| J2 | 9144484000 | D-SUB,DE-09SLURL2 |
| J3 | 9167073600 | GP1FA550RZ |
| L1,2 | 9122021230 | COIL,47UH ELJPA470KF CHIP |
| L3,4 | 9122022230 | EMI FILTER,NFM51R00P506 |
| R1,2 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R32,35 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R36,37 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R38 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| U1,2 | 9167076130 | IC,TC74HCT244AFP |
| U3,6 | 9167055830 | IC,HD74LV541AFPEL |
| U4 | 9167075130 | IC,HD74LV74AFPEL |
| U5 | 9167075330 | IC,HD74LV139AFPEL |
| U7,9 | 9167075030 | IC,HD74LV04AFPEL |
| U8,14 | 9167055830 | IC,HD74LV541AFPEL |
| U10,13 | 9167076130 | IC,TC74HCT244AFP |
| U11,12 | 9167075230 | IC,HD74LV138AFPEL |
| U15 | 9167055830 | IC,HD74LV541AFPEL |
| U16 | 9167068830 | IC,TC74HCT245AFP |
| U17 | 9167067730 | IC,HD74LV245AFPEL |
| U18,21 | 9167051030 | IC,NJM78L05UA-TE1(3P) |
| U19 | 9167066630 | IC,AL1401A |
| U20 | 9167051430 | IC,TC74VHCT04AF(14P) |
| U22 | 9167066730 | IC,AL1402 |
| U23,24 | 9167075030 | IC,HD74LV04AFPEL |
| U25,28 | 9167075430 | IC,HD74LV273AFPEL |
| U26 | 9167070530 | IC,PC410 |
| U27 | 9167040030 | IC,M66230FP |
| X1 | 9173013930 | CRYSTAL,SK3 16MHZ |

## IF-CS/DM (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9260366100 | PANEL,CS/DM CARD |
| | *9260366200 | LEVER SLOT |
| | *9260330600 | D-SUB WASHER,HW-C050MN00 |
| | *9260330800 | D-SUB SCREW,HW-H118EN00 |
| | *9109031900 | CABLE,CASCADE-DM |
| | *9145333000 | GATHER PCB ASSY,IF-CS/DM |
| | | PCB,IF-CS/DM |
| D1,2 | 9174027430 | LED,KPK-3020NC(ORG) |
| J1 | 9144483000 | D-SUB DB-37SLURL2 |
| L1-14 | 9122022230 | EMI FILTER,NFM51R00P506 |
| R24-27 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R48 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| U1,2 | 9167055830 | IC,HD74LV541AFPEL |
| U3,9 | 9167055830 | IC,HD74LV541AFPEL |
| U4 | 9167066330 | IC,HD74LV32AFPEL |
| U5 | 9167075030 | IC,HD74LV04AFPEL |
| U7 | 9167066230 | IC,HD74LV125AFPEL |
| U8,10 | 9167075230 | IC,HD74LV138AFPEL |
| U11,12 | 9167055830 | IC,HD74LV541AFPEL |
| U13,15 | 9167055830 | IC,HD74LV541AFPEL |
| U14,19 | 9167067730 | IC,HD74LV245AFPEL |
| U16 | 9167064830 | IC,HD74LV08AFP |
| U17 | S0038953 | IC,ADSP-21065L |
| U18 | 9173020430 | CRYSTAL,MIN35A-T 30.0MHZ |
| U20 | 9167069130 | IC,HD74LV574AFPEL |
| U21 | 9167055830 | IC,HD74LV541AFPEL |
| U22,23 | 9167070830 | IC,DS90LV032ATM |
| U24,25 | 9167070930 | IC,DS90LV031ATM |

## IF-AN/DM (OPTION)

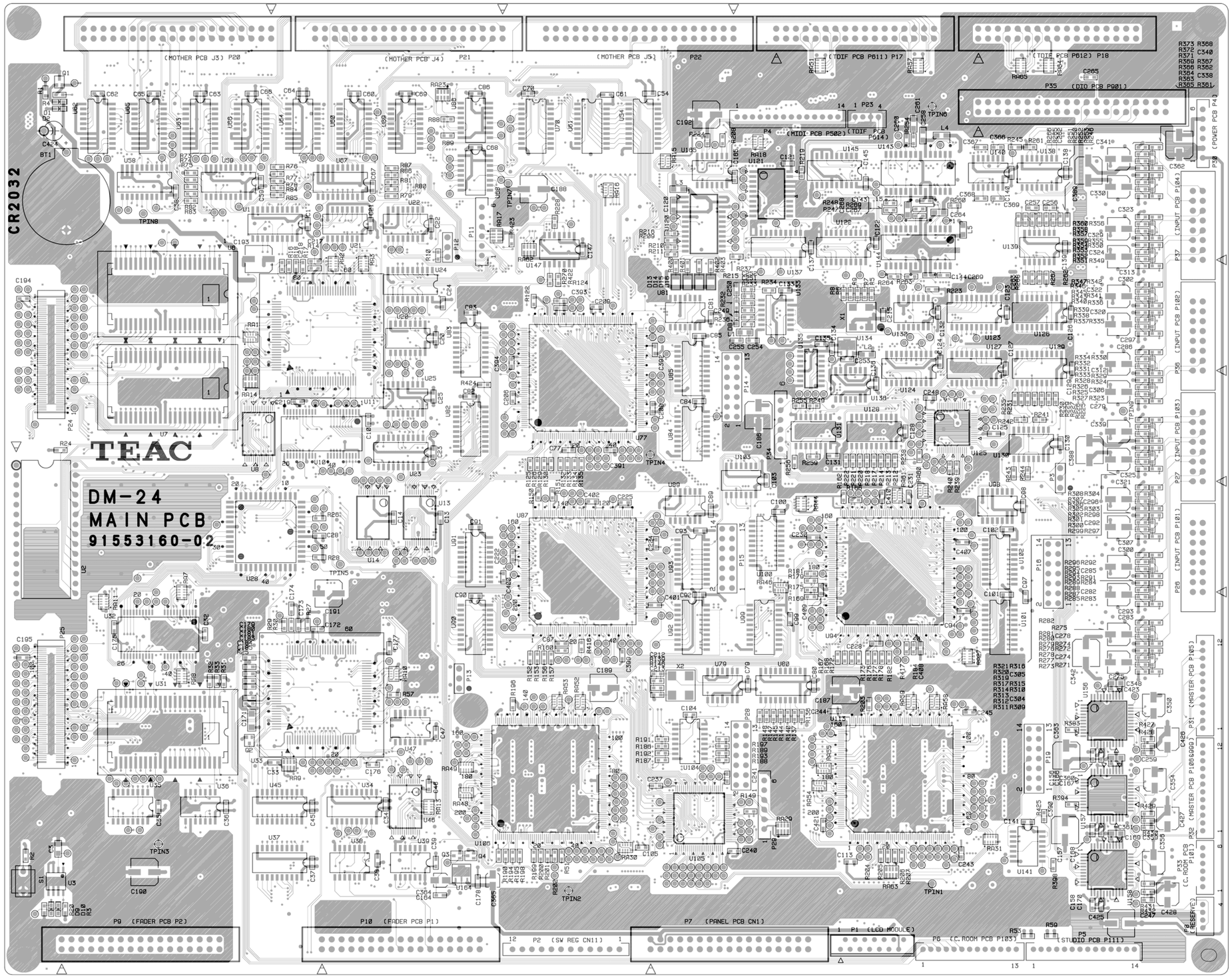
| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9260366000 | PANEL,AN/DM CARD |
| | *9260366200 | LEVER SLOT |
| | *9260330700 | D-SUB SCREW,HW-H118MN02 |
| | *9145332000 | GATHER PCBA,IF-AN/DM |
| | | PCB,IF-AN/DM |
| D010,020 | 9165023530 | DIODE,1SS355 TE17 |
| D011-018 | 9165023530 | DIODE,1SS355 TE17 |
| D021-028 | 9165023530 | DIODE,1SS355 TE17 |
| D031-038 | 9165023530 | DIODE,1SS355 TE17 |
| D041-048 | 9165023530 | DIODE,1SS355 TE17 |
| J010,020 | 9144482000 | D-SUB,DB-25SLURL2 |
| L010,020 | 9122022330 | COIL,LQH4C100K04 |
| L011-018 | 9173020930 | BEADS,BLM11B121SD |
| L021-028 | 9173020930 | BEADS,BLM11B121SD |
| L031-038 | 9173020930 | BEADS,BLM11B121SD |
| L041-048 | 9173020930 | BEADS,BLM11B121SD |
| L050,060 | 9122022730 | BEAD,BK1608HS102-T |
| L070,080 | 9122022730 | BEAD,BK1608HS102-T |

## IF-AN/DM (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| L090,100 | 9122022730 | BEAD,BK1608HS102-T |
| L110,120 | 9122022730 | BEAD,BK1608HS102-T |
| L130,140 | 9122022730 | BEAD,BK1608HS102-T |
| L150,160 | 9122022730 | BEAD,BK1608HS102-T |
| L501-504 | 9122022330 | COIL,LQH4C100K04 |
| P020 | 9143174000 | PLUG,6P B6B-EH-A |
| Q010,030 | 9163021430 | DTR,DTA114EKAT-146 |
| Q011-018 | 9163021430 | DTR,DTA114EKAT-146 |
| Q020,040 | 9163461230 | DTR,DTC114YKAT-146 |
| R300,310 | 9111306030 | R,ARRAY MNR15E0RPJ103 |
| R320,330 | 9111306030 | R,ARRAY MNR15E0RPJ103 |
| U010 | S00438000A | IC,PLD(AD)DM OPT |
| U020 | 9167026700 | IC,NJM7812FA (3P) |
| U030 | 9167035800 | IC,NJM7912FA (3P) |
| U501-504 | 9167064530 | IC,AK5383VS-E2 |
| U521-U524 | 9167076430 | IC,AK4393VF |
| SW011-018 | 9135041730 | SLIDE SW,CHS-01TA1 |
| SW021-028 | 9135041730 | SLIDE SW,CHS-01TA1 |
| SW031-038 | 9135041730 | SLIDE SW,CHS-01TA1 |
| SW041-048 | 9135041730 | SLIDE SW,CHS-01TA1 |

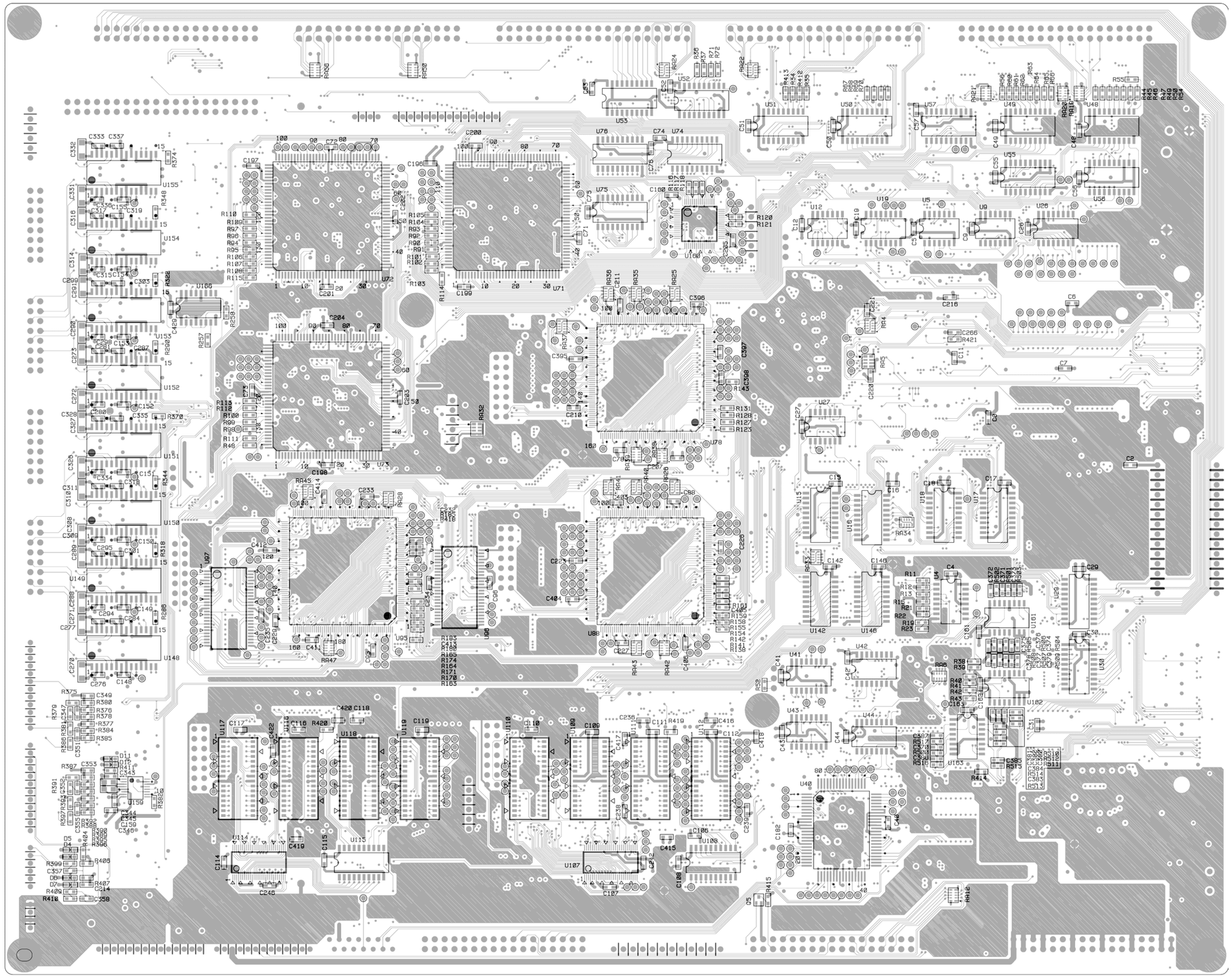
**MAIN PCB**

SIDE A

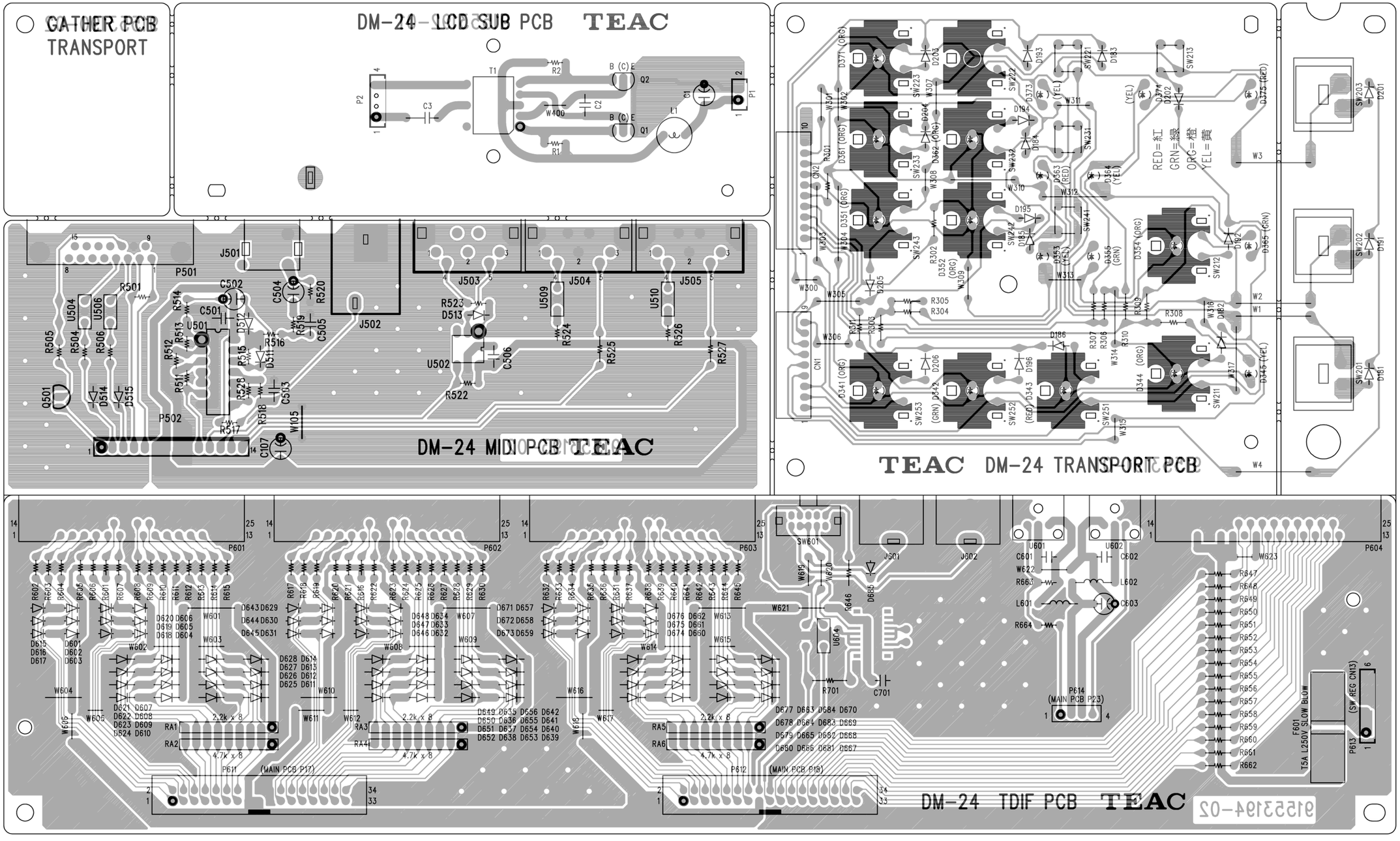


**MAIN PCB**

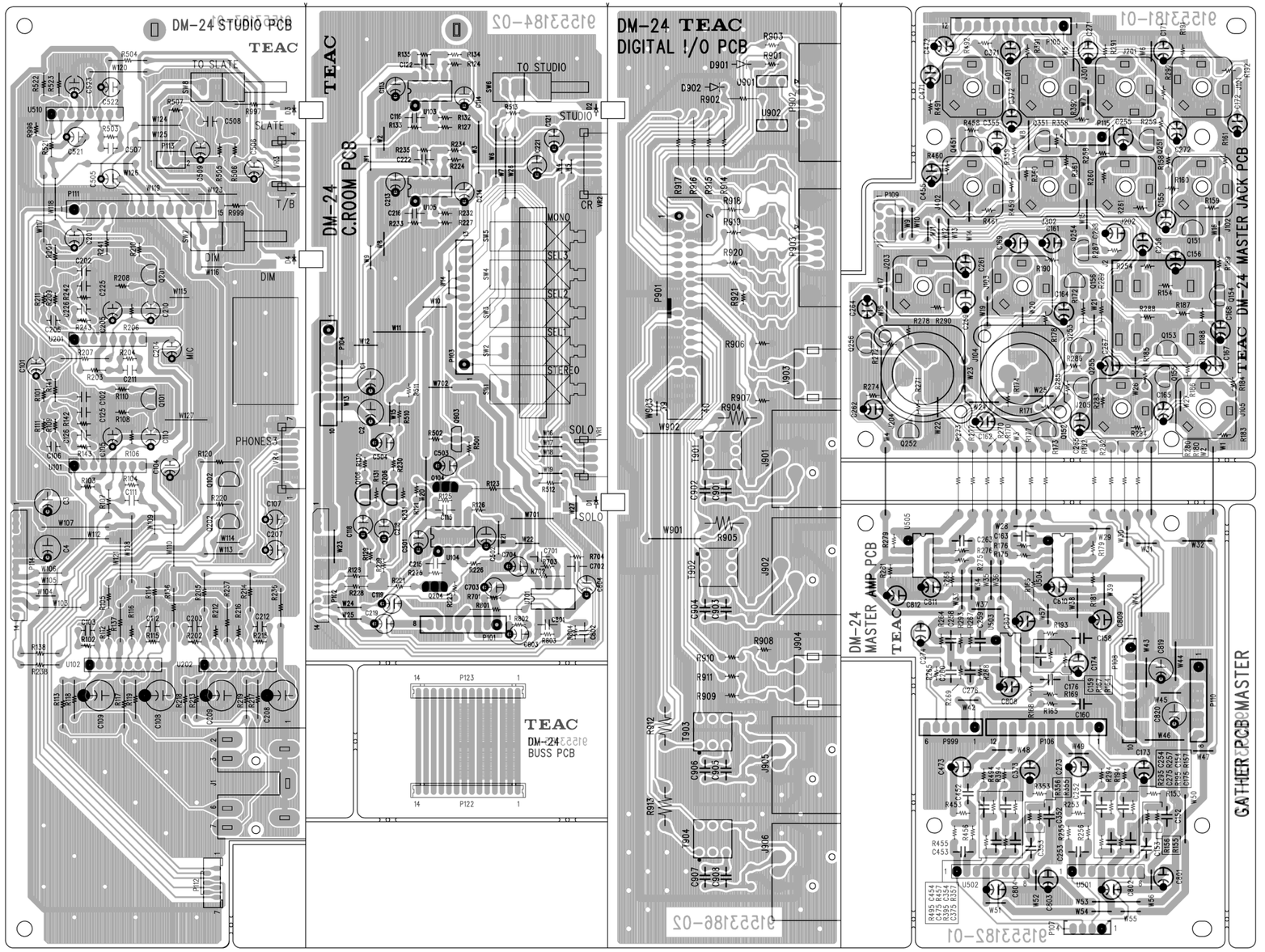
SIDE B



**GATHER PCB, TRANSPORT (TRANSPORT PCB, LCD SUB PCB, MIDI PCB, TDIF PCB)**

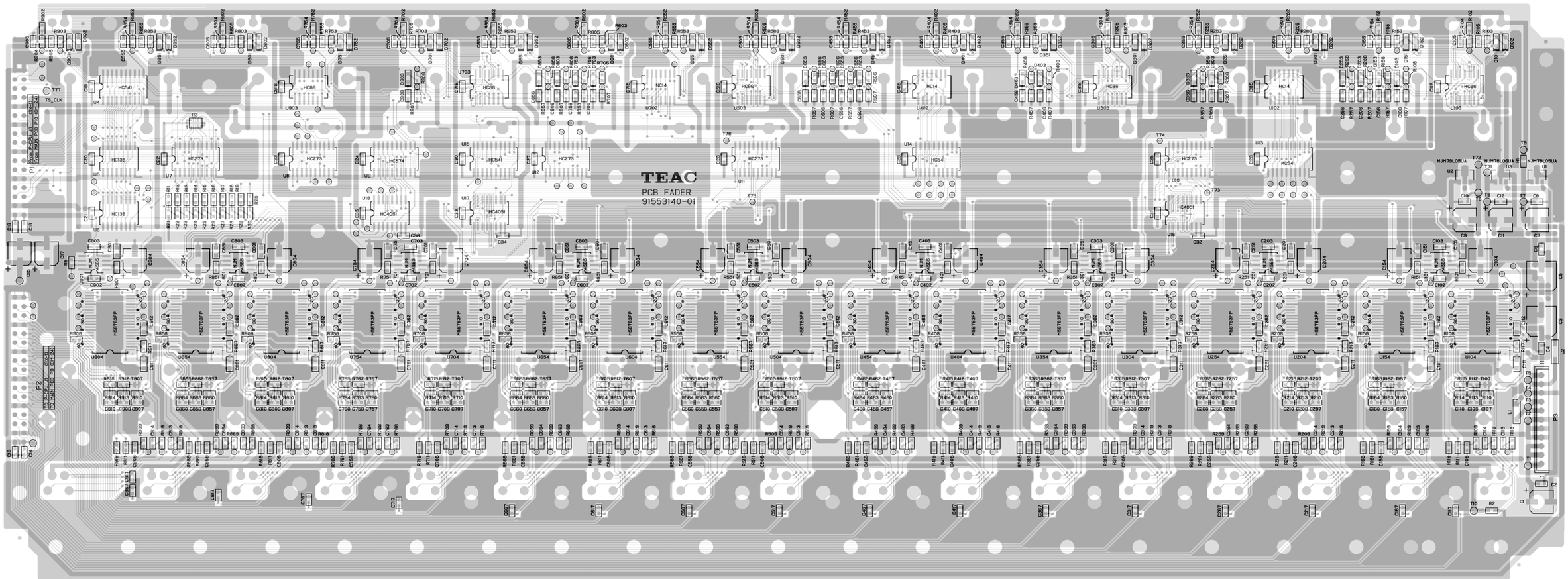


**GATHER PCB, MASTER (STUDIO PCB, C.ROOM PCB, DIGITAL I/O PCB, MASTER JACK PCB, MASTER AMP PCB, BUSS PCB)**



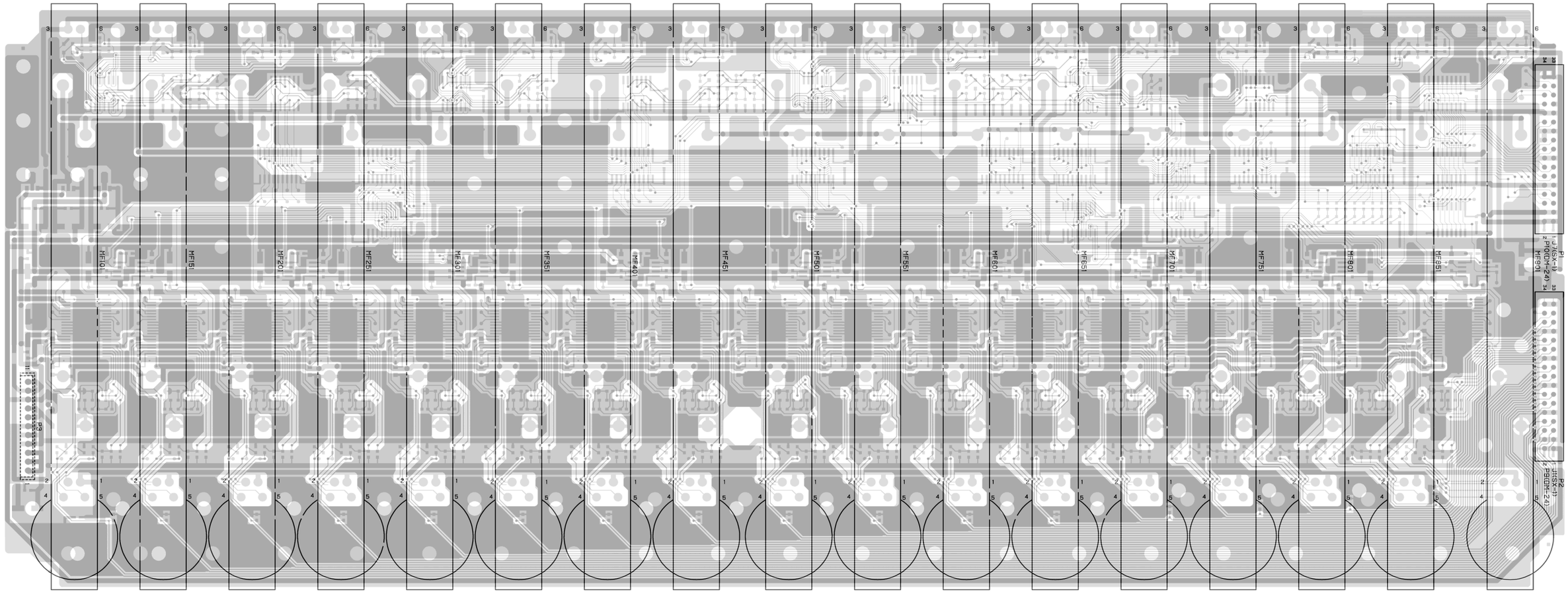
**FADER PCB**

SIDE A



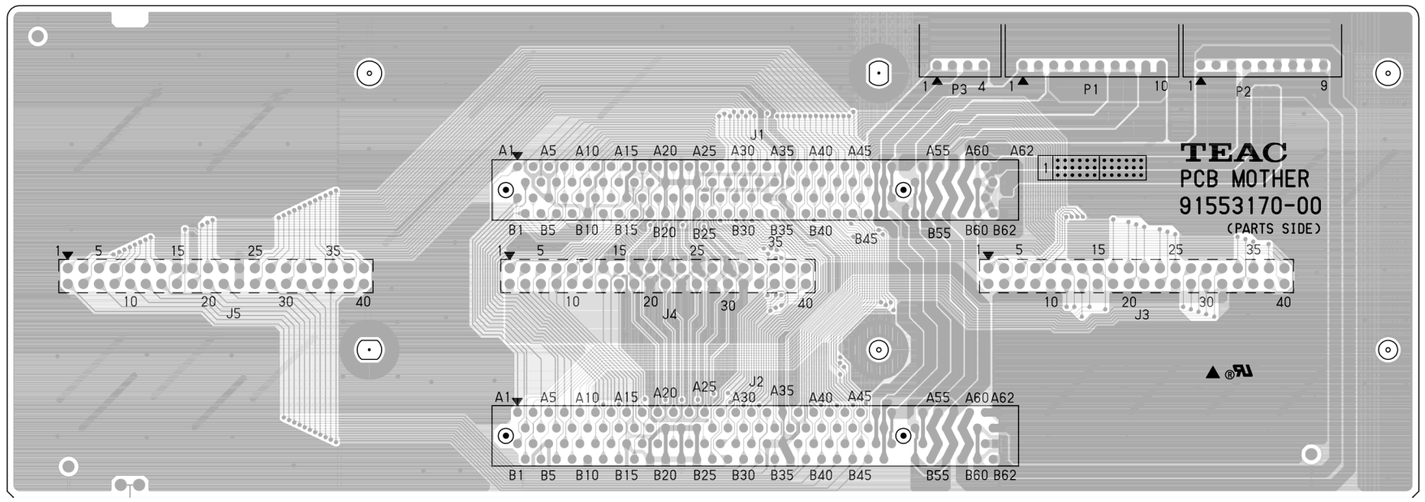
**FADER PCB**

SIDE B



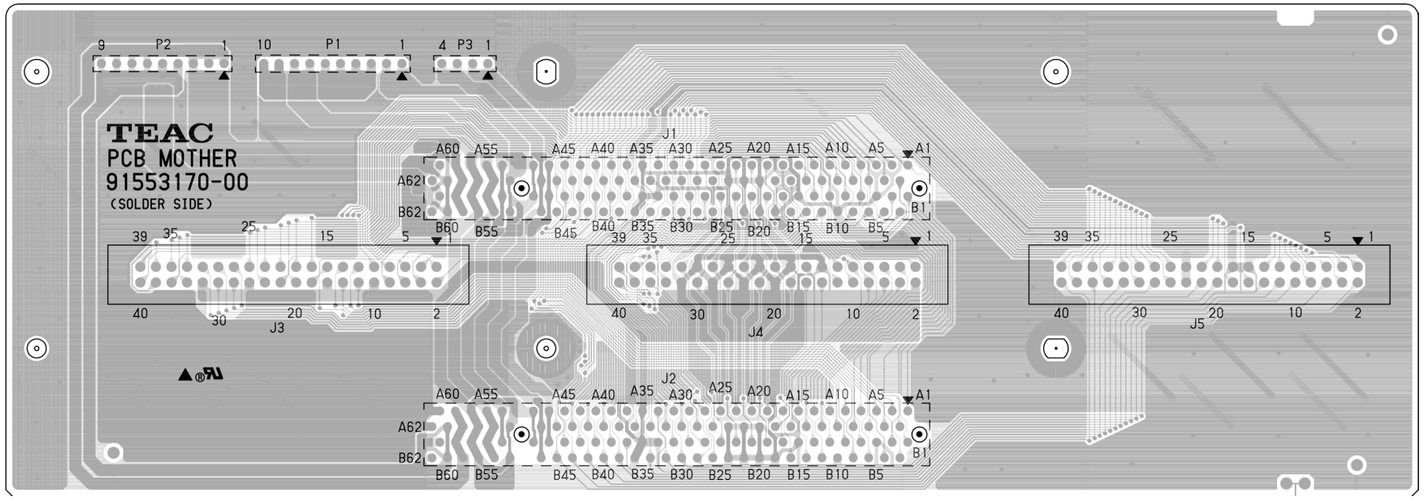
**MOTHER PCB**

SIDE A



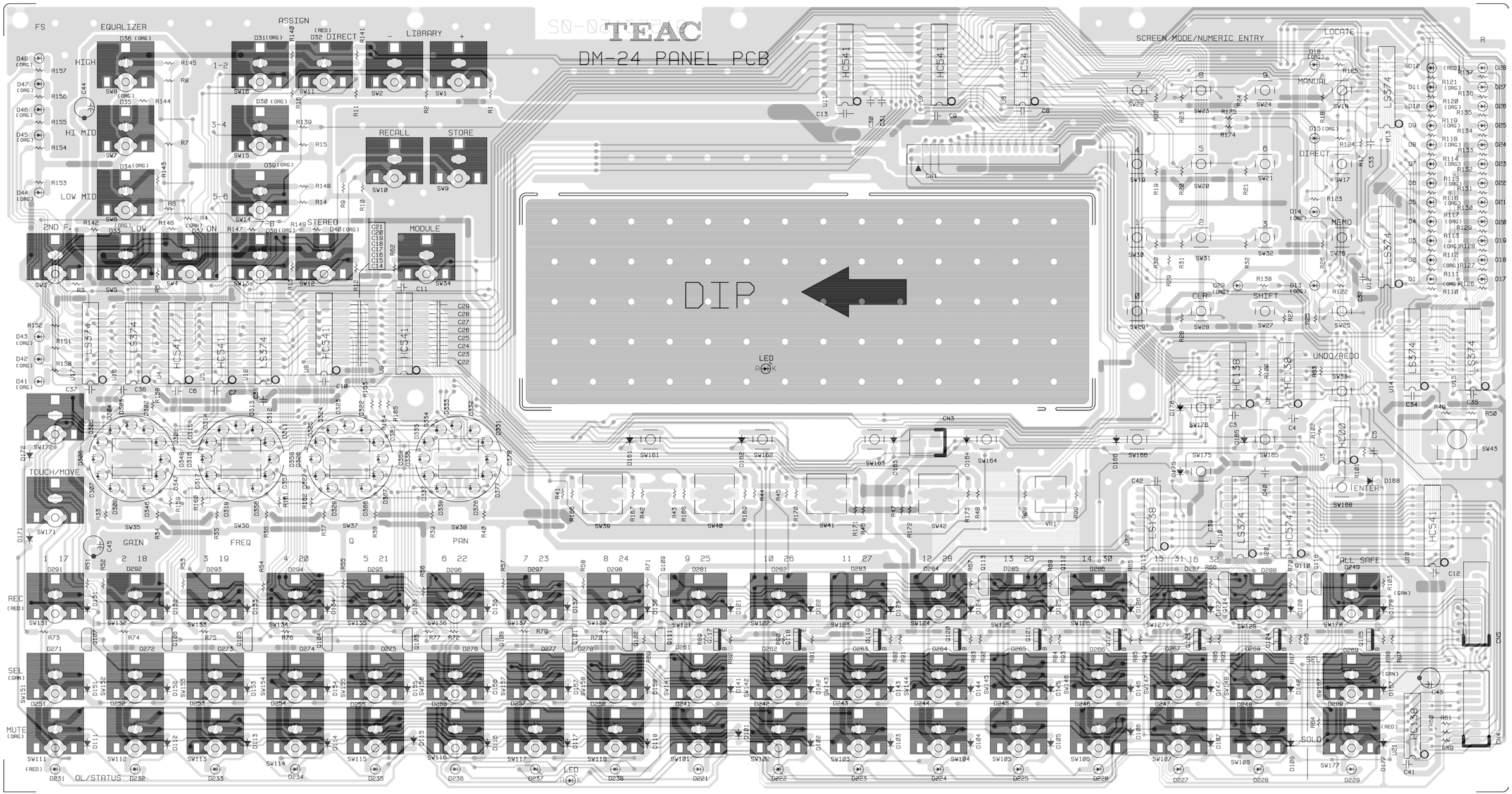

**MOTHER PCB**

SIDE B



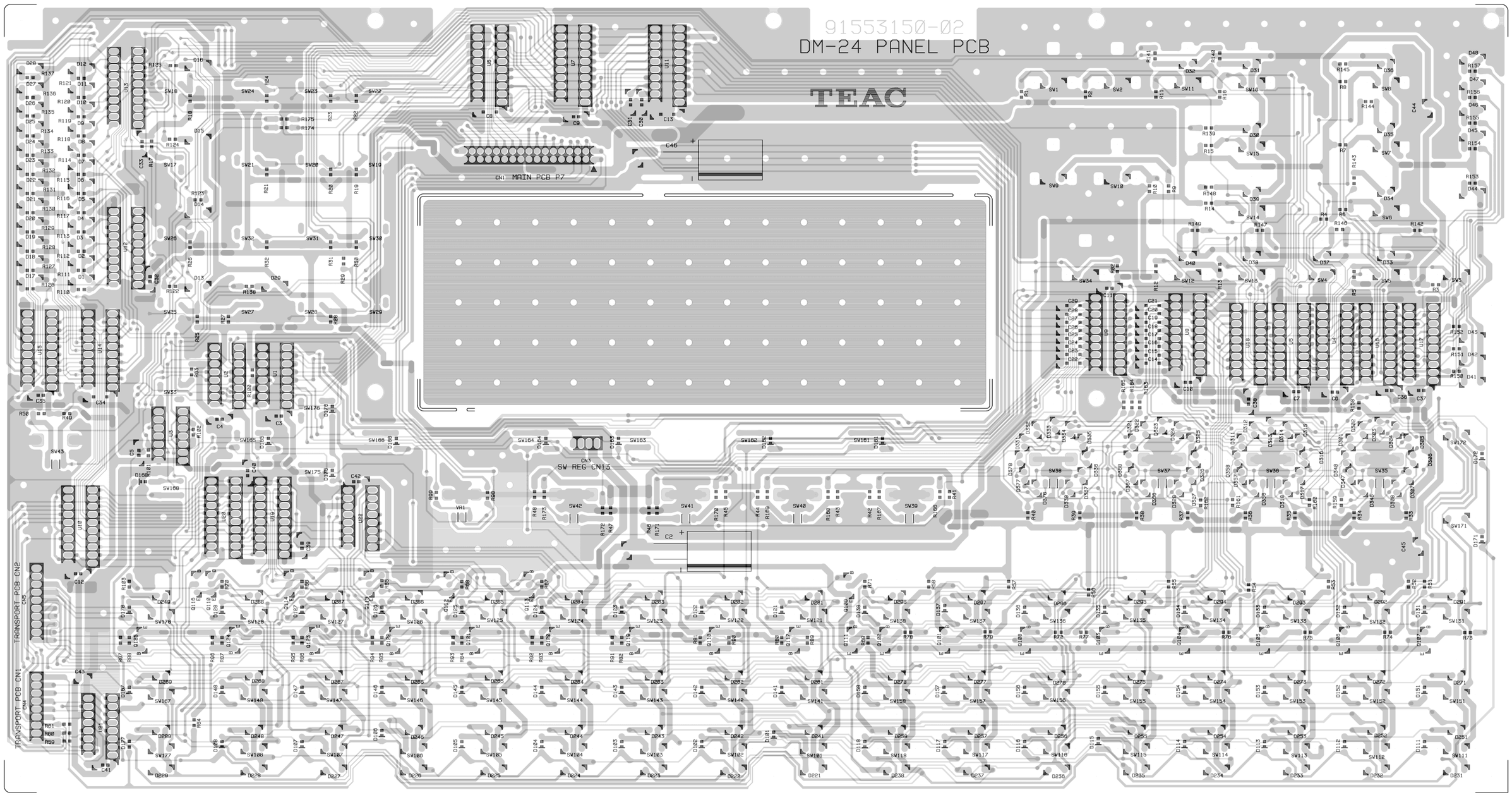
**PANEL PCB**

SIDE A

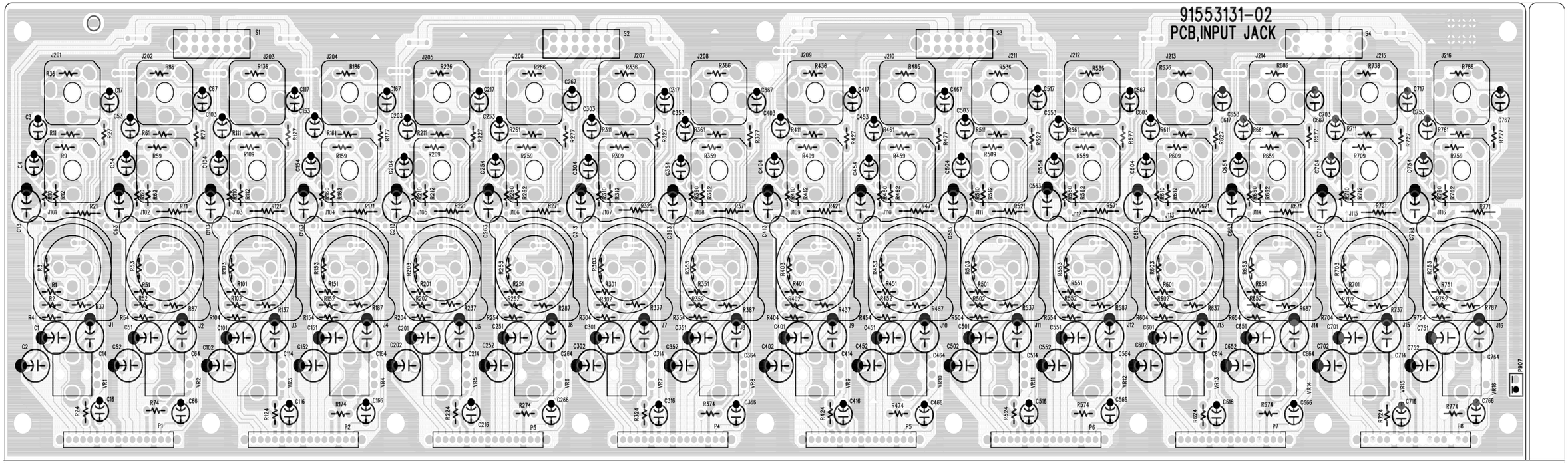


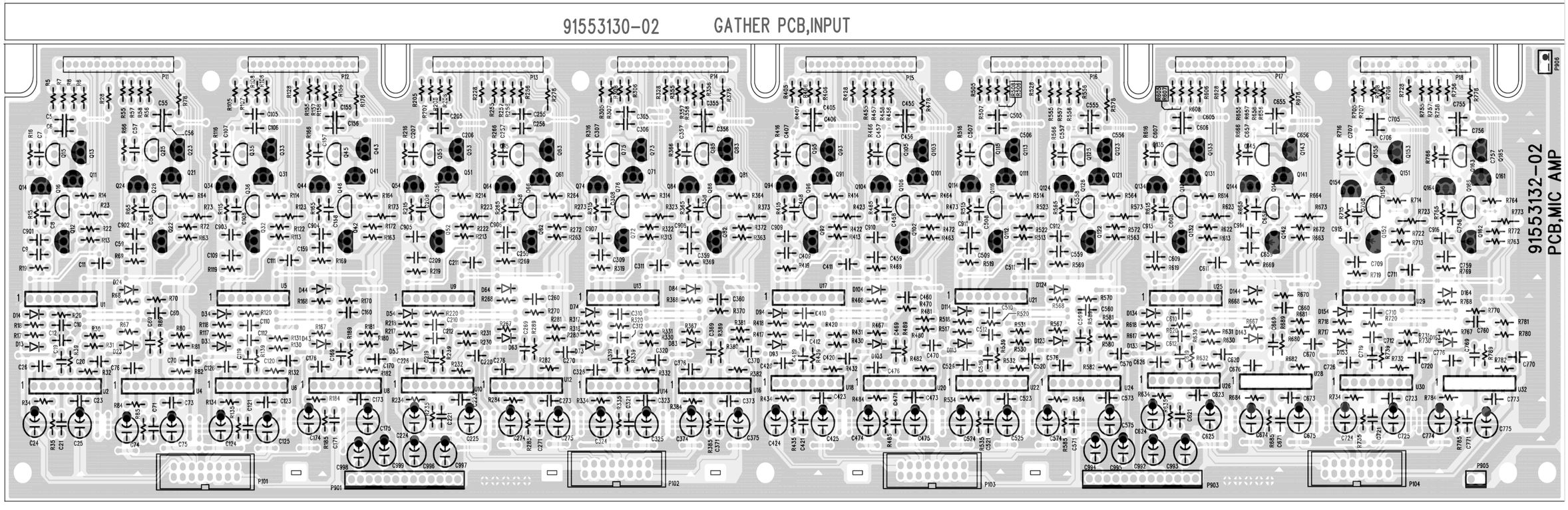
**PANEL PCB**

SIDE B

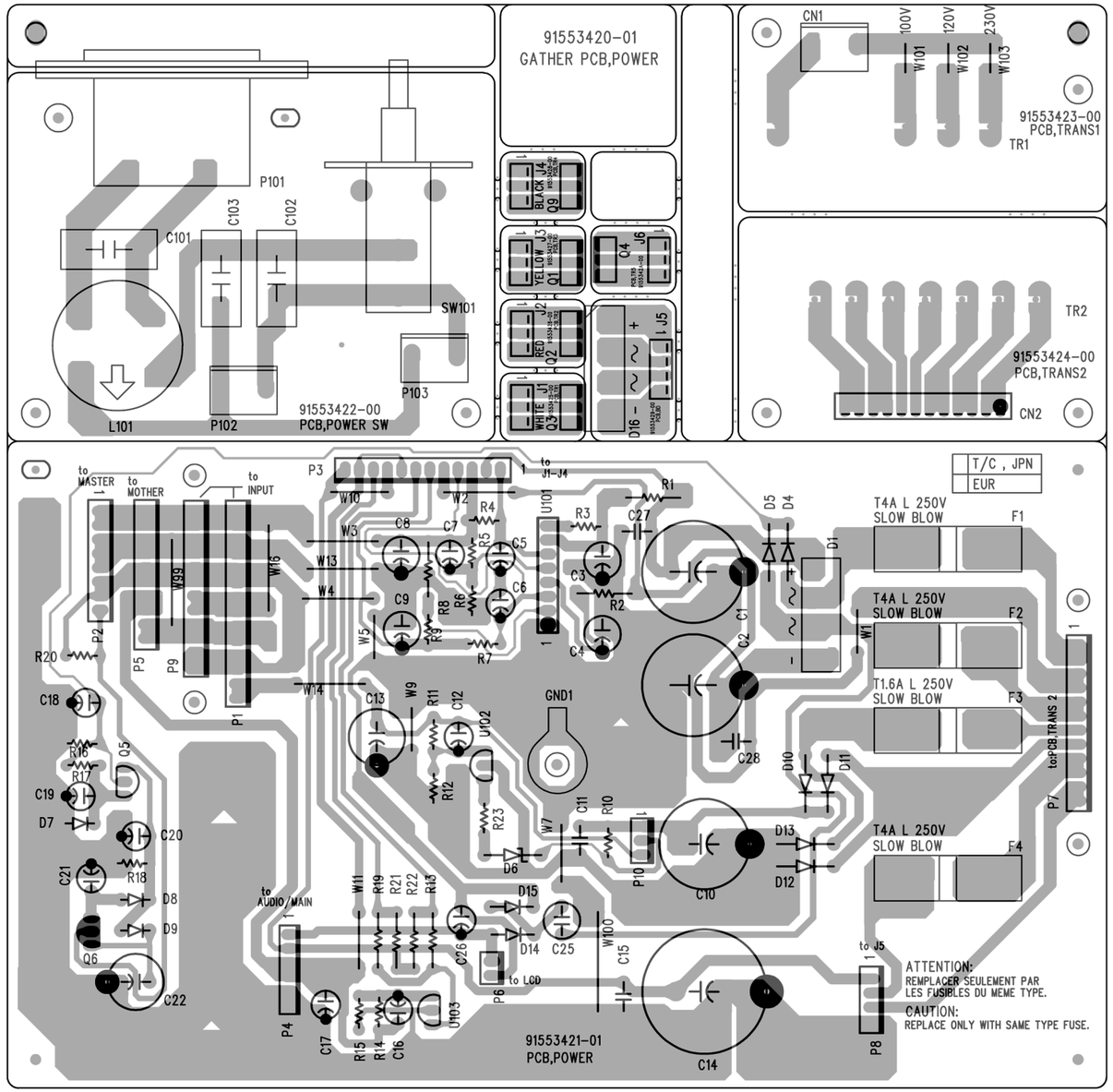


## GATHER PCB, INPUT (INPUT JACK PCB, MIC AMP PCB)

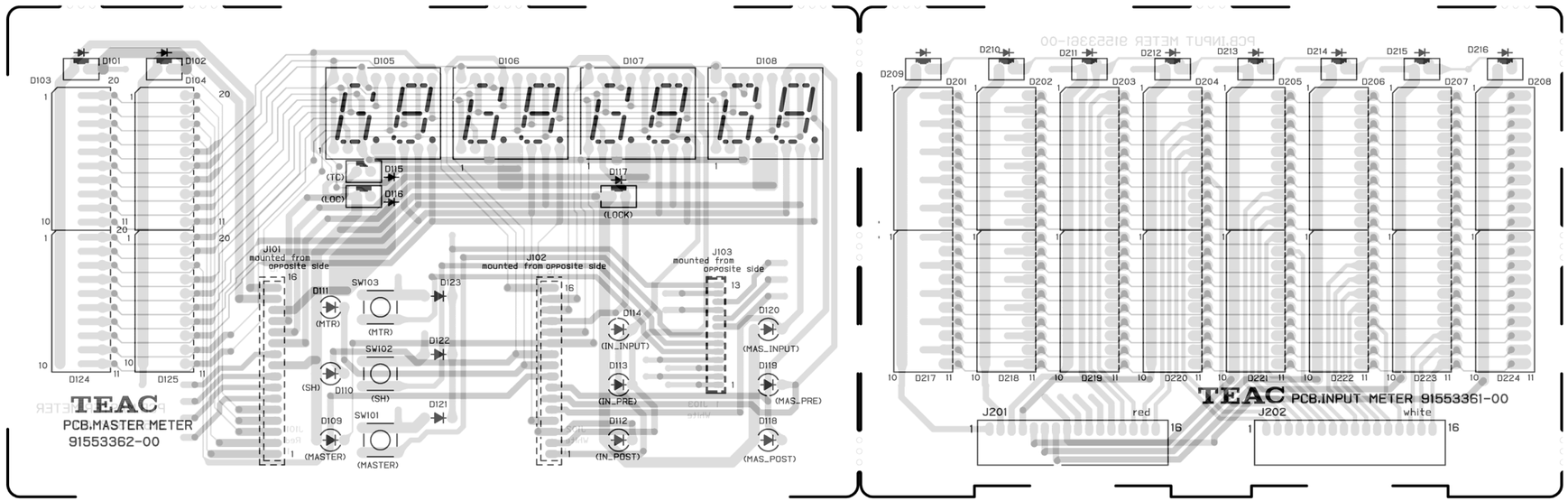


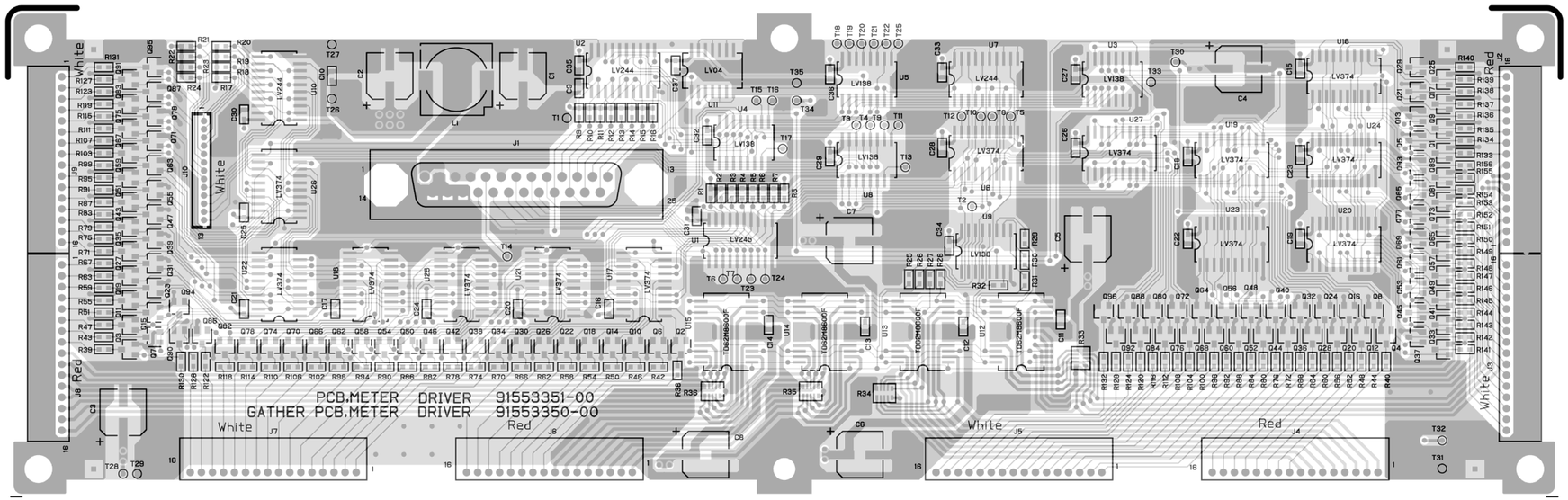
**GATHER PCB, POWER (POWER PCB, POWER SW PCB, TRANS1/2 PCB, TR1/2/3/4/5 PCB, BD PCB)**



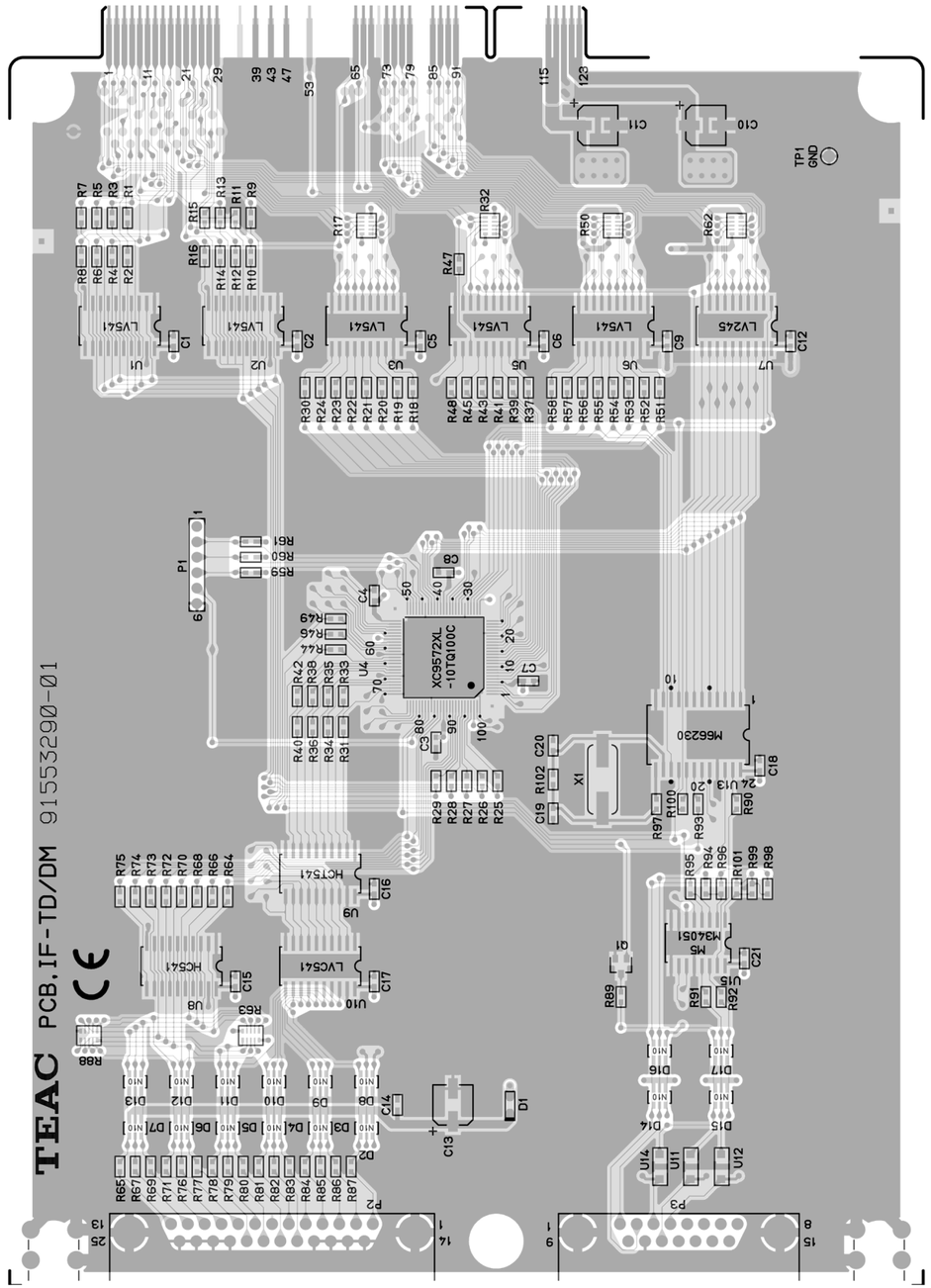
## GATHER PCB,METER BRIDGE (MASTER METER PCB, INPUT METER PCB) (OPTION)



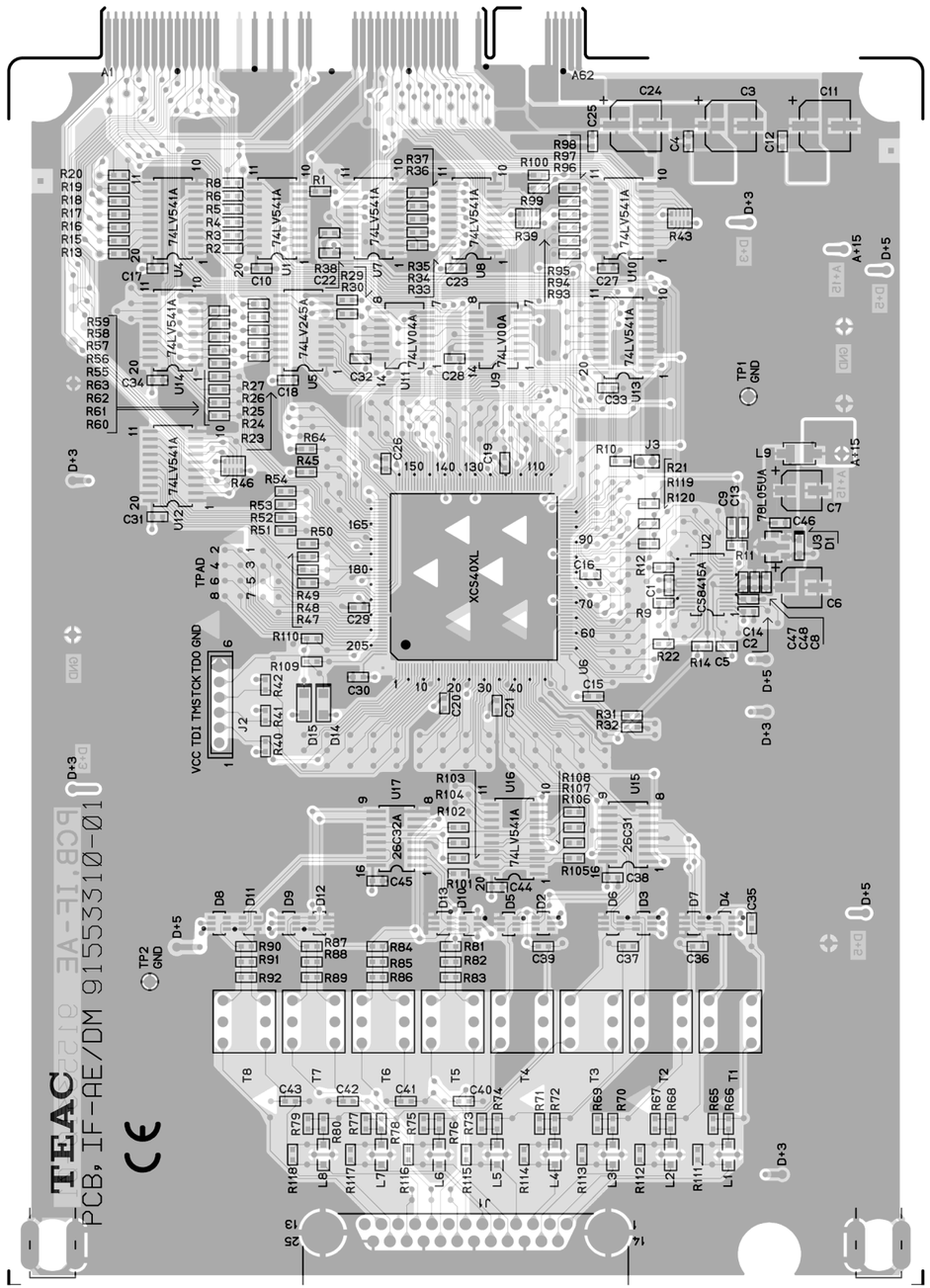

## METER DRIVER PCB (OPTION)



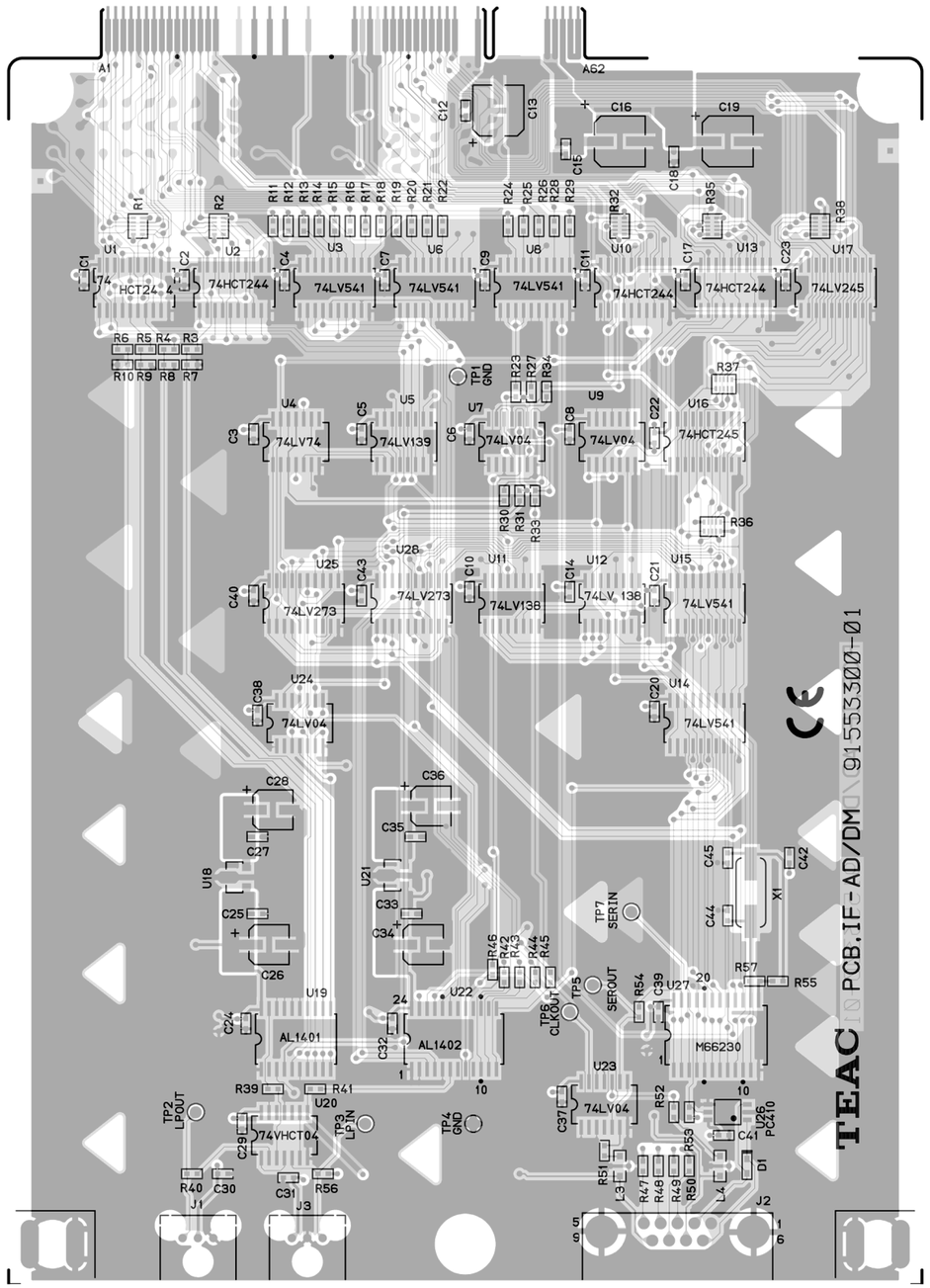
**IF-TD/DM PCB (OPTION)**



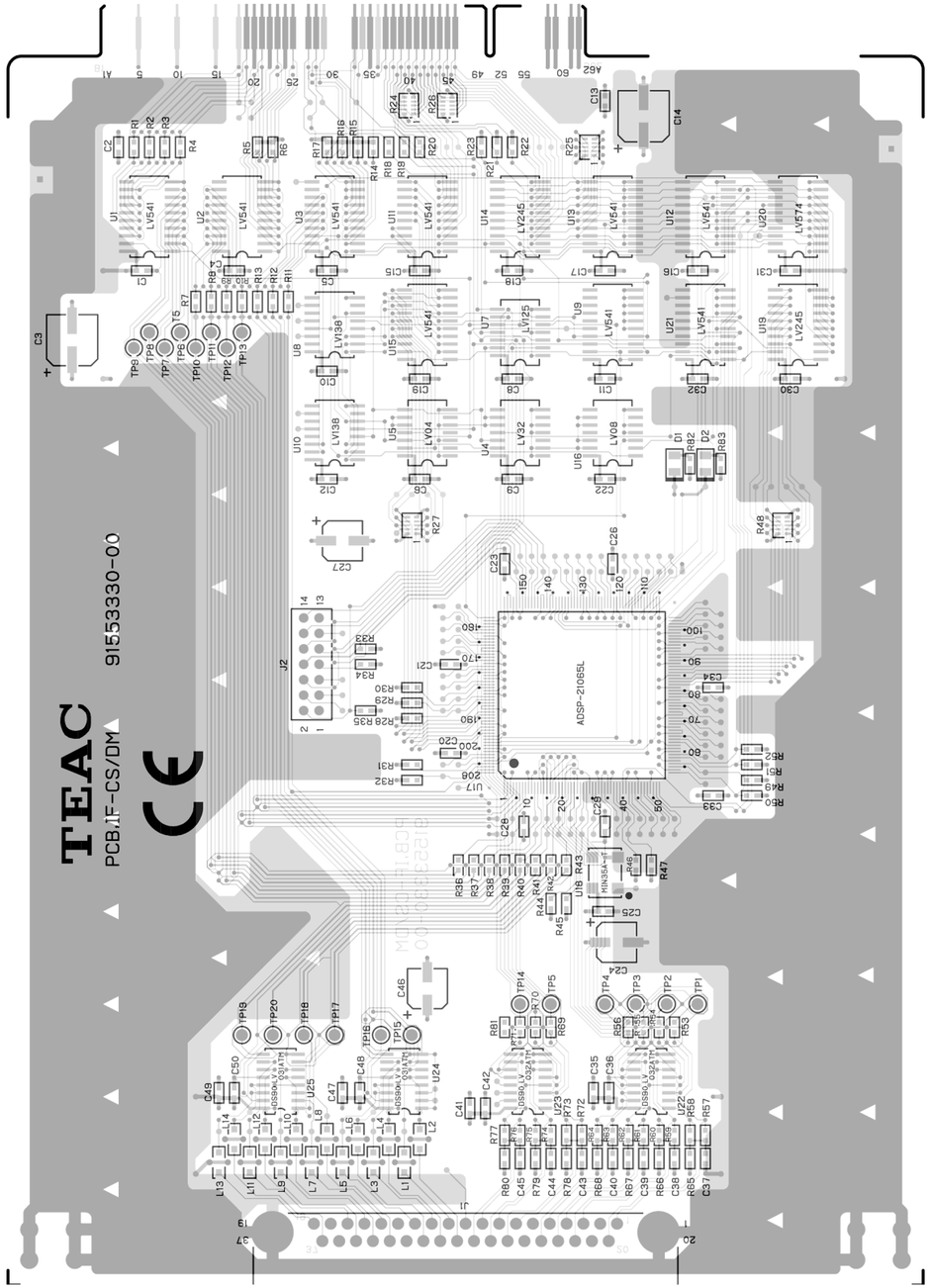

**IF-AE/DM PCB (OPTION)**



**IF-AD/DM PCB (OPTION)**

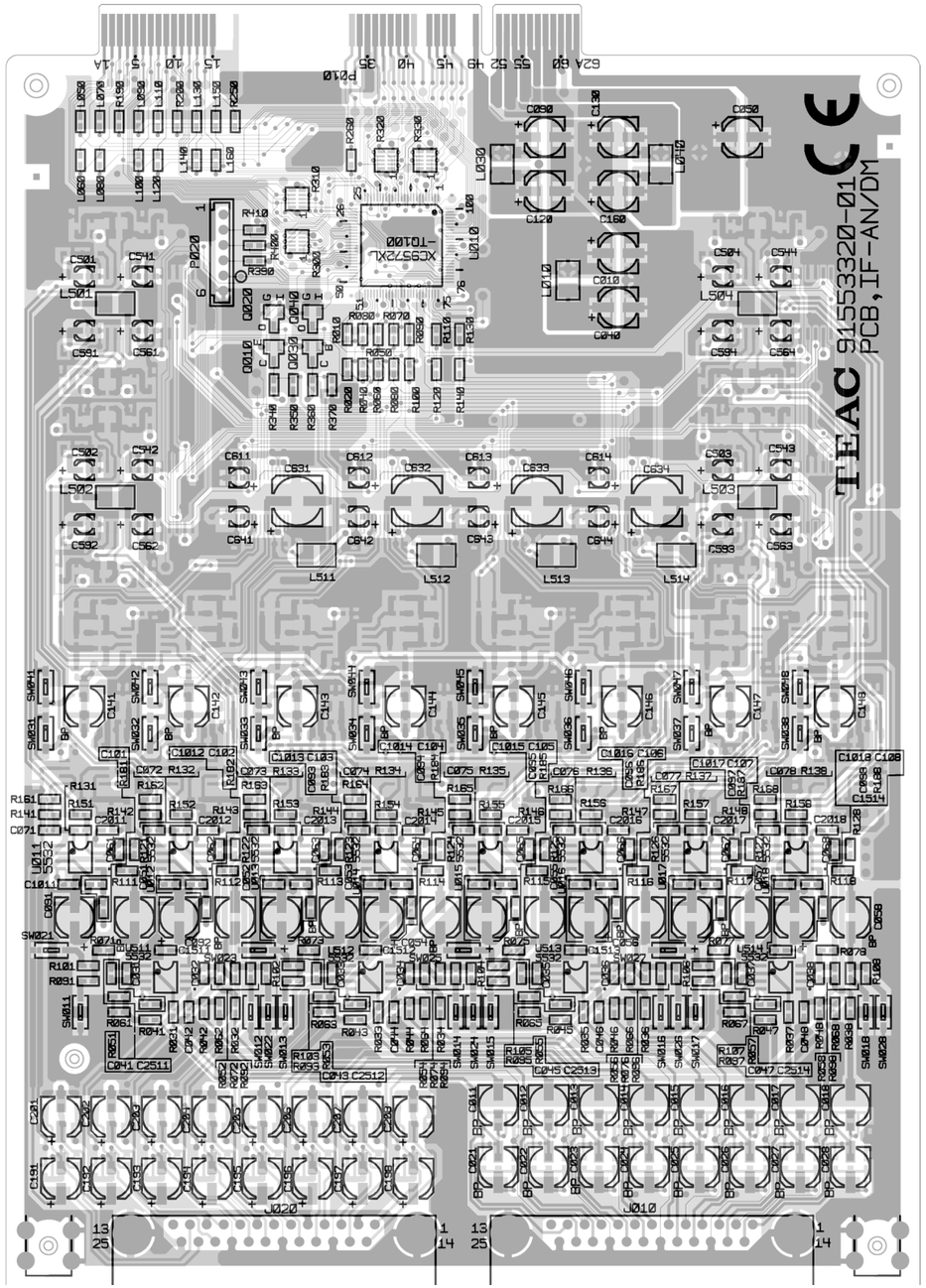



**IF-CS/DM PCB (OPTION)**



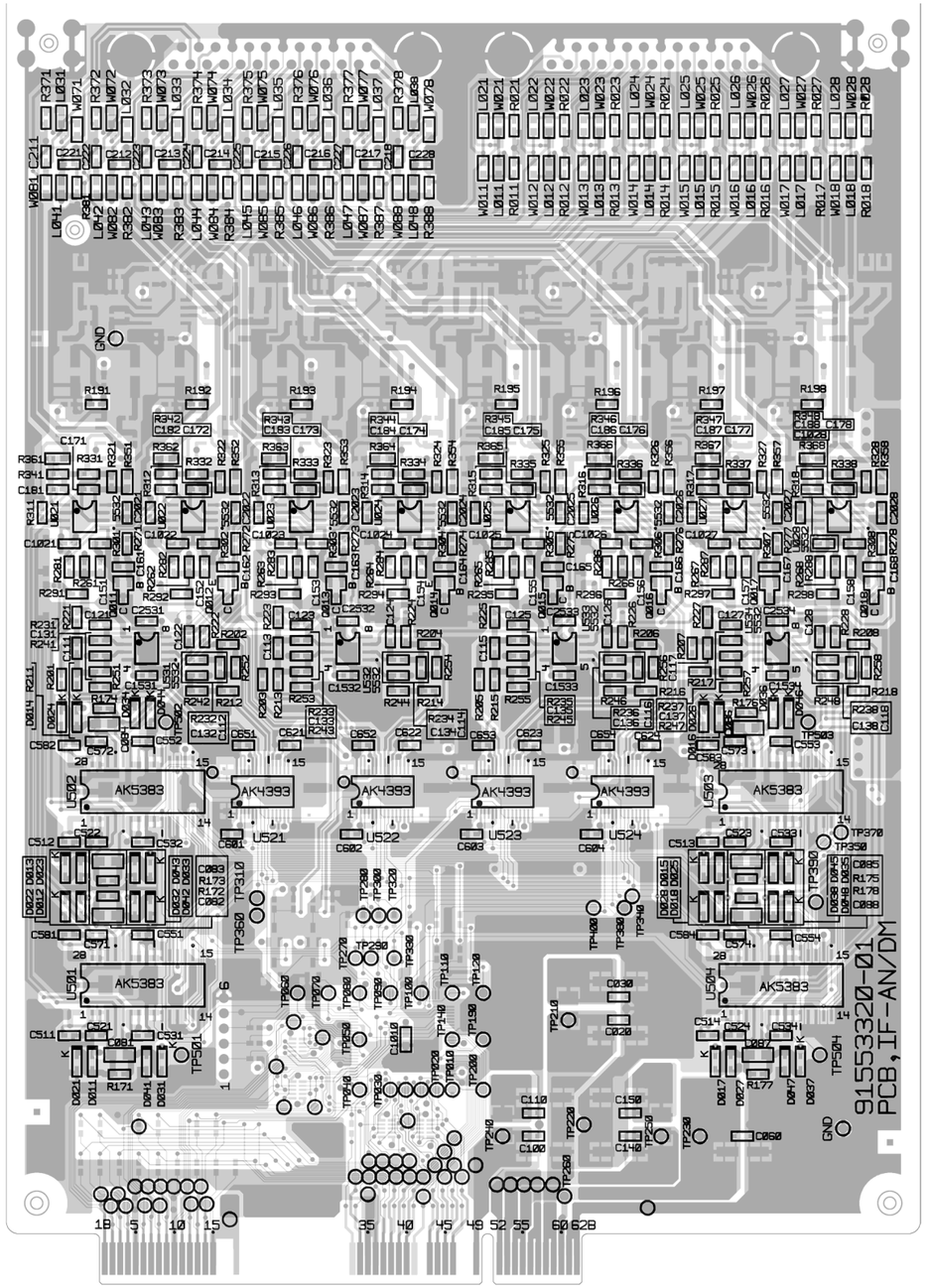
**IF-AN/DM PCB (OPTION)**

SIDE A




**IF-AN/DM PCB (OPTION)**

SIDE B



# 10. INCLUDED ACCESSORIES
付属品

## INCLUDED ACCESSORIES

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| | *9101439600 | OWNER'S MANUAL(JPNANESE) [J] | |
| | *9101439700 | OWNER'S MANUAL(ENGLISH) [EXCEPT J] | |

# PARTS LIST SECTION

## CONTENTS

EXPLODED VIEWS AND PARTS LIST ·····2
PC BOARDS AND PARTS LIST·····8
INCLUDED ACCESSORIES·····32

## 目次

分解図とパーツリスト ·····2
基板図とパーツリスト ·····8
付属品·····32

### NOTES

- PC boards shown are viewed from parts side.
- Parts marked with ∗ require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in the manual.
- ⚠Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J]: JAPAN [K]: KOREA [A]: AUSTRALIA [US/C]: U.S.A./CANADA
  [E]: EUROPE [UK]: U.K.

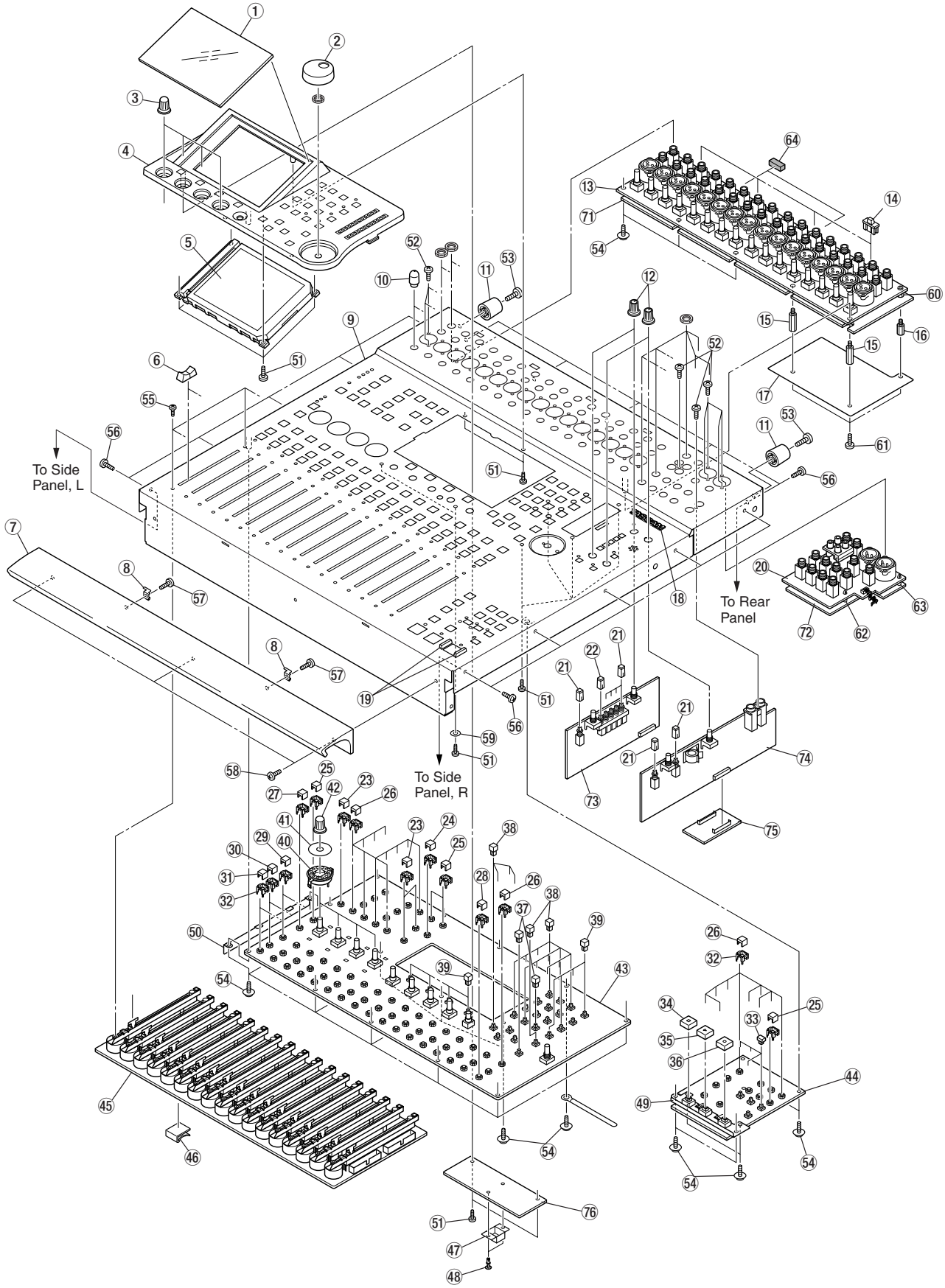
### 注 意

- プリント基板は部品面が示されています。
- ∗印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品及び品番のない部品は供給しません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠は安全重要部品です。
  交換する時は必ずティアック指定の部品を使用してください。
- 仕向先
  [J]: JAPAN [K]: KOREA [A]: AUSTRALIA [US/C]: U.S.A./CANADA
  [E]: EUROPE [UK]: U.K.

# EXPLODED VIEWS AND PARTS LIST

分解図とパーツリスト

## EXPLODED VIEW-1



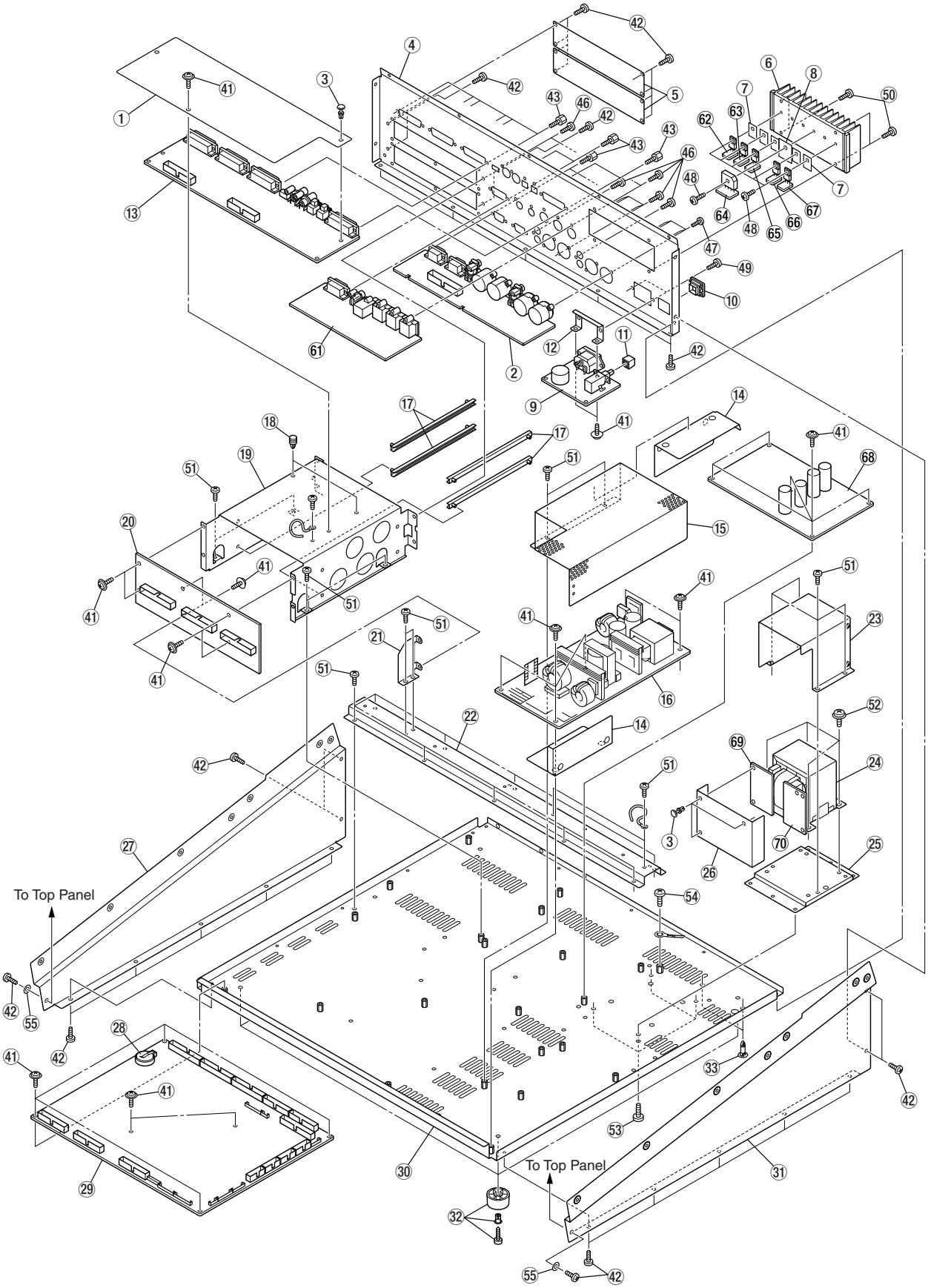
## EXPLODED VIEW-1

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| 1- 1 | 9260363101 | WINDOW,LCD | |
| 1- 2 | 9260385100 | KNOB,JOG N63 | |
| 1- 3 | M00630600C | KNOB,POD N61 | |
| 1- 4 | 9260361701 | ESCUTCHEON,LCD | |
| 1- 5 | 9174027100 | LCD,MG3224C3-SBF | |
| 1- 6 | 9260357800 | KNOB,S-VR NICKEL | |
| 1- 7 | 9260363201 | PAD,582 | |
| 1- 8 | *9260299600 | BRACKET,PAD | |
| 1- 9 | *9260364904 | TOP PANEL ASSY | |
| 1-10 | 9260368000 | KNOB,TRIM N61/N64 | |
| 1-11 | 9260354800 | FOOT,FFT-4 | |
| 1-12 | 5801631800 | KNOB,R-VR N61/N66 | |
| 1-13 | | INPUT JACK PCB ASSY ····· | GATHER PCB ASSY,INPUT (Refer to page 9) |
| 1-14 | M00006100A | KNOB,SLIDE GY | |
| 1-15 | *9783803025 | LOCK SCREW,M3X25X6 | |
| 1-16 | *9783803015 | LOCK SCREW,M3X15X6 | |
| 1-17 | *9260388600 | SHIELD COVER,INPUT | |
| 1-18 | 9260268802 | TASCAM BADGE | |
| 1-19 | M00207800A | ESCUTCHEON,GUARD | |
| 1-20 | | MASTER JACK PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 11) |
| 1-21 | 5801632501 | PUSH BUTTON COVER,WHT/N63 | |
| 1-22 | 9260306400 | PUSH BUTTON COVER,WHT/N61 | |
| 1-23 | 9260362701 | BUTTON,BLT-IN (WHT) | |
| 1-24 | 9260362601 | BUTTON,BLT-IN (R23) | |
| 1-25 | 9260362801 | BUTTON,BLT-IN (N64) | |
| 1-26 | 9260299302 | BUTTON,BLT-IN LED | |
| 1-27 | 9260362901 | BUTTON,BLT-IN (266C) | |
| 1-28 | 9260324702 | BUTTON,BLT-IN LED(SOLO) | |
| 1-29 | 9260351901 | BUTTON,BLT-IN LED(REC) | |
| 1-30 | 9260351701 | BUTTON,BLT-IN LED(SEL) | |
| 1-31 | 9260324502 | BUTTON,BLT-IN LED (MUTE) | |
| 1-32 | 9260299400 | BASE,BLT-IN LED | |
| 1-33 | M00630703A | BUTTON,6.4X8.4 266C | |
| 1-34 | 9260351300 | BUTTON,STOP | |
| 1-35 | 9260351400 | BUTTON,PLAY | |
| 1-36 | 9260351500 | BUTTON,REC | |
| 1-37 | 9260362000 | BUTTON,8X8 WHT | |
| 1-38 | 9260362100 | BUTTON,8X8 N62 | |
| 1-39 | 9260362200 | BUTTON,8X8 N64 | |
| 1-40 | 9260363300 | ESCUTCHEON RING | |
| 1-41 | 9260362301 | PLATE RING | |
| 1-42 | M00630601C | KNOB,POD N63 | |
| 1-43 | | PANEL PCB ASSY ····· | GATHER PCB ASSY,PANEL (Refer to page 11) |
| 1-44 | | TRANSPORT PCB ASSY ····· | GATHER PCB ASSY,TRANSPORT (Refer to page 12) |
| 1-45 | | FADER PCB ASSY ····· | GATHER PCB ASSY,FADER (Refer to page 10) |
| 1-46 | 9260367300 | WIRE CLAMP,FCC-20 | |
| 1-47 | 9260384700 | SHIELD COVER,LCD | |
| 1-48 | 9260385200 | PUSH RIVET,P3045 | |
| 1-49 | *9260363400 | BRACKET,TRANSPORT | |
| 1-50 | *9260388700 | BRACKET,PANEL | |

## EXPLODED VIEW-1

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| 1-51 | *9783602606 | SCREW,BTT-P M2.6X6 | |
| 1-52 | *9783613008 | SCREW,BTT-P M3X8 (BLK) | |
| 1-53 | *9780504010 | SCREW,BH M4X10 (BLK) | |
| 1-54 | *9783103006 | SCREW,CAP-S M3X6 | |
| 1-55 | *9783573004 | SCREW,WHIS BIND M3X4 (BLK) | |
| 1-56 | *9780503006 | SCREW,BH M3X6 (BLK) | |
| 1-57 | *9783213006 | SCREW,BTT-B M3X6 | |
| 1-58 | *9780503008 | SCREW,BH M3X8 (BLK) | |
| 1-59 | Vacant | | |
| 1-60 | *9260389100 | PCB SUPPORT,HP-8 | |
| 1-61 | *9780403006 | SCREW,BH M3X6 | |
| 1-62 | *9260356300 | SPACER SUPPORT,LCC-8 | |
| 1-63 | *9260355700 | SPACER SUPPORT,MC-8 | |
| 1-64 | *9260366700 | CUSHION,10X20X9 | |
| 1-71 | | MIC AMP PCB ····· | GATHER PCB ASSY,INPUT (Refer to page 9) |
| 1-72 | | MASTER AMP PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 11) |
| 1-73 | | C.ROOM PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 11) |
| 1-74 | | STUDIO PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 11) |
| 1-75 | | BUSS PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 11) |
| 1-76 | | LCD SUB PCB ASSY ····· | GATHER PCB ASSY,TRANSPORT (Refer to page 12) |

## EXPLODED VIEW-2



## EXPLODED VIEW-2

| REF.NO. | | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|---|
| 2- 1 | | *9260384901 | SHIELD SHEET,TDIF | |
| 2- 2 | | | DIGITAL I/O PCB ASSY ····· | GATHER PCB ASSY,MASTER (Refer to page 11) |
| 2- 3 | | 9260361500 | PUSH RIVET,SR3-5.5 | |
| 2- 4 | | *9260364401 | REAR PANEL | |
| 2- 5 | | *9260359300 | PANEL,SLOT | |
| 2- 6 | | *9260364502 | HEAT SINK | |
| 2- 7 | | 9260317800 | SI-INSULATOR,T-220 | |
| 2- 8 | | *9260232900 | SHEET,RADIATOR D | |
| 2- 9 | | | POWER SW PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |
| 2-10 | | 5801486601 | ESCUTCHEON D,P-N15-A | |
| 2-11 | | 5801503800 | BUTTON,EJECT P-N15-A | |
| 2-12 | | 9260320701 | BRACKET,PWRSW | |
| 2-13 | | | TDIF PCB ASSY ····· | GATHER PCB ASSY,TRANSPORT (Refer to page 12) |
| 2-14 | | *9260383300 | SHEET,SW REG | |
| 2-15 | | 9260364801 | COVER,SW REG | |
| 2-16 | | 9125146300 | SW-PWR,UPS220-1061-L [J,US/C] | |
| | | 9125146400 | SW-PWR,UPS220-1061-H [K,A,E,UK] | |
| 2-17 | | 9260356700 | CARD GUIDE,CG-600 | |
| 2-18 | | *9260364000 | PCB SUPPORT,DCB-5 | |
| 2-19 | | *9260363901 | BRACKET,SLOT | |
| 2-20 | | | MOTHER PCB ASSY ····· | GATHER PCB ASSY,MOTHER (Refer to page 13) |
| 2-21 | | *9260364301 | BRACKET,MOTHER PCB | |
| 2-22 | | 9260363701 | FRAME,BOTTOM | |
| 2-23 | | *9260384800 | SHIELD COVER,TRANS | |
| 2-24 | ⚠ | 9125145202 | POWER TRANSFORMER | |
| 2-25 | | *9260364101 | BRACKET,TRANS | |
| 2-26 | | *9260364201 | COVER,TRANS PCB | |
| 2-27 | | 9260364601 | SIDE PANEL,L | |
| 2-28 | | 9151003000 | BATTERY,CR2032 | |
| 2-29 | | | MAIN PCB ASSY ····· | GATHER PCB ASSY,MAIN (Refer to page 8) |
| 2-30 | | *9260363601 | CHASSIS,BOTTOM | |
| 2-31 | | 9260364701 | SIDE PANEL,R | |
| 2-32 | | 9260233100 | FOOT,FF015 | |
| 2-33 | | *9260366800 | PCB SUPPORT,RCC-12 | |
| 2-41 | | *9783103006 | SCREW,CAP-S M3X6 | |
| 2-42 | | 9780503006 | SCREW,BH M3X6 (BLK) | |
| 2-43 | | *9260330700 | D-SUB SCREW,HW-H118MN02 | |
| 2-44 | | Vacant | | |
| 2-45 | | Vacant | | |
| 2-46 | | *9783613008 | SCREW,BTT-P M3X8 (BLK) | |
| 2-47 | | *9783242608 | SCREW,BTT-B M2.6X8 (BLK) | |
| 2-48 | | *9783243012 | SCREW,BTT-B M3X12 (BLK) | |
| 2-49 | | *9783243008 | SCREW,BTT-B M3X8 (BLK) | |
| 2-50 | | *9780503010 | SCREW,BH M3X10 (BLK) | |
| 2-51 | | *9780403006 | SCREW,BH M3X6 | |
| 2-52 | | *9783294008 | SCREW,BTT-SSB M4X8 | |
| 2-53 | | *9780404008 | SCREW,BH M4X8 | |
| 2-54 | | *9780504008 | SCREW,BH M4X8 (BLK) | |

## EXPLODED VIEW-2

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| 2-61 | | MIDI PCB ASSY ····· | GATHER PCB ASSY,TRANSPORT (Refer to page 12) |
| 2-62 | | TR4 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |
| 2-63 | | TR3 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |
| 2-64 | | BD PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |
| 2-65 | | TR2 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |
| 2-66 | | TR1 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |
| 2-67 | | TR5 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |
| 2-68 | | POWER PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |
| 2-69 | | TRANS 2 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |
| 2-70 | | TRANS 1 PCB ASSY ····· | GATHER PCB ASSY,POWER (Refer to page 13) |

# PC BOARDS AND PARTS LIST

基板図とパーツリスト

## GATHER PCB ASSY, MAIN

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145316000 | GATHER PCB ASSY,MAIN |
| | | MAIN PCB |
| BT1 | 9260303900 | BATTERY HOLDER SN-2032-1 |
| D1,2 | 9165025030 | DIODE,BR751V-40/TE17 |
| D4-7 | 9165023530 | DIODE 1SS355 TE17 |
| D8 | 9165028930 | DIODE,HVC376B |
| D9-12 | 9165023530 | DIODE 1SS355 TE17 |
| D13-16 | 9174027430 | LED,KPK-3020NC(ORG) |
| L1 | 9173019830 | COIL,EBL2012-2R7K |
| L2-5 | 9173020830 | COIL,MLF2012E100MT |
| P1 | 9144521900 | CN,14FE-BT-VK-N |
| P2 | 9143180000 | CONNECTOR PLUG, 12P |
| P3 | 9144513000 | HEADER,2556P03UA00 |
| P4 | 9143242000 | PLUG 14P B14B-PH-K |
| P5 | 9143239000 | PLUG,11P B11B-PH-K |
| P6 | 9143241000 | PLUG 13P(B13B-PH-K) |
| P7 | 9144521000 | CN 3675P 34VUA0 |
| P8 | 9143232000 | PLUG B4B-PH 4P |
| P9,10 | 9144521000 | CN 3675P 34VUA0 |
| P11 | 9143174000 | PLUG 6P B6B-EH-A |
| P17,18 | 9144521000 | CN 3675P 34VUA0 |
| P20-22 | 9144510000 | CONNECTOR 3675P 40VUA0 |
| P23 | 9143232000 | PLUG B4B-PH 4P |
| P26,27 | 9144523700 | CN 3675P 16VUA0 |
| P29 | 9143174000 | PLUG 6P B6B-EH-A |
| P30 | 9143174000 | PLUG 6P B6B-EH-A |
| P31 | 9143240000 | CONNECTOR PLUG,B12B-PH-K |
| P32 | 9143240020 | CONNECTOR B12B-PH-K-R |
| P33 | 9143234000 | PLUG B6B-PH 6P |
| P34 | 9143174000 | PLUG 6P B6B-EH-A |
| P35 | 9144521000 | CN 3675P 34VUA0 |
| P36,37 | 9144523700 | CN 3675P 16VUA0 |
| Q1 | 9163018030 | TR,2SA1586Y |
| Q2,4 | 9163018530 | DTR,DTA124EU |
| Q3,5 | 9163018630 | DTR,DTC124EU |
| RA1-4 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA5,9 | 9111287030 | R,ARRAY FCA340 103J |
| RA6-8 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA10-13 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA14,17 | 9111287030 | R,ARRAY FCA340 103J |
| RA15,16 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA18,22 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA23,29 | 9111287030 | R,ARRAY FCA340 103J |
| RA24-28 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA30,31 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA32,63 | 9111287030 | R,ARRAY FCA340 103J |
| RA33,34 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA35-37 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |
| RA38,39 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA40,41 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |
| RA42,43 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA44,45 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |

## GATHER PCB ASSY, MAIN

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| RA46-49 | 9111281030 | R,ARRAY 10KX8 FCA350 CHIP |
| RA50-53 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |
| RA60,61 | 9111303030 | R,ARRAY 47KX8 YC-15J CHIP |
| RA62 | 9111287030 | R,ARRAY FCA340 103J |
| U1 | 9167075430 | IC,HD74LV273AFPEL |
| U2 | 5220049400 | IC,UPD65013 |
| U3 | 9167039930 | IC,M62006FP |
| U4 | 9167077130 | IC,HD29051FP |
| U5 | 9167075030 | IC,HD74LV04AFPEL |
| U6,7 | S0035153 | IC,MBM29F800BA-70PF |
| U6,7 | E0033093 | SOCKET,44PIN SOP IC179 |
| U8 | 9167073230 | IC,BS62LV256TC-70 |
| U9 | 9167041730 | IC,TC74VHC00F (14P) |
| U10 | 9167074630 | IC,T2316162A-60S |
| U11 | 9167064430 | IC,CPU HD6417014R |
| U12 | 9167074930 | IC,HD74LV00AFPEL |
| U13,14 | 9167074730 | IC,T14L256A-15P |
| U15,16 | 9167067730 | IC,HD74LV245AFPEL |
| U17,18 | 9167055830 | IC,HD74LV541AFPEL |
| U19-21 | 9167075330 | IC,HD74LV139AFPEL |
| U22,25 | 9167075230 | IC,HD74LV138AFPEL |
| U23,24 | 9167075430 | IC,HD74LV273AFPEL |
| U26 | 9167075330 | IC,HD74LV139AFPEL |
| U27 | 9167066230 | IC,HD74LV125AFPEL |
| U28 | 9167065330 | IC,IDT7130SA55J |
| U29 | 9167067730 | IC,HD74LV245AFPEL |
| U30 | 9167055830 | IC,HD74LV541AFPEL |
| U31 | S0035153 | IC,MBM29F800BA-70PF |
| U31 | E0033093 | SOCKET,44PIN SOP IC179 |
| U32 | 9167074630 | IC,T2316162A-60S |
| U33 | 9167064430 | IC,CPU HD6417014R |
| U34 | 9167075430 | IC,HD74LV273AFPEL |
| U35 | 9167075330 | IC,HD74LV139AFPEL |
| U36 | 9167066330 | IC,HD74LV32AFPEL |
| U37 | 9167067730 | IC,HD74LV245AFPEL |
| U38,39 | 9167066330 | IC,HD74LV32AFPEL |
| U40 | 9167048230 | IC,HD64646FS |
| U41-44 | 9167049430 | IC,HD74LV157FPEL(16P) |
| U45 | 9167067730 | IC,HD74LV245AFPEL |
| U46 | 9167073230 | IC,BS62LV256TC-70 |
| U47 | 9167048730 | IC,HD74LV02FPEL |
| U48-53 | 9167055830 | IC,HD74LV541AFPEL |
| U54 | 9167067730 | IC,HD74LV245AFPEL |
| U55-57 | 9167052930 | IC,HD74LVC240FPEL |
| U58-61 | 9167054230 | IC,HD74HC540FPEL(20P) |
| U62-67 | 9167055830 | IC,HD74LV541AFPEL |
| U68 | 9167075330 | IC,HD74LV139AFPEL |
| U69 | 9167055830 | IC,HD74LV541AFPEL |
| U70 | 9167075430 | IC,HD74LV273AFPEL |
| U71-73 | S00190600A | IC, IOX |

## GATHER PCB ASSY, MAIN

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| U74-76 | 9167067730 | IC,HD74LV245AFPEL |
| U77,78 | S0038953 | IC,ADSP-21065L |
| U79 | 9167041630 | IC,TC74VHCU04F (14P) |
| U80 | 9167064330 | IC,HD74LVC541AFPEL(20P) |
| U81 | 9167074930 | IC,HD74LV00AFPEL |
| U82,83 | 9167055830 | IC,HD74LV541AFPEL |
| U84,85 | 9167067730 | IC,HD74LV245AFPEL |
| U86 | 9167049430 | IC,HD74LV157FPEL(16P) |
| U87,88 | S0038953 | IC,ADSP-21065L |
| U89,98 | 9167074930 | IC,HD74LV00AFPEL |
| U90,91 | 9167055830 | IC,HD74LV541AFPEL |
| U92,93 | 9167067730 | IC,HD74LV245AFPEL |
| U94,95 | S0038953 | IC,ADSP-21065L |
| U96,97 | 9167074030 | IC,T431616A-8S |
| U99,100 | 9167055830 | IC,HD74LV541AFPEL |
| U101,102 | 9167067730 | IC,HD74LV245AFPEL |
| U103 | 9167066230 | IC,HD74LV125AFPEL |
| U104 | 9167049430 | IC,HD74LV157FPEL(16P) |
| U105 | S0043543 | IC,XC9572X2-10 TQ100 |
| U106 | S0038953 | IC,ADSP-21065L |
| U107 | 9167069030 | IC,HD74LVCH16543 |
| U108 | 9167069130 | IC,HD74LV574AFPEL |
| U109-112 | 9167068630 | IC,T14L102N-12J(32P) |
| U120 | 9167066730 | IC,AL1402 |
| U121 | 9167066630 | IC,AL1401A |
| U122-124 | 9167075430 | IC,HD74LV273AFPEL |
| U125 | S0043533 | IC,XC9536X2-10 VQ64 |
| U126,127 | 9167055830 | IC,HD74LV541AFPEL |
| U128 | 9167075730 | IC,HD74LV540AFPEL |
| U129 | 9167055830 | IC,HD74LV541AFPEL |
| U130,131 | 9167049430 | IC,HD74LV157FPEL(16P) |
| U132 | 9167081230 | IC,HD74LV14AFPEL |
| U133 | 9167041630 | IC,TC74VHCU04F (14P) |
| U134 | 9167051030 | IC,NJM78L05UA-TE1(3P) |
| U135 | 9167068030 | IC,MC74HC4046ADR2(16P) |
| U136 | 9167070630 | IC,TC74VHCT00AF |
| U137 | 9167075430 | IC,HD74LV273AFPEL |
| U138 | 9167077130 | IC,HD29051FP |
| U139 | 9167041630 | IC,TC74VHCU04F (14P) |
| U140 | 9167048730 | IC,HD74LV02FPEL |
| U141 | 9167075130 | IC,HD74LV74AFPEL |
| U143,144 | 9167064930 | IC,CS8420 |
| U145 | 9167065430 | IC,HD74LV244AFPEL |
| U146 | 9167051030 | IC,NJM78L05UA-TE1(3P) |
| U147 | 9167075130 | IC,HD74LV74AFPEL |
| U148-155 | 9167064530 | IC,AK5383VS-E2 |
| U156-158 | 9167064730 | IC,AK4527VQ |
| U159 | 9167064630 | IC,AK5353VT-E2 |
| U160 | S0043533 | IC,XC9536X2-10 VQ64 |
| U161-163 | 9167048330 | IC,HD74HC4052FPEL |
| U164 | 9167074830 | IC,NJM79L24UA-TE1 |
| U165 | 9167075030 | IC,HD74LV04AFPEL |
| X1 | 9173016430 | OSC,MIN95A-T 7.056MHZ |
| X2 | 9173019730 | XTAL,LIM-C 30MHZ |

## GATHER PCB ASSY, INPUT

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145313000 | GATHER PCB ASSY,INPUT |
| | | PCB,INPUT JACK |
| | | PCB,MIC AMP |
| D13,14 | 9165022150 | DIODE TP 1SS133T |
| D23,24 | 9165022150 | DIODE TP 1SS133T |
| D33,34 | 9165022150 | DIODE TP 1SS133T |
| D43,44 | 9165022150 | DIODE TP 1SS133T |
| D53,54 | 9165022150 | DIODE TP 1SS133T |
| D63,64 | 9165022150 | DIODE TP 1SS133T |
| D73,74 | 9165022150 | DIODE TP 1SS133T |
| D83,84 | 9165022150 | DIODE TP 1SS133T |
| D93,94 | 9165022150 | DIODE TP 1SS133T |
| D103,104 | 9165022150 | DIODE TP 1SS133T |
| D113,114 | 9165022150 | DIODE TP 1SS133T |
| D123,124 | 9165022150 | DIODE TP 1SS133T |
| D133,134 | 9165022150 | DIODE TP 1SS133T |
| D143,144 | 9165022150 | DIODE TP 1SS133T |
| D153,154 | 9165022150 | DIODE TP 1SS133T |
| D163,164 | 9165022150 | DIODE TP 1SS133T |
| J1-16 | 9144277001 | MIC JACK NC3FAV-0 |
| J101-116 | 9144271001 | PHONE JACK JY-6353-02-030 |
| J201-216 | 9144272001 | PHONE JACK JY-6353-02-040 |
| P1-8 | 9144523800 | CABLE BOTTON,51048-1510 |
| P11-18 | 9144523800 | CABLE BOTTON,51048-1510 |
| P101-104 | 9144523700 | CN 3675P 16VUA0 |
| P901-904 | 9143174000 | PLUG 6P B6B-EH-A |
| P905 | 9143170000 | CONNECTOR PLUG, 2P |
| Q11,12 | 9163021320 | TR,2SA1048GR |
| Q13,14 | S0039452 | TR,2SA1084E |
| Q15,16 | 9163019420 | TR,2SC5395-T12-F |
| Q21,22 | 9163021320 | TR,2SA1048GR |
| Q23,24 | S0039452 | TR,2SA1084E |
| Q25,26 | 9163019420 | TR,2SC5395-T12-F |
| Q31,32 | 9163021320 | TR,2SA1048GR |
| Q33,34 | S0039452 | TR,2SA1084E |
| Q35,36 | 9163019420 | TR,2SC5395-T12-F |
| Q41,42 | 9163021320 | TR,2SA1048GR |
| Q43,44 | S0039452 | TR,2SA1084E |
| Q45,46 | 9163019420 | TR,2SC5395-T12-F |
| Q51,52 | 9163021320 | TR,2SA1048GR |
| Q53,54 | S0039452 | TR,2SA1084E |
| Q55,56 | 9163019420 | TR,2SC5395-T12-F |
| Q61,62 | 9163021320 | TR,2SA1048GR |
| Q63,64 | S0039452 | TR,2SA1084E |
| Q65,66 | 9163019420 | TR,2SC5395-T12-F |
| Q71,72 | 9163021320 | TR,2SA1048GR |
| Q73,74 | S0039452 | TR,2SA1084E |
| Q75,76 | 9163019420 | TR,2SC5395-T12-F |
| Q81,82 | 9163021320 | TR,2SA1048GR |
| Q83,84 | S0039452 | TR,2SA1084E |
| Q85,86 | 9163019420 | TR,2SC5395-T12-F |
| Q91,92 | 9163021320 | TR,2SA1048GR |
| Q93,94 | S0039452 | TR,2SA1084E |

## GATHER PCB ASSY, INPUT

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| Q95,96 | 9163019420 | TR,2SC5395-T12-F |
| Q101,102 | 9163021320 | TR,2SA1048GR |
| Q103,104 | S0039452 | TR,2SA1084E |
| Q105,106 | 9163019420 | TR,2SC5395-T12-F |
| Q111,112 | 9163021320 | TR,2SA1048GR |
| Q113,114 | S0039452 | TR,2SA1084E |
| Q115,116 | 9163019420 | TR,2SC5395-T12-F |
| Q121,122 | 9163021320 | TR,2SA1048GR |
| Q123,124 | S0039452 | TR,2SA1084E |
| Q125,126 | 9163019420 | TR,2SC5395-T12-F |
| Q131,132 | 9163021320 | TR,2SA1048GR |
| Q133,134 | S0039452 | TR,2SA1084E |
| Q135,136 | 9163019420 | TR,2SC5395-T12-F |
| Q141,142 | 9163021320 | TR,2SA1048GR |
| Q143,144 | S0039452 | TR,2SA1084E |
| Q145,146 | 9163019420 | TR,2SC5395-T12-F |
| Q151,152 | 9163021320 | TR,2SA1048GR |
| Q153,154 | S0039452 | TR,2SA1084E |
| Q155,156 | 9163019420 | TR,2SC5395-T12-F |
| Q161,162 | 9163021320 | TR,2SA1048GR |
| Q163,164 | S0039452 | TR,2SA1084E |
| Q165,166 | 9163019420 | TR,2SC5395-T12-F |
| R21,71 | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R121,171 | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R221,271 | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R321,371 | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R421,471 | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R521,571 | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R621,671 | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| R721,771 | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| S1-4 | 9135036300 | SLIDE SW,SSSU042NA2-TK |
| U1-32 | 9167025200 | IC,BA15532N |
| VR1-16 | 9172038900 | VR,20KZD EVUF2LFL3 24D |

## GATHER PCB ASSY, FADER

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145314000 | GATHER PCBA,FADER<br>PCB,FADER |
| D101-103 | 9165023530 | DIODE,1SS355 TE17 |
| D151-153 | 9165023530 | DIODE,1SS355 TE17 |
| D201-203 | 9165023530 | DIODE,1SS355 TE17 |
| D251-253 | 9165023530 | DIODE,1SS355 TE17 |
| D301-303 | 9165023530 | DIODE,1SS355 TE17 |
| D351-353 | 9165023530 | DIODE,1SS355 TE17 |
| D401-403 | 9165023530 | DIODE,1SS355 TE17 |
| D451-453 | 9165023530 | DIODE,1SS355 TE17 |
| D501-503 | 9165023530 | DIODE,1SS355 TE17 |
| D551-553 | 9165023530 | DIODE,1SS355 TE17 |

## GATHER PCB ASSY, FADER

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| D601-603 | 9165023530 | DIODE,1SS355 TE17 |
| D651-653 | 9165023530 | DIODE,1SS355 TE17 |
| D701-703 | 9165023530 | DIODE,1SS355 TE17 |
| D751-753 | 9165023530 | DIODE,1SS355 TE17 |
| D801-803 | 9165023530 | DIODE,1SS355 TE17 |
| D851-853 | 9165023530 | DIODE,1SS355 TE17 |
| D901-903 | 9165023530 | DIODE,1SS355 TE17 |
| MF101-901 | R00979400A | VAR RES,5KB T-SENSE |
| MF151-851 | R00979400A | VAR RES,5KB T-SENSE |
| L1,2 | 9173020730 | COIL,BLM41P750SPT |
| P1 | 9144521000 | CN 3675P 34VUA0 |
| P2 | 9144521000 | CN 3675P 34VUA0 |
| P3 | 9143179000 | CONNECTOR PLUG,B11B-EH-A |
| R3 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R4 | 9111300030 | RA,GUS-QS009-01-1002-G |
| U1 | 9167051030 | IC,NJM78L05UA-TE1(3P) |
| U2 | 9167073330 | IC,NJM79L05UA-TE1 |
| U3 | 9167073430 | IC,NJM78L06UA-TE1 |
| U4 | 9167045830 | IC,HD74HC541FPV |
| U5,6 | 9167071330 | IC,TC74HC138AF |
| U7,8 | S0044474 | IC,HD74LV273AFPEL |
| U9 | S0044514 | IC,HD74LV574AFPEL |
| U10 | S0044474 | IC,HD74LV273AFPEL |
| U11,12 | S0044474 | IC,HD74LV273AFPEL |
| U13-15 | 9167045830 | IC,HD74HC541FPV |
| U16-18 | 9167071430 | IC,TC74HC4051AF |
| U101,201 | 9167055330 | IC NJM4565M(8P)-TE1 |
| U102,402 | 9167032800 | LOGIC IC,TC74HC14AF |
| U103,303 | 9167071230 | IC,TC74HC86AF |
| U104,154 | S0031454 | IC,M56783FP |
| U204,254 | S0031454 | IC,M56783FP |
| U301,401 | 9167055330 | IC NJM4565M(8P)-TE1 |
| U304,354 | S0031454 | IC,M56783FP |
| U404,454 | S0031454 | IC,M56783FP |
| U501,601 | 9167055330 | IC NJM4565M(8P)-TE1 |
| U503,703 | 9167071230 | IC,TC74HC86AF |
| U504,554 | S0031454 | IC,M56783FP |
| U604,654 | S0031454 | IC,M56783FP |
| U701,801 | 9167055330 | IC NJM4565M(8P)-TE1 |
| U702 | 9167032800 | LOGIC IC,TC74HC14AF |
| U704,754 | S0031454 | IC,M56783FP |
| U804,854 | S0031454 | IC,M56783FP |
| U901 | 9167055330 | IC NJM4565M(8P)-TE1 |
| U903 | 9167071230 | IC,TC74HC86AF |
| U904 | S0031454 | IC,M56783FP |

## GATHER PCB ASSY, PANEL

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145315000 | GATHER PCBA,PANEL |
| | | PANEL PCB |
| | 9260363300 | ESCUTCHEON RING |
| CN1 | 9107142100 | FLAT CABLE ASSY A |
| CN3 | 9107140600 | CABLE ASSY H |
| CN4 | 9107140700 | CABLE ASSY I |
| CN5 | 9107140800 | CABLE ASSY J |
| D1-11 | 9174028520 | LED,LA12540/TBF-4(ORG) |
| D12,28 | 9174028620 | LED,LI12540/TBF-4(RED) |
| D13-27 | 9174028520 | LED,LA12540/TBF-4(ORG) |
| D29 | 9174028520 | LED,LA12540/TBF-4(ORG) |
| D30,31 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D32 | 9174027520 | LED,SLR-332VR T32(RED) |
| D33 -36 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D37 | 9174027720 | LED,SLR-332MG T32(GRN) |
| D38-40 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D41-48 | 9174028720 | LED,LA12540/TBF-2(ORG) |
| D101-108 | 9165022150 | DIODE,TP 1SS133T |
| D111-118 | 9165022150 | DIODE,TP 1SS133T |
| D121-128 | 9165022150 | DIODE,TP 1SS133T |
| D131-138 | 9165022150 | DIODE,TP 1SS133T |
| D141-148 | 9165022150 | DIODE,TP 1SS133T |
| D151-158 | 9165022150 | DIODE,TP 1SS133T |
| D161-168 | 9165022150 | DIODE,TP 1SS133T |
| D171-172 | 9165022150 | DIODE,TP 1SS133T |
| D175-178 | 9165022150 | DIODE,TP 1SS133T |
| D221-229 | 9174028820 | LED,LI12540/TBF-2(RED) |
| D231-238 | 9174028820 | LED,LI12540/TBF-2(RED) |
| D241-248 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D249 | 9174027720 | LED,SLR-332MG T32(GRN) |
| D251-258 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D261-269 | 9174027720 | LED,SLR-332MG T32(GRN) |
| D271-278 | 9174027720 | LED,SLR-332MG T32(GRN) |
| D281-289 | 9174027520 | LED,SLR-332VR T32(RED) |
| D291-298 | 9174027520 | LED,SLR-332VR T32(RED) |
| D301-308 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D311-318 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D321-328 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D331-338 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D346-348 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D356-358 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D366-368 | 9174027620 | LED,SLR-332DU T32(ORG) |
| D376-378 | 9174027620 | LED,SLR-332DU T32(ORG) |
| Q101-116 | 9163018420 | DTR,DTC123ES |
| Q117-125 | 9163019020 | TR,2SB1237R |
| SW1-16 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW17-33 | 9136002000 | TACT SW SKHHDA |
| SW34 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW35-42 | 9172039800 | ENCODER,EC12E24204F25 |
| SW43 | 9172040200 | ENCODER,EC12E2420802 |
| SW101-108 | 9136003020 | TACT SW,EVQ11L H=5 TP |

## GATHER PCB ASSY, PANEL

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| SW111-118 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW121-128 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW131-138 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW141-148 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW151-158 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW161-166 | 9136002000 | TACT SW,SKHHDA |
| SW167 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW168 | 9136002000 | TACT SW,SKHHDA |
| SW171-172 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW175 | 9136002000 | TACT SW,SKHHDA |
| SW176 | 9136002000 | TACT SW,SKHHDA |
| SW177-178 | 9136003020 | TACT SW,EVQ11L H=5 TP |
| U1,2 | 9167026400 | IC,TC74HC138AP |
| U3 | 9167029400 | IC,TC74HC00AP (14P) |
| U4-11 | 9167037200 | IC TC74HC541AP(20P) |
| U12-19 | 9167067500 | IC,HD74LS374P |
| U20 | 9167075600 | IC,HD74HC574P |
| U21 | 9167026400 | IC,TC74HC138AP |
| U22 | 9167067600 | IC,HD74LS138P |
| VR1 | 9172036300 | VR,RK09K113Z401-10KB |

## GATHER PCB ASSY,MASTER

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | *9145318000 | GATHER PCB ASSY,MASTER |
| | | MASTER JACK PCB |
| | | MASTER AMP PCB |
| | | STUDIO PCB |
| | | C.ROOM PCB |
| | | BUSS PCB |
| | | DIGITAL I/O PCB |
| | 9107143900 | CABLE ASSY V |
| | 9260366900 | WIRE CLAMP,WLD-50T |
| D1,4 | 9174020200 | 3 LED (RED) L-341D |
| D2 | 9174022700 | LED L-34AD |
| D3 | 9174022700 | LED L-34AD |
| D901,902 | 9165022150 | DIODE TP 1SS133T |
| J1 | 9143385010 | CPJ-066-005 |
| J2 | 9144269100 | 4P B402A-B R/W |
| J101,201 | 9144520200 | PHONE JACK,JY-6353-02-250 |
| J102,202 | 9144271001 | PHONE JACK JY-6353-02-030 |
| J103,203 | 9144272001 | PHONE JACK JY-6353-02-040 |
| J104,204 | 9144487000 | MIC JACK NC3MAV |
| J105,205 | 9144271001 | PHONE JACK JY-6353-02-030 |
| J301,401 | 9144520200 | PHONE JACK,JY-6353-02-250 |
| J302,402 | 9144271001 | PHONE JACK JY-6353-02-030 |
| J901,902 | 9144438000 | MIC JACK NC3FAH1-0 (XLR) |
| J903,904 | 9144522100 | 2RCA HSP-242 V2-23 |
| J905,906 | 9144000200 | MIC JACK NC3MBH(XLR) |
| P101 | 9107140000 | CABLE ASSY A |
| P102 | 9143999000 | CN,TUC-P14X-B1 |

## GATHER PCB ASSY,MASTER

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| P103 | | 9107140100 | CABLE ASSY B |
| P104 | | 9107140200 | CABLE ASSY C |
| P105 | | 9107140300 | CABLE ASSY D |
| P106 | | 9107140400 | CABLE ASSY E |
| P107 | | 9143172000 | PLUG CONNECTOR B4B-EH-A |
| P108 | | 9143178000 | CONNECTOR PLUG 10P |
| P109 | | 9144523900 | CN,TWG-P7P-A1 |
| P110 | | 9107141100 | CABLE ASSY M |
| P111 | | 9107140900 | CABLE ASSY K |
| P112 | | 9144524000 | CN,TWG-P7X-A1 |
| P113 | | 9143170000 | CONNECTOR PLUG, 2P |
| P114 | | 9143999000 | CN,TUC-P14X-B1 |
| P115 | | 9107141200 | CABLE ASSY N |
| P122,123 | | 9144043000 | CN,TUC-P14P-B1 |
| P901 | | 9144521000 | CN 3675P 34VUA0 |
| P902,903 | | 9144484000 | D-SUB DE-09SLURL2 |
| Q101,201 | | 9163310620 | TR,TP 2SC-2878A |
| Q102,202 | | 9163310620 | TR,TP 2SC-2878A |
| Q104,204 | | 9164005420 | FET,2SJ498D |
| Q106,206 | | 9163310620 | TR,TP 2SC-2878A |
| Q151,251 | | 9163310620 | TR,TP 2SC-2878A |
| Q152,252 | | 9163310620 | TR,TP 2SC-2878A |
| Q153,253 | | 9163310620 | TR,TP 2SC-2878A |
| Q154,254 | | 9163310620 | TR,TP 2SC-2878A |
| Q155,255 | | 9163310620 | TR,TP 2SC-2878A |
| Q156,256 | | 9163310620 | TR,TP 2SC-2878A |
| Q351,451 | | 9163310620 | TR,TP 2SC-2878A |
| Q903 | | 9163310420 | DTR,DTC 124ES TP |
| R136,137 | ⚠ | 9114409000 | R,NON-F 1/4W 100 FH-15 |
| R236,237 | ⚠ | 9114409000 | R,NON-F 1/4W 100 FH-15 |
| SW1-5 | | 9135041100 | PUSH SW,SPUJ50H803-TK |
| SW6 | | 9135041000 | PUSH SW,SPUJ19A602-TK |
| SW7,8 | | 9135041000 | PUSH SW,SPUJ19A602-TK |
| T901-904 | | 9173021100 | TRANS PULSE 400UH |
| U1 | | 9179000200 | MIC CONDENSER,U-620-A |
| U101,201 | | 9167017300 | IC,NJM4565LD (8P) |
| U102,202 | | 9167017300 | IC,NJM4565LD (8P) |
| U103-105 | | 9167040700 | IC,NE5532N |
| U501,502 | | 9167017300 | IC,NJM4565LD (8P) |
| U503-505 | | 9167040700 | IC,NE5532N |
| U510 | | 9167017300 | IC,NJM4565LD (8P) |
| U901-910 | | 9122020620 | FILTER,EXCEMT103BT TP |
| U911-914 | | 9173014020 | FILTER,EXCEMT101BT (100PF) |
| U915-922 | | 9173014020 | FILTER,EXCEMT101BT (100PF) |
| VR1 | | 9172039000 | 5K(B) EVUE2JFK3 B53 |
| VR2 | | 9172023100 | 1S2UVR,14 10K(A)X2 |
| VR3 | | 9172023200 | 1S1UVR,11 50K(W) |
| VR4 | | 9172023100 | 1S2UVR,14 10K(A)X2 |

## GATHER PCB ASSY, TRANSPORT

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| | | *9145319020 | GATHER PCB ASSY,TRANSPORT [J,US/C] |
| | | *9145319050 | GATHER PCB ASSY,TRANSPORT [K,A,E,UK] |
| | | | TRANSPORT PCB |
| | | | LCD SUB PCB |
| | | | MIDI PCB |
| | | | TDIF PCB |
| CN1 | | 9143198000 | CONNECTOR,S9B-EH |
| CN2 | | 9173199000 | PLUG,10P S10B-EH-A |
| D181-186 | | 9165022150 | DIODE,TP 1SS133T |
| D191-196 | | 9165022150 | DIODE,TP 1SS133T |
| D201-206 | | 9165022150 | DIODE,TP 1SS133T |
| D341,344 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D342 | | 9174027720 | LED,SLR-332MG T32(GRN) |
| D343 | | 9174027520 | LED,SLR-332VR T32(RED) |
| D345,353 | | 9174028720 | LED,LA12540/TBF-2(ORG) |
| D351,352 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D354 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D355,365 | | 9174028920 | LED,LG12540/TBF-2(GRN) |
| D361,362 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D363,375 | | 9174028820 | LED,LI12540/TBF-2(RED) |
| D364 | | 9174028720 | LED,LA12540/TBF-2(ORG) |
| D371 | | 9174027620 | LED,SLR-332DU T32(ORG) |
| D373,374 | | 9174028720 | LED,LA12540/TBF-2(ORG) |
| D511-513 | | 9165022150 | DIODE,TP 1SS133T |
| D514,515 | | 9165022150 | DIODE,TP 1SS133T |
| D601-684 | | 9165022150 | DIODE,TP 1SS133T |
| D685,686 | | 9165022150 | DIODE,TP 1SS133T |
| F601 | ⚠ | 9150062400 | FUSE,5A 250V 51S050H [J,US/C] |
| | ⚠ | 9150062500 | FUSE,5A 250V 50T050H [K,A,E,UK] |
| F601 | | 9150062100 | FUSE HOLDER,CQ-203B |
| J501 | | 9144462000 | PIN JACK 1P,HSP-241V1B |
| J502 | | 9144520300 | PHONE JACK,069-2 |
| J503-505 | | 9144481000 | DIN JACK,HDC-052A-13 |
| J601,602 | | 9144488000 | BNC,COH2201-A |
| L1 | | 9173019900 | COIL,RCH875-151K |
| L601,602 | | 9173019850 | COIL,47UH-EC24-470KT5 |
| P1 | | 9143170000 | CONNECTOR PLUG,2P |
| P2 | | 9143172000 | CONNECTOR PLUG,B4B-EH-A |
| P501 | | 9144489000 | D-SUB,DA-15PLURL2 |
| P502 | | 9107140500 | CABLE ASSY G |
| P601-604 | | 9144445001 | D-SUB,205A-25FSTBBB3 |
| P611,612 | | 9144521000 | CN 3675P 34VUA0 |
| P613 | | 9143174000 | PLUG,6P B6B-EH-A |
| P614 | | 9107143200 | FLAT CABLE ASSY L |
| Q1,2 | | 9163461020 | TR,2SC2236-0 TP |
| Q501 | | 9163310420 | DTR,DTC 124ES TP |
| RA1,3,5 | | 9111304000 | R,ARRAY 2.2K*8 P=2.54 |
| RA2,4,6 | | 9111305000 | R,ARRAY 4.7K*8 P=2.54 |
| SW201-203 | | 9135041400 | PUSH SW,SKBMFA000A-TK |

## GATHER PCB ASSY, TRANSPORT

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| SW211,212 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW213,221 | | 9136002000 | TACT SW,SKHHDA |
| SW222,223 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW231,241 | | 9136002000 | TACT SW,SKHHDA |
| SW232,233 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW242,243 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW251-253 | | 9136003020 | TACT SW,EVQ11L H=5 TP |
| SW601 | | 9135041200 | SLIDER SW,SSSF123NA1-TK |
| T1 | | 9125145000 | TRANS,EW-12H/TW |
| U501 | | 9167026900 | IC,TC4069UBP |
| U502 | | 9167051100 | PHOTO COUPLER,PC-900 |
| U504,506 | | 9122020620 | FILTER,EXCEMT103BT TP |
| U509,510 | | 9122020620 | FILTER,EXCEMT103BT TP |
| U601 | | 9167073600 | GP1FA550RZ |
| U602 | | 9167073700 | GP1FA550TZ |
| U604 | | 9173014020 | FILTER,EXCEMT101BT (100PF) |

## GATHER PCB ASSY,MOTHER

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| | | *9145317000 | GATHER PCBA,MOTHER |
| | | | MOTHER PCB |
| J1,2 | | 9144520400 | CARD EDGE 4024S120F0B |
| J3-5 | | 9144510000 | CONNECTOR 3675P 40VUA0 |
| P1 | | 9143199000 | CONNE.PLUG,10P(S10B-EH-A) |
| P2 | | 9143198000 | CONNECTOR S9B-EH |
| P3 | | 9144332000 | PULG S4B-EH |

## GATHER PCB ASSY,POWER

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| | | *9145342020 | GATHER PCB ASSY,POWER |
| | | | [J,US/C] |
| | | *9145342050 | GATHER PCB ASSY,POWER |
| | | | [K,A,E,UK] |
| | | | PCB,POWER |
| | | | PCB,POWER SW |
| | | | PCB,TRANS 1 |
| | | | PCB,TRANS 2 |
| | | | PCB,TR1 |
| | | | PCB,TR2 |
| | | | PCB,TR3 |
| | | | PCB,TR4 |
| | | | PCB,TR5 |
| | | | PCB,BD |
| CN1 | | 9144491000 | CONNECTOR,B2P3-VH |
| C1,2 | ⚠ | 9117304100 | C,ELEC 4700U 35V |
| C3,4 | ⚠ | 9117200020 | C,ELEC TP 100M 35V |
| C101-103 | ⚠ | 9120000101 | SPARK KILLER,0.0047M 250V |
| D1 | ⚠ | 9165026900 | BRIDGE DIODE,RS403L |

## GATHER PCB ASSY,POWER

| REF.NO. | | PARTS NO. | DESCRIPTION |
|---|---|---|---|
| D3 | | 9165027000 | BRIDGE DIODE,KBU6D |
| D4,5 | | 9165020550 | DIODE,LT 1N4003 TP 0.6MM |
| D6 | | 9166055551 | Z-DIODE,MTZJ39B |
| D7 | | 9166054651 | Z-DIODE,MTZ J 16 B |
| D8,9 | | 9165022150 | DIODE,TP 1SS133T |
| D10-13 | | 9165020550 | DIODE,LT 1N4003 TP 0.6MM |
| D14,15 | | 9165020550 | DIODE,LT 1N4003 TP 0.6MM |
| EP1 | | 9229088000 | EARTH PLATE B (GND-8) |
| F1,2 | ⚠ | 9150036000 | T-LAG FUSE,4A 250V T |
| | | | [J,US/C] |
| F1,2 | ⚠ | 9150047000 | T-LAG FUSE,4A 250V T |
| | | | [K,A,E,UK] |
| F3 | ⚠ | 9150028000 | T-LAG FUSE,1.6A 250V T |
| | | | [K,A,E,UK] |
| F3 | ⚠ | 9150037000 | T-LAG FUSE,1.6A 250V T |
| | | | [J,US/C] |
| F4 | ⚠ | 9150036000 | T-LAG FUSE,4A 250V T |
| | | | [J,US/C] |
| F4 | ⚠ | 9150047000 | T-LAG FUSE,4A 250V T |
| | | | [K,A,E,UK] |
| F1-4 | | 9150062100 | FUSE HOLDER CQ-203B |
| L101 | ⚠ | 5292806300 | FILTER,FK0B16MH13 |
| P1 | | 9143182000 | PLUG,14P B14B-EH-A |
| P2 | | 9143176000 | PLUG,8P B8B-EH-A |
| P3 | | 9143180000 | CONNECTOR PLUG,12P |
| P4 | | 9143174000 | PLUG,6P B6B-EH-A |
| P5 | | 9143178000 | CONNECTOR PLUG,10P |
| P6 | | 9143170000 | CONNECTOR PLUG,2P |
| P7 | | 9143180000 | CONNECTOR PLUG,12P |
| P8 | | 9143172000 | CONNECTOR PLUG,B4B-EH-A |
| P9 | | 9143180000 | CONNECTOR PLUG,12P |
| P101 | ⚠ | 9144493000 | AC INLET,M1908-B |
| P102,103 | | 9144491000 | CONNECTOR,B2P3-VH |
| Q1 | ⚠ | 9163202900 | TR,2SB1274R |
| Q2 | ⚠ | 9163202900 | TR,2SB1274R |
| Q3 | ⚠ | 9163610300 | TR,2SD1913R |
| Q4 | ⚠ | 9163018920 | TR,2SB1238R |
| Q5 | | 9163019120 | TR,2SD1858R |
| Q6 | | 9163013320 | DTR,DTA115ES |
| Q9 | ⚠ | 9163202900 | TR,2SB1274R |
| R1,2 | ⚠ | 9114526700 | R,NONFLAMMABLE 1/4W 270 |
| SW101 | ⚠ | 9135037200 | POWER SW,SFDLB11M7U TK |
| U101 | ⚠ | 9167022400 | IC,M5230L (8P) |
| U102,103 | ⚠ | 9167016700 | IC M5237L (3P) |

## IF-TD/DM (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | 9260365700 | PANEL,TD/DM CARD |
| | 9260366200 | LEVER SLOT |
| | 9260330700 | D-SUB SCREW,HW-H118MN02 |
| | 9145329000 | GATHER PCB ASSY,IF-TD/DM |
| | | PCB,IF-TD/DM |
| D1 | 9165023530 | DIODE,1SS355 TE17 |
| D2-17 | 9165024730 | DA,IMN10 T108 CHIP |
| P1 | 9144522200 | HEADER6,2556P6UA00 |
| P2 | 9144482000 | D-SUB DB-25SLURL2 |
| P3 | 9144489000 | D-SUB DA-15PLURL2 |
| Q1 | 9163459030 | DTR,DTC363EK T146 |
| R17,32 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R50,62 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R63 | 9111282030 | R,ARRAY 2.2K*8 MNR35 CHIP |
| R88 | 9111283030 | R,ARRAY 4.7K*8 MNR35 CHIP |
| U1-3 | 9167055830 | IC,HD74LV541AFPEL |
| U5,6 | 9167055830 | IC,HD74LV541AFPEL |
| U7 | 9167067730 | IC,HD74LV245AFPEL |
| U8 | 9167045830 | IC,HD74HC541FPV |
| U9 | 9167050730 | IC,SN74HCT541NSR(20P) |
| U10 | 9167064330 | IC,HD74LVC541AFPEL(20P) |
| U11,12 | 9173016230 | EMI,EXC CET 471U |
| U13 | 9167040030 | IC,M66230FP |
| U14 | 9173016230 | EMI,EXC CET 471U |
| U15 | 9167050230 | IC,M5M34051FP |
| X1 | 9173013930 | CRYSTAL,SK3 16MHZ |

## IF-AE/DM (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | 9260365900 | PANEL,AE/DM CARD |
| | 9260366200 | LEVER SLOT |
| | 9260330600 | D-SUB WASHER,HW-C050MN00 |
| | 9260330700 | D-SUB SCREW,HW-H118MN02 |
| | 9145331000 | GATHER PCB ASSY,IF-AE/DM |
| | | PCB,IF-AE/DM |
| D1 | 9165023530 | DIODE 1SS355 TE17 |
| D2,3 | 9165024730 | DA,IMN10 T108 CHIP |
| D4,5 | 9165024730 | DA,IMN10 T108 CHIP |
| D6,7 | 9165024730 | DA,IMN10 T108 CHIP |
| D8,9 | 9165024730 | DA,IMN10 T108 CHIP |
| D10,11 | 9165024730 | DA,IMN10 T108 CHIP |
| D12,13 | 9165024730 | DA,IMN10 T108 CHIP |
| J1 | 9144482000 | D-SUB DB-25SLURL2 |
| J2 | 9143174000 | PLUG 6P B6B-EH-A |
| L1,2 | 9122022230 | EMI FILTER,NFM51R00P506 |
| L3,4 | 9122022230 | EMI FILTER,NFM51R00P506 |
| L5,6 | 9122022230 | EMI FILTER,NFM51R00P506 |
| L7,8 | 9122022230 | EMI FILTER,NFM51R00P506 |
| R39,43 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R46 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| T1-8 | E00595800A | TRANS,PULSE 400UH |
| U1,4 | 9167055830 | IC,HD74LV541AFPEL |
| U2 | S0043574 | IC,CS8415A-CZ |
| U3 | 9167051030 | IC,NJM78L05UA-TE1(3P) |
| U5,7 | 9167055830 | IC,HD74LV541AFPEL |
| U6 | S0042443 | IC,XCS40XL-4PQ208C |
| U8,12 | 9167055830 | IC,HD74LV541AFPEL |
| U9 | 9167074930 | IC,HD74LV00AFPEL |
| U10 | 9167067730 | IC,HD74LV245AFPEL |
| U11 | 9167075030 | IC,HD74LV04AFPEL |
| U13,14 | 9167055830 | IC,HD74LV541AFPEL |
| U15 | 9167076230 | IC,DS26C31TM |
| U16 | 9167055830 | IC,HD74LV541AFPEL |
| U17 | 9167076330 | IC,DS26C32ATM |

## IF-AD/DM (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | 9260365800 | PANEL,AD/DM CARD |
| | 9260366200 | LEVER SLOT |
| | 9260330600 | D-SUB WASHER,HW-C050MN00 |
| | 9260330800 | D-SUB SCREW,HW-H118EN00 |
| | 9145330000 | GATHER PCBA,IF-AD/DM |
| | | PCB,IF-AD/DM |
| D1 | 9165023530 | DIODE,1SS355 TE17 |
| J1 | 9167073700 | GP1FA550TZ |
| J2 | 9144484000 | D-SUB,DE-09SLURL2 |
| J3 | 9167073600 | GP1FA550RZ |
| L1,2 | 9122021230 | COIL,47UH ELJPA470KF CHIP |
| L3,4 | 9122022230 | EMI FILTER,NFM51R00P506 |
| R1,2 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R32,35 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R36,37 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R38 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| U1,2 | 9167076130 | IC,TC74HCT244AFP |
| U3,6 | 9167055830 | IC,HD74LV541AFPEL |
| U4 | 9167075130 | IC,HD74LV74AFPEL |
| U5 | 9167075330 | IC,HD74LV139AFPEL |
| U7,9 | 9167075030 | IC,HD74LV04AFPEL |
| U8,14 | 9167055830 | IC,HD74LV541AFPEL |
| U10,13 | 9167076130 | IC,TC74HCT244AFP |
| U11,12 | 9167075230 | IC,HD74LV138AFPEL |
| U15 | 9167055830 | IC,HD74LV541AFPEL |
| U16 | 9167068830 | IC,TC74HCT245AFP |
| U17 | 9167067730 | IC,HD74LV245AFPEL |
| U18,21 | 9167051030 | IC,NJM78L05UA-TE1(3P) |
| U19 | 9167066630 | IC,AL1401A |
| U20 | 9167051430 | IC,TC74VHCT04AF(14P) |
| U22 | 9167066730 | IC,AL1402 |
| U23,24 | 9167075030 | IC,HD74LV04AFPEL |
| U25,28 | 9167075430 | IC,HD74LV273AFPEL |
| U26 | 9167070530 | IC,PC410 |
| U27 | 9167040030 | IC,M66230FP |
| X1 | 9173013930 | CRYSTAL,SK3 16MHZ |

## IF-AN/DM (OPTION)

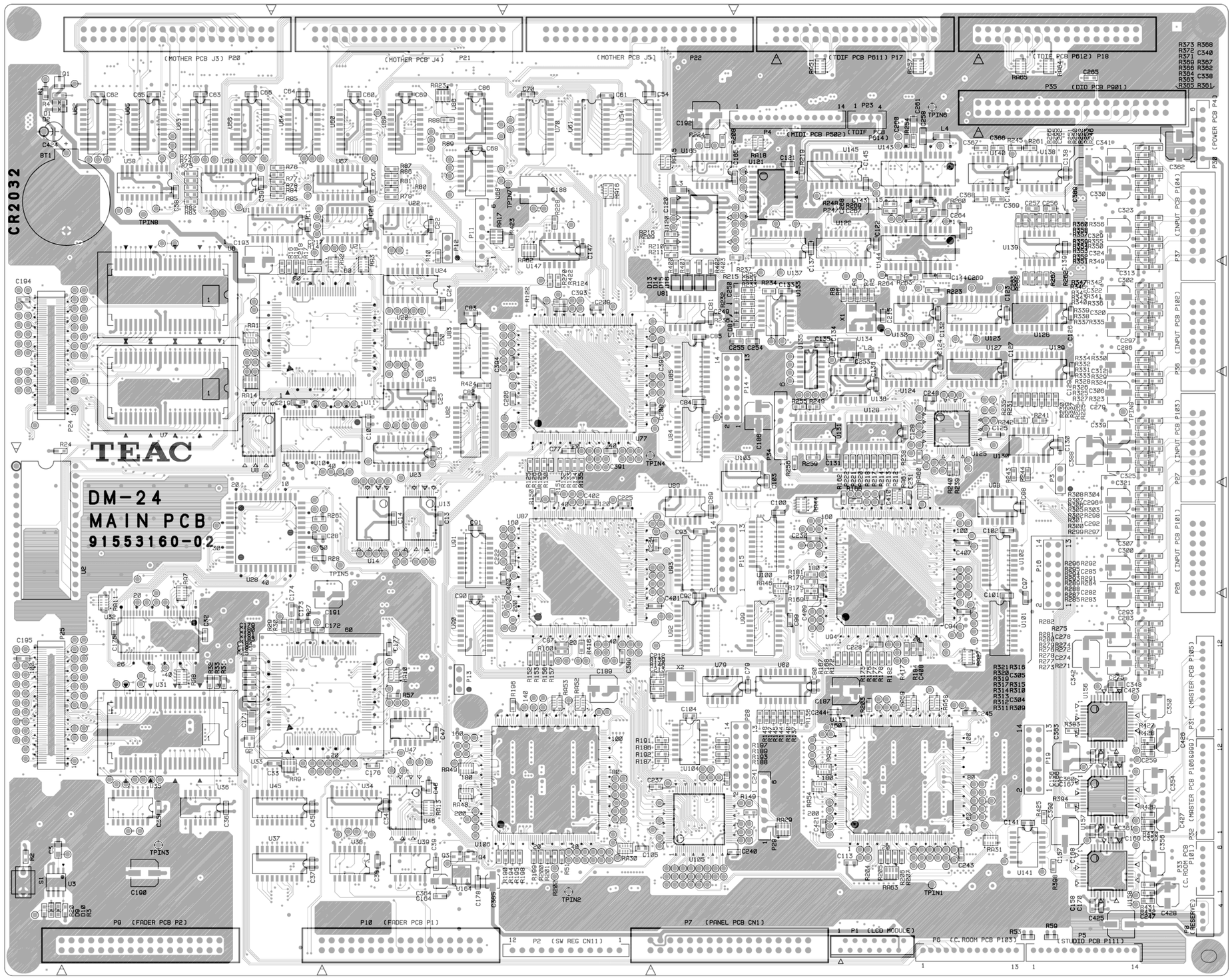
| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | 9260366000 | PANEL,AN/DM CARD |
| | 9260366200 | LEVER SLOT |
| | 9260330700 | D-SUB SCREW,HW-H118MN02 |
| | 9145332000 | GATHER PCBA,IF-AN/DM |
| | | PCB,IF-AN/DM |
| D010,020 | 9165023530 | DIODE,1SS355 TE17 |
| D011-018 | 9165023530 | DIODE,1SS355 TE17 |
| D021-028 | 9165023530 | DIODE,1SS355 TE17 |
| D031-038 | 9165023530 | DIODE,1SS355 TE17 |
| D041-048 | 9165023530 | DIODE,1SS355 TE17 |
| J010,020 | 9144482000 | D-SUB,DB-25SLURL2 |
| L010,020 | 9122022330 | COIL,LQH4C100K04 |
| L011-018 | 9173020930 | BEADS,BLM11B121SD |
| L021-028 | 9173020930 | BEADS,BLM11B121SD |
| L031-038 | 9173020930 | BEADS,BLM11B121SD |
| L041-048 | 9173020930 | BEADS,BLM11B121SD |
| L050,060 | 9122022730 | BEAD,BK1608HS102-T |
| L070,080 | 9122022730 | BEAD,BK1608HS102-T |
| L090,100 | 9122022730 | BEAD,BK1608HS102-T |
| L110,120 | 9122022730 | BEAD,BK1608HS102-T |
| L130,140 | 9122022730 | BEAD,BK1608HS102-T |
| L130,140 | 9122022730 | BEAD,BK1608HS102-T |
| L501-504 | 9122022330 | COIL,LQH4C100K04 |
| P020 | 9143174000 | PLUG 6P B6B-EH-A |
| Q010,030 | 9163021430 | DTR,DTA114EKAT-146 |
| Q011-018 | 9163021430 | DTR,DTA114EKAT-146 |
| Q020,040 | 9163461230 | DTR,DTC114YKAT-146 |
| R300,310 | 9111306030 | R,ARRAY MNR15E0RPJ103 |
| R320,330 | 9111306030 | R,ARRAY MNR15E0RPJ103 |
| U010 | S00438000A | IC,PLD(AD)DM OPT |
| U020 | 9167026700 | IC,NJM7812FA (3P) |
| U030 | 9167035800 | IC,NJM7912FA (3P) |
| U501-504 | 9167064530 | IC,AK5383VS-E2 |
| U521-U524 | 9167076430 | IC,AK4393VF |
| SW011-018 | 9135041730 | SLIDE SW,CHS-01TA1 |
| SW021-028 | 9135041730 | SLIDE SW,CHS-01TA1 |
| SW031-038 | 9135041730 | SLIDE SW,CHS-01TA1 |
| SW041-048 | 9135041730 | SLIDE SW,CHS-01TA1 |

## IF-CS/DM (OPTION)

| REF.NO. | PARTS NO. | DESCRIPTION |
|---|---|---|
| | 9260366100 | PANEL,CS/DM CARD |
| | 9260366200 | LEVER SLOT |
| | 9260330600 | D-SUB WASHER,HW-C050MN00 |
| | 9260330800 | D-SUB SCREW,HW-H118EN00 |
| | 9109031900 | CABLE,CASCADE-DM |
| | 9145333000 | GATHER PCB ASSY,IF-CS/DM |
| | | PCB,IF-CS/DM |
| D1,2 | 9174027430 | LED,KPK-3020NC(ORG) |
| J1 | 9144483000 | D-SUB DB-37SLURL2 |
| L1-16 | 9122022230 | EMI FILTER,NFM51R00P506 |
| R24-27 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| R48 | 9111297030 | R,ARRAY 10K*8 YC-15J |
| U1,2 | 9167055830 | IC,HD74LV541AFPEL |
| U3,9 | 9167055830 | IC,HD74LV541AFPEL |
| U4 | 9167066330 | IC,HD74LV32AFPEL |
| U5 | 9167075030 | IC,HD74LV04AFPEL |
| U7 | 9167066230 | IC,HD74LV125AFPEL |
| U8,10 | 9167075230 | IC,HD74LV138AFPEL |
| U11,12 | 9167055830 | IC,HD74LV541AFPEL |
| U13,15 | 9167055830 | IC,HD74LV541AFPEL |
| U14,19 | 9167067730 | IC,HD74LV245AFPEL |
| U16 | 9167064830 | IC,HD74LV08AFP |
| U17 | S0038953 | IC,ADSP-21065L |
| U18 | 9173020430 | CRYSTAL,MIN35A-T 30.0MHZ |
| U20 | 9167069130 | IC,HD74LV574AFPEL |
| U21 | 9167055830 | IC,HD74LV541AFPEL |
| U22,23 | 9167070830 | IC,DS90LV032ATM |
| U24,25 | 9167070930 | IC,DS90LV031ATM |

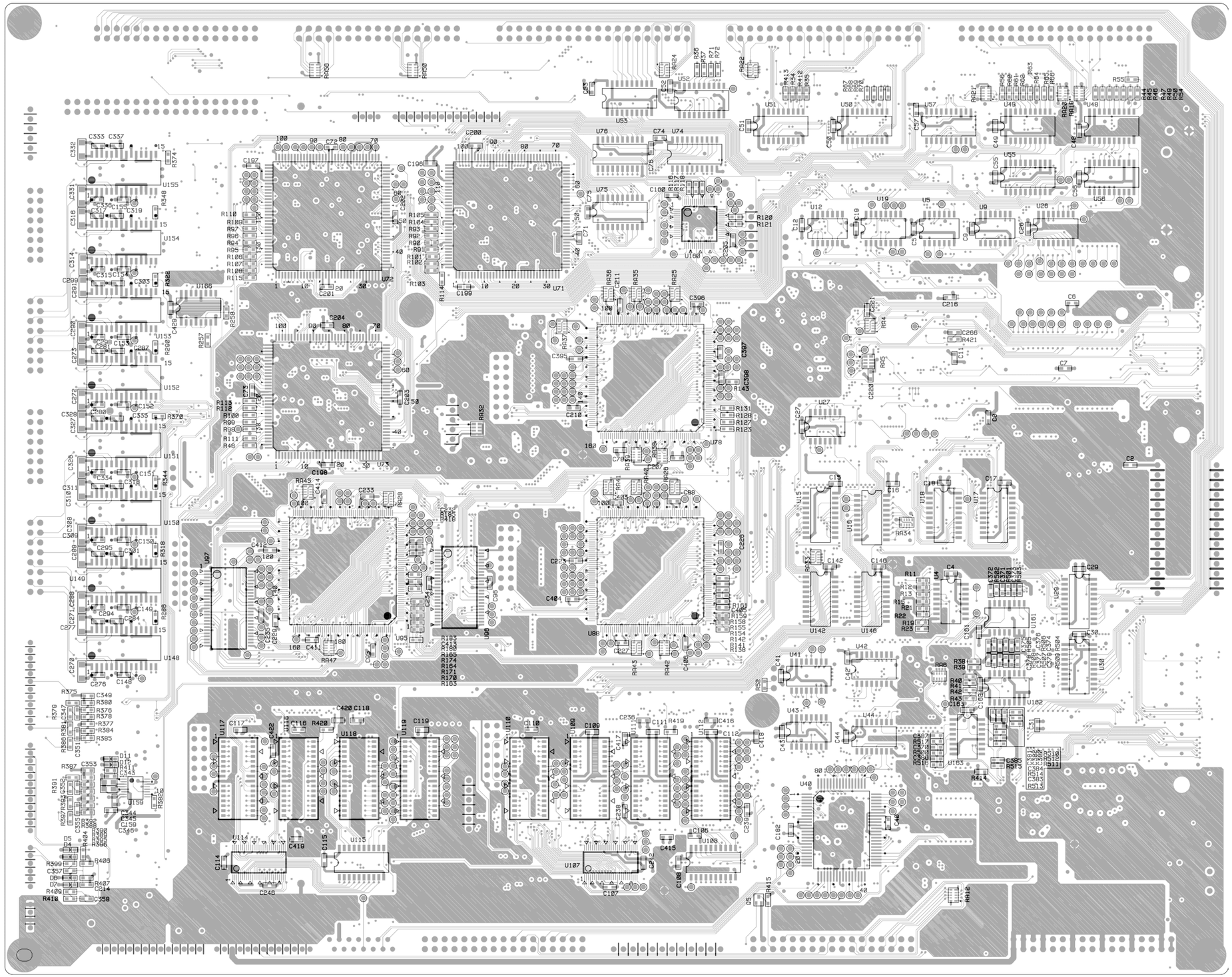
**MAIN PCB**

SIDE A

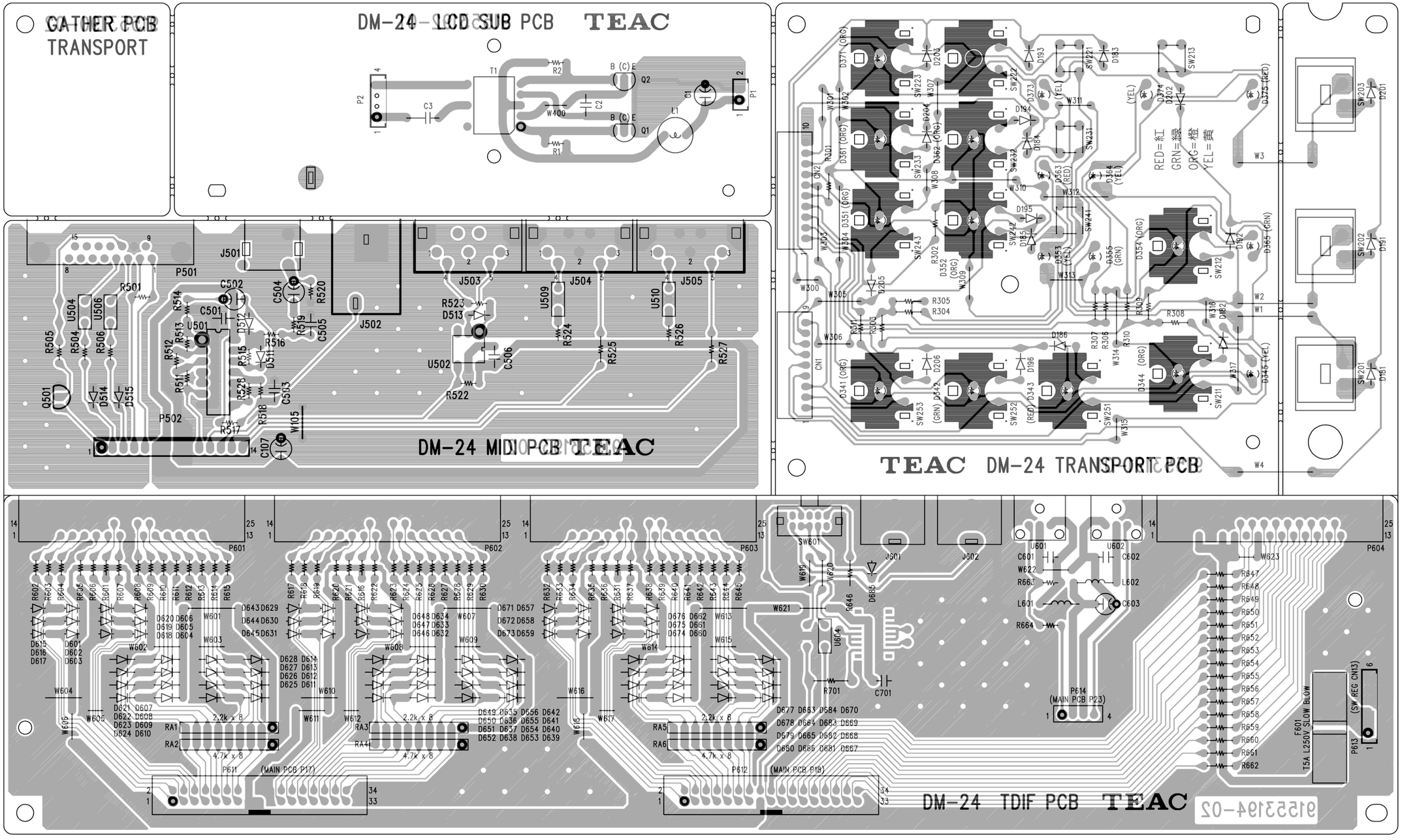


**MAIN PCB**

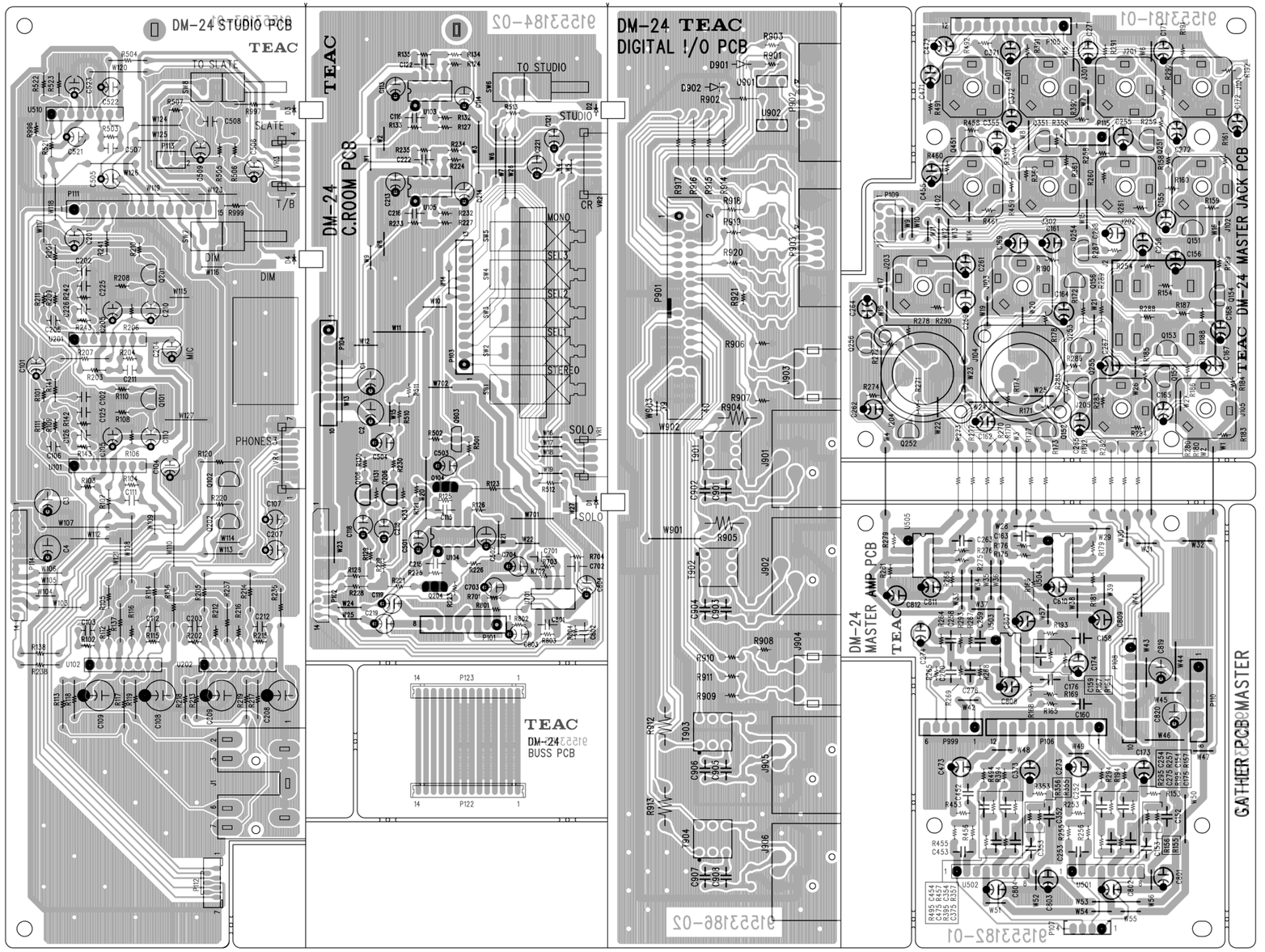
SIDE B



**GATHER PCB, TRANSPORT (TRANSPORT PCB, LCD SUB PCB, MIDI PCB, TDIF PCB)**

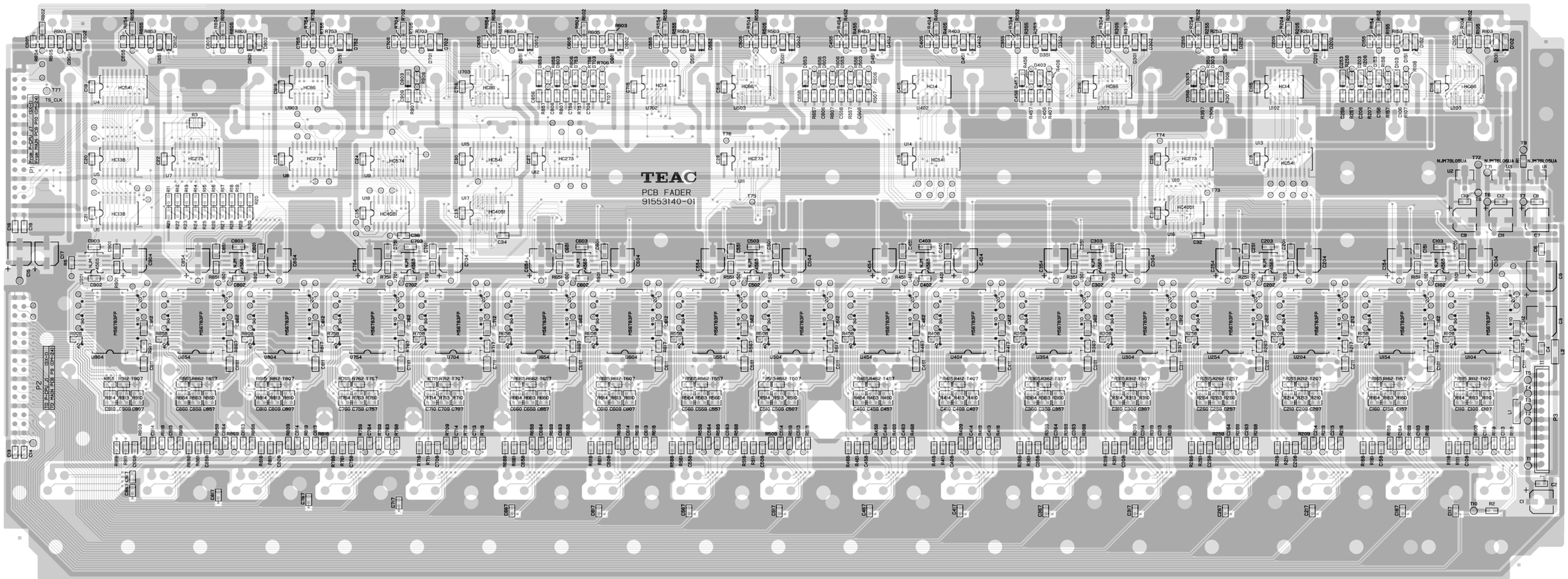


**GATHER PCB, MASTER (STUDIO PCB, C.ROOM PCB, DIGITAL I/O PCB, MASTER JACK PCB, MASTER AMP PCB, BUSS PCB)**



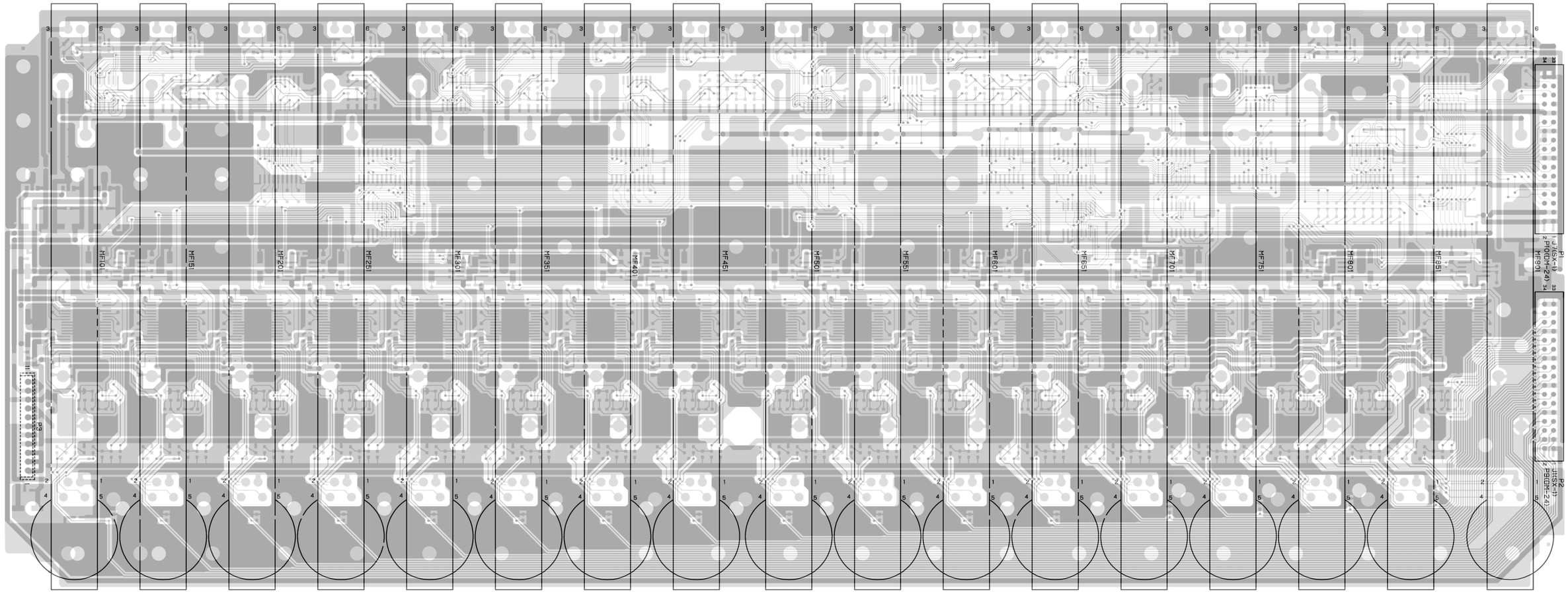
**FADER PCB**

SIDE A



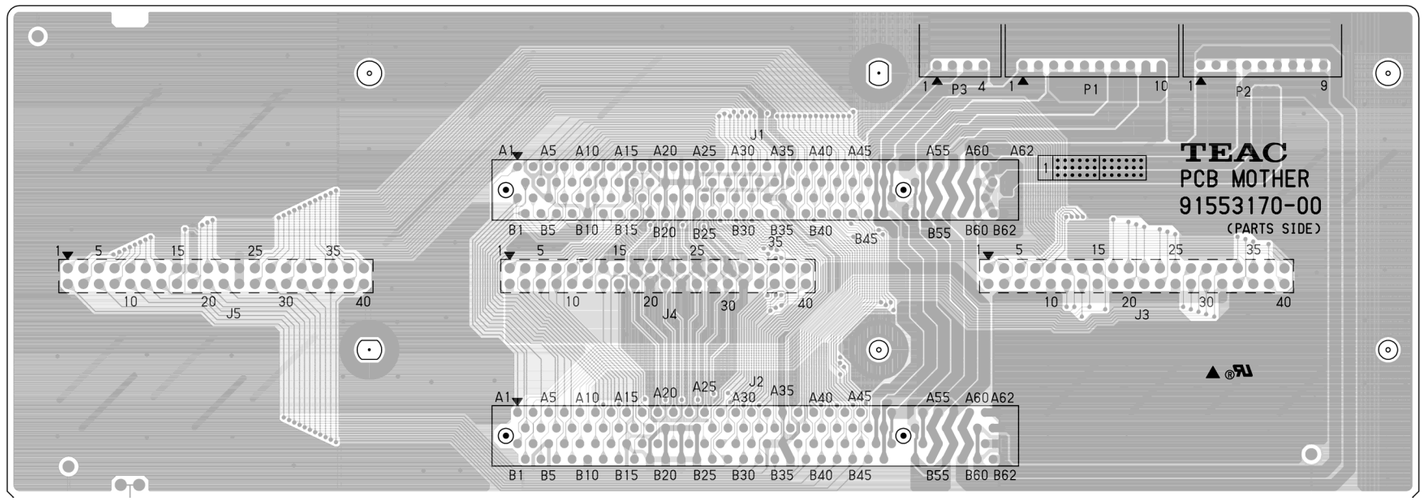
**FADER PCB**

SIDE B



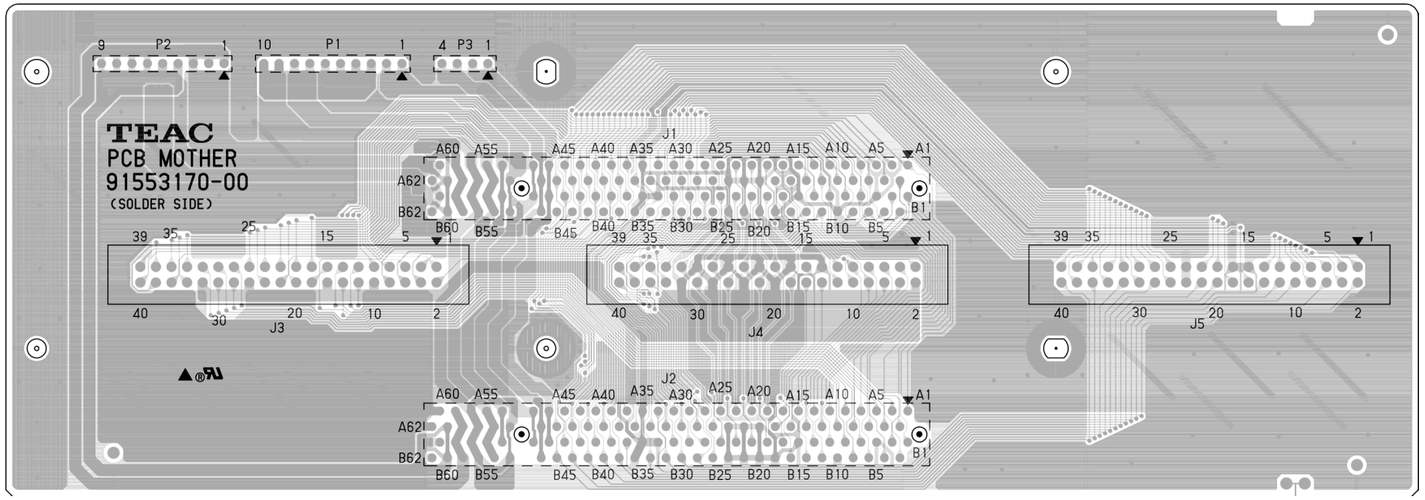
**MOTHER PCB**

SIDE A



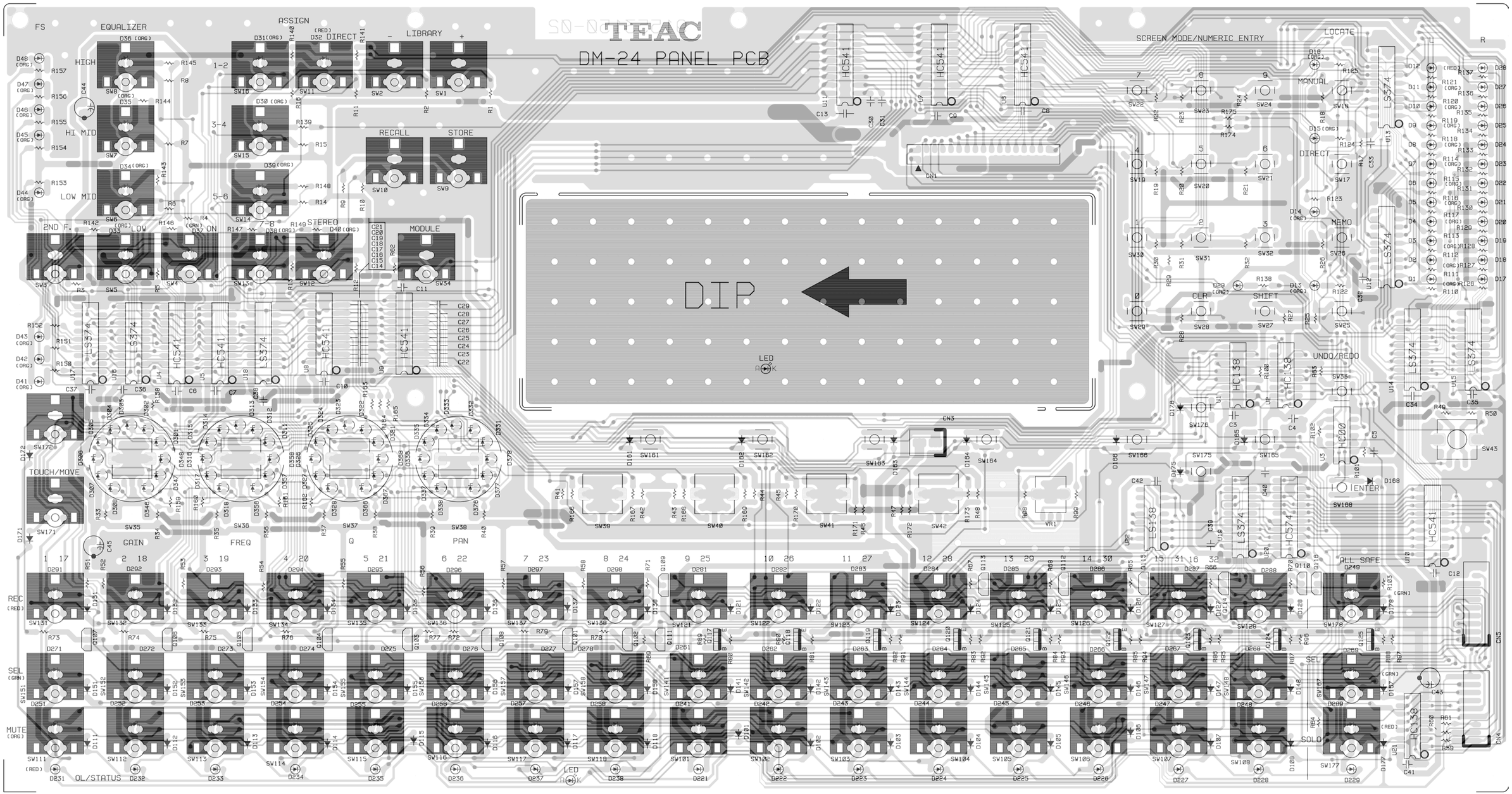

**MOTHER PCB**

SIDE B



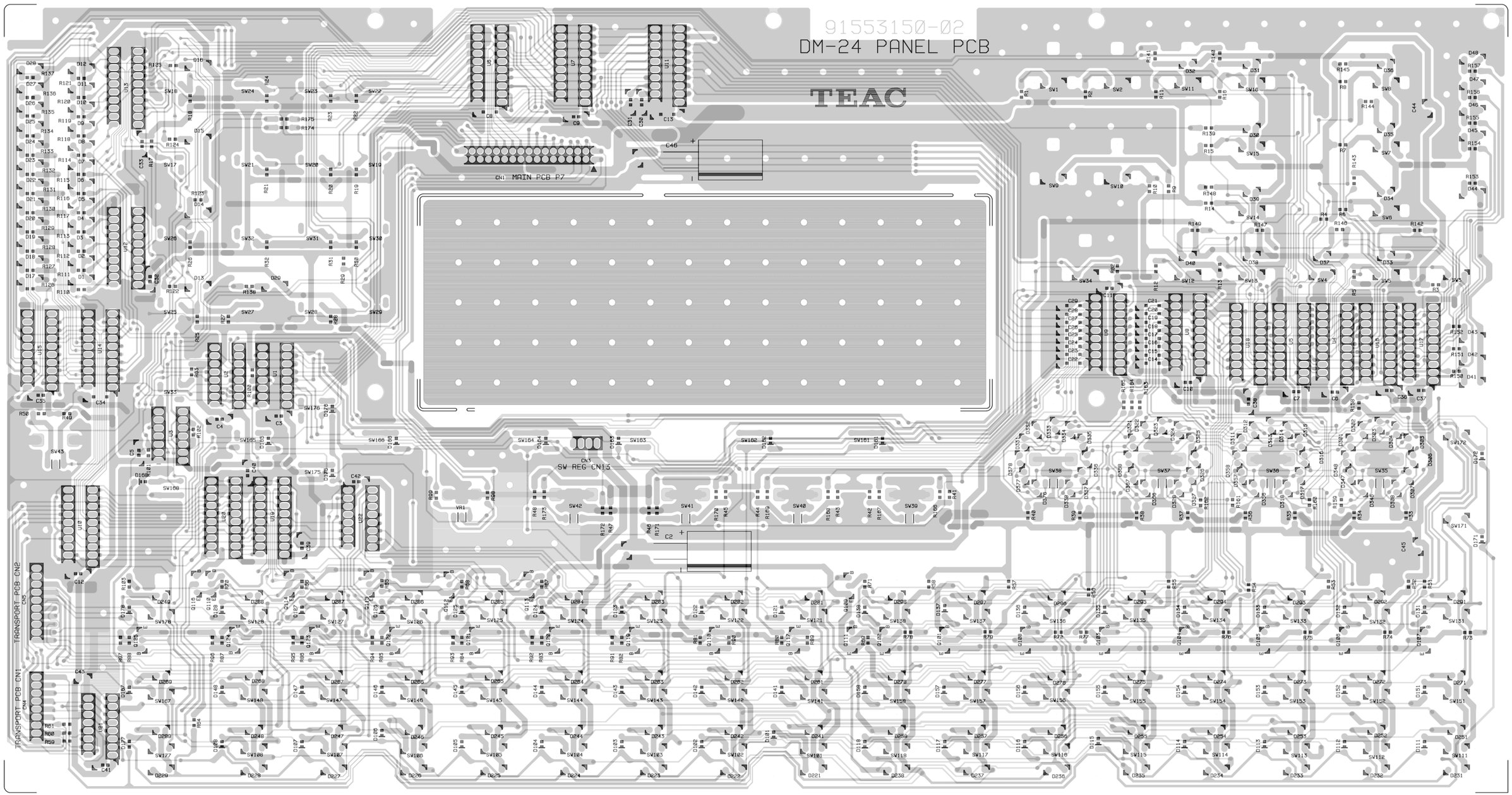
**PANEL PCB**

SIDE A

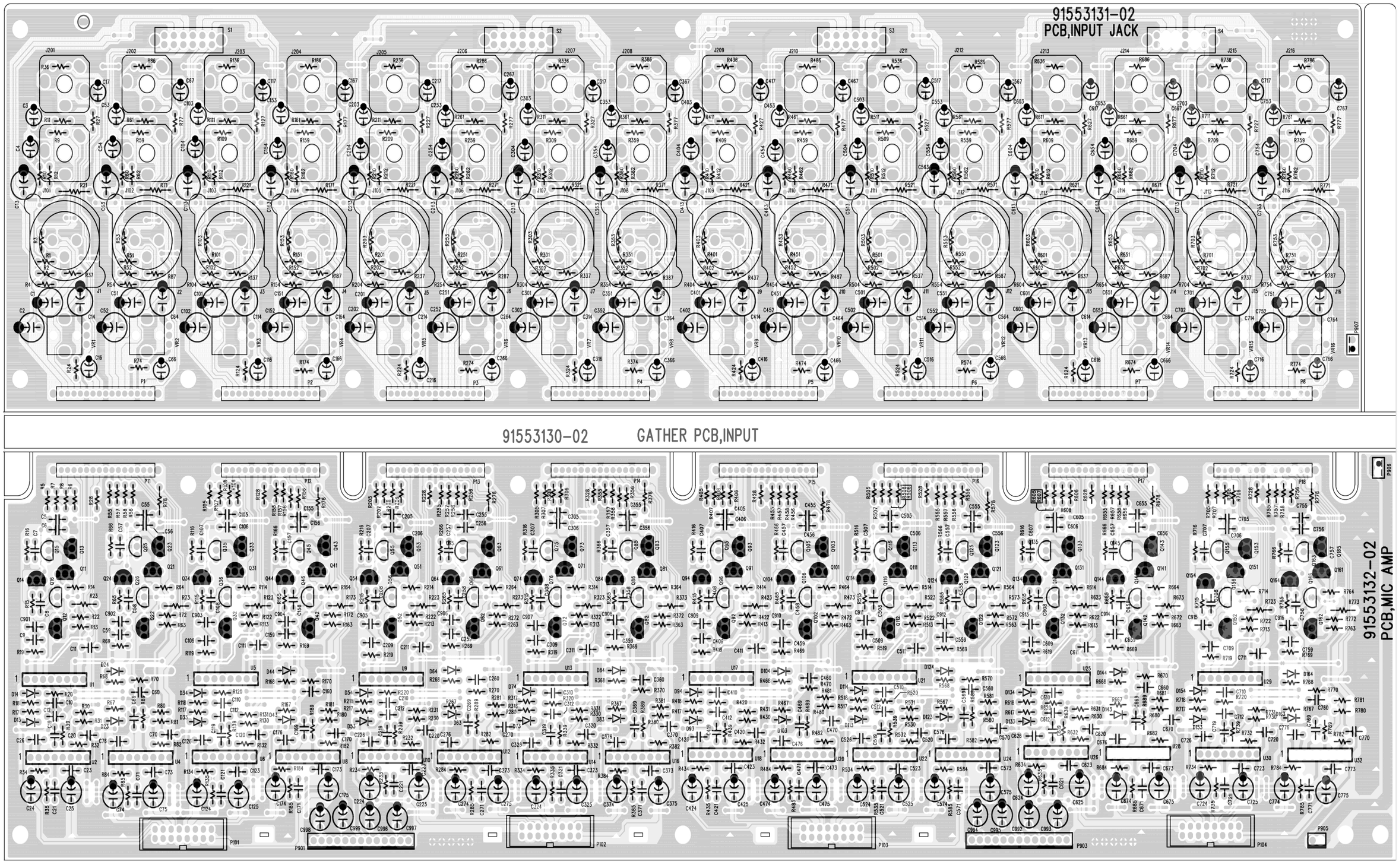


**PANEL PCB**

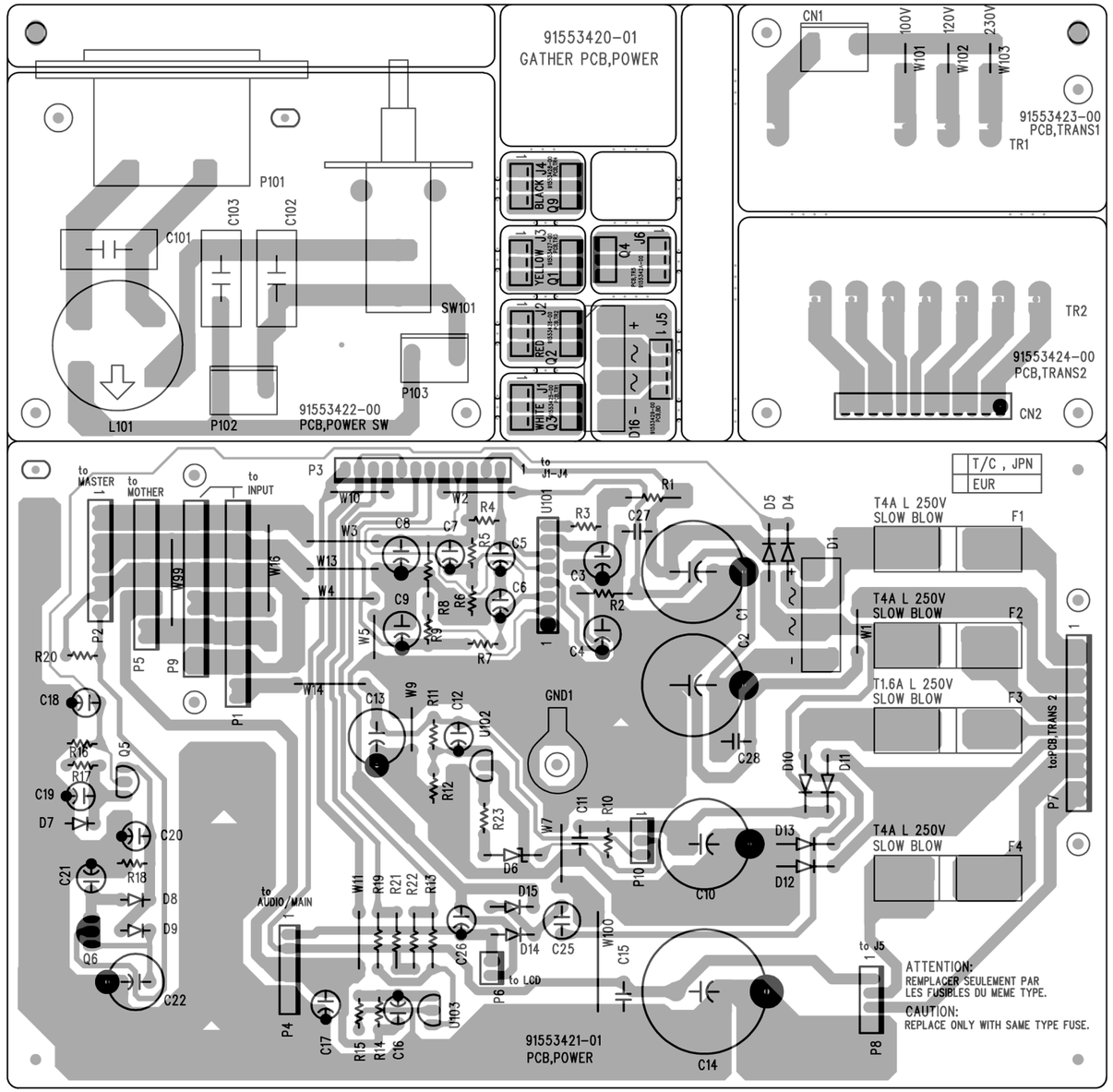
SIDE B



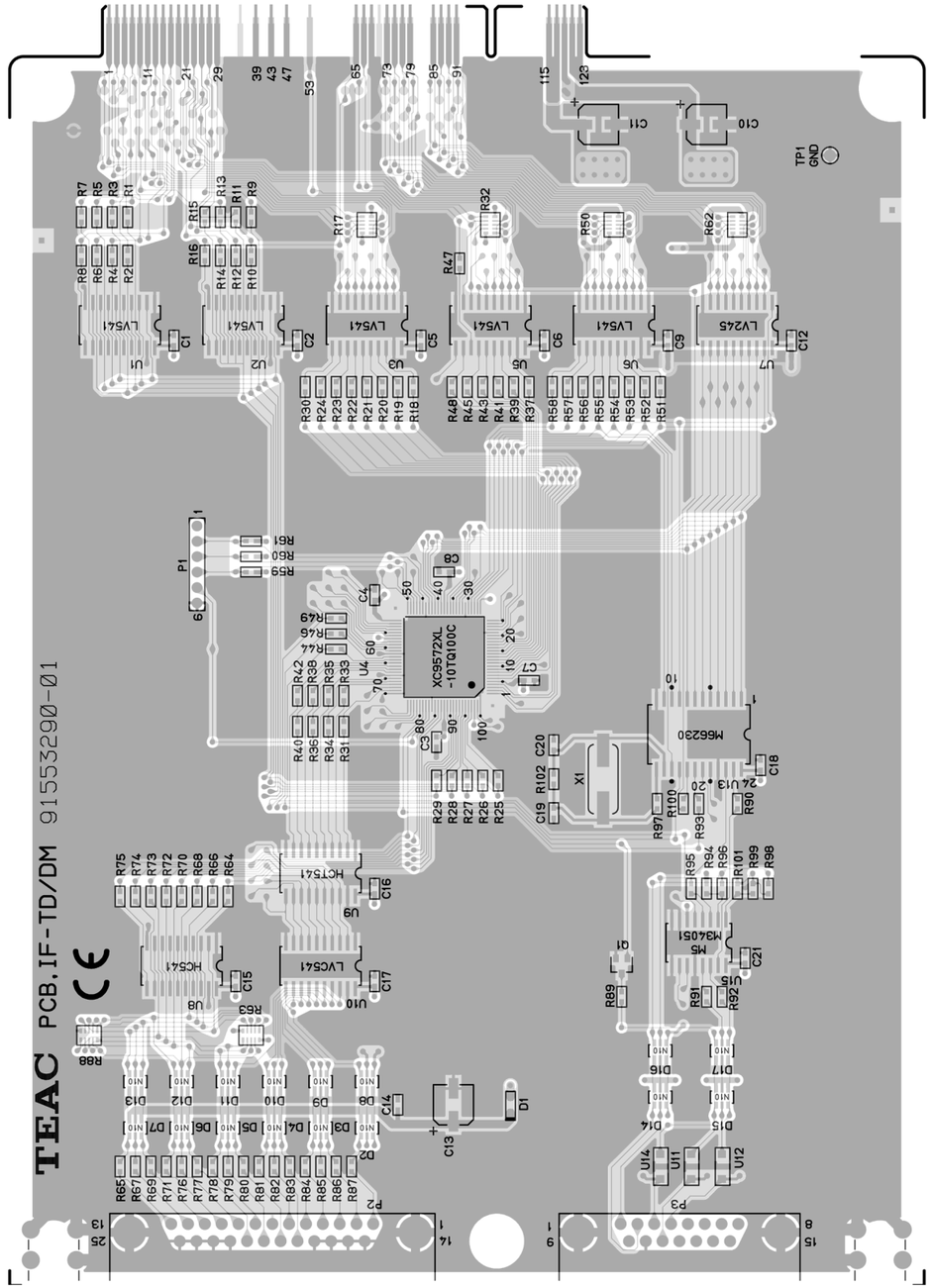
## GATHER PCB, INPUT (INPUT JACK PCB, MIC AMP PCB)



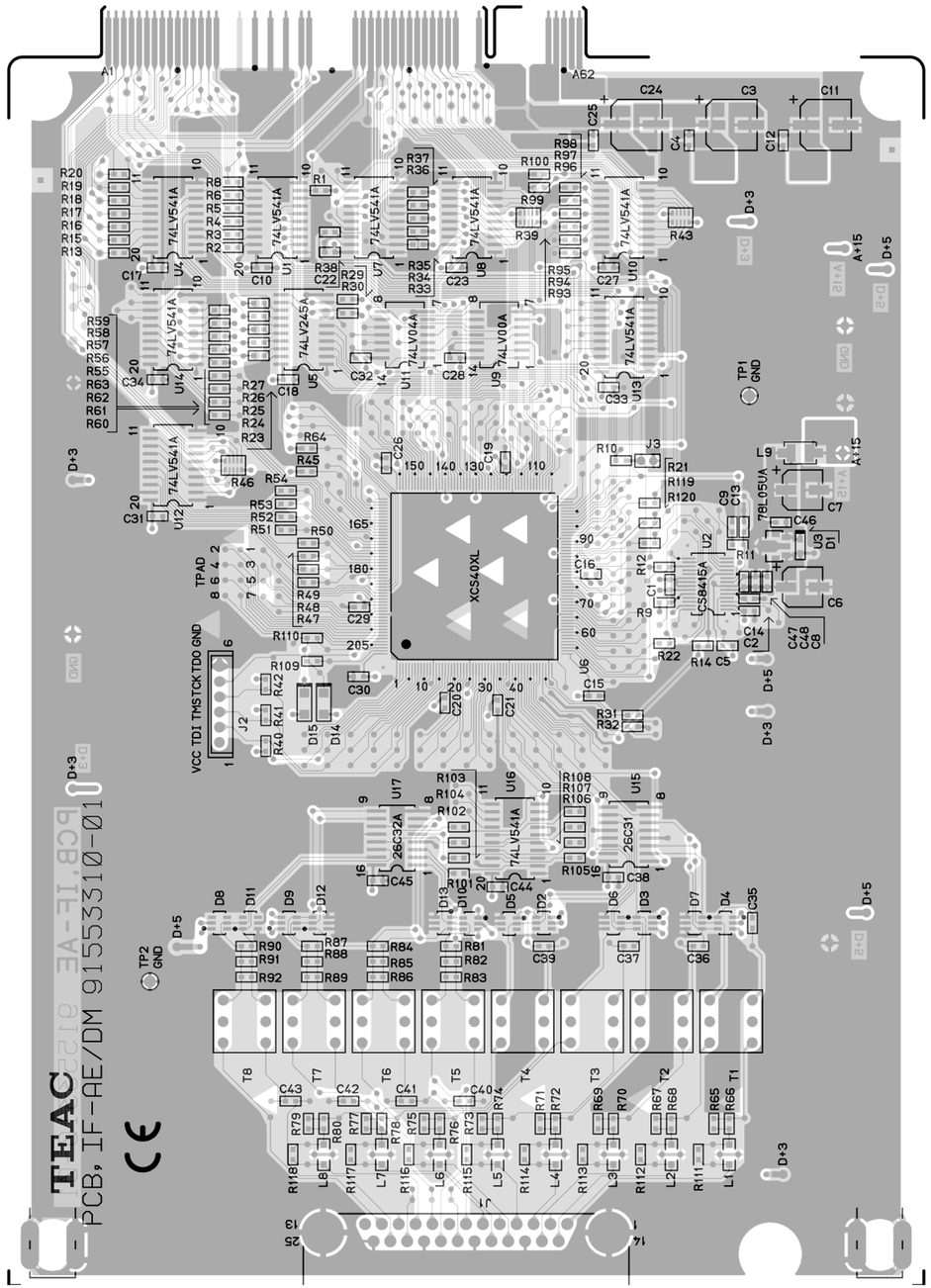
**GATHER PCB, POWER (POWER PCB, POWER SW PCB, TRANS1/2 PCB, TR1/2/3/4/5 PCB, BD PCB)**



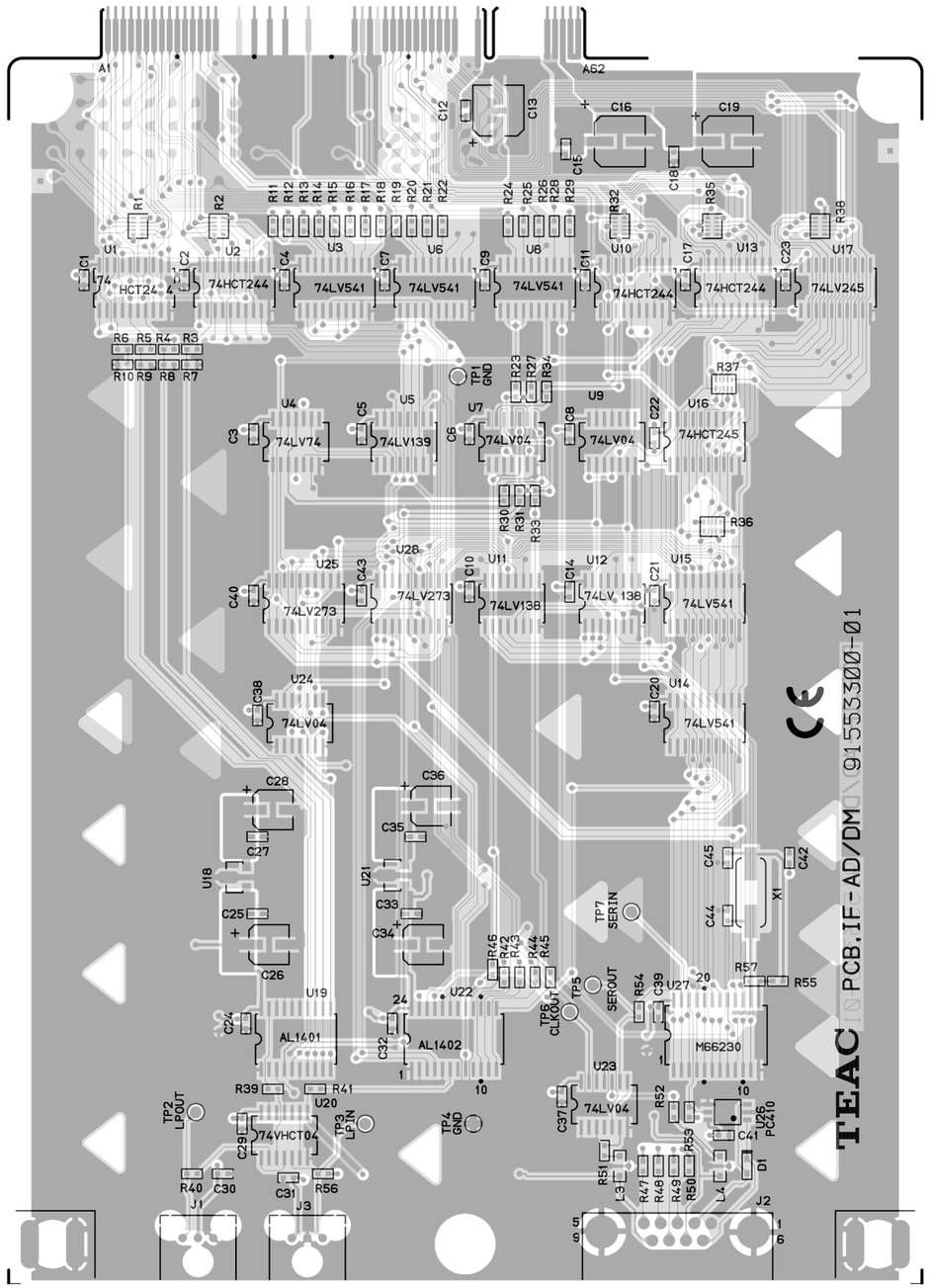
**IF-TD/DM PCB (OPTION)**



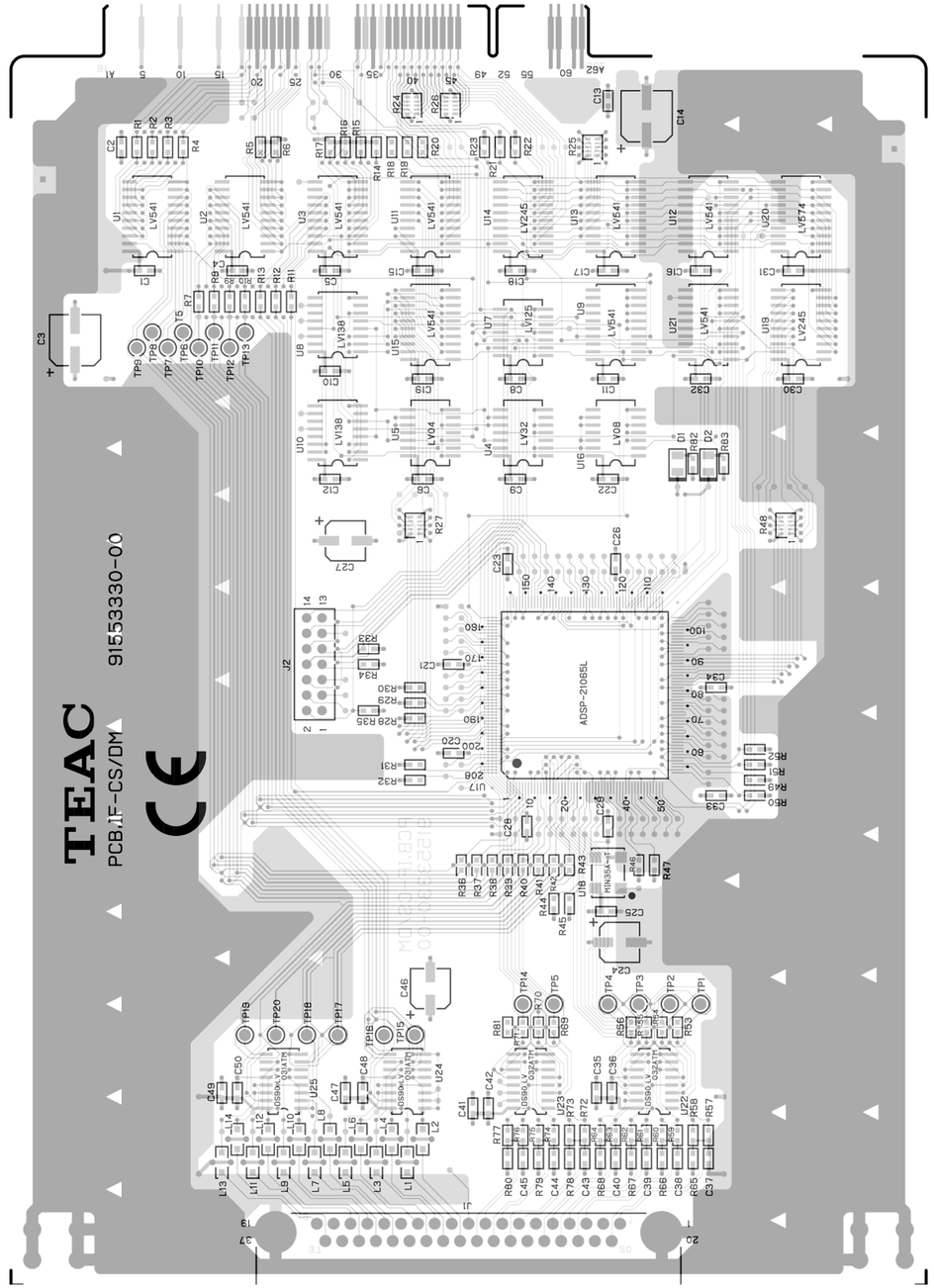

**IF-AE/DM PCB (OPTION)**



## IF-AD/DM PCB (OPTION)

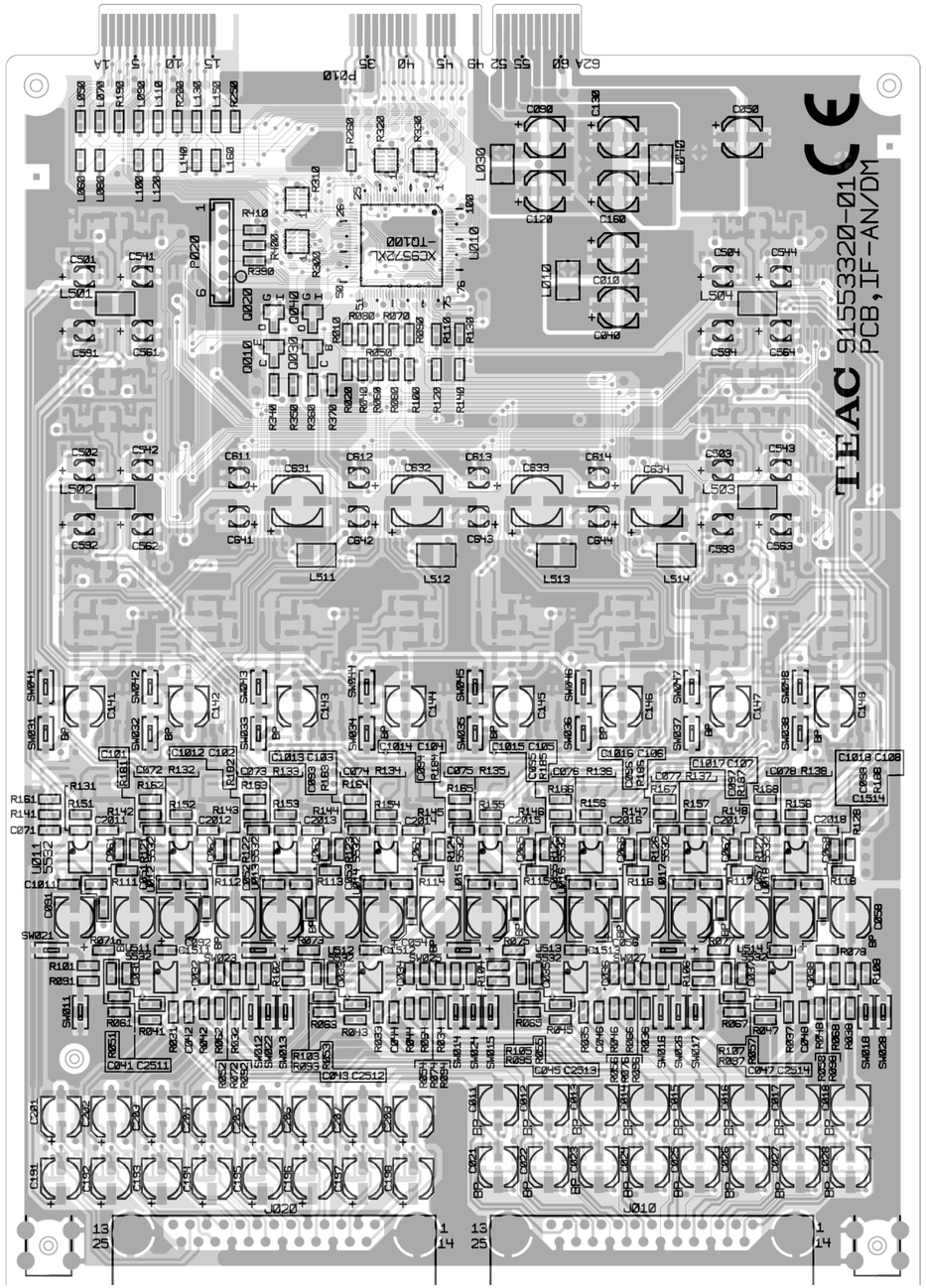



## IF-CS/DM PCB (OPTION)



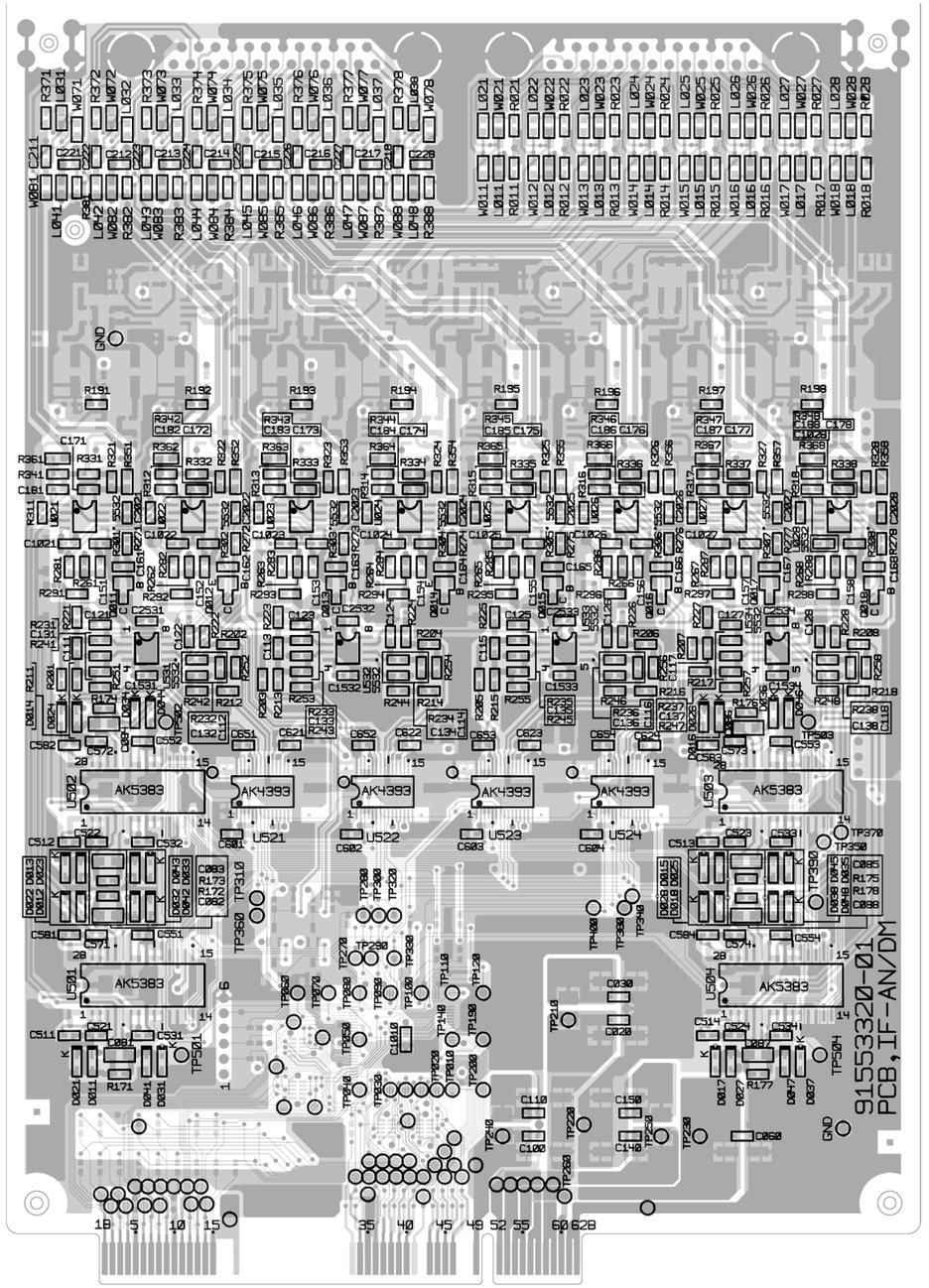
**IF-AN/DM PCB (OPTION)**

SIDE A

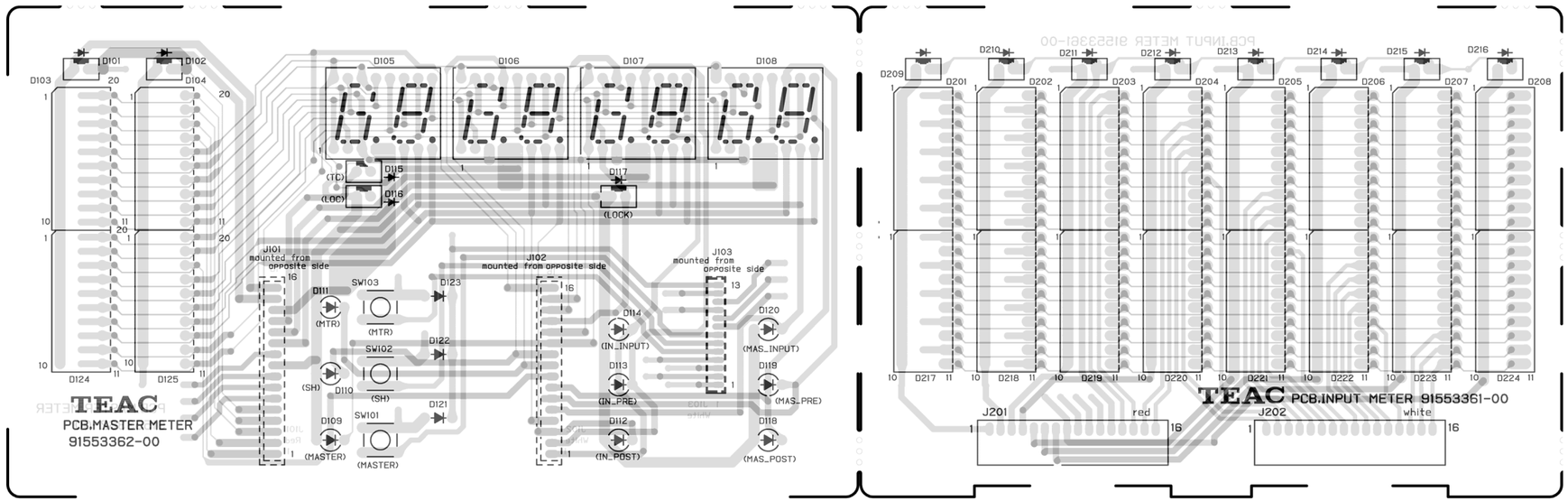



**IF-AN/DM PCB (OPTION)**

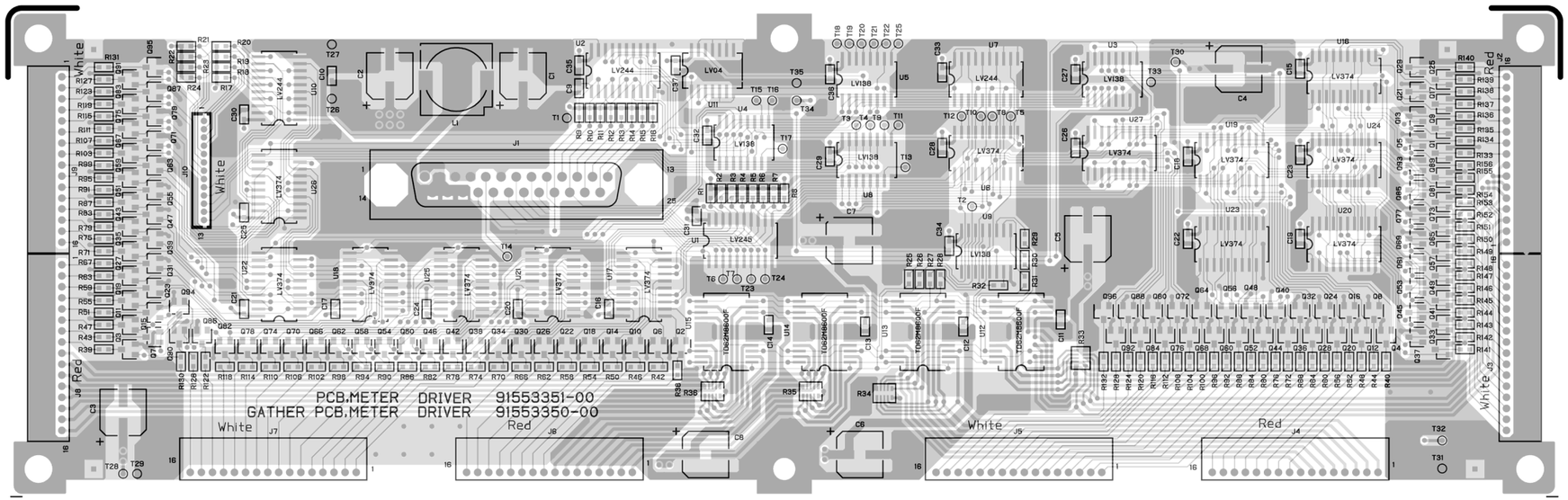
SIDE B



## GATHER PCB,METER BRIDGE (MASTER METER PCB, INPUT METER PCB) (OPTION)




## METER DRIVER PCB (OPTION)



# INCLUDED ACCESSORIES
付属品

## INCLUDED ACCESSORIES

| REF.NO. | PARTS NO. | DESCRIPTION | REMARKS |
|---|---|---|---|
| | *9101439600 | OWNER'S MANUAL(JPNANESE) [J] | |
| | *9101439700 | OWNER'S MANUAL(ENGLISH) [EXCEPT J] | |

**DM-24 Service Support Manual (2001.10.15 Update)**

1. SRAM Data

Routing Data: I/O Screen, Assign Screen
Grouping Data: Group Screen
Mixing Data: Module Screen, Effect Screen, Dynamics Screen, Pan/Bal Surround Screen, Digital Trim Screen, Delay Screen, Aux1-2/3-4/5-6 Screen
System Data: Option Screen, Digital Screen, MIDI/MC Screen, Automation Screen, Link Screen, Monitor Screen, Meter/Fader Screen

2. Flash Data Library(FLASH ROM U7)

EQ Library: 20 Preset: 108 User Data
Gate Library: 20 Preset: 108 User Data
Comp Library: 20 Preset: 108 User Data
Effect Library: 1006 TC Works: 2 Anters: 128 Tascam: 128 User Data
Snapshot Library(Routing + Grouping + Mixing): 4 Preset: 96 User Data

3. Special Message Popup

Panel Fatal (Output Queue Overflow)
This indication means that Errors Panel Queue.

| |
|---|
| Fatal Error:<br>PP-xxxxxxxx-00<br><br>Please note for reference |

Panel Fatal (Input Queue Overflow)
This indication means that Errors Panel Queue.

| |
|---|
| Fatal Error:<br>PP-xxxxxxxx-05<br><br>Please note for reference |

Panel Fatal (Flash ROM Update Error)
This indication means that Errors Panel Update.

| |
|---|
| Fatal Error:<br>PP-xxxxxxxx-06<br><br>Please note for reference |

Panel Fatal (Popup Message Error)
This indication means that Errors Display Message.

```
Fatal Error:
PP-xxxxxxxx-07

Please note for reference
```

Panel Fatal (Hardware)
This indication means that Panel CPU Errors.

```
Fatal Error:
PP-xxxxxxxx-09

Please note for reference
```

Panel Fatal (Hardware)
This indication means that Panel CPU Errors.

```
Fatal : Address Error
PC=xxxxxxxx SP=xxxxxxxx SP=xxxxxxxx
Stack=xxxxxxxx

xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
```

Panel Fatal(Hardware)
This indication means that Panel CPU Errors.

```
Fatal : Illegal slot Instruction
PC=xxxxxxxx SP=xxxxxxxx SP=xxxxxxxx |
Stack=xxxxxxxx

xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
```

Panel Fatal(Hardware)
This indication means that Panel CPU Errors.

```
Fatal : General Illegal Instruction at
PC=xxxxxxxx SP=xxxxxxxx SP=xxxxxxxx
Stack=xxxxxxxx

xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
```

Under 5 volts
This indication means that Under 5 volts.

```
Power Supply Voltage (+5V) is too Low
for stable operation.

Please Restart DM-24.
```

Main Fatal (Boot)
This indication means that Main Boot Errors.

```
Fatal Error:
00-xxxxxxxx-00

Please note for reference
```

Main Fatal (Hardware)
This indication means that Main CPU Errors.

```
Fatal Error:
00-xxxxxxxx-01

Please note for reference
```

Main Fatal (Software)
This indication means that Main Software Errors.

```
Fatal Error:
xx-xxxxxxxx-xx

Please note for reference
```

Main Fatal(DSP)
This indication means that DSP Errors.

```
NaN Occurred on the DSP
```

Sram Data Error
This indication means that SRAM Data breaks.

```
Out of Sram Range !
Initialize Sram Data?
   xxch(xxx) xxxxxxxxxxxxx

Press ENTER to confirm,
or a cursor key to cancel.
```

Effect Read Timeout
This indication means that Effector Hardware Errors.

```
Wait_for_read_ready_flag xx time out !
```

Effect Write Timeout
This indication means that Effector Hardware Errors.

```
Wait_for_write_ready_flug xx time out !
```

Effect Load Error
This indication means that Effecter Loading Errors.

```
Effect Plug-in Load Incomplete

TC works : Error
Antures   : Error
TASCAM : Error

Check Version Information
```

# TASCAM DM-24, Main PCB Assy Troubleshooting

It is recommended to read following documents (downloadable from SVHP) with this troubleshooting. These docs will contribute to a better understanding of Main PCB Assy.

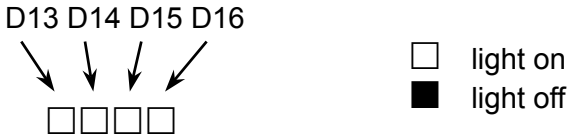
*Brief explanation on circuit diagram*
*Block diagram for Main PCB Assy*
*Block diagram for IOX*
*Block diagram for DSP*
*DSP architecture1*
*DSP architecture2*

1. PANEL CPU Boot Error [Circuit Diagram Main PCB 2/13]

If LED, LCD or fader does not work correctly, Panel CPU boot error is thought.

- Soldering on Panel CPU (U33), DRAM (U32), ROM Socket (U31).
- Soldering on RA7, RA8, RA10, R32, R33.
- Reset signal for Panel CPU (U33-84).
- Clock for Panel CPU (U33-74, 7056kHz).
- Signals on Data Bus (PD[15:0]), Address Bus (PA[19:0]), RD (#PRD), WR (#PWR).
- Replace DRAM (U32).
- Replace Panel CPU (U33).

On the Main PCB Assy (top side), there are 4 LEDs, D13-D16. When powering on, these LEDs will light on/off and finally all go to off. In case there is a problem during boot, these LED will show a particular pattern that can be used for troubleshooting.




2. □□□□ MAIN CPU Boot Error [Circuit Diagram Main PCB 1/13]

- Soldering on Main CPU (U11), SRAM (U8), DRAM (U10), ROM Socket (U6, U7).
- Soldering on RA2, RA3, RA4 and RA5.
- Reset signal for Main CPU (U11-84).
- Clock for Main CPU (U11-74, 7056kHz).
- Signals on Data Bus (MD[15:0]), Address Buss (MA[20:0]), RD (#MRD), WR (#MWR)
- Replace DRAM (U10).
- Replace Main CPU (U11).

3. ■■■■ DUAL PORT RAM, Communication Error with PANEL CPU
[Circuit Diagram Main PCB 2/13]

● Soldering on Dual Port RAM (U28), R26, R28, DRAM (U32).
● Signals on Data Bus (PD[15:0]), Address Bus (PA[19:0])
● Replace DRAM (U32).
● Replace Dual Port RAM (U28).
● Replace Panel CPU (U33).

4. □■■■ SRAM (U8) [Circuit Diagram Main PCB 1/13]

● Initialize SRAM.
● Soldering on SRAM.
● Replace SRAM.

5. ■■■□ DSP1 (U77), DSP2 (U78) [Circuit Diagram Main PCB 6/13]

● Soldering on U13, U14, U77, U78.
● Soldering on PLD (U160).
● Soldering on Resistor Array, R122, R124.
● Reset signal for U77-157 and U78-157.
● Clock for U77-30 and U78-30 (30MHz).
● Replace U77.
● Replace U78.

6. □■■□ DSP2 (U78) [Circuit Diagram Main PCB 6/13]

● Soldering on U78.
● Replace U78.

7. ■□■□ DSP3 (U87), DSP4 (U88) [Circuit Diagram Main PCB 7/13]

● Soldering on U87, U88.
● Soldering on Resistor Array, R150, R151.
● Reset signal for U87-157 and U88-157.
● Clock for U87-30 and U88-30 (30MHz).
● Replace U87.
● Replace U88.

8. □□■□ DSP4 (U88) [Circuit Diagram Main PCB 7/13]

● Soldering on U88.
● Replace of U88.

9. ■■□□ DSP5 (U94), DSP6 (U95) [Circuit Diagram Main PCB 8/13]

- Soldering on U94, U95.
- Soldering on Resistor Array, SDRAM (U96, U97), R162, R166.
- Reset signal for U94-157 and U95-157.
- Clock for U94-30 and U95-30 (30MHz).
- Replace U94.
- Replace U95.

10. □■□□ DSP7 (U106) [Circuit Diagram Main PCB 9/13]

- Soldering on U107, U106, U105.
- Soldering on Resistor Array, R196.
- Check soldering bridge on vacant patterns (U113 and so on).
- Reset signal for U106-157.
- Clock for U106-30 (30MHz).
- Replace U106.

11. DSPs boot up but no sound or distorted sound.

- +5V for AD/DA (Connector P30-3/4, A+5V).
- Clock for AD/DA (LRCK/BCLK/256Fs/512Fs). *Circuit Diagram Main PCB 11/13, A7-C7*
- Sound is distorted if there is cold soldering or solder bridge on the serial signal line connecting DSPs. See "DSP Block Diagram" to confirm the sound on each signal routes.
- ADC (ch1-16) and all DAC are inputted/outputted by DSP1 (U77) through IOX. ADC (meter, TB-MIC) and Digital I/O are handled by DSP3 (U87) and DSP4 (U88). If no problem on digital I/O, cause of problem must be on DSP1 or IOX. In this case, go to 12.
- SDRAM (U96, U97) on DSP5 (U94) are working for channel delay. Even if delay=OFF, signals go through SDRAM. In case both of "Analog IN (ch1-16) → Stereo OUT" and "Digital IN → Digital OUT" are distorted, there is a possibility on DSP5, DSP6, SDRAM.
- OSC is handled by DSP6. If OSC signal is outputted from DAC normally, it is judged that signal route of “DSP6 → DSP7 → DSP1 → IOX → DAC” is working.
- If sound is distorted with EFFECTOR using, DSP7 (U106) is suspected. After DSPs boot, if "Init Flag never went to 0" is displayed in LCD, it means that LRCK has not come to U106-206.

12. No sound or distorted sound related to DSP1 or IOX.

- Soldering on U74, U75, U76.
- Clock (512Fs) for U160-19, pin21 of IOX (U71, U72, U73).
- LRCK (inverted) for pin27 of IOX (U71, U72, U73).
- Confirm DSP1 Data Bus (D8-D23) triggered by LRCK. Only D0-D7 is used for DSP boot, then, it can boot even if D8-D23 have solder bridge.
- Check PLD (U160).

# DM-24 MAIN PCB BLOCK DIAGRAM

Contents of the circuit schema


PAGE 1 MAIN CPU
PAGE 2 PANEL CPU
PAGE 3 BUFFER for SLOTs
PAGE 4 INPUT SELECTOR for IOXs
PAGE 5 IOXs
PAGE 6 DSP1 & DSP2
PAGE 7 DSP3 & DSP4
PAGE 8 DSP5, DSP6 & SDRAMs
PAGE 9 DSP7 (for EFFECTOR)
PAGE 10 DSP8 (RESERVE)
PAGE 11 PLL & DIGITAL I/O
PAGE 12 ADCs for 1-16 inputs
PAGE 13 CODECs & ADC for TBM


PAGE 1
PORT G
PORT H
PORT I
74LV273 (U23)
74LV273 (U24)
74LV273 (U1)
MAIN CPU DATA BUSS
RESET_MAIN
BATTERY
CR2032
MAIN CPU (U11)
LAS*
CASL*
CASH*
RD/WR*
RES*
A0-20 D0-15 EXTAL
DRAM (U10) 16Mbit
A1-10 D0-15
SRAM (U8) 256kbit
A0-11 D0-7
F.ROM (U6) 8Mbit
F.ROM (U7) 8Mbit
A1-20 D0-15
RP*
MAIN CPU ADDRESS BUSS
MAIN CPU DATA BUSS
Time Cord
TC IN
uPD65013 (U2)
SYCK
CLOCK 7.056MHz
7.056MHz (X1)
PAGE 11
PLL CIRCUIT
U133 - U136
XC9536XL for PLL (U125)
GCK2
Dual Port RAM (U28) 8kbit
A0-9 D0-7
RESET_MAIN

PAGE 4
PORT J
74LV273 (U70)
PAGE 11
PORT K
PORT L
PORT M
PORT N
74LV273 (U122)
74LV273 (U123)
74LV273 (U137)
74LV273 (U124)
PAGE 4
PORT O
74HC540 (U61)

Hi Speed SRAM (U13) 256kbit
Hi Speed SRAM (U14) 256kbit
A0-11
D8-15
Common RAMs for MAIN CPU & six DSPs.
74LV541 (U17)
74LV541 (U18)
74LV245 (U15)
74LV245 (U16)
A1-8
A9-15

PAGE 6
74LV541 (U82)
74LV541 (U83)
74LV245 (U84)
74LV245 (U85)
A0-7
A8-14
DSP1 (U77)
DSP2 (U78)
CLKIN
D0-31 A0-23
DSPA_A0-23
DSPA_D0-31
30MHz (X2, U79&U80)
CLOCK 30MHz

PAGE 5
XC9536XL for IOX (U160)
A4, 5
74LV245 (U74)
74LV245 (U75)
74LV245 (U76)
D0-7
D8-15
D15-23
IOX_D0-23
IOX1 (U71)
IOX2 (U72)
IOX3 (U73)
A0-3
A0-1
D0-23
MAIN CPU DATA BUSS

RESERVE
DSP8 CIRCUIT
U113 - U119
PAGE 10

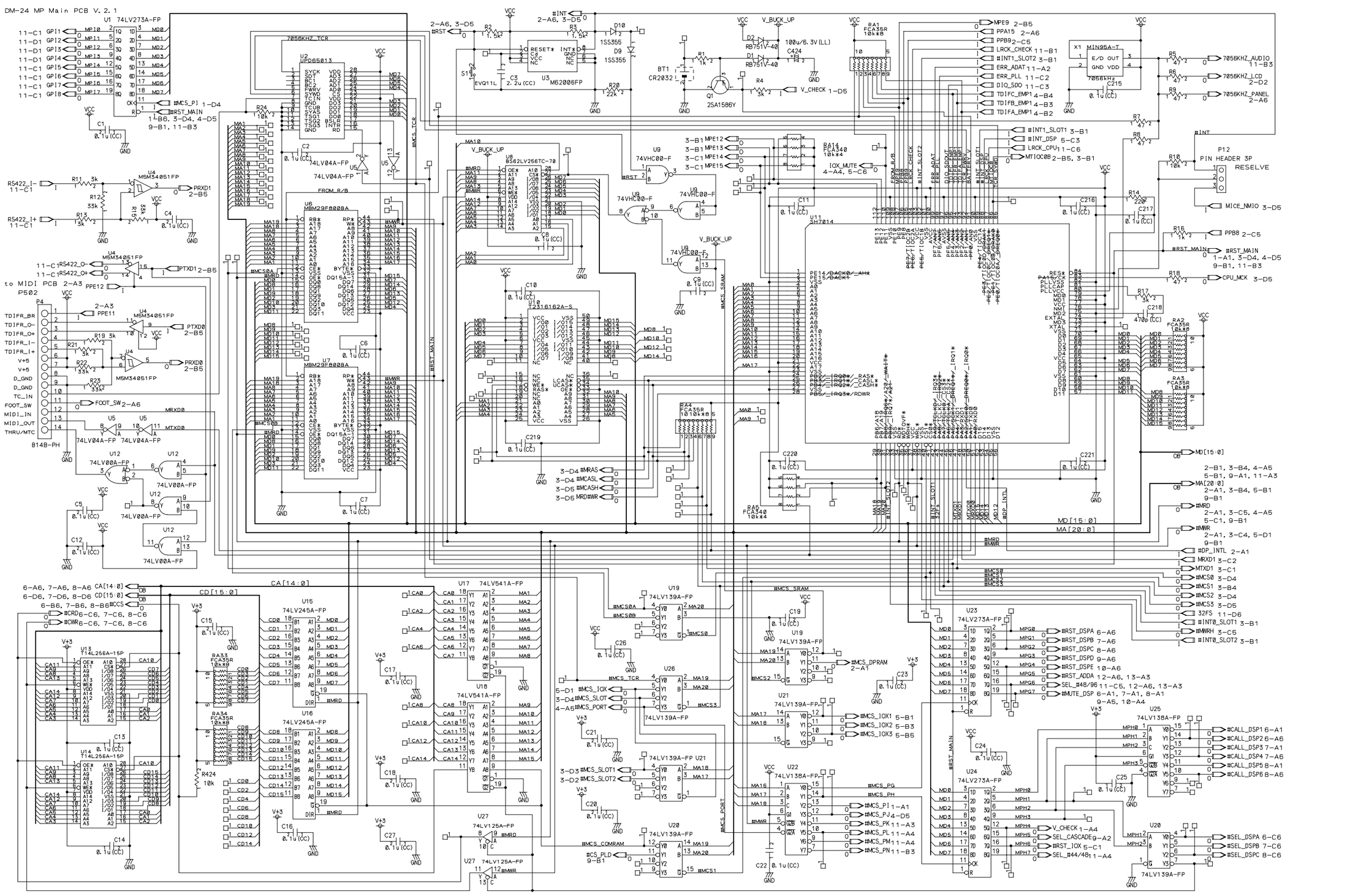
PAGE 7
74LV541 (U90)
74LV541 (U91)
74LV245 (U92)
74LV245 (U93)
DSP3 (U87)
DSP4 (U88)
DSPB_A0-23
DSPB_D0-31
TS CLK
Q3
to FADER PCB via P10

Hi Speed SRAM (U109) 1Mbit
Hi Speed SRAM (U110) 1Mbit
Hi Speed SRAM (U111) 1Mbit
Hi Speed SRAM (U112) 1Mbit
D16-23
D24-31

DSP7 (U106)
A0-16 D0-31
DSPD_D0-31
DSPD_A0-16
D0-15
CLOCK 30MHz for DSP7
74ALVCH 16543 (U107)
Control
GCK1 I/O
XC9572XL for DSP (U105)
GSR
A1-3
RESET_MAIN

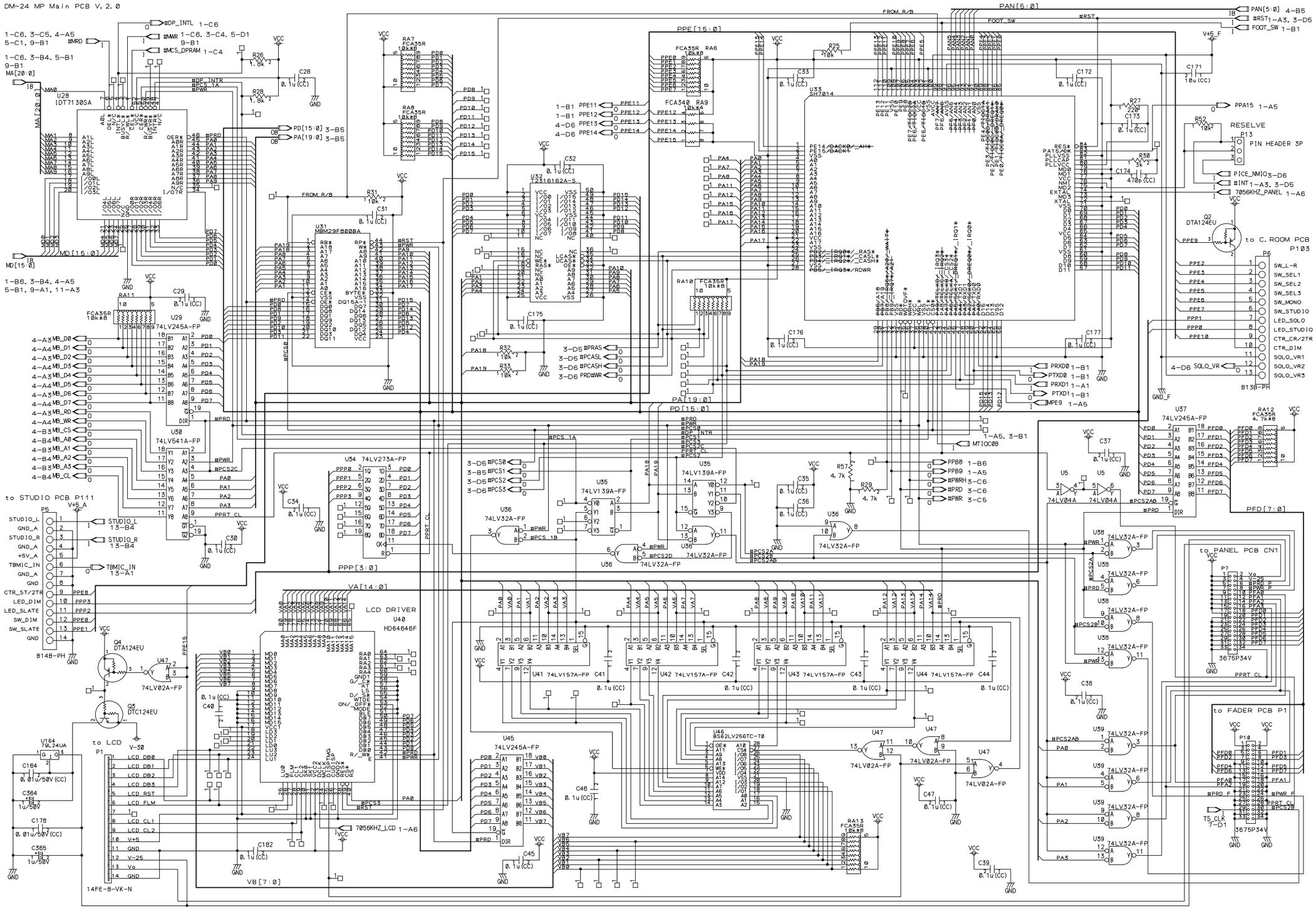
PAGE 8
74LV541 (U99)
74LV541 (U100)
74LV245 (U101)
74LV245 (U102)
DSP5 (U94)
DSP6 (U95)
SDRAM (U96) 16Mbit
SDRAM (U97) 16Mbit
SDRAM_IFC0-7
D0-15 A1-9,13
D16-31 A1-9,13
DSPC_A0-23
DSPC_D0-31
74LV574 (U108)
74LV245 (U142)
74LV245 (U146)
PAGE 9
COMMON DATA BUSS
COMMON ADDRESS BUSS
MAIN CPU ADDRESS BUSS
MAIN CPU DATA BUSS

PANEL CPU DATA BUSS
PANEL CPU ADDRESS BUSS
PANEL CPU (U33)
A0-19 D0-15 EXTAL
PB8
DRAM (U32) 16Mbit
F.ROM (U31) 8Mbit
PORT P
74LV273 (U34)
74LV245 (U45)
RESET (U3)
RESET
PANEL CPU ADDRESS BUSS
LCD DRIVER (U40)
RES* DCLK
to LCD MODULE via P1
LCD DATA BUSS
74LV157 (U41)
74LV157 (U42)
74LV157 (U43)
74LV157 (U44)
A0-3
A4-7
A8-11
A12-14
LCD ADDRESS BUSS
SRAM (U46) 256kbit
A0-14
PAGE 2



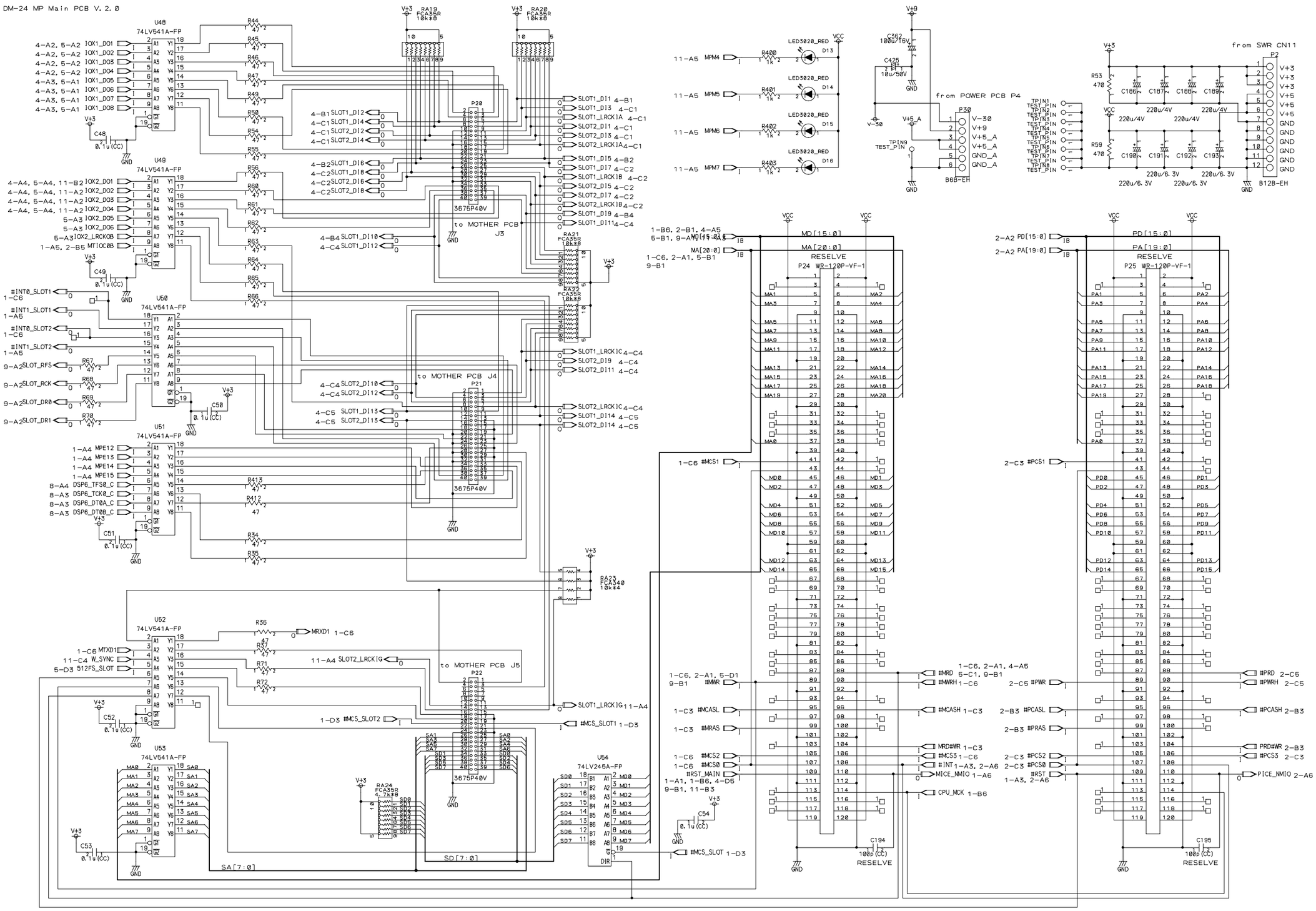

# Digital Mixing Console DM-24

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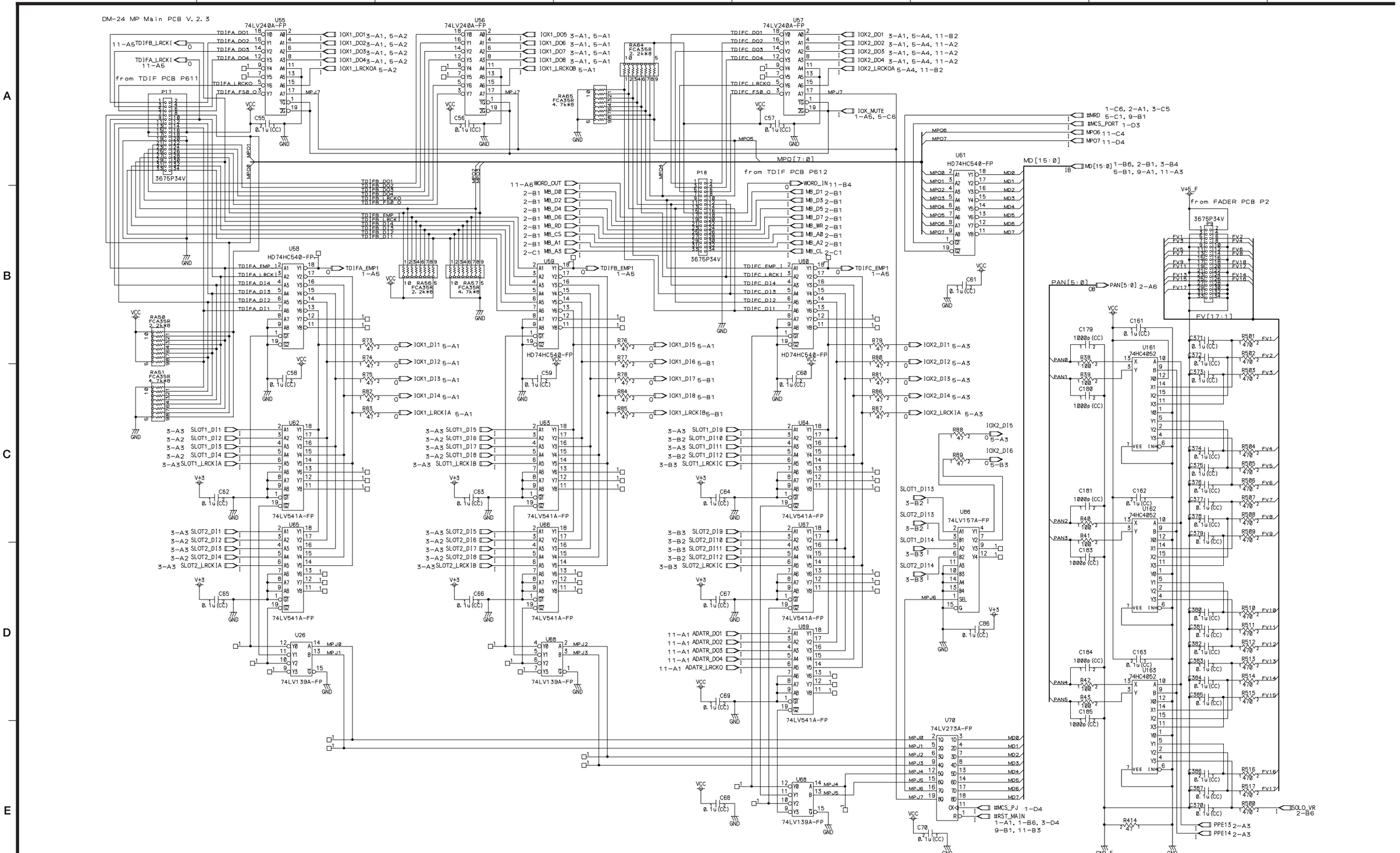
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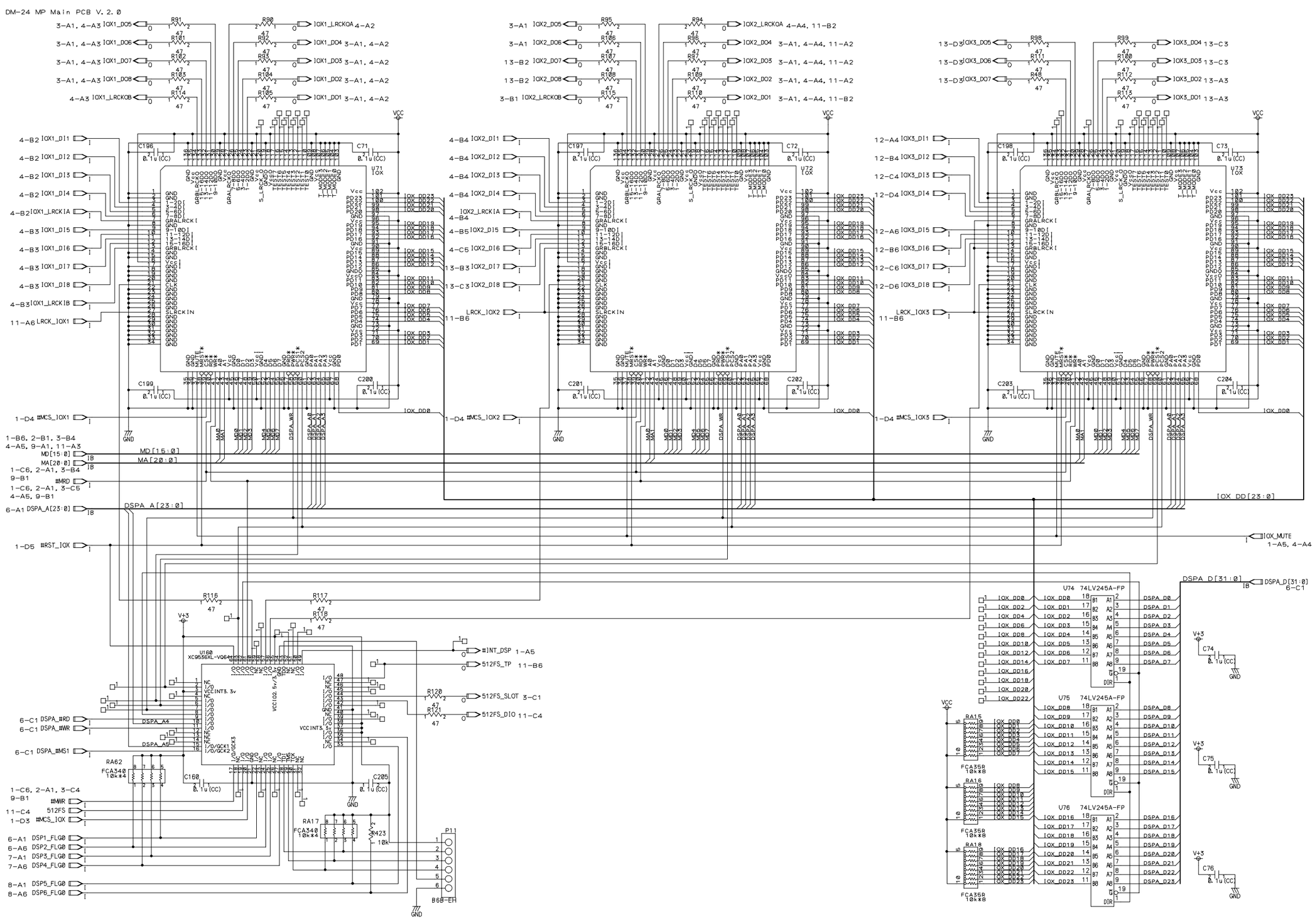
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# SCHEMATIC DIAGRAM DM-24 MAIN PCB (4/13)



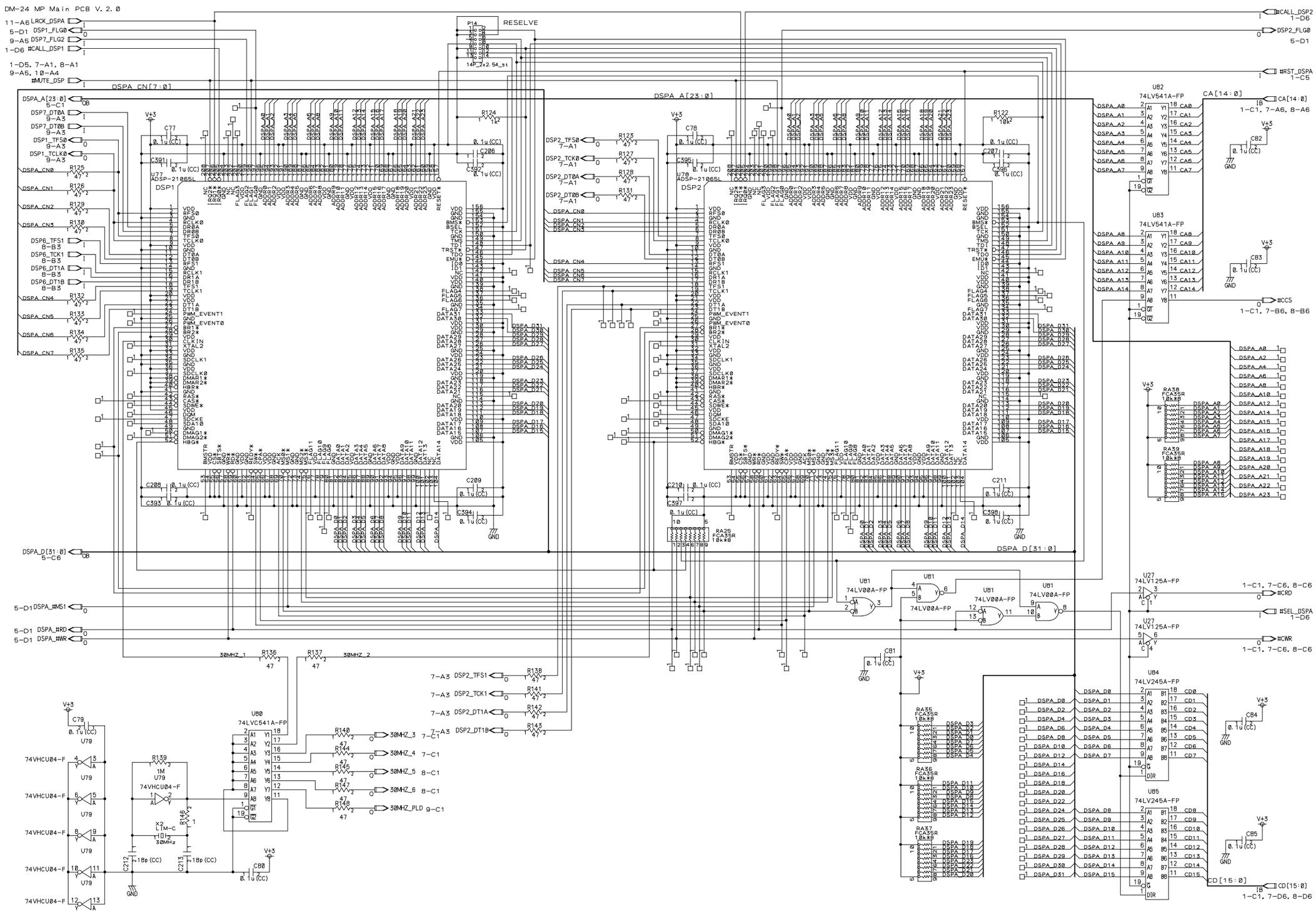

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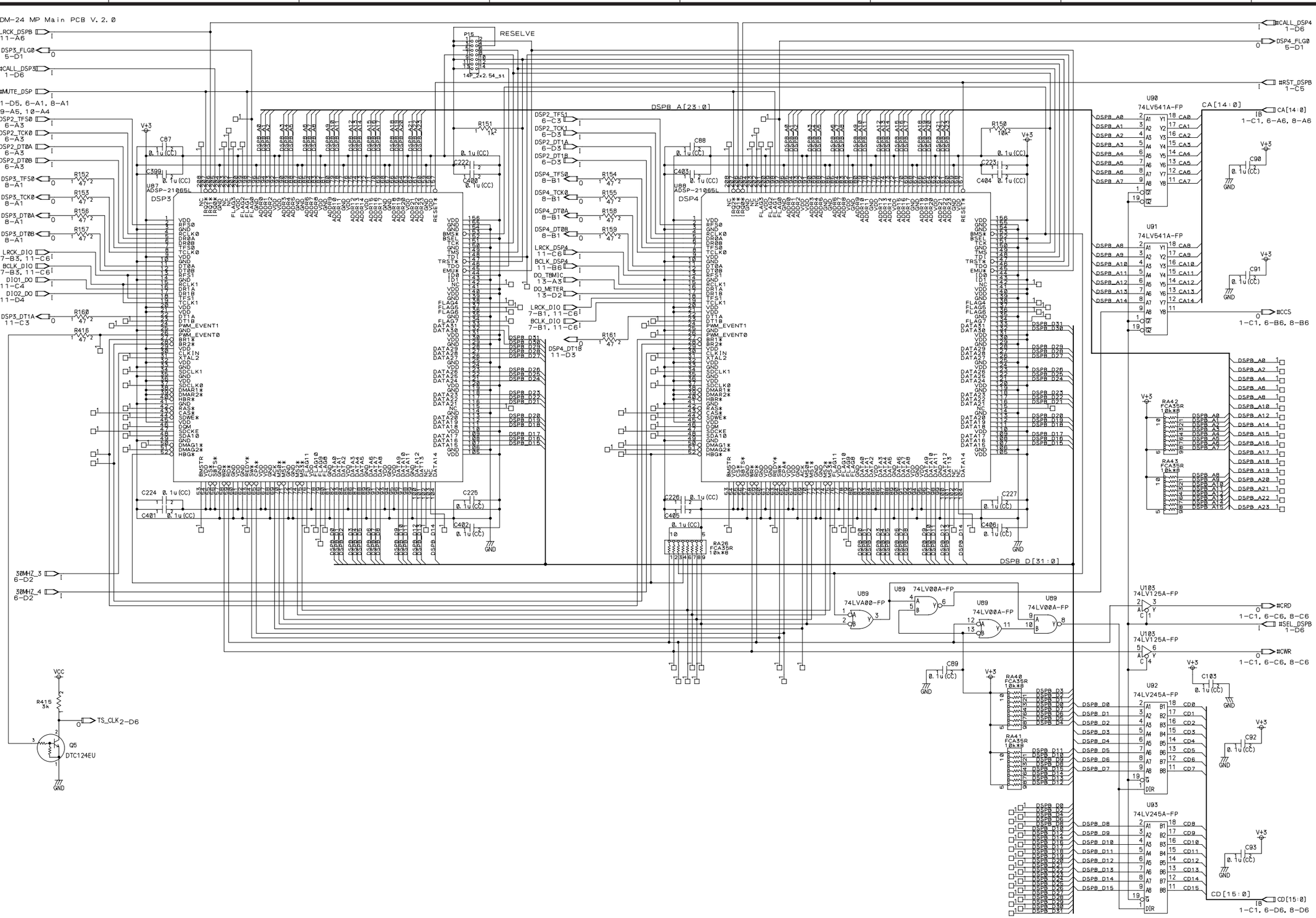

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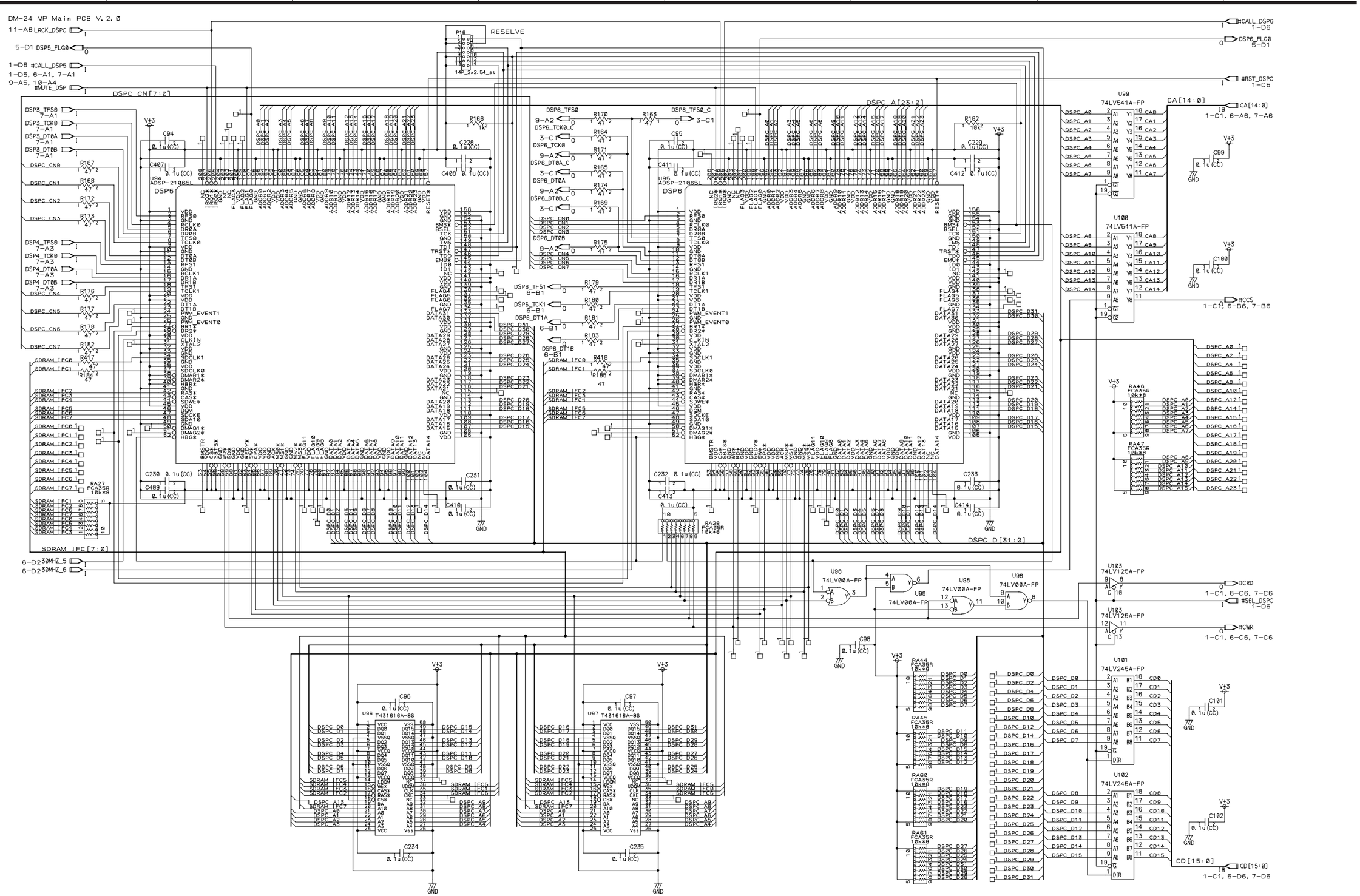

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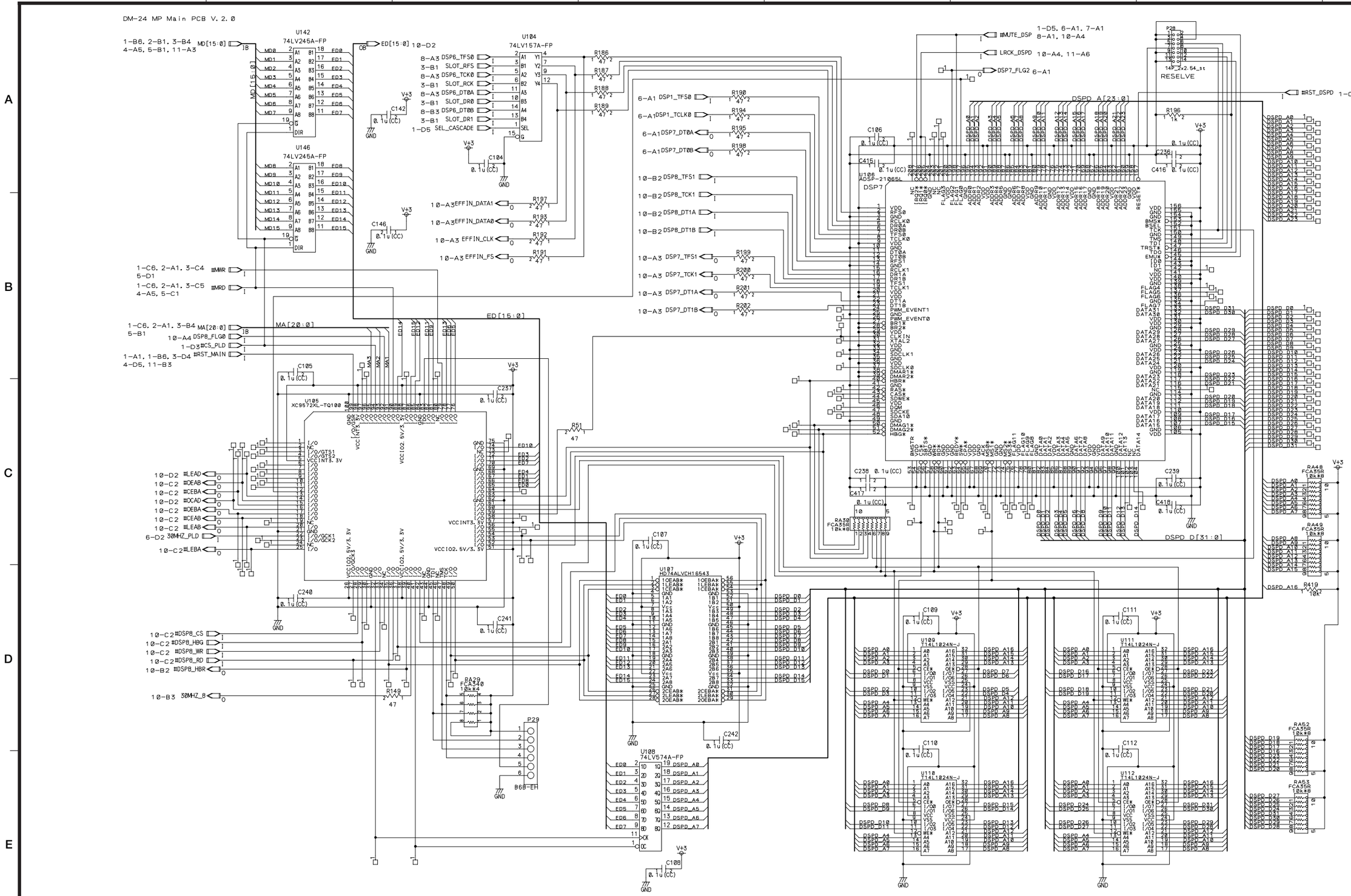
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# Digital Mixing Console DM-24

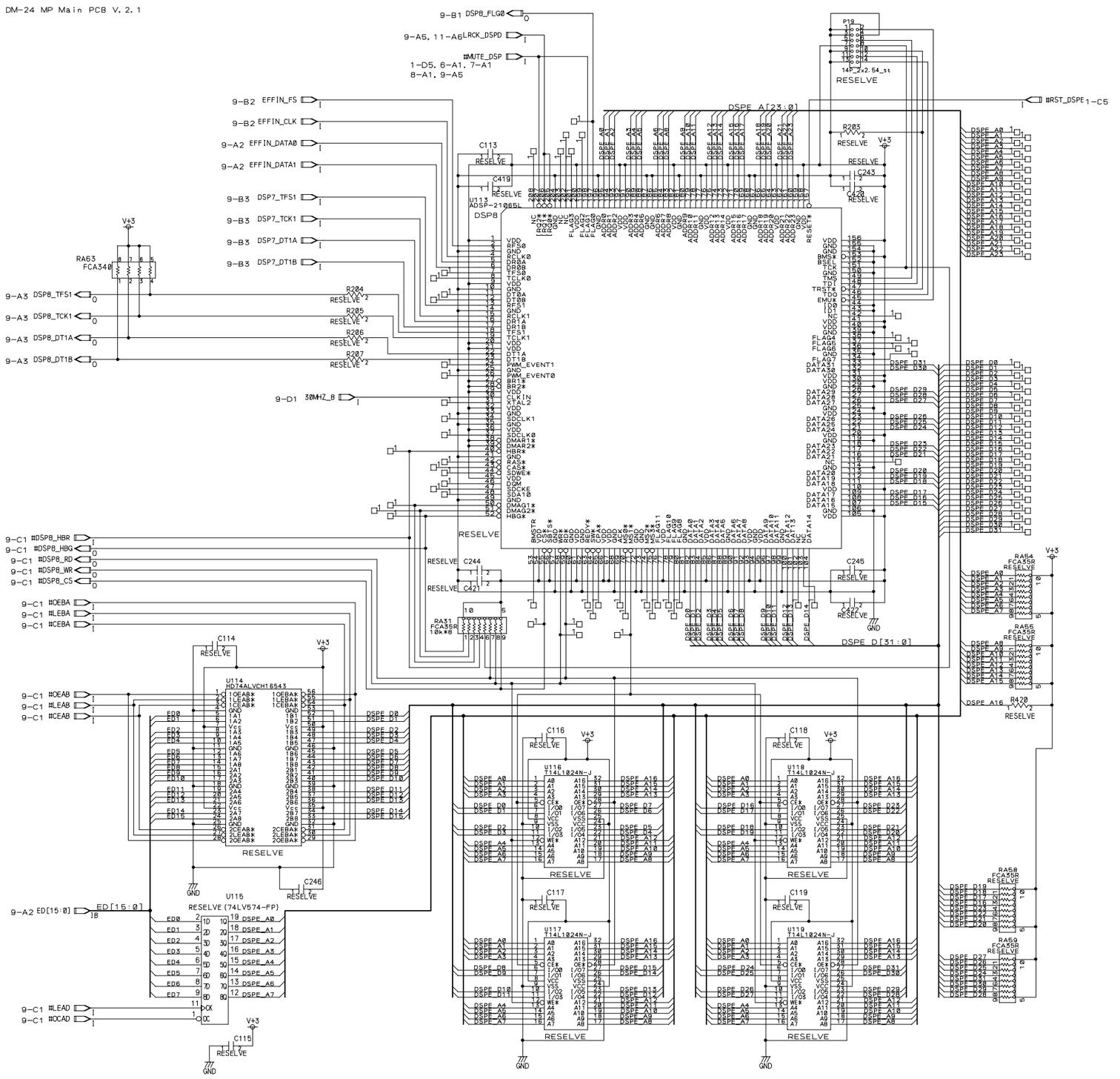
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DM-24 MP Main PCB V.2.0
DSPC CN[7:0]
DSPC A[23:0]
DSPC D[31:0]
SDRAM IFC[7:0]
RESELVE
U94 ADSP-21065L
DSP5
U95 ADSP-21065L
DSP6
U96 T451616A-8S
U97 T451616A-8S
U98 74LV00A-FP
U99 74LV541A-FP
U100 74LV541A-FP
U101 74LV245A-FP
U102 74LV245A-FP
U103 74LV125A-FP
CA[14:0]
CD[15:0]
30MHZ_5
30MHZ_6
V+3
GND




# Digital Mixing Console DM-24

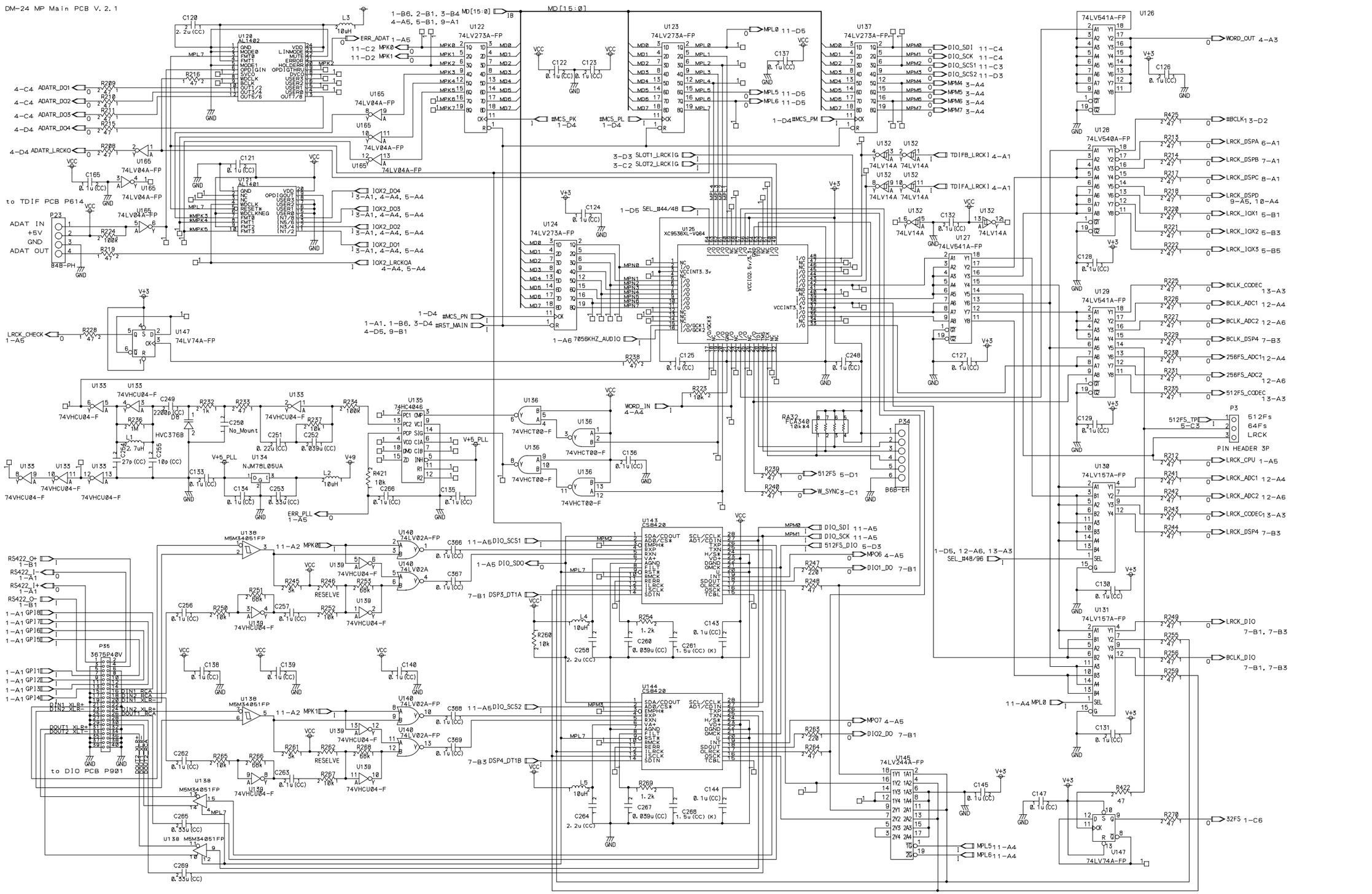
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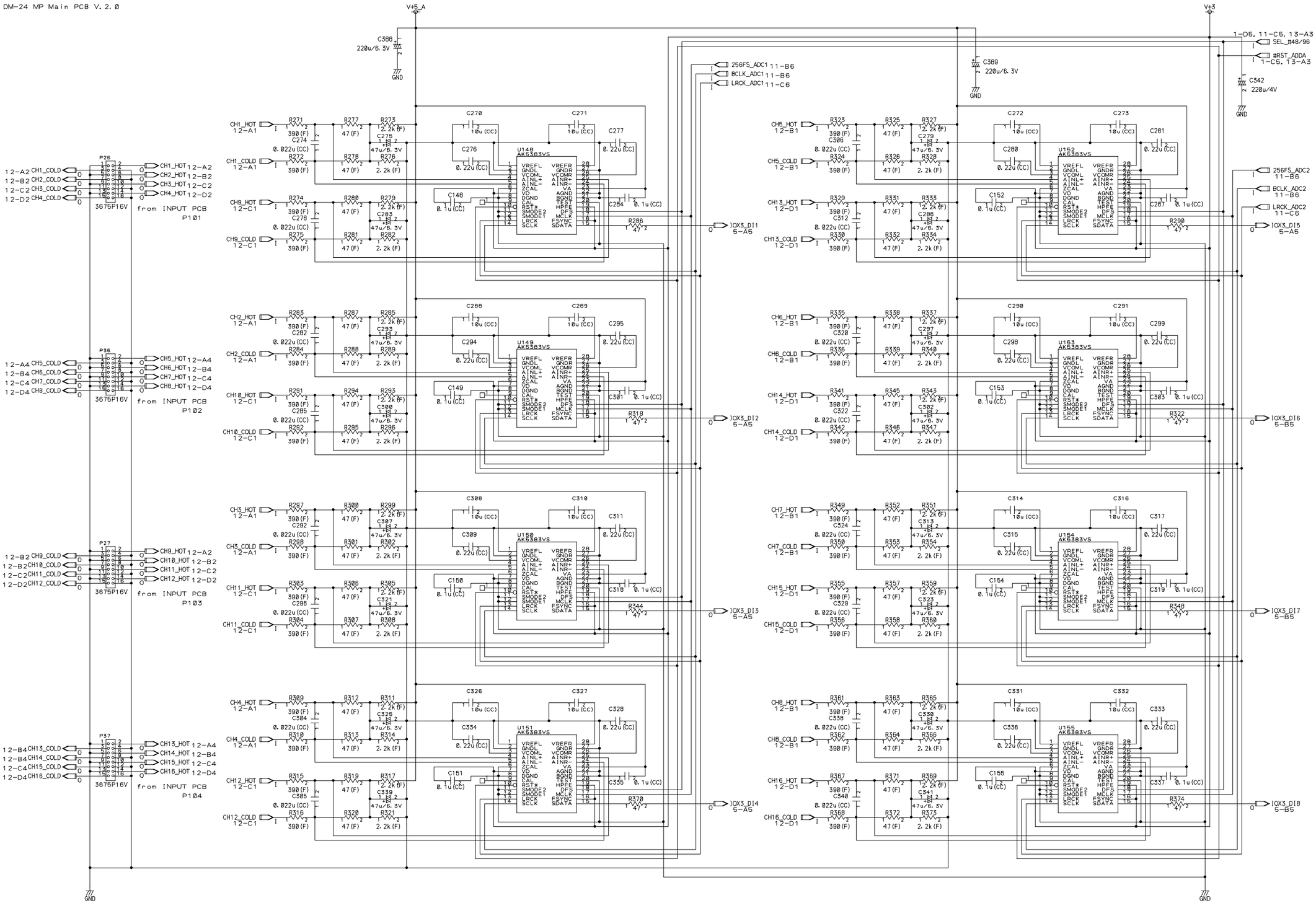

# Digital Mixing Console DM-24

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# SCHEMATIC DIAGRAM DM-24 MAIN PCB (11/13)



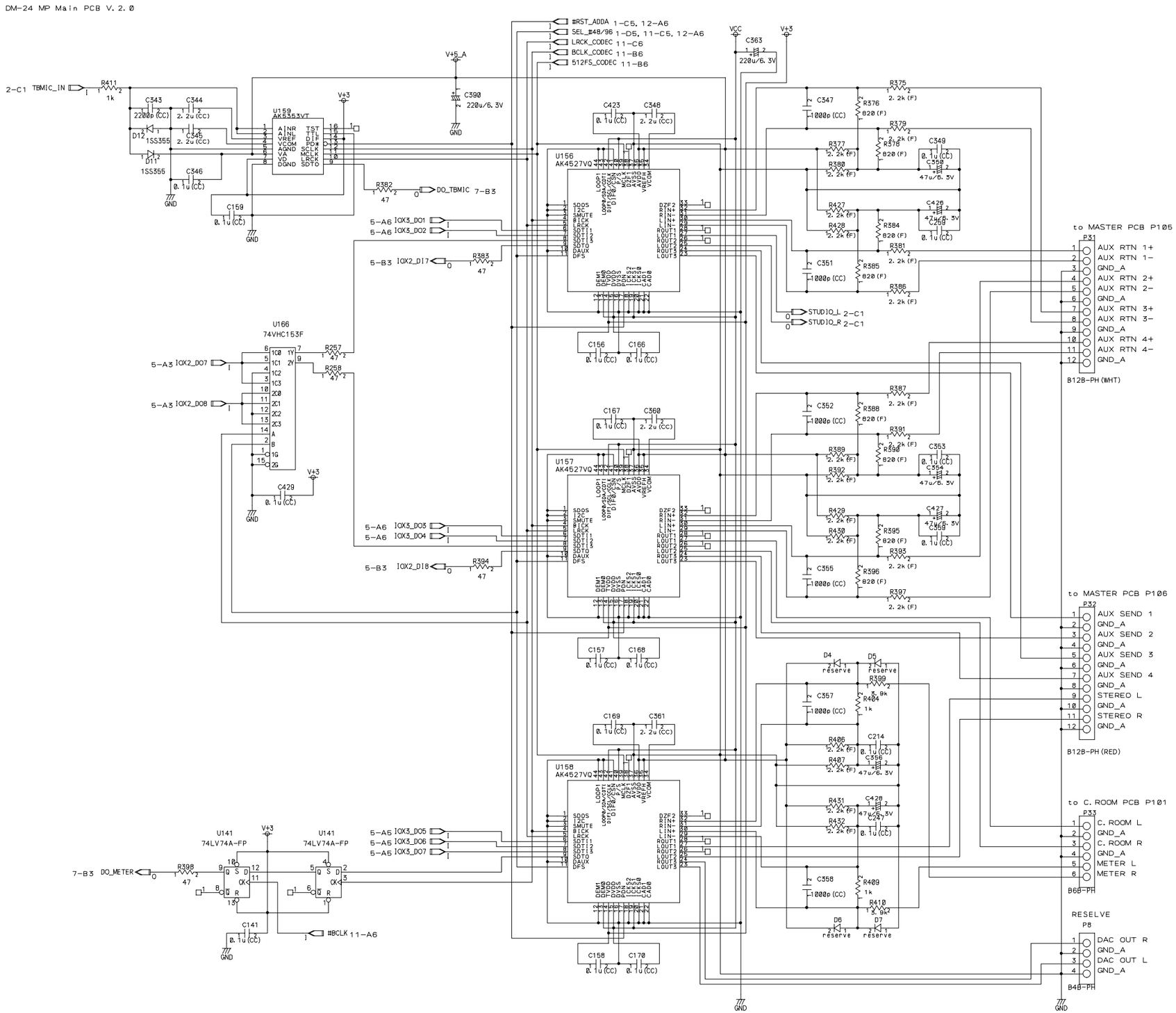
DM-24 MP Main PCB V.2.0




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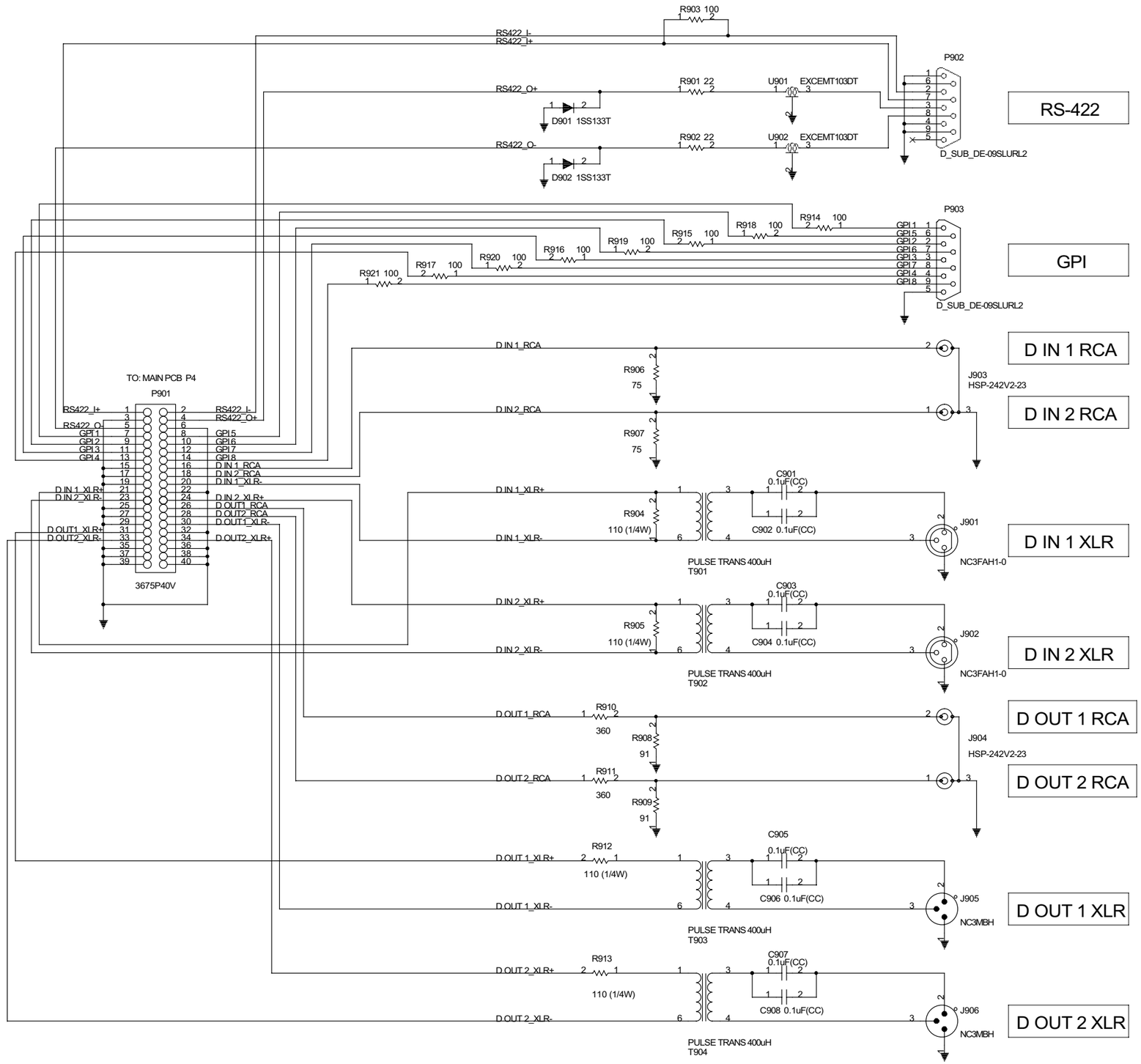
DM-24 MP Main PCB V.2.0




# Digital Mixing Console DM-24

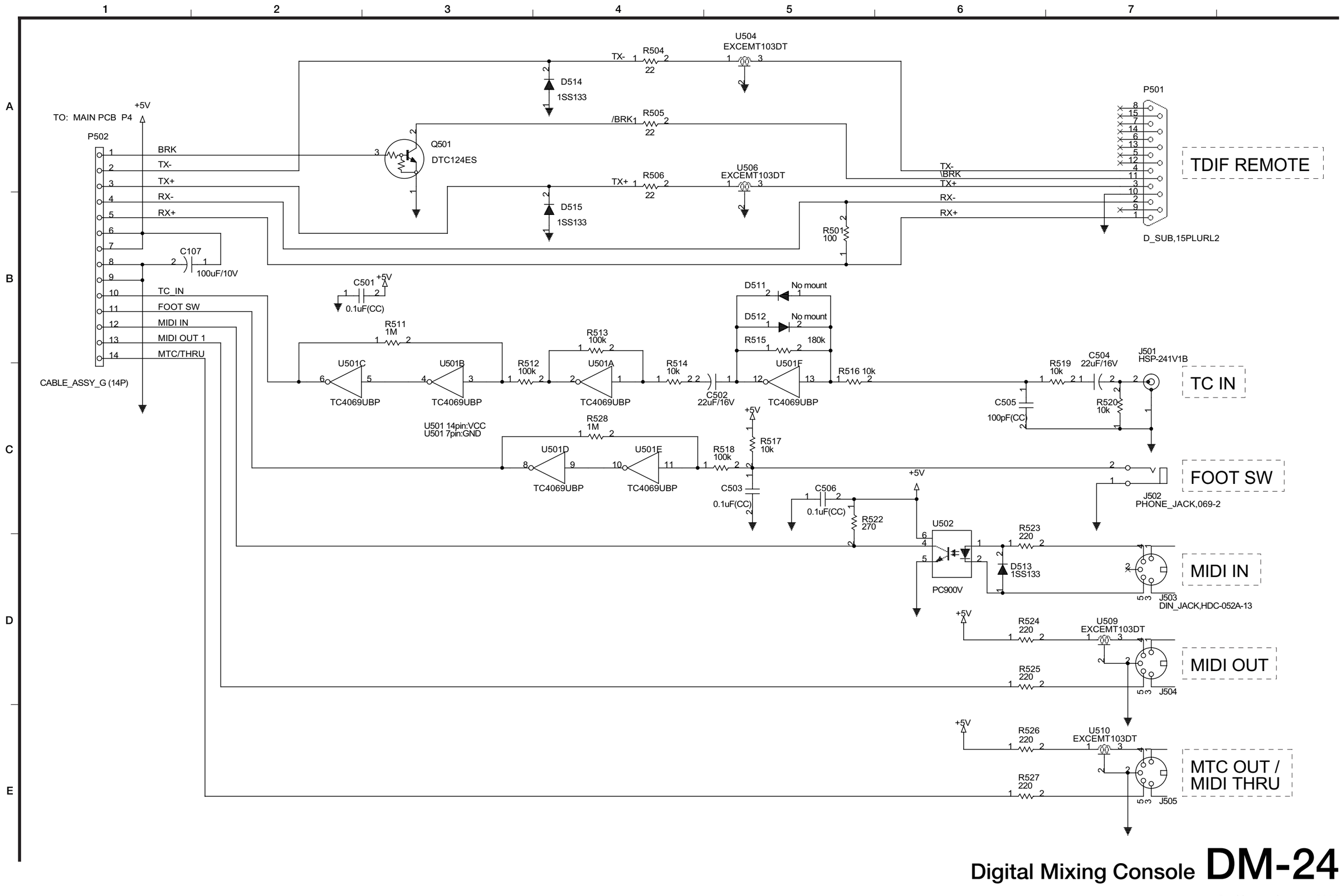
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# SCHEMATIC DIAGRAM DM-24 DIGITAL I/O PCB




## Digital Mixing Console DM-24

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Digital Mixing Console **DM-24**

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1 2 3 4 5 6 7

A B C D E

1SS133 * 28

D613 D611 D609 D607 D605 D603 D601
D614 D612 D610 D608 D606 D604 D602

RA1
No Mount

R601
1.5k

P601

TDIF1 DO 1/2
TDIF1 DO 3/4
TDIF1 DO 5/6
TDIF1 DO 7/8
TDIF1 LRCK O
TDIF1 FS0 I
TDIF1 FS1 I
TDIF1 FS0 I
TDIF1 EMP I
TDIF1 LRCK I
TDIF1 DI 7/8
TDIF1 DI 5/6
TDIF1 DI 3/4
TDIF1 DI 1/2

R602 47
R603 47
R604 47
R605 47
R606 47
R607 47
R608 47
R609 47
R610 47
R611 47
R612 47
R613 47
R614 47
R615 47

D-SUB 205A-25FSTBBB3

TDIF 1

RA2
No Mount

D627 D625 D623 D621 D619 D617 D615
D628 D626 D624 D622 D620 D618 D616

TO: MAIN PCB P17
P611
3675P34V

1SS133 * 28

D641 D639 D637 D635 D633 D631 D629
D642 D640 D638 D636 D634 D632 D630

RA3
No Mount

R616
1.5k

P602

TDIF2 DO 1/2
TDIF2 DO 3/4
TDIF2 DO 5/6
TDIF2 DO 7/8
TDIF2 LRCK O
TDIF2 FS0 O
TDIF2 FS1 I
TDIF2 FS0 I
TDIF2 EMP I
TDIF2 LRCK I
TDIF2 DI 7/8
TDIF2 DI 5/6
TDIF2 DI 3/4
TDIF2 DI 1/2

R617 47
R618 47
R619 47
R620 47
R621 47
R622 47
R623 47
R624 47
R625 47
R626 47
R627 47
R628 47
R629 47
R630 47

D-SUB 205A-25FSTBBB3

TDIF 2

RA4
No Mount

D655 D653 D651 D649 D647 D645 D643
D656 D654 D652 D650 D648 D646 D644

| MAIN PCB Version | 00 or 01 | 02 or LATER |
|---|---|---|
| RA1 | 2.2k * 8 | Needless |
| RA2 | 4.7k * 8 | Needless |
| RA3 | 2.2k * 8 | Needless |
| RA4 | 4.7k * 8 | Needless |
| RA5 | 2.2k * 8 | Needless |
| RA6 | 4.7k * 8 | Needless |
| LRCK PCB | Use | Needless |

L601
47uH_EC24-470K-T5-70MA

L602
47uH_EC24-470K-T5-70MA

R663
3.3k

R664
47

C601
0.1uF(CC)

C602
0.1uF(CC)

C603
100uF/10V

P614
TO: MAIN PCB P23
FLAT CABLE_ASSY_L (4P)

U601
Vcc
GND
Vout
OPT IN
GP1FA550RZ

ADAT IN

U602
Vin
Vcc
GND
OPT OUT
GP1FA550TZ

ADAT OUT

1SS133 * 28

D669 D667 D665 D663 D661 D659 D657
D670 D668 D666 D664 D662 D660 D658

RA5
No Mount

R631
1.5k

P603

TDIF3 DO 1/2
TDIF3 DO 3/4
TDIF3 DO 5/6
TDIF3 DO 7/8
TDIF3 LRCK O
TDIF3 FS0 O
TDIF3 FS1 I
TDIF3 FS0 I
TDIF3 EMP I
TDIF3 LRCK I
TDIF3 DI 7/8
TDIF3 DI 5/6
TDIF3 DI 3/4
TDIF3 DI 1/2

R632 47
R633 47
R634 47
R635 47
R636 47
R637 47
R638 47
R639 47
R640 47
R641 47
R642 47
R643 47
R644 47
R645 47

D-SUB 205A-25FSTBBB3

TDIF 3

RA6
No Mount

D683 D681 D679 D677 D675 D673 D671
D684 D682 D680 D678 D676 D674 D672

TO: MAIN PCB P18
P612
3675P34V

WORD SYNC IN

R701
47

U701C
TC74VHCT00

U701D
TC74VHCT00

75Ω OFF / 75Ω ON

R646
75

SW601
SSSF123-S06N0

D685
1SS133

J601
COH2201-A

J602
COH2201-A

THRU / OUT

WORD SYNC OUT

U604
EXCEMT101DT

WORD SYNC OUT / THRU

P604

D0
D1
D2
D3
D4
D5
D6
D7
*RD
*WR
*CS
A0
A1
A2
A3
*EN

R647 100
R648 100
R649 100
R650 100
R651 100
R652 100
R653 100
R654 100
R655 100
R656 100
R657 100
R658 100
R659 100
R660 100
R661 100
R662 100

TO METER BRIDGE

D-SUB 205A-25FSTBBB3

TO: SW REG PCB CN13
P613
B6B-EH

F601
FUSE 5A/125V

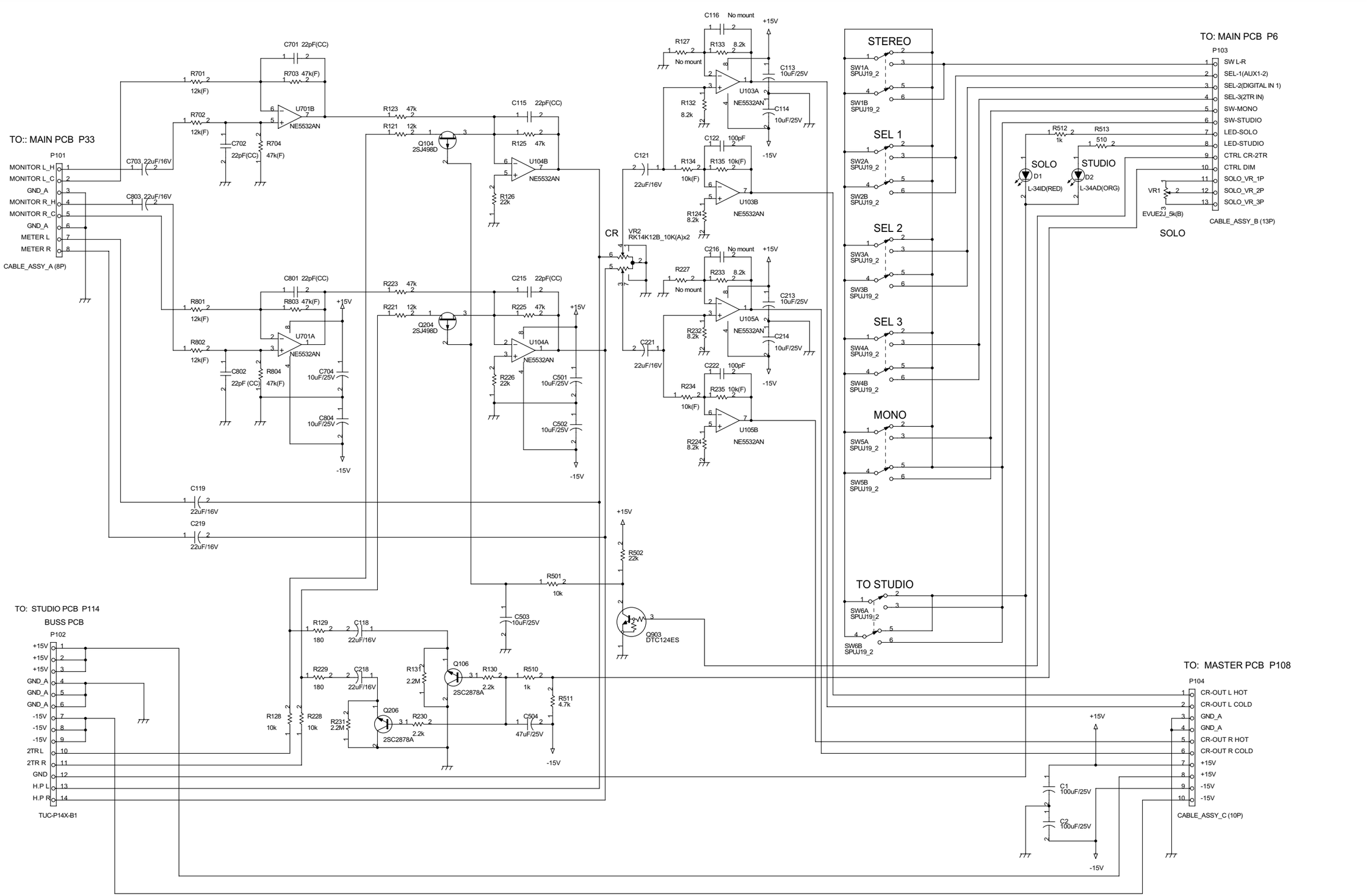
U701B
TC74VHCT00

U701A
TC74VHCT00

C701
0.1uF(CC)

# Digital Mixing Console DM-24

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# Digital Mixing Console DM-24

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# DM-24 IOX BLOCK DIAGRAM

Contents of the circuit schema


| | |
|---|---|
| PAGE 1 MAIN CPU | PAGE 8 DSP5, DSP6 & SDRAMs |
| PAGE 2 PANEL CPU | PAGE 9 DSP7 (for EFFECTOR) |
| PAGE 3 BUFFER for the SLOT | PAGE 10 DSP8 (RESERVE) |
| PAGE 4 INPUT SELECTOR for IOXs | PAGE 11 PLL & DIGITAL I/O |
| PAGE 5 IOXs | PAGE 12 ADCs for 1-16 inputs |
| PAGE 6 DSP1 & DSP2 | PAGE 13 CODECs & ADC for TBM |
| PAGE 7 DSP3 & DSP4 | |


MOTHER PCB

SLOT1

SLOT2

J3

J4

P20

P21

PAGE 3

74LV541 (U48)

74LVC240 (U55)

74LVC240 (U56)

74LVC240 (U57)

IOX1 OUT1 … IOX1 OUT8

IOX2 OUT1 … IOX2 OUT6

TDIF 1 (P601)

TDIF 2 (P602)

TDIF 3 (P603)

P611

P612

P614

P17

P18

P23

74LV04 (U165)

OPT IN (U601)

OPT OUT (U602)

TDIF PCB

ADAT Receive (U120)

ADAT Transmitter (U121)

PAGE 11

PAGE 12

MIC AMP 1ch … MIC AMP 16ch

P101 P102 P103 P104

P26 P36 P27 P37

ADC1 (U148)

ADC2 (U149)

ADC3 (U150)

ADC4 (U151)

ADC5 (U152)

ADC6 (U153)

ADC7 (U154)

ADC8 (U155)

INPUT PCB

PAGE 4

74HC540 (U58)

74HC540 (U59)

74HC540 (U60)

74LV541 (U62)

74LV541 (U63)

74LV541 (U64)

74LV541 (U65)

74LV541 (U66)

74LV541 (U67)

74LV541 (U69)

74LV157 (U86)

74LV139 (U68 1/2)

74LV139 (U26 1/2)

MPJ0 MPJ1 MPJ2 MPJ3 MPJ4 MPJ5 MPJ6

MAIN PCB

PAGE 5

IOX 1 (U71)

IOX 2 (U72)

IOX 3 (U73)

74LV245 (U74)

74LV245 (U75)

74LV245 (U76)

DSP 1 DATA BUSS

IOX DATA BUSS

DSP 1 ADRESS BUSS

DSP 1 (U77)

PAGE 6

PLD for IOX (U160)

ADRESS DECODE

RD/WR TIMING

512Fs

ADC CODEC1 (U156) DAC1 DAC2 DAC3

ADC CODEC2 (U157) DAC1 DAC2 DAC3

ADC CODEC3 (U158) DAC1 DAC2 DAC3

74VHC153 (U166)

74LV74 (U141)

DR1B

DSP4 (U88)

PAGE 7

PAGE 13

P5 P106 STUDIO OUT L STUDIO OUT R — STUDIO PCB

P31 P105 A.RTN 1 (H&C) A.RTN 2 (H&C) A.RTN 3 (H&C) A.RTN 4 (H&C)

P32 P106 A.SEND 1 A.SEND 2 A.SEND 3 A.SEND 4

P999 STEREO OUT L STEREO OUT R — MASTER PCB

P33 P101 C.ROOM OUT L C.ROOM OUT R METER IN L METER IN R — C.ROOM PCB

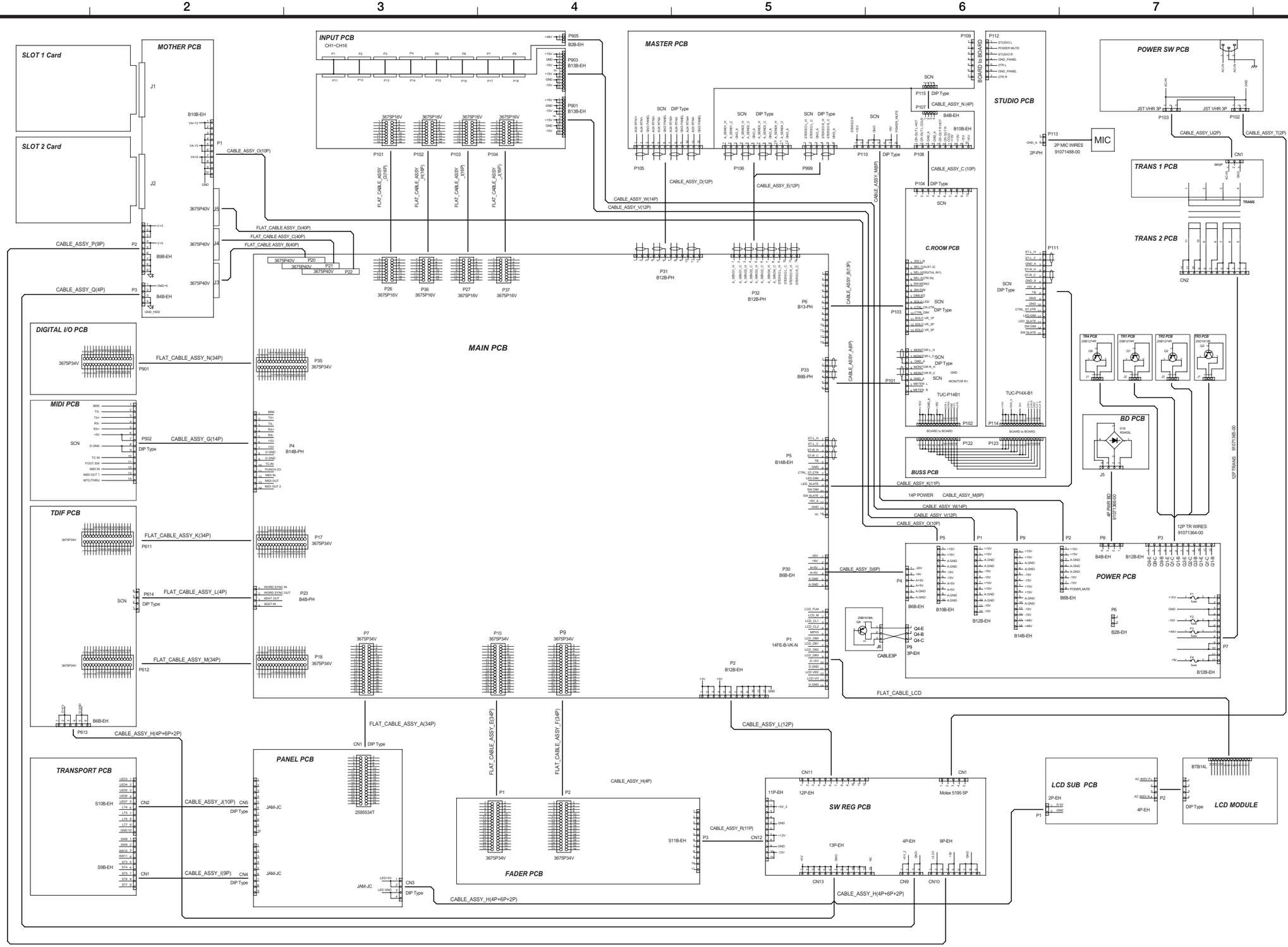
P8 (reserve)

# SCHEMATIC DIAGRAMS
回路図

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WIRING ..... Page 1/44
MAIN PCB ..... Pages 2-14/44
INPUT PCB ..... Pages 15-23/44
FADER PCB ..... Pages 24-29/44
PANEL PCB ..... Pages 30-34/44
MASTER PCB ..... Page 35/44
STUDIO PCB ..... Page 36/44
DIGITAL I/O PCB ..... Page 37/44
MIDI PCB ..... Page 38/44
TDIF PCB ..... Page 39/44
TRANSPORT PCB ..... Page 40/44
C.ROOM PCB ..... Page 41/44
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MOTHER PCB ..... Page 43/44
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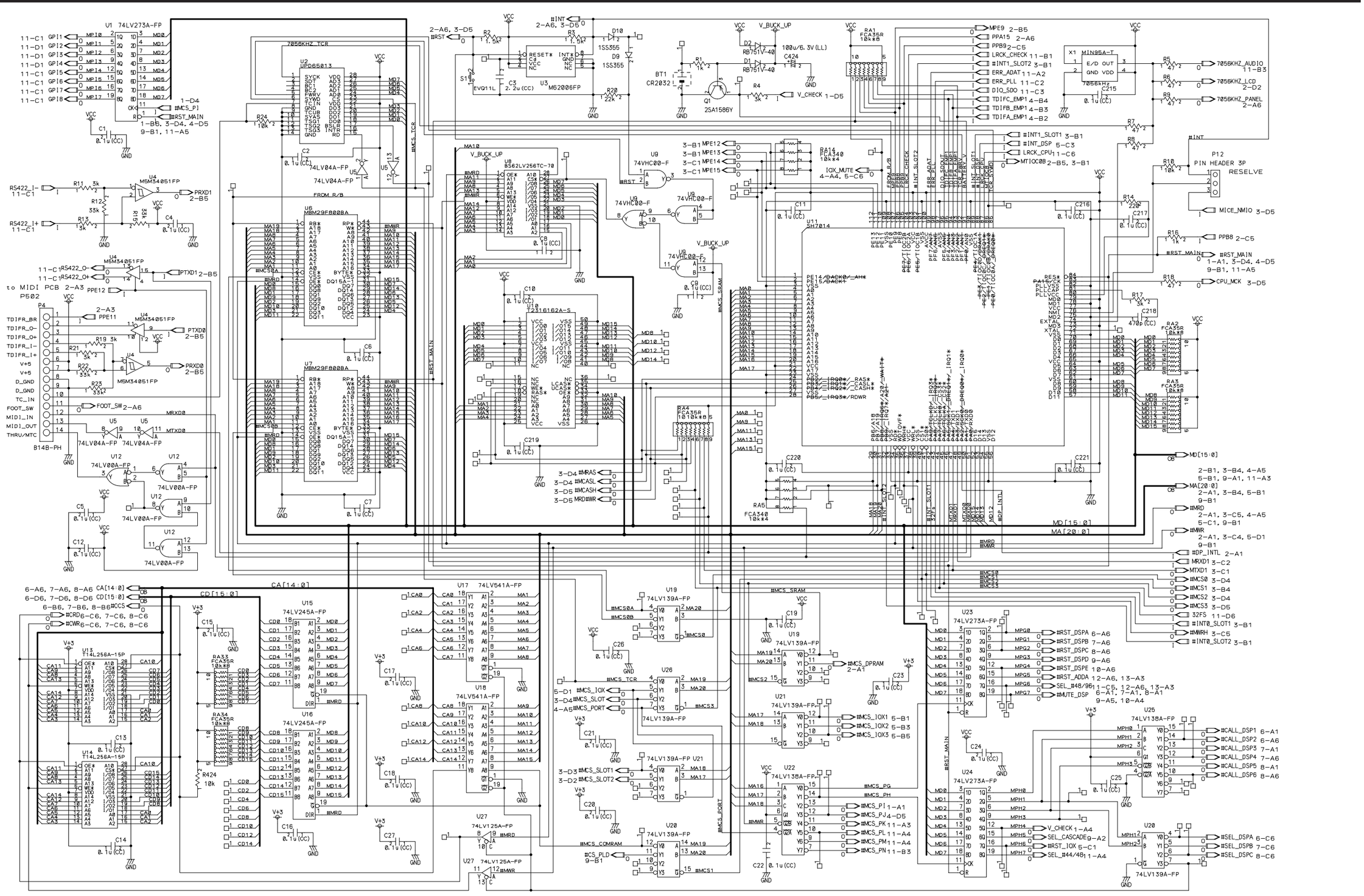
# SCHEMATIC DIAGRAM DM-24 WIRING DIAGRAM






Digital Mixing Console **DM-24**

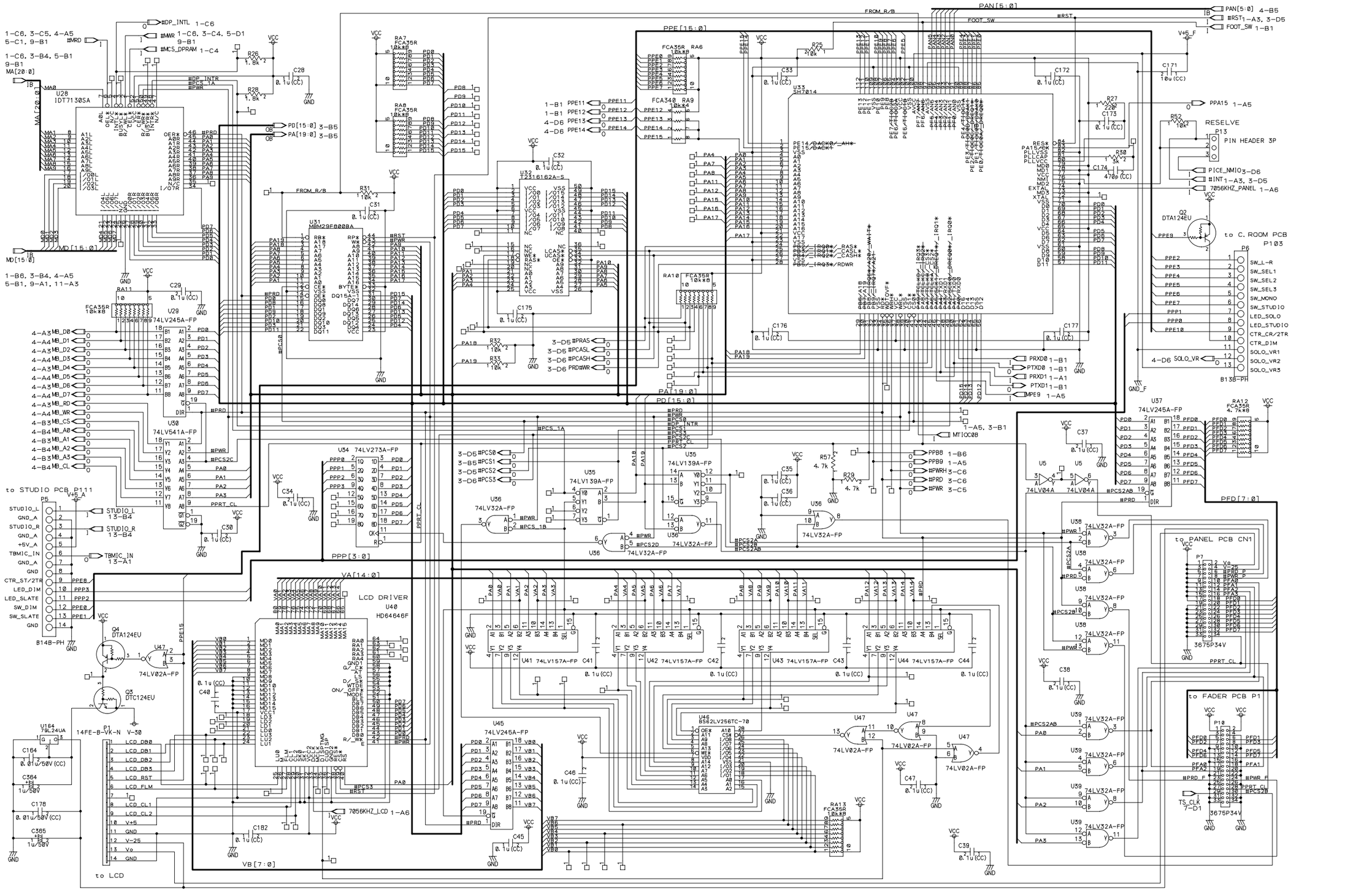
1 st Issue; September 2001






Digital Mixing Console DM-24

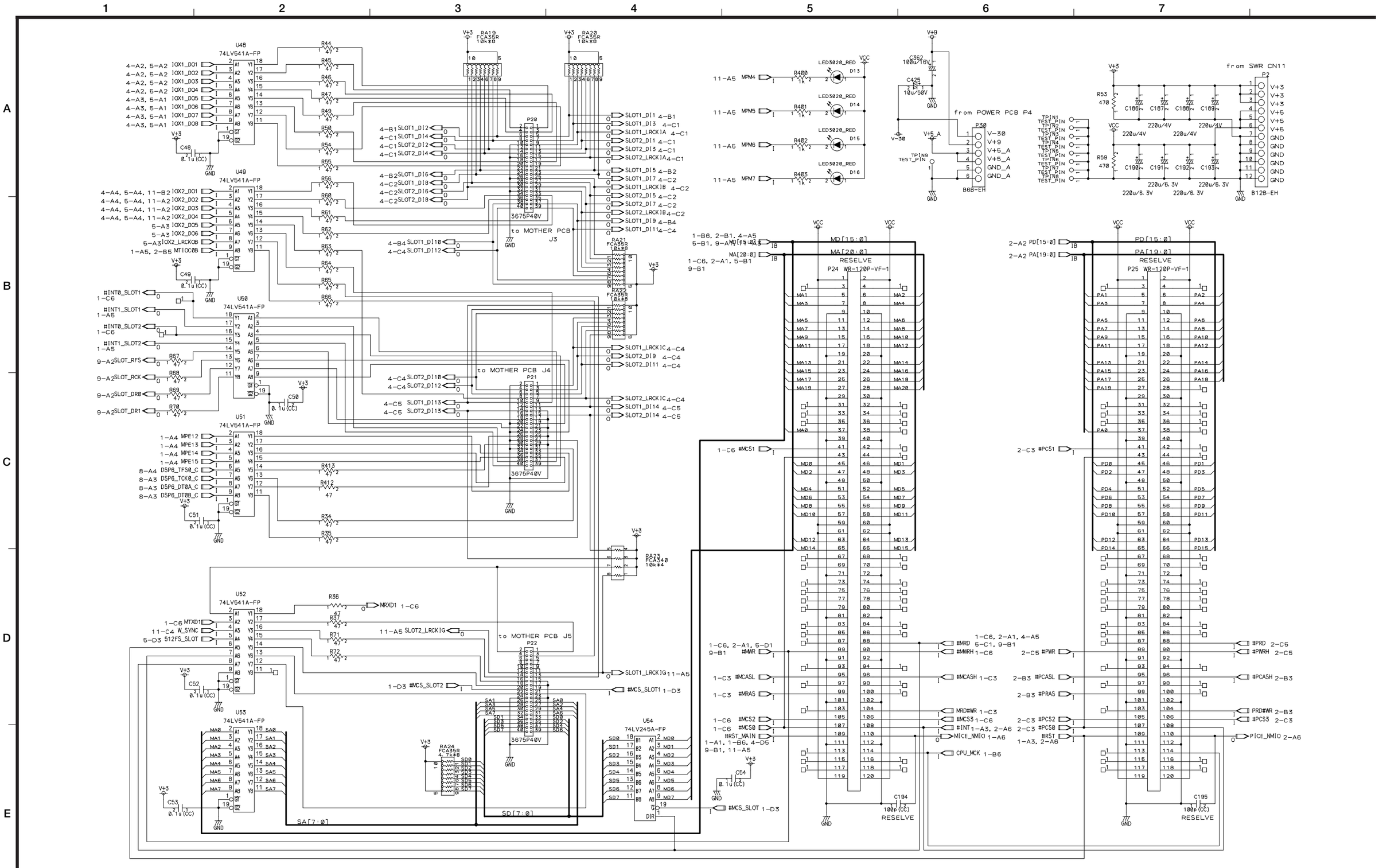
1 st Issue; September 2001

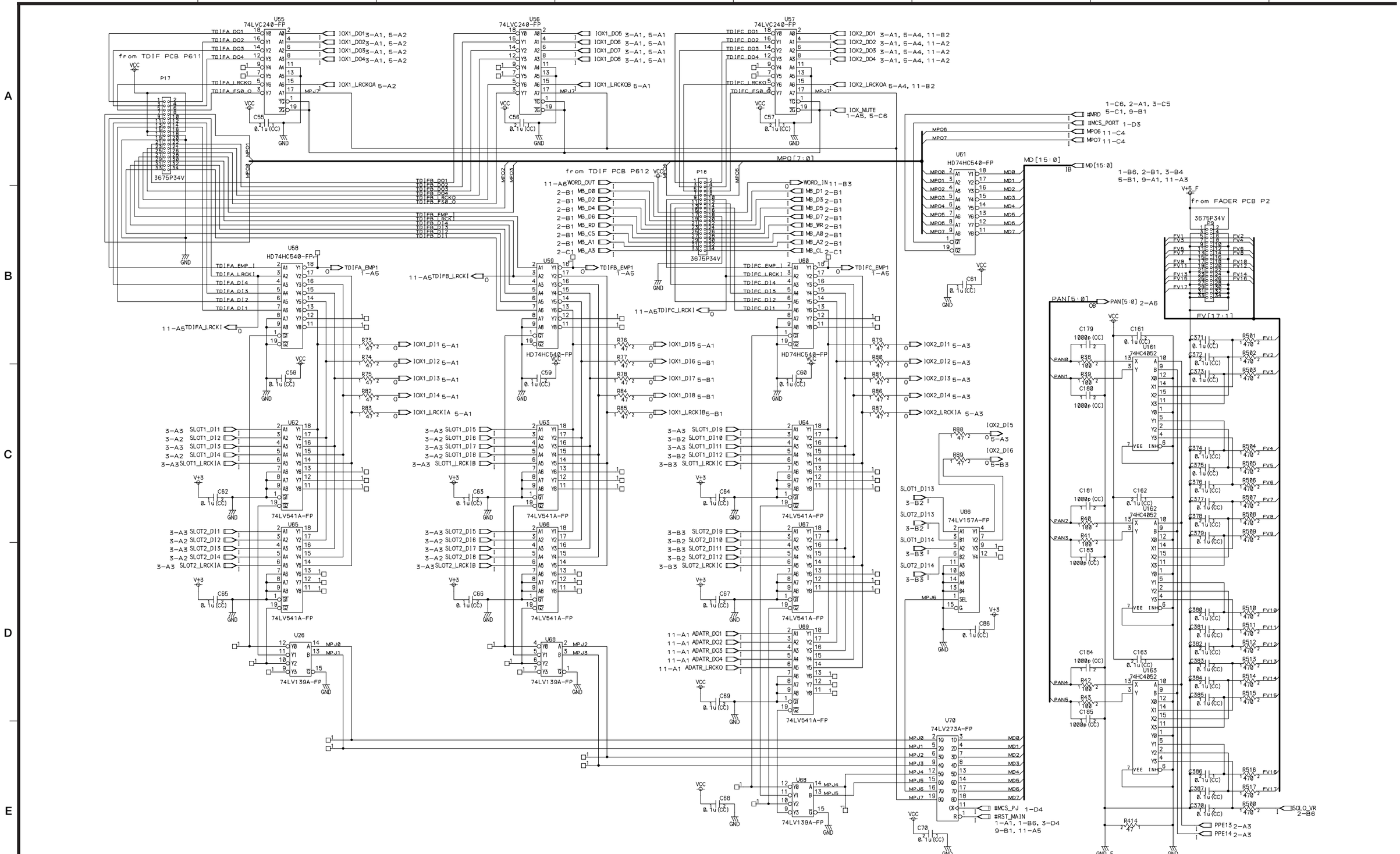


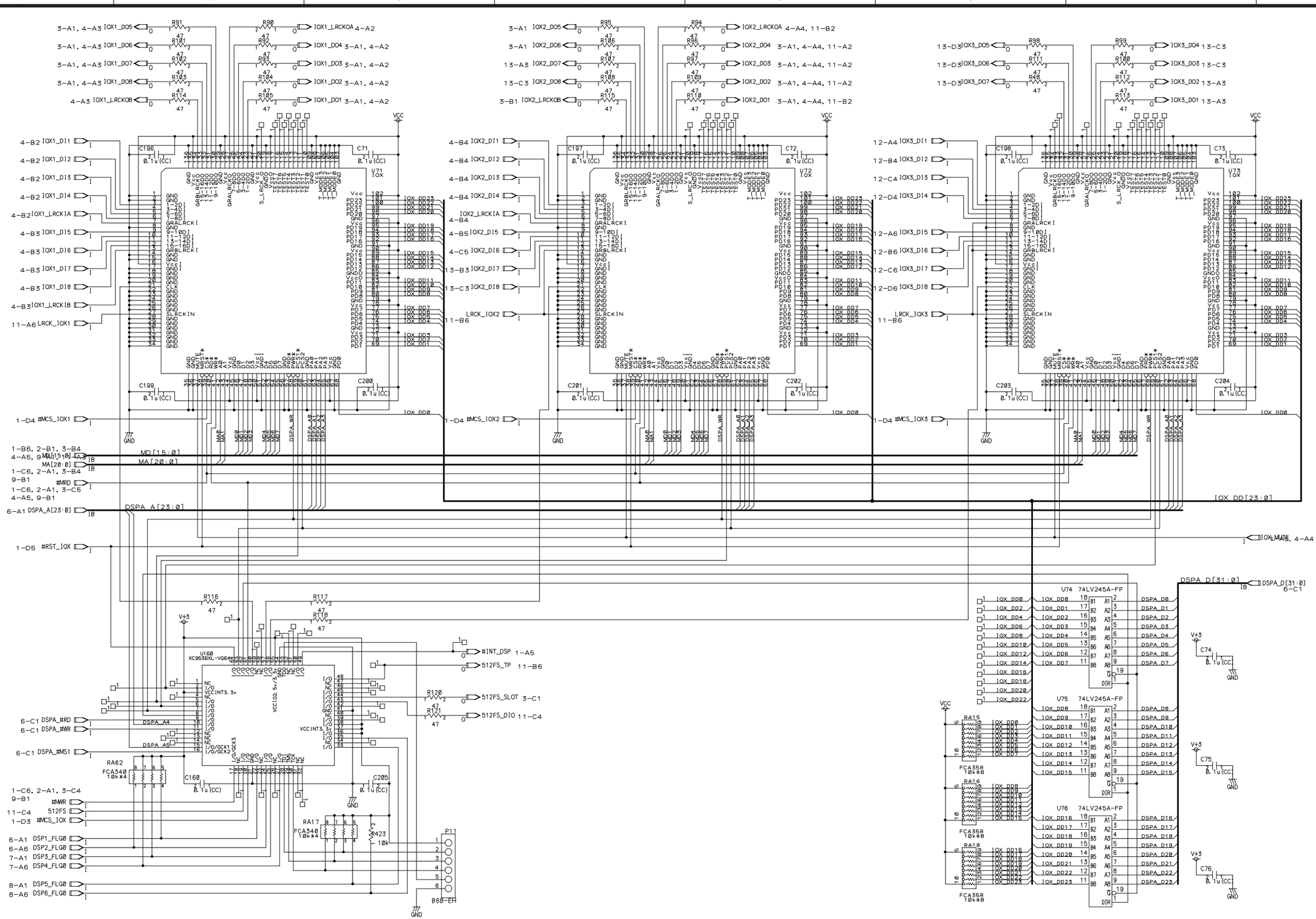



Digital Mixing Console DM-24

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1
2
3
4
5
6
7
A
B
C
D
E
U48
74LV541A-FP
U49
74LV541A-FP
U50
74LV541A-FP
U51
74LV541A-FP
U52
74LV541A-FP
U53
74LV541A-FP
U54
74LV245A-FP
RA19 FCA35R 10k×8
RA20 FCA35R 10k×8
RA21 FCA35R 10k×8
RA22 FCA35R 10k×8
RA23 FCA340 10k×4
RA24 FCA35R 4.7k×8
P20
P21
P22
3675P40V
to MOTHER PCB J3
to MOTHER PCB J4
to MOTHER PCB J5
P24 WR-120P-VF-1
P25 WR-120P-VF-1
RESELVE
P30
B6B-EH
P2
B12B-EH
from POWER PCB P4
from SWR CN11
SD[7:0]
SA[7:0]
MD[15:0]
MA[20:0]
PD[15:0]
PA[19:0]

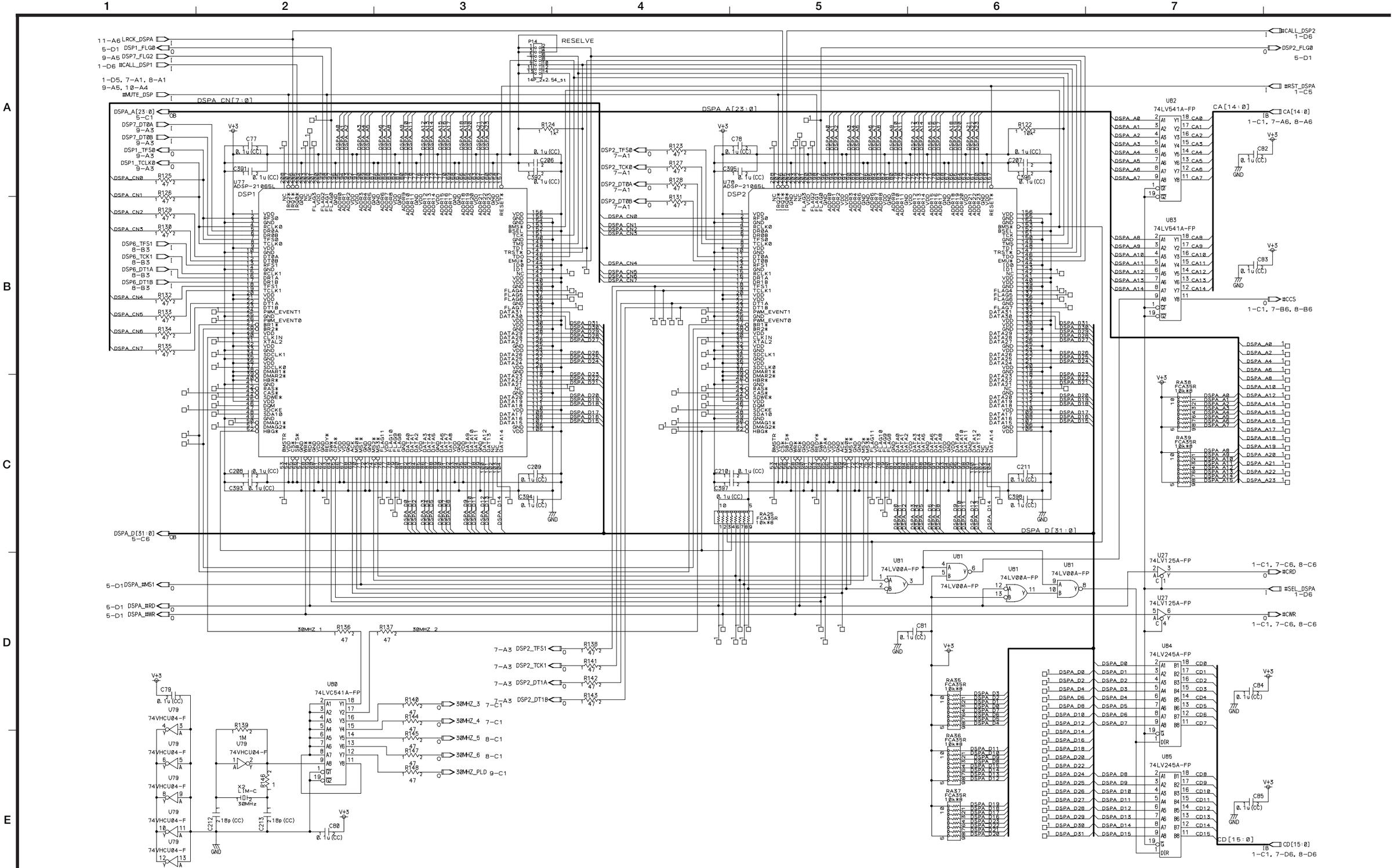

1
2
3
4
5
6
7
A
B
C
D
E
from TDIF PCB P611
from TDIF PCB P612
from FADER PCB P2
3675P34V
74LVC240-FP
74LV541A-FP
HD74HC540-FP
74LV139A-FP
74LV157A-FP
74LV273A-FP
74HC4052
MPO[7:0]
MD[15:0]
PAN[5:0]
FV[17:1]
0.1u (CC)
1000p (CC)
GND
VCC
V+3
V+5_F
GND_F






Digital Mixing Console **DM-24**

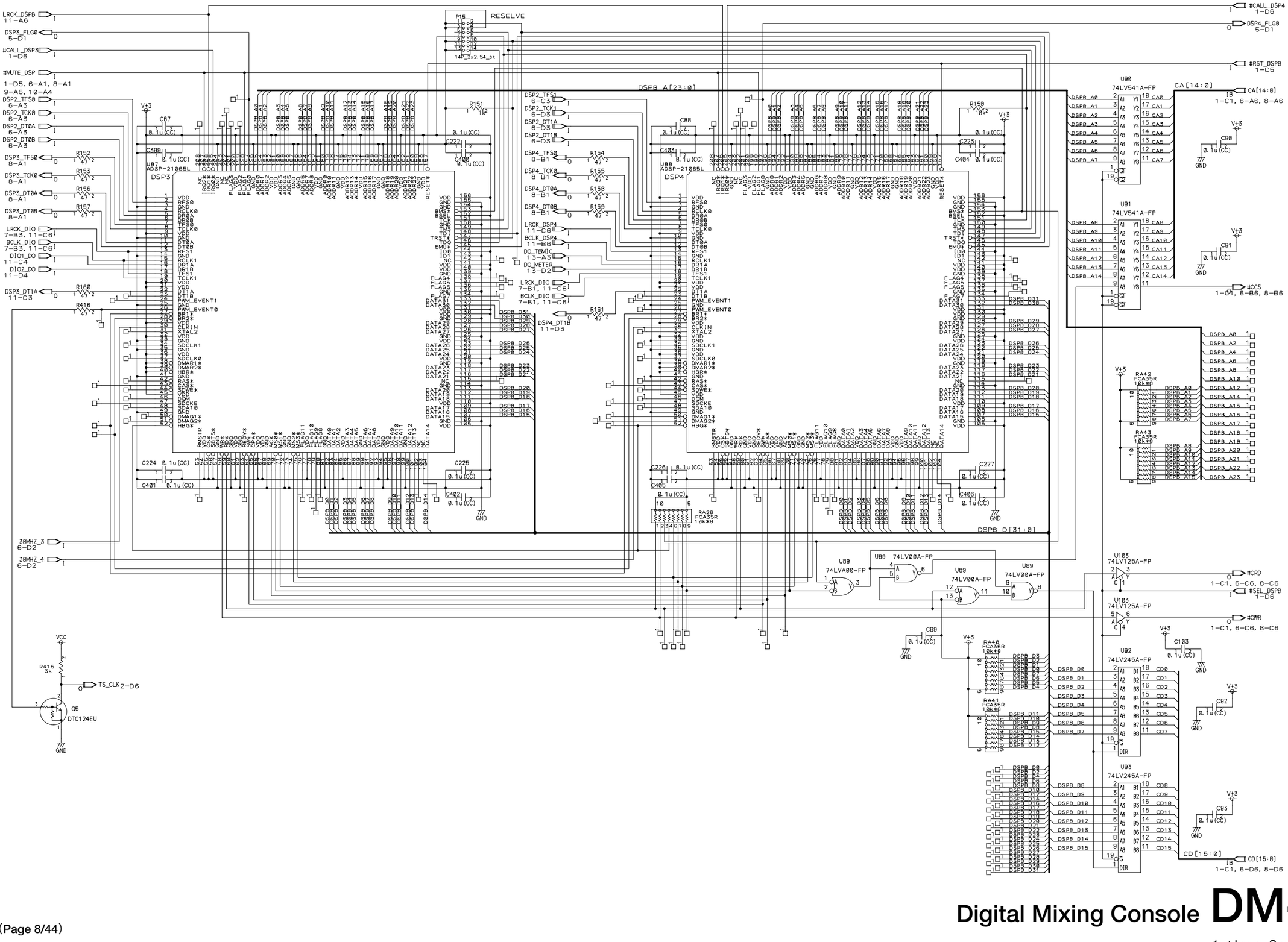
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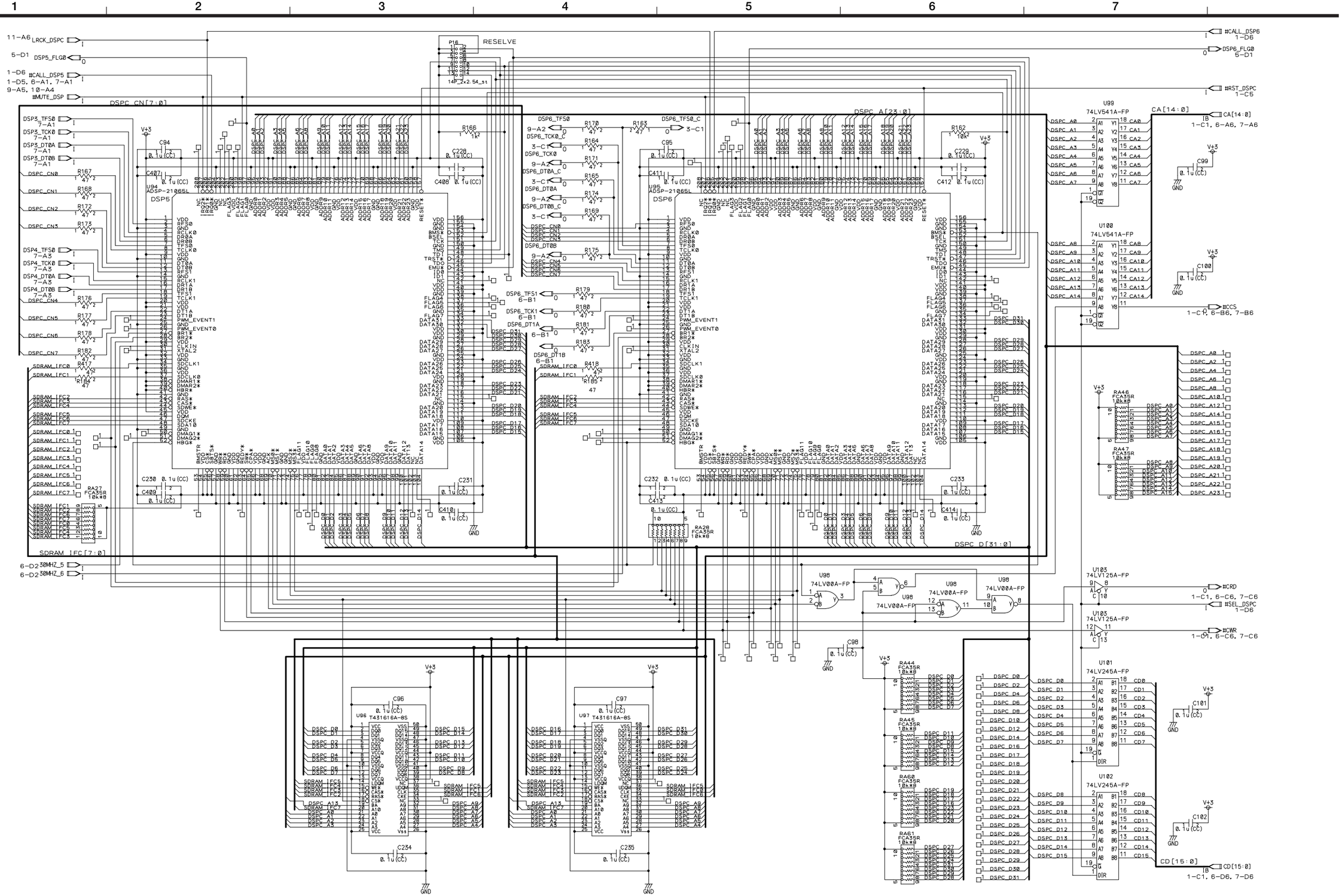


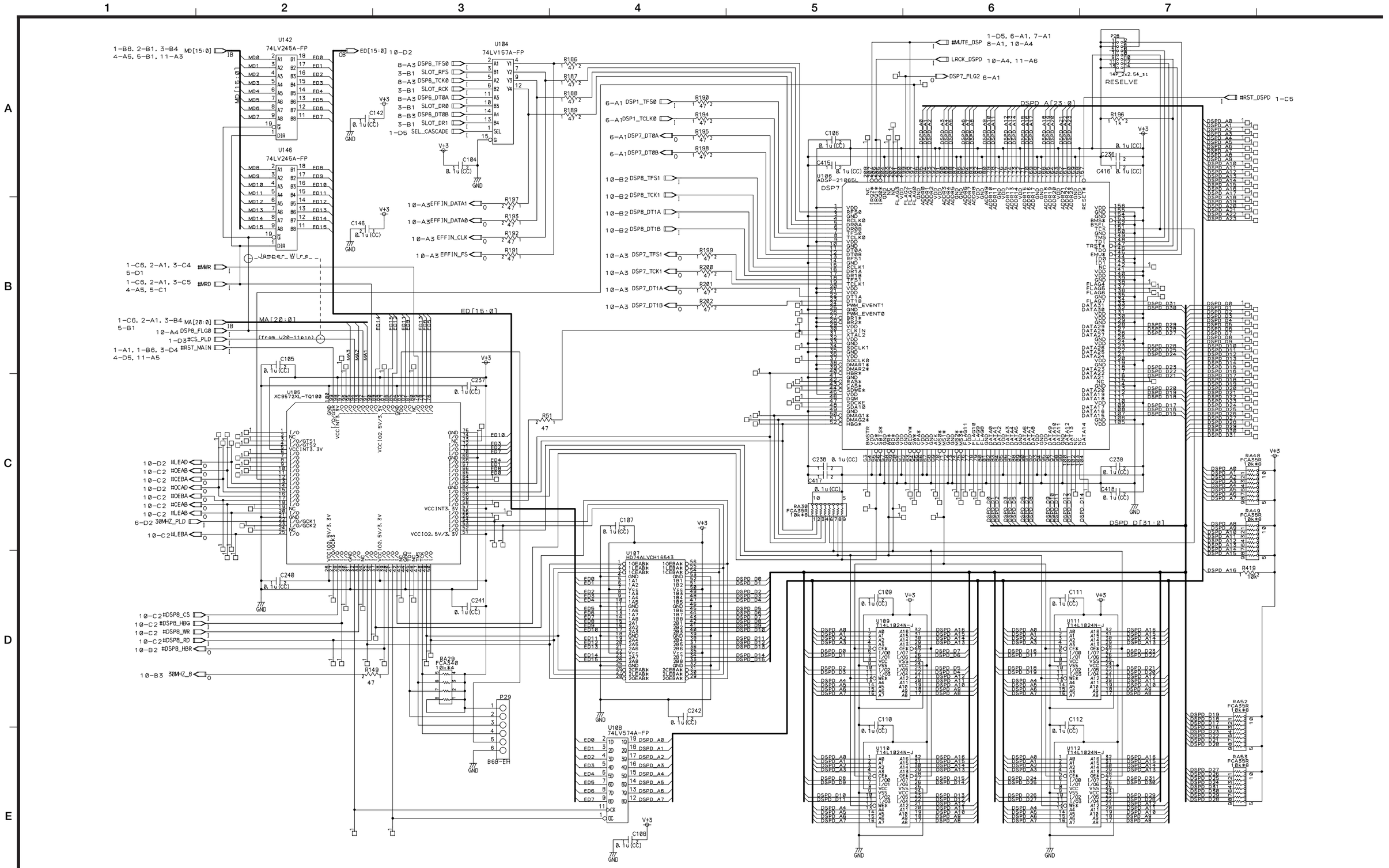



Digital Mixing Console DM-24

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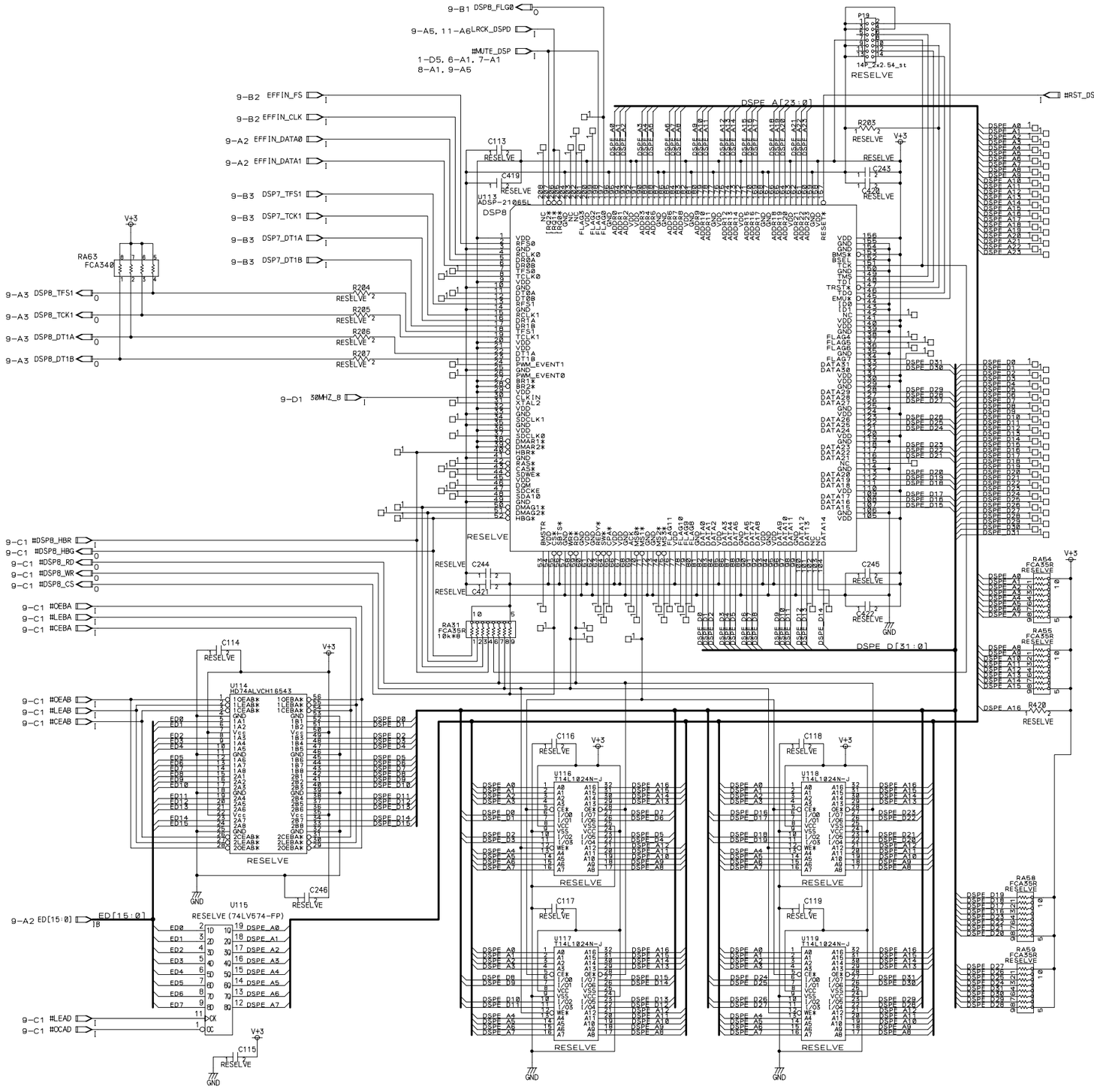

1
2
3
4
5
6
7
A
B
C
D
E
DSP3
DSP4
U87 ADSP-21065L
U88 ADSP-21065L
P15 RESELVE
DSPB_A[23:0]
DSPB_D[31:0]
LRCK_DSPB 11-A6
DSP3_FLG0 5-D1
#CALL_DSP3 1-D6
#MUTE_DSP 1-D5, 6-A1, 8-A1 9-A5, 10-A4
DSP2_TFS0 6-A3
DSP2_TCK0 6-A3
DSP2_DT0A 6-A3
DSP2_DT0B 6-A3
DSP3_TFS0 8-A1
DSP3_TCK0 8-A1
DSP3_DT0A 8-A1
DSP3_DT0B 8-A1
LRCK_DIO 7-B3, 11-C6
BCLK_DIO 7-B3, 11-C6
DIO1_DO 11-C4
DIO2_DO 11-D4
DSP3_DT1A 11-C3
30MHZ_3 6-D2
30MHZ_4 6-D2
DSP2_TFS1 6-C5
DSP2_TCK1 6-D3
DSP2_DT1A 6-D3
DSP2_DT1B 6-D3
DSP4_TFS0 8-B1
DSP4_TCK0 8-B1
DSP4_DT0A 8-B1
DSP4_DT0B 8-B1
LRCK_DSP4 11-C6
BCLK_DSP4 11-B6
DO_TBMIC 13-A3
DO_METER 13-D2
DSP4_DT1B 11-D3
#CALL_DSP4 1-D6
DSP4_FLG0 5-D1
#RST_DSPB 1-C5
U90 74LV541A-FP
U91 74LV541A-FP
CA[14:0]
CA[14:0] 1-C1, 6-A6, 8-A6
BCCS 1-D1, 6-B6, 8-B6
U89 74LV00A-FP
U89 74LVA00-FP
#CRD 1-C1, 6-C6, 8-C6
#SEL_DSPB 1-D6
#CWR 1-C1, 6-C6, 8-C6
U92 74LV245A-FP
U93 74LV245A-FP
CD[15:0]
CD[15:0] 1-C1, 6-D6, 8-D6
DIR
VCC
R415 3k
TS_CLK 2-D6
Q5 DTC124EU
GND
V+3


1
2
3
4
5
6
7
A
B
C
D
E
DSPC_CN[7:0]
DSPC_A[23:0]
DSPC_D[31:0]
SDRAM_FC[7:0]
RESELVE
U94
ADSP-21065L
DSP5
U95
DSP6
U99
74LV541A-FP
U100
74LV541A-FP
CA[14:0]
U96
T431616A-8S
U97
T431616A-8S
U98
74LV00A-FP
U101
74LV245A-FP
U102
74LV245A-FP
U103
74LV125A-FP
U105
74LV125A-FP
RA27
FCA35R
10k*8
RA28
FCA35R
10k*8
RA44
FCA35R
10k*8
RA45
FCA35R
10k*8
RA46
FCA35R
10k*8
RA47
FCA35R
10k*8
RA59
FCA35R
10k*8
RA61
FCA35R
10k*8
GND
V+3
30MHZ_5
30MHZ_6
#CALL_DSP5
#MUTE_DSP
#RST_DSPC
#CALL_DSP6
DSP5_FLG0
DSP6_FLG0
#CCS
#RCRD
#WCRD
#SEL_DSPC
#WCWR
CD[15:0]
DIR



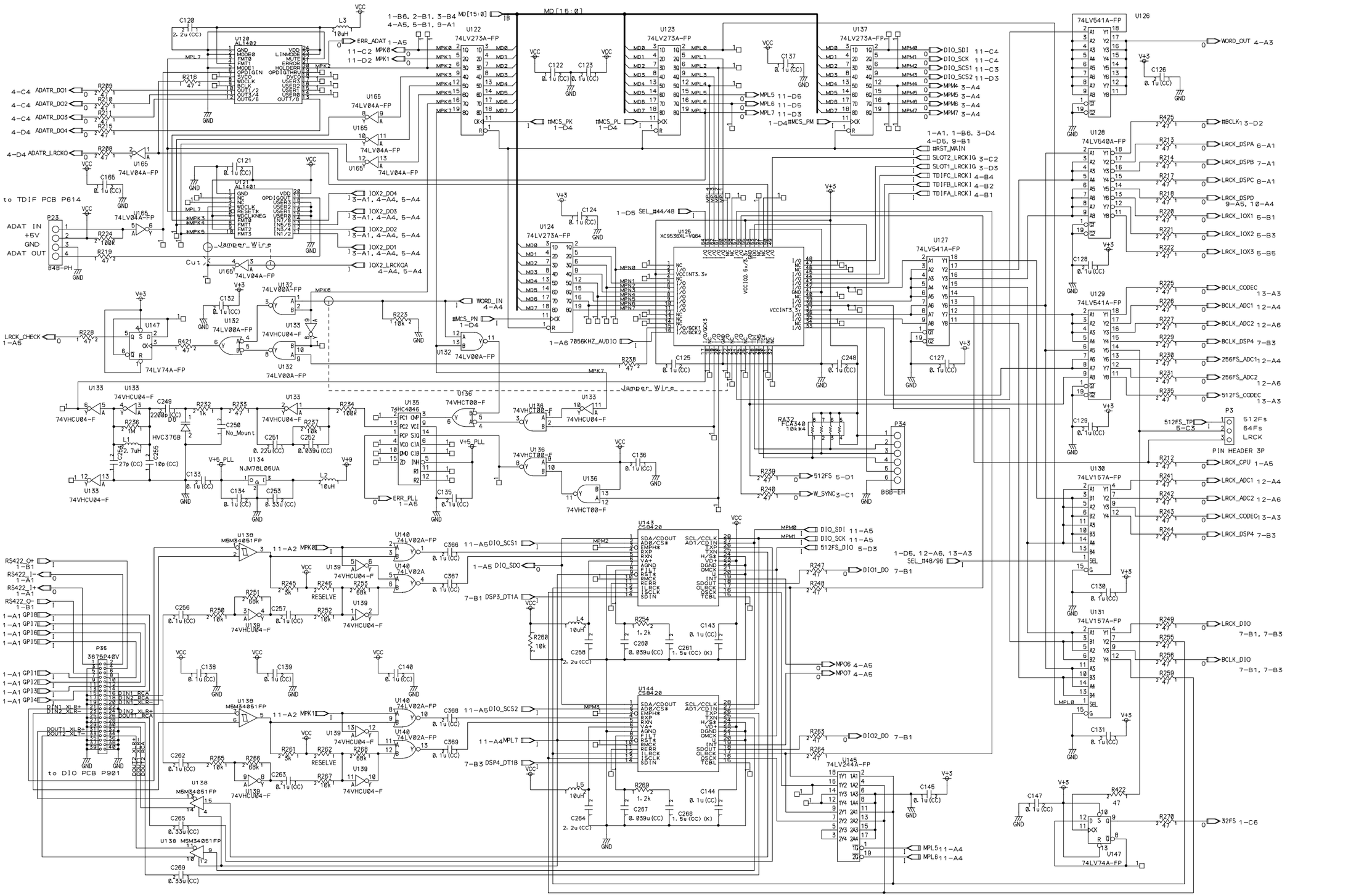



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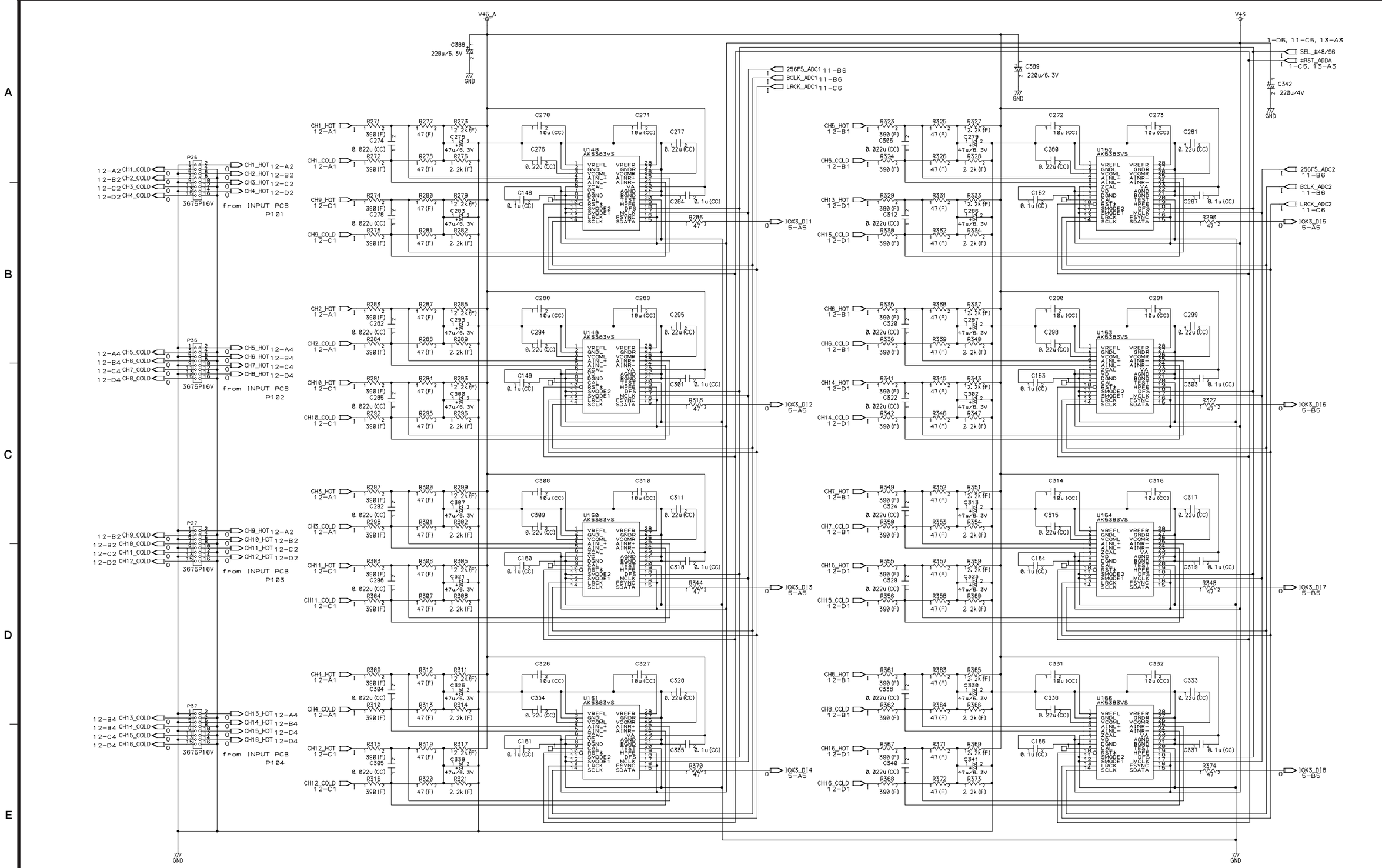


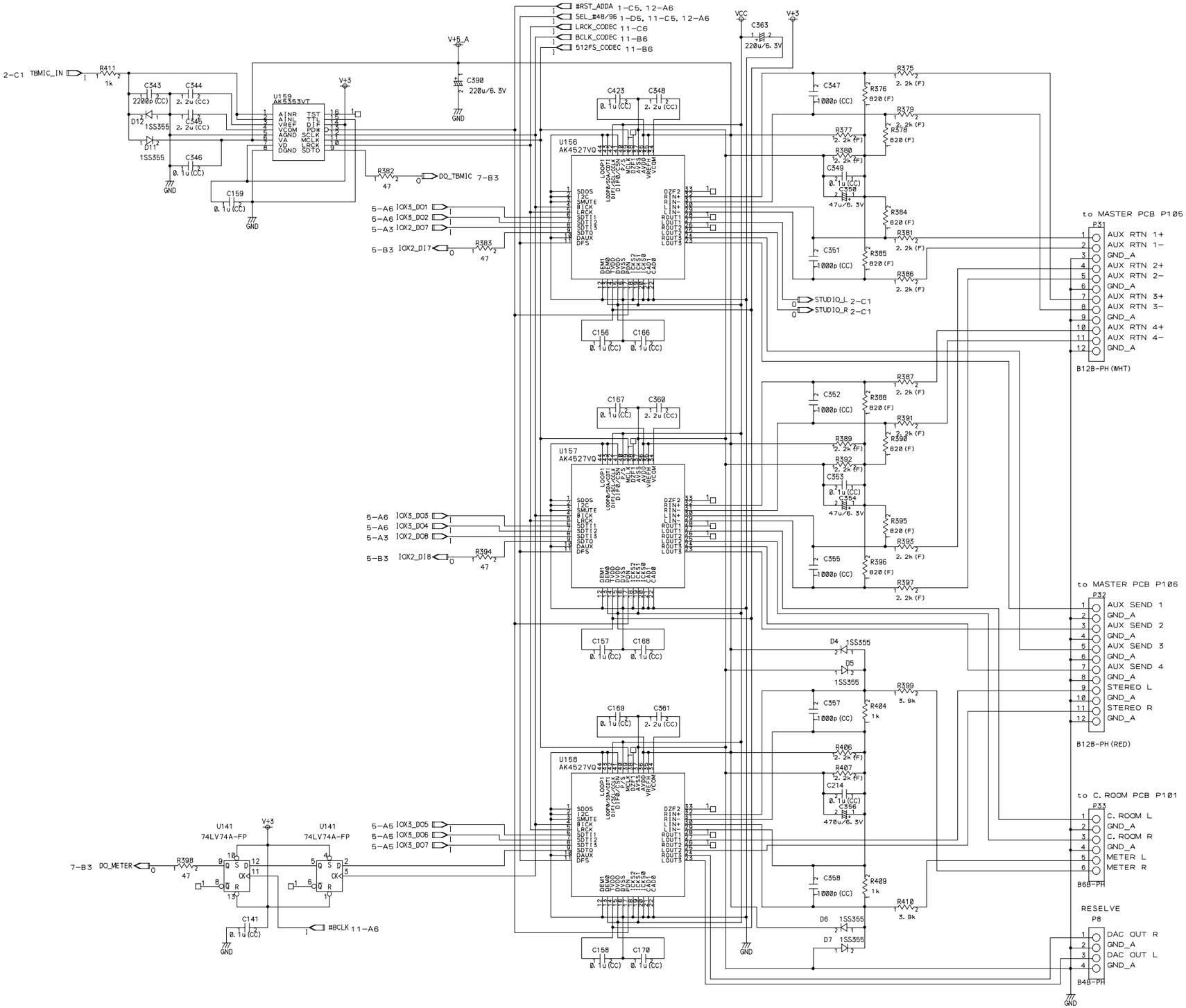

Digital Mixing Console DM-24
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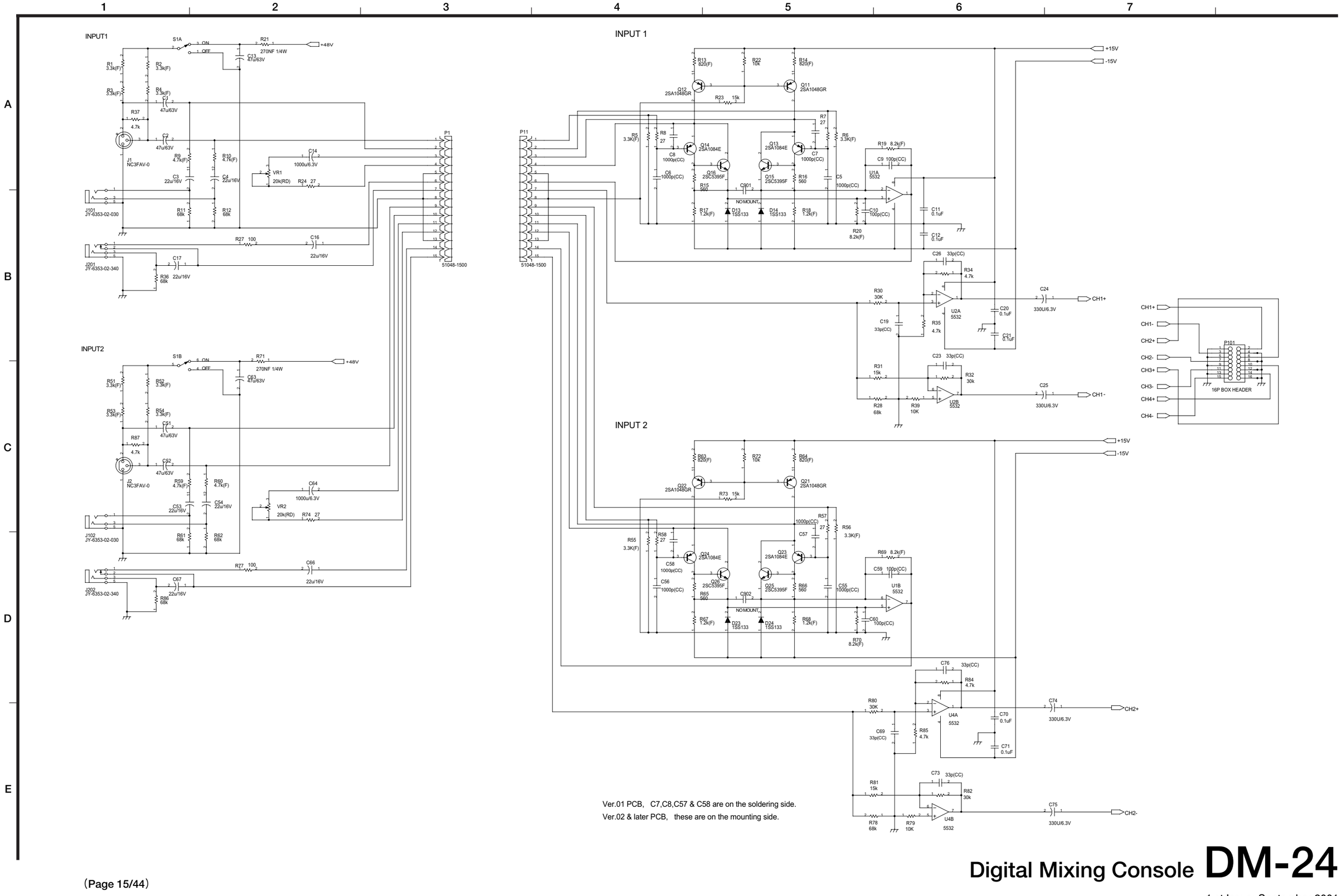



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1
2
3
4
5
6
7
A
B
C
D
E
V+5_A
V+3
GND
C388 220u/6.3V
C389 220u/6.3V
C342 220u/4V
1-D5, 11-C5, 13-A3
SEL_#48/96
#RST_ADDA
1-C5, 13-A3
256FS_ADC1 11-B6
BCLK_ADC1 11-B6
LRCK_ADC1 11-C6
256FS_ADC2 11-B6
BCLK_ADC2 11-B6
LRCK_ADC2 11-C6
P26
P36
P27
P37
3675P16V
from INPUT PCB P101
from INPUT PCB P102
from INPUT PCB P103
from INPUT PCB P104
U148 AK5383VS
U149 AK5383VS
U150 AK5383VS
U151 AK5383VS
U152 AK5383VS
U153 AK5383VS
U154 AK5383VS
U155 AK5383VS
IOX3_DI1 5-A5
IOX3_DI2 5-A5
IOX3_DI3 5-A5
IOX3_DI4 5-A5
IOX3_DI5 5-A5
IOX3_DI6 5-B5
IOX3_DI7 5-B5
IOX3_DI8 5-B5


#RST_ADDA 1-C5, 12-A6
SEL_#48/96 1-D5, 11-C5, 12-A6
LRCK_CODEC 11-C6
BCLK_CODEC 11-B6
512FS_CODEC 11-B6
2-C1 TBMIC_IN
R411 1k
C343 2200p (CC)
C344 2.2u (CC)
C345 2.2u (CC)
C346 0.1u (CC)
D12 1SS355
D11 1SS355
U159 AK5353VT
V+5_A
C390 220u/6.3V
V+3
C159 0.1u (CC)
R382 47
DO_TBMIC 7-B3
5-A6 IOX3_DO1
5-A6 IOX3_DO2
5-A3 IOX2_DO7
5-B3 IOX2_DI7
R383 47
U156 AK4527VQ
C423 0.1u (CC)
C548 2.2u (CC)
C156 0.1u (CC)
C166 0.1u (CC)
STUDIO_L 2-C1
STUDIO_R 2-C1
C363 220u/6.3V
VCC
R375 2.2k (F)
R376 820 (F)
R378 2.2k (F)
R379 820 (F)
R377 2.2k (F)
R380 2.2k (F)
C347 1000p (CC)
C349 0.1u (CC)
C350 47u/6.3V
R384 820 (F)
R381 2.2k (F)
C351 1000p (CC)
R385 820 (F)
R386 2.2k (F)
to MASTER PCB P105
P31
AUX RTN 1+
AUX RTN 1-
GND_A
AUX RTN 2+
AUX RTN 2-
GND_A
AUX RTN 3+
AUX RTN 3-
GND_A
AUX RTN 4+
AUX RTN 4-
GND_A
B12B-PH (WHT)
5-A6 IOX3_DO3
5-A6 IOX3_DO4
5-A3 IOX2_DO8
5-B3 IOX2_DI8
R394 47
U157 AK4527VQ
C167 0.1u (CC)
C360 2.2u (CC)
C157 0.1u (CC)
C168 0.1u (CC)
R387 2.2k (F)
R388 820 (F)
R391 2.2k (F)
R390 820 (F)
R389 2.2k (F)
R392 2.2k (F)
C352 1000p (CC)
C353 0.1u (CC)
C354 47u/6.3V
R395 820 (F)
R393 2.2k (F)
C355 1000p (CC)
R396 820 (F)
R397 2.2k (F)
to MASTER PCB P106
P32
AUX SEND 1
GND_A
AUX SEND 2
GND_A
AUX SEND 3
GND_A
AUX SEND 4
GND_A
STEREO L
GND_A
STEREO R
GND_A
B12B-PH (RED)
D4 1SS355
D5 1SS355
R399 3.9k
C357 1000p (CC)
R404 1k
R406 2.2k (F)
R407 2.2k (F)
C214 0.1u (CC)
C356 470u/6.3V
U158 AK4527VQ
C169 0.1u (CC)
C361 2.2u (CC)
C158 0.1u (CC)
C170 0.1u (CC)
5-A5 IOX3_DO5
5-A5 IOX3_DO6
5-A5 IOX3_DO7
U141 74LV74A-FP
U141 74LV74A-FP
7-B3 DO_METER
R398 47
C141 0.1u (CC)
#BCLK 11-A6
C358 1000p (CC)
R409 1k
R410 3.9k
D6 1SS355
D7 1SS355
to C.ROOM PCB P101
P33
C.ROOM L
GND_A
C.ROOM R
GND_A
METER L
METER R
B6B-PH
RESELVE
P8
DAC OUT R
GND_A
DAC OUT L
GND_A
B4B-PH
GND

# SCHEMATIC DIAGRAM DM-24 INPUT PCB (1/9)

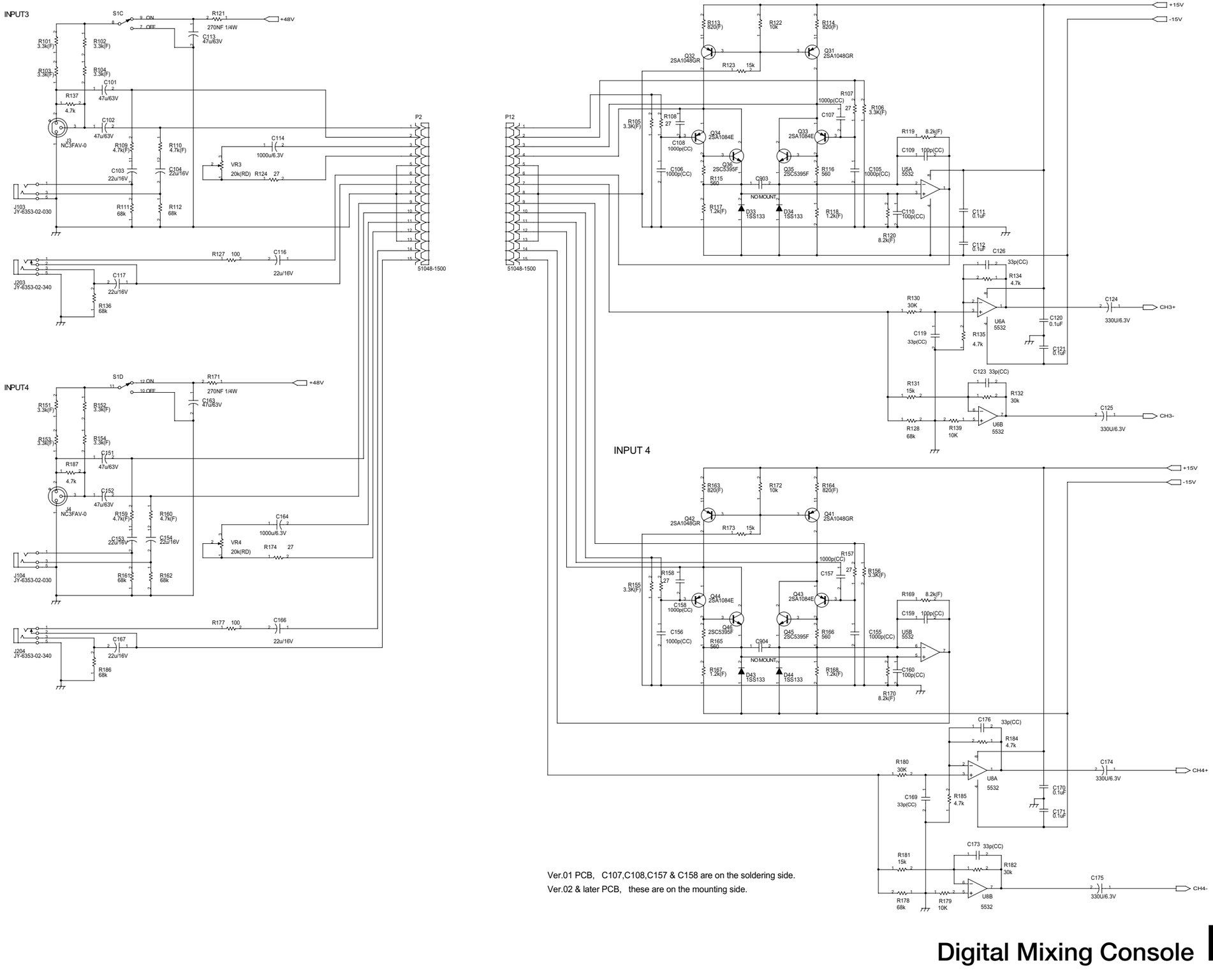



Ver.01 PCB, C7,C8,C57 & C58 are on the soldering side.
Ver.02 & later PCB, these are on the mounting side.



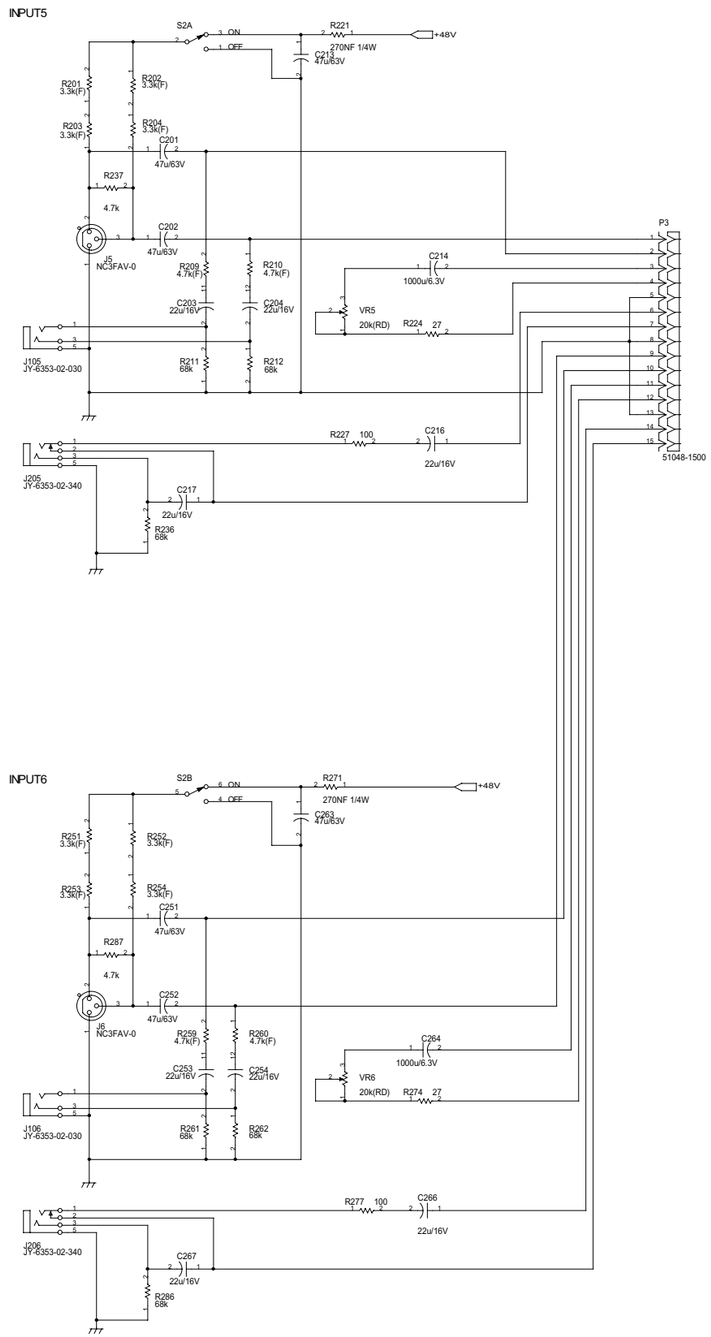
Digital Mixing Console DM-24
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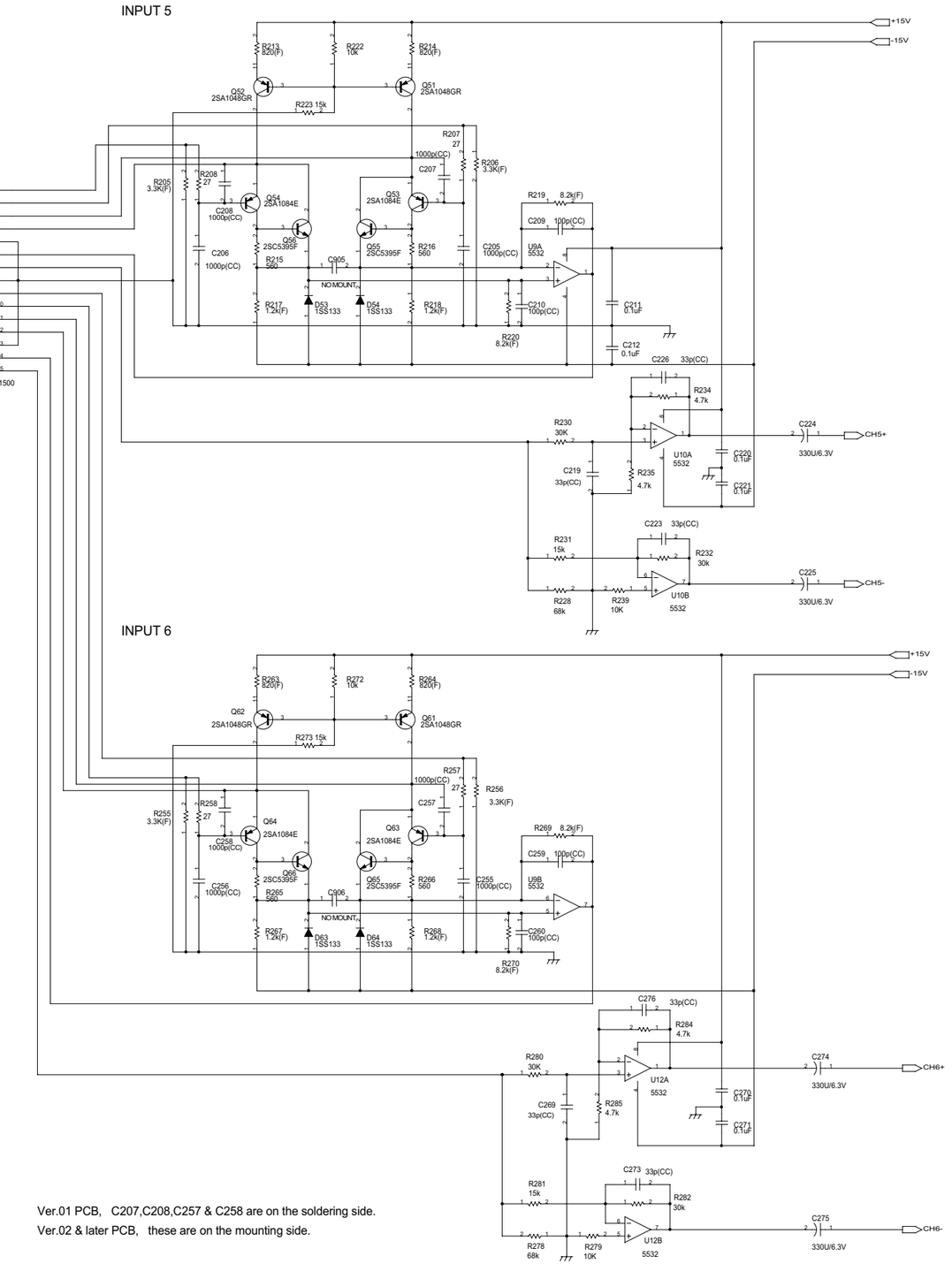
# SCHEMATIC DIAGRAM DM-24 INPUT PCB (2/9)




Ver.01 PCB, C107,C108,C157 & C158 are on the soldering side.
Ver.02 & later PCB, these are on the mounting side.

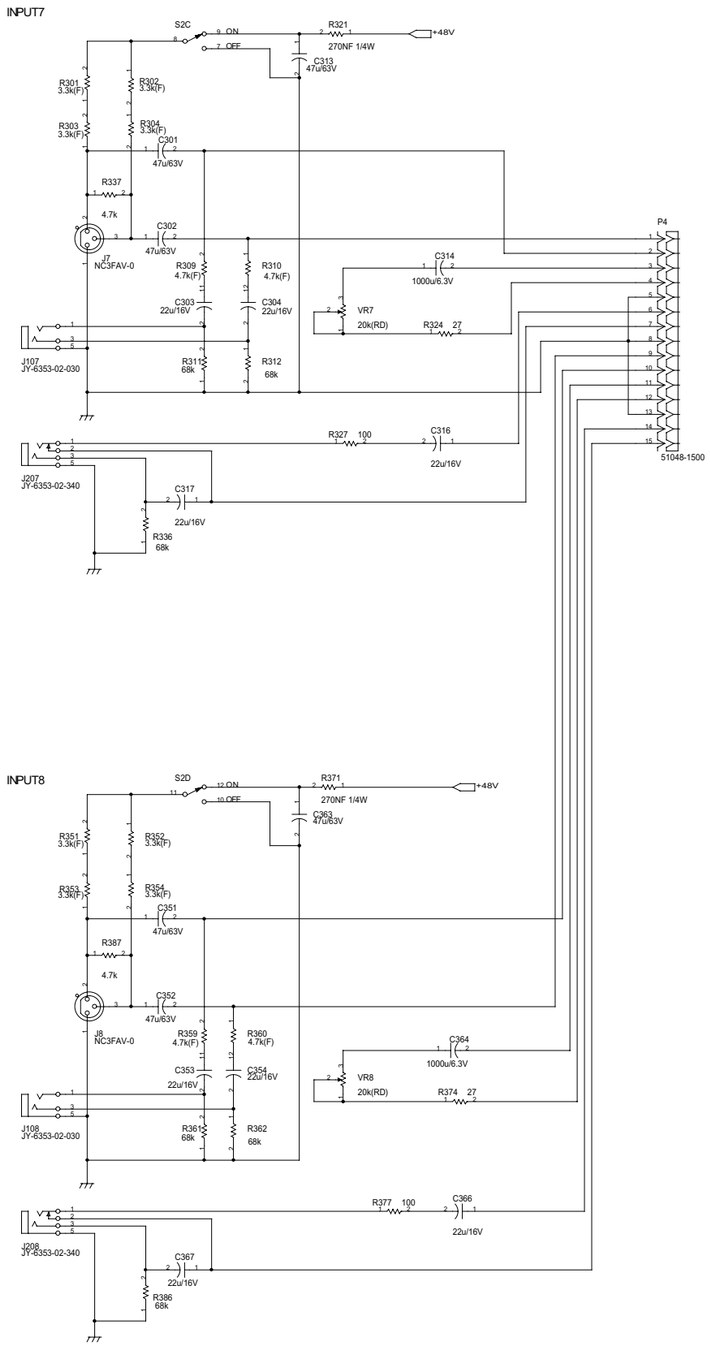
# SCHEMATIC DIAGRAM DM-24 INPUT PCB (3/9)

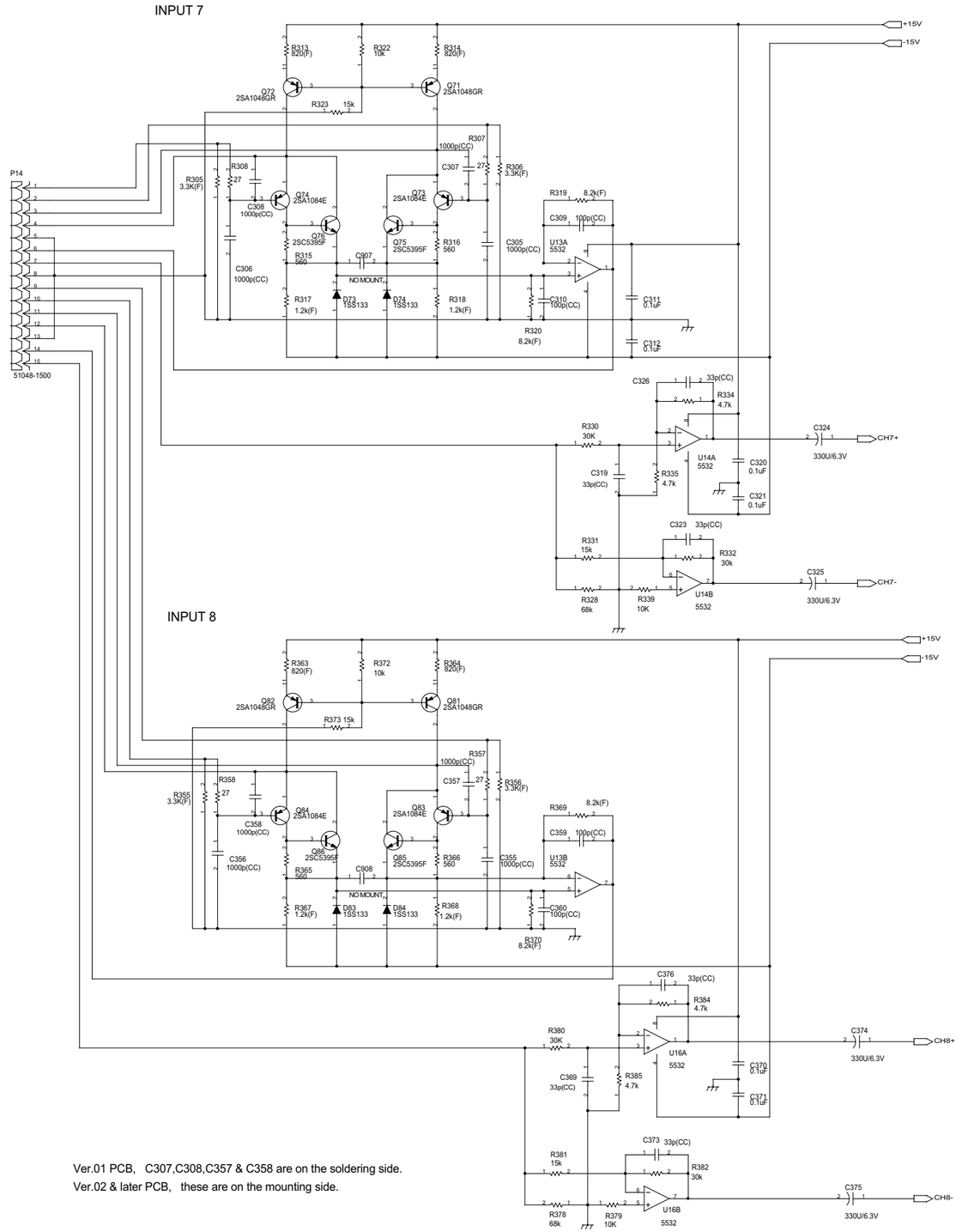


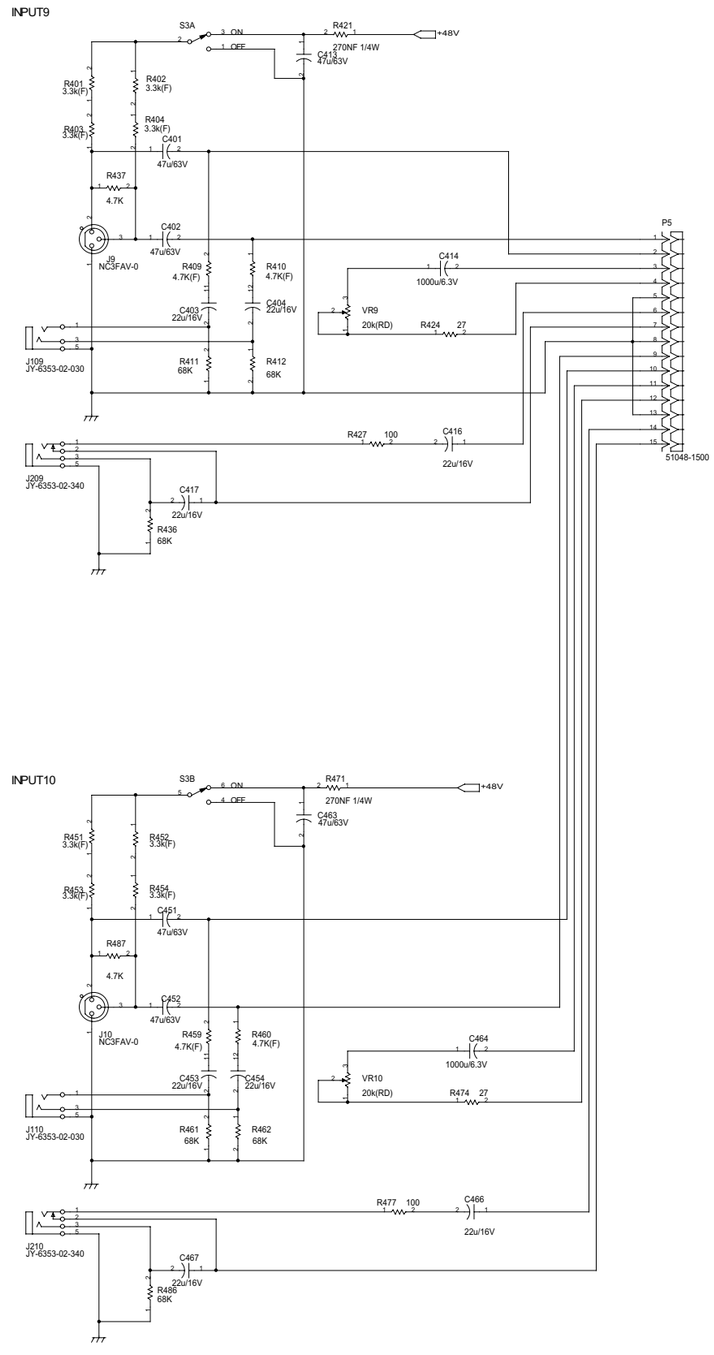

Ver.01 PCB, C207,C208,C257 & C258 are on the soldering side.
Ver.02 & later PCB, these are on the mounting side.

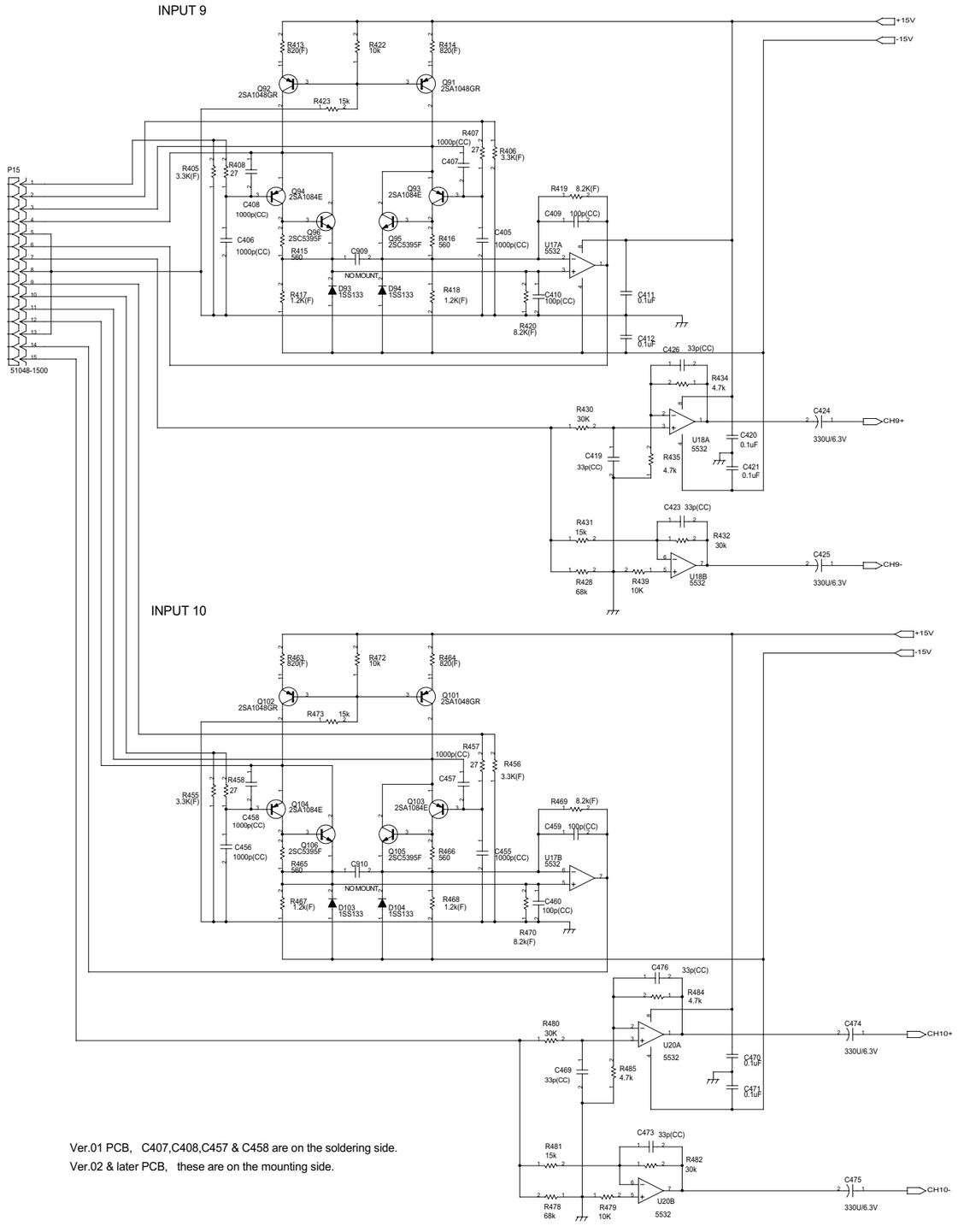
# SCHEMATIC DIAGRAM DM-24 INPUT PCB (4/9)



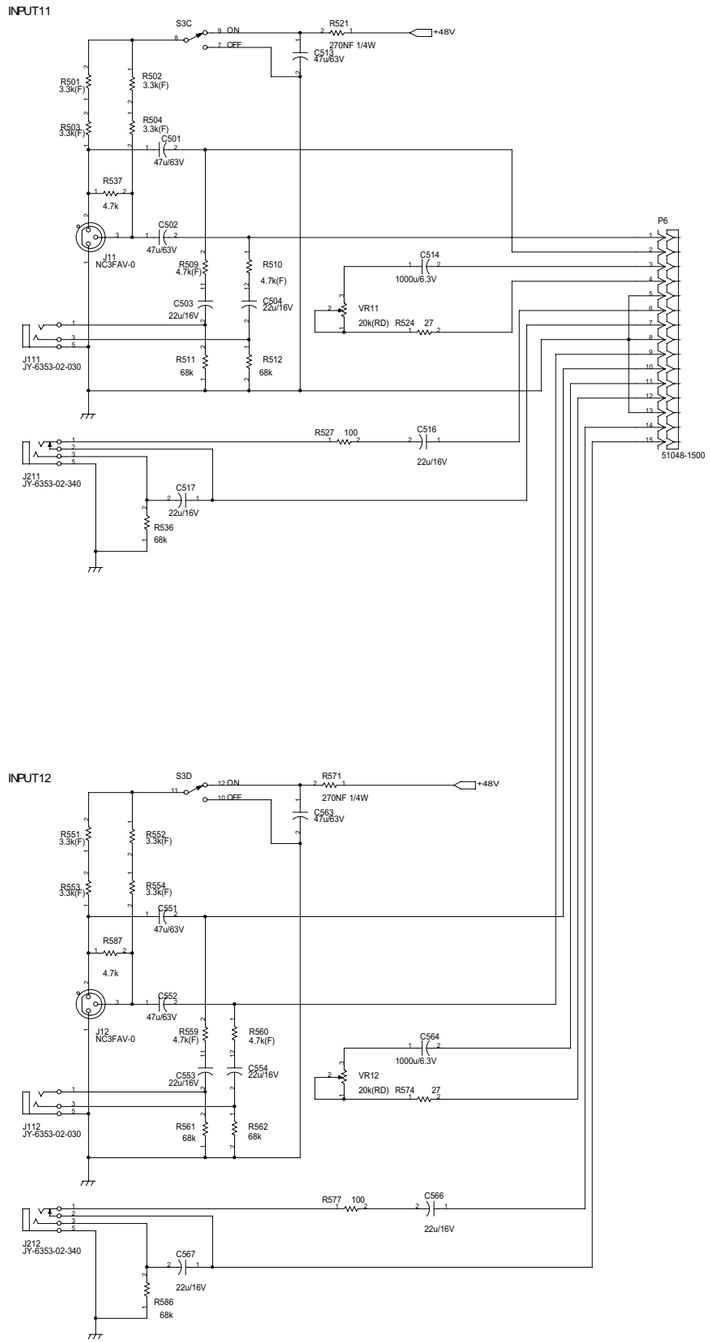

Ver.01 PCB, C307,C308,C357 & C358 are on the soldering side.
Ver.02 & later PCB, these are on the mounting side.

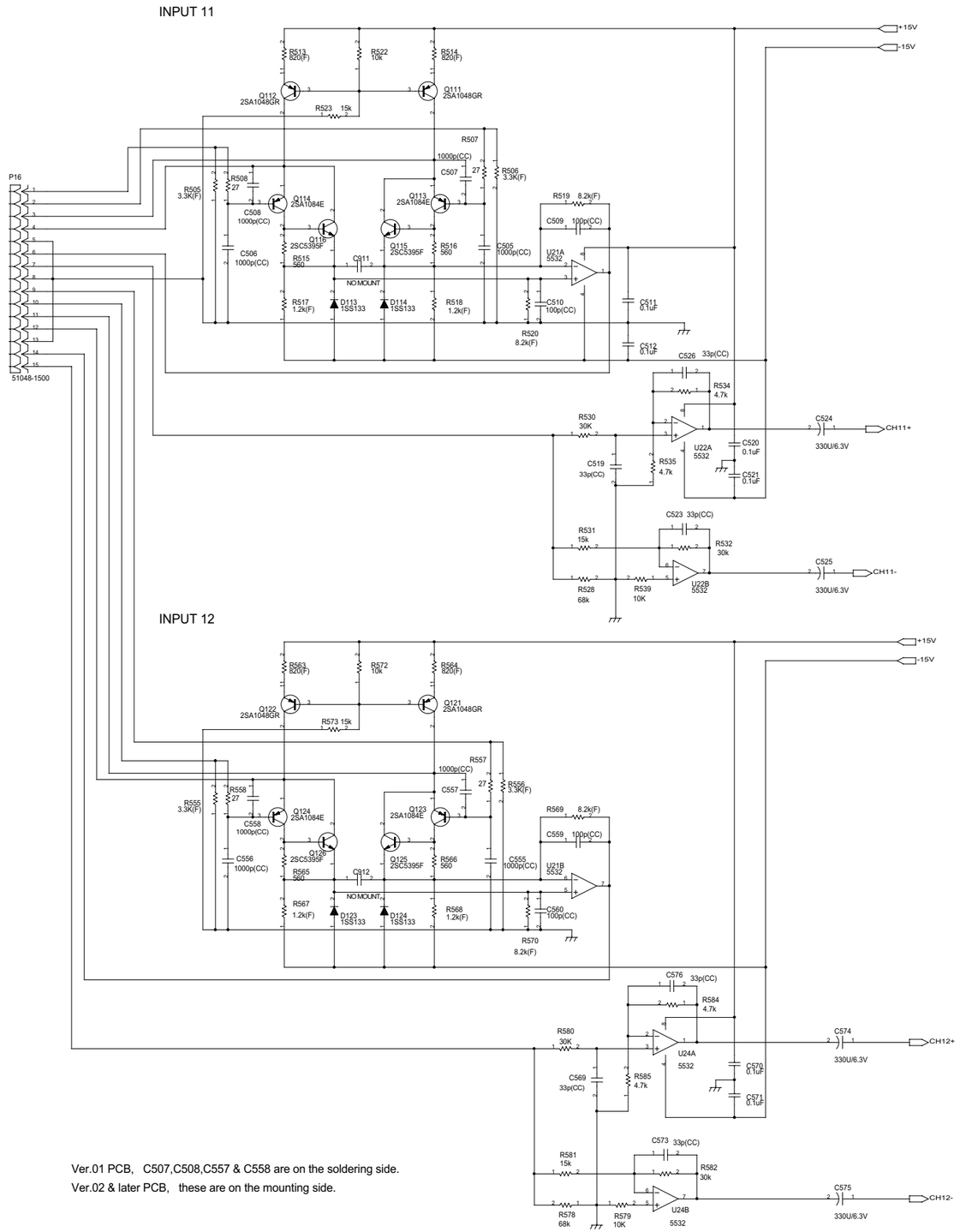


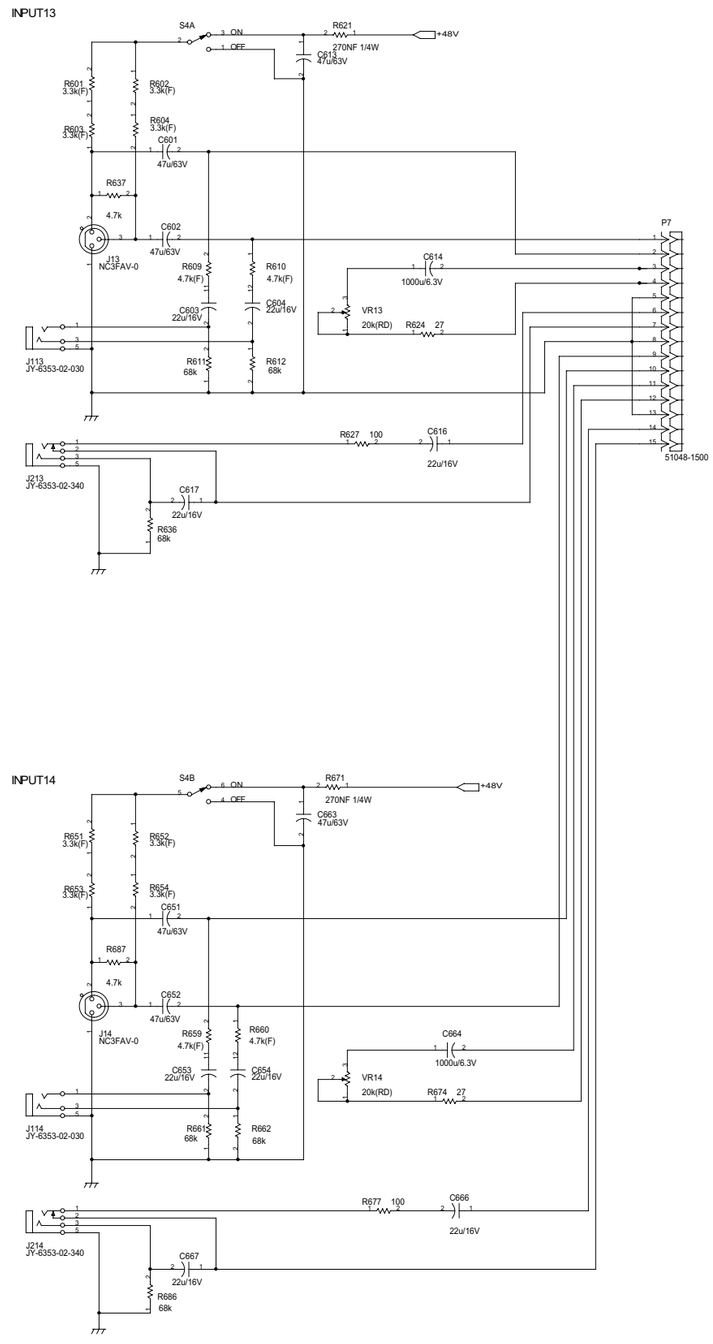

Ver.01 PCB, C407,C408,C457 & C458 are on the soldering side.
Ver.02 & later PCB, these are on the mounting side.

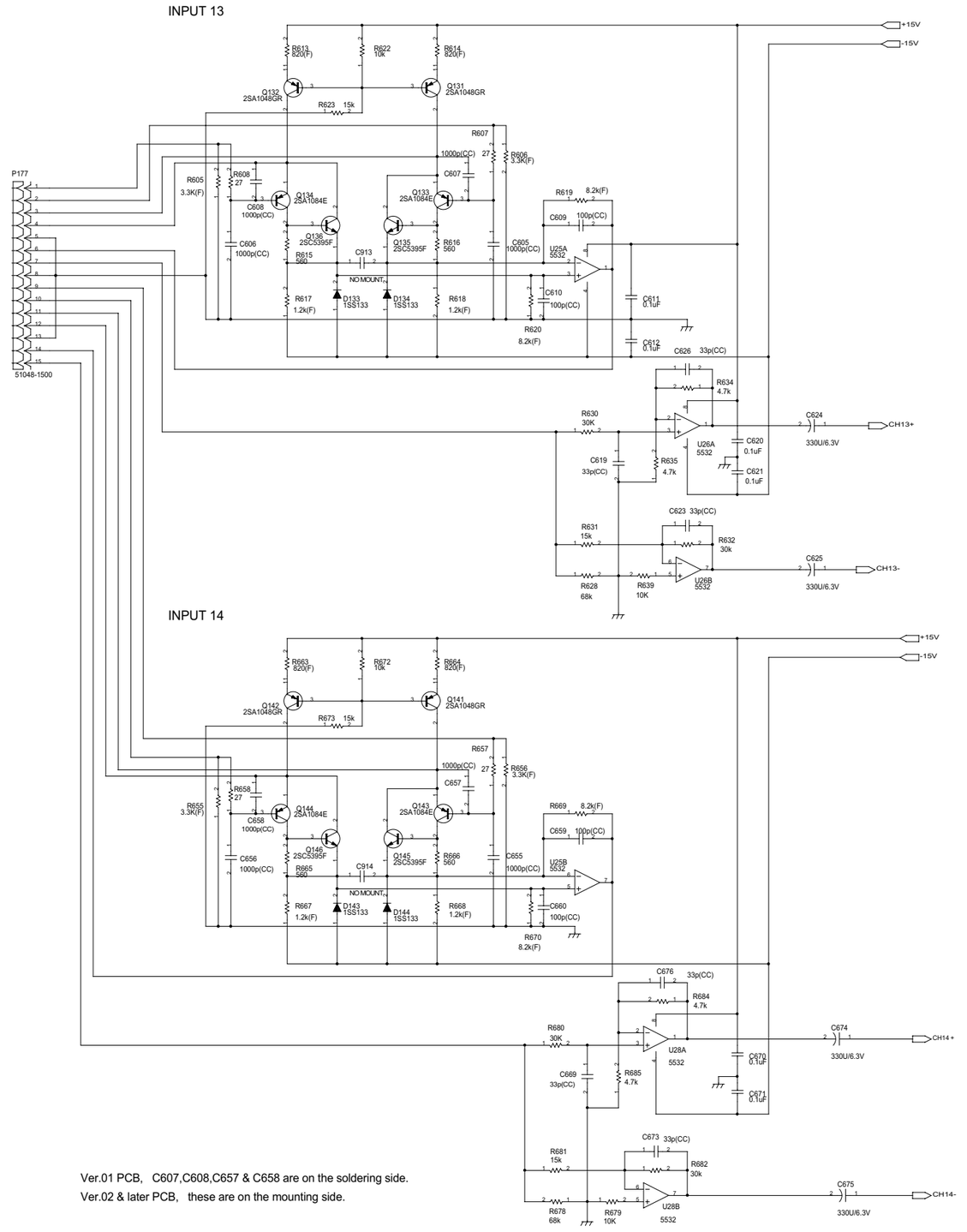
# SCHEMATIC DIAGRAM DM-24 INPUT PCB (6/9)



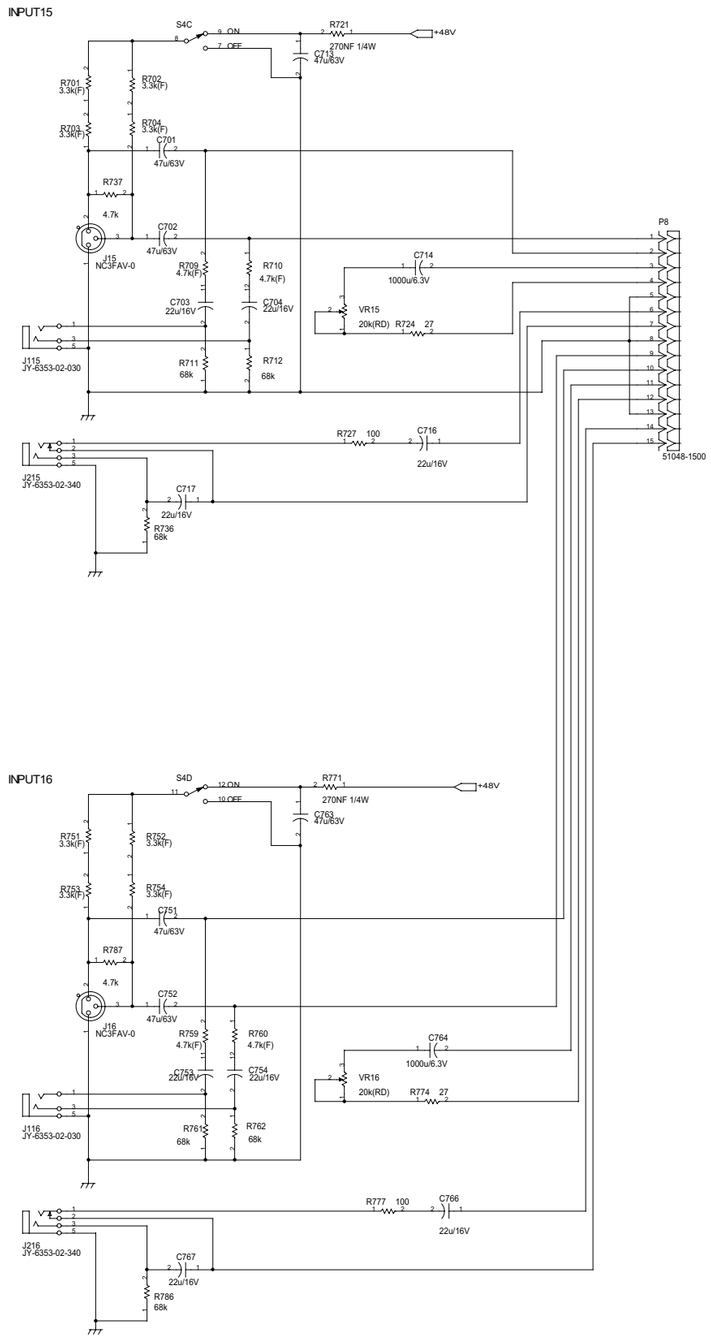

Ver.01 PCB, C507,C508,C557 & C558 are on the soldering side.
Ver.02 & later PCB, these are on the mounting side.

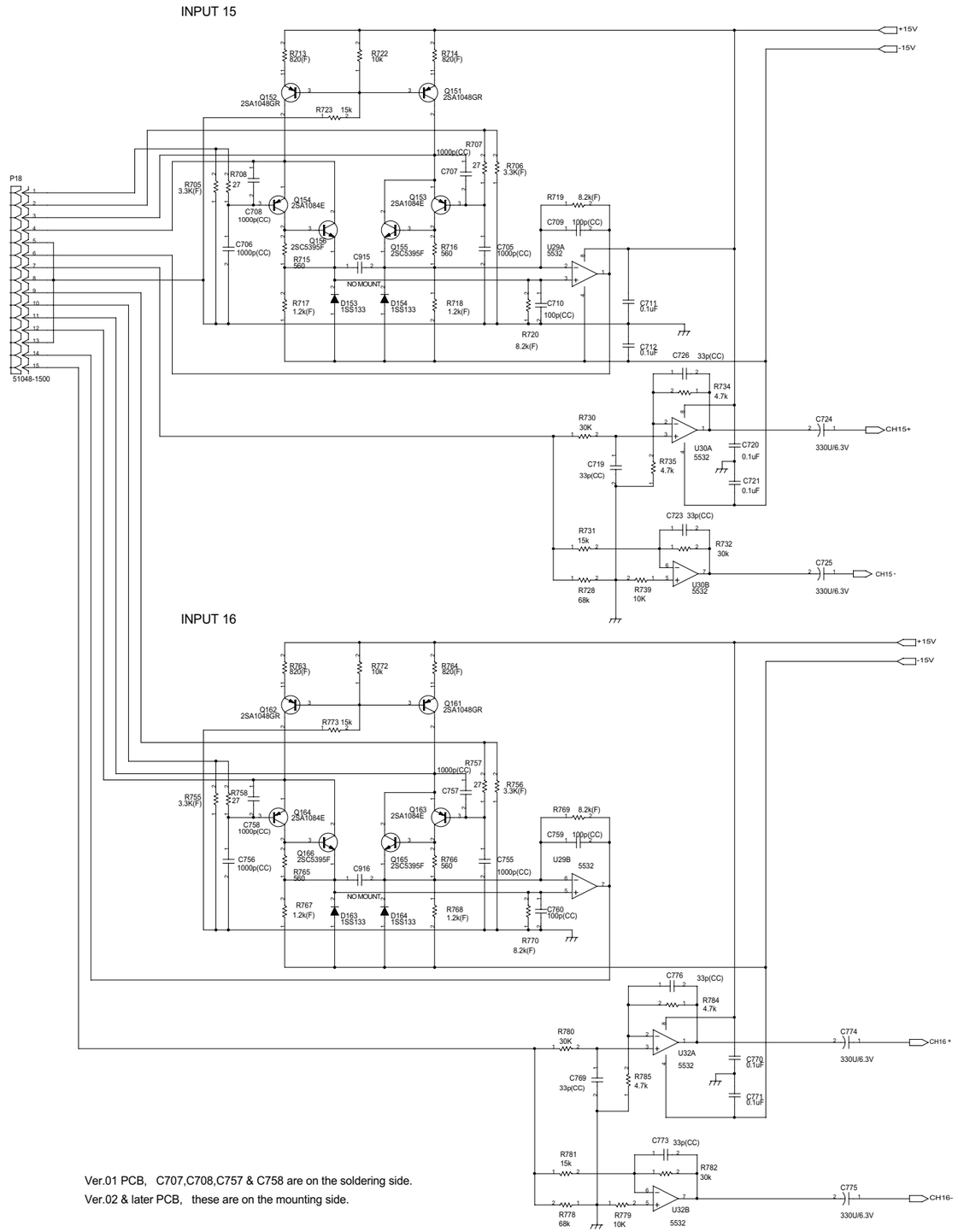


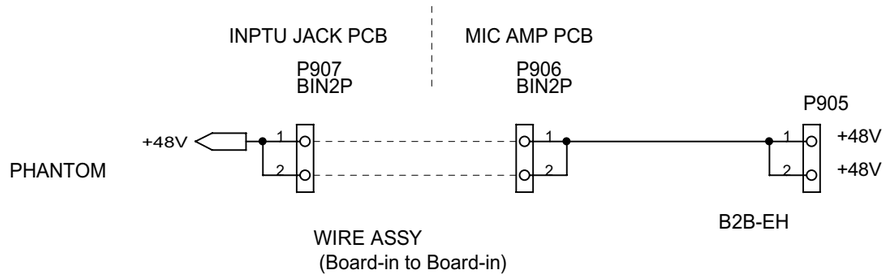

Ver.01 PCB, C607,C608,C657 & C658 are on the soldering side.
Ver.02 & later PCB, these are on the mounting side.

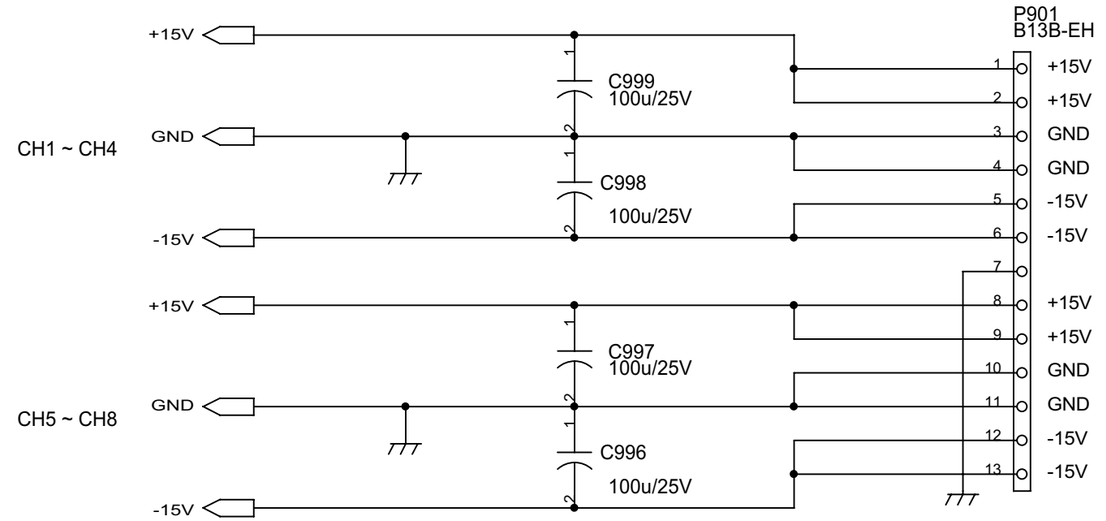
# SCHEMATIC DIAGRAM DM-24 INPUT PCB (8/9)

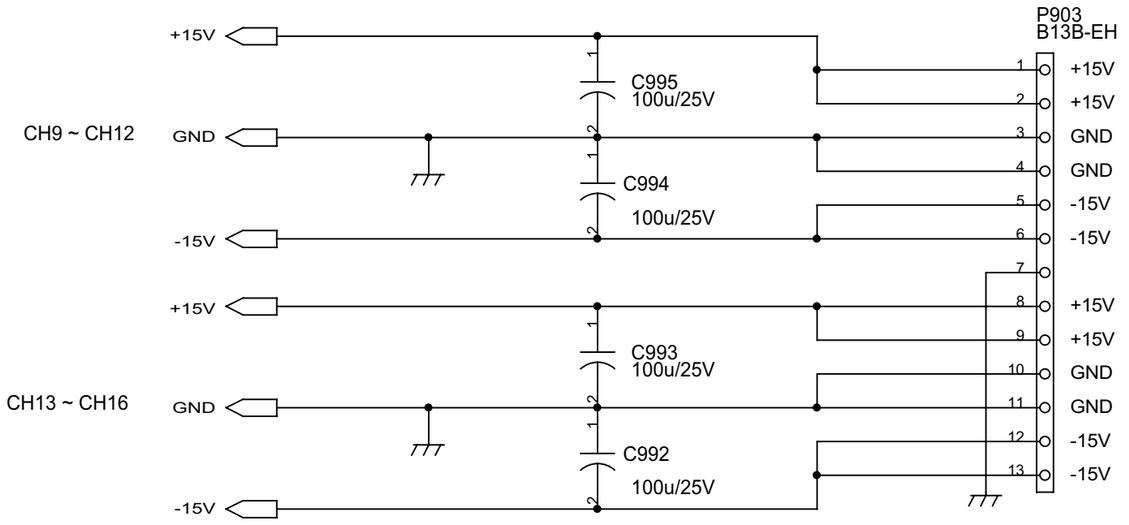


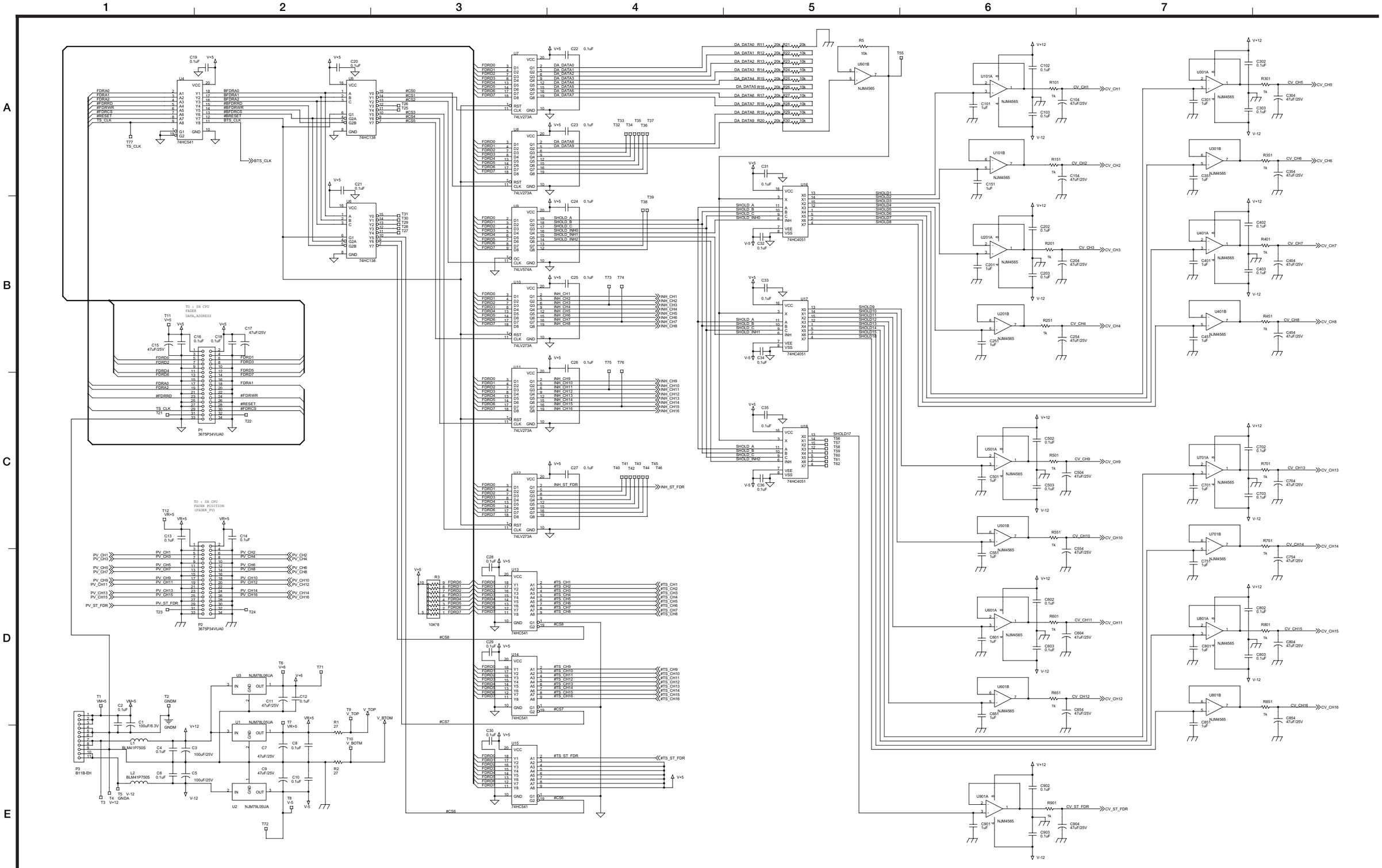




Ver.01 PCB, C707,C708,C757 & C758 are on the soldering side.
Ver.02 & later PCB, these are on the mounting side.


INPTU JACK PCB
MIC AMP PCB
P907
BIN2P
P906
BIN2P
P905
+48V
PHANTOM
+48V
+48V
B2B-EH
WIRE ASSY
(Board-in to Board-in)


P901
B13B-EH
CH1 ~ CH4
CH5 ~ CH8
+15V
GND
-15V
C999
100u/25V
C998
100u/25V
C997
100u/25V
C996
100u/25V
+15V
+15V
GND
GND
-15V
-15V
+15V
+15V
GND
GND
-15V
-15V

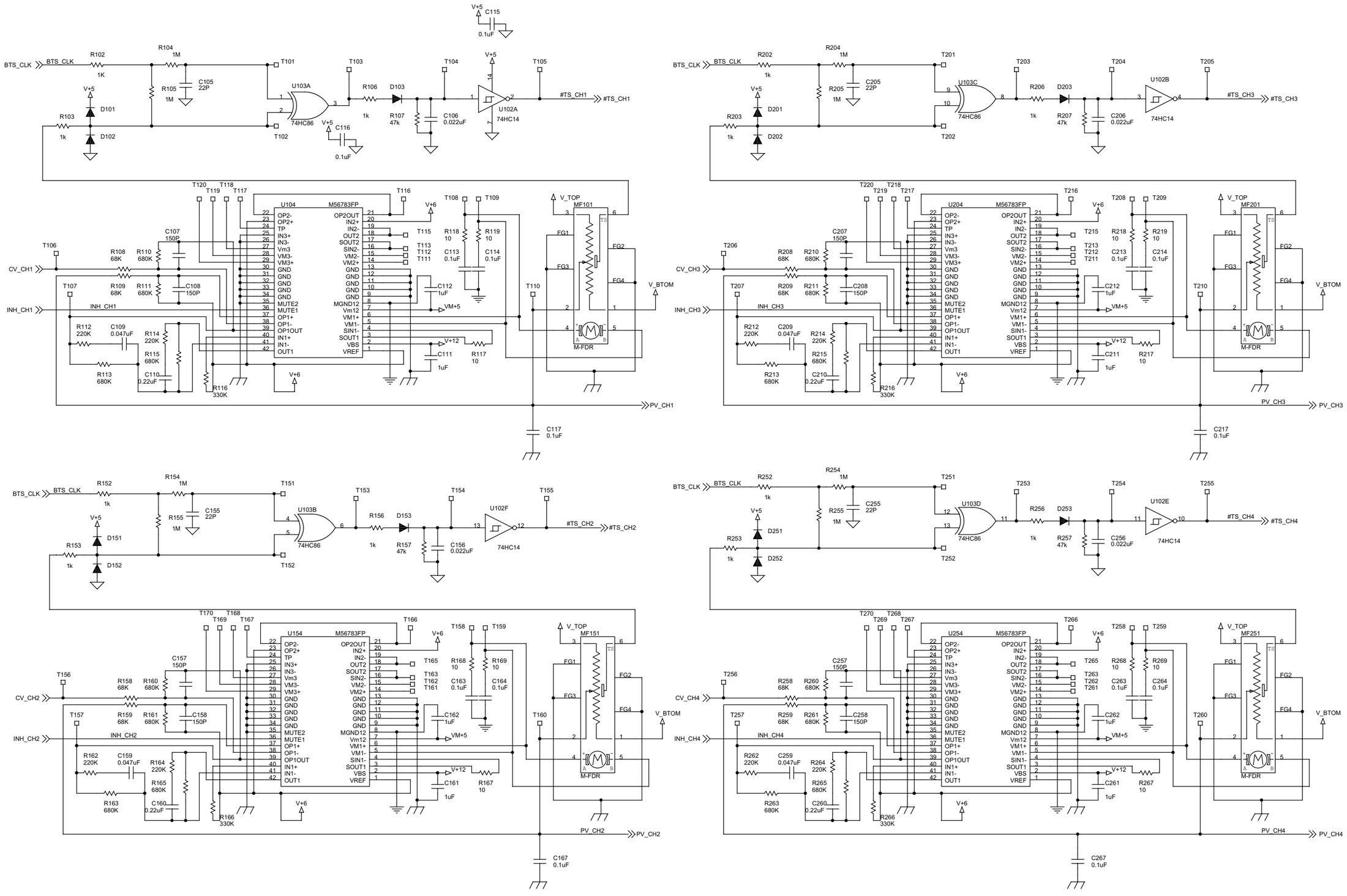

P903
B13B-EH
CH9 ~ CH12
CH13 ~ CH16
+15V
GND
-15V
C995
100u/25V
C994
100u/25V
C993
100u/25V
C992
100u/25V
+15V
+15V
GND
GND
-15V
-15V
+15V
+15V
GND
GND
-15V
-15V






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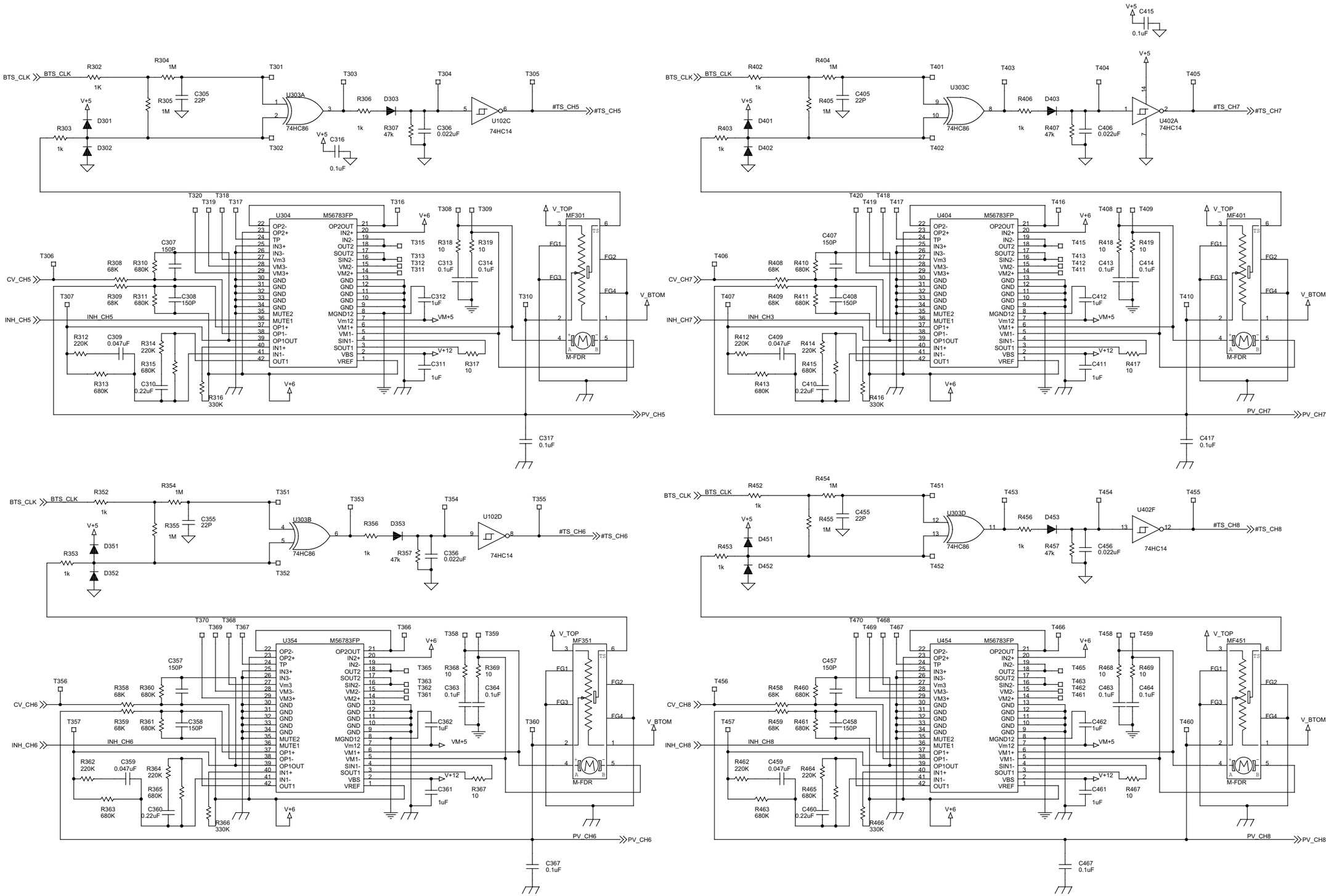
# SCHEMATIC DIAGRAM DM-24 FADER PCB (2/6)






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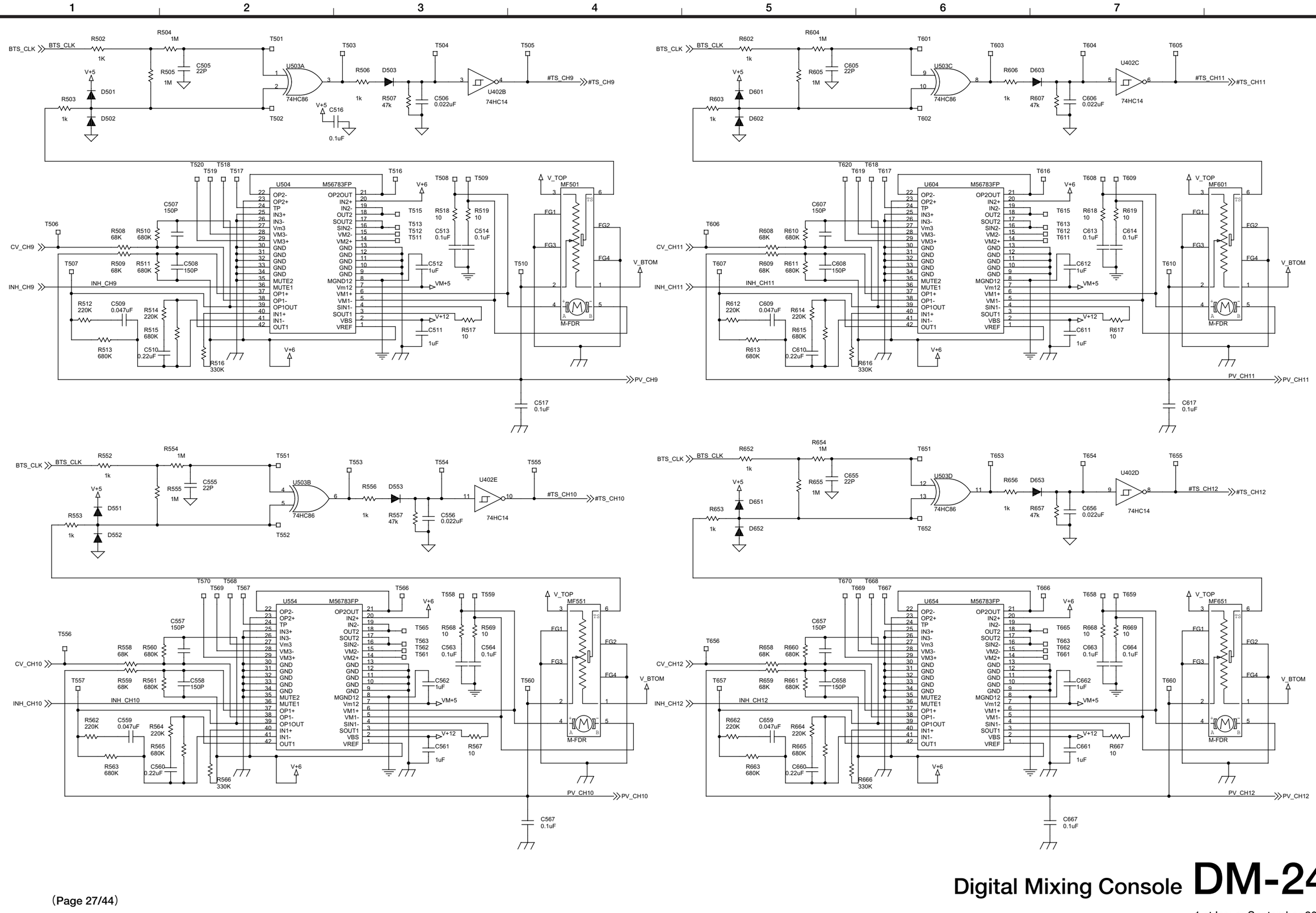
# SCHEMATIC DIAGRAM DM-24 FADER PCB (3/6)





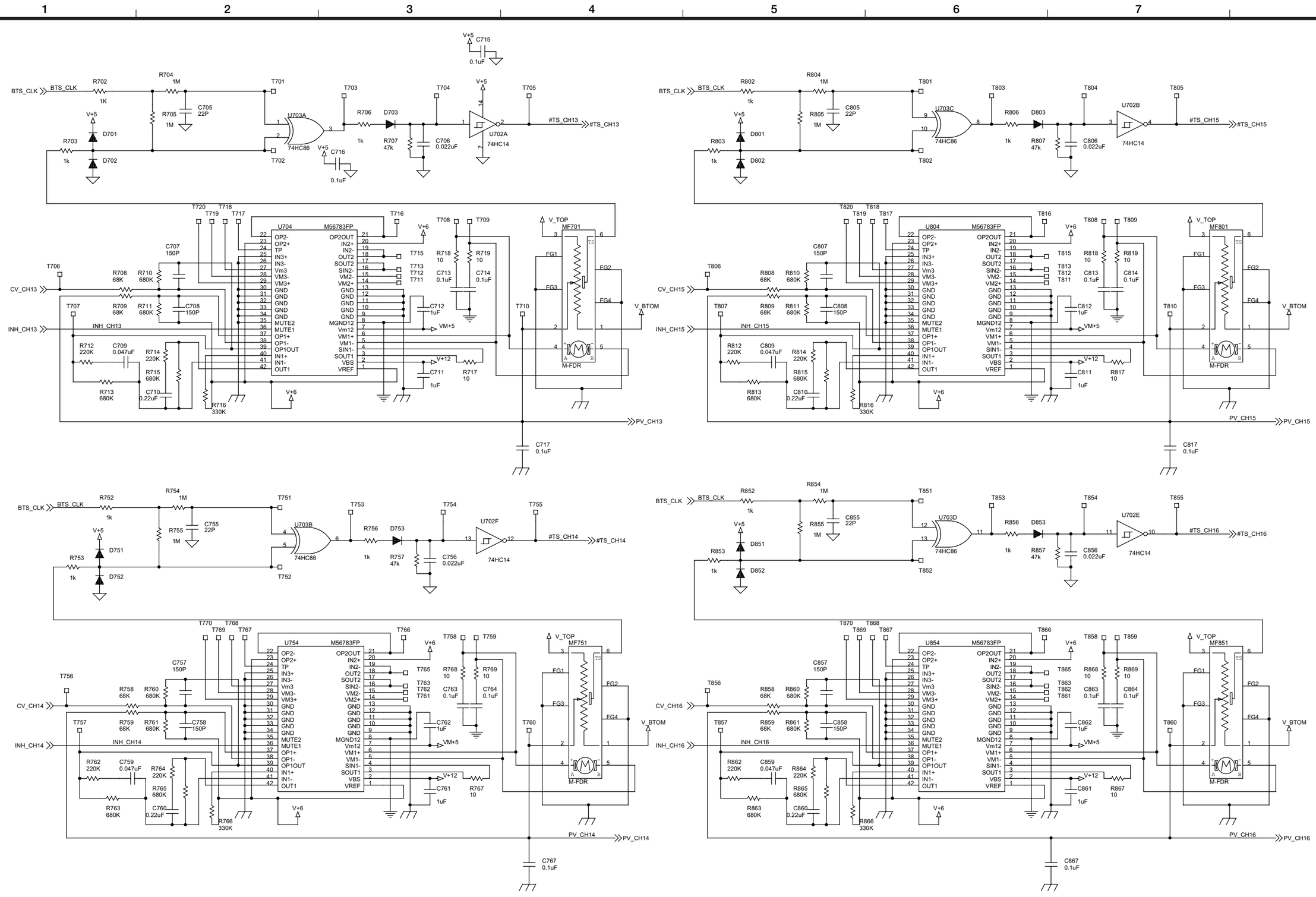

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# SCHEMATIC DIAGRAM DM-24 FADER PCB (4/6)






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Digital Mixing Console DM-24
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1 2 3 4 5 6 7

A B C D E

BTS_CLK
R902 1k
R904 1M
R905 1M
C905 22P
T901
V+5
D901
R903 1k
D902
T902
U903A 74HC86
T903
R906 1k
D903
R907 47k
T904
C906 0.022uF
U702C 74HC14
T905
#TS_ST_FDR
V+5 C916 0.1uF

T920 T918 T919 T917 T916

U904 M56783FP

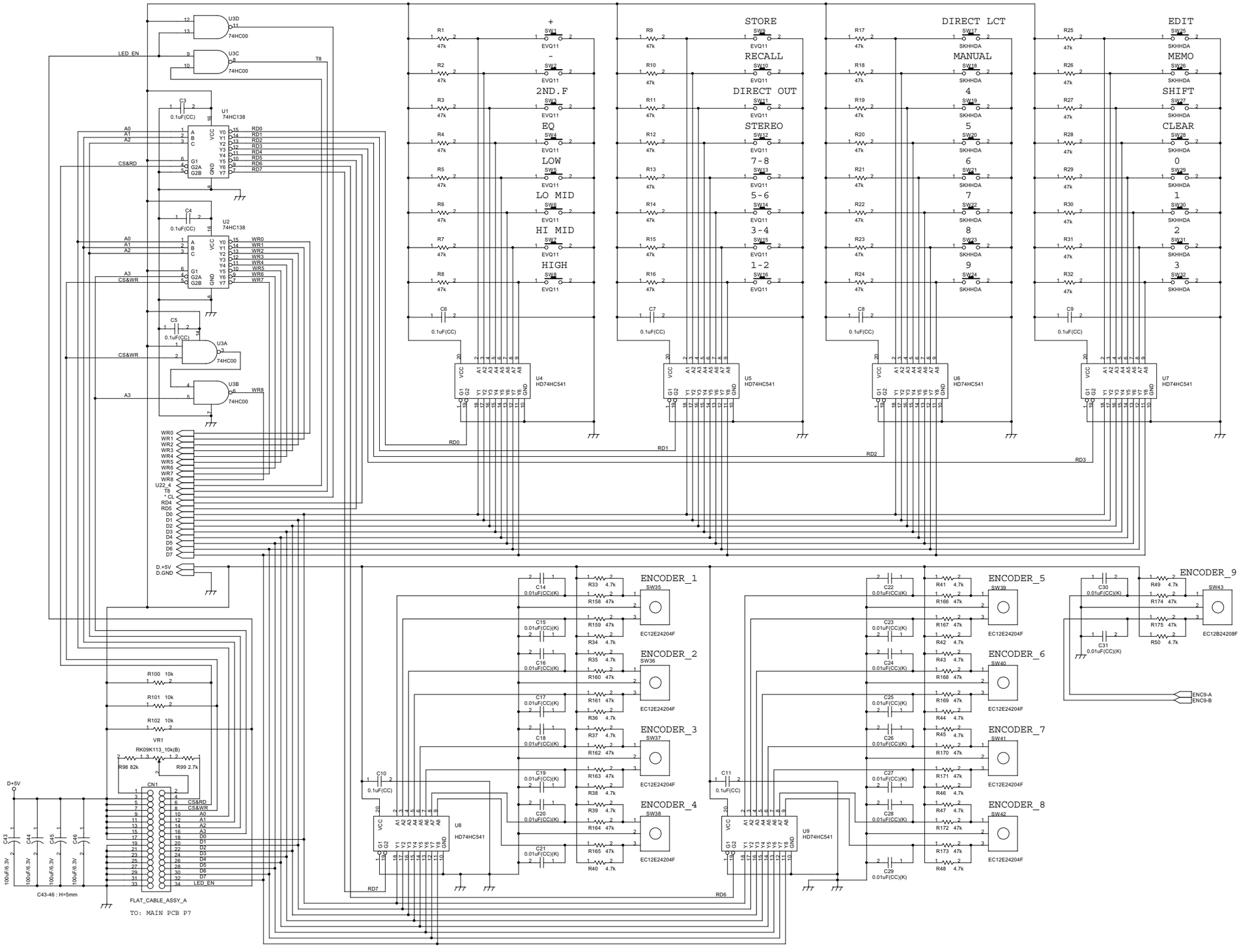
| | | | |
|---|---|---|---|
| 22 | OP2- | OP2OUT | 21 |
| 23 | OP2+ | IN2+ | 20 |
| 24 | TP | IN2- | 19 |
| 25 | IN3+ | OUT2 | 18 |
| 26 | IN3- | SOUT2 | 17 |
| 27 | Vm3 | SIN2- | 16 |
| 28 | VM3- | VM2- | 15 |
| 29 | VM3+ | VM2+ | 14 |
| 30 | GND | GND | 13 |
| 31 | GND | GND | 12 |
| 32 | GND | GND | 11 |
| 33 | GND | GND | 10 |
| 34 | GND | GND | 9 |
| 35 | GND | MGND12 | 8 |
| 36 | MUTE2 | Vm12 | 7 |
| 37 | MUTE1 | VM1+ | 6 |
| 38 | OP1+ | VM1- | 5 |
| 39 | OP1- | SIN1- | 4 |
| 40 | OP1OUT | SOUT1 | 3 |
| 41 | IN1+ | VBS | 2 |
| 42 | IN1- | VREF | 1 |
| | OUT1 | | |

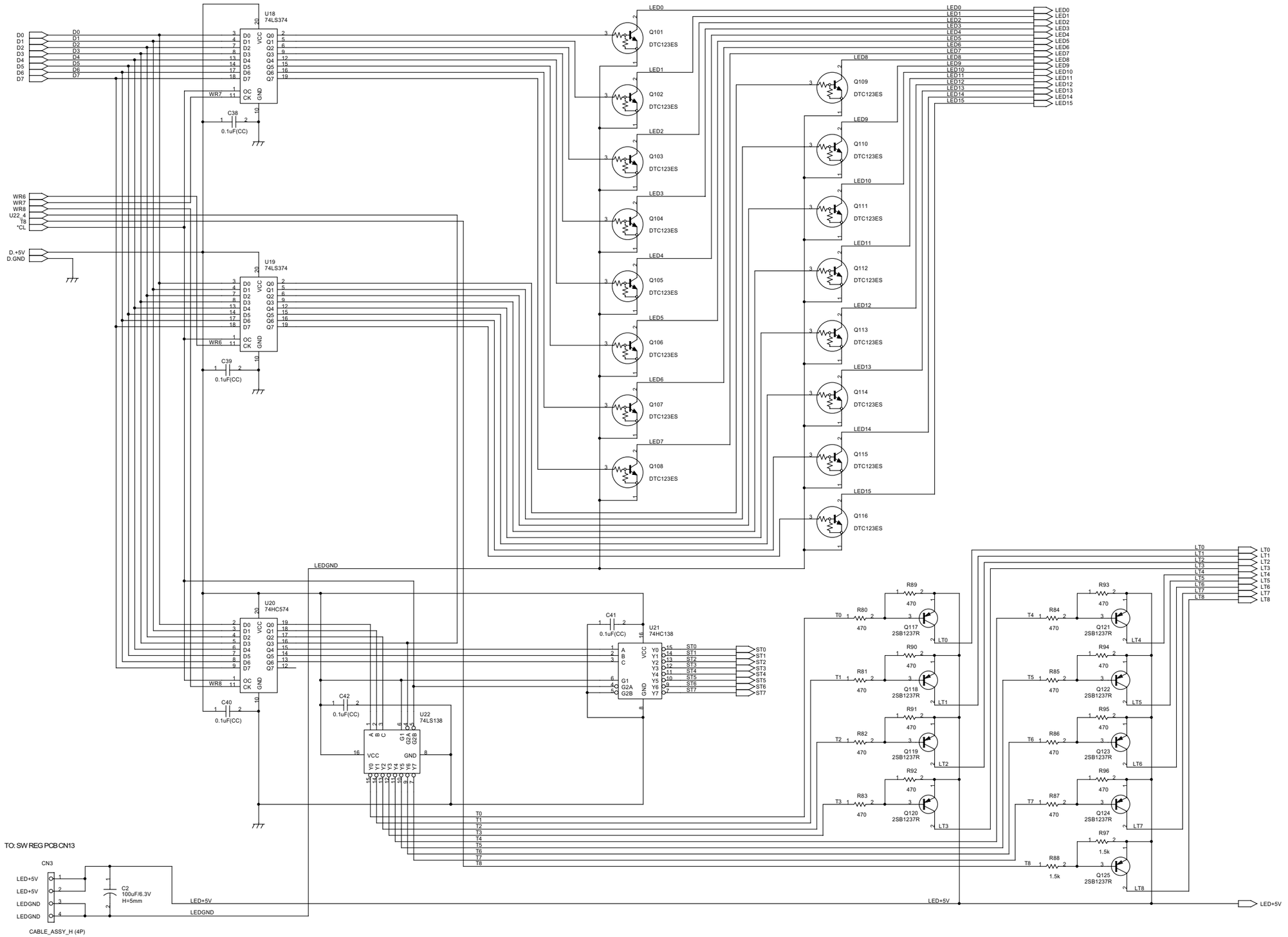
T915 T913 T912 T911
V+6
C907 150P
T906
R908 68K
R910 680K
CV_ST_FDR
T907
R909 68K
R911 680K
C908 150P
INH_ST_FDR
R912 220K
C909 0.047uF
R914 220K
R915 680K
R913 680K
C910 0.22uF
R916 330K
V+6
C912 1uF
VM+5
V+12
C911 1uF
R917 10
T908
T909
R918 10
R919 10
C913 0.1uF
C914 0.1uF
T910
V_TOP
MF901
FG1
FG2
FG3
FG4
TS
A B
M-FDR
V_BTOM
PV_ST_FDR
PV_ST_FDR
C917 0.1uF

U902,U903 POWER :
V+5(14 ), GND(7 )

U903B 74HC86
T922
U903C 74HC86
T923
U903D 74HC86
T924

U702D 74HC14
T921

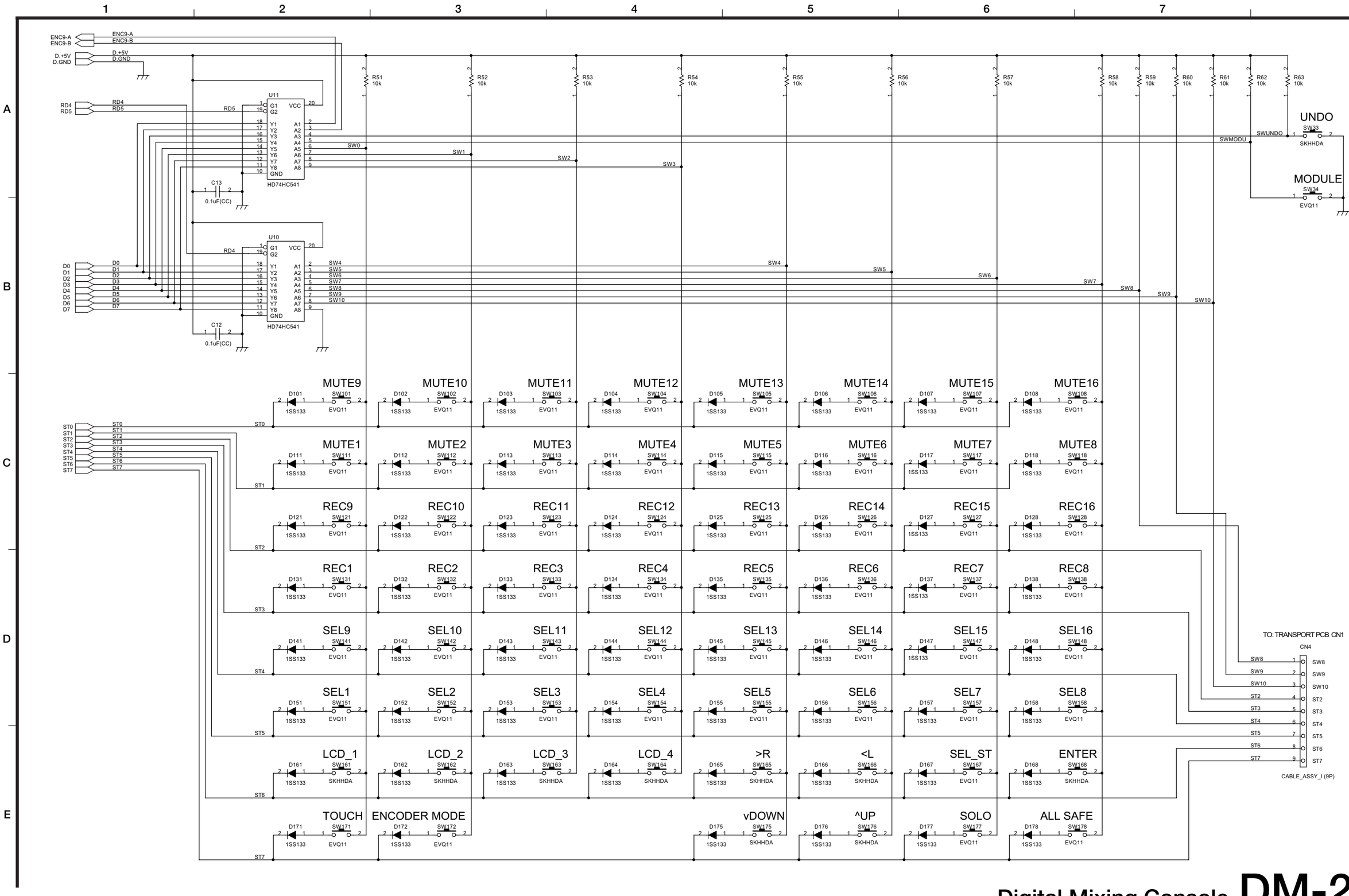

1
2
3
4
5
6
7
A
B
C
D
E
U3D
74HC00
U3C
74HC00
LED_EN
T8
C3
0.1uF(CC)
U1
74HC138
A0
A1
A2
CS&RD
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
C4
0.1uF(CC)
U2
74HC138
WR0
WR1
WR2
WR3
WR4
WR5
WR6
WR7
C5
0.1uF(CC)
U3A
74HC00
CS&WR
U3B
74HC00
A3
WR8
U22_4
T8
* CL
D0
D1
D2
D3
D4
D5
D6
D7
D.+5V
D.GND
R1
R2
R3
R4
R5
R6
R7
R8
47k
+
SW1
EVQ11
–
SW2
2ND.F
SW3
EQ
SW4
LOW
SW5
LO MID
SW6
HI MID
SW7
HIGH
SW8
C6
0.1uF(CC)
U4
HD74HC541
R9
R10
R11
R12
R13
R14
R15
R16
STORE
SW9
RECALL
SW10
DIRECT OUT
SW11
STEREO
SW12
7-8
SW13
5-6
SW14
3-4
SW15
1-2
SW16
C7
0.1uF(CC)
U5
HD74HC541
R17
R18
R19
R20
R21
R22
R23
R24
DIRECT LCT
SW17
MANUAL
SW18
4
SW19
5
SW20
6
SW21
7
SW22
8
SW23
9
SW24
SKHHDA
C8
0.1uF(CC)
U6
HD74HC541
R25
R26
R27
R28
R29
R30
R31
R32
EDIT
SW25
MEMO
SW26
SHIFT
SW27
CLEAR
SW28
0
SW29
1
SW30
2
SW31
3
SW32
C9
0.1uF(CC)
U7
HD74HC541
R100 10k
R101 10k
R102 10k
VR1
RK09K113_10k(B)
R98 82k
R99 2.7k
CN1
CS&RD
CS&WR
A0
A1
A2
A3
D0
D1
D2
D3
D4
D5
D6
D7
LED_EN
D+5V
C43
C44
C45
C46
100uF/6.3V
C43-46 : H=5mm
FLAT_CABLE_ASSY_A
TO: MAIN PCB P7
C14
C15
C16
C17
C18
C19
C20
C21
0.01uF(CC)(K)
R33
R158
R159
R34
R35
R160
R161
R36
R37
R162
R163
R38
R39
R164
R165
R40
4.7k
ENCODER_1
SW35
ENCODER_2
SW36
ENCODER_3
SW37
ENCODER_4
SW38
EC12E24204F
C10
0.1uF(CC)
U8
HD74HC541
C22
C23
C24
C25
C26
C27
C28
C29
R41
R166
R167
R42
R43
R168
R169
R44
R45
R170
R171
R46
R47
R172
R173
R48
ENCODER_5
SW39
ENCODER_6
SW40
ENCODER_7
SW41
ENCODER_8
SW42
C11
0.1uF(CC)
U9
HD74HC541
C30
C31
R49
R174
R175
R50
ENCODER_9
SW43
EC12B24208F
ENC9-A
ENC9-B

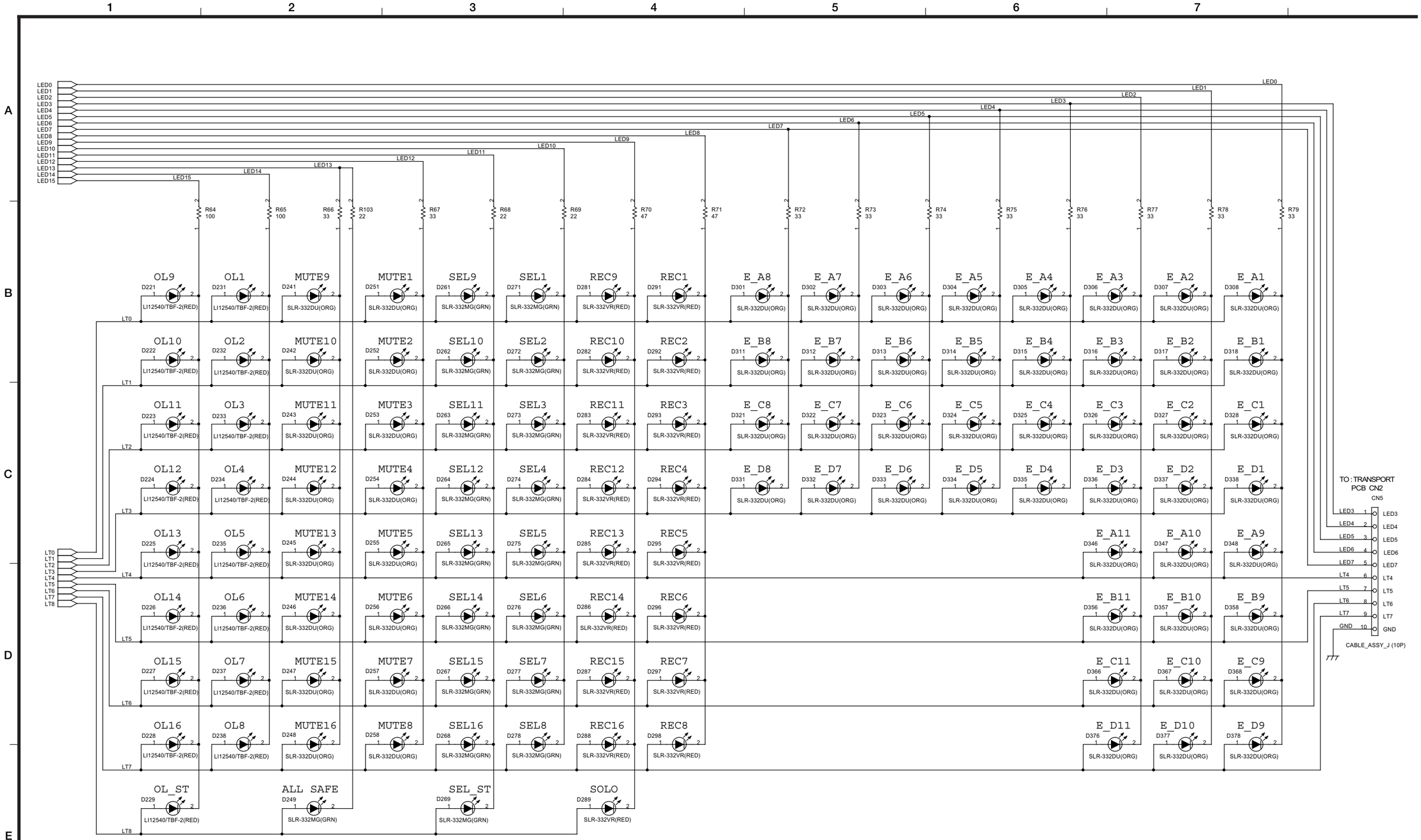





Digital Mixing Console DM-24

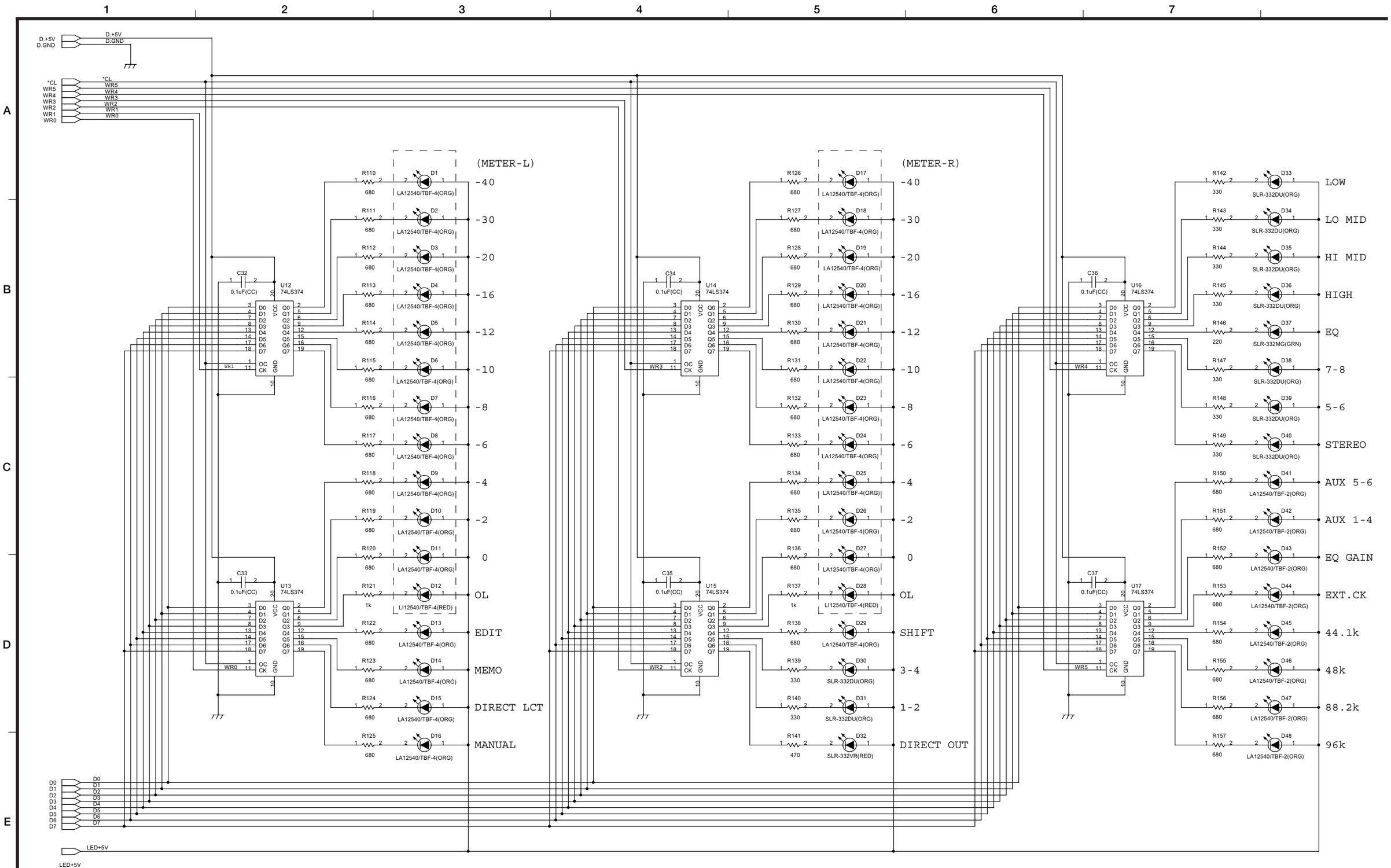
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ENC9-A
ENC9-B
D.+5V
D.GND
RD4
RD5
D0
D1
D2
D3
D4
D5
D6
D7
U11
U10
HD74HC541
C13
C12
0.1uF(CC)
R51 10k
R52 10k
R53 10k
R54 10k
R55 10k
R56 10k
R57 10k
R58 10k
R59 10k
R60 10k
R61 10k
R62 10k
R63 10k
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SWMODU
SWUNDO
UNDO
SW33
SKHHDA
MODULE
SW34
EVQ11
ST0
ST1
ST2
ST3
ST4
ST5
ST6
ST7
MUTE1
MUTE2
MUTE3
MUTE4
MUTE5
MUTE6
MUTE7
MUTE8
MUTE9
MUTE10
MUTE11
MUTE12
MUTE13
MUTE14
MUTE15
MUTE16
REC1
REC2
REC3
REC4
REC5
REC6
REC7
REC8
REC9
REC10
REC11
REC12
REC13
REC14
REC15
REC16
SEL1
SEL2
SEL3
SEL4
SEL5
SEL6
SEL7
SEL8
SEL9
SEL10
SEL11
SEL12
SEL13
SEL14
SEL15
SEL16
LCD_1
LCD_2
LCD_3
LCD_4
>R
<L
SEL_ST
ENTER
TOUCH
ENCODER MODE
vDOWN
^UP
SOLO
ALL SAFE
1SS133
TO: TRANSPORT PCB CN1
CN4
CABLE_ASSY_I (9P)





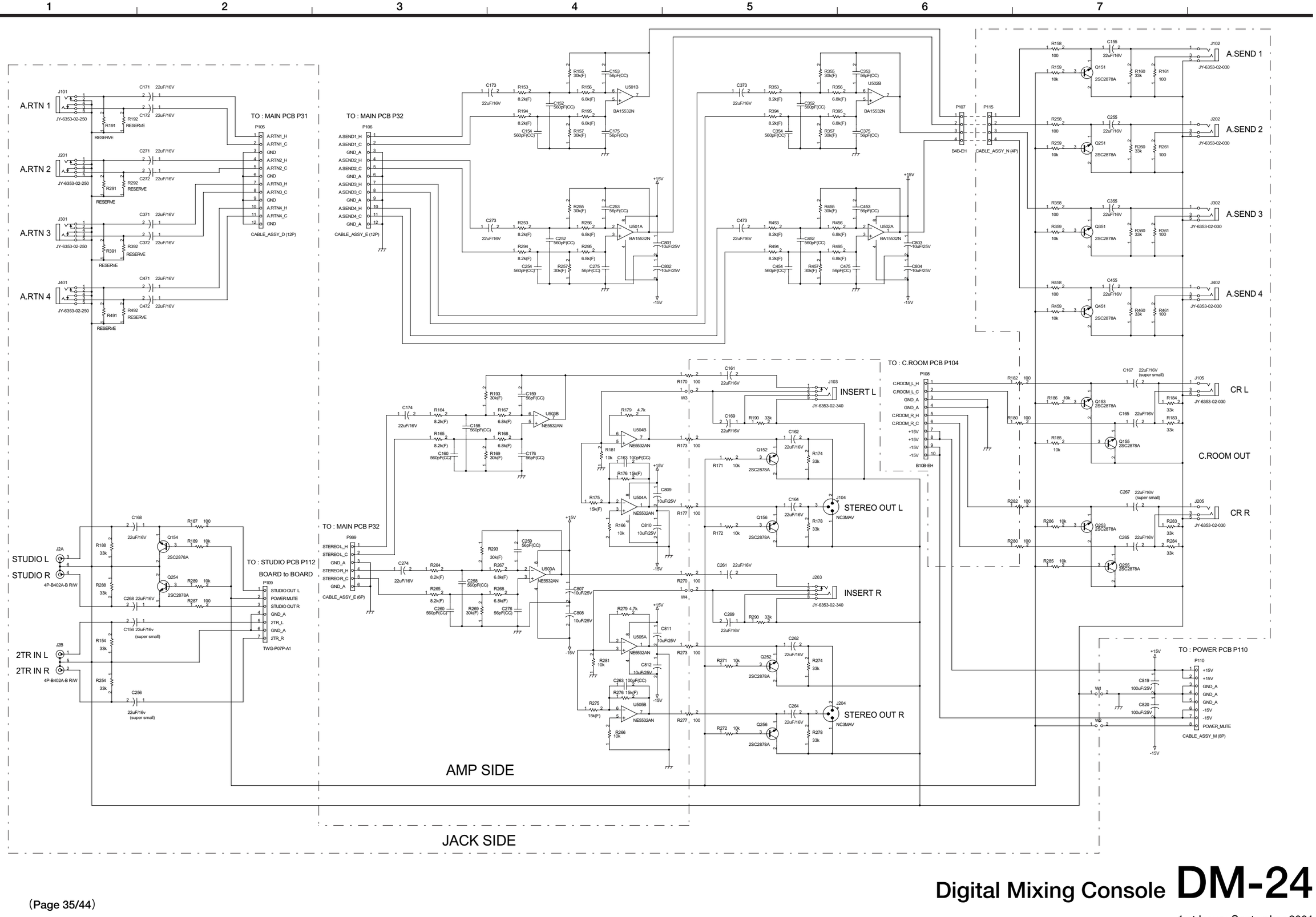

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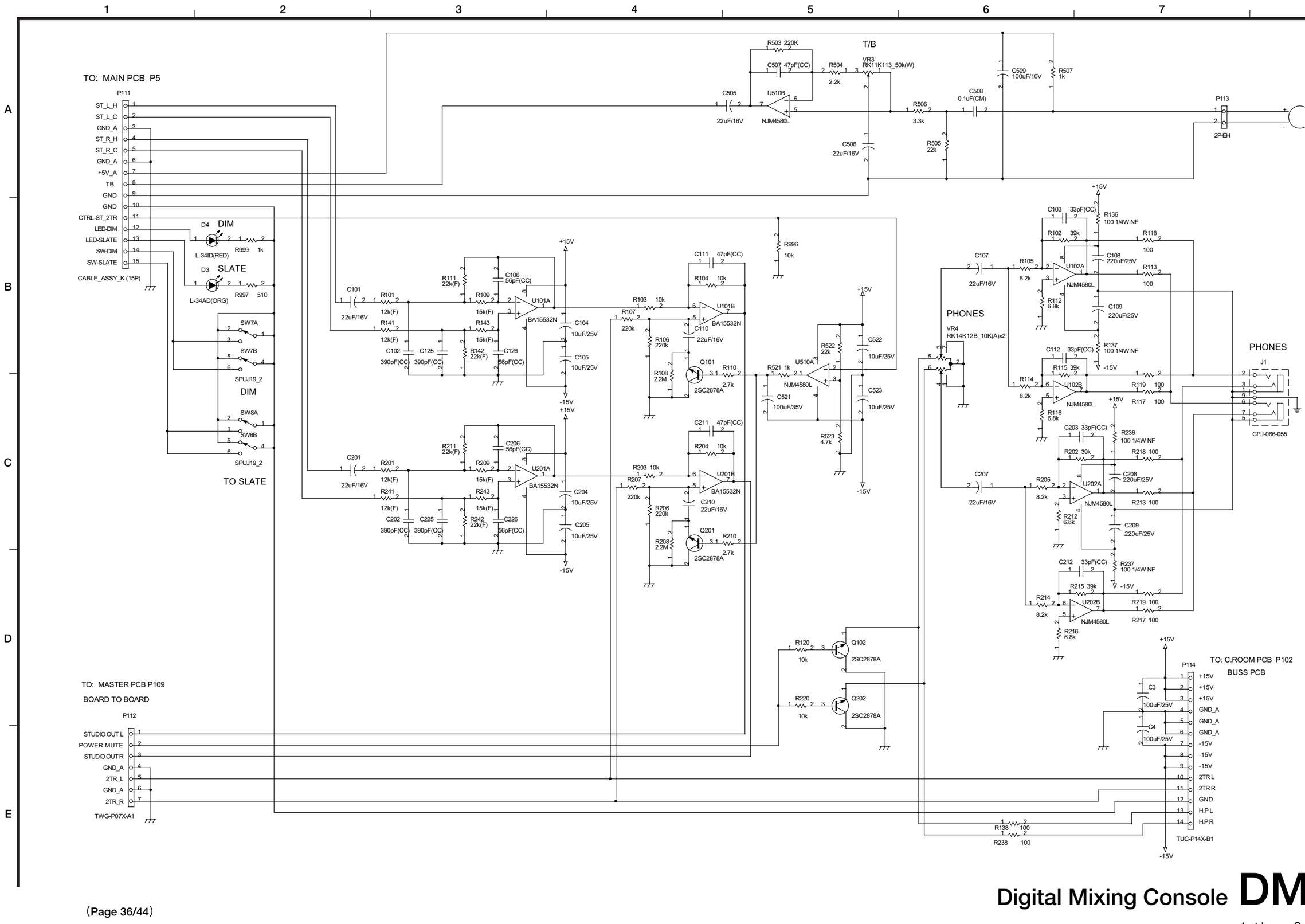
# SCHEMATIC DIAGRAM DM-24 MASTER PCB






Digital Mixing Console **DM-24**

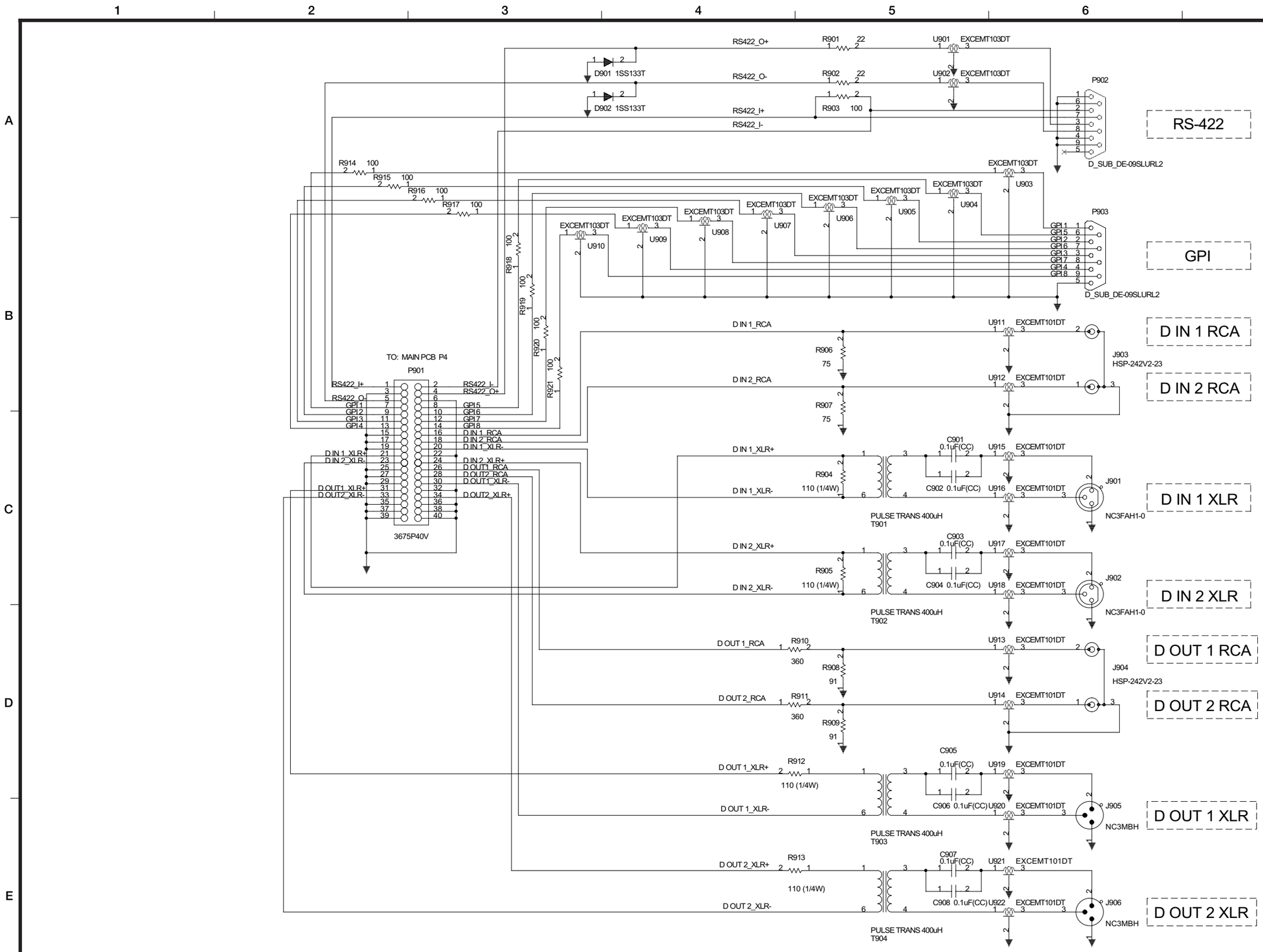
1 st Issue; September 2001

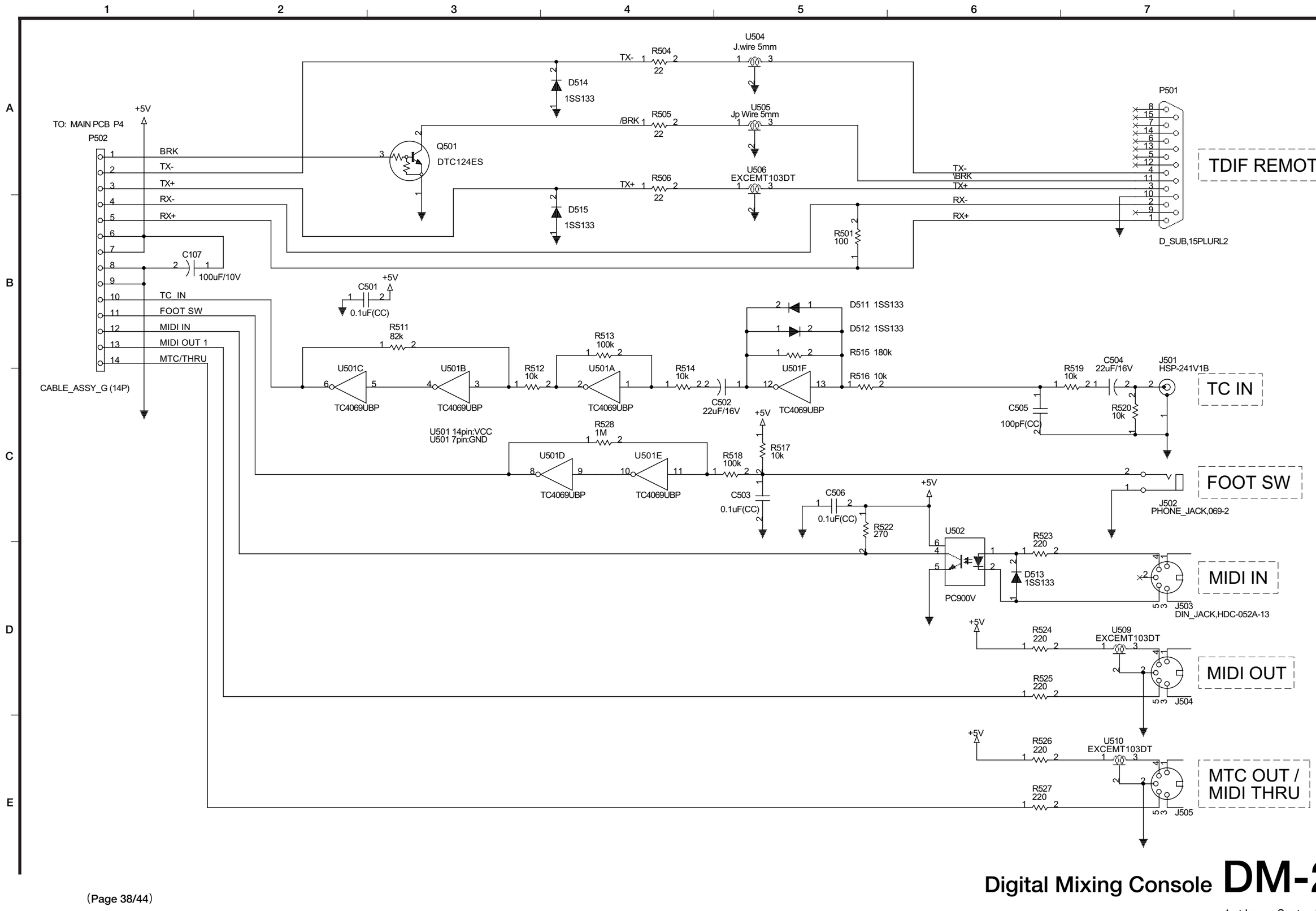


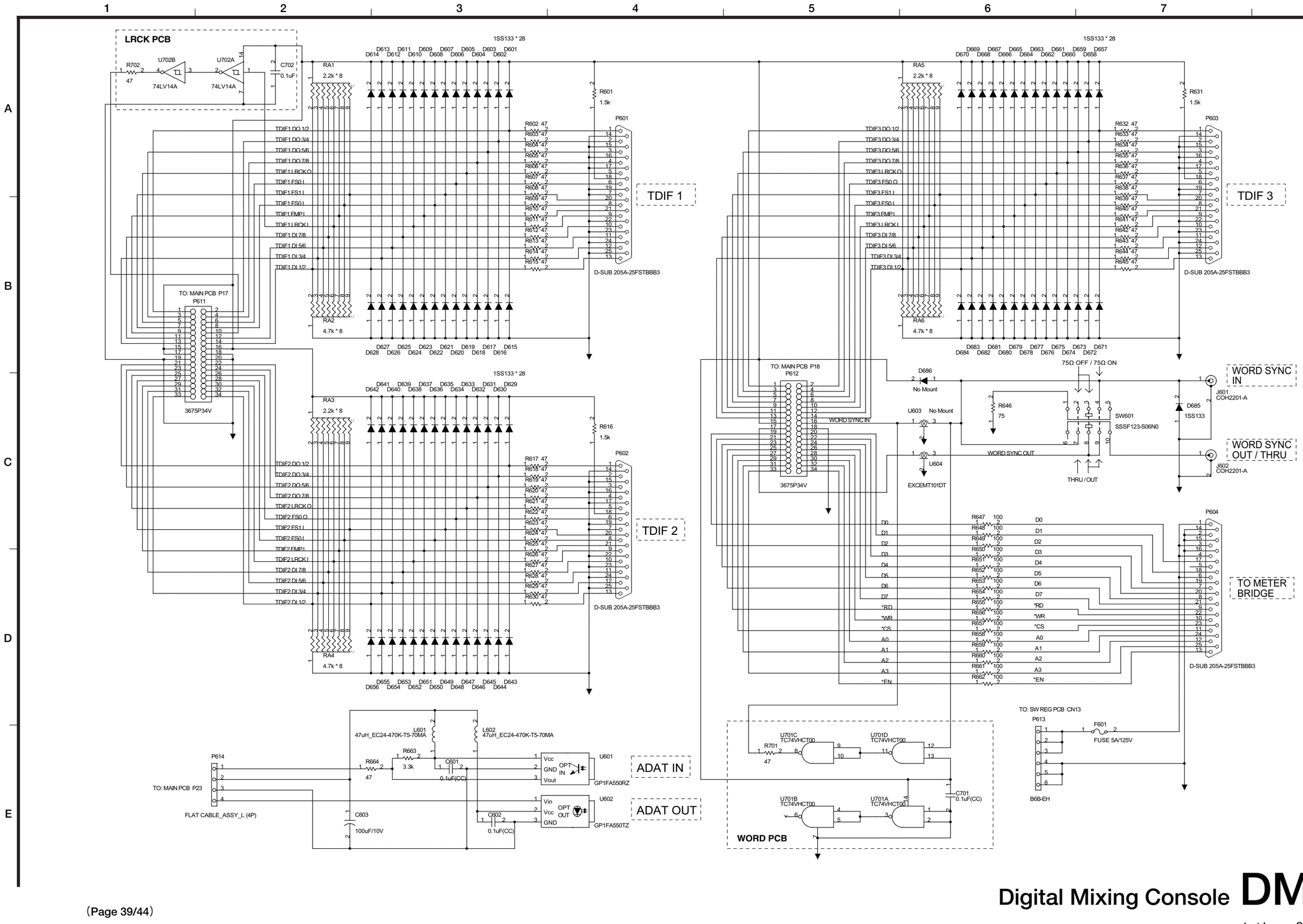


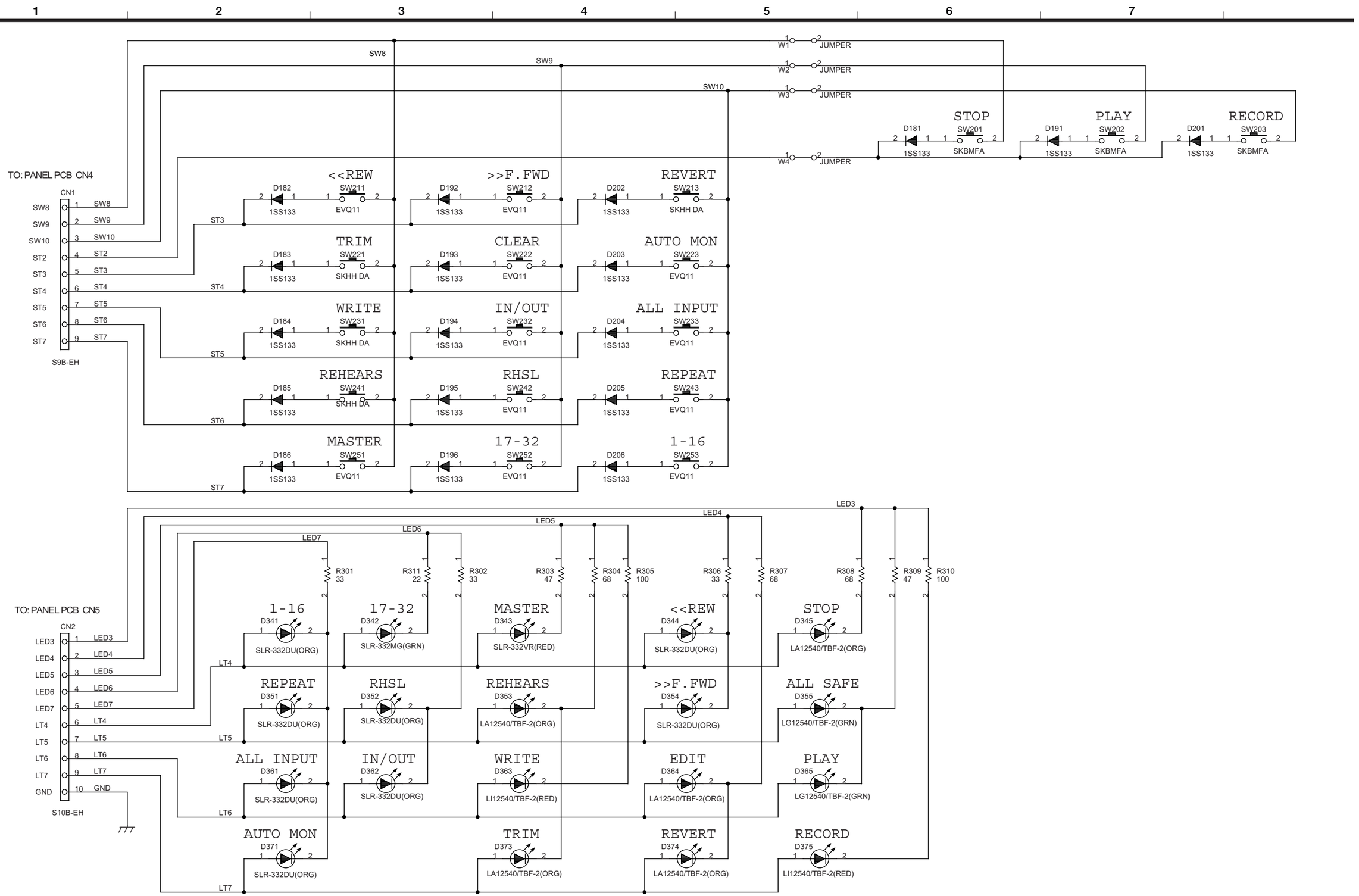

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RS422_O+
RS422_O-
RS422_I+
RS422_I-
D901 1SS133T
D902 1SS133T
R901 22
R902 22
R903 100
U901 EXCEMT103DT
U902 EXCEMT103DT
P902
D_SUB_DE-09SLURL2
RS-422
R914 100
R915 100
R916 100
R917 100
R918 100
R919 100
R920 100
R921 100
U903 EXCEMT103DT
U904 EXCEMT103DT
U905 EXCEMT103DT
U906 EXCEMT103DT
U907 EXCEMT103DT
U908 EXCEMT103DT
U909 EXCEMT103DT
U910 EXCEMT103DT
P903
GPI1
GPI5
GPI2
GPI6
GPI3
GPI7
GPI4
GPI8
D_SUB_DE-09SLURL2
GPI
TO: MAIN PCB P4
P901
3675P40V
D IN 1_RCA
D IN 2_RCA
R906 75
R907 75
U911 EXCEMT101DT
U912 EXCEMT101DT
J903
HSP-242V2-23
D IN 1 RCA
D IN 2 RCA
D IN 1_XLR+
D IN 1_XLR-
D IN 2_XLR+
D IN 2_XLR-
R904 110 (1/4W)
R905 110 (1/4W)
C901 0.1uF(CC)
C902 0.1uF(CC)
C903 0.1uF(CC)
C904 0.1uF(CC)
U915 EXCEMT101DT
U916 EXCEMT101DT
U917 EXCEMT101DT
U918 EXCEMT101DT
J901
J902
NC3FAH1-0
PULSE TRANS 400uH
T901
T902
D IN 1 XLR
D IN 2 XLR
D OUT 1_RCA
D OUT 2_RCA
R910 360
R911 360
R908 91
R909 91
U913 EXCEMT101DT
U914 EXCEMT101DT
J904
HSP-242V2-23
D OUT 1 RCA
D OUT 2 RCA
D OUT 1_XLR+
D OUT 1_XLR-
D OUT 2_XLR+
D OUT 2_XLR-
R912 110 (1/4W)
R913 110 (1/4W)
C905 0.1uF(CC)
C906 0.1uF(CC)
C907 0.1uF(CC)
C908 0.1uF(CC)
U919 EXCEMT101DT
U920 EXCEMT101DT
U921 EXCEMT101DT
U922 EXCEMT101DT
J905
J906
NC3MBH
PULSE TRANS 400uH
T903
T904
D OUT 1 XLR
D OUT 2 XLR

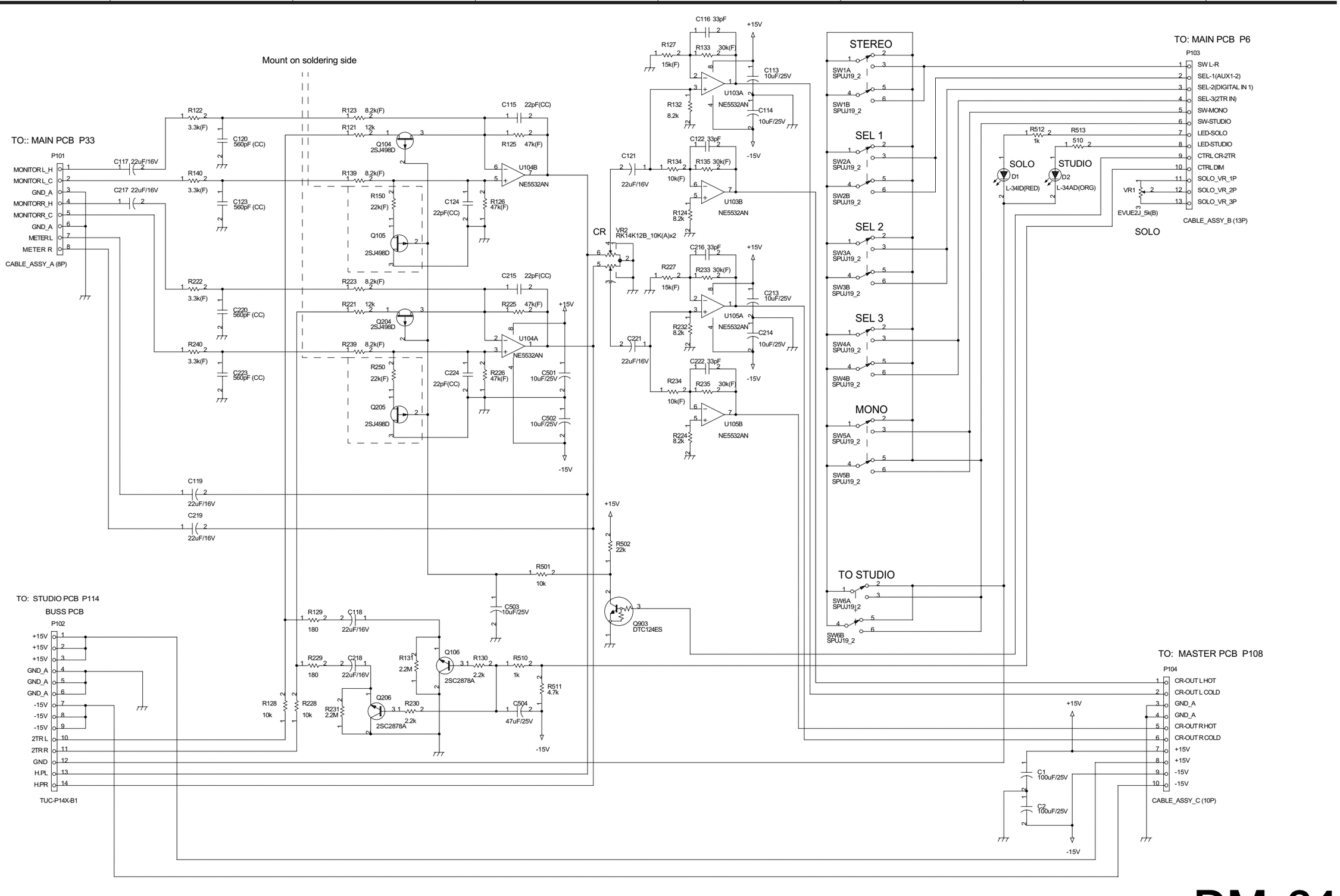

1
2
3
4
5
6
7
A
B
C
D
E
TO: MAIN PCB P4
P502
+5V
BRK
TX-
TX+
RX-
RX+
TC_IN
FOOT SW
MIDI IN
MIDI OUT 1
MTC/THRU
CABLE_ASSY_G (14P)
C107
100uF/10V
Q501
DTC124ES
R504
22
R505
22
R506
22
D514
1SS133
D515
1SS133
U504
J.wire 5mm
U505
Jp Wire 5mm
U506
EXCEMT103DT
R501
100
P501
D_SUB,15PLURL2
TDIF REMOTE
C501
0.1uF(CC)
R511
82k
U501C
U501B
TC4069UBP
R512
10k
R513
100k
U501A
R514
10k
C502
22uF/16V
U501F
D511 1SS133
D512 1SS133
R515 180k
R516 10k
R519
10k
C504
22uF/16V
J501
HSP-241V1B
TC IN
C505
100pF(CC)
R520
10k
U501 14pin:VCC
U501 7pin:GND
R528
1M
U501D
U501E
R518
100k
R517
10k
C503
0.1uF(CC)
C506
0.1uF(CC)
R522
270
J502
PHONE_JACK,069-2
FOOT SW
U502
PC900V
R523
220
D513
1SS133
J503
DIN_JACK,HDC-052A-13
MIDI IN
R524
220
U509
EXCEMT103DT
R525
220
J504
MIDI OUT
R526
220
U510
EXCEMT103DT
R527
220
J505
MTC OUT /
MIDI THRU


LRCK PCB
R702
47
U702B
74LV14A
U702A
74LV14A
C702
0.1uF
1SS133 * 28
RA1
2.2k * 8
RA2
4.7k * 8
R601
1.5k
P601
D-SUB 205A-25FSTBBB3
TDIF 1
TDIF1 DO 1/2
TDIF1 DO 3/4
TDIF1 DO 5/6
TDIF1 DO 7/8
TDIF1 LRCK O
TDIF1 FS0 I
TDIF1 FS1 I
TDIF1 FS0 I
TDIF1 EMP I
TDIF1 LRCK I
TDIF1 DI 7/8
TDIF1 DI 5/6
TDIF1 DI 3/4
TDIF1 DI 1/2
TO: MAIN PCB P17
P611
3675P34V
RA3
RA4
R616
P602
TDIF 2
TDIF2 DO 1/2
TDIF2 DO 3/4
TDIF2 DO 5/6
TDIF2 DO 7/8
TDIF2 LRCK O
TDIF2 FS0 O
TDIF2 FS1 I
TDIF2 FS0 I
TDIF2 EMP I
TDIF2 LRCK I
TDIF2 DI 7/8
TDIF2 DI 5/6
TDIF2 DI 3/4
TDIF2 DI 1/2
RA5
RA6
R631
P603
TDIF 3
TDIF3 DO 1/2
TDIF3 DO 3/4
TDIF3 DO 5/6
TDIF3 DO 7/8
TDIF3 LRCK O
TDIF3 FS0 O
TDIF3 FS1 I
TDIF3 FS0 I
TDIF3 EMP I
TDIF3 LRCK I
TDIF3 DI 7/8
TDIF3 DI 5/6
TDIF3 DI 3/4
TDIF3 DI 1/2
TO: MAIN PCB P18
P612
WORD SYNC IN
U603 No Mount
U604
EXCEMT101DT
WORD SYNC OUT
THRU / OUT
75Ω OFF / 75Ω ON
D686
No Mount
R646
75
SW601
SSSF123-S06N0
D685
1SS133
WORD SYNC IN
J601
COH2201-A
WORD SYNC OUT / THRU
J602
COH2201-A
P604
TO METER BRIDGE
D0
D1
D2
D3
D4
D5
D6
D7
*RD
*WR
*CS
A0
A1
A2
A3
*EN
TO: SW REG PCB CN13
P613
F601
FUSE 5A/125V
B6B-EH
L601
47uH_EC24-470K-T5-70MA
L602
47uH_EC24-470K-T5-70MA
R663
3.3k
R664
47
C601
0.1uF(CC)
U601
GP1FA550RZ
ADAT IN
U602
GP1FA550TZ
ADAT OUT
C602
0.1uF(CC)
C603
100uF/10V
P614
TO: MAIN PCB P23
FLAT CABLE_ASSY_L (4P)
U701C TC74VHCT00
U701D TC74VHCT00
U701B TC74VHCT00
U701A TC74VHCT00
R701
47
C701
0.1uF(CC)
WORD PCB






Digital Mixing Console DM-24
1 st Issue; September 2001





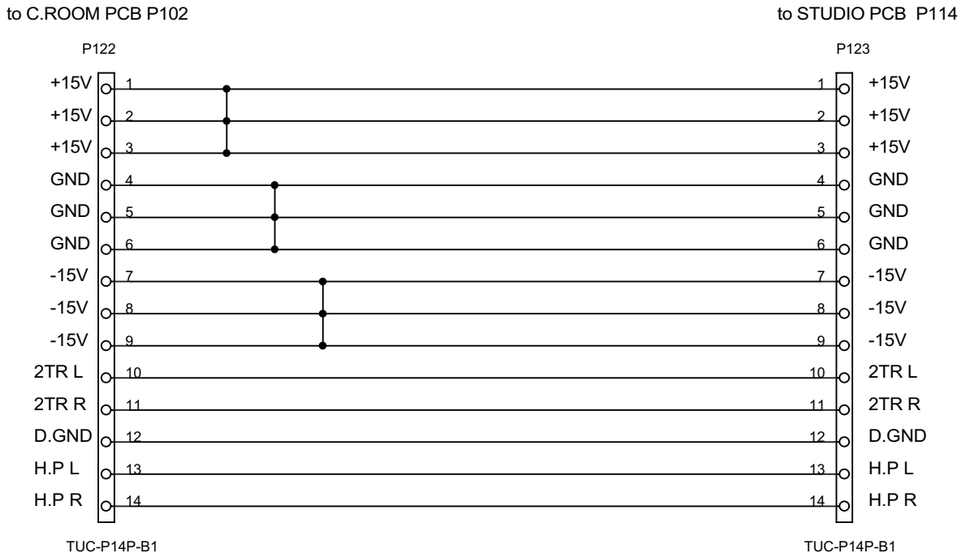

Digital Mixing Console DM-24

1 st Issue; September 2001

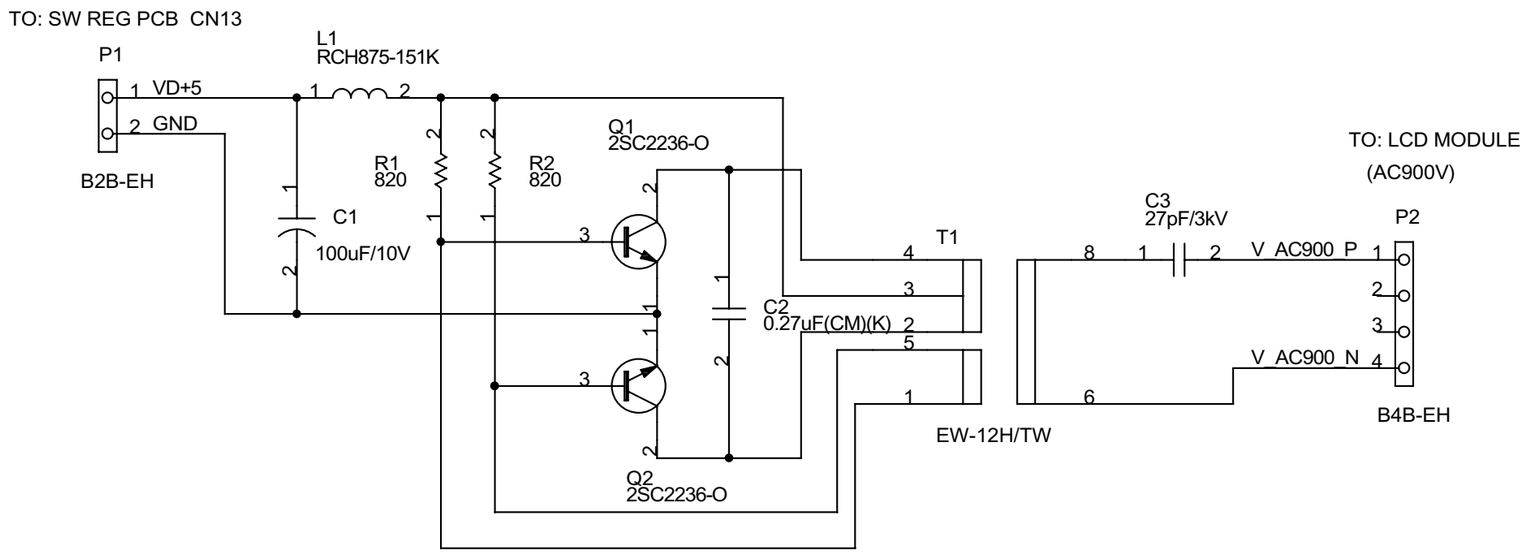
1 2 3 4 5 6 7

A B C D E

**BUSS PCB**



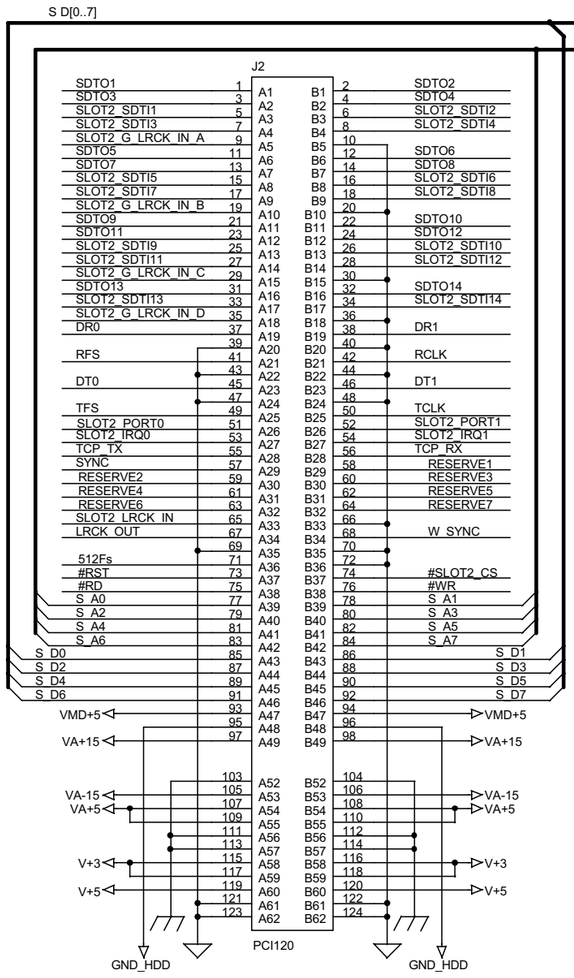

**LCD SUB PCB**



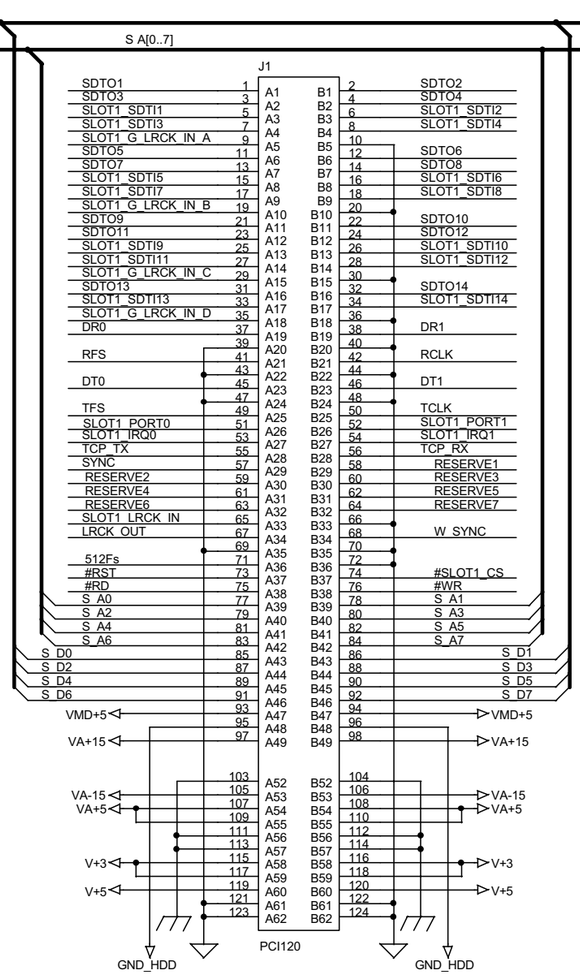
1 2 3 4 5 6 7

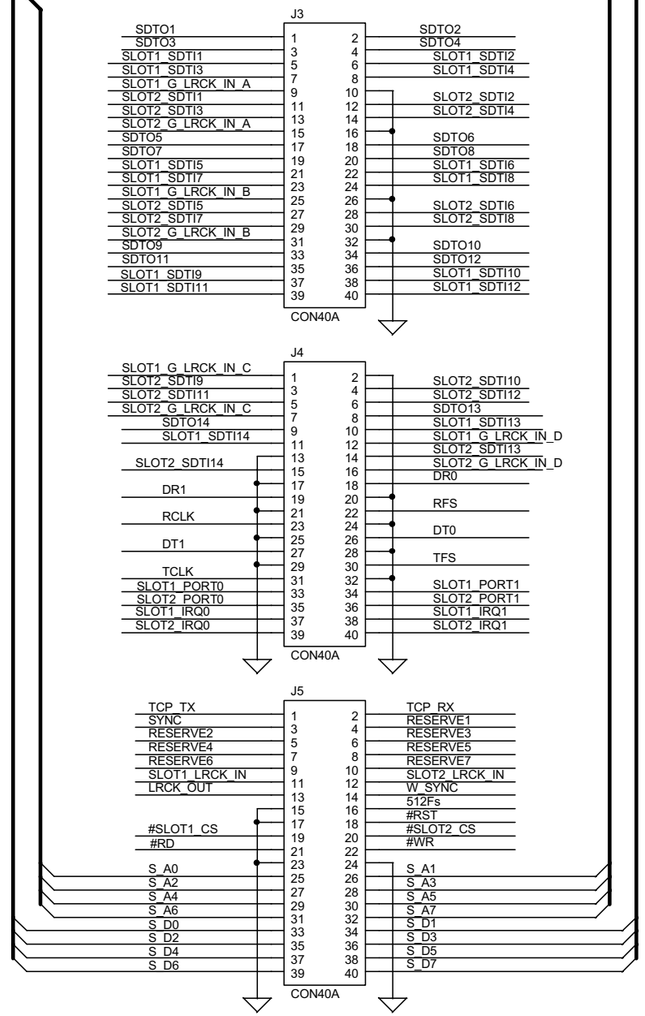
A B C D E

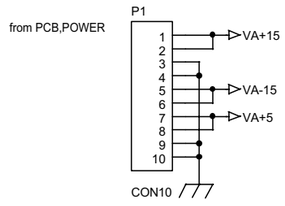
## SLOT2

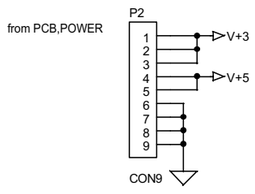


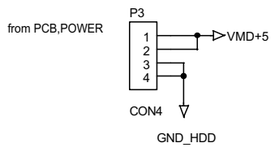

## SLOT1



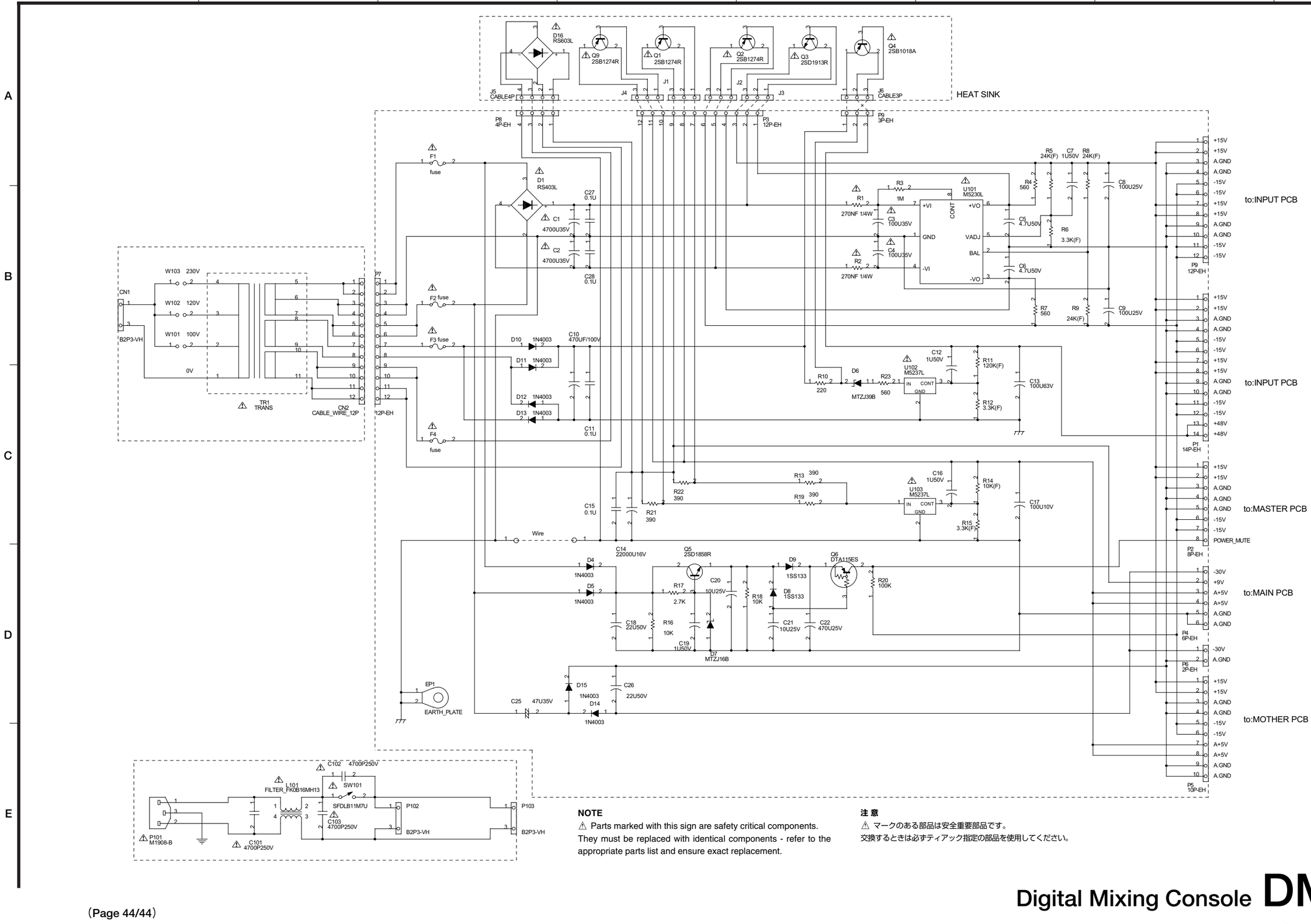






Digital Mixing Console DM-24
1 st Issue; September 2001

# SCHEMATIC DIAGRAM DM-24 POWER SUPPLY SECTION




**NOTE**

⚠ Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.

**注 意**

⚠ マークのある部品は安全重要部品です。
交換するときは必ずティアック指定の部品を使用してください。



Digital Mixing Console DM-24
1 st Issue; September 2001

TEAC **TECHNICAL INFORMATION**

## TASCAM DA-24, Change of Trim VR

No. **0325R**
DATE 27th January 2004

*This is the revised edition of Tech-Info No. 0325.*

Line/Mic input trim VR, VR1 to VR16, on Input Jack PCB Assy has been changed as follows on the products of S/N ~~2800001~~ and up.

→ 3900101

| | P/N | Description | Remark |
|---|---|---|---|
| Original | 91720389-00 | VR, 20KZD EVUF2LFL3 24D | "20KZD" is marked on the side. (*) |
| New | 91720420-00 | VR, 20K EVUJDNFL324Y | "20KZY" is marked on the side. (*) |

* If the VR is mounted to Input Jack PCB, "20KZD" or "20KZY" mark cannot be seen as they will hide behind electrolytic capacitors.

This change is to ease Line/Mic input level control at around the maximum position. Resistance taper (attenuation curve) of original VR is steep around the maximum position resulting in that a fine adjustment is not easy. Therefore, new trim with a smooth taper has been designed.

Note: SX-1 has the new trim VR from beginning of the products.

# TECHNICAL INFORMATION

## TASCAM DM-24, Change of Main PCB and TDIF PCB

No. **0209**
DATE 21st June 2002

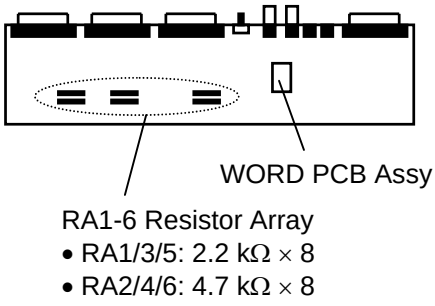
Main PCB Assy and TDIF PCB Assy have been changed on the way of the production.
Purpose of the change is to remove 1) pattern cuts, 2) jumper wires and 3) additional small PCB's.

New PCB Assy's can be identified by the part number printed on the PCB.
Main PCB: 91553160-02 (This is part number for PCB itself, not for PCB Assy)
TDIF PCB: 91553194-02 (This is part number for PCB itself, not for PCB Assy)

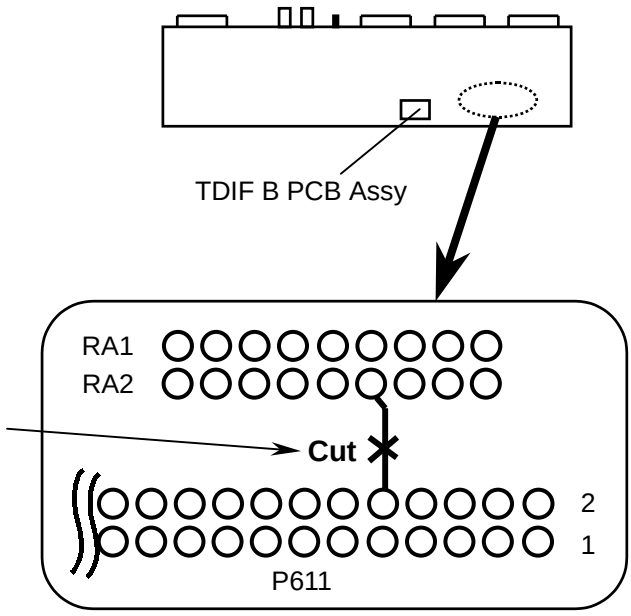
Notice:
1. PCB (-00) does not exist. (-01) is the original.
2. Combination of Main PCB and TDIF PCB should be cared on using them. Some small works are required to combine the different version of them.

Firstly, it is absolutely be needed to know a condition of early productions that have Main PCB (-01) and TDIF PCB (-01). In this case, there are key items on the TDIF PCB as shown below:
- WORD PCB
- TDIF B PCB
- Resistor Array, RA1-6
- One pattern cut

**TDIF PCB (-01) Top Side**




**TDIF PCB (-01) Bottom Side**



## About the Production of DM-24

On the way of the production, notable changes are:
- WORD PCB Assy has been implemented to TDIF PCB (-02).
- TDIF B PCB Assy has been implemented to Main PCB (-02).

Due to above, there are 4 types of combination produced in the factory until all (-01) PCB will be utilized. In the future, of course, production will be made with (-02) PCB only.

| Case 1 Main PCB (-01) + TDIF PCB (-01) | Case 3 Main PCB (-02) + TDIF PCB (-01) |
|---|---|
| WORD PCB Assy is mounted.<br>TDIF B PCB Assy is mounted.<br>Pattern cut is made.<br>RA1-6 are mounted. | WORD PCB Assy is mounted.<br>TDIF B PCB Assy is NOT mounted.<br>Pattern cut is NOT made (connected).<br>RA1-6 are NOT mounted. |
| **Case 2 Main PCB (-01) + TDIF PCB (-02)** | **Case 4. Main PCB (-02) + TDIF PCB (-02)** |
| WORD PCB Assy is NOT mounted.<br>TDIF B PCB Assy is mounted.<br>Pattern cut is made.<br>RA1-6 are mounted. | WORD PCB Assy is NOT mounted.<br>TDIF B PCB Assy is NOT mounted.<br>RA1-6 are NOT mounted.<br>Pattern cut is NOT made. |

## Actual Servicing

Only (-02) PCB is available as a spare part. Then actual servicing will become as follows:

Servicing the unit that has Main PCB (-01) + TDIF PCB (-01)

1. Replacing only Main PCB with (-02).
   Remove TDIF B PCB on the TDIF PCB and restore a pattern cut.
   Remove RA1-6 on the TDIF PCB.
2. Replacing only TDIF PCB with (-02)
   Move the TDIF B PCB from TDIF PCB (-01) to (-02).
   Apply pattern cut.
   Move RA1-6 from TDIF PCB (-01) to (-02).
3. Replacing Main PCB and TDIF PCB with (-02).
   No notices. Just replace them at the same time.

Servicing the unit that has Main PCB (-01) + TDIF PCB (-02)

1. Replacing Main PCB with (-02).
   Remove TDIF B PCB on the TDIF PCB and restore a pattern cut.
   Remove RA1-6 on the TDIF PCB.

Servicing the unit that has Main PCB (-02) + TDIF PCB (-01)

1. Replacing TDIF PCB with (-02)
   No notices. Just replace it.

**Related Parts List**

| Ref No. | Descriptions | Part Number |
|---|---|---|
| 2-29 | MAIN PCB Assy | 91453160-00 |
| 2-13 | Gather PCB Assy, Transport | 91453190-20 [J, US/C]<br>91453190-50 [K, A, E, UK] |
| - | RA1, 3, 5 (2.2 kΩ x 8) | 91113040-00, |
| - | RA2, 4, 6 (4.7 kΩ x 8) | 91113050-00 |
| - | TDIF B PCB Assy | 91453741-00 |

Note:
1. There is no part number for TDIF PCB Assy independently.
   Since it is included in **"Gather PCB Assy, Transport"** listed above.
2. There is no change on the part number for MAIN PCB Assy and Gather PCB Assy, Transport.

**Other changes applied to the Main PCB (-02)**

1. U166 and C429 have been added to correct following:
When changing Fs from normal mode to Hi-Fs mode, click noise will appear from the DAC of AUX SEND3 and 4.

2. There is a possibility that the unit connected to the DM-24 cannot receive the TDIF output of the DM-24.
U55, 56, 57 have been changed from HD74LVC240A to HD74LV240A (P/No. 91670651-30).

TEAC **TECHNICAL INFORMATION**

## TASCAM DM-24, Change of Various PCB's

No. **0210**
DATE 21st June 2002

Following changes have been made on each PCB's.

**MIDI PCB** S/No. 1Y00001 and higher
For the cost down purpose, a jumper wire at U505 has been removed and foil pattern has been connected.

**Digital I/O PCB** S/No. 1Z00001 and higher
For the cost down purpose, U903-U922 (20 pcs of EMI filter) have been removed.

**C. ROOM PCB** S/No. 2200211 and higher
Output level of the Control Room Output has been decreased by 10 dB.
After this change, maximum output level becomes +21 dBu ± 1 dB.

| | | | | |
|---|---|---|---|---|
| C116, C216 | 33 pF | → | removed | |
| C122, C222 | 33 pF | → | 100 pF | (P/No. 91157871-21) |
| R127, R227 | 15 kΩ | → | removed | |
| R133, R233 | 30 kΩ | → | 8.2 kΩ | (P/No. 91130940-50) |
| R135, R235 | 30 kΩ | → | 10 kΩ | (P/No. 91130962-50) |

**STUDIO PCB** S/No. 2400492 and higher
1. Gain of talkback mic has been increased from 40 dB to 60 dB.
   R504 2.2 kΩ → 180 Ω (P/No. 91130540-50)

2. Signal to Noise Ratio of the talkback mic has been improved.
   W124 Jumper → 180 Ω (P/No. 91130540-50)
   C509 100 μF → 470 μF/6.3V (P/No. 91172410-20)

# TECHNICAL INFORMATION

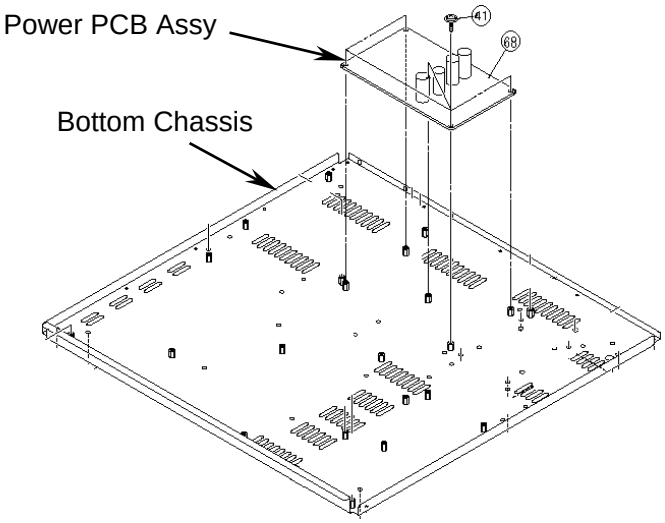
## TASCAM DM-24, Removing C11

No. **0213**
DATE 13th September 2002

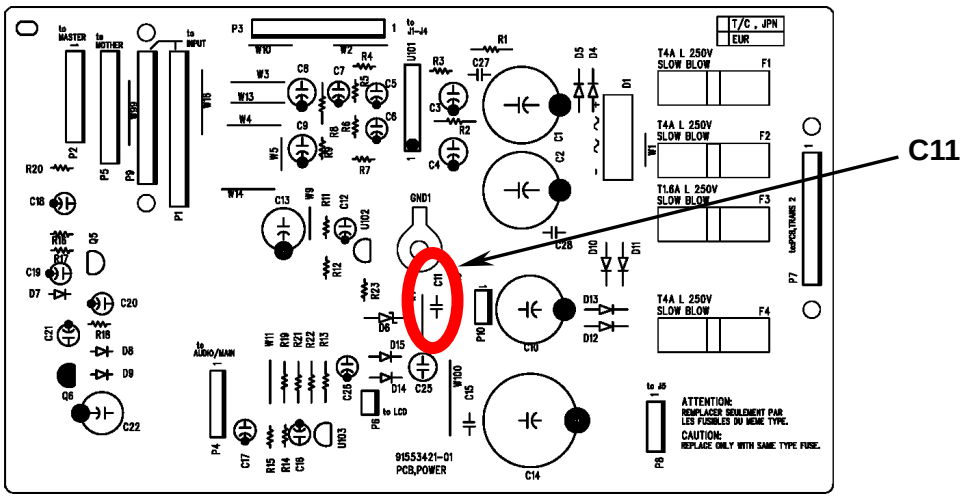
There is a little possibility that C11 on the Power PCB Assy will become short state.
Therefore C11 has been removed on the following products:

- S/No. 2400251 through 2400265 reworked. They have “2F” marked on the carton.
- All products with S/No. 2400266 and higher. They have no “2F” mark.

If there is an opportunity to service the DM-24, remove C11.




**Power PCB Assy**



# TEAC TECHNICAL INFORMATION

## TASCAM SX-1/DM-24, Change of Capacitors on SW PSU

No. **0304**
DATE 27th February 2003

**Symptom:**
There is a little possibility that unit won't work. In the case of DM-24, following message will be displayed on LCD upon turning on the unit, then unit will freeze.
a) "Power Supply Voltage (+5V) is too Low for stable operation. Please Restart DM-24."
b) "Starting Fader Calibration··· ## Don't touch Faders ##"

**Cause:**
Premature lifetime of some electrolytic capacitors, China made. This is especially experienced on C45, C47 and C51 on the SW PSU.

* If the lifetime has expired, swollen explosion-proof valve at top of the capacitor may be present.
* As of date, no SX-1 problem has been reported since there is a cooling fan for the SW PSU.

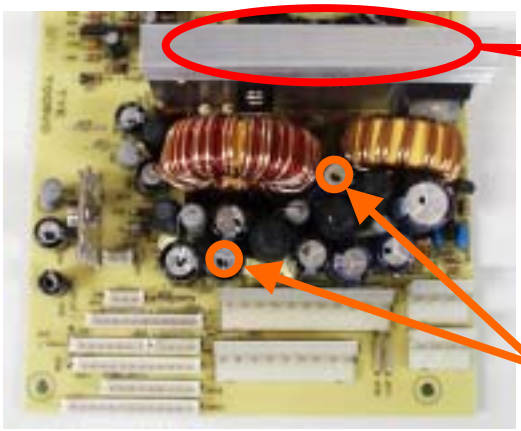
**Solution:**
Change totally 7 electrolytic capacitors to longer lifetime type or higher heat-proof made by Nippon Chemi-Con. Practical work is shown in page 2 of 2.

* This change has been made on the products as follows:
SX-1: S/N 190011 and up
DM-24: S/N 2Z00001 and up
SX-1/DM-24: TCJ stock has been reworked and "3A" mark is stamped on their carton box.

* P/N of the SW PSU has been changed as follows:

| | Former | New | Description |
|---|---|---|---|
| For 100V to 120V | 91251463-00 | **91251463-01** | SW PER, UPS220-1061-L T/C |
| For 220V to 240V | 91251464-00 | **91251464-01** | SW PER, UPS220-1061-H EUR |

Note:
There is no print of the P/N etc anywhere on the former SW PSU but the new PSU can be identified by "01" or "02" mark stamped on the top of a heat sink as following picture. "01" means reworked SW PSU of TTC stock. "02" means the new SW PSU supplied from original manufacture.



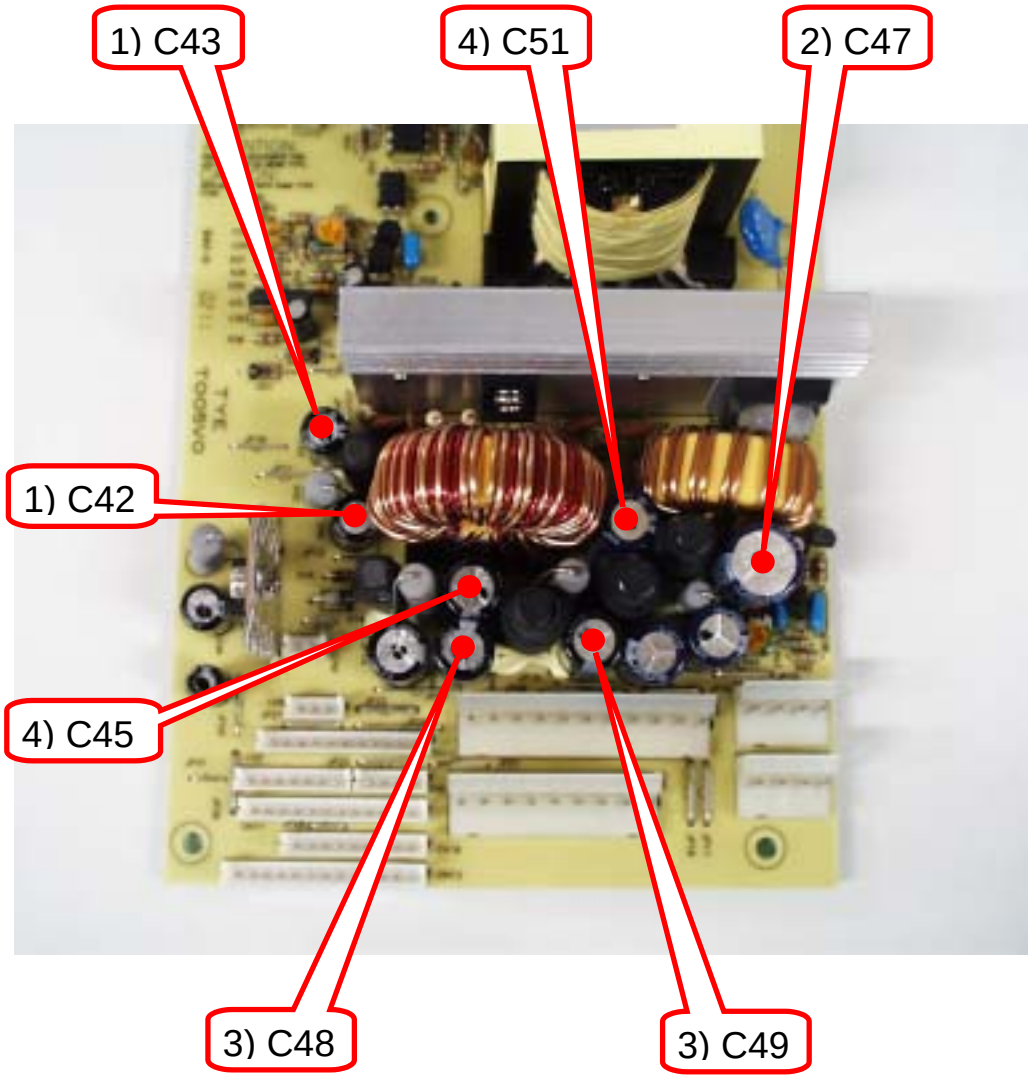

* Early reworked SW PSU has no "01" or "02" mark. A sign of rework can be identified in case the C45 and C51 have an orange color sleeve fitted.

Change Of The 7 Electrolytic Capacitors

* Required Parts
2 pcs P/N 91159580-00, 470uF/16V/105°C (KY16VB470MH15)
2 pcs P/N 91159590-00, 1000uF/10V/125°C (GXE10VB1000M)
2 pcs P/N 91159600-00, 1000uF/16V/105°C (KY16VB1000MJ20)
1 pcs P/N 91159610-00, 2200uF/10V/105°C (KY10VB2200MK20)

* Procedure
1) Change C42/C43 (470uF) to P/N 91159580-00 (KY16VB470MH15).
2) Change C47 (2200uF) to P/N 91159610-00 (KY10VB2200MK20).
3) Change C48/C49 (1000uF) to P/N 91159600-00 (KY16VB1000MJ20).
4) Change C45/C51 (1000uF) to P/N 91159590-00 (GXE10VB1000M). --- (Orange Color Sleeve)

Note:
The capacitors to be changed have been fixed by bond firmly. To ease the change, release the capacitors from bond by inserting small flat head screw driver between them. No need to apply bond again upon change. Mount the capacitors so that undersurface of the capacitors touches to the PCB surface firmly.



# TECHNICAL INFORMATION

## TASCAM SX-1/DM-24, Change of Capacitors on SW PSU

No. **0304R**
DATE 04th Mar 2003

*This is the revised edition of Tech Info No. 0304 to correct a wrong pointing up an electrolytic capacitor by arrow mark (lower one) in Note of page 1/2.*

**Symptom:**
There is a little possibility that unit won't work. In the case of DM-24, following message will be displayed on LCD upon turning on the unit, then unit will freeze.
a) "Power Supply Voltage (+5V) is too Low for stable operation. Please Restart DM-24."
b) "Starting Fader Calibration··· ## Don't touch Faders ##"

**Cause:**
Premature lifetime of some electrolytic capacitors, China made. This is especially experienced on C45, C47 and C51 on the SW PSU.

* If the lifetime has expired, swollen explosion-proof valve at top of the capacitor may be present.
* As of date, no SX-1 problem has been reported since there is a cooling fan for the SW PSU.

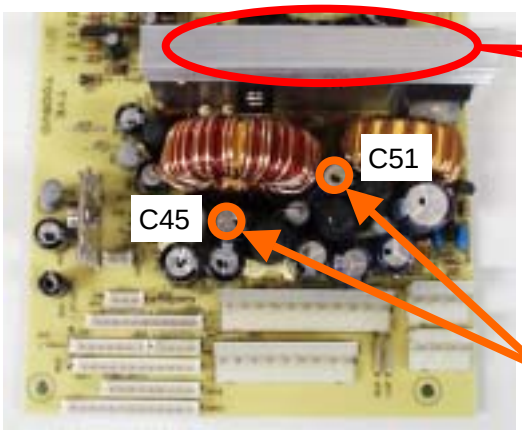
**Solution:**
Change totally 7 electrolytic capacitors to longer lifetime type or higher heat-proof made by Nippon Chemi-Con. Practical work is shown in page 2 of 2.

* This change has been made on the products as follows:
SX-1: S/N 190011 and up
DM-24: S/N 2Z00001 and up
SX-1/DM-24: TCJ stock has been reworked and "3A" mark is stamped on their carton box.

* P/N of the SW PSU has been changed as follows:

| | Former | New | Description |
|---|---|---|---|
| For 100V to 120V | 91251463-00 | **91251463-01** | SW PER, UPS220-1061-L T/C |
| For 220V to 240V | 91251464-00 | **91251464-01** | SW PER, UPS220-1061-H EUR |

Note:
There is no print of the P/N etc anywhere on the former SW PSU but the new PSU can be identified by "01" or "02" mark stamped on the top of a heat sink as following picture. "01" means reworked SW PSU of TTC stock. "02" means the new SW PSU supplied from original manufacture.




The New SW PSU identification "01" or "02" is stamped here.

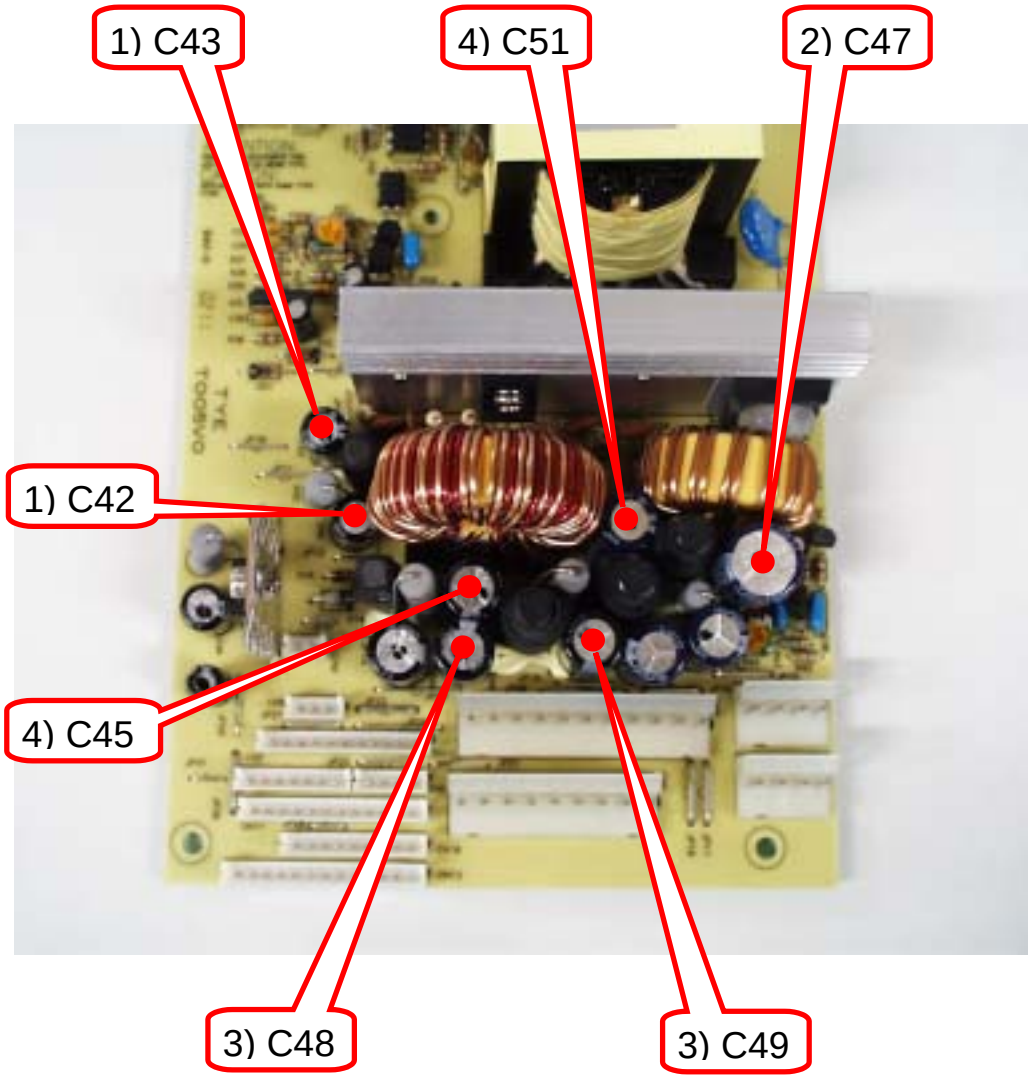
* Early reworked SW PSU has no "01" or "02" mark. A sign of rework can be identified in case the C45 and C51 have an orange color sleeve fitted.

Change Of The 7 Electrolytic Capacitors

* Required Parts
2 pcs P/N 91159580-00, 470uF/16V/105°C (KY16VB470MH15)
2 pcs P/N 91159590-00, 1000uF/10V/125°C (GXE10VB1000M)
2 pcs P/N 91159600-00, 1000uF/16V/105°C (KY16VB1000MJ20)
1 pcs P/N 91159610-00, 2200uF/10V/105°C (KY10VB2200MK20)

* Procedure
1) Change C42/C43 (470uF) to P/N 91159580-00 (KY16VB470MH15).
2) Change C47 (2200uF) to P/N 91159610-00 (KY10VB2200MK20).
3) Change C48/C49 (1000uF) to P/N 91159600-00 (KY16VB1000MJ20).
4) Change C45/C51 (1000uF) to P/N 91159590-00 (GXE10VB1000M). --- (Orange Color Sleeve)

Note:
The capacitors to be changed have been fixed by bond firmly. To ease the change, release the capacitors from bond by inserting small flat head screw driver between them. No need to apply bond again upon change. Mount the capacitors so that undersurface of the capacitors touches to the PCB surface firmly.



TEAC **TECHNICAL INFORMATION**

## TASCAM DA-24, Change of Trim VR

No. **0325**
DATE 25th June 2003

Line/Mic input trim VR, VR1 to VR16, on Input Jack PCB Assy has been changed as follows on the products of S/N 2800001 and up.

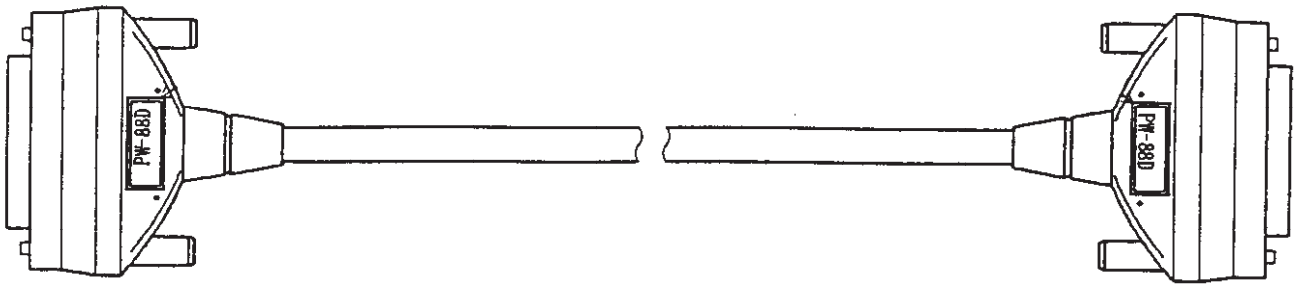
| | P/N | Description | Remark |
|---|---|---|---|
| Original | 91720389-00 | VR, 20KZD EVUF2LFL3 24D | "20KZD" is marked on the side. (*) |
| New | 91720420-00 | VR, 20K EVUJDNFL324Y | "20KZY" is marked on the side. (*) |

* If the VR is mounted to Input Jack PCB, "20KZD" or "20KZY" mark cannot be seen as they will hide behind electrolytic capacitors.

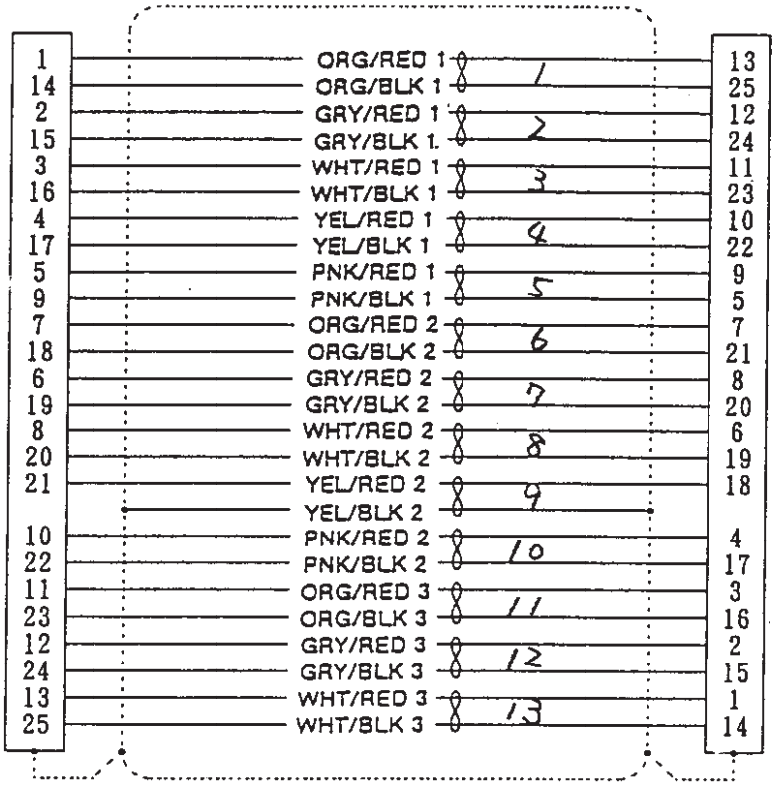
This change is to ease Line/Mic input level control at around the maximum position. Resistance taper (attenuation curve) of original VR is steep around the maximum position resulting in that a fine adjustment is not easy. Therefore, new trim with a smooth taper has been designed.

Note: SX-1 has the new trim VR from beginning of the products.

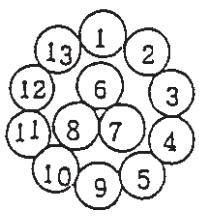
# THE CABLES FOR TDIF




Male Male

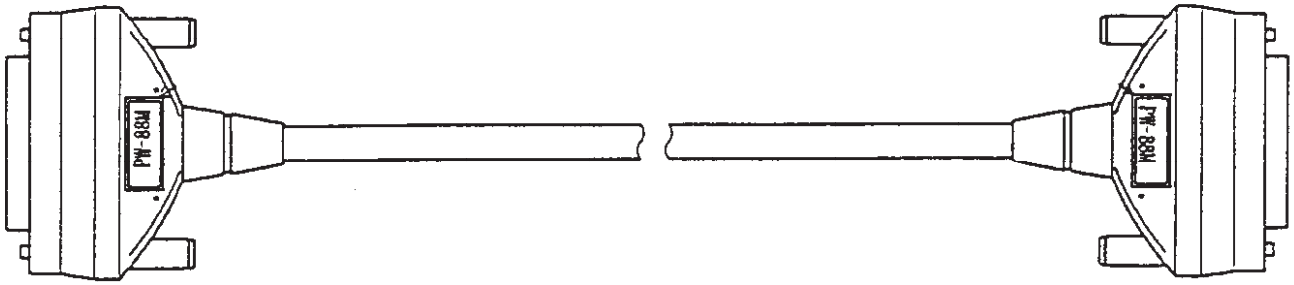



means Twisted wire

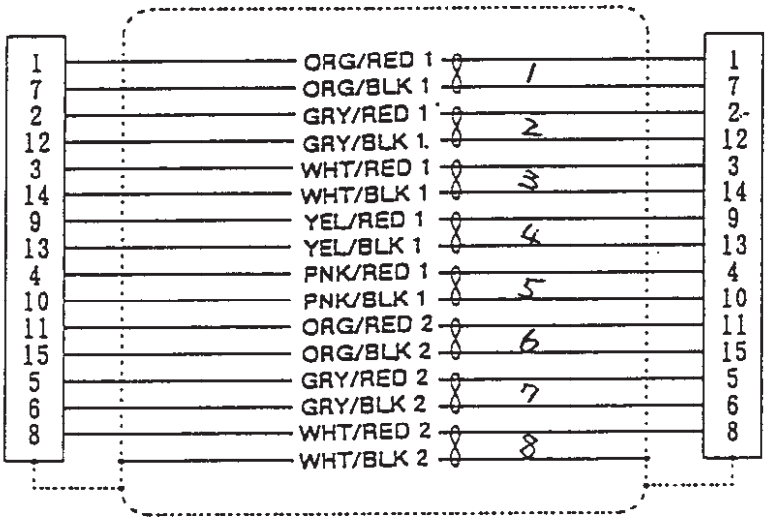



| | | |
|---|---|---|
| 2 pcs. | 1315 2908- | Connector Plug, 25 pin D-Sub (Male) |
| 2 pcs. | 5336 3581-00 | Case Assy, 25 pin D-Sub |

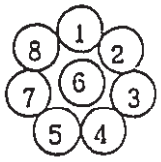
# THE CABLES FOR METER



Female Male

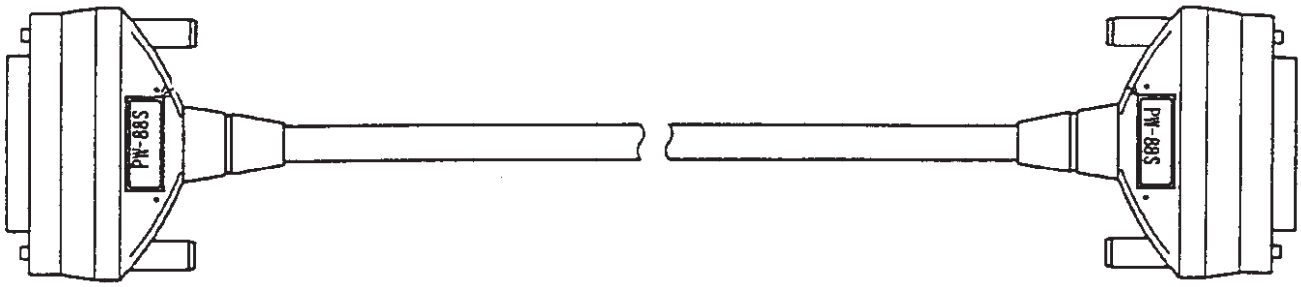



means Twisted wire

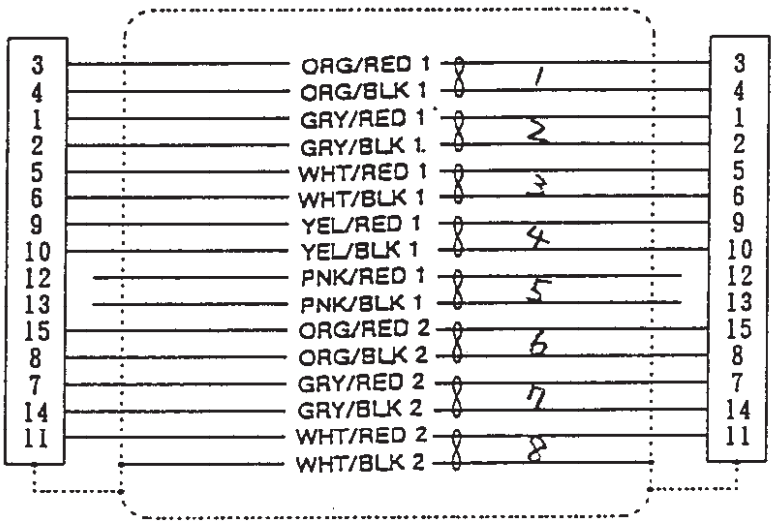



| | | |
|---|---|---|
| 1 pce. | 5336 3570-00 | Connector Plug, 15 pin D-Sub (Male) |
| 1 pce. | 1315 2907- | Connector Socket, 15 pin D-Sub (Female) |
| 2 pcs. | 5336 3580-00 | Case Assy, 15 pin D-Sub |

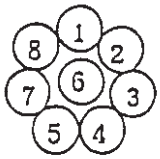
# THE CABLES FOR SYNC




Male Male

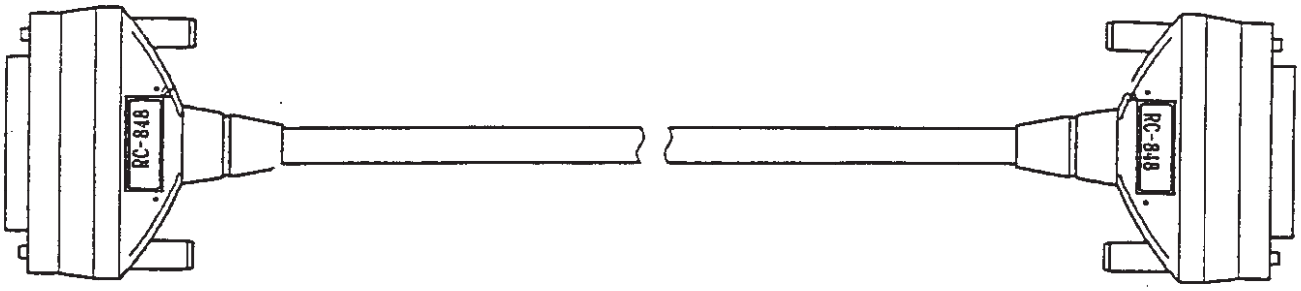



means Twisted wire



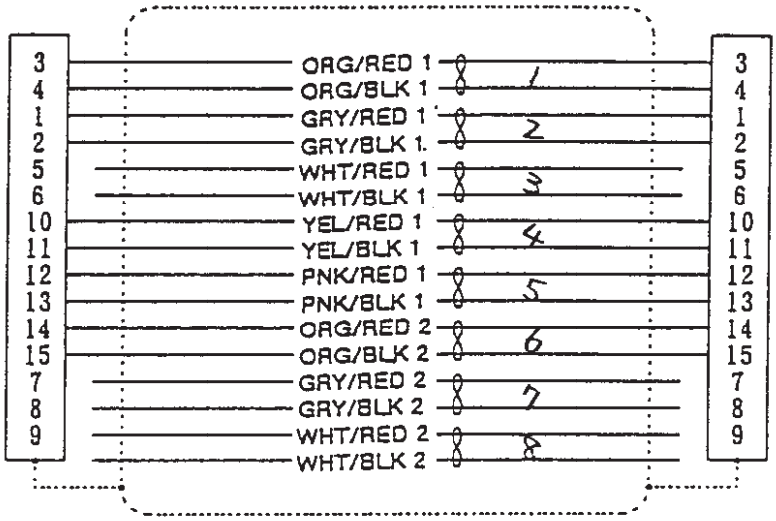

| | | |
|---|---|---|
| 2 pcs. | 5336 3570-00 | Connector Plug, 15 pin D-Sub (Male) |
| 2 pcs. | 5336 3580-00 | Case Assy, 15 pin D-Sub |

# THE CABLES FOR REMOTE

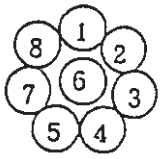



Female

Male




means Twisted wire




| | | |
|---|---|---|
| 1 pce. | 5336 3570-00 | Connector Plug, 15 pin D-Sub (Male) |
| 1 pce. | 1315 2907- | Connector Socket, 15 pin D-Sub (Female) |
| 2 pcs. | 5336 3580-00 | Case Assy, 15 pin D-Sub |

# AK4393

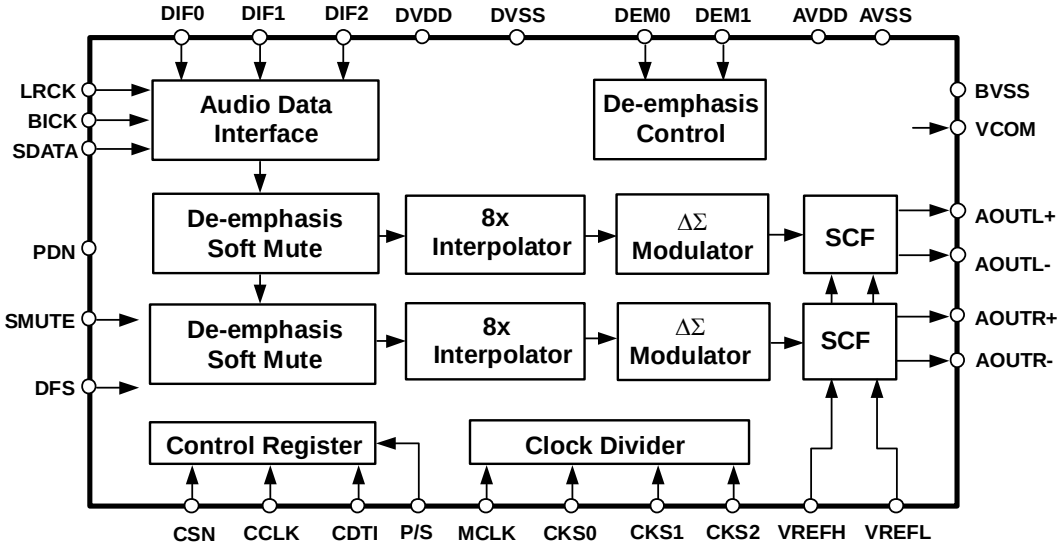
## Advanced Multi-Bit 96kHz 24-Bit ΔΣ DAC

### GENERAL DESCRIPTION

The AK4393 is a high performance stereo DAC for the 96kHz sampling mode of DAT, DVD including a 24bit digital filter. The AK4393 introduces the advanced multi-bit system for ΔΣ modulator. This new architecture achieves the wider dynamic range, while keeping much the same superior distortion characteristics as conventional Single-Bit way. In the AK4393, the analog outputs are filtered in the analog domain by switched-capacitor filter (SCF) with high tolerance to clock jitter. The analog outputs are full differential output, so the device is suitable for hi-end applications. The operating voltages support analog 5V and digital 3.3V, so it is easy to I/F with 3.3V logic IC.

### FEATURES

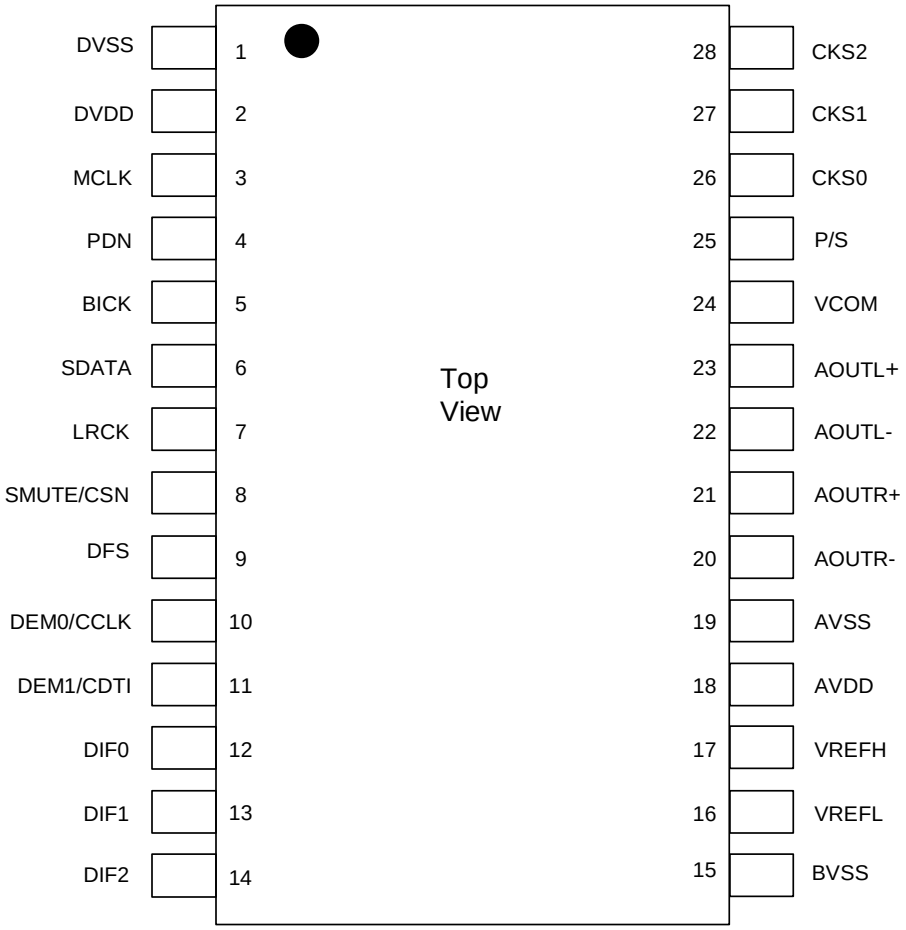
- **128x Oversampling**
- **Sampling Rate up to 108kHz**
- **24Bit 8x Digital Filter**
  **Ripple: ±0.005dB, Attenuation: 75dB**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **Digital de-emphasis for 32, 44.1, 48 & 96kHz sampling**
- **Soft Mute**
- **THD+N: -100dB**
- **DR, S/N: 120dB**
- **I/F format : MSB justified, 16/20/24bit LSB justified, $I^2S$**
- **Master Clock: Normal Speed: 256fs, 384fs, 512fs or 768fs**
  **Double Speed: 128fs, 192fs, 256fs or 384fs**
- **Power Supply: 4.75 to 5.25V (Analog), 3 to 5.25V (Digital)**
- **Small Package: 28pin VSOP**



## ■ Ordering Guide

| | | |
|---|---|---|
| AK4393VF | -40 ~ +85 °C | 28pin VSOP (0.65mm pitch) |
| AKD4393 | Evaluation Board | |

## ■ Pin Layout



## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | DVSS | - | Digital Ground Pin |
| 2 | DVDD | - | Digital Power Supply Pin, 3.3V or 5.0V |
| 3 | MCLK | I | Master Clock Input Pin |
| 4 | PDN | I | Power-Down Mode Pin<br>When at "L", the AK4393 is in power-down mode and is held in reset.<br>The AK4393 should always be reset upon power-up. |
| 5 | BICK | I | Audio Serial Data Clock Pin<br>The clock of 64fs or more than is recommended to be input on this pin. |
| 6 | SDATA | I | Audio Serial Data Input Pin<br>2's complement MSB-first data is input on this pin. |
| 7 | LRCK | I | L/R Clock Pin |
| 8 | SMUTE | I | Soft Mute Pin in parallel mode<br>When this pin goes "H", soft mute cycle is initiated.<br>When returning "L", the output mute releases. |
| | CSN | I | Chip Select Pin in serial mode |
| 9 | DFS | I | Double Speed Sampling Mode Pin (Internal pull-down pin)<br>"L": Normal Speed , "H": Double Speed |
| 10 | DEM0 | I | De-emphasis Enable Pin in parallel mode |
| | CCLK | I | Control Data Clock Pin in serial mode |
| 11 | DEM1 | I | De-emphasis Enable Pin in parallel mode |
| | CDTI | I | Control Data Input Pin in serial mode |
| 12 | DIF0 | I | Digital Input Format Pin |
| 13 | DIF1 | I | Digital Input Format Pin |
| 14 | DIF2 | I | Digital Input Format Pin |
| 15 | BVSS | - | Substrate Ground Pin, 0V |
| 16 | VREFL | I | Low Level Voltage Reference Input Pin |
| 17 | VREFH | I | High Level Voltage Reference Input Pin |
| 18 | AVDD | - | Analog Power Supply Pin, 5.0V |
| 19 | AVSS | - | Analog Ground Pin, 0V |
| 20 | AOUTR- | O | Rch Negative analog output Pin |
| 21 | AOUTR+ | O | Rch Positive analog output Pin |
| 22 | AOUTL- | O | Lch Negative analog output Pin |
| 23 | AOUTL+ | O | Lch Positive analog output Pin |
| 24 | VCOM | O | Common Voltage Output Pin, 2.6V |
| 25 | P/S | I | Parallel/Serial Select Pin (Internal pull-up pin)<br>"L": Serial control mode, "H": Parallel control mode |
| 26 | CKS0 | I | Master Clock Select Pin |
| 27 | CKS1 | I | Master Clock Select Pin |
| 28 | CKS2 | I | Master Clock Select Pin |

Note: All input pins except internal pull-up/down pins should not be left floating.

## ABSOLUTE MAXIMUM RATINGS

(AVSS, BVSS, DVSS = 0V; Note 1)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | -0.3 | 6.0 | V |
| | Digital | DVDD | -0.3 | 6.0 | V |
| | \| BVSS-DVSS \| (Note 2) | Δ GND | - | 0.3 | V |
| Input Current , Any pin Except Supplies | | IIN | - | ±10 | mA |
| Input Voltage | | VIND | -0.3 | DVDD+0.3 | V |
| Ambient Operating Temperature | | Ta | -40 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Notes: 1. All voltages with respect to ground.
2. AVSS, BVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(AVSS, BVSS, DVSS=0V; Note 1)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | 4.75 | 5.0 | 5.25 | V |
| (Note 3) | Digital | DVDD | 3.0 | 3.3 | 5.25 | V |
| Voltage Reference | "H" voltage reference | VREFH | AVDD-0.5 | - | AVDD | V |
| (Note 4) | "L" voltage reference | VREFL | AVSS | - | - | V |
| | VREFH-VREFL | Δ VREF | 3.0 | - | AVDD | V |

Notes: 3. The power up sequence between AVDD and DVDD is not critical.
4. Analog output voltage scales with the voltage of (VREFH-VREFL).
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = ±2.4Vpp×(VREFH-VREFL)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

## ANALOG CHARACTERISTICS

(Ta = 25°C; AVDD = 5V, DVDD = 3.3V; AVSS, BVSS, DVSS = 0V, VREFH = AVDD, VREFL = AVSS;
fs = 44.1kHz; BICK = 64fs; Signal Frequency = 1kHz; 24bit Input Data; Measurement Bandwidth = 20Hz~20kHz;
$R_L \geq 600\Omega$; External circuit: Figure 11; unless otherwise specified)

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Resolution | | | | | 24 | Bits |
| **Dynamic Characteristics** (Note 5) | | | | | | |
| THD+N | fs=44.1kHz | 0dBFS | | -100 | -90 | dB |
| | BW=20kHz | -60dBFS | | -53 | - | dB |
| | fs=96kHz | 0dBFS | | -97 | -86 | dB |
| | BW=40kHz | -60dBFS | | -51 | - | dB |
| Dynamic Range (-60dBFS with A-weighted) | fs=44.1kHz | (Note 6) | 112 | 117 | | dB |
| | | (Note 7) | - | 120 | | dB |
| | fs=96kHz | | 111 | 116 | | dB |
| | | (Note 7) | - | 118 | | dB |
| S/N (A-weighted | fs=44.1kHz | (Note 8) | 112 | 117 | | dB |
| | | (Note 7) | - | 120 | | dB |
| | fs=96kHz | | 111 | 116 | | dB |
| | | (Note 7) | - | 118 | | dB |
| Interchannel Isolation (1kHz) | | | 100 | 120 | | dB |
| **DC Accuracy** | | | | | | |
| Interchannel Gain Mismatch | | | | 0.15 | 0.3 | dB |
| Gain Drift | | (Note 9) | | 20 | - | ppm/°C |
| Output Voltage | | (Note 10) | ±2.25 | ±2.4 | ±2.55 | Vpp |
| Load Resistance | | (Note 11) | 600 | | | Ω |
| Output Current | | | | | 3.5 | mA |
| **Power Supplies** | | | | | | |
| Power Supply Current | | | | | | |
| Normal Operation (PDN = "H") | | | | | | |
| AVDD | | | | 60 | - | mA |
| DVDD(fs=44.1kHz) | | | | 3 | - | mA |
| DVDD(fs=96kHz) | | | | 5 | - | mA |
| AVDD + DVDD | | | | | 90 | mA |
| Power-Down Mode (PDN = "L") | | | | | | |
| AVDD + DVDD | | (Note 12) | | 10 | 50 | μA |
| Power Supply Rejection | | (Note 13) | | 50 | | dB |

Notes: 5. At 44.1kHz, measured by Audio Precision, System Two. Averaging mode.
At 96kHz, measured by ROHDE & SCHWARZ, UPD. Averaging mode.
Refer to the eva board manual.
6. 101dB at 16bit data and 116dB at 20bit data.
7. By Figure12. External LPF Circuit Example 2.
8. S/N does not depend on input bit length.
9. The voltage on (VREFH-VREFL) is held +5V externally.
10. Full-scale voltage (0dB). Output voltage scales with the voltage of (VREFH-VREFL).
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = ±2.4Vpp×(VREFH-VREFL)/5.
11. For AC-load. 1kΩ for DC-load.
12. In the power-down mode. P/S = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.
13. PSR is applied to AVDD, DVDD with 1kHz, 100mVpp. VREFH pin is held +5V.

## FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; fs = 44.1kHz; Normal Speed Mode; DEM = OFF)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Passband ±0.01dB (Note 14) | | PB | 0 | | 20.0 | kHz |
| -6.0dB | | | - | 22.05 | - | kHz |
| Stopband (Note 14) | | SB | 24.1 | | | kHz |
| Passband Ripple | | PR | | | ± 0.005 | dB |
| Stopband Attenuation | | SA | 75 | | | dB |
| Group Delay (Note 15) | | GD | - | 28 | - | 1/fs |
| **Digital Filter + SCF** | | | | | | |
| Frequency Response 0 ~ 20.0kHz | | | - | ± 0.2 | - | dB |

Note: 14. The passband and stopband frequencies scale with fs.
For example, PB = 0.4535×fs (@±0.01dB), SB = 0.546×fs.

15. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

## FILTER CHARACTERISTICS (fs = 96kHz)

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; fs = 96kHz; Double Speed Mode; DEM = OFF)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Passband ±0.01dB (Note 14) | | PB | 0 | | 43.5 | kHz |
| -6.0dB | | | - | 48.0 | - | kHz |
| Stopband (Note 14) | | SB | 52.5 | | | kHz |
| Passband Ripple | | PR | | | ± 0.005 | dB |
| Stopband Attenuation | | SA | 75 | | | dB |
| Group Delay (Note 15) | | GD | - | 28 | - | 1/fs |
| **Digital Filter + SCF** | | | | | | |
| Frequency Response 0 ~ 40.0kHz | | | - | ± 0.3 | - | dB |

## DC CHARACTERISTICS

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| High-Level Input Voltage | | VIH | 70%DVDD | - | - | V |
| Low-Level Input Voltage | | VIL | - | - | 30%DVDD | V |
| Input Leakage Current | (Note 16) | Iin | - | - | ± 10 | μA |

Note: 16. DFS and P/S pins have internal pull-down or pull-up devices, nominally 100kΩ.

## SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; $C_L$ = 20pF)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Master Clock Timing** (Note 17) | | | | | |
| Normal Speed: 256fs, Double Speed: 128fs | fCLK | 7.7 | | 13.824 | MHz |
| Pulse Width Low | tCLKL | 28 | | | ns |
| Pulse Width High | tCLKH | 28 | | | ns |
| Normal Speed: 384fs, Double Speed: 192fs | fCLK | 11.5 | | 20.736 | MHz |
| Pulse Width Low | tCLKL | 20 | | | ns |
| Pulse Width High | tCLKH | 20 | | | ns |
| Normal Speed: 512fs, Double Speed: 256fs | fCLK | 15.4 | | 27.648 | MHz |
| Normal Speed: 768fs, Double Speed: 384fs | fCLK | 23.0 | | 41.472 | MHz |
| Pulse Width Low | tCLKL | 7 | | | ns |
| Pulse Width High | tCLKH | 7 | | | ns |
| **LRCK Frequency** (Note 18) | | | | | |
| Normal Speed Mode (DFS = "L") | fsn | 30 | 44.1 | 54 | kHz |
| Double Speed Mode (DFS = "H") | fsd | 60 | 88.2 | 108 | kHz |
| Duty Cycle | Duty | 45 | | 55 | % |
| **Serial Interface Timing** | | | | | |
| BICK Period | tBCK | 140 | | | ns |
| BICK Pulse Width Low | tBCKL | 60 | | | ns |
| Pulse Width High | tBCKH | 60 | | | ns |
| BICK "↑" to LRCK Edge (Note 19) | tBLR | 20 | | | ns |
| LRCK Edge to BICK "↑" (Note 19) | tLRB | 20 | | | ns |
| SDATA Hold Time | tSDH | 20 | | | ns |
| SDATA Setup Time | tSDS | 20 | | | ns |
| **Control Interface Timing** | | | | | |
| CCLK Period | tCCK | 200 | | | ns |
| CCLK Pulse Width Low | tCCKL | 80 | | | ns |
| Pulse Width High | tCCKH | 80 | | | ns |
| CDTI Setup Time | tCDS | 50 | | | ns |
| CDTI Hold Time | tCDH | 50 | | | ns |
| CSN High Time | tCSW | 150 | | | ns |
| CSN "↓" to CCLK "↑" | tCSS | 50 | | | ns |
| CCLK "↑" to CSN "↑" | tCSH | 50 | | | ns |
| **Reset Timing** | | | | | |
| PDN Pulse Width (Note 20) | tPW | 150 | | | ns |

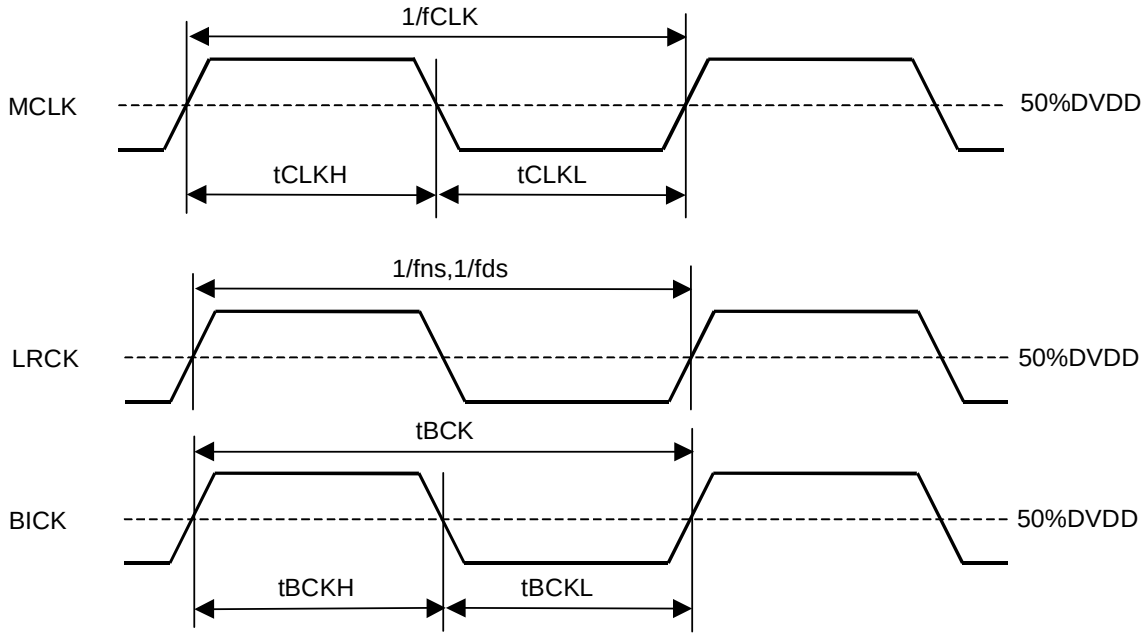
Notes: 17. **For Double Speed mode please see Appendix A for relationship of MCLK and BCLK/LRCK.**

18. When the normal and double speed modes are switched, AK4393 should be reset by PDN pin or RSTN bit.

19. BICK rising edge must not occur at the same time as LRCK edge.

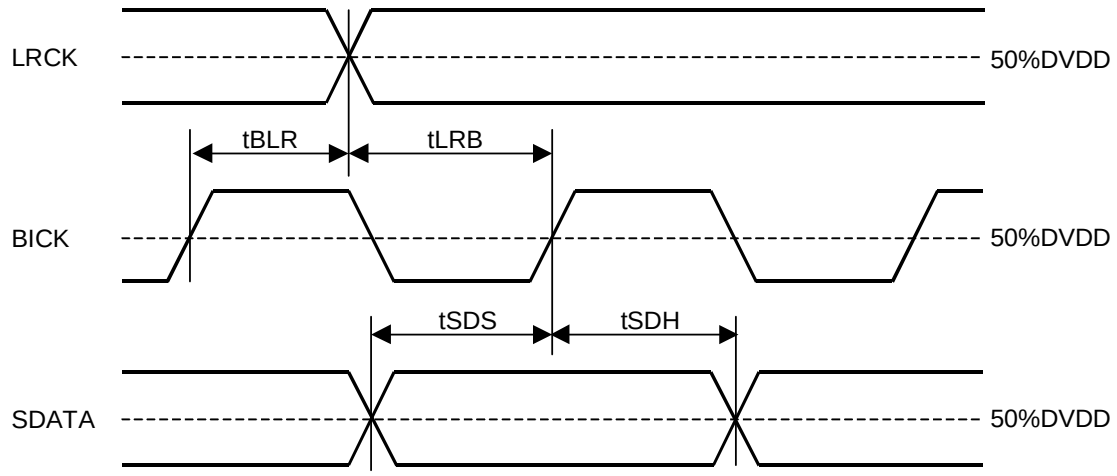
20. The AK4393 can be reset by bringing PDN "L" to "H".
When the states of CKS2-0 or DFS change, the AK4393 should be reset by PDN pin or RSTN bit.

■ **Timing Diagram**

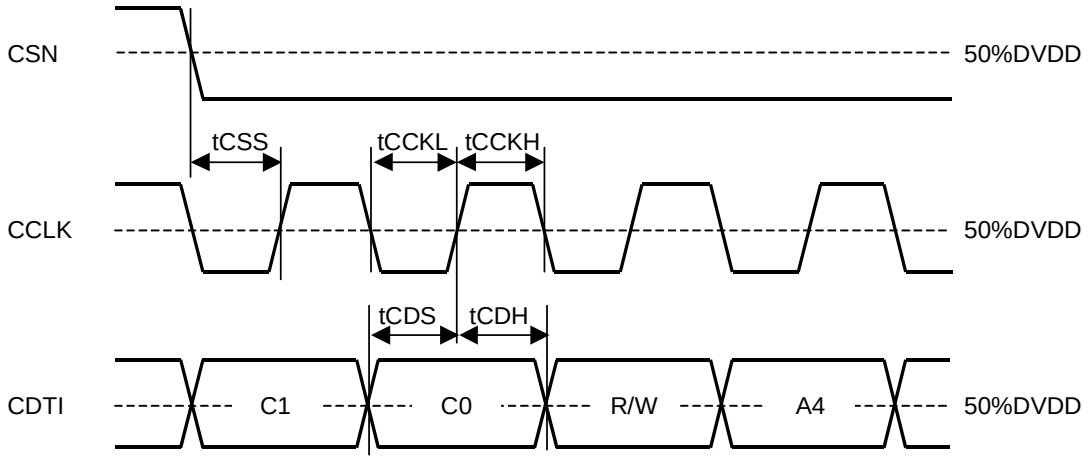



Clock Timing

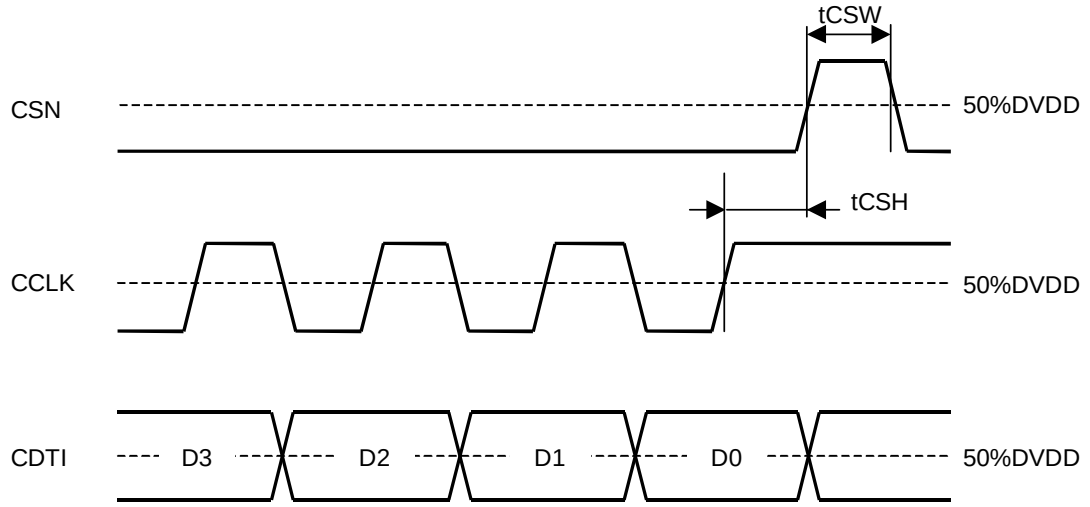
**For Double Speed mode timing please see Appendix A for relationship of MCLK and BCLK/LRCK.**



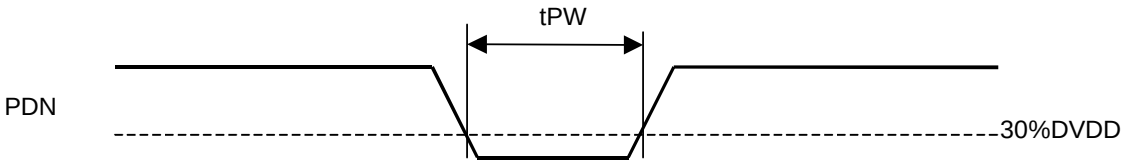

Audio Interface Timing




WRITE Command Input Timing




WRITE Data Input Timing




Power-down Timing

## OPERATION OVERVIEW

### ■ System Clock

The external clocks, which are required to operate the AK4393, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. **However, in Double Speed Mode, the phase relationship between MCLK and LRCK/BICK is limited. (Refer to Appendix A).** The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The sampling speed is set by DFS (Table 1). The sampling rate (LRCK), CKS0/1/2 and DFS determine the frequency of MCLK (Table 2).

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4393 is in normal operation mode (PDN = "H"). If these clocks are not provided, the AK4393 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4393 should be in the power-down mode (PDN = "L") or in the reset mode (RSTN = "0"). After exiting reset at power-up etc., the AK4393 is in power-down mode until MCLK and LRCK are input.

| DFS | Sampling Rate (fs) | | |
|---|---|---|---|
| 0 | Normal Speed Mode | 30kHz~54kHz | Default |
| 1 | Double Speed Mode | 60kHz~108kHz | |

Table 1. Sampling Speed

| Mode | CKS2 | CKS1 | CKS0 | Normal | Double | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 256fs | 128fs | Default |
| 1 | 0 | 0 | 1 | 256fs | 256fs | |
| 2 | 0 | 1 | 0 | 384fs | 192fs | |
| 3 | 0 | 1 | 1 | 384fs | 384fs | |
| 4 | 1 | 0 | 0 | 512fs | 256fs | |
| 5 | 1 | 0 | 1 | 512fs | N/A | |
| 6 | 1 | 1 | 0 | 768fs | 384fs | |
| 7 | 1 | 1 | 1 | 768fs | N/A | |

Table 2. System Clocks

| LRCK | MCLK | | | | BICK |
|---|---|---|---|---|---|
| fs | 256fs | 384fs | 512fs | 768fs | 64fs |
| 32.0kHz | 8.1920MHz | 12.2880MHz | 16.3840MHz | 24.5760MHz | 2.0480MHz |
| 44.1kHz | 11.2896MHz | 16.9344MHz | 22.5792MHz | 33.8688MHz | 2.8224MHz |
| 48.0kHz | 12.2880MHz | 18.4320MHz | 24.5760MHz | 36.8640MHz | 3.0720MHz |

Table 3. System clock example (Normal Speed Mode)

| LRCK | MCLK | | | | BICK |
|---|---|---|---|---|---|
| fs | 128fs | 192fs | 256fs | 384fs | 64fs |
| 88.2kHz | 11.2896MHz | 16.9344MHz | 22.5792MHz | 33.8688MHz | 5.6448MHz |
| 96.0kHz | 12.2880MHz | 18.4320MHz | 24.5760MHz | 36.8640MHz | 6.1440MHz |

Table 4. System clock example (Double Speed Mode)

## ■ Audio Serial Interface Format

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Five data formats are supported and selected by the DIF0-2 as shown in Table 5. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

| Mode | DIF2 | DIF1 | DIF0 | Mode | BICK | Figure |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0: 16bit LSB Justified | ≥32fs | Figure 1 |
| 1 | 0 | 0 | 1 | 1: 20bit LSB Justified | ≥40fs | Figure 2 |
| 2 | 0 | 1 | 0 | 2: 24bit MSB Justified | ≥48fs | Figure 3 |
| 3 | 0 | 1 | 1 | 3: $I^2S$ Compatible | ≥48fs | Figure 4 |
| 4 | 1 | 0 | 0 | 4: 24bit LSB Justified | ≥48fs | Figure 2 |

Table 5. Audio Data Formats

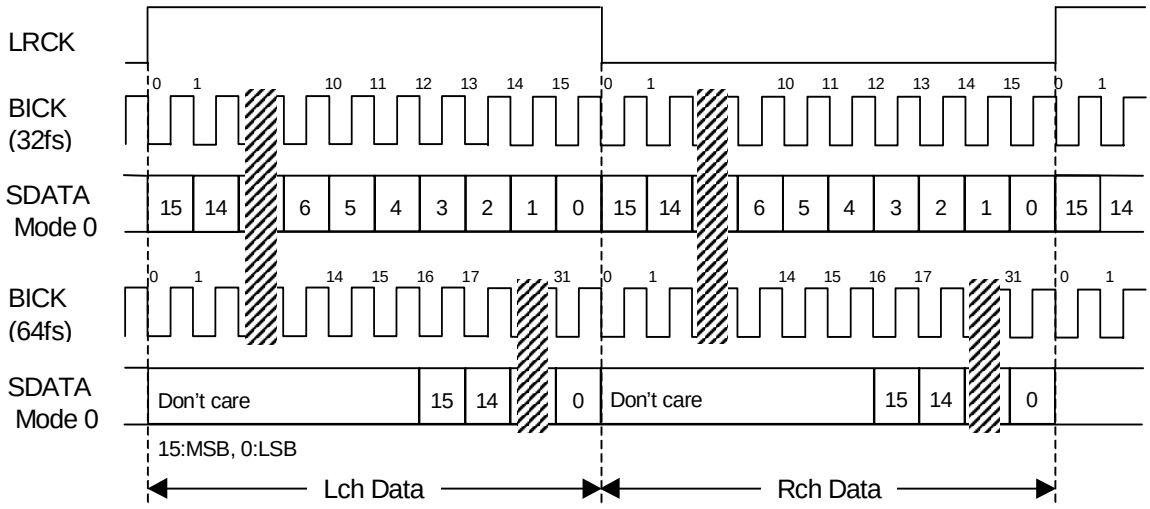



Figure 1. Mode 0 Timing

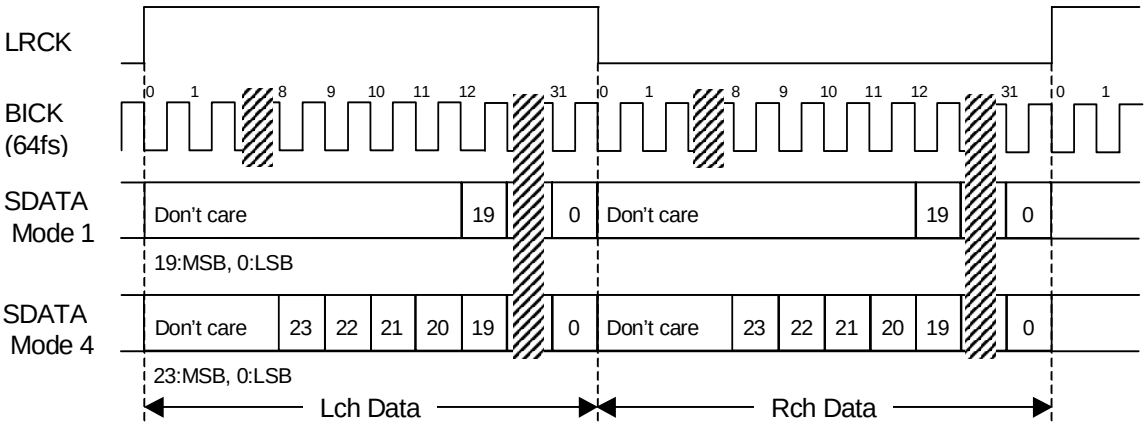



Figure 2. Mode 1,4 Timing

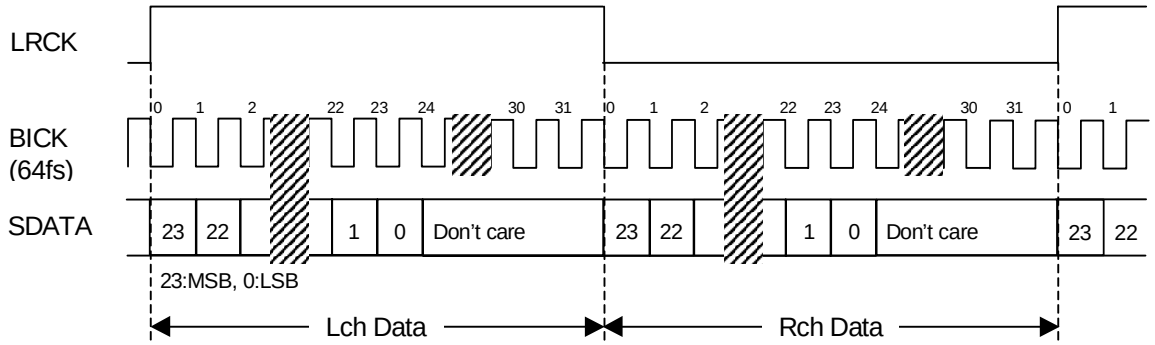



Figure 3. Mode 2 Timing

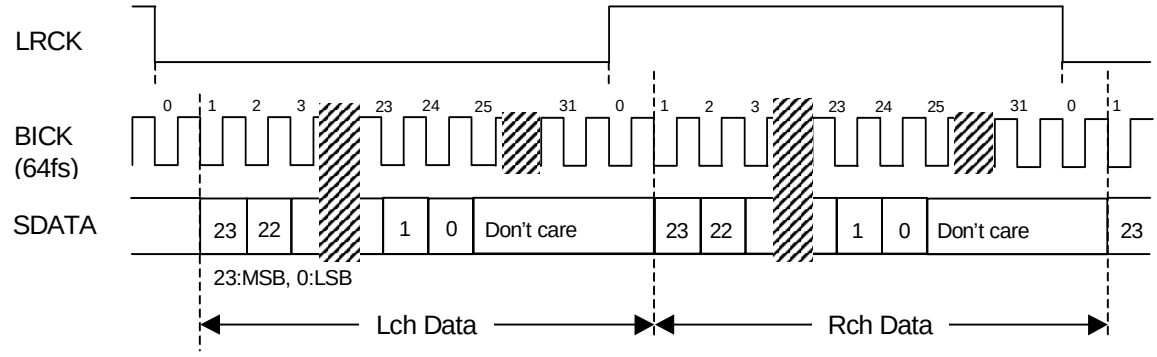



Figure 4. Mode 3 Timing

## ■ De-emphasis filter

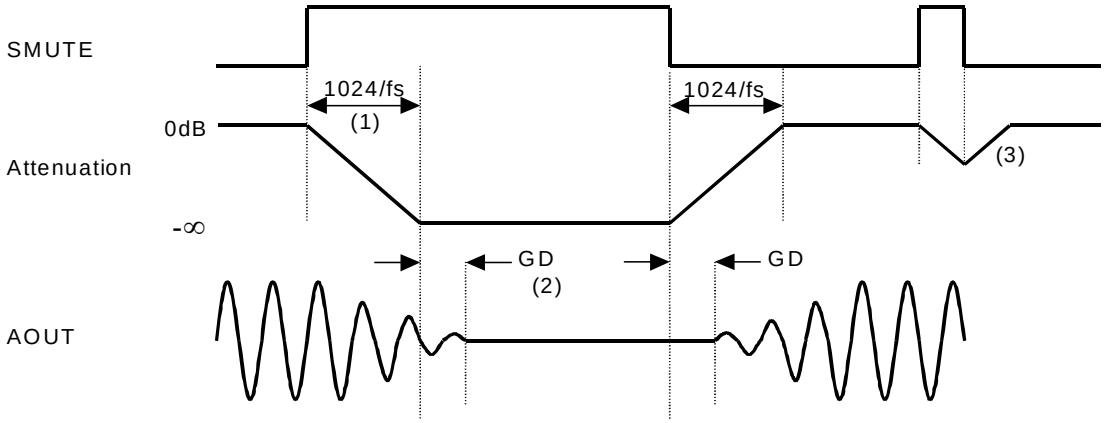
A digital de-emphasis filter is available for 32, 44.1, 48 or 96kHz sampling rates (tc = 50/15μs) and is enabled or disabled with the DEM0, DEM1 and DFS input pins.

| DEM1 | DEM0 | DFS | Mode | |
|---|---|---|---|---|
| 0 | 0 | 0 | 44.1kHz | Default |
| 0 | 1 | 0 | OFF | |
| 1 | 0 | 0 | 48kHz | |
| 1 | 1 | 0 | 32kHz | |
| 0 | 0 | 1 | OFF | |
| 0 | 1 | 1 | OFF | |
| 1 | 0 | 1 | 96kHz | |
| 1 | 1 | 1 | OFF | |

Table 6. De-emphasis filter control

## ■ Soft mute operation

Soft mute operation is performed at digital domain. When SMUTE goes to "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.




Notes:

(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

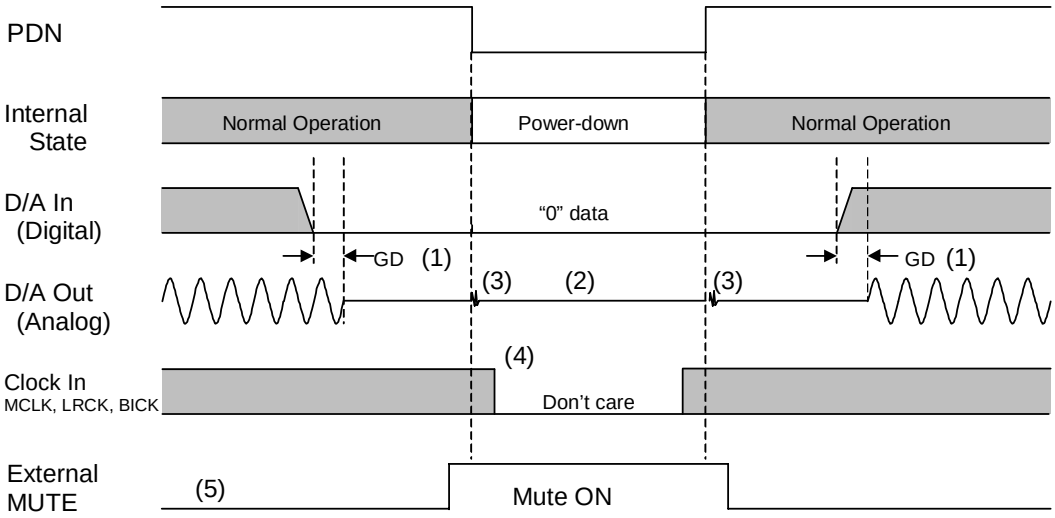
Figure 5. Soft mute operation

## ■ System Reset

The AK4393 should be reset once by bringing PDN = "L" upon power-up. The AK4393 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4393 is in the power-down mode until MCLK and LRCK are input.

## ■ Power-Down

The AK4393 is placed in the power-down mode by bringing PDN pin "L" and the anlog outputs are floating (Hi-Z). Figure 6 shows an example of the system timing at the power-down and power-up.




Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = "L").
(5) Please mute the analog output externally if the click noise (3) influences system application. The timing example is shown in this figure.

Figure 6. Power-down/up sequence example

## ■ Click Noise from analog output

Click noise occurs from analog output in the following cases.

1) When switching de-emphasis mode by DEM0, DEM1 and DFS pins,
2) When switching serial data mode by DIF0, DIF1 and DIF2 pins,
3) When going and exiting power down mode by PDN pin,
4) When switching normal speed and double speed by DFS pin,

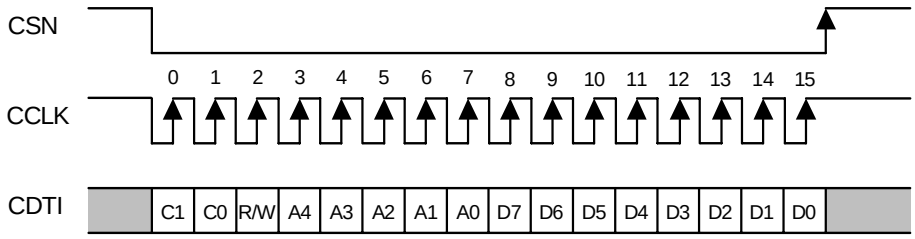
However in case of 1) & 2), If the input data is "0" or the soft mute is enabled (after 1024 LRCK cycles from SMUTE = "H"), no click noise occur except for switching DFS pin.

## ■ Mode Control Interface

Pins (parallel control mode) or registers (serial control mode) can control each functions of the AK4393. For DIF2-0, CKS2-0 and DFS, the setting of pin and register are "ORed" internally. So, even serial control mode, pin setting can also control these functions.

The serial control interface is enabled by the P/S pin = "L". In this mode, pin setting must be all "L". Internal registers may be written by 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2bits, C1/0; fixed to "01"), Read/Write (1bit; fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). The AK4393 latches the data on the rising edge of CCLK, so data should be clocked in on the falling edge. The writing of data becomes valid by CSN "↑". The clock speed of CCLK is 5MHz(max). The CSN and CCLK must be fixed to "H" when the register does not be accessed.

PDN = "L" resets the registers to their default values. When the state of P/S pin is changed, the AK4393 should be reset by PDN = "L". In serial mode, the internal timing circuit is reset by RSTN bit, but the registers are not initialized.




C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 7. Control I/F Timing

*The AK4393 does not support the read command and chip address. C1/0 and R/W are fixed to "011"
*When the AK4393 is in the power down mode (PDN = "L") or the MCLK is not provided, writing into the control register is inhibited.
*For setting the registers, the following sequence is recommended.

- Control 1 register
  (1) Writing RSTN = "0" and other bits (D6-D1) to the register at the same time.
  (2) Writing RSTN = "1" to the register. The other bits are no change.
- Control 2 register
  This writing sequence has no limitation like control 1 register.

*When RSTN = "0", the click noise is output from AOUT pins.
*If the mode setting is done without setting RSTN = "0", large noise may be output from AOUT pins. (Especially when CKS0/1/2 are changed.)

## ■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | 0 | CKS2 | CKS1 | CKS0 | DIF2 | DIF1 | DIF0 | RSTN |
| 01H | Control 2 | 0 | 0 | 0 | 0 | DFS | DEM1 | DEM0 | SMUTE |
| 02H | Test | TEST7 | TEST6 | TEST5 | TEST4 | TEST3 | TEST2 | TEST1 | TEST0 |

Notes:

For addresses from 03H to 1FH, data must not be written.

When PDN pin goes to "L", the registers are initialized to their default values. When RSTN bit goes to "0", the only internal timing is reset and the registers are not initialized to their default values. DIF2-0, CKS2-0 and DFS bits are ORed with pins respectively.

## ■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | 0 | CKS2 | CKS1 | CKS0 | DIF2 | DIF1 | DIF0 | RSTN |
| default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

RSTN: Internal timing reset

0: Reset. All registers are not initialized.

1: Normal Operation

When the states of CKS2-0 or DFS change, the AK4393 should be reset by PDN pin or RSTN bit.

DIF2-0: Audio data interface modes (see Table 5)

Initial: "000", Mode 0

Register bits are ORed with DIF2-0 pins if P/S = "L".

CKS2-0: Master Clock Frequency Select (see Table 2)

Initial: "000", Mode 0

Register bits are ORed with CKS2-0 pins if P/S = "L".

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | Control 2 | 0 | 0 | 0 | 0 | DFS | DEM1 | DEM0 | SMUTE |
| default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SMUTE: Soft Mute Enable

0: Normal operation

1: DAC outputs soft-muted

DEM1-0: De-emphasis response (see Table 6)

Initial: "00", 44.1kHz

DFS: Sampling speed control (see Table 1)

0: Normal speed

1: Double speed

Register bit is ORed with DFS pin if P/S = "L".

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02H | Test | TEST7 | TEST6 | TEST5 | TEST4 | TEST3 | TEST2 | TEST1 | TEST0 |
| default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TEST7-0: Test mode. Do not write any data to 02H.

## SYSTEM DESIGN

Figure 8 and 9 show the system connection diagram. An evaluation board (AKD4393) is available which demonstrates the optimum layout, power supply arrangements and measurement results.

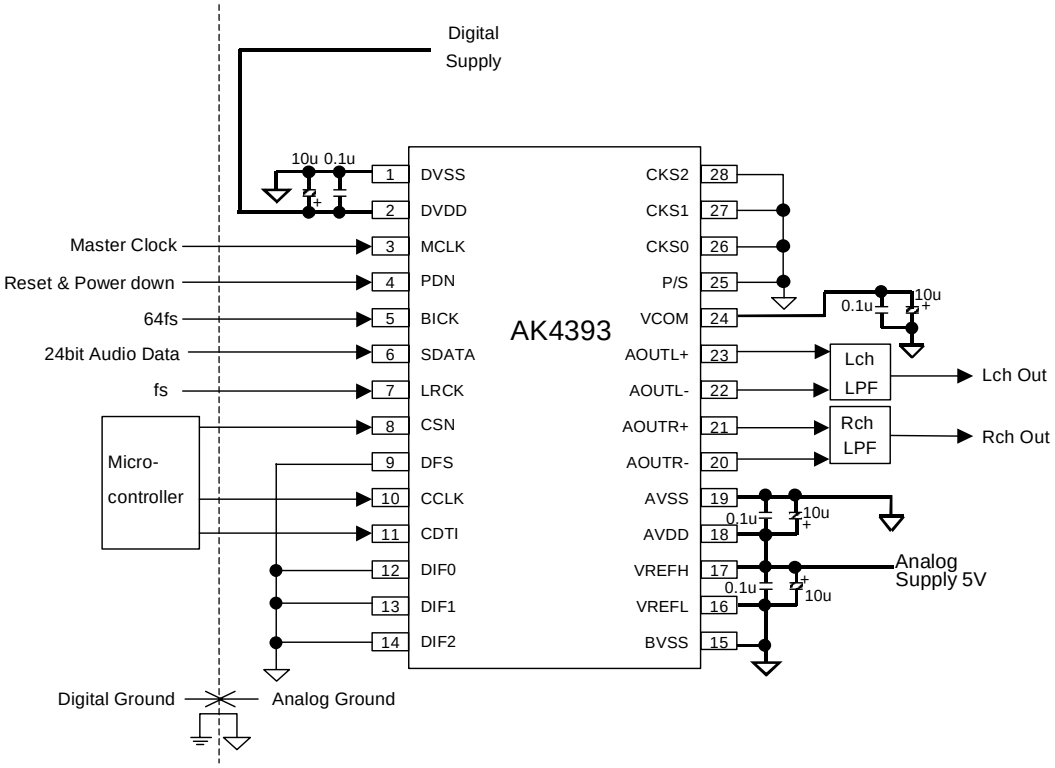



Figure 8. Typical Connection Diagram (Serial mode)

Notes:

- LRCK = fs, BICK = 64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS, BVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

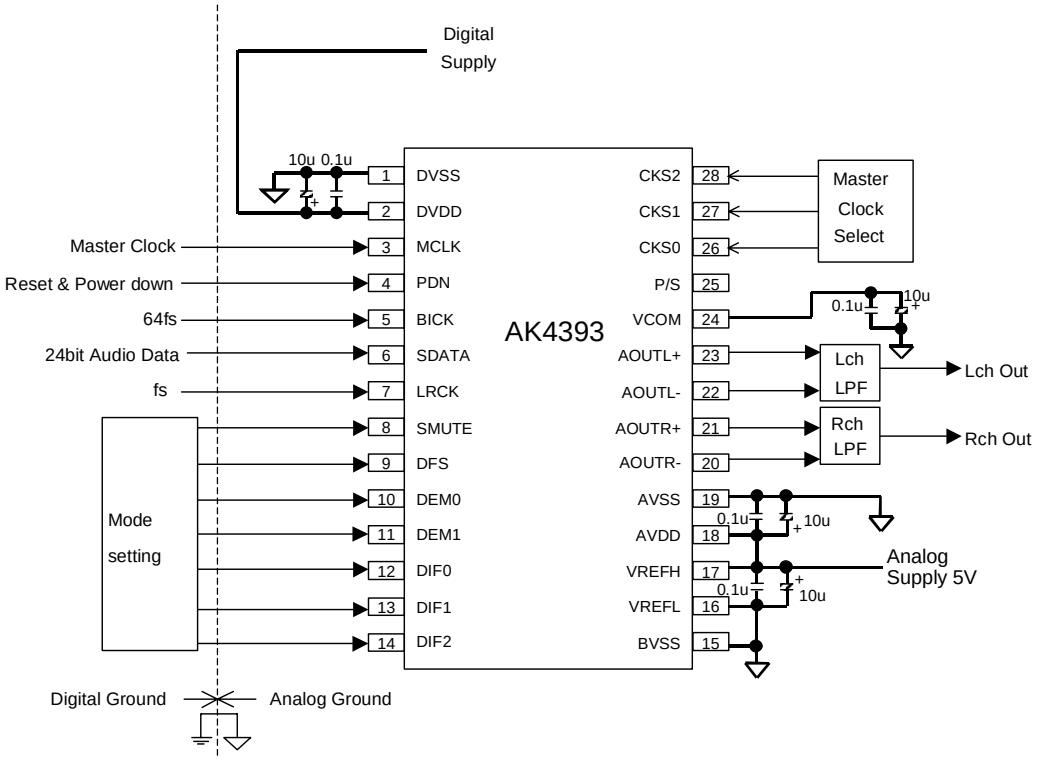



Figure 9. Typical Connection Diagram (Parallel mode)

Notes:

- LRCK = fs, BICK = 64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS, BVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

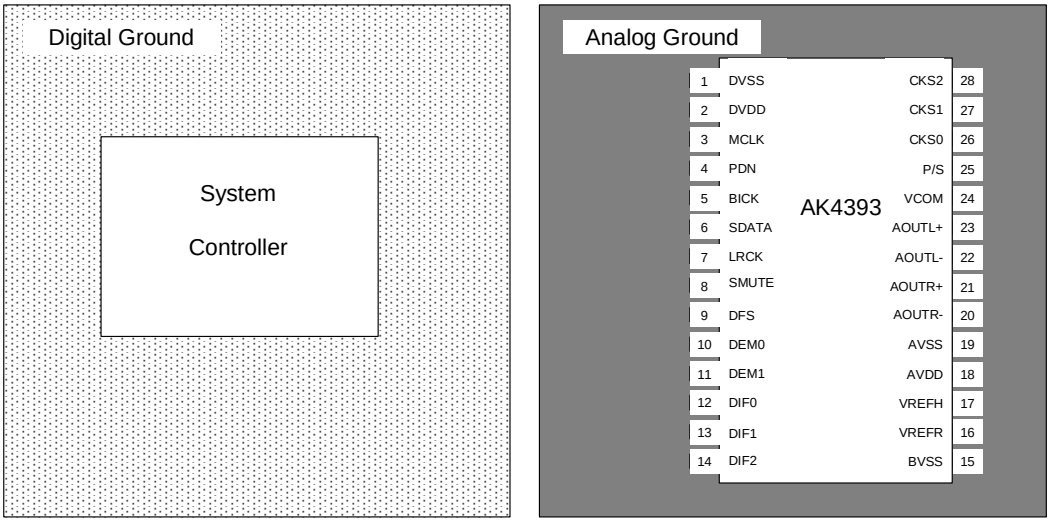



Figure 10. Ground Layout

## 1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from digital supply in system. If AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS, BVSS and DVSS must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible.

## 2. Voltage Reference

The differential Voltage between VREFH and VREFL set the analog output range. VREFH pin is normally connected to AVDD and VREFL pin is normally connected to AVSS. VREFH and VREFL should be connected with a 0.1µF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH, VREFL and VCOM pins in order to avoid unwanted coupling into the AK4393.

## 3. Analog Outputs

The analog outputs are full differential outputs and 2.4Vpp (typ@VREF=5V) centered around VCOM. The differential outputs are summed externally, $V_{AOUT}$ = (AOUT+) - (AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 4.8Vpp (typ@VREF=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage ($V_{AOUT}$) is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal $V_{AOUT}$ is 0V for 000000H(@24bit).

The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

Figure 11 shows an example of external LPF circuit summing the differential outputs by an op-amp.
Figure 12 shows an example of differential outputs and LPF circuit example by three op-amps.

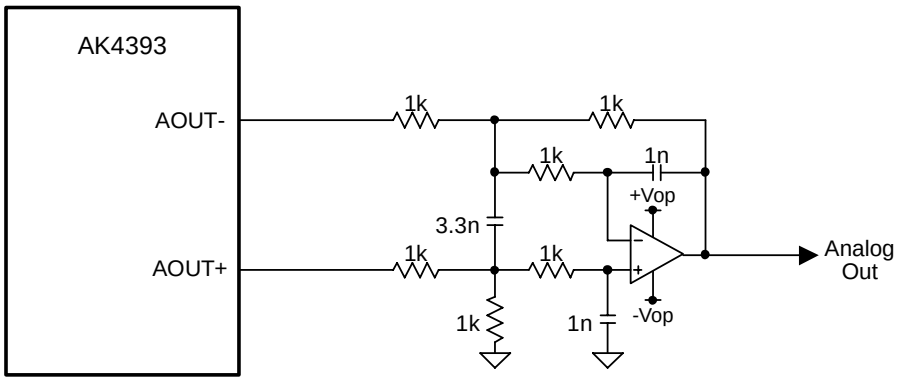



Figure 11. External LPF Circuit Example 1

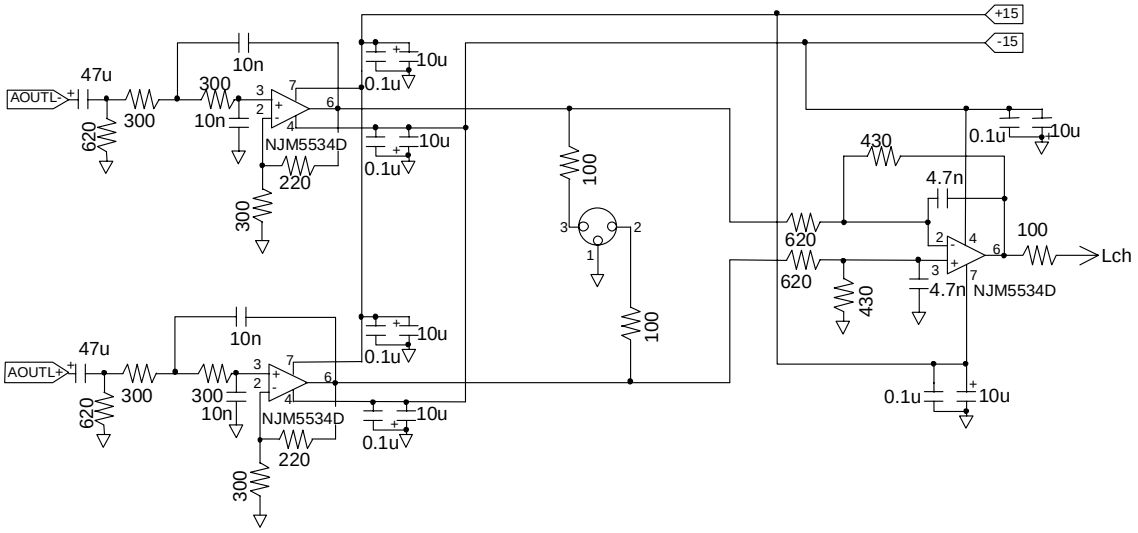
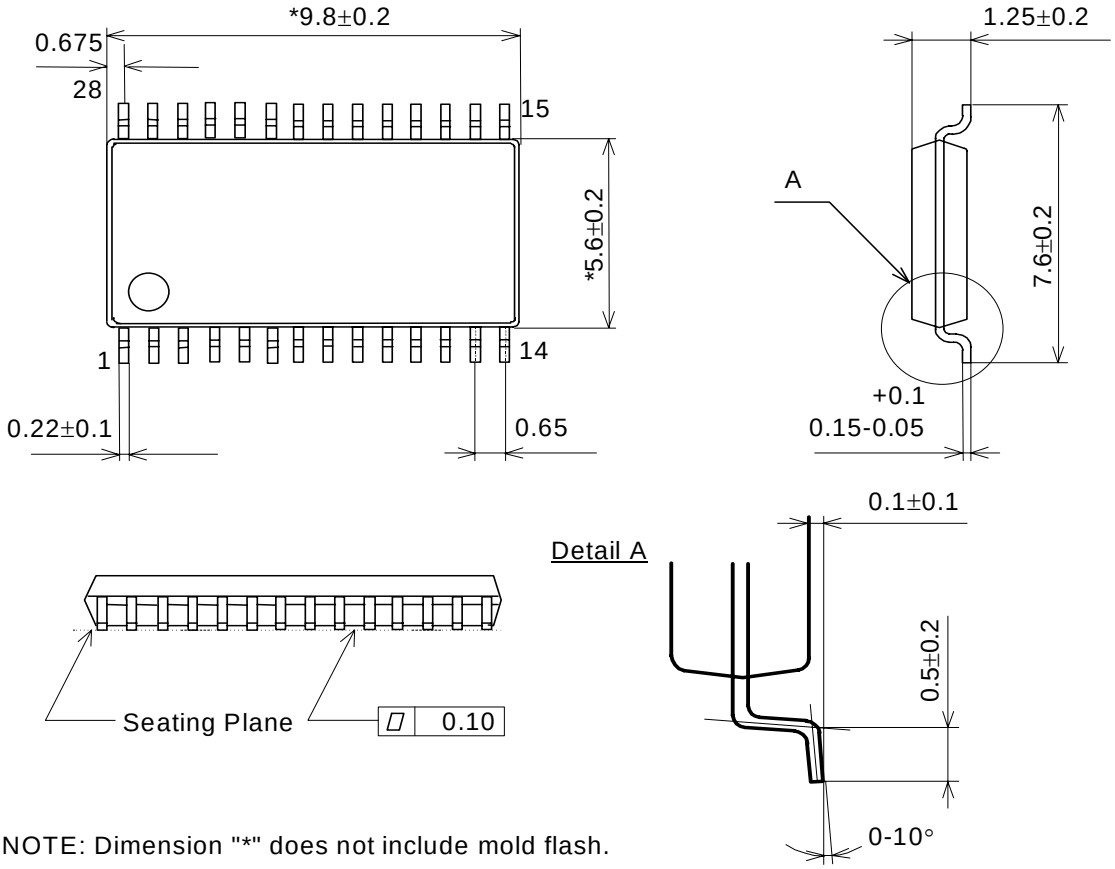



Figure 12. External LPF Circuit Example 2

## PACKAGE

28pin VSOP (Unit: mm)

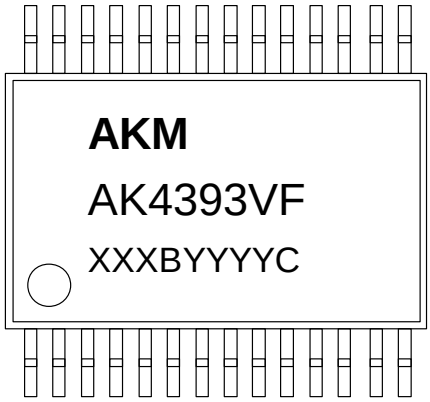



NOTE: Dimension "*" does not include mold flash.

■ **Material & Lead finish**

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

## MARKING




XXXXBYYYYC data code identifier

XXXB: Lot number (X : Digit number, B : Alpha character )
YYYYC: Assembly date (Y : Digit number C : Alpha character)

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## Appendix A

In Double Speed Mode, the phase relationship between MCLK and LRCK/BICK is limited (Table 7). If the phase relationship happens during this prohibited period, it is possible to occur the inverse of output channel. The phase relationship must be set to avoid the prohibited period when the AK4393 operates at Double Speed Mode. The prohibited period is specified by the combination of digital power supply voltage (DVDD), MCLK frequency and audio data format (Table 5). When the audio data formats are 16/20/24bit LSB Justified (Mode 0,1,4) and 24bit MSB Justified (Mode 2), the phase relationship (tLRM: Figure 11) between the rising edge of LRCK and the rising edge of MCLK has the prohibited period of min to max in Table 7. In case of $I^2S$ Compatible (Mode 3), the relationship between the falling edge of BICK and the rising edge of MCLK has the prohibited period (tBCM: Figure 12)

| Sampling Mode | Digital Power Supply, DVDD | MCLK Frequency | Mode Setting | | | | Prohibited Period | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | CKS2 | CKS1 | CKS0 | DFS | min | max | |
| Double Speed | 3.0 to 5.25V | 128fs | 0 | 0 | 0 | 1 | 0.4 | 1.7 | ns |
| Double Speed | 3.0 to 5.25V | 192fs | 0 | 1 | 0 | 1 | -0.5 | 0.8 | ns |
| Double Speed | 3.0 to 5.25V | 256fs | 0 | 0 | 1 | 1 | -0.7 | 0.7 | ns |
| Double Speed | 3.0 to 5.25V | 256fs | 1 | 0 | 0 | 1 | -0.7 | 0.7 | ns |
| Double Speed | 3.0 to 5.25V | 384fs | 0 | 1 | 1 | 1 | -1.7 | -0.3 | ns |
| Double Speed | 3.0 to 5.25V | 384fs | 1 | 1 | 0 | 1 | -1.7 | -0.3 | ns |
| Double Speed | 4.75 to 5.25V | 128fs | 0 | 0 | 0 | 1 | 0.8 | 1.5 | ns |
| Double Speed | 4.75 to 5.25V | 192fs | 0 | 1 | 0 | 1 | -0.2 | 0.5 | ns |
| Double Speed | 4.75 to 5.25V | 256fs | 0 | 0 | 1 | 1 | -0.3 | 0.4 | ns |
| Double Speed | 4.75 to 5.25V | 256fs | 1 | 0 | 0 | 1 | -0.3 | 0.4 | ns |
| Double Speed | 4.75 to 5.25V | 384fs | 0 | 1 | 1 | 1 | -1.0 | -0.3 | ns |
| Double Speed | 4.75 to 5.25V | 384fs | 1 | 1 | 0 | 1 | -1.0 | -0.3 | ns |

Table **7**. Prohibited Period

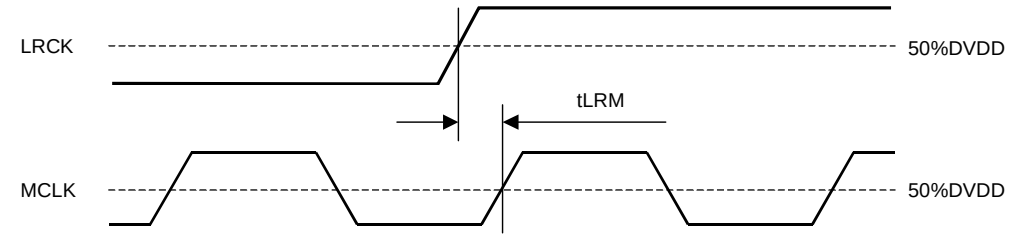



Figure 11. 16/20/24bit LSB Justified, 24bit MSB Justified

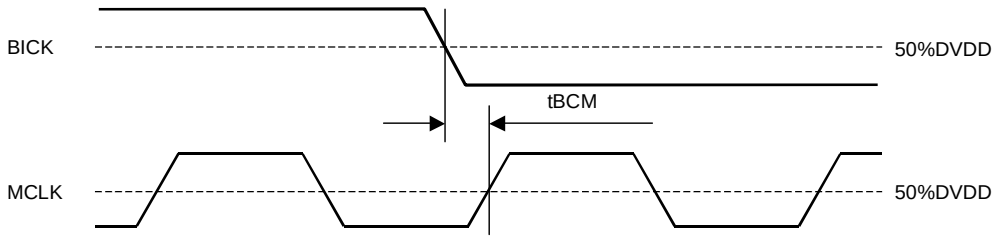



Figure 12. $I^2S$ Compatible

# AK4527B
## High Performance Multi-channel Audio CODEC

## GENERAL DESCRIPTION

The AK4527B is a single chip CODEC that includes two channels of ADC and six channels of DAC. The ADC outputs 24bit data and the DAC accepts up to 24bit input data. The ADC has the Enhanced Dual Bit architecture with wide dynamic range. The DAC introduces the new developed Advanced Multi-Bit architecture, and achieves wider dynamic range and lower outband noise. An auxiliary digital audio input interface maybe used instead of the ADC for passing audio data to the primary audio output port. Control may be set directly by pins or programmed through a separate serial interface.

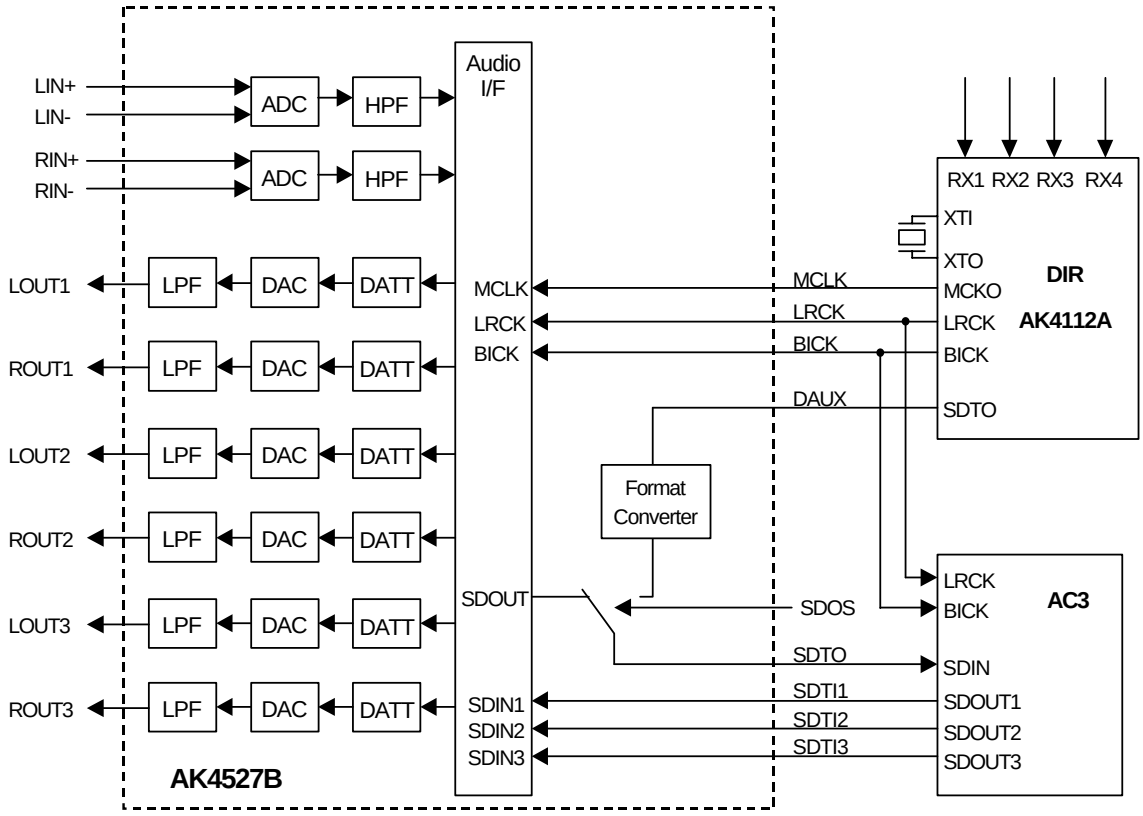
The AK4527B has a dynamic range of 102dB for ADC, 106dB for DAC and is well suited for digital surround for home theater and car audio. An AC-3 system can be built with a IEC60958(SPDIF) receiver such as the AK4112A. The AK4527B is available in a small 44pin LQFP package which will reduce system space.

*AC-3 is a trademark of Dolby Laboratories.

## FEATURES

- **2ch 24bit ADC**
  - **64x Oversampling**
  - **Sampling Rate up to 96kHz**
  - **Linear Phase Digital Anti-Alias Filter**
  - **Differential Inputs with single-ended use capability**
  - **S/(N+D): 92dB**
  - **Dynamic Range, S/N: 102dB**
  - **Digital HPF for offset cancellation**
  - **I/F format: MSB justified or $I^2S$**
  - **Overflow flag**
- **6ch 24bit DAC**
  - **128x Oversampling**
  - **Sampling Rate up to 96kHz**
  - **24bit 8 times Digital Filter**
  - **Single-Ended Outputs**
  - **On-chip Switched-Capacitor Filter**
  - **S/(N+D): 90dB**
  - **Dynamic Range, S/N: 106dB**
  - **I/F format: MSB justified, LSB justified(20bit,24bit) or $I^2S$**
  - **Individual channel digital volume with 256 levels and 0.5dB step**
  - **Soft mute**
  - **De-emphasis for 32kHz, 44.1kHz and 48kHz**
  - **Zero Detect Function**
- **High Jitter Tolerance**
- **TTL Level Digital I/F**
- **3-wire Serial and $I^2C$ Bus µP I/F for mode setting**
- **Master clock:256fs, 384fs or 512fs for fs=32kHz to 48kHz**
  **128fs, 192fs or 256fs for fs=64kHz to 96kHz**
- **Power Supply: 4.5 to 5.5V**
- **Power Supply for output buffer: 2.7 to 5.5V**
- **Small 44pin LQFP**

## ■ Block Diagram

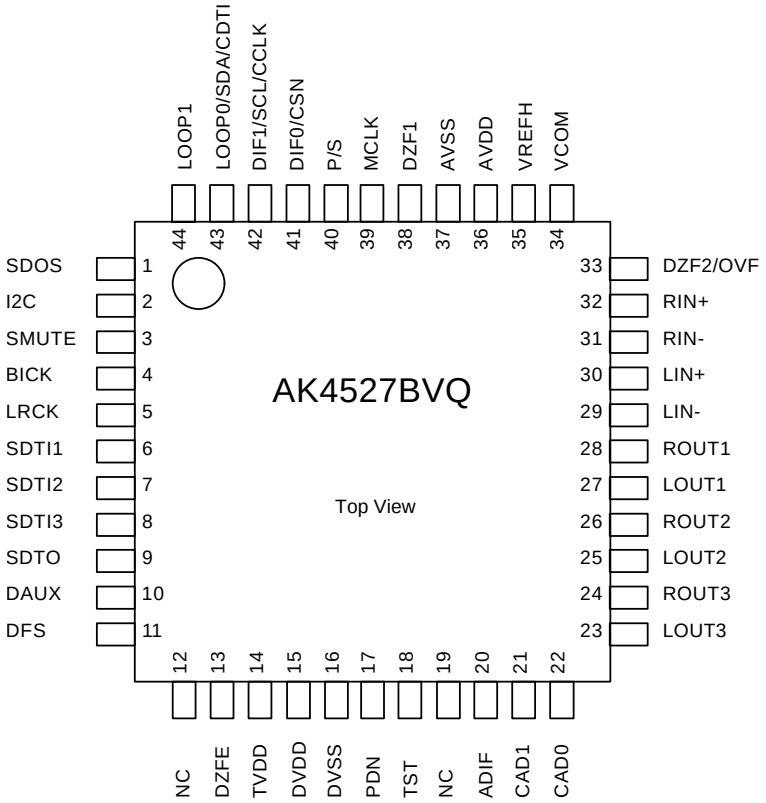



Block Diagram (DIR and AC-3 DSP are external parts)

## ■ Ordering Guide

| | | |
|---|---|---|
| AK4527BVQ | -40 ~ +85°C | 44pin LQFP(0.8mm pitch) |
| AKD4527B | Evaluation Board for AK4527B | |

## ■ Pin Layout



## ■ Compatibility with AK4527

### 1. Functions

| Functions | AK4527 | AK4527B |
|---|---|---|
| Overflow flag | Not available | Available |
| Clock mode | Setting by pin/bit | Auto setting |
| Sampling speed mode auto setting | Not available | Available<br>(MCLK is fixed at auto setting mode;<br>Normal: 512fs, Double: 256fs) |
| Zero detection | Serial mode only | Parallel/Serial mode |
| De-emphasis setting | Pin/Register | Register only |
| $I^2C$ bus mode | Not available | Available |
| Analog output at power down mode | Hi-Z | VCOM voltage |

### 2. Pin Configuration

| Pin# | AK4527 | AK4527B |
|---|---|---|
| 12 | DEM1 | NC |
| 13 | DEM0 | DZFE |
| 18 | ICKS2 | TST |
| 19 | ICKS1 | NC |
| 20 | ICKS0 | ADIF |
| 33 | DZF2 | DZF2/OVF |

### 3. Register

| Addr | Changed items |
|---|---|
| 00H | DIF1-0 default values are changed from mode 0 to mode 2. |
| 01H | ACKS (Clock auto setting mode) is added. |
| 08H | DEMA1-C0 default values are changed from “44.1kHz” to “OFF”. |
| 09H | ICKS2-0 are removed. |
| 0AH | OVFE (Overflow detection enable) is added. |

## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | SDOS | I | SDTO Source Select Pin (Note 1)<br>"L": Internal ADC output, "H": DAUX input |
| 2 | I2C | I | Control Mode Select Pin<br>"L": 3-wire Serial, "H": $I^2C$ Bus |
| 3 | SMUTE | I | Soft Mute Pin (Note 1)<br>When this pin goes to "H", soft mute cycle is initialized.<br>When returning to "L", the output mute releases. |
| 4 | BICK | I | Audio Serial Data Clock Pin |
| 5 | LRCK | I | Input Channel Clock Pin |
| 6 | SDTI1 | I | DAC1 Audio Serial Data Input Pin |
| 7 | SDTI2 | I | DAC2 Audio Serial Data Input Pin |
| 8 | SDTI3 | I | DAC3 Audio Serial Data Input Pin |
| 9 | SDTO | O | Audio Serial Data Output Pin |
| 10 | DAUX | I | AUX Audio Serial Data Input Pin |
| 11 | DFS | I | Double Speed Sampling Mode Pin (Note 1)<br>"L": Normal Speed, "H": Double Speed |
| 12 | NC | - | No Connect<br>No internal bonding. |
| 13 | DZFE | I | Zero Input Detect Enable Pin<br>"L": mode 7 (disable) at parallel mode,<br>zero detect mode is selectable by DZFM2-0 bits at serial mode<br>"H": mode 0 (DZF1 is AND of all six channels) |
| 14 | TVDD | - | Output Buffer Power Supply Pin, 2.7V~5.5V |
| 15 | DVDD | - | Digital Power Supply Pin, 4.5V~5.5V |
| 16 | DVSS | - | Digital Ground Pin, 0V |
| 17 | PDN | I | Power-Down & Reset Pin<br>When "L", the AK4527B is powered-down and the control registers are reset to default state. If the state of P/S or CAD0-1 changes, then the AK4527B must be reset by PDN. |
| 18 | TST | I | Test Pin<br>This pin should be connected to DVSS. |
| 19 | NC | - | No Connect<br>No internal bonding. |
| 20 | ADIF | I | Analog Input Format Select Pin<br>"H": Full-differential input, "L": Single-ended input |
| 21 | CAD1 | I | Chip Address 1 Pin |
| 22 | CAD0 | I | Chip Address 0 Pin |

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 23 | LOUT3 | O | DAC3 Lch Analog Output Pin |
| 24 | ROUT3 | O | DAC3 Rch Analog Output Pin |
| 25 | LOUT2 | O | DAC2 Lch Analog Output Pin |
| 26 | ROUT2 | O | DAC2 Rch Analog Output Pin |
| 27 | LOUT1 | O | DAC1 Lch Analog Output Pin |
| 28 | ROUT1 | O | DAC1 Rch Analog Output Pin |
| 29 | LIN- | I | Lch Analog Negative Input Pin |
| 30 | LIN+ | I | Lch Analog Positive Input Pin |
| 31 | RIN- | I | Rch Analog Negative Input Pin |
| 32 | RIN+ | I | Rch Analog Positive Input Pin |
| 33 | DZF2 | O | Zero Input Detect 2 Pin (Note 2)<br>When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". |
| | OVF | O | Analog Input Overflow Detect Pin (Note 3)<br>This pin goes to "H" if the analog input of Lch or Rch is overflows. |
| 34 | VCOM | O | Common Voltage Output Pin, AVDD/2<br>Large external capacitor around 2.2µF is used to reduce power-supply noise. |
| 35 | VREFH | I | Positive Voltage Reference Input Pin, AVDD |
| 36 | AVDD | - | Analog Power Supply Pin, 4.5V~5.5V |
| 37 | AVSS | - | Analog Ground Pin, 0V |
| 38 | DZF1 | O | Zero Input Detect 1 Pin (Note 2)<br>When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". |
| 39 | MCLK | I | Master Clock Input Pin |
| 40 | P/S | I | Parallel/Serial Select Pin<br>"L": Serial control mode, "H": Parallel control mode |
| 41 | DIF0 | I | Audio Data Interface Format 0 Pin in parallel control mode |
| | CSN | I | Chip Select Pin in 3-wire serial control mode<br>This pin should be connected to DVDD at $I^2C$ bus control mode |
| 42 | DIF1 | I | Audio Data Interface Format 1 Pin in parallel control mode |
| | SCL/CCLK | I | Control Data Clock Pin in serial control mode<br>I2C = "L": CCLK (3-wire Serial), I2C = "H": SCL ($I^2C$ Bus) |
| 43 | LOOP0 | I | Loopback Mode 0 Pin in parallel control mode<br>Enables digital loop-back from ADC to 3 DACs. |
| | SDA/CDTI | I/O | Control Data Input Pin in serial control mode<br>I2C = "L": CDTI (3-wire Serial), I2C = "H": SDA ($I^2C$ Bus) |
| 44 | LOOP1 | I | Loopback Mode 1 Pin (Note 1)<br>Enables all 3 DAC channels to be input from SDTI1. |

Notes: 1. SDOS, SMUTE, DFS, and LOOP1 pins are ORed with register data if P/S = "L".
2. The group 1 and 2 can be selected by DZFM2-0 bits if P/S = "L" and DZFE = "L".
3. This pin becomes OVF pin if OVFE bit is set to "1" at serial control mode.
4. All input pins should not be left floating.

## ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 5)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supplies | Analog | AVDD | -0.3 | 6.0 | V |
| | Digital | DVDD | -0.3 | 6.0 | V |
| | Output buffer | TVDD | -0.3 | 6.0 | V |
| | \|AVSS-DVSS\| (Note 6) | ΔGND | - | 0.3 | V |
| Input Current (any pins except for supplies) | | IIN | - | ±10 | mA |
| Analog Input Voltage | | VINA | -0.3 | AVDD+0.3 | V |
| Digital Input Voltage | | VIND | -0.3 | DVDD+0.3 | V |
| Ambient Temperature (power applied) | | Ta | -40 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Notes: 5. All voltages with respect to ground.
6. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 5)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Power Supplies (Note 7) | Analog | AVDD | 4.5 | 5.0 | 5.5 | V |
| | Digital | DVDD | 4.5 | 5.0 | 5.5 | V |
| | Output buffer | TVDD | 2.7 | 5.0 | 5.5 | V |

Notes: 5. All voltages with respect to ground.
7. The power up sequence between AVDD, DVDD and TVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

## ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, TVDD=5V; AVSS, DVSS=0V; VREFH=AVDD; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at fs=44.1kHz, 20Hz~40kHz at fs=96kHz; unless otherwise specified)

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **ADC Analog Input Characteristics: Differential Inputs; Analog Source Impedance=470Ω** | | | | | | |
| Resolution | | | | | 24 | Bits |
| S/(N+D) | (-0.5dBFS) | fs=44.1kHz | 84 | 92 | | dB |
| | (Note 8) | fs=96kHz | - | 83 | | dB |
| DR | (-60dBFS) | fs=44.1kHz, A-weighted | 94 | 102 | | dB |
| | | fs=96kHz | 88 | 96 | | dB |
| | | fs=96kHz, A-weighted | 93 | 102 | | dB |
| S/N | (Note 9) | fs=44.1kHz, A-weighted | 94 | 102 | | dB |
| | | fs=96kHz | 88 | 96 | | dB |
| | | fs=96kHz, A-weighted | 93 | 102 | | dB |
| Interchannel Isolation | | | 90 | 110 | | dB |
| **DC Accuracy** | | | | | | |
| Interchannel Gain Mismatch | | | | 0.2 | 0.3 | dB |
| Gain Drift | | | | 20 | - | ppm/°C |
| Input Voltage | AIN=0.6xVREFH | (Note 10) | 2.85 | 3.0 | 3.15 | Vpp |
| Input Resistance | | (Note 11) | 18 | 28 | | kΩ |
| Power Supply Rejection | | (Note 12) | | 50 | | dB |
| **DAC Analog Output Characteristics:** | | | | | | |
| Resolution | | | | | 24 | Bits |
| S/(N+D) | | fs=44.1kHz | 80 | 90 | | dB |
| | | fs=96kHz | 78 | 88 | | dB |
| DR | (-60dBFS) | fs=44.1kHz, A-weighted | 95 | 106 | | dB |
| | | fs=96kHz | 88 | 100 | | dB |
| | | fs=96kHz, A-weighted | 94 | 106 | | dB |
| S/N | (Note 13) | fs=44.1kHz, A-weighted | 95 | 106 | | dB |
| | | fs=96kHz | 88 | 100 | | dB |
| | | fs=96kHz, A-weighted | 94 | 106 | | dB |
| Interchannel Isolation | | | 90 | 110 | | dB |
| **DC Accuracy** | | | | | | |
| Interchannel Gain Mismatch | | | | 0.2 | 0.5 | dB |
| Gain Drift | | | | 20 | - | ppm/°C |
| Output Voltage | AOUT=0.6xVREFH | | 2.75 | 3.0 | 3.25 | Vpp |
| Load Resistance | | | 5 | | | kΩ |
| Power Supply Rejection | | (Note 12) | | 50 | | dB |
| **Power Supplies** | | | | | | |
| Power Supply Current | | | | | | |
| Normal Operation (PDN = "H") | | | | | | |
| AVDD | | | | 35 | 56 | mA |
| DVDD+TVDD | fs=44.1kHz | (Note 14) | | 25 | 40 | mA |
| | fs=96kHz | | | 35 | 56 | mA |
| Power-down mode (PDN = "L") | | (Note 15) | | 80 | 200 | μA |

Notes:
8. In case of single ended input, S/(N+D)=80dB(typ, @AVDD=5V, fs=44.1kHz).
9. S/N measured by CCIR-ARM is 98dB(@fs=44.1kHz).
10. Full scale input for each AIN+/- pin is 1.5Vpp in differential mode.
11. Input resistance is 14kΩ typically at fs=96kHz.
12. PSR is applied to AVDD, DVDD and TVDD with 1kHz, 50mVpp. VREFH pin is held a constant voltage.
13. S/N measured by CCIR-ARM is 102dB(@fs=44.1kHz).
14. DVDD=TBDmA, TVDD=TBDmA(typ).
15. In the power-down mode. All digital input pins including clock pins (MCLK, BICK, LRCK) are held DVSS.

## FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=4.5~5.5V; TVDD=2.7~5.5V; fs=44.1kHz; DEM=OFF)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 16) | -0.005dB | PB | 0 | | 19.76 | kHz |
| | -0.02dB | | - | 20.02 | - | kHz |
| | -0.06dB | | - | 20.20 | - | kHz |
| | -6.0dB | | - | 22.05 | - | kHz |
| Stopband | | SB | 24.34 | | | kHz |
| Passband Ripple | | PR | | | ±0.005 | dB |
| Stopband Attenuation | | SA | 80 | | | dB |
| Group Delay (Note 17) | | GD | | 27.6 | | 1/fs |
| Group Delay Distortion | | ΔGD | | 0 | | μs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency Response (Note 16) | -3dB | FR | | 0.9 | | Hz |
| | -0.5dB | | | 2.7 | | Hz |
| | -0.1dB | | | 6.0 | | Hz |
| **DAC Digital Filter:** | | | | | | |
| Passband (Note 16) | -0.1dB | PB | 0 | | 20.0 | kHz |
| | -6.0dB | | - | 22.05 | - | kHz |
| Stopband | | SB | 24.2 | | | kHz |
| Passband Ripple | | PR | | | ±0.02 | dB |
| Stopband Attenuation | | SA | 56 | | | dB |
| Group Delay (Note 17) | | GD | | 21.9 | | 1/fs |
| **DAC Digital Filter + Analog Filter:** | | | | | | |
| Frequency Response: 0 ~ 20.0kHz | | FR | | ±0.2 | | dB |
| 40.0kHz (Note 18) | | FR | | ±0.3 | | dB |

Notes: 16. The passband and stopband frequencies scale with fs.
For example, 20.02kHz at –0.02dB is 0.454 x fs. The reference frequency of these responses is 1kHz.

17. The calculating delay time which occurred by digital filtering. This time is from setting the input of analog signal to setting the 24bit data of both channels to the output register for ADC.
For DAC, this time is from setting the 20/24bit data of both channels on input register to the output of analog signal.

18. fs=96kHz.

## DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=4.5~5.5V; TVDD=2.7~5.5V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | VIH | 2.2 | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 0.8 | V |
| High-Level Output Voltage | | | | | |
| (SDTO pin: Iout=-100μA) | VOH | TVDD-0.5 | - | - | V |
| (DZF1, DZF2/OZF pins: Iout=-100μA) | VOH | AVDD-0.5 | - | - | V |
| Low-Level Output Voltage | | | | | |
| (SDTO, DZF1, DZF2/OZF pins: Iout= 100μA) | VOL | - | - | 0.5 | V |
| (SDA pin: Iout= 3mA) | VOL | - | - | 0.4 | V |
| Input Leakage Current | Iin | - | - | ±10 | μA |

## SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=4.5~5.5V; $C_L$=20pF)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Master Clock Input** | | | | | |
| 256fsn, 128fsd: | fCLK | 8.192 | | 12.288 | MHz |
| Pulse Width Low | tCLKL | 27 | | | ns |
| Pulse Width High | tCLKH | 27 | | | ns |
| 384fsn, 192fsd: | fCLK | 12.288 | | 18.432 | MHz |
| Pulse Width Low | tCLKL | 20 | | | ns |
| Pulse Width High | tCLKH | 20 | | | ns |
| 512fsn, 256fsd: | fCLK | 16.384 | | 24.576 | MHz |
| Pulse Width Low | tCLKL | 15 | | | ns |
| Pulse Width High | tCLKH | 15 | | | ns |
| **LRCK frequency** | | | | | |
| Normal Speed Mode | fsn | 32 | | 48 | kHz |
| Double Speed Mode | fsd | 64 | | 96 | kHz |
| Duty Cycle | Duty | 45 | | 55 | % |
| **Audio Interface Timing** | | | | | |
| BICK Period | tBCK | 160 | | | ns |
| BICK Pulse Width Low | tBCKL | 65 | | | ns |
| Pulse Width High | tBCKH | 65 | | | ns |
| LRCK Edge to BICK "↑" (Note 19) | tLRB | 45 | | | ns |
| BICK "↑" to LRCK Edge (Note 19) | tBLR | 45 | | | ns |
| LRCK to SDTO(MSB) | tLRS | | | 40 | ns |
| BICK "↓" to SDTO | tBSD | | | 40 | ns |
| SDTI1-3, DAUX Hold Time | tSDH | 40 | | | ns |
| SDTI1-3, DAUX Setup Time | tSDS | 25 | | | ns |

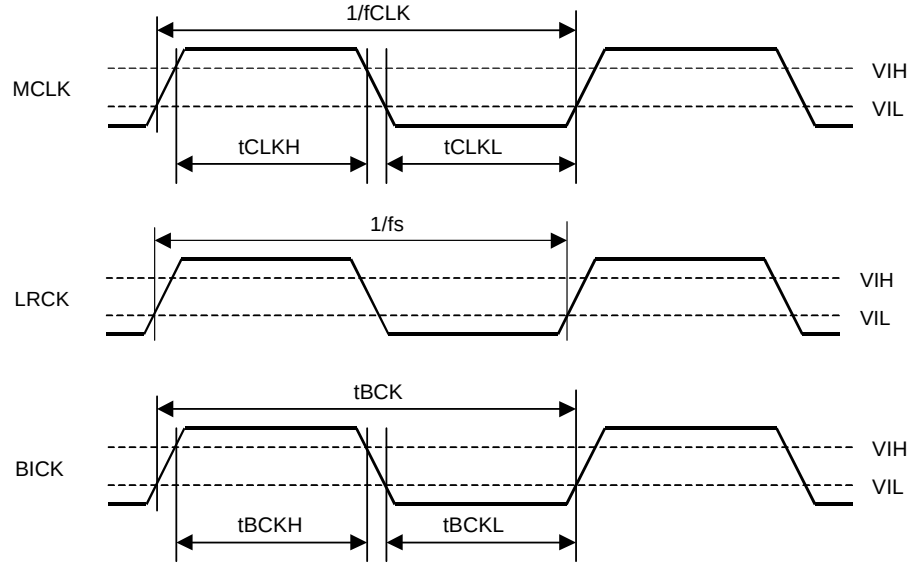
Notes: 19. BICK rising edge must not occur at the same time as LRCK edge.

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Control Interface Timing (3-wire Serial mode):** | | | | | |
| CCLK Period | tCCK | 200 | | | ns |
| CCLK Pulse Width Low | tCCKL | 80 | | | ns |
| Pulse Width High | tCCKH | 80 | | | ns |
| CDTI Setup Time | tCDS | 40 | | | ns |
| CDTI Hold Time | tCDH | 40 | | | ns |
| CSN "H" Time | tCSW | 0.025*1/fs | | | ns |
| CSN "↓" to CCLK "↑" | tCSS | 50 | | | ns |
| CCLK "↑" to CSN "↑" | tCSH | 50 | | | ns |
| Rise Time of CSN | tR1 | | | 20 | ns |
| Fall Time of CSN | tF1 | | | 20 | ns |
| Rise Time of CCLK | tR2 | | | 20 | ns |
| Fall Time of CCLK | tF2 | | | 20 | ns |
| **Control Interface Timing ($I^2C$ Bus mode):** | | | | | |
| SCL Clock Frequency | fSCL | - | | 100 | kHz |
| Bus Free Time Between Transmissions | tBUF | 4.7 | | - | µs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 4.0 | | - | µs |
| Clock Low Time | tLOW | 4.7 | | - | µs |
| Clock High Time | tHIGH | 4.0 | | - | µs |
| Setup Time for Repeated Start Condition | tSU:STA | 4.7 | | - | µs |
| SDA Hold Time from SCL Falling (Note 20) | tHD:DAT | 0 | | - | µs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.25 | | - | µs |
| Rise Time of Both SDA and SCL Lines | tR | - | | 1.0 | µs |
| Fall Time of Both SDA and SCL Lines | tF | - | | 0.3 | µs |
| Setup Time for Stop Condition | tSU:STO | 4.0 | | - | µs |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | | 50 | ns |
| **Power-down & Reset Timing** | | | | | |
| PDN Pulse Width (Note 21) | tPD | 150 | | | ns |
| PDN "↑" to SDTO valid (Note 22) | tPDV | | 522 | | 1/fs |

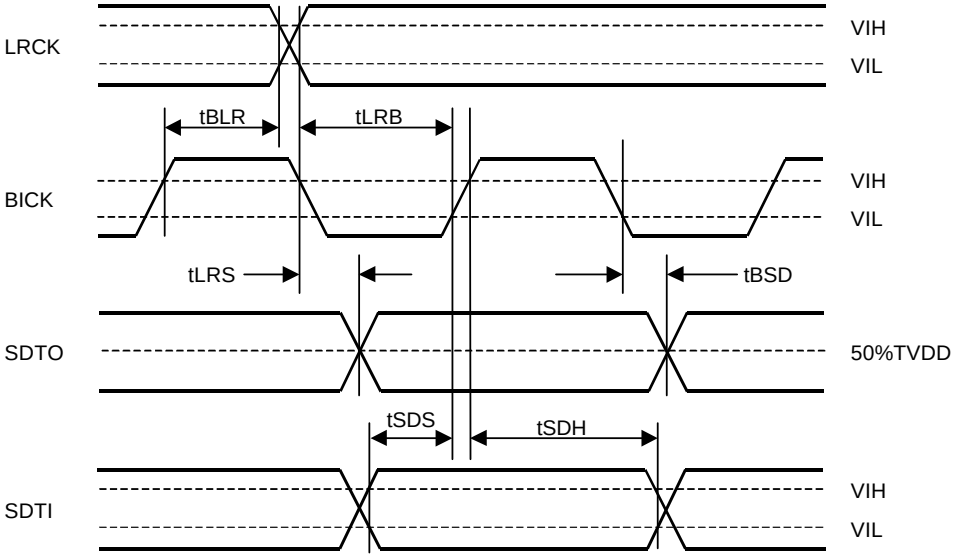
Notes: 20. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
21. The AK4527B can be reset by bringing PDN "L" to "H" upon power-up.
22. These cycles are the number of LRCK rising from PDN rising.
23. $I^2C$ is a registered trademark of Philips Semiconductors.

Purchase of Asahi Kasei Microsystems Co., Ltd $I^2C$ components conveys a license under the Philips $I^2C$ patent to use the components in the $I^2C$ system, provided the system conform to the $I^2C$ specifications defined by Philips.

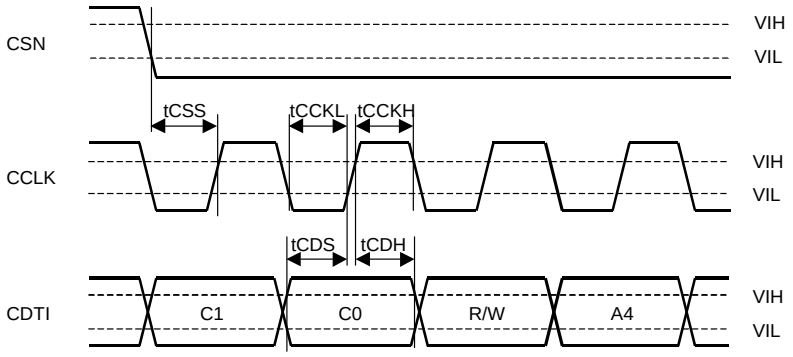
■ **Timing Diagram**



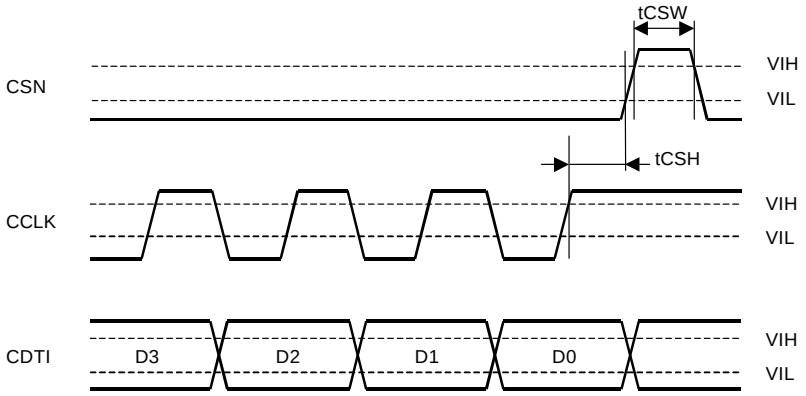

Clock Timing



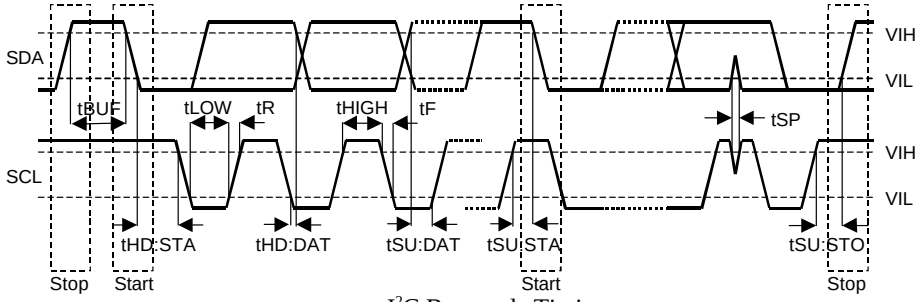

Audio Interface Timing



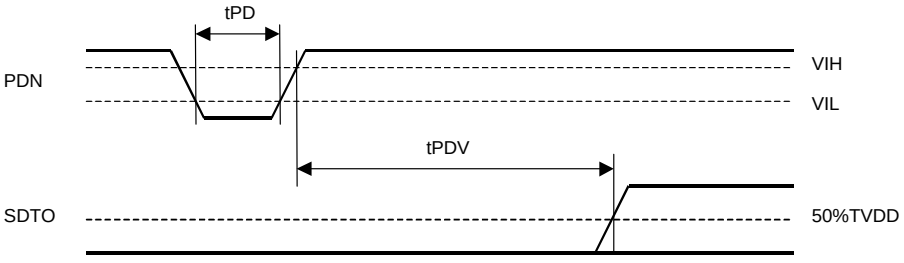

WRITE Command Input Timing (3-wire Serial mode)




WRITE Data Input Timing (3-wire Serial mode)




$I^2C$ Bus mode Timing




Power-down & Reset Timing

## OPERATION OVERVIEW

### ■ System Clock

The external clocks, which are required to operate the AK4527B, are MCLK, LRCK and BICK. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS = "0": Default), the sampling speed is set by DFS (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 2, 3). In Auto Setting Mode (ACKS = "1"), as MCLK frequency is detected automatically (Table 4), and the internal master clock becomes the appropriate frequency (Table 5), it is not necessary to set DFS.

MCLK should be synchronized with LRCK but the phase is not critical. External clocks (MCLK, BICK) should always be present whenever the AK4527B is in normal operation mode (PDN = "H"). If these clocks are not provided, the AK4527B may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4527B should be in the power-down mode (PDN = "L") or in the reset mode (RSTN = "0"). After exiting reset at power-up etc., the AK4527B is in the power-down mode until MCLK and LRCK are input.

| DFS | Sampling Speed (fs) | | |
|---|---|---|---|
| 0 | Normal Speed Mode | 32kHz~48kHz | Default |
| 1 | Double Speed Mode | 64kHz~96kHz | |

Table 1. Sampling Speed (Manual Setting Mode)

| LRCK | MCLK (MHz) | | | BICK (MHz) |
|---|---|---|---|---|
| fs | 256fs | 384fs | 512fs | 64fs |
| 32.0kHz | 8.1920 | 12.2880 | 16.3840 | 2.0480 |
| 44.1kHz | 11.2896 | 16.9344 | 22.5792 | 2.8224 |
| 48.0kHz | 12.2880 | 18.4320 | 24.5760 | 3.0720 |

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode)

| LRCK | MCLK (MHz) | | | BICK (MHz) |
|---|---|---|---|---|
| fs | 128fs | 192fs | 256fs | 64fs |
| 88.2kHz | 11.2896 | 16.9344 | 22.5792 | 5.6448 |
| 96.0kHz | 12.2880 | 18.4320 | 24.5760 | 6.1440 |

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)
(Note: At double speed mode(DFS = "1"), 128fs and 192fs are not available for ADC.)

| MCLK | Sampling Speed |
|---|---|
| 512fs | Normal |
| 256fs | Double |

Table 4. Sampling Speed (Auto Setting Mode)

| LRCK | MCLK (MHz) | | Sampling Speed |
|---|---|---|---|
| fs | 256fs | 512fs | |
| 32.0kHz | - | 16.3840 | Normal |
| 44.1kHz | - | 22.5792 | |
| 48.0kHz | - | 24.5760 | |
| 88.2kHz | 22.5792 | - | Double |
| 96.0kHz | 24.5760 | - | |

Table 5. System Clock Example (Auto Setting Mode)

## ■ De-emphasis Filter

The AK4527B includes the digital de-emphasis filter (tc=50/15µs) by IIR filter. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis of each DAC can be set individually by register data of DEMA1-C0 (DAC1: DEMA1-0, DAC2: DEMB1-0, DAC3: DEMC1-0, see "Register Definitions").

| Mode | Sampling Speed | DEM1 | DEM0 | DEM | |
|---|---|---|---|---|---|
| 0 | Normal Speed | 0 | 0 | 44.1kHz | |
| 1 | Normal Speed | 0 | 1 | OFF | Default |
| 2 | Normal Speed | 1 | 0 | 48kHz | |
| 3 | Normal Speed | 1 | 1 | 32kHz | |
| 4 | Double Speed | 0 | 0 | OFF | |
| 5 | Double Speed | 0 | 1 | OFF | |
| 6 | Double Speed | 1 | 0 | OFF | |
| 7 | Double Speed | 1 | 1 | OFF | |

Table 6. De-emphasis control

## ■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 0.9Hz at fs=44.1kHz and also scales with sampling rate (fs).

## ■ Audio Serial Interface Format

Four serial data modes can be selected by the DIF0 and DIF1 pins (P/S = "H") or bits (P/S = "L") as shown in Table 7. In all modes the serial data is MSB-first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK and the SDTI/DAUX are latched on the rising edge of BICK.

Figures 1~4 shows the timing at SDOS = "L". In this case, the SDTO outputs the ADC output data. When SDOS = "H", the data input to DAUX is converted to SDTO's format and output from SDTO. Mode 2 and mode 3 in SDTI/DAUX input formats can be used for 16-20bit data by zeroing the unused LSBs.

| Mode | DIF1 | DIF0 | SDTO | SDTI1-3, DAUX | LRCK | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 24bit, MSB justified | 20bit, LSB justified | H/L | |
| 1 | 0 | 1 | 24bit, MSB justified | 24bit, LSB justified | H/L | |
| 2 | 1 | 0 | 24bit, MSB justified | 24bit, MSB justified | H/L | Default |
| 3 | 1 | 1 | 24bit, IIS (I2S) | 24bit, IIS (I2S) | L/H | |

Table 7. Audio data formats

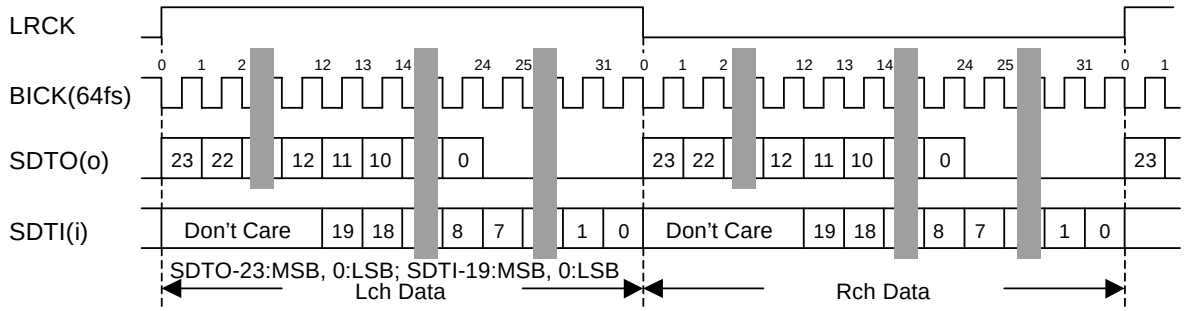



Figure 1. Mode 0 Timing

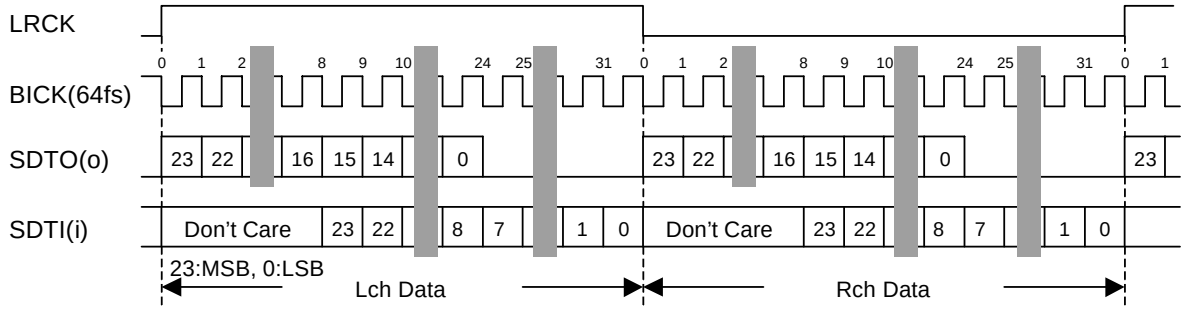



Figure 2. Mode 1 Timing

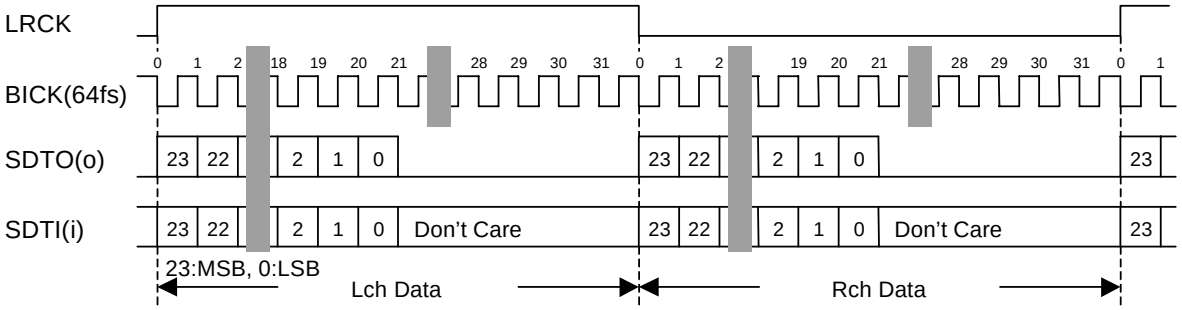



Figure 3. Mode 2 Timing

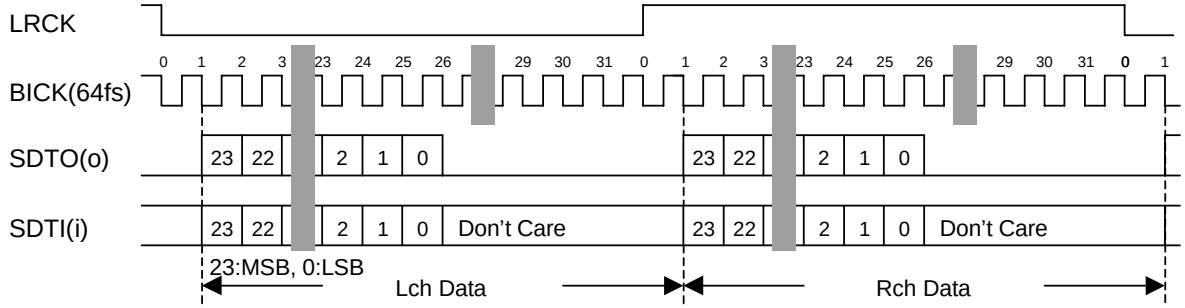



Figure 4. Mode 3 Timing

## ■ Overflow Detection

The AK4527B has overflow detect function for analog input. Overflow detection is enabled when OVFE bit is set to "1" at serial control mode. OVF pin goes to "H" if analog input of Lch or Rch overflows. OVF output for overflowed analog input has the same group delay as ADC (GD=27.6/fs=626µs@fs=44.1kHz).
OVF is "L" for 522/fs(=11.8ms@fs=44.1kHz) after PDN = "↑", and then overflow detection is enabled.

## ■ Zero detection

The AK4527B has two pins for zero detect flag outputs. Channel grouping can be selected by DZFM2-0 bits if P/S = "L" and DZFE = "L" (table 8). DZF1 pin corresponds to the group 1 channels and DZF2 pin corresponds to the group 2 channels. However DZF2 pin becomes OVF pin if OVFE bit is set to "1". Zero detection mode is set to mode 0 if DZFE= "H" regardless of P/S pin. DZF1 is AND of all six channels and DZF2 is disabled ("L") at mode 0. Table 9 shows the relation of P/S, DZFE, OVFE and DZF.

When the input data of all channels in the group 1(group 2) are continuously zeros for 8192 LRCK cycles, DZF1(DZF2) pin goes to "H". DZF1(DZF2) pin immediately goes to "L" if input data of any channels in the group 1(group 2) is not zero after going DZF1(DZF2) "H".

| Mode | DZFM | | | AOUT | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 2 | 1 | 0 | L1 | R1 | L2 | R2 | L3 | R3 |
| 0 | 0 | 0 | 0 | DZF1 | DZF1 | DZF1 | DZF1 | DZF1 | DZF1 |
| 1 | 0 | 0 | 1 | DZF1 | DZF1 | DZF1 | DZF1 | DZF1 | DZF2 |
| 2 | 0 | 1 | 0 | DZF1 | DZF1 | DZF1 | DZF1 | DZF2 | DZF2 |
| 3 | 0 | 1 | 1 | DZF1 | DZF1 | DZF1 | DZF2 | DZF2 | DZF2 |
| 4 | 1 | 0 | 0 | DZF1 | DZF1 | DZF2 | DZF2 | DZF2 | DZF2 |
| 5 | 1 | 0 | 1 | DZF1 | DZF2 | DZF2 | DZF2 | DZF2 | DZF2 |
| 6 | 1 | 1 | 0 | DZF2 | DZF2 | DZF2 | DZF2 | DZF2 | DZF2 |
| 7 | 1 | 1 | 1 | disable (DZF1=DZF2 = "L") | | | | | |

Default

Table 8. Zero detect control

| P/S pin | DZFE pin | OVFE bit | DZF mode | DZF1 pin | DZF2/OVF pin |
|---|---|---|---|---|---|
| "H" (parallel mode) | "L" | disable | Mode 7 | "L" | "L" |
| | "H" | disable | Mode 0 | AND of 6ch | "L" |
| "L" (serial mode) | "L" | "0" | Selectable | Selectable | Selectable |
| | | "1" | Selectable | Selectable | OVF output |
| | "H" | "0" | Mode 0 | AND of 6ch | "L" |
| | | "1" | Mode 0 | AND of 6ch | OVF output |

Table 9. DZF1-2 pins outputs

## ■ Digital Attenuator

AK4527B has channel-independent digital attenuator (256 levels, 0.5dB step). Attenuation level of each channel can be set by each ATT7-0 bits (table 10).

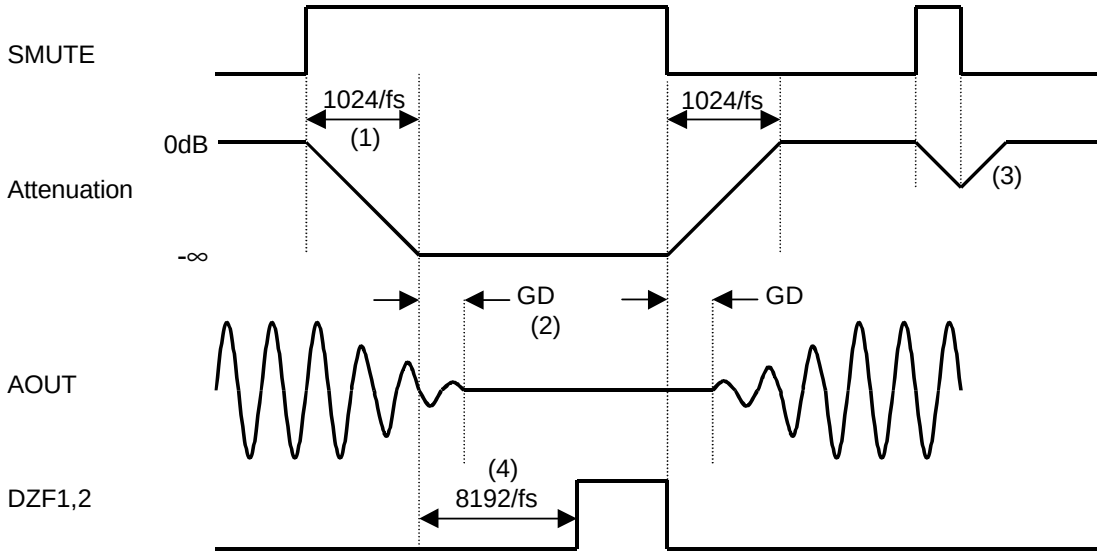
| ATT7-0 | Attenuation Level | |
|---|---|---|
| 00H | 0dB | Default |
| 01H | -0.5dB | |
| 02H | -1.0dB | |
| : | : | |
| FDH | -126.5dB | |
| FEH | -127.0dB | |
| FFH | MUTE (-∞) | |

Table 10. Attenuation level of digital attenuator

The transition between set values is soft transition of 7425 levels. It takes 7424/fs (168ms@fs=44.1kHz) from 00H(0dB) to FFH(MUTE). If PDN pin goes to “L”, the ATTs are initialized to 00H. The ATTs are 00H when RSTN = “0”. When RSTN return to “1”, the ATTs fade to their current value. Digital attenuator is independent of soft mute function.

## ■ Soft mute operation

Soft mute operation is performed at digital domain. When the SMUTE pin goes to "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When the SMUTE pin is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.




Notes:

(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output corresponding to digital input have the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.
(4) When the input data of all channels in the group are continuously zeros for 8192 LRCK cycles, DZF pin corresponding to the group goes to "H". DZF pin immediately goes to "L" if input data of any channel in the group is not zero after going DZF "H".

Figure 5. Soft mute and zero detection

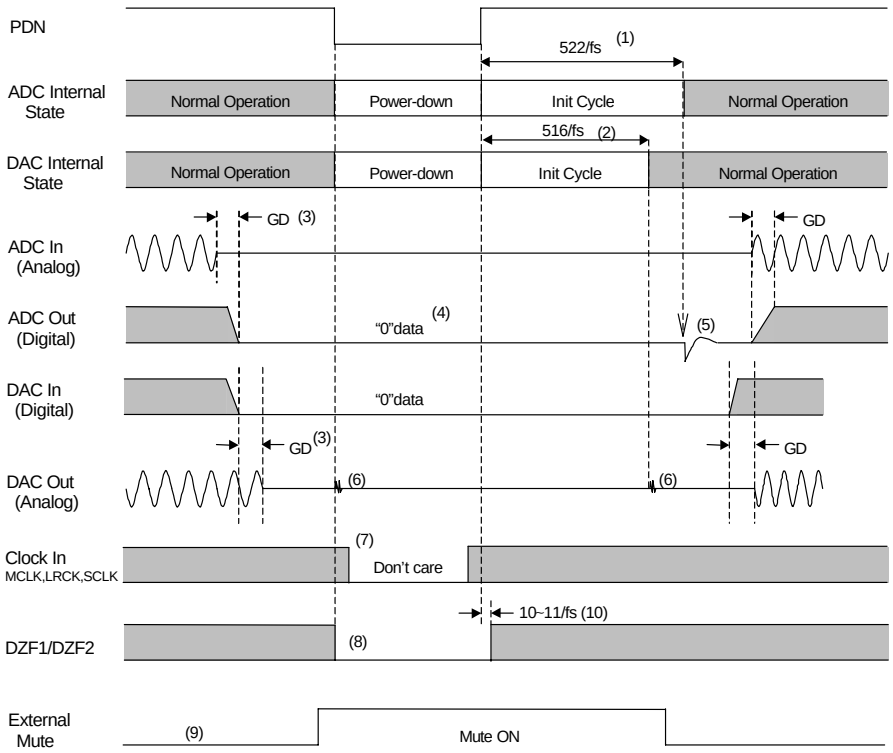
## ■ System Reset

The AK4527B should be reset once by bringing PDN = "L" upon power-up. The AK4527B is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4527B is in the power-down mode until MCLK and LRCK are input.

## ■ Power-Down

The ADC and DACs of AK4527B are placed in the power-down mode by bringing PDN "L" and both digital filters are reset at the same time. PDN "L" also reset the control registers to their default values. In the power-down mode, the analog outputs go to VCOM voltage and DZF1-2 pins go to "L". This reset should always be done after power-up. In case of the ADC, an analog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 522 cycles of LRCK clock. In case of the DAC, an analog initialization cycle starts after exiting the power-down mode. The analog outputs are VCOM voltage during the initialization. Figure 6 shows the power-up sequence.

The ADC and DACs can be powered-down individually by PWADN and PWDAN bits. In this case, the internal register values are not initialized. When PWADN = "0", SDTO goes to "L". When PWDAN = "0", the analog outputs go to VCOM voltage and DZF1-2 pins go to "H". Because some click noise occurs, the analog output should muted externally if the click noise influences system application.



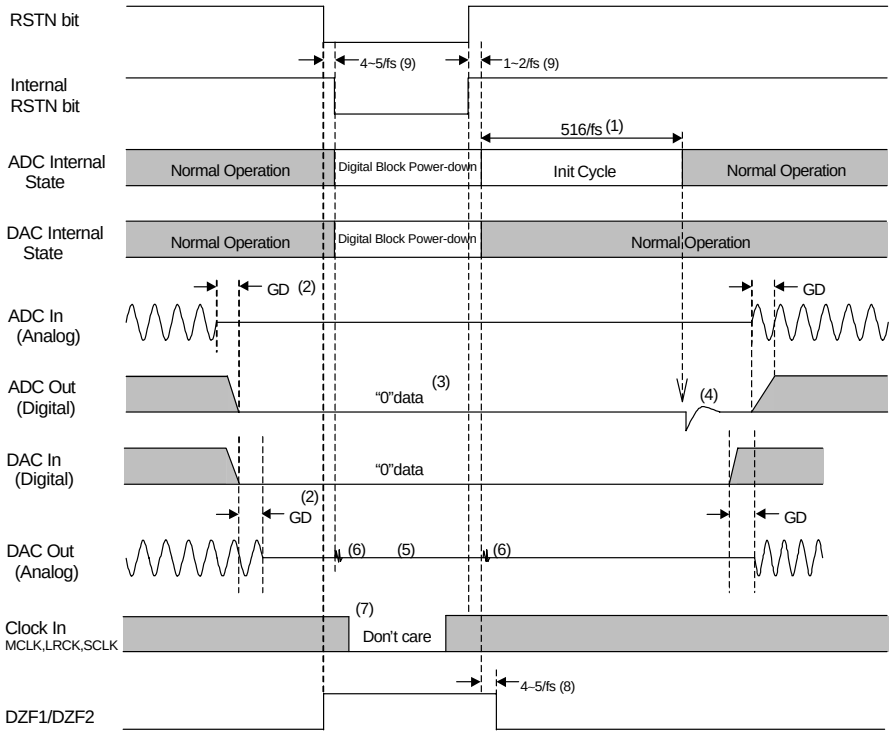

Notes:

(1) The analog part of ADC is initialized after exiting the power-down state.
(2) The analog part of DAC is initialized after exiting the power-down state.
(3) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).
(4) ADC output is "0" data at the power-down state.
(5) Click noise occurs at the end of initialization of the analog part. Please mute the digital output externally if the click noise influences system application. Required muting time depends on the configuration of the input buffer circuits.
Figure 12,13: 1s
Figure 14,15: 200ms
(6) Click noise occurs at the falling edge of PDN and at 512/fs after the rising edge of PDN.
(7) When the external clocks (MCLK, BICK and LRCK) are stopped, the AK4527B should be in the power-down mode.
(8) DZF pins are "L" in the power-down mode (PDN = "L").
(9) Please mute the analog output externally if the click noise (6) influences system application.
(10) DZF= "L" for 10~11/fs after PDN= "↑".

Figure 6. Power-down/up sequence example

## ■ Reset Function

When RSTN = "0", ADC and DACs are powered-down but the internal register are not initialized. The analog outputs go to VCOM voltage, DZF1-2 pins go to "H" and SDTO pin goes to "L". Because some click noise occurs, the analog output should muted externally if the click noise influences system application. Figure 7 shows the power-up sequence.




Notes:

(1) The analog part of ADC is initialized after exiting the reset state.

(2) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).

(3) ADC output is "0" data at the power-down state.

(4) Click noise occurs when the internal RSTN bit becomes "1". Please mute the digital output externally if the click noise influences system application. Required muting time depends on the configuration of the input buffer circuits.
Figure 12,13: 1s
Figure 14,15: 200ms

(5) The analog outputs go to VCOM voltage.

(6) Click noise occurs at 4~5/fs after RSTN bit becomes "0", and occurs at 1~2/fs after RSTN bit becomes "1". This noise is output even if "0" data is input.

(7) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode. When exiting the reset mode, "1" should be written to RSTN bit after the external clocks (MCLK, BICK and LRCK) are fed.

(8) DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 6~7/fs after RSTN bit becomes "1".

(9) There is a delay, 4~5/fs from RSTN bit "0" to the internal RSTN bit "0".

Figure 7. Reset sequence example

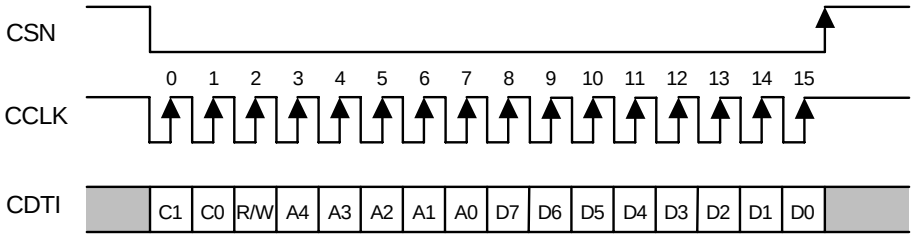
## ■ Serial Control Interface

The AK4527B can control its functions via registers. Internal registers may be written by 2 types of control mode. The chip address is determined by the state of the CAD0 and CAD1 inputs. PDN = "L" initializes the registers to their default values. Writing "0" to the RSTN bit can initialize the internal timing circuit. But in this case, the register data is not be initialized. When the state of P/S pin is changed, the AK4527B should be reset by PDN pin.

* Writing to control register is invalid when PDN = "L" or the MCLK is not fed.
* AK4527B does not support the read command.

(1) 3-wire Serial Control Mode (I2C = "L")

Internal registers may be written to the 3 wire µP interface pins (CSN,CCLK and CDTI). The data on this interface consists of Chip address (2bits, CAD0/1), Read/Write (1bit, Fixed to "1"; Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after a low-to-high transition of CSN. The clock speed of CCLK is 5MHz(max). The CSN pins should be held to "H" except for access.

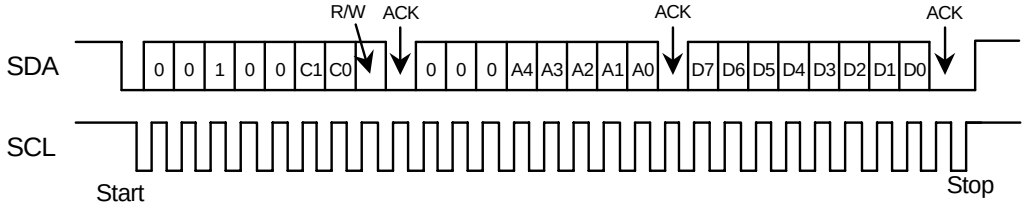



C1-C0: Chip Address (C1=CAD1, C0=CAD0)
R/W: Read/Write (Fixed to "1" : Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 8. 3-wire Serial Control I/F Timing

(2) I²C Bus Control Mode (I2C = "H")

Internal registers may be written to I²C Bus interface pins: SCL & SDA. The data on this interface consists of Chip address (2bits, CAD0/1), Read/Write (1bit, Fixed to "0"; Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of SCL and data is clocked out on the falling edge. Data can be written after a high-to-low transition of SDA when SCL is "H"(start condition), and is latched after a low-to-high transition of SDA when SCL is "H"(stop condition). The clock speed of SCL is 100kHz(max). The CSN pin should be connected to DVDD at I²C Bus control mode. The AK4527B does not have a register address auto increment capability.




C1-C0: Chip Address (C1=CAD1, C0=CAD0)
R/W: Read/Write (Fixed to "0" : Write only)
A4-A0: Register Address
D7-D0: Control Data
ACK: Acknowledge

Figure 9. I²C-bus Control I/F Timing

## ■ Mapping of Program Registers

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | 0 | 0 | 0 | 0 | DIF1 | DIF0 | 0 | SMUTE |
| 01H | Control 2 | 0 | 0 | LOOP1 | LOOP0 | SDOS | DFS | ACKS | 0 |
| 02H | LOUT1 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 03H | ROUT1 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 04H | LOUT2 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 05H | ROUT2 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 06H | LOUT3 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 07H | ROUT3 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 08H | De-emphasis | 0 | 0 | DEMA1 | DEMA0 | DEMB1 | DEMB0 | DEMC1 | DEMC0 |
| 09H | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RSTN |
| 0AH | Zero detect | OVFE | 0 | DZFM2 | DZFM1 | DZFM0 | PWVRN | PWADN | PWDAN |

Note: For addresses from 0BH to 1FH, data is not written.
When PDN goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the internal timing is reset and DZF1-2 pins go to “H”, but registers are not initialized to their default values.
SMUTE, DFS, SDOS and LOOP1 are ORed with pins.

## ■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | 0 | 0 | 0 | 0 | DIF1 | DIF0 | 0 | SMUTE |
| default | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

SMUTE: Soft Mute Enable
0: Normal operation
1: All DAC outputs soft-muted
Register bit of SMUTE is ORed with the SMUTE pin if P/S = "L".

DIF1-0: Audio Data Interface Modes (see table 7.)
Initial: "10", mode 2

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | Control 2 | 0 | 0 | LOOP1 | LOOP0 | SDOS | DFS | ACKS | 0 |
| default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the setting of DFS are ignored. When this bit is "0", DFS sets the sampling speed mode.

DFS: Sampling speed mode (see table 1.)
0: Normal speed
1: Double speed
Register bit of DFS is ORed with DFS pin if P/S = "L". The setting of DFS are ignored at ACKS bit "1".

SDOS: SDTO source select
0: ADC
1: DAUX
Register bit of SDOS is ORed with SDOS pin if P/S = "L".

LOOP1-0: Loopback mode enable
00: Normal (No loop back)
01: LIN → LOUT1, LOUT2, LOUT3
RIN → ROUT1, ROUT2, ROUT3
The digital ADC output (DAUX input if SDOS = "1") is connected to the digital DAC input. In this mode, the input DAC data to SDTI1-3 is ignored. The audio format of SDTO at loopback mode becomes mode 2 at mode 0, and mode 3 at mode 1, respectively.
10: SDTI1(L) → SDTI2(L), SDTI3(L)
SDTI1(R) → SDTI2(R), SDTI3(R)
In this mode the input DAC data to SDTI2-3 is ignored.
11: N/A
Register bit of LOOP1 is ORed with LOOP1 pin if P/S = "L".

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02H | LOUT1 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 03H | ROUT1 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 04H | LOUT2 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 05H | ROUT2 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 06H | LOUT3 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 07H | ROUT3 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ATT7-0: Attenuation Level (see table 9.)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 08H | De-emphasis | 0 | 0 | DEMA1 | DEMA0 | DEMB1 | DEMB0 | DEMC1 | DEMC0 |
| Default | | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

DEMA1-0: De-emphasis response control for DAC1 data on SDTI1 (see table 6.)
Initial: “01”, OFF

DEMB1-0: De-emphasis response control for DAC2 data on SDTI2 (see table 6.)
Initial: “01”, OFF

DEMC1-0: De-emphasis response control for DAC3 data on SDTI3 (see table 6.)
Initial: “01”, OFF

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 09H | Clock mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RSTN |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

RSTN: Internal timing reset
0: Reset. DZF1-2 pins go to “H”, but registers are not initialized.
1: Normal operation

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0AH | Zero detect | OVFE | 0 | DZFM2 | DZFM1 | DZFM0 | PWVRN | PWADN | PWDAN |
| Default | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

PWDAN: Power-down control of DAC1-3
0: Power-down
1: Normal operation

PWADN: Power-down control of ADC
0: Power-down
1: Normal operation

PWVRN: Power-down control of reference voltage
0: Power-down
1: Normal operation

DZFM2-0: Zero detect mode select (see table 8.)
Initial: “111”, disable

OVFE: Overflow detection enable
0: Disable, pin#33 becomes DZF2 pin.
1: Enable, pin#33 becomes OVF pin.

## SYSTEM DESIGN

Figure 10 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

Condition: TVDD=5V, 3-wire serial control mode, CAD1-0 = "00", Full-differential input

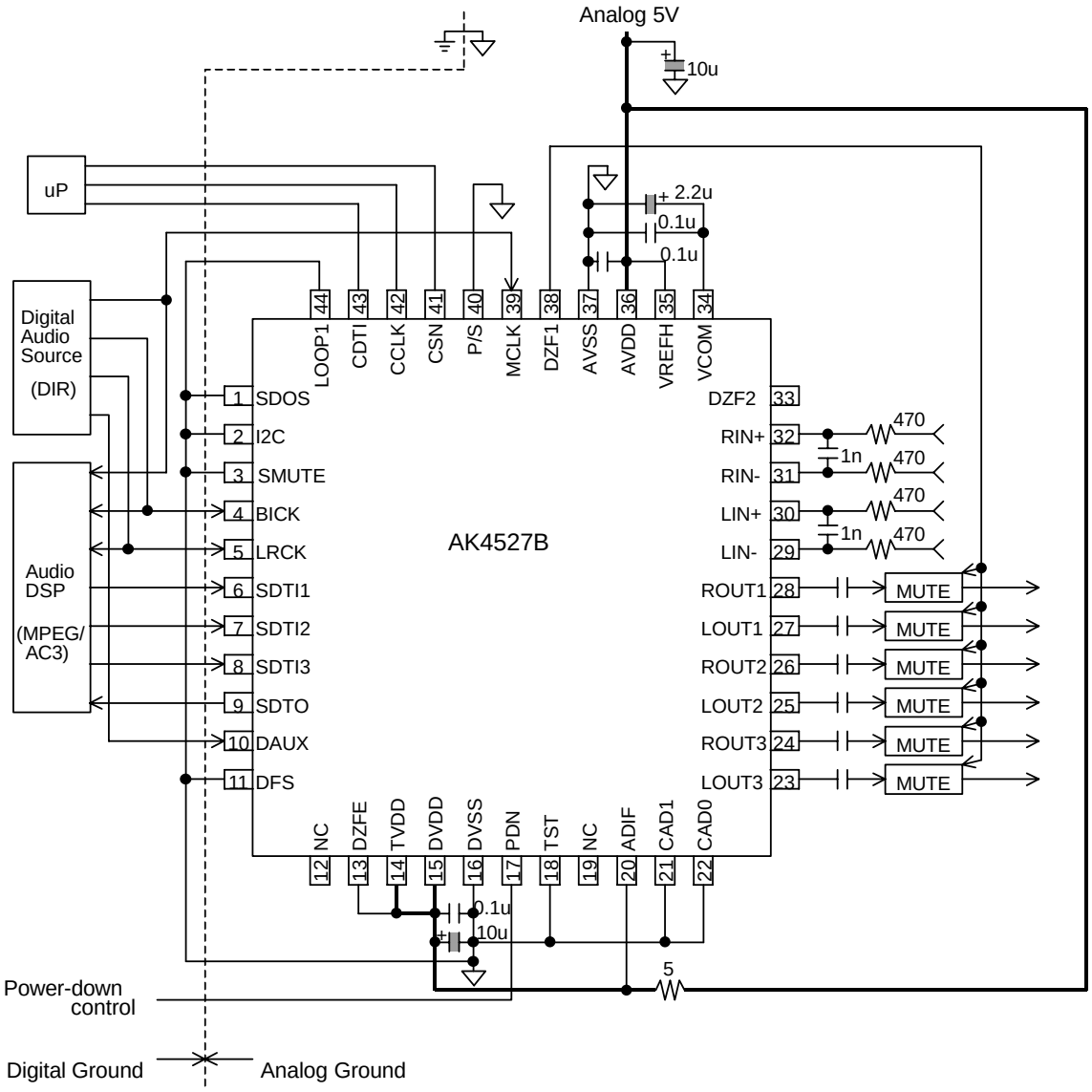



Figure 10. Typical Connection Diagram

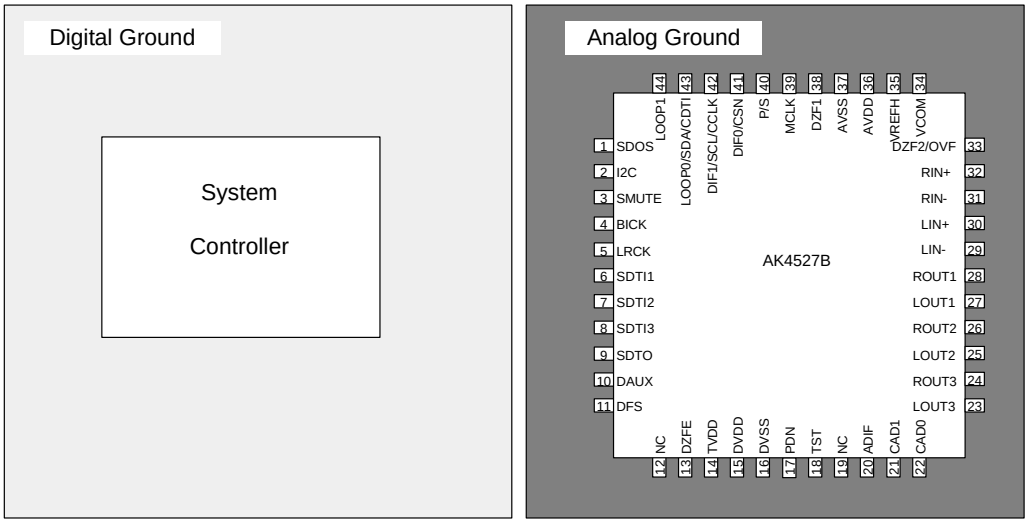



Figure 11. Ground Layout

Note: AVSS and DVSS must be connected to the same analog ground plane.

### 1. Grounding and Power Supply Decoupling

The AK4527B requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from analog supply in system. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS and DVSS of the AK4527B must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4527B as possible, with the small value ceramic capacitor being the nearest.

### 2. Voltage Reference Inputs

The voltage of VREFH sets the analog input/output range. VREFH pin is normally connected to AVDD with a 0.1µF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 2.2µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH and VCOM pins in order to avoid unwanted coupling into the AK4527B.

### 3. Analog Inputs

The ADC inputs are differential. Figures 12 and 13 are circuit examples which analog signal is input by single end (ADIF= “L”). The signal can be input from either positive or negative input and the input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. In case of single ended input, the distortion around full scale degrades compared with differential input (ADIF= “H”). Figures 14 and 15 are circuit examples which analog signal is input to both positive and negative input and the input signal range scales with the supply voltage and nominally 0.3 x VREFH Vpp. The AK4527B can accept input voltages from AVSS to AVDD. The ADC output data format is 2’s complement. The output code is 7FFFFFH(@24bit) for input above a positive full scale and 800000H(@24bit) for input below a negative fill scale. The ideal code is 000000H(@24bit) with no input signal. The DC offset is removed by the internal HPF.

The AK4527B samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. A simple RC filter (fc=150kHz) may be used to attenuate any noise around 64fs and most audio signals do not have significant energy at 64fs.

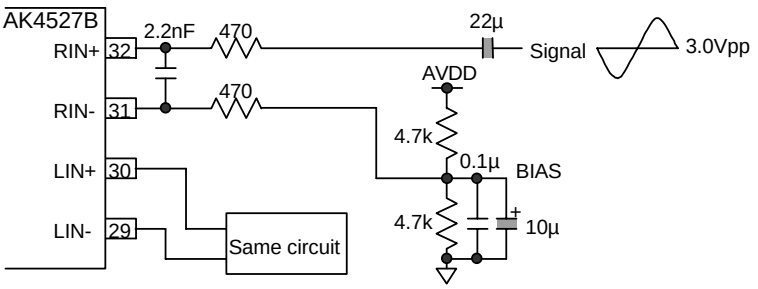



Figure 12. Single End Input Example (ADIF= "L"; Not using op-amp)

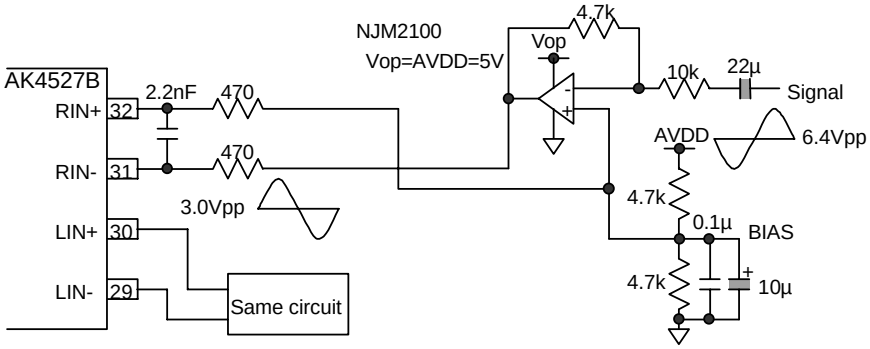



Figure 13. Single End Input Example (ADIF= "L"; Using op-amp)

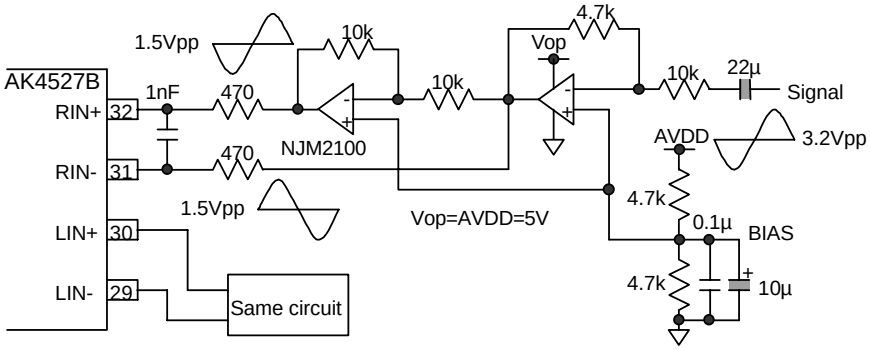



Figure 14. Differential Input Buffer Example (ADIF= "H"; Using op-amp with single power supply)

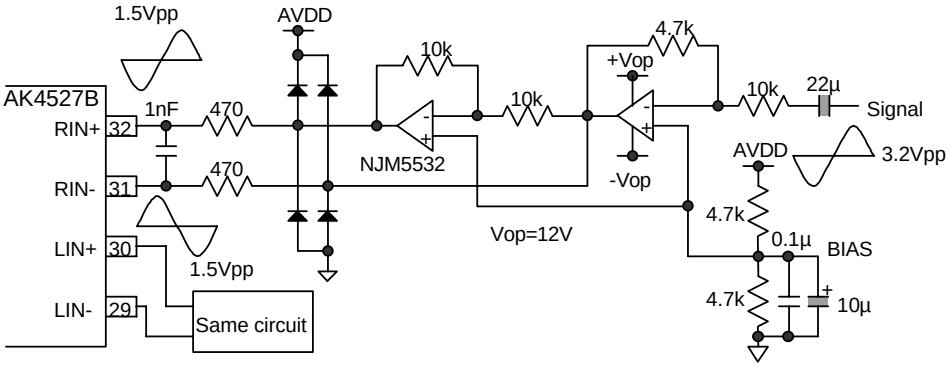



Figure 15. Differential Input Buffer Example (ADIF= "H"; Using op-amp with dual power supply)

### 4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

## ■ Peripheral I/F Example

The AK4527B can accept the signal of device with a nominal 3.3V supply because of TTL input. The power supply for output buffer (TVDD) of the AK4527B should be 3.3V when the peripheral devices operate at a nominal 3.3V supply. Figure 16 shows an example with the mixed system of 3.3V and 5V.

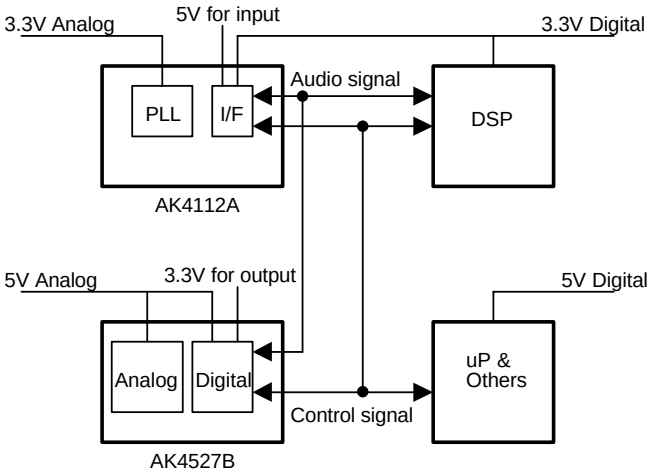



Figure 16. Power supply connection example

## ■ Applications

1) Zoran AC3 decoder, ZR38650

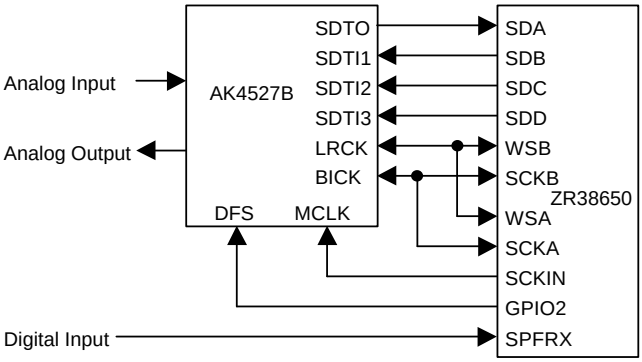



Figure 17. Application circuit example (ZR38650)

2) Yamaha AC3 decoder, YSS912

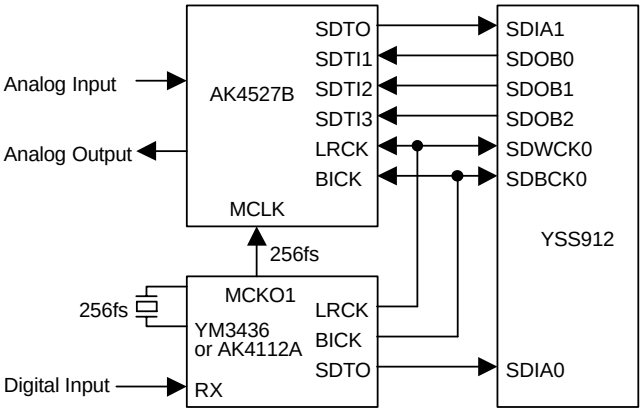



Figure 18. Application circuit example (YSS912)

3) Motorola AC3 decoder, DSP56362

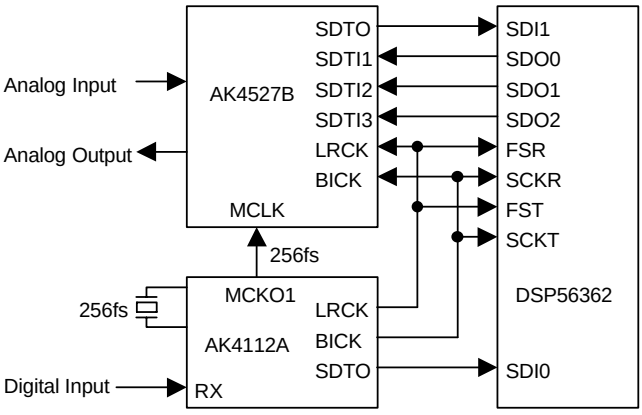
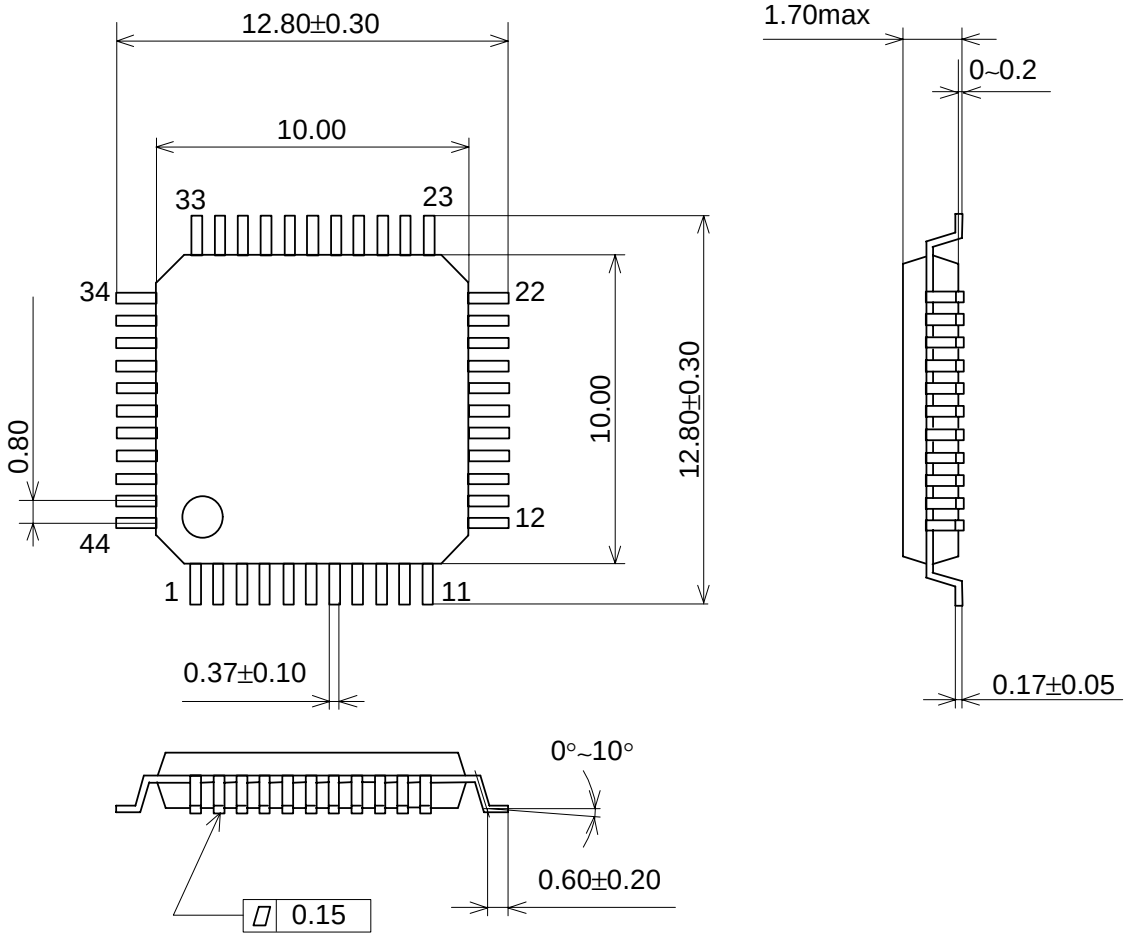



Figure 19. Application circuit example (DSP56362)

## PACKAGE

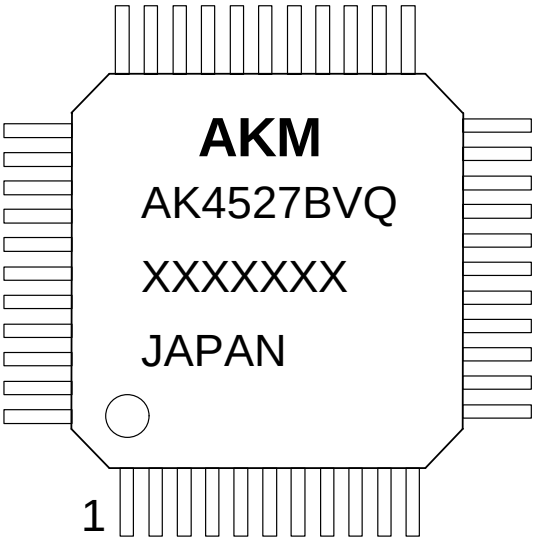
44pin LQFP (Unit: mm)




■ **Package & Lead frame material**

| | |
|---|---|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder plate |

## MARKING




1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4527BVQ
4) Country of Origin
5) Asahi Kasei Logo

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# AK5383

## 24-Bit, 96kHz Analog-to-Digital Converter

## Features

- Proprietary dual-bit delta-sigma (ΔΣ) architecture
- Sampling rate from 1kHz to 108kHz
- Full differential inputs
- Dynamic range = 110dB
- Signal-to-noise = 110dB
- Signal-to-(Noise + Distortion) = 103dB
- On-chip linear phase digital anti-alias filter
  - Passband from 0 to 21.768kHz at fs = 48kHz
  - Ripple = 0.001dB
  - Stopband attenuation = 110dB
- Selectable digital HPF or offset calibration
- Power supplies
  - Analog: 5V ± 5%
  - Digital: from 3V to 5.25V
- Low power dissipation: 210mW
- Small 28-pin SOP package
- Pin compatible with the AK5391, AK5392, and AK5393

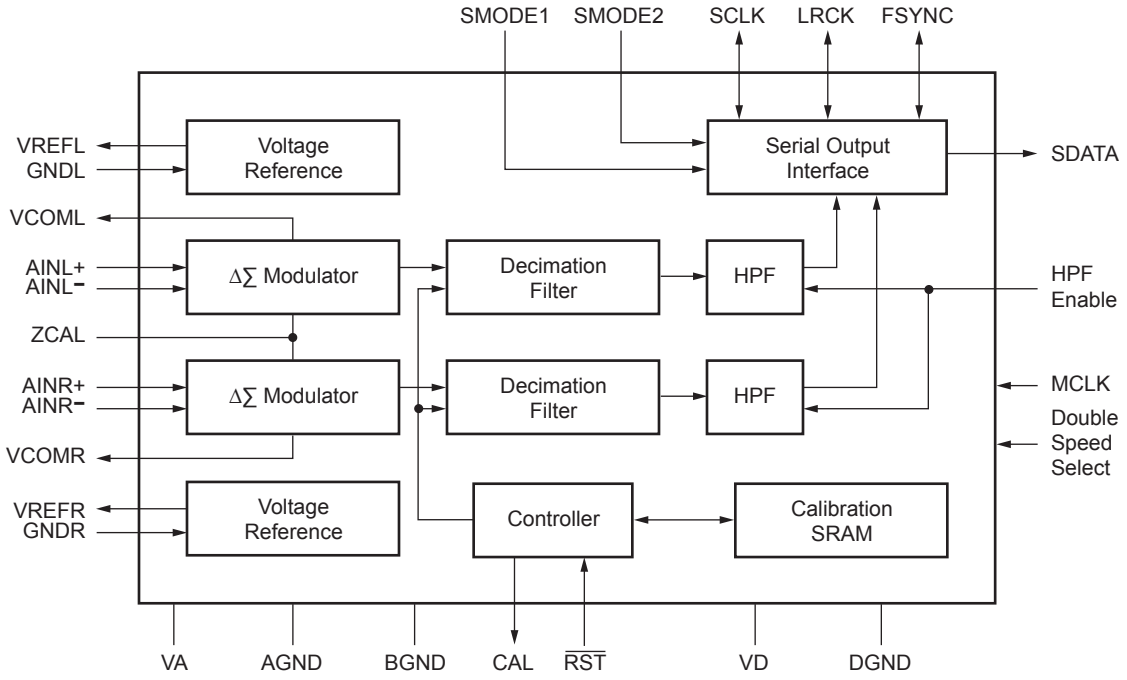
## Description

The AK5383 is a 24-bit, 96kHz stereo Analog-to-Digital Converter (ADC) that offers up to 110dB of dynamic range and a 103dB Signal-to-(Noise + Distortion) Ratio. The improved dynamic range and lowered distortion are achieved using an innovative dual-bit ΣΔ architecture that reduces power consumption and improves reliability.

The AK5383 include full differential inputs for maximum signal range and performance. It also includes a reference filter and a digital decimation filter to minimize application requirements for anti-aliasing filtering. The user can select an internal HPF to eliminate DC inputs or offset calibration. The AK5383 outputs data at up to 108kHz, in several selectable formats.

The AK5383 is available in a space-saving 28-pin SOP package, and it operates over the full commercial temperature range: –10˚C to 70˚C.

## Block Diagram






ASAHI KASEI MICROSYSTEMS CO., LTD.

# Performance Specifications

**Analog Characteristics**

Ta = 25°C, VA = 5.0V, VD = 3.3V, AGND= SGND = DGND = 0V, fs = 48kHz, Signal Frequency = 1kHz, 24-bit output, and measurement frequency = 10Hz to 20kHz, unless otherwise specified.

| Parameter | Conditions/Comments | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Resolution | | | | 24 | Bits |
| **Analog Input Characteristics** | | | | | |
| Dynamic Range | -60dBFS, A-Weighted | 105 | 110 | | dB |
| Signal-to-Noise Ratio | A-Weighted | 105 | 110 | | dB |
| Signal-to-(Noise + Distortion) Ratio | -1dBFS | 96 | 103 | | dB |
| | -20dBFS | | 87 | | |
| | -60dBFS | | 47 | | |
| | -1dBFS, fs = 96kHz[1] | 93 | 100 | | |
| | -20dBFS, fs = 96kHz[1] | | 81 | | |
| | -60dBFS, fs = 96kHz[1] | | 41 | | |
| Interchannel Isolation | | 110 | 120 | | dB |
| Interchannel Gain Mismatch | | | 0.1 | 0.5 | dB |
| Gain Drift | | | | 150 | ppm/°C |
| Offset Error After Calibration | HPF = Off | | ±200 | ±1000 | LSB[2] |
| | HPF = On | | ±1 | | |
| Offset Drift | HPF = Off | | ±10 | | LSB/°C |
| Offset Calibration Range | HPF = Off | | ±50 | | mV |
| Input Voltage | (AIN+) - (AIN-) | ±2.3 | ±2.45 | ±2.6 | V |
| Input Impedance | | 8 | 14 | | kΩ |
| **Power Supplies** | | | | | |
| Analog Power Supply Current | | | 38 | 54 | mA |
| Digital Power Supply Current | | | 6 | 9 | mA |
| | fs = 96kHz | | 9 | 14 | |
| Power Dissipation | | | 210 | 300 | mW |
| Power Supply Rejection[3] | | | 70 | | dB |

**Digital Characteristics**

Ta = 25°C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V

| Parameter | Conditions/Comments | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Input** | | | | | |
| High-Level Input Voltage | | 0.7VD | | | V |
| Low-Level Input Voltage | | | | 0.3VD | V |
| Input Leakage Current | | | | ±10 | µA |
| **Output** | | | | | |
| High-Level Output Voltage | Iout = -20µA | VD - 0.1 | | | V |
| Low-Level Output Voltage | Iout = 20µA | | | 0.1 | V |

# Performance Specification (Continued)

**Filter Characteristics—fs = 48kHz**

**fs = 48kHz,** Ta = 25˚C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V, DFS = Low.

| Parameter | | Conditions/Comments | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ADC Digital Filter (Decimation LPF) | | | | | | |
| PB | Passband[4] | | 0 | | 21.768 | kHz |
| SB | Stopband[4] | | 26.232 | | | kHz |
| PR | Passband Ripple | | | | ±0.001 | dB |
| SA | Stopband Attenuation[5] | | 110 | | | dB |
| GD | Group Delay[6] | | | 38.7 | | 1/fs |
| ΔGD | Group Delay Distortion | | | 0 | | μs |
| **ADC Digital Filter (HPF)** | | | | | | |
| FR | Frequency Response[4] | -3dB | | 1.0 | | Hz |
| | | -0.5dB | | 2.9 | | |
| | | -0.1dB | | 6.5 | | |

**Filter Characteristics—fs = 96kHz**

**fs = 96kHz,** Ta = 25˚C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V, DFS = High.

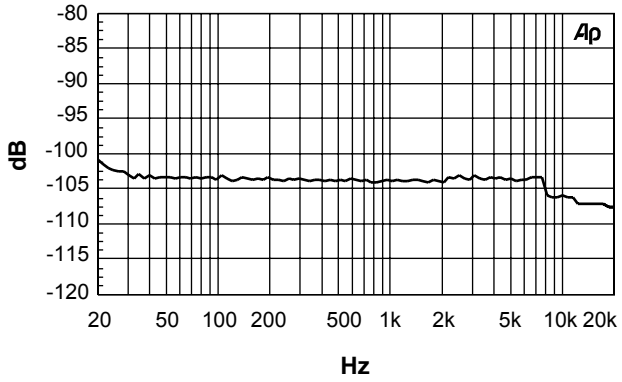
| Parameter | | Conditions/Comments | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ADC Digital Filter (Decimation LPF) | | | | | | |
| PB | Passband[4] | | 0 | | 43.536 | kHz |
| SB | Stopband[4] | | 52.464 | | | kHz |
| PR | Passband Ripple | | | | ±0.003 | dB |
| SA | Stopband Attenuation[7] | | 110 | | | dB |
| GD | Group Delay[6] | | | 38.8 | | 1/fs |
| ΔGD | Group Delay Distortion | | | 0 | | μs |
| **ADC Digital Filter (HPF)** | | | | | | |
| FR | Frequency Response[4] | -3dB | | 2.0 | | Hz |
| | | -0.1dB | | 13.0 | | |

**Notes:**

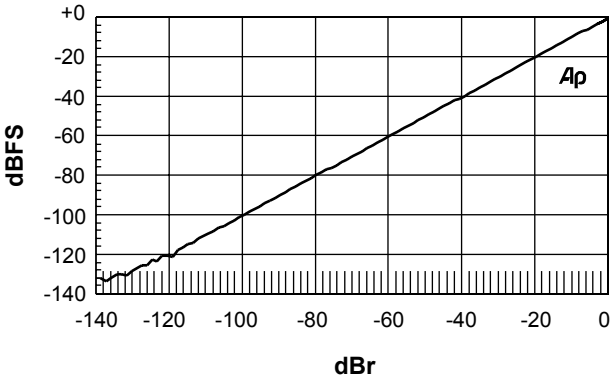
1. When fs = 96kHz, a measurement bandwidth of 40kHz is used.
2. LSB refers to the Least Significant Bit of the 24-bit output data.
3. The Power Supply Rejection ratio is measured with a 1kHz, 20m$V_{P-P}$ input to VA and VD. VREFH is held at a constant voltage.
4. The passband and stopband frequencies are proportional to fs.
5. The analog modulator samples the input at 6.144MHz for 48kHz output. There is no rejection of input signals which are multiples of the sampling frequency. That is, there is no rejection for signals of the following frequencies:
   n x 6.144MHz ± 21.768kHz, where n = 1, 2, 3, 4, ...
6. The Group Delay is the calculated delay time which takes place due to the digital filtering process. This time is taken from when the analog signal is input, to the time of setting the 24-bit data (from both channels) to the output register. When the HPF is on, this time is typically 40.7/fs if the DFS pin is Low, and 40.8/fs if the DFS pin is High.
7. The analog modulator samples the input at 6.144MHz for 96kHz output. There is no rejection of input signals which are multiples of the sampling frequency. That is, there is no rejection for signals of the following frequencies:
   n x 6.144MHz ± 43.536kHz, where n = 1, 2, 3, 4, ...

# Typical Performance Curves

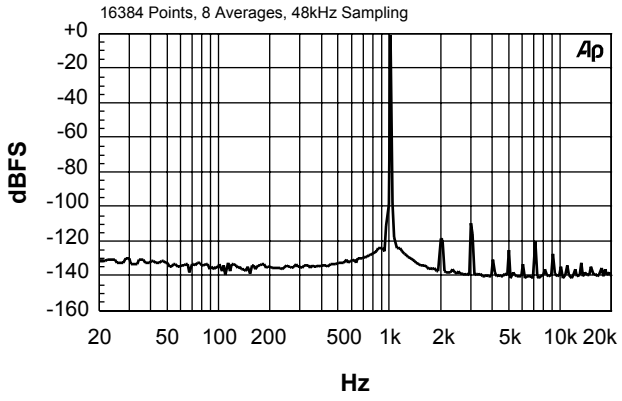
**THD + N vs. Frequency**



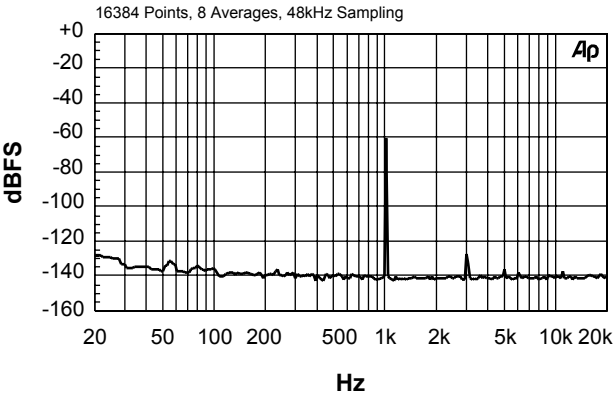

**Linearity**




**0dB FFT**




**-60dB FFT**



# Absolute Maximum Ratings

AGND, SGND, and DGND = 0V. All voltages are with respect to ground.

| Parameter | | Min. | Max. | Units |
|---|---|---|---|---|
| **Power Supplies** | | | | |
| VA | Analog Power Supply | -0.3 | 6.0 | V |
| VD | Digital Power Supply | -0.3 | 6.0 | V |
| ΔGND[1] | \|SGND - DGND\| | | 0.3 | V |
| IIN | Input Current—All pins except supply pins | | ±10 | mA |
| VINA | Analog Input Voltage | -0.3 | VA + 0.3 | V |
| VIND | Digital Input Voltage | -0.3 | VD + 0.3 | V |
| Temperature | | | | |
| Ta | Ambient Operating Temperature (Power Applied) | -10 | 70 | °C |
| Tstg | Storage Temperature | -65 | 150 | °C |

**Note:**

1. AGND and SGND must be at the same voltage.

**Caution:**
Exceeding minimum and maximum ratings may result in damage to the device.

# Recommended Operating Conditions

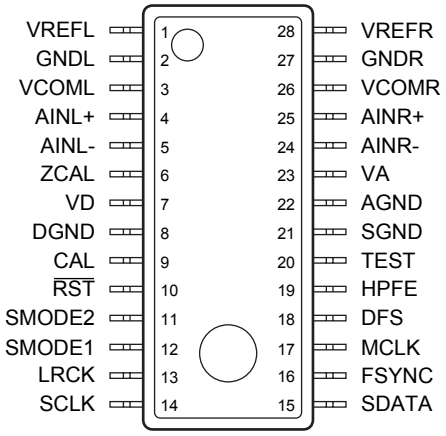
AGND, SGND, and DGND = 0V. All voltages are with respect to ground.

| Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Power Supplies[1]** | | | | | |
| VA | Analog Power Supply | 4.75 | 5.0 | 5.25 | V |
| VD | Digital Power Supply | 3.0 | 3.3 | 5.25 | V |

**Note:**

1. The VA and VD power-up sequences are not critical.

# Pin Descriptions




**Note:**
See Table 1 for compatibility with other AKM devices.

# Pin Descriptions

| No. | Pin Name | I/O | Pin Function and Description |
|---|---|---|---|
| 1 | VREFL | O | **Left Channel Reference Voltage.** VREFL = 3.75V. This pin is normally connected to the GNDL pin through a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor in parallel. Refer to the Design Considerations section for additional information. |
| 2 | GNDL | - | **Left Channel Reference Ground.** GNDL = 0V. |
| 3 | VCOML | O | **Left Common Voltage.** VCOML = 2.75V. |
| 4 | AINL+ | I | **Left Channel Analog Positive Input.** |
| 5 | AINL- | I | **Left Channel Analog Negative Input.** |
| 6 | ZCAL | I | **Zero Calibration Control.** This pin controls the calibration reference signal. When ZCAL is Low, the VCOML and VCOMR are selected. When High, the analog inputs (AINL+, AINL-, AINR+, and AINR-) are used for the reference level. |
| 7 | VD | - | **Digital Power Supply.** VD = 3.3V. |
| 8 | DGND | - | **Digital Ground.** DGND = 0V. |
| 9 | CAL | O | **Calibration Active Signal.** When this pin outputs a High signal, it shows that the offset calibration cycle is in progress. The offset calibration cycle starts when the RST pin goes High. The CAL pin goes Low after 8704 clock cycles when DFS is Low or after 17408 cycles when DFS is High. |
| 10 | $\overline{\text{RST}}$ | I | **Reset.** When this pin is Low, the digital section is powered down. When this pin returns to High, an offset calibration cycle starts. An offset calibration cycle should always be initiated upon powering up the device. |
| 11 | SMODE2 | I | **Serial Interface Mode Select.** The serial interface mode data should always be MSB first, 2's complement formatted. See Table 3 for these pin definitions. |
| 12 | SMODE1 | I | |
| 13 | LRCK | I/O | **Left Channel and Right Channel Select Clock.** During reset—when the SMODE1 pin is High—the LRCK pin goes High when the SMODE2 pin is Low, and the LRCK pin goes Low when the SMODE2 pin is High. |
| 14 | SCLK | I/O | **Serial Data Clock.** Data is clocked on the falling edge of SCLK. In the slave mode, the SCLK pin requires a clock greater than 48fs. In the master mode, this pin outputs a 128fs (when DFS is Low) clock or a 64fs clock. SCLK is Low during reset. |
| 15 | SDATA | O | **Serial Data Output.** Serial data output is MSB first and 2's complement formatted. This pin is low during reset. |
| 16 | FSYNC | I/O | **Frame Synchronization Signal.** In slave mode, when FSYNC is High, the data bits are clocked on SDATA. In the master mode, FSYNC outputs a 2fs clock and it is Low during reset. |

## Pin Descriptions (Continued)

| No. | Pin Name | I/O | Pin Function and Description |
|---|---|---|---|
| 17 | MCLK | I | **Master Clock Input.** Set the DFS pin Low for a 256fs input clock. Set the DFS pin High for a 128fs clock. |
| 18 | DFS | I | **Double Speed Sampling Mode.** When this pin is Low, the chip is in normal speed mode. When High, the double speed mode is selected. |
| 19 | HPFE | I | **High Pass Filter Enable.** When this pin is High, the high pass filter is enabled. When Low, this pin is disabled. |
| 20 | TEST | I | **Test.** This pin should be connected to ground. |
| 21 | SGND | - | **Substrate Ground.** SGND = 0V. |
| 22 | AGND | - | **Analog Ground.** AGND = 0V. |
| 23 | VA | - | **Analog Power Supply.** VA = 5V. |
| 24 | AINR- | I | **Right Channel Analog Negative Input.** |
| 25 | AINR+ | I | **Right Channel Analog Positive Input.** |
| 26 | VCOMR | O | **Right Common Voltage Pin.** VCOMR = 2.75V. |
| 27 | GNDR | - | **Right Channel Reference Ground**. GNDR = 0V. |
| 28 | VREFR | O | **Right Channel Reference Voltage.** VREFR = 3.75V. This pin is normally connected to the GNDR pin through a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor in parallel. Refer to the Design Considerations section for additional information. |

**Note:**

1. All input pins, except pull-down pins, should not be left floating.

**Table 1. AK5383 Compatibility**

| | AK5383 | AK5393 | AK5392 | AK5391 |
|---|---|---|---|---|
| Pin 2 | GNDL | GNDL | GNDL | VREFL- |
| Pin 18 | DFS | DFS | CMODE | CMODE |
| Pin 19 | HPFE | HPFE | HPFE | SEL24 |
| Pin 27 | GNDR | GNDR | GNDR | VREFR- |
| Maximum fs | 108kHz | 108kHz | 54kHz | 54kHz |
| Master Clock at 48kHz | 256fs | 256fs | 256fs or 384fs | 256fs or 384fs |
| Master Clock at 96kHz | 128fs | 128fs | N/A | N/A |
| Dynamic Range | 110dB | 117dB | 116dB | 113dB |
| Signal-to-Noise Ratio | 110dB | 117dB | 116dB | 113dB |
| Signal-to-(Noise + Distortion) | 103dB | 105dB | 105dB | 97dB |

# Swithching Characteristics

Ta = 25˚C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V, $C_L$ = 20pF.

| Parameter | | Conditions/Comments | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Control Clock Frequency | | | | | | |
| fCLK | Master Clock Frequency | 256fs | 0.256 | 12.288 | 13.824 | MHz |
| tCLKL | Clock Pulse Width Low | | 29 | | | ns |
| tCLKH | Clock Pulse Width High | | 29 | | | ns |
| fSLK | Serial Data Output Clock (SCLK) Frequency | | | 6.144 | 6.912 | MHz |
| fs | Channel Select Clock (LRCK) Frequency | | 1 | 48 | 108 | kHz |
| Duty Cycle | | | 25 | | 75 | % |
| **Serial Interface Timing—Slave Mode**[1] (SMODE = Low) | | | | | | |
| tSLK | SCLK Period | | 144.7 | | | ns |
| tSLKL | SCLK Pulse Width Low | | 65 | | | ns |
| tSLKH | SCLK Pulse Width High | | 65 | | | ns |
| tSLR | SCLK Falling Edge to LRCK Edge | Note 2 | -45 | | 45 | ns |
| tDLR | LRCK Edge to SDATA MSB Valid | | | | 45 | ns |
| tDSS | SCLK Falling Edge to SDATA Valid | | | | 45 | ns |
| tSF | SCLK Falling Edge to FSYNC Edge | | -45 | | 45 | ns |
| **Serial Interface Timing—Master Mode** (SMODE = High) | | | | | | |
| tSCLK | SCLK Frequency | DFS = Low | | 128fs | | Hz |
| | | DFS = High | | 64fs | | |
| SCLK Frequency Duty Cycle | | | | 50 | | % |
| fFSYNC | FSYNC Frequency | | | 2fs | | Hz |
| FSYNC Frequency Duty Cycle | | | | 50 | | % |
| tSLR | SCLK Falling Edge to LRCK Edge | | -20 | | 20 | ns |
| tLRF | LRCK Edge to FSYNC Rising Edge | | | 1 | | tSLK |
| tDSS | SCLK Falling Edge to SDATA Valid | | | | 45 | ns |
| tSF | SCLK Falling Edge to FSYNC Edge | | -20 | | 20 | ns |
| Reset and Calibration Timing | | | | | | |
| tRTW | $\overline{\text{RST}}$ Pulse Width | | 150 | | | ns |
| tRCR | $\overline{\text{RST}}$ Falling to CAL Rising Edge | | | | 50 | ns |
| tRCF | $\overline{\text{RST}}$ Rising to CAL Falling Edge | Note 3 | | 8704 | | 1/fs |
| tRTV | $\overline{\text{RST}}$ Rising Edge to SDATA Valid | Note 3 | | 8960 | | 1/fs |

**Notes:**

1. Refer to the Serial Data Interface section.
2. The specified LRCK edges do not coincide with the rising edges of SCLK.
3. tRCF and tRTV specify the number of LRCK rising edges after $\overline{\text{RST}}$ is brought High. This value is given for when the device is operated in master mode. In slave mode, this value is one LRCK clock (1/fs) longer. When the DFS is High, the number of cycles, 1/fs, is doubled.

# Timing Diagrams

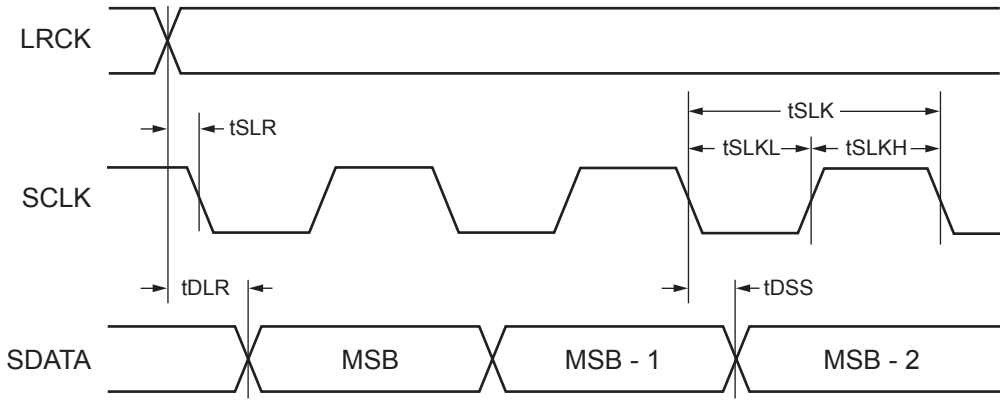



**Figure 1. Serial Data Timing (Slave Mode, FSYNC = High)**

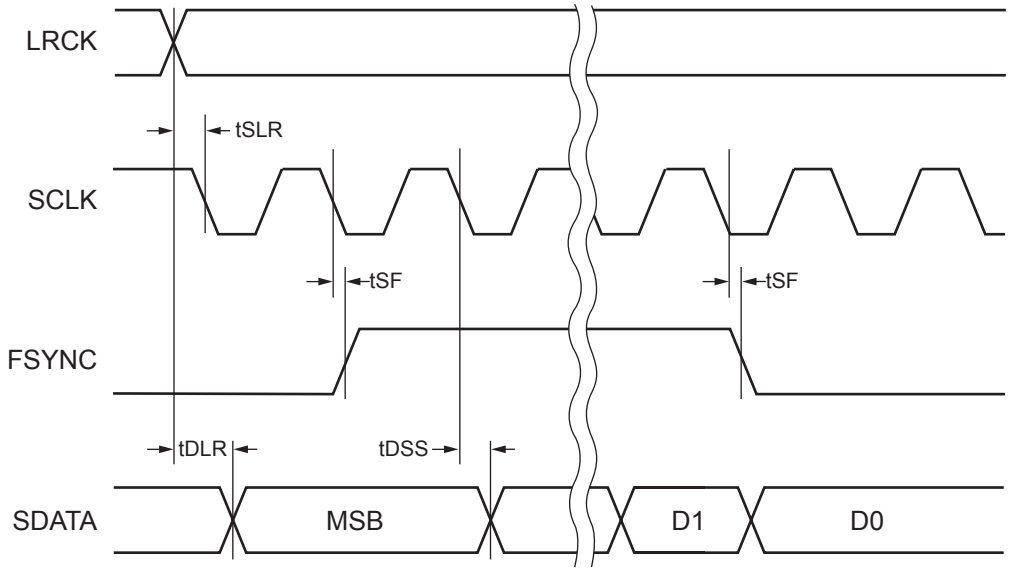



**Figure 2. Serial Data Timing (Slave Mode)**

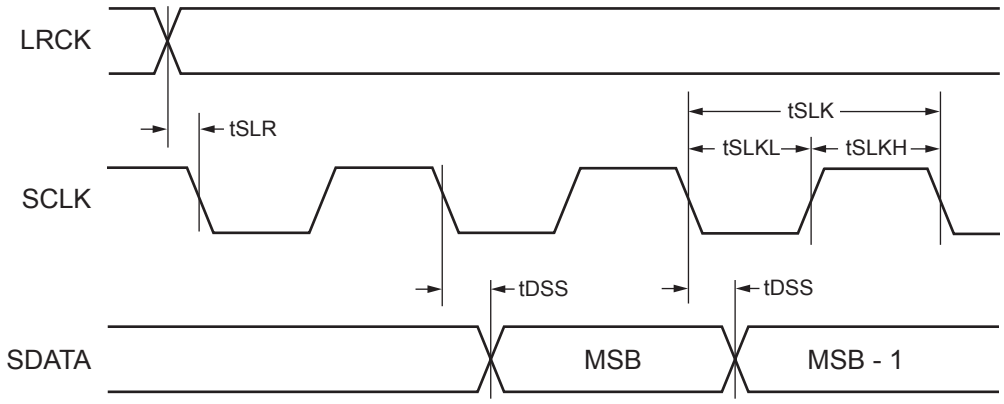



**Figure 3. Serial Data Timing ($I^2S$ Slave Mode, FSYNC = Don't Care)**

## Timing Diagrams (Continued)

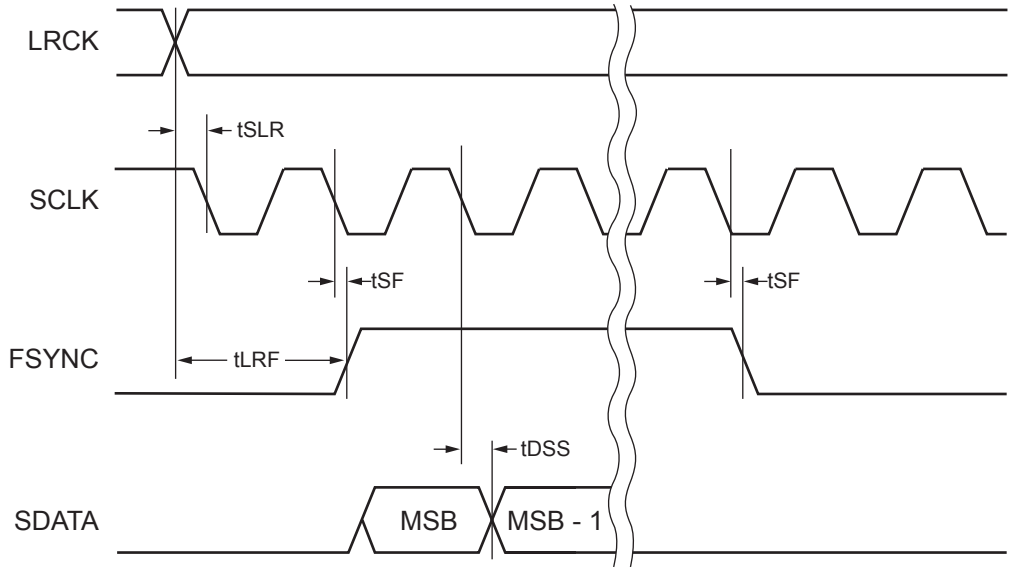



**Figure 4. Serial Data Timing (Master Mode and $I^2S$ Master Mode, DFS = Low)**

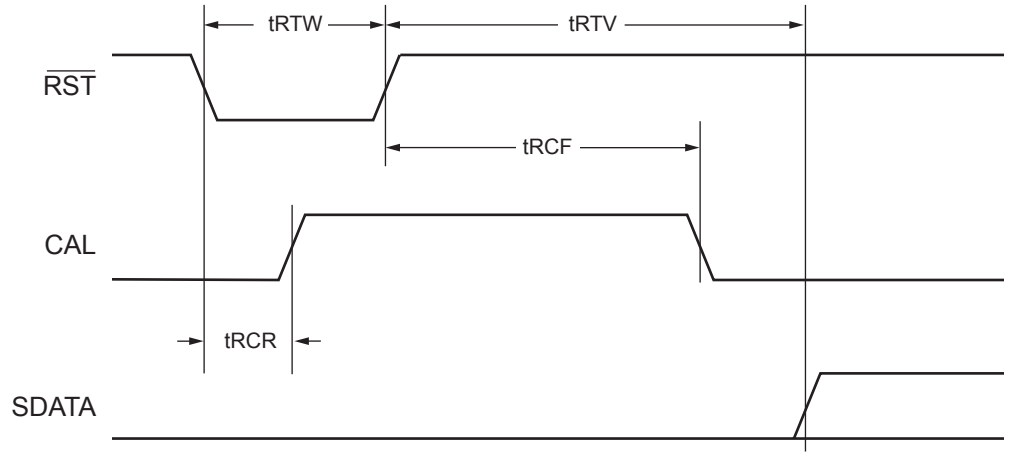



**Figure 5. Reset and Calibration Timing**

# Device Operation

## System Clock Input

Three clocks are requiered to operate the AK5383: the Master Clock (MCLK), the Left/Right Channels Select Clock (LRCK), and the Serial Data Clock (SCLK). Refer to Table 1. The MCLK should be synchronized with the LRCK, but the phase is not critical. MCLK should be 256fs when in the normal sampling mode (i.e. DFS = Low), and should be 128fs when in the double sampling mode. Table 2 shows the standard audio word rates and their corresponding frequencies.

**Table 1. System Clocks**

| | Normal Speed (DFS = Low) | Double Speed (DFS = High) |
|---|---|---|
| LRCK (maximum) | 54kHz | 108kHz |
| BICK | Up to 128fs | Up to 64fs |
| MCLK | 256fs | 128fs |

**Table 2. System Clocks**

| fs | MCLK | SCLK |
|---|---|---|
| 32.0kHz | 8.1920MHz | 4.0960MHz |
| 44.1kHz | 11.2896MHz | 5.6448MHz |
| 48.0kHz | 12.2880MHz | 6.1440MHz |
| 96.0kHz | 12.2880MHz | 6.1440MHz |

The AK5383 includes a phase detect circuit for the LRCK; thus, by changing the clock frequencies, the device is reset automatically when synchronization of MCLK on LRCK is not maintained. With this feature, resetting the AK5383 is only needed during power-up.

Ideally, all external clocks—MCLK, BICK, and LRCK—should always be present whenever the AK5383 is in normal operation (that is, when $\overline{RST}$ is High). In real applications, however, one or more of these clocks may not be present for a short amount of time. When this occurs, the AK5383 should be reset by setting the $\overline{RST}$ pin Low, which resets and powers down the device. Once all the clocks have been reinstated, the $\overline{RST}$ pin can again be set High for normal operation, completing the reset procedure.

**Caution:**
Due to its internal dynamic refresh logic, prolonged periods of time without external clock input may result in damage to the device.

## Serial Data Interface

The AK5383 supports four serial data formats which can be selected using the SMODE1 and SMODE2 pins. Refer to Table 3. The data format is MSB first and 2's complement. Figures 6 through 9 show the timing diagrams for the four different types of serial data formats.

**Table 3. Serial Interface Formats**

| Timing Diagram | SMODE2 | SMODE1 | Mode | LRCK | |
|---|---|---|---|---|---|
| | | | | Left Channel | Right Channel |
| Figure 6 | L | L | Slave Mode | H | L |
| Figure 7 | L | H | Master Mode | H | L |
| Figure 8 | H | L | $I^2S$ Slave Mode | L | H |
| Figure 9 | H | H | $I^2S$ Master Mode | L | H |

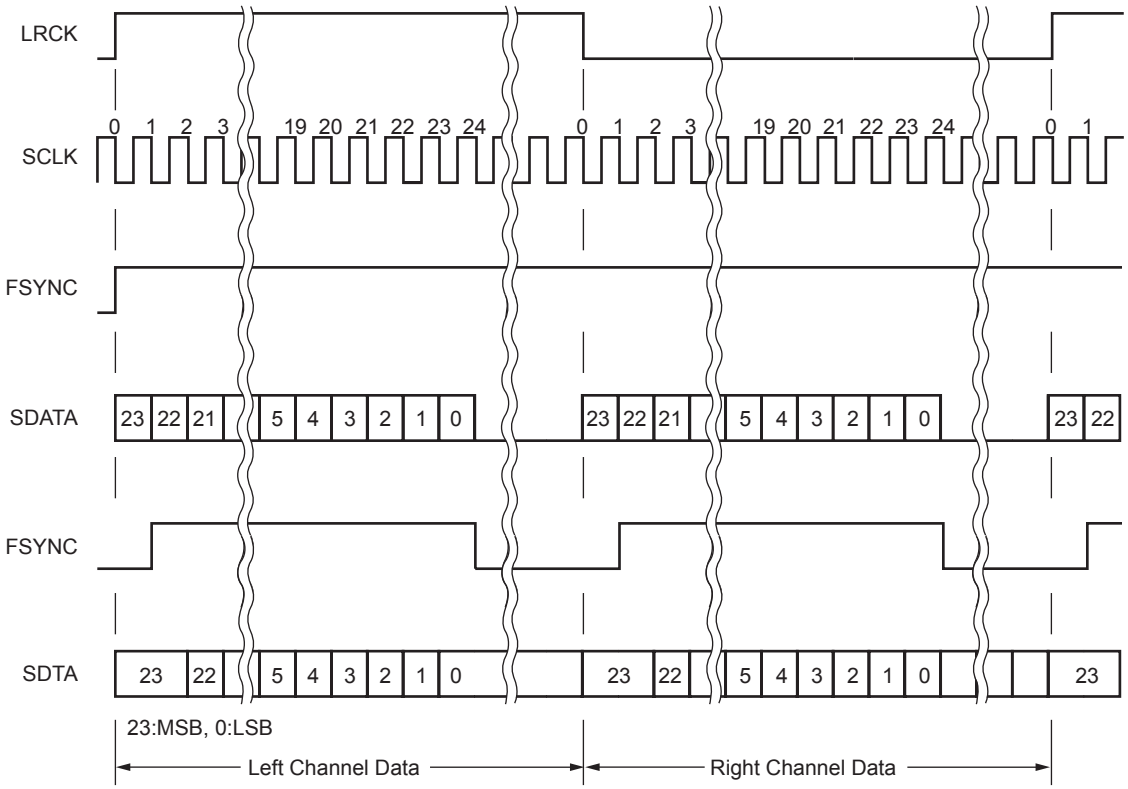



**Figure 6. Serial Data Timing—Slave Mode**

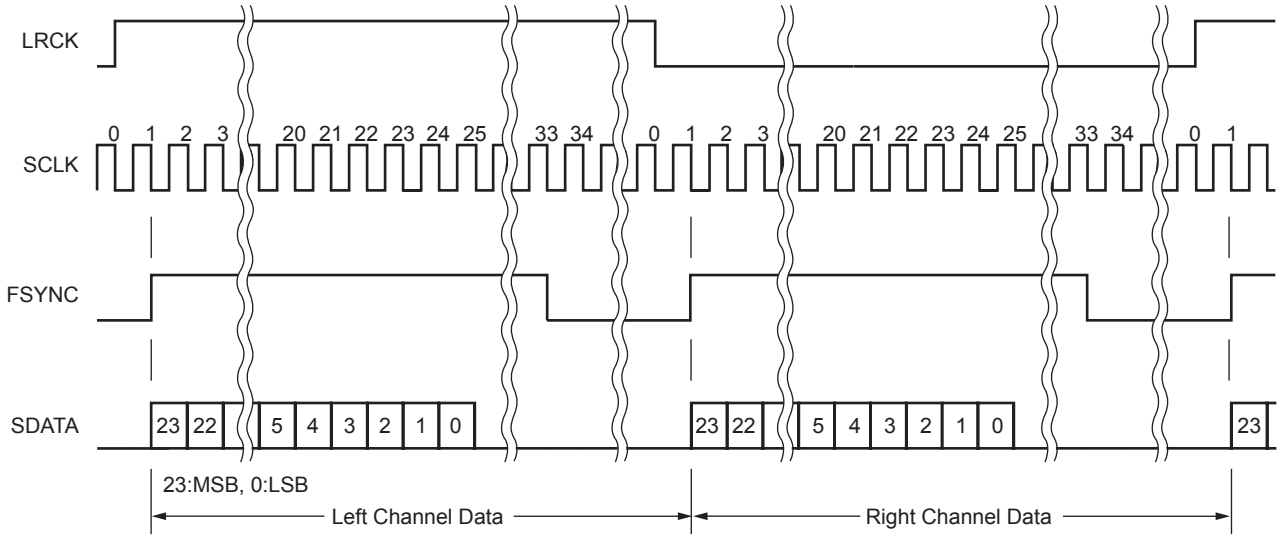



**Figure 7. Serial Data Timing—Master Mode (DFS = Low)**

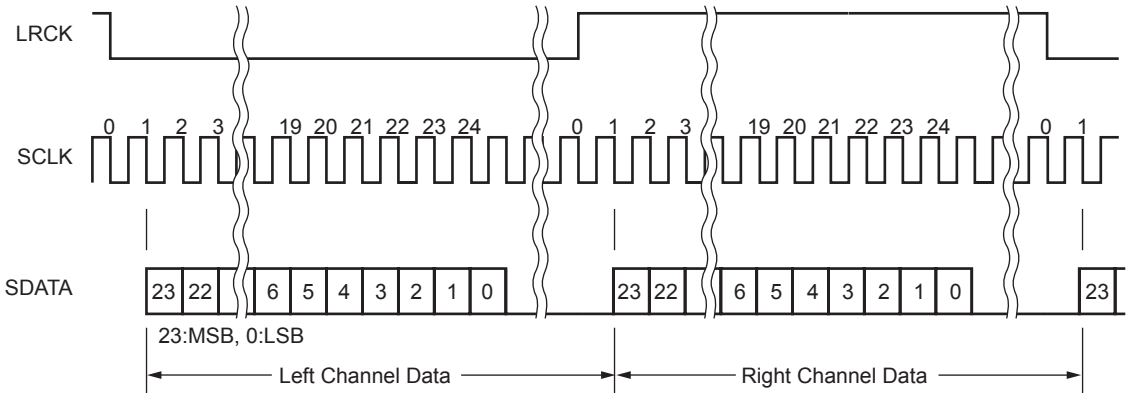



**Figure 8. Serial Data Timing—I²S Slave Mode**

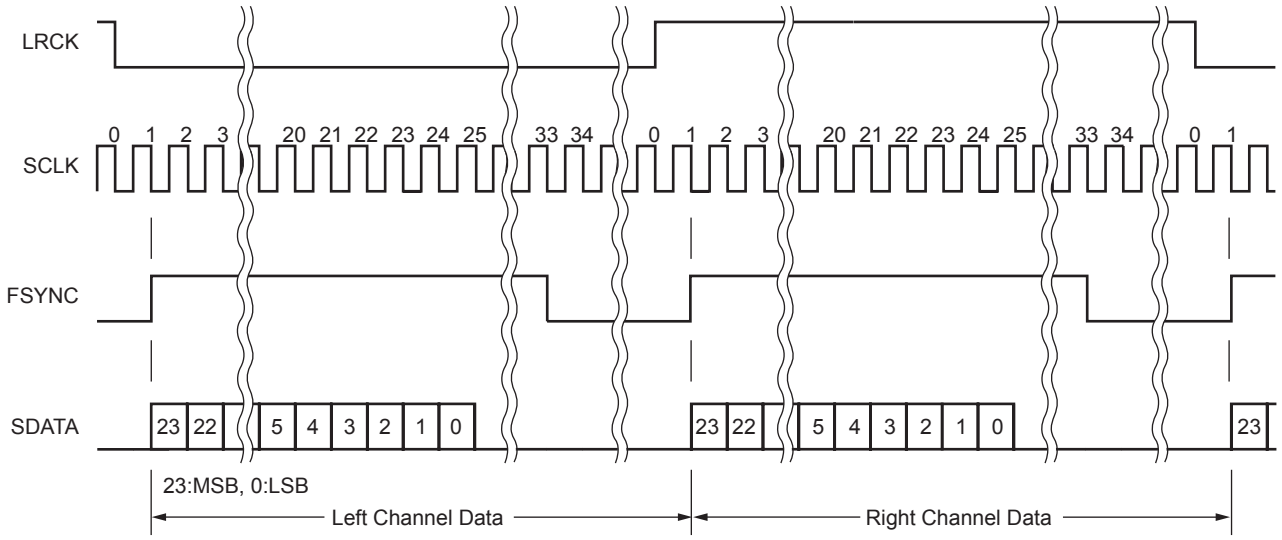



**Figure 9. Serial Data Timing—I²S Master Mode (DFS = Low)**

## Offset Calibration

When the $\overline{\text{RST}}$ pin goes Low, the digital section of the AK5383 is powered down. When this pin returns to High, an offset calibration cycle is started. Such cycle should always be initiated after power-up.

During the offset calibration cycle, the digital section of the AK5383 measures and store the calibration value of each channel into the registers. These calibration values are subtracted from all future outputs. Calibration values may be obtained from the analog input pins (AINL-, AINL+, AINR-, and AINR+) or from the common voltage pins (VCOML and VCOMR) depending on the state of the ZCAL pin. When ZCAL is High, voltages from the analog input pins are measured. When ZCAL is Low, the common voltage pins are measured. The CAL pin is High during calibration.

## Digital High Pass Filter

The AK5383 includes a digital High Pass Filter (HPF) used for DC offset cancellation. The cut-off frequency, fc, for the HPF is 1Hz at fs = 48kHz. This frequency also scales with the sampling rate, fs. The cut-off frequency can be calculated by fc = fs/48k.

# Design Considerations

Figure 10 shows a system connection diagram. An evaluation board for this device is available, the AKD5383 (see the Ordering Information section). This board demonstrates the applications circuits, an optimum layout, power supply arrangements, and measurement results.

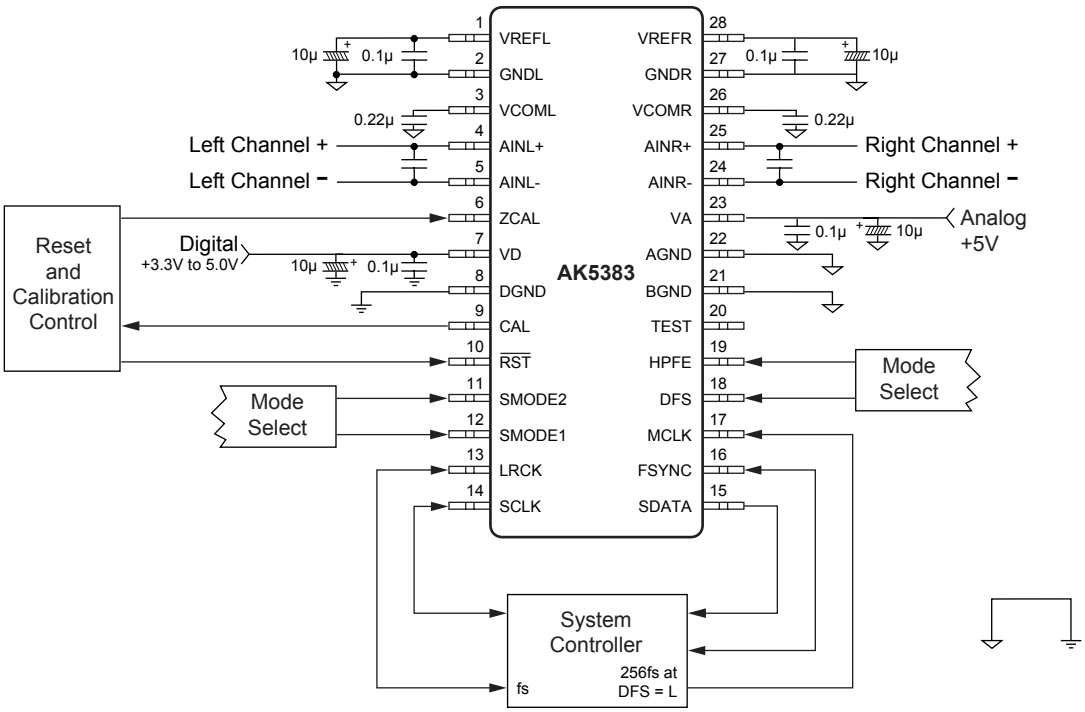



**Figure 10. Typical Connection Diagram for Crystal Mode**

## Grounding and Power Supply Decoupling

Careful attention should be observed for the power supply and grounding of the AK5383. The system's analog and digital grounds are kept separate, but they should be connected together close to where the supplies are brought together into the printed circuit board. The decoupling capacitors should be as close to the AK5383 as possible, with the smaller valued ceramic capacitor being the one nearest to the device.

## Voltage Reference and Common Voltage

The AK5383 reference voltage is a differential voltage between the output voltage reference pins (VREFL and VREFR) and the ground pins (GNDL and GNDR). The GNDL and GNDR pins are connected to AGND. In addition, 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor should be connected between the VREFL and GNDL, and between the VREFR and GNDR pins to eliminate the effects of high-frequency noise. It is especially important to place the ceramic capacitors as close to the pins as possible.

All digital signals, especially the clocks, should be kept away from the VREFL and VREFR pins to avoid unwanted coupling with the AK5383. No load current may be drawn from these pins.

The VCOML and VCOMR pins are the common voltages of the analog signals. To eliminate the effects of high-frequency noise, a 0.22µF ceramic capacitor should be connected as close to each of these pins as possible. All signals, especially the clocks, should be kept away from the VCOML and VCOMR pins to avoid unwanted noise coupled into the AK5383. No load current may be drawn from these pins.

## Analog Inputs

The AK5383 receives analog signals differentially into the modulator through the analog input pins (AINL-, AINL+, AINR-, and AINR+). Each pin full scale is typically $\pm 2.45V_{P-P}$. The AK5383 can accept input voltages from AGND to VA (that is, from 0V to 5V). The ADC output data is 2's complement. The 24-bit output code is 7FFFFFH for an input signal above a positive full scale, and 800000H for an input signal below a negative full scale. With no input signal, the ideal 24-bit code is 000000H. The DC offset is removed during the offset calibration, or by the HPF in the AK5383.

Internally, the AK5383 samples the analog input signal at 128fs (that is, 6.144MHz at fs = 48kHz when the DFS pin is Low). The digital filter rejects noise above the stop band, except for multiples of 128fs. A simple RC filter may be used to attenuate any noise around 128fs so that most audio signals do not have significant energy at 128fs.

The AK5383 accepts +5V voltage supply. The following conditions should be avoided.

- Any voltage above VA + 0.3V,
- Any voltage below AGND - 0.3V, and
- Any current beyond 10mA for the analog input pins.

**Caution:**
Excessive currents to the input pins may damage the device. Protect input pins from signals at or beyond the limits stated above, especially if using ±15V in other analog circuits.

Figure 11 shows a fully differential input buffer circuit example with an inverted amplifier (gain = -10dB). The 22nF capacitor between AINL-/AINR- and AINL+/AINR+ decreases the feed through noise of the modulator. The 51Ω resistor has been inserted to stabilize the op-amps before the ADC. This circuit acts also as a LPF with a cut-off frequency of about 140kHz. In this example, the internal offset is removed by self calibration. Refer to the evaluation board data sheet for complete details.

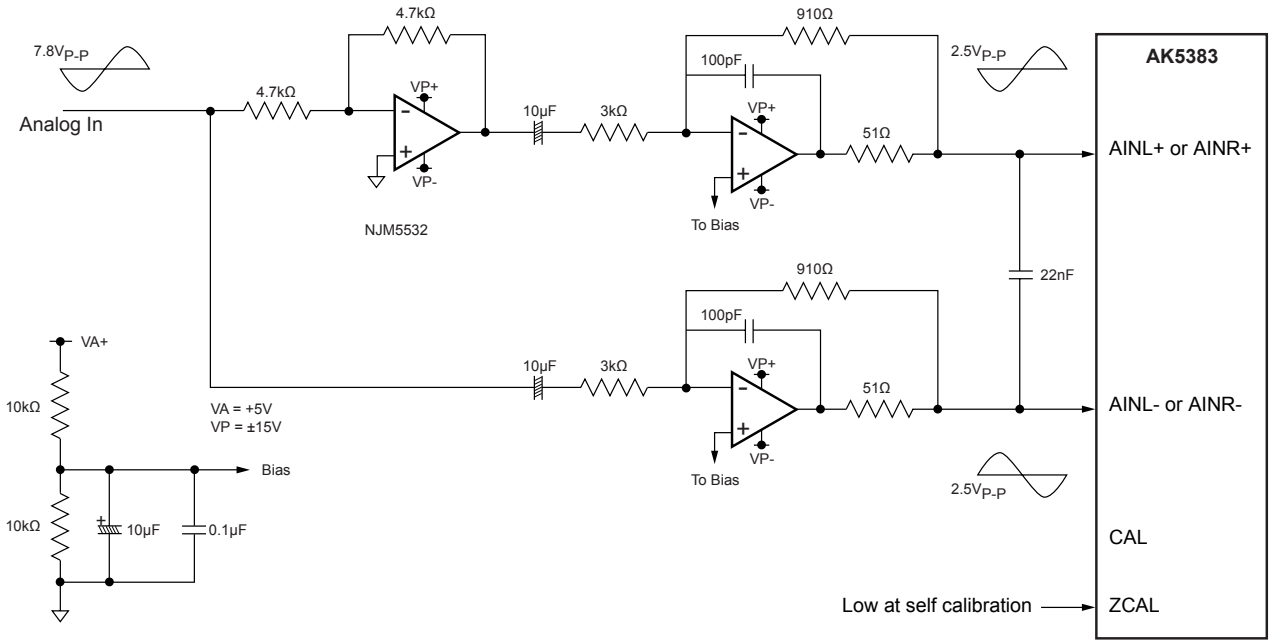



**Figure 11. Example of a Differential Input Buffer Circuit**

## Notes:

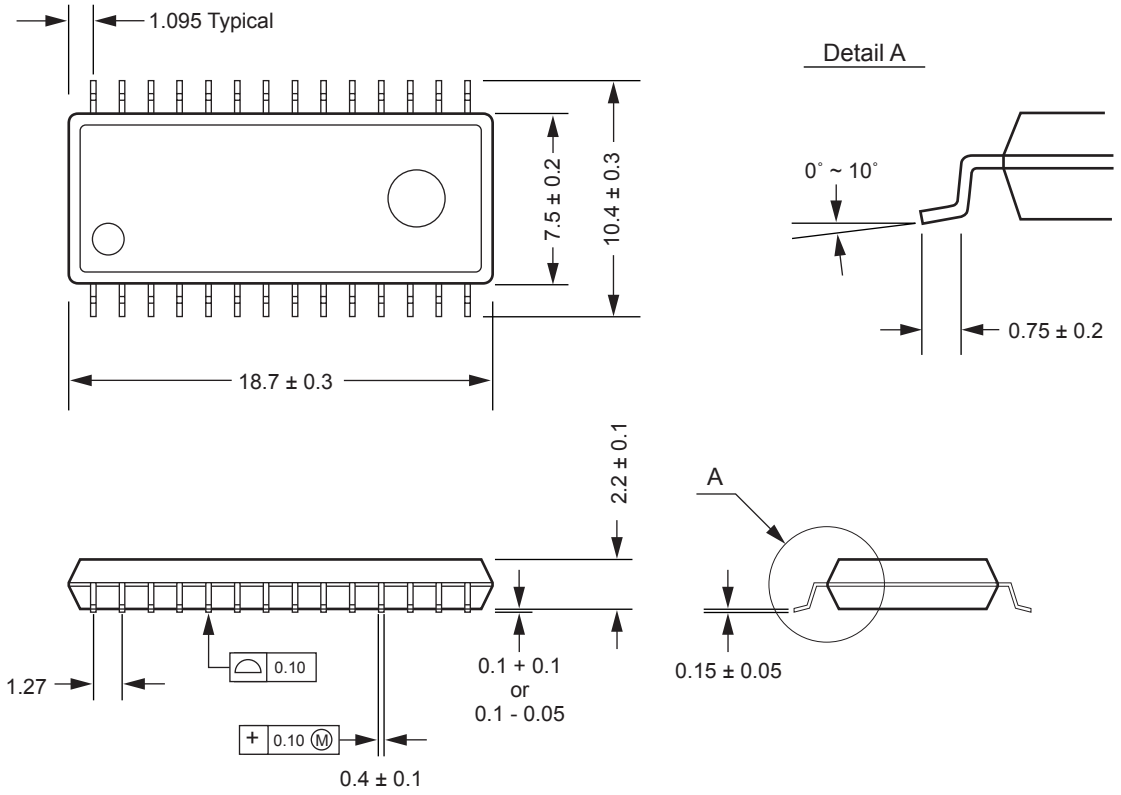
## Notes:

## Notes:

# Package Dimensions

## 28-Pin SOP

**Units: mm**




**Material and Lead Frame Material:**

| | |
|---|---|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder Plate |

# Package Markings




XXXBYYYYC: Data Code Identifier

XXXB: Lot Number (X: Digit Number, B: Alpha Character)
YYYYC: Assembly Date (YYYY: Digit Number, C: Alpha Character)

# Ordering Information

| Part Number | Temperature Range | Package |
|---|---|---|
| AK5383VS | -10˚C to +70˚C | 28-Pin SOP |
| AKD5383 | | Evaluation Board |

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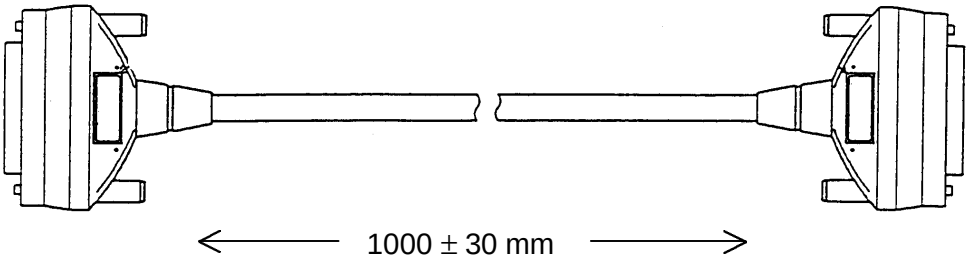
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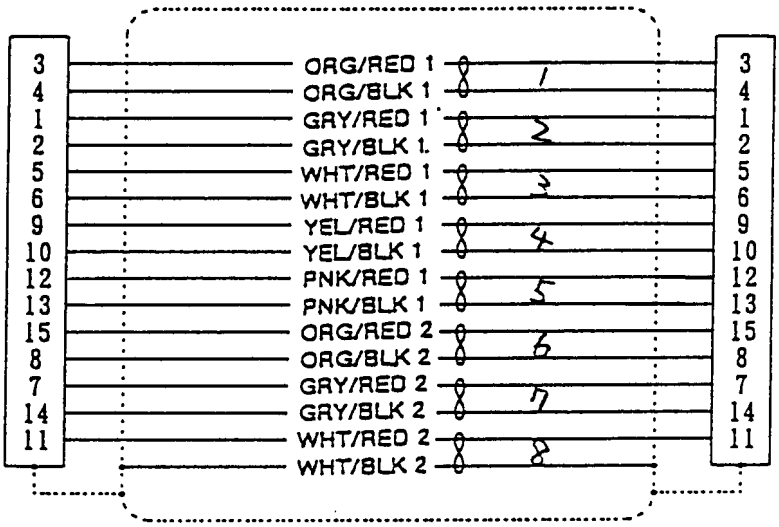
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# Cable Assy, MMC-38

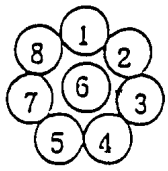
Male
DA-38 SYNC IN

Female
MMC-38 REMOTE OUT




means Twisted wire




| | | |
|---|---|---|
| 1 pce | 53363570-00 | Connector Plug, 15 pin D-Sub(Male) |
| 1 pce | 13152907 | Connector Socket, 15 pin D-Sub(Female) |
| 2 pcs | 53363580-00 | Case Assy, 15 pin D-Sub |




# The DM-24 as a Controller for Steinberg Cubase and Nuendo

It's possible to control most of the functions of Cubase and Nuendo via the DM-24's faders and switches. This is accomplished by using VST's Generic Controller mode and the DM24VST.XML template file available on the TASCAM website (http://www.tascam.com/products/digital_mixers/dm24/index.php)

NOTE that DM-24 firmware version 1.60 or later is required for the procedures below to function.

- Connect MIDI In and Out from your computer's MIDI interface to the DM-24.

**In Cubase VST 5.xx:**

- In the Options/MIDI Setup/System menu, make sure the MIDI outputs and inputs connected to the DM-24 are enabled.
- In the Options/VST Remote menu, select Generic Remote from the Remote menu, and select the aforementioned MIDI input and output.

**In Nuendo 1.5x,**

- In the Devices menu:
    - Select the Add/Remove tab and choose Generic Remote from the list on the right. Then click the Add button.
    - Select the Setup tab and choose Generic Remote from the list of available devices on the left.
    - Select the MIDI In and MIDI out ports connected to the DM-24.

Now, in either program,

- Click the Edit button, and in the Edit window select Import
- Select the file DM24VST.XML and click Okay.

**Notes on the Generic Remote template**

The Generic Remote template can be customized to a considerable degree. Individual functions like EQ, FX sends, etc. can be mapped out to the DM-24's faders, soft knobs and switches. We've included a few example banks (Buss Channels, Groups, and EQ's) to get you started.

In the template you will find:

- Four banks of 16 faders
- One bank for 8 group faders, solos and aux send levels
- One bank for buss faders (this will vary in number depending on your audio device)
- Three banks for EQ control. The EQ control functions as follows:

- Faders 1, 4, 7 and 10 = EQ level for each of four bands
- MUTE 1,4,7, and 10 = EQ on/off for each of four bands
- Faders 2,5,8,and 11 = EQ frequency for each of four bands
- Faders 3,6,9 and 12 = EQ bandwidth for each of four bands

Note that the EQ controls have only been created for the first three channels. If you are comfortable with their implementation, it is a simple matter to open the XML file in a word processor and amend the file to include all channels by cutting and pasting. If you do not wish to use this function, simply delete these banks and save the new file.
These different banks can be accessed in the VST REMOTE window which appears when a remote is selected.

**A few notes and caveats:**

- The FF and RWD keys on the DM-24 are not capable of sending out a dual command (press-on/release-off). Once you press FF (or RWD), the transport remains in that state until you press FF (or RWD) again.
- The STOP command in Cubase does not function as expected in the current version (v5.1r1). Pressing STOP once will return the transport to zero and continue playing. Pressing STOP a second time will actually stop the transport. Steinberg are aware of this and plan on fixing it in an update.
- In the current version of Nuendo (1.52), MMC does not work. Again, Steinberg will be fixing this in an update.

# HUI MIDI Protocol, version 1.1A  12/19/97

Preface…

Written by CMalone and BMcCully, throughout 1997.

Portions subject to change at any moment - but we feel that everything in this version is very stable, since the product is shipping.

For technical I/O, please contact Brian McCully at Brian@Mackie.com
I'm usually relatively prompt with email, and it sure is a heck of a lot more convenient that 'phonus interruptus'

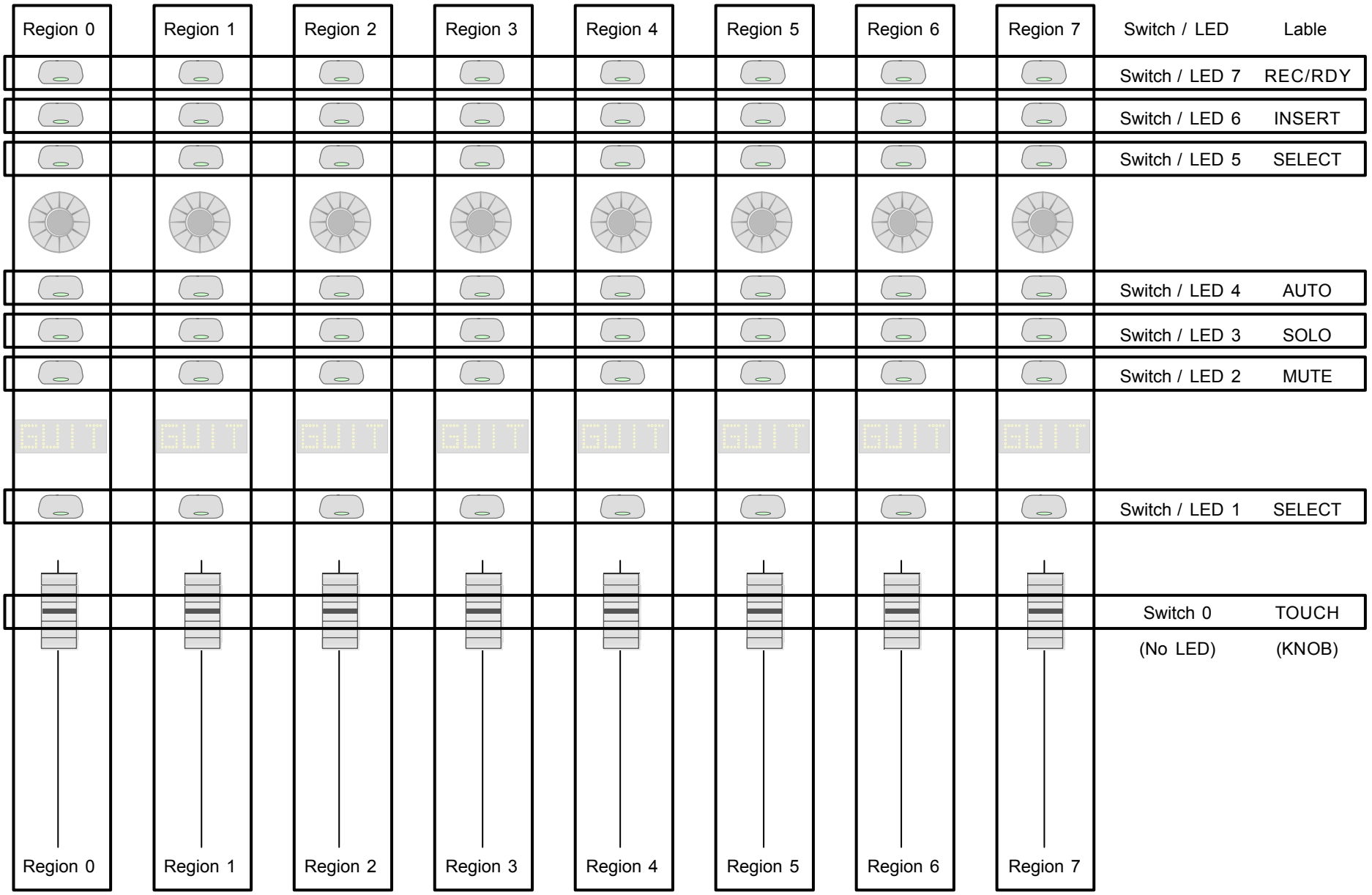
Please do not call, unless you absolutely have to.

For HUI self test and demo modes, please see page 14.

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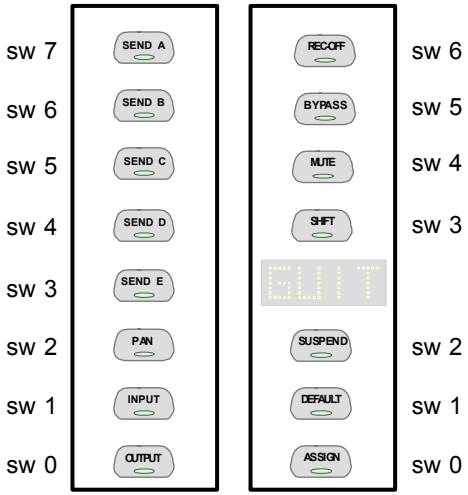
Thanks,

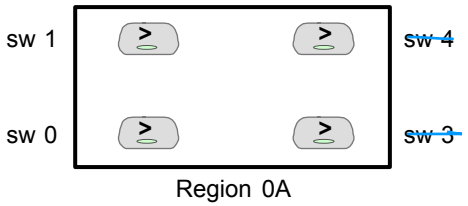
Brian McCully
Mackie Designs

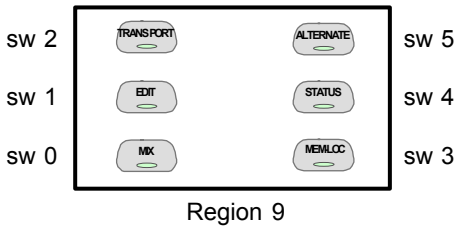


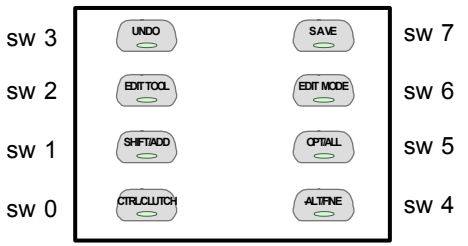

Switch Example
B0, 0F, 03, 2F, 41 = midi ch 0, on
B0, 0F, 03, 2F, 01 = midi ch 0, off
Region 3 on or off Switch 1

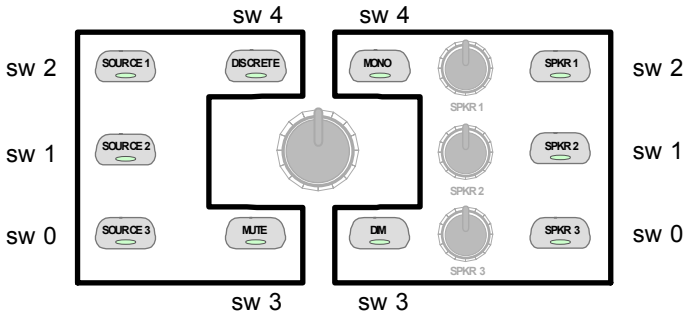
LED Example
B0, 0C, 03, 2C, 41 = midi ch 0, on
B0, 0C, 03, 2C, 01 = midi ch 0, off
Region 3 on or off LED 1

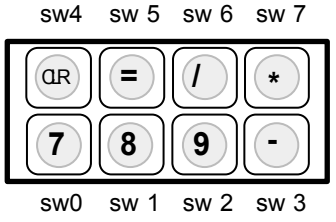

sw 7
sw 6
sw 5
sw 4
sw 3
sw 2
sw 1
sw 0
SEND A
SEND B
SEND C
SEND D
SEND E
PAN
INPUT
OUTPUT
RECOFF
BYPASS
MUTE
SHIFT
SUSPEND
DEFAULT
ASSIGN
sw 6
sw 5
sw 4
sw 3
sw 2
sw 1
sw 0
Region 0B
Region 0C

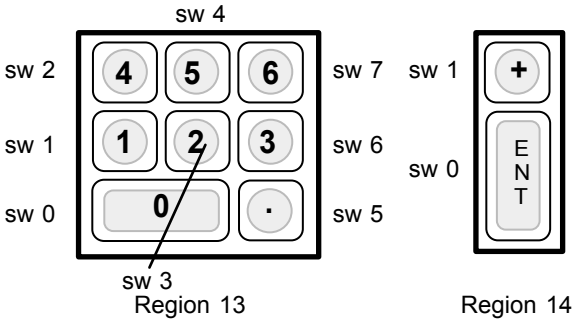

sw 1
sw 0
sw 4
sw 3
Region 0A

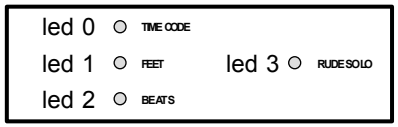

sw 2
sw 1
sw 0
TRANSPORT
EDIT
MIX
ALTERNATE
STATUS
MEMLOC
sw 5
sw 4
sw 3
Region 9

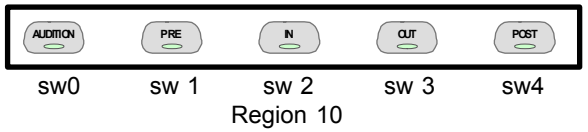

sw 3
sw 2
sw 1
sw 0
UNDO
EDIT TOOL
SHIFT/ADD
CTRL/CLUTCH
SAVE
EDIT MODE
OPT/ALL
ALT/FINE
sw 7
sw 6
sw 5
sw 4
Region 8

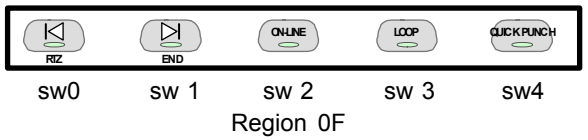

sw 4
sw 4
sw 2
sw 1
sw 0
SOURCE 1
DISCRETE
SOURCE 2
SOURCE 3
MUTE
MONO
DIM
SPKR 1
SPKR 2
SPKR 3
sw 2
sw 1
sw 0
sw 3
sw 3
Region 11
Region 12

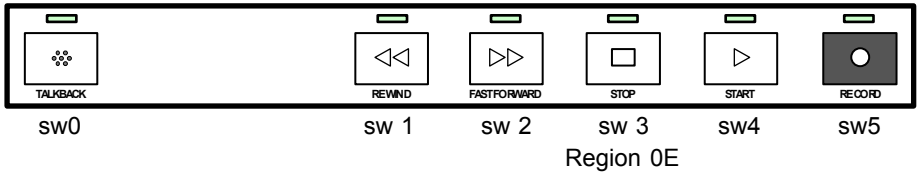

sw4 sw 5 sw 6 sw 7
CLR
=
/
*
7
8
9
-
sw0 sw 1 sw 2 sw 3
Region 15

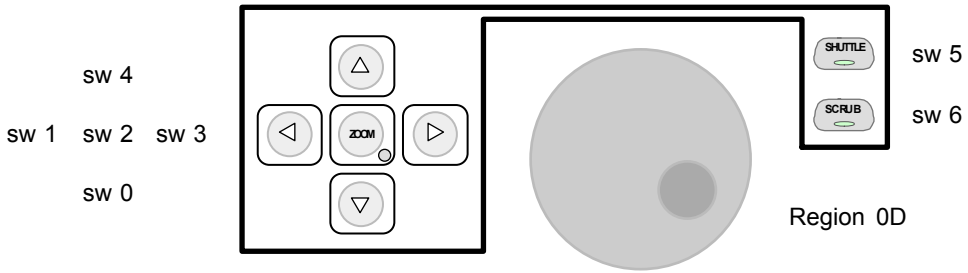

sw 4
sw 2
sw 1
sw 0
4
5
6
1
2
3
0
.
sw 7
sw 6
sw 5
sw 3
Region 13
sw 1
sw 0
+
ENT
Region 14

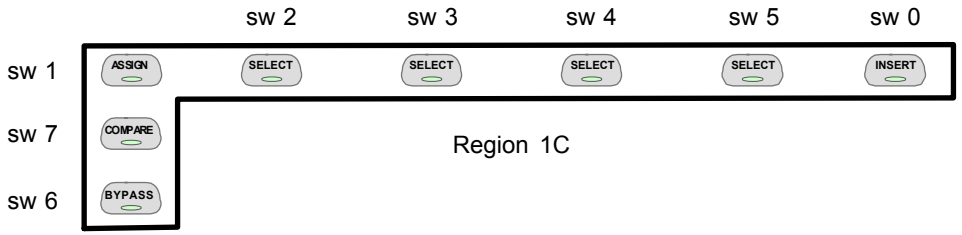

led 0 TIME CODE
led 1 FEET
led 2 BEATS
led 3 RUDE SOLO
Region 16


AUDITION
PRE
IN
OUT
POST
sw0 sw 1 sw 2 sw 3 sw4
Region 10

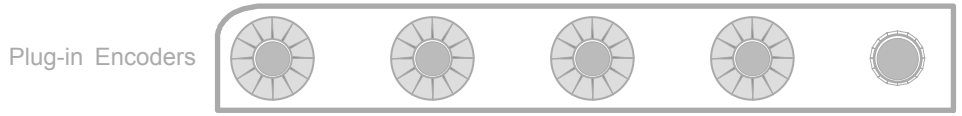

RTZ
END
ON-LINE
LOOP
QUICK PUNCH
sw0 sw 1 sw 2 sw 3 sw4
Region 0F

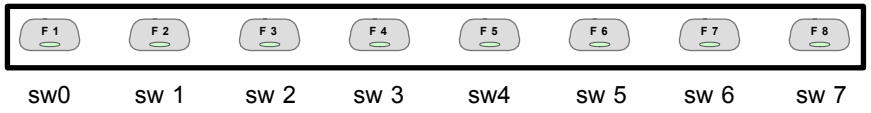

TALKBACK
REWIND
FASTFORWARD
STOP
START
RECORD
sw0 sw 1 sw 2 sw 3 sw4 sw5
Region 0E


sw 4
sw 1 sw 2 sw 3
sw 0
ZOOM
SHUTTLE
SCRUB
sw 5
sw 6
Region 0D

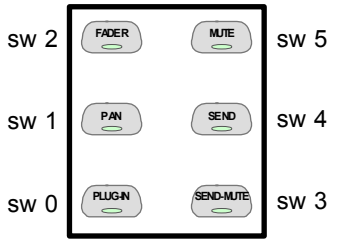



Region 1C

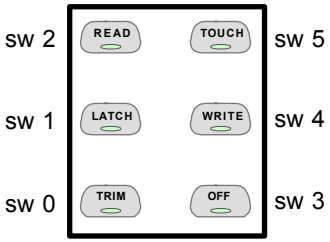


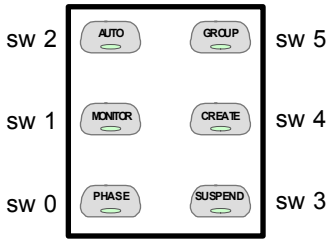

Region 1B



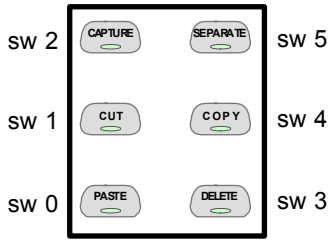

Region 17




Region 18

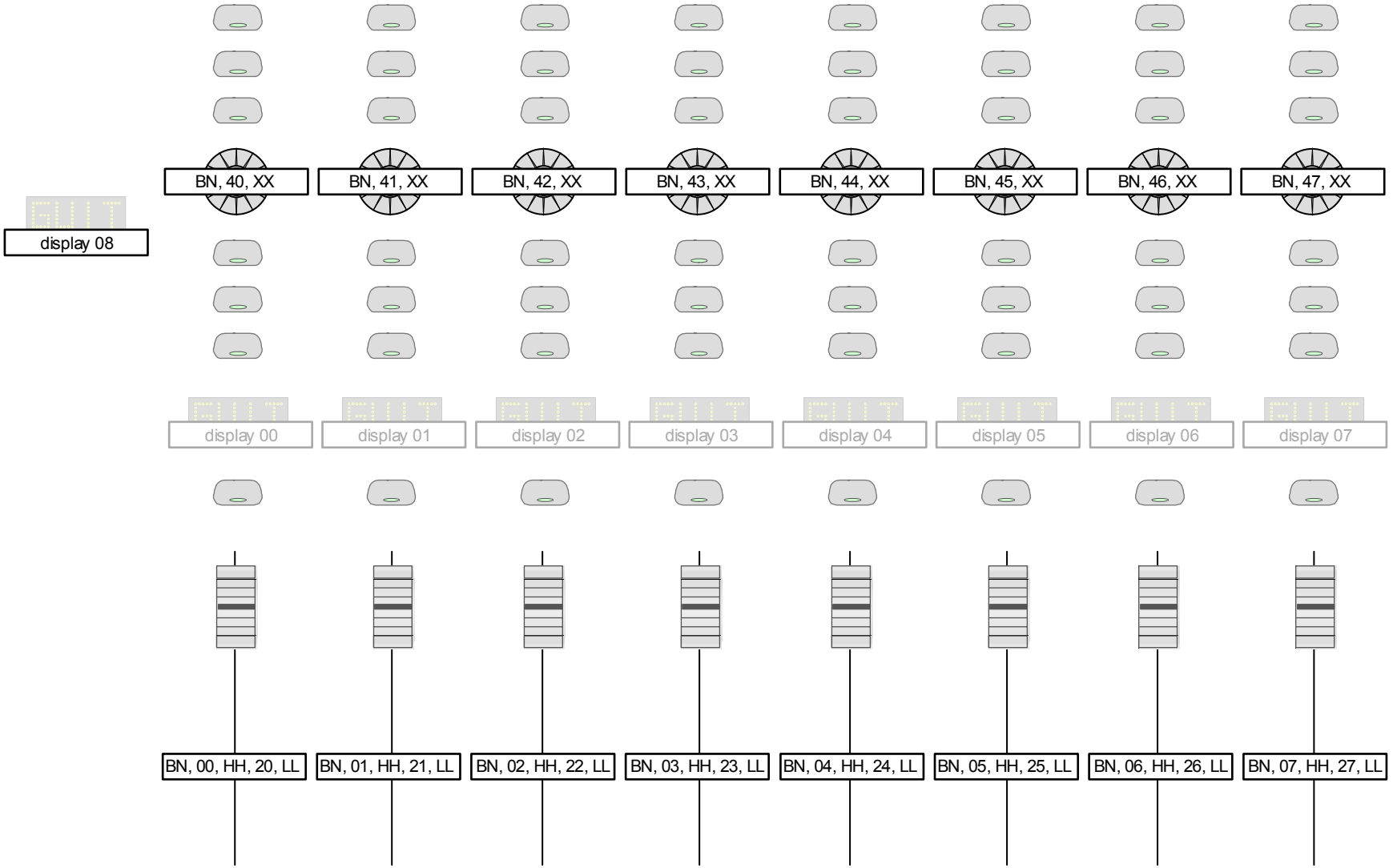


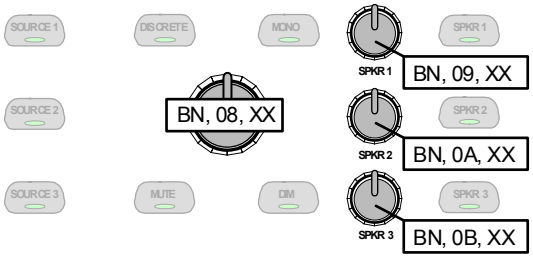

Region 19




Region 1A

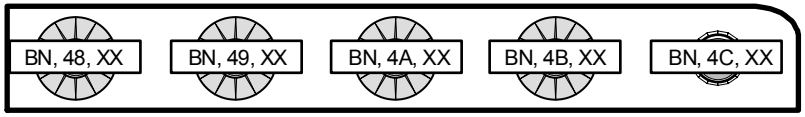
**Note1: fader output messages are the same as incoming servo control messages.**
**Note2: active sensing must be fed to HUI in order for the servos to react to incoming fader commands. There is not currently a mode to disable active sensing, relative to servo control.**



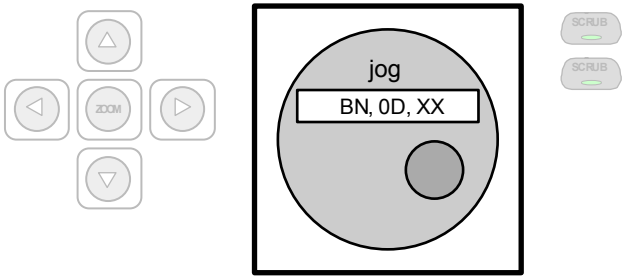



Control Room

Note: these 4 messages are currently disabled.




Plug-in Encoders




Jog = status, +/-, 6 bits of value
positive going is 65 to 127
negative going is 1 to 63
scan rate =

MIDI communication summary

Transmitted

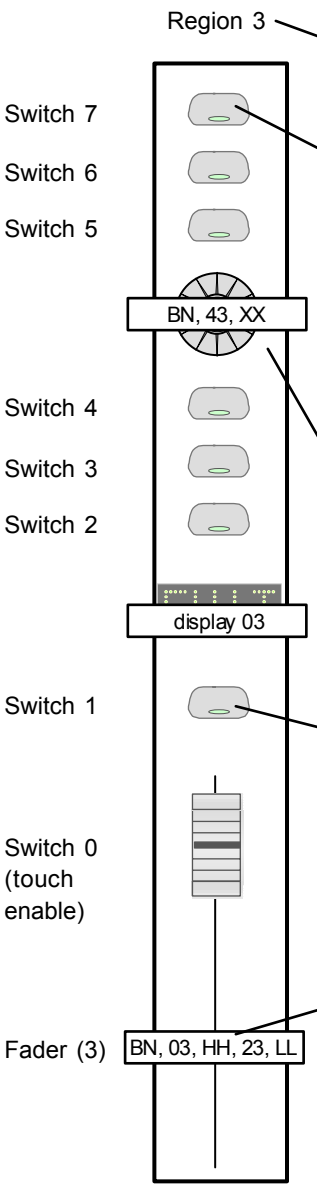
Faders - BN, 00-07, HH, 20-27, LL
Jog - BN, 0D, ...
Control Rm - BN, 08-0B
Reserve - BN, 0E, ...
Switches - BN, 0F, RR, 2F, SS
  RR = region
  SS = status / #
V-Pots - BN, 40-4C

**add footswitches (toggling TB too)**

Received

LEDs - BN, 0C, RR, 2C, LL
  RR = region
  LL = status / #
V-Pot LEDs - BN, 10-1C, ...
4 char LED - sysex
8 char TC display (?)
  -sysex and
  increment rollover
  or 1/4 frame
40 char LCD - Sysex

**Add relay(s)**
**Add active sensing**
**Add meters**




Examples

B0, 0F, 03, 2F, 47 = midi ch 0, on
B0, 0F, 03, 2F, 07 = midi ch 0, off

on or off  Switch 7

LL data bits = 0, 1, 0,0,0,1,1,1
LL data bits = 0, 0, 0,0,0,1,1,1

Switch format: BN, 0F, HH, 2F, LL
BN = controller on MIDI channel N
HH = region number
LL data bits = 0, v, x,x,x,x,x,x
v: 1 = on, 0 = off
x: 00-3F switch number

turn clockwise 16 steps = B0, 43, 50 — 0,1,0,0,0,0,0,0
turn c-clockwise 33 steps = B0, 43, 21 — 0,0,1,0,0,0,0,1

maximum = 7FH

B0, 0F, 03, 2F, 41 = midi ch 0, on
B0, 0F, 03, 2F, 01 = midi ch 0, off

sw4  Region 15

QR  B0, 0F, 15, 2F, 44 = midi ch 0, on

7  B0, 0F, 15, 2F, 40 = midi ch 0, on

sw0

B0, 03, 55, 23, 40 = midi ch 0

MSB  LSB

MSB format = 0, x, x, x, x, x, x, x = 00H to 7FH  (128 values)
LSB format = 0, L, L, 0, 0, 0, 0, 0  = 00H, 20H, 40H, 60H  (4 possible values)

128 x 4 = 512 resolution

**All numbers in hexidecimal**

Sysex display calls: F0, 00, 00, 66, dd, nn, mm, ff, data ....., F7

66 = Mackie ID
dd = device ID, HUI is 05
nn = MIDI channel
mm = message ID
ff = field or character #
data = ascii equivalents for display characters

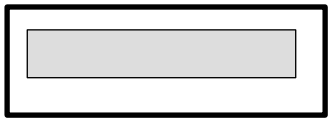
Three types of character display:

1) 4 char, 5x7 LED; mm = 10



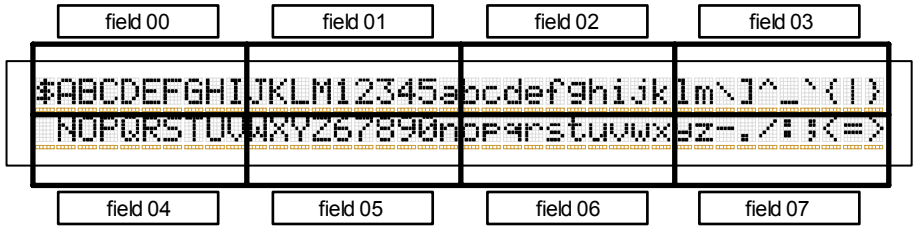

update all 4 characters at once

2) 8 char, 7 segment w/decimal point LED; mm = 11



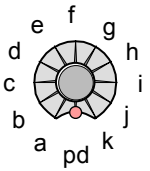
update any one or all characters depending on implementation

3) 40 x 2 character 5x7 pixel with underline, or 5x8, backlit LCD mm = 12




update ten characters at a time left justified to each area

Two illuminated switch types (top to bottom):
12 LED segmented V-Pot ;
Switch LEDs;

4) 


11 LEDs at 7 to 5 clock positions and one larger LED at 6 o'clock

5) 

on or off - blink rate set remotely (no provision for blinking on HUI)

6) Meter sticks

1) 4 char, 5x7 LED;




F0, 00, 00, 66, dd, nn, mm, ff, data ....., F7

displays 00-07 are the channel scribble strips left to right and display 08 is the Select / Assign in the upper left.

mm = 10 for these 4 char display 00-08
ff = which display of the 9 displays
data will be 4 ASCII bytes

For Mackie HUI on MIDI channel 0, scribble display 03 to say 'GUIT' the sysex would be:

F0, 00, 00, 66, 05, 00, 10, 03, 47, 55, 49, 54, F7

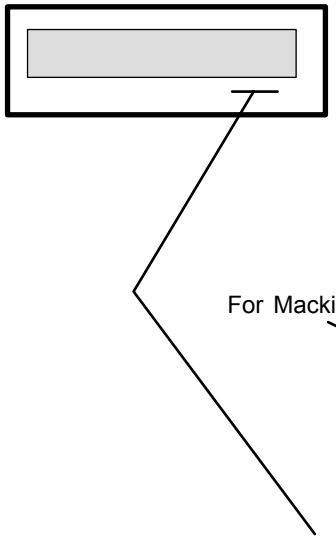
For Mackie HUI on MIDI channel 0, scribble display 03 to say 'GUIT' and scribble display 04 to say 'guit' the sysex would be:

F0, 00, 00, 66, 05, 00, 10, 03, 47, 55, 49, 54, 04, 67, 75, 69, 74, F7

2a) 8 char, 7 segment w/decimal point LED;

F0, 00, 00, 66, dd, nn, mm, ff, data ....., F7

mm = 11 for this 8 char display
data will be 8 ASCII bytes
decimal point 'on' will be bit 4 (add 10 hex)



For Mackie HUI on MIDI channel 0, time display to show 01. 04. 33. 29 (note decimal point on)

F0, 00, 00, 66, 05, 00, 11, 00, 11, 00, 14, 03, 13, 02, 19, F7

F0, 00, 00, 66, 05, 00, 11, 00, 01, 00, 04, 03, 03, 02, 09, F7 - would contain no decimal points

2b) use 'F8' to increment frame digits
and use sysex to roll over according to SMPTE format (24FPS, 25FPS, etc.)

**Note: this method aids MIDI bandwidth questions moreso than method 2a or 2c.**

2c) or use MTC (MIDI Time Code) 1/4 frame messaging

**Note:** DON'T USE BOTH - use either sysex (2a, 2b) or MTC 1/4 frame (2c) ...although...
In order to avoid all-broadcast problems in MIDI systems, the current implementation will filter out MTC 1/4 frame messages, if the sys-ex timecode scheme is encountered in HUI's incoming MIDI messages. i.e. Sys-ex has a higher priority than MTC.

For example, if the end user defines HUI as a MIDI device that receives MTC, but the application is sending Sys-ex Time code, there could be a conflict, if an offset was defined between relative and absolute Time code.

3) 40 x 2 character 5x7 pixel with underline, or 5x8, backlit LCD




F0, 00, 00, 66, dd, nn, mm, ff, data ....., F7

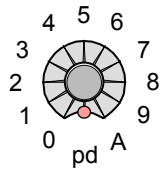
mm = 12 for this 40x2 char display
ff = 00-07 for each 10 char field
data will be 10 ASCII bytes per field

For Mackie HUI on MIDI channel 0, field 04 to show "_ _ _ 13dB _ _ _"

F0, 00, 00, 66, 05, 00, 12, 04, 5F, 5F, 5F, 31, 33, 64, 42, 5F, 5F, 5F, F7

For Mackie HUI on MIDI channel 0, field 04 to show "_ _ 13dB _ _" and field 05 to show "INVERTED"

F0, 00, 00, 66, 05, 00, 12, 04, 5F, 5F, 31, 33, 64, 42, 5F, 5F, 05, 44, 45 , 54, 52, 45, 56, 4E, 49, F7

4) 

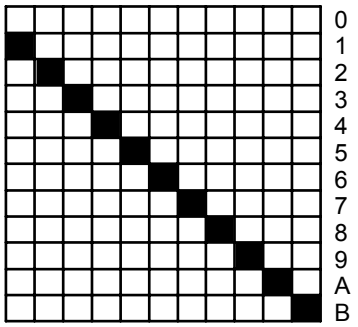

11 LEDs at 7 to 5 clock positions
and one larger LED at 6 o'clock

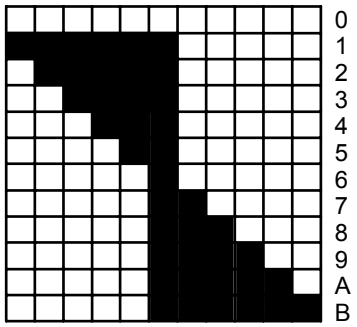
format: B0, 10, XX = V-Pot in Region 00 addressed on midi ch 0

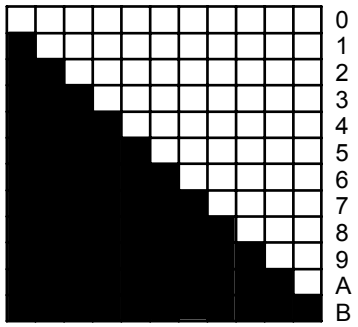
V-Pots 10-17 on channel strips left to right
V-Pots 18-1B address (not a region) in upper right editing section

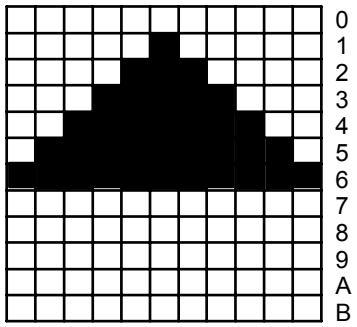
bit map key for below graphics
nnnn = MIDI channel
r r r r = region
p = toggle LED at 6 o'clock
xx = mode
v v v v = LED address (0 to A) shown below - Y axis

| | Single dot Mode (mode 0) | Boost/cut Mode (mode 1) | Wrap Mode (mode 2) | Spread Mode (mode 3) |
|---|---|---|---|---|
| BN | 1011nnnn | 1011nnnn | 1011nnnn | 1011nnnn |
| 1R | 0001r r r r | 0001r r r r | 0001r r r r | 0001r r r r |
| XX | 0 p x x v v v v | 0 p x x v v v v | 0 p x x v v v v | 0 p x x v v v v |
| | (xx = 00) | (xx = 01) | (xx = 10) | (xx = 11) |

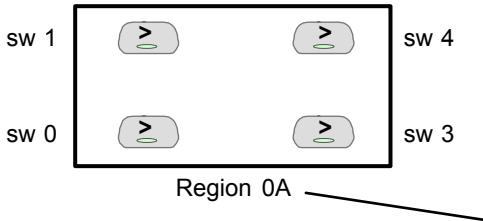


5) 0C (LED) vs 0F (switch toggle) messages.




e.g. for switch 4 the on and off messages are below:

B0, 0C, 0A, 2C, 44 = midi ch 0, on
B0, 0C, 0A, 2C, 04 = midi ch 0, off

on or off — LED #4

LL data bits = 0, 1, 0,0,0,1,1,1
LL data bits = 0, 0, 0,0,0,1,1,1

SWITCH format: BN, 0F, RR, 2F, SS
LED format: BN, 0C, RR, 2C, LL
BN = controller on MIDI channel N
RR = region number

whereas:
SS = Switch #
SS data bits = 0, v, 0,0,0,x,x,x
v: 1 = on, 0 = off
x: 00-07 switch number

Note: Blinking LEDs is the result of the DAW toggling on and off LEDs, hence blink rate or duration is set by the DAW, not by HUI.

whereas:
LL = LED #
LL data bits = 0, p, s, 0, 0,x,x,x
p: primary color, 1 = on, 0 = off
s: secondary color, 1 = on, 0 = off
x: 00-07 switch number

note: currently the only switch with bicolor LEDs is switch #4, regions 0-7, where the primary color is red and the secondary color is green.

examples:
BN 0C 01 2C 04 = switch LED 4 fader 1 = off
BN 0C 01 2C 24 = switch LED 4 fader 1 = green
BN 0C 01 2C 44 = switch LED 4 fader 1 = red
BN 0C 01 2C 64 = switch LED 4 fader 1 = both

6)



Meter sticks

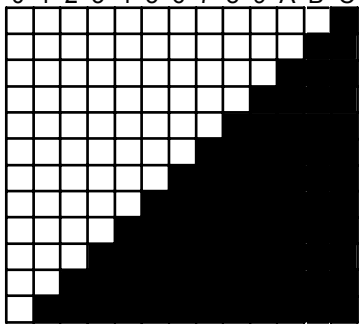
12 LEDs - (appearance wise 2 each x 12 high)

format: AN utilising polyphonic aftertouch on midi ch N
1R = region 0-7
XX = as defined below

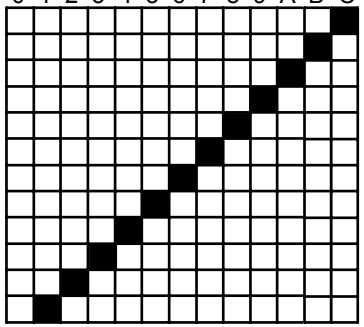
bit map key for below graphics
nnnn = MIDI channel
r r r r = region
c = toggle peak LED (address C) on/off
s = side, where 0 = left and 1 = right
v v v v = LED address (0 = all off, and 1 to C for 12 LEDs) shown below - X axis
Note: peak and rising bar can occur independently of one another and once a peak LED is latched, it needs to be re-addressed to unlatch the LED

| | Rising bar and peak addressing | |
|---|---|---|
| AN | 1010nnnn | Left Rising bar XX = 00-0C |
| 1R | 0000 0 r r r | Right Rising bar XX = 10-1C |
| XX | 0 0 c s vvvv | Left Peak bar XX = 20-2C |
| | | Right Rising bar XX = 30-3C |

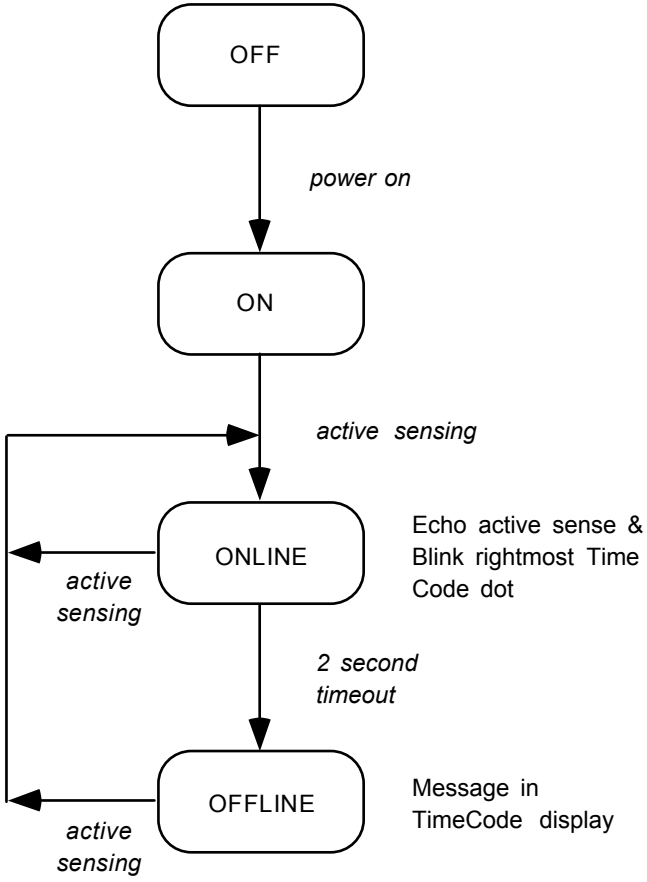
vvvv 0 1 2 3 4 5 6 7 8 9 A B C



0 1 2 3 4 5 6 7 8 9 A B C



Active Sensing Protocol




current active sensing bi-directional message is:
90 00 00

Self test (end user and factory) and Demo mode

1) To enter the end user demo mode:

Turn on HUI
Within three seconds or so, the VFD will light up and display characters (a message)
Immediately press and hold the bottom two left keys (left of the faders), 'ctrl/clutch' and 'alt /fine'
The HUI will enter the Self Demo mode. This will give you an intended usage overview.

2) To enter the end user self test mode:

Plug a normally opened footswitch into footswitch 2
Turn on HUI
Within three seconds or so, the VFD will light up and display characters (a message)
Immediately press and hold the 'next to bottom' two left keys (left of the faders), 'shift/add' and 'opt/all'
The HUI will enter the Self Test mode. This will step you through test functionality.

3) To enter the factory self test mode:

Plug two normally opened footswitches into footswitch jacks 1& 2
Turn on HUI
Within three seconds or so, hold both footswitches down (closed)
The HUI will enter the Factory test mode. There are 8 categories on the VFD, which are the main testing heirarchies. Each of these will open into sub categories.
To enter MAIN Categories: press the Select switch directly under the corresponding 'blinking' topic - the upper and lower blinking rows are toggled using the Insert/Param switch
To exit any category or subcategory - use footswitch 2 and sometimes the Insert/Param

**Please note: we are still working on portions of this protocol - changes may occur at any point. Updates will be forthcoming.**

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# ■ EXT. CTRL

## 1. HUI emulate

### 1.1 verup 内容

| Item | Note. |
|---|---|
| 対応 | HUI emulation<br>・未使用のキーでダイレクトに各機能を操作できるようにした<br>・MIX Window,EDIT Window,ZOOM,∧/∨/＜/＞機能を追加 |

### 1.2 EXT.CTRL screen

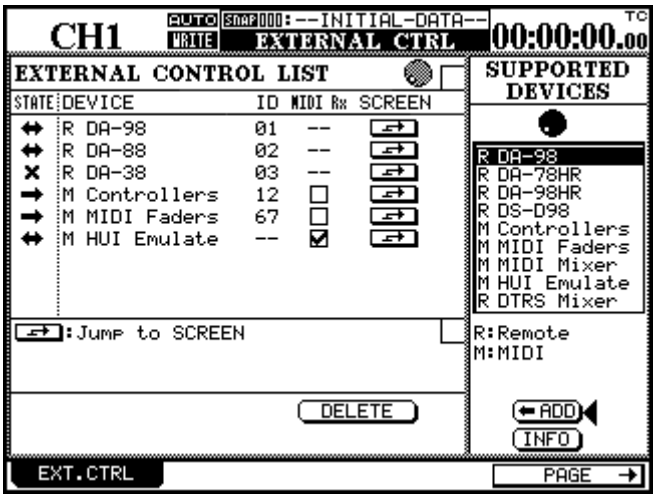



Fig 1 [ext_ctrl07c.gif]

- State

  HUI Emulate は MIDI Closed loop 接続が必要なので State 表示が下記の様になる。

  Status は Active sensing の送受信で判断する。

| State | LCD 表示 | Note |
|---|---|---|
| On line | ↔ | 通信可能な状態 |
| Off line | ✖ | 通信が正常で無い状態 |

- Supported device

  HUI emulate は MIDI I/O を使用するので下記のように表示する。

| Device | Protocol | LCD 表示 |
|---|---|---|
| HUI Emulate | MIDI | M HUI Emulate |

### 1.3 HUI Emulate screen

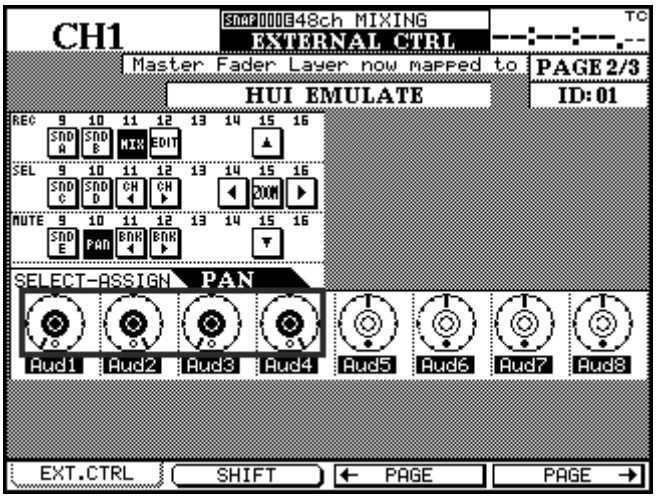



Fig 2 [New_LCD/Ver2.1/HUI/HUI_DefaultName.gif]

- パラメータ操作

| Edit 部 | Edit 可能時 | 操作子 | Note. |
|---|---|---|---|
| V pod | 枠表示<br>POD 反転 | POD1-4 | 左右 4 つずつのコントロール<br>Cursor key / Dial で Cursor 移動 |
| PAN | Layer:Master | Ch10 MUTE | |
| SEND A<>E | Layer:Master | Ch9-10 REC/SEL/MUTE | |
| SHIFT | | LCD SW2 | |
| BANK </> | Layer:Master | Ch11-12 MUTE | |
| CH </> | Layer:Master | Ch11-12 SEL | |
| MIX | Layer:Master | Ch11 REC | |
| EDIT | Layer:Master | Ch12 REC | |
| ZOOM | Layer:Master | Ch15 SEL | |
| ∧/∨/</> | Layer:Master | Ch14-16 REC/SEL/MUTE | |

- PAN SW

  DM-24 LCD 画面上の V pod でコントロールする対象パラメータを Pan に指定する。

  Layer Status:Master の Ch10 MUTE Key で On/Off 切替。

  On 時、反転表示となる。DAW 側から Off に設定するコマンドを受信すると Off 表示となる。

- SEND A <> E SW

  DM-24 LCD 画面上の V pod でコントロールする対象パラメータを Send A<>E に指定する。

  Layer Status:Master の Ch9-10 REC/SEL/MUTE Key で On/Off 切替。

  On 時、反転表示となる。DAW 側から Off に設定するコマンドを受信すると Off 表示となる。

- SHIFT SW

  Pan, Send A <> E のいずれかがセレクトされている時に SHIFT SW を押すと Fader flip mode になり、Send A<>E コントロールにフェーダーを使用することが可能になる。

  LCD SW2 で On/Off 切替。

- Bank / Channel select

  DAW mixer のバンク / チャンネルの切り替えコマンドを送信する。

  Layer Status:Master の Ch11-12 SEL/MUTE Key で操作。

  DAW 側からの Bank / Channel select コマンド受信によって On/Off 表示する。

  Fader / Mute / Rec をコントロールする操作子は常に Ch1-8 位置のコントローラーが対応。

| Item | SW | Note. |
|---|---|---|
| Bank |  | DAW mixer 操作対象を左方向へ 8Ch 単位で切り替えるコマンドを送信 |
| |  | DAW mixer 操作対象を右方向へ 8Ch 単位で切り替えるコマンドを送信 |
| Channel |  | DAW mixer 操作対象を左方向へ 1Ch 単位で切り替えるコマンドを送信 |
| |  | DAW mixer 操作対象を右方向へ 1Ch 単位で切り替えるコマンドを送信 |

- MIX / EDIT SW

  DAW の Mix/Edit Window を表示するコマンドを送信する。

  Layer Status:Master の Ch11-12 REC Key で On/Off 切替。

  On 時、反転表示となる。DAW 側から Off に設定するコマンドを受信すると Off 表示となる。

- ZOOM SW

  DAW Edit Window の ZOOM Mode を切り替えるコマンドを送信する。

  Layer Status:Master の Ch15 SEL Key で操作。

  DAW 側からの ZOOM コマンド受信によって On/Blink/Off 表示となる。

  DAW 側から定期的に ZOOM コマンド On/Off が送られてくることで Blink 表示になる。

- ∧/∨/＜/＞ SW

  DAW Edit Window の ZOOM 率切替、カーソル移動コマンドを送信する。

  Layer Status:Master の Ch14-16 REC/SEL/MUTE Key で操作。

  DAW 側からの∧/∨/＜/＞コマンド受信によって On/ Off 表示となる。

- Select-Assign

  V-pod がコントロールする対象となっているパラメータ名を表示する。

  表示は全て DAW から送られてくる文字データに従って表示する。

- V pod

  Select-Assign でセレクトされている DAW mixer の対象パラメータをコントロールする。

  POD1-4 を操作する事によってパラメータ・コントロール・コマンドを送信するが、表示は DAW からのコマンドを受信することによって行う。

| 状態 | LCD 表示 | Note. |
|---|---|---|
| 全点灯 |  | カレント・カーソル位置：POD 以外 |
| |  | カレント・カーソル位置：POD 時 |
| 全消灯 |  | カレント・カーソル位置：POD 以外 |
| |  | カレント・カーソル位置：POD 時 |

- Channel scribble strip data indication

  V-pod の下に DAW で設定された各 Module name を表示する。

  表示は DAW より送られてきたコマンドを受信する事によって表示する。

| LCD 表示 | Note. |
|---|---|
|  | 表示文字数：4<br>反転表示 |

- Parameters

  Pan,Send A<> E,SHIFT,BANK </>,CH </>,MIX,EDIT,ZOOM,∧/∨/＜/＞

  On / Off

  操作：Command 送信

  表示：Command 受信

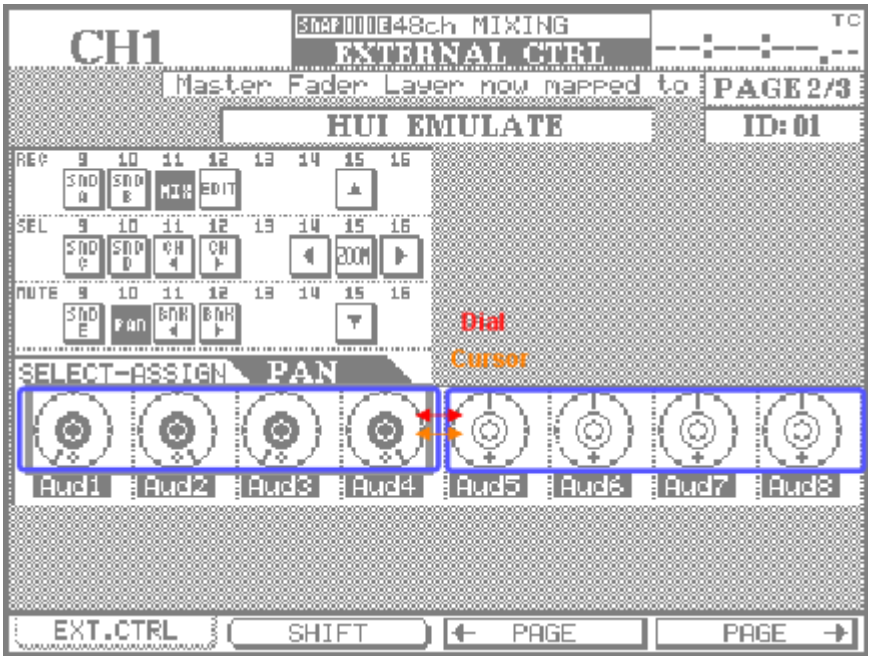
  V pod 操作：Command 送信

  表示：Command 受信

  Module name 表示：Command 受信

  Select Assign 表示：Command 受信

- Cursor position transition



## 2. History

**Rev: A -> B**

| No. | Page | Note | Modify |
|---|---|---|---|
| 1 | 4 | Fig. 2 差し替え | 2002/06/25 |
| 2 | - | 1.2.2 MIDI Mixer: Stereo fader を対象外に変更 | 2002/06/25 |

**Rev: B -> C**

| No. | Page | Note | Modify |
|---|---|---|---|
| 1 | | 2. sp184 追加 | 2002/07/05 |

**Rev: C -> D**

| No. | Page | Note | Modify |
|---|---|---|---|
| 1 | 2 | Fig. 1 差し替え SCREEN と MIDI Rx に位置を入れ替え | 2002/07/08 |
| 2 | 6 | Fig. 3 差し替え SCREEN と MIDI Rx に位置を入れ替え | 2002/07/08 |
| 3 | 7 | Fig. 4 差し替え 図選択ミス | 2002/07/08 |

**Rev: D -> E**

| No. | Page | Note | Modify |
|---|---|---|---|
| 1 | 6 | ➢ Status コメント追加 「Status は Active sensing の送受信で判断する。」 | 2002/07/09 |

**Rev: E -> F**

| No. | Page | Note | Modify |
|---|---|---|---|
| 1 | 7 | Fig. 4 差し替え | 2002/07/11 |
| 2 | 8 | ➢ Channel scribble strip data 項追加 | 2002/07/11 |
| 3 | 9 | 3. sp268 [EXT. CRTL Fader を使用する Device の Ext Ctrl layer への自動切り替え] 項追加 | 2002/07/11 |

**Rev: F -> G**

| No. | Page | Note | Modify |
|---|---|---|---|
| 1 | - | 2. sp184 [HUI emulate]<br>Emulate 対象に send A<>E 追加 | 2002/08/12 |

**Rev: G -> H**

| No. | Page | Note | Modify |
|---|---|---|---|
| 1 | 3 | Fig 2 差し替え<br>➢ パラメータ操作<br>PANSEND A<>E,SHIFT,BANK/CHANNEL の Edit 可能時/操作子欄を変更<br>SHIFT,MIX,EDIT,ZOOM,∧/∨/＜/＞を追加 | 2003/03/04 |
| 2 | 4 | ➢ PAN SW<br>「Layer Status:Master の Ch10 MUTE Key で On/Off 切替。」を追加<br>➢ SEND A<>E SW<br>「Layer Status:Master の Ch9-10 REC/SEL/MUTE Key で On/Off 切替。」を追加<br>➢ SHIFT SW<br>「LCD SW2 で On/Off 切替。」を追加<br>➢ Bank / Channel select<br>「Layer Status:Master の Ch11-12 SEL/MUTE Key で操作。」「DAW 側からの Bank / Channel select コマンド受信によって On/Off 表示する。」を追加。<br>表のボタン画像を差し替え。<br>➢ MIX / EDIT SW<br>➢ ZOOM SW<br>➢ ∧/∨/＜/＞ SW<br>項目追加 | 2003/03/04 |
| 3 | 6 | ➢ Parameters<br>SHIFT,MIX,EDIT,ZOOM,∧/∨/＜/＞を追加<br>➢ Cursor position transition<br>画面差し替え | 2003/03/04 |




## DM-24 Logic Environment
## Instructions for PC

This "DM-24 Template PC" file provides you with two powerful tools for integrating Emagic's Logic sequencing software with TASCAM's DM-24 digital console. It requires Logic 4.5 or higher.

DM-24 MIXER MACRO

The first tool is a Logic environment macro that appears as a visual representation of various DM-24 functions. Macros are a single Logic environment object that are actually comprised of many different objects packed together. Ultimately this allows you to view things such as fader position, mute status, panning, and preset recall of effects and snapshots. Also, the status of these functions will automatically update on screen as you change setting on the DM-24. You can also grab controls on Logic's environment screen, and watch the DM-24 immediately respond as well. Although this looks cool, and is sure to impress your friends, the real power is in being able to automate these functions within Logic's sequencer. Getting the DM-24 macro installed into your Logic session requires a few steps. Logic has to be made aware that the DM-24 exists in your system, and this is accomplished by simply copying the macro from this downloaded session file, and pasting it into your Logic session. You'll probably want to paste the macro into your autoload session, so that the DM-24 will be present in any new sessions you create.

1. It is necessary to have bi-directional MIDI communication between Logic and the DM-24. Connect a MIDI cable from an output of your MIDI interface to the MIDI IN of the DM-24, and from the MIDI OUT of the DM-24 to an input of your MIDI interface.
2. Launch Logic. This should automatically create a new session from your autoload template.
3. Go to the windows heading, and select "Open Environment".
4. In the Environment window, select "options", and go down to where it says "Import Environment", and then select "Layer...".
5. Logic now asks you to locate the file from which you want to import the environment layer. Locate and select the "DM-24 template PC" file on your drive.
6. It now asks you to choose the layer you want to import. Select the "DM-24" layer, and press "Import". Now select "Exit".
7. You should now see the DM-24 macro on your screen, along with a small object name "DM-24 Output" Click on the DM-24 Output object, and in the object attributes area, select the MIDI port output you have the DM-24

connected to.
8. Now we need to split the signal coming from the "Physical Input" in Logic's environment to go to both the "Sequencer Input" and to the "DM-24". The Physical Input object is most likely in the "Click & Ports" Environment layer. Under the Environment Tools box, you will see a pull down menu that currently says "DM-24". Click and hold down the mouse button, and scroll to the "Click & Ports" option. The environment screen will now change.
9. Under the "New" heading, select the "Monitor" option. This creates a new object that we are going to use to split the output of the "Physical Input".
10. An object called "Physical Input" will have a virtual cable connecting it to another object. Click and hold this cable, and then reconnect it to the Monitor object you just created.
11. The monitor has a small arrow in the upper right hand corner. Click and hold down the mouse. This creates another virtual patch cable. Connect this cable to the object that the Physical Input used to be connected to. Do this by dragging the cable to that object.
12. The monitor object should now have a second small arrow in the upper right hand corner. You'll use this to split the signal to the DM-24 macro. Because the DM-24 is on a different environment layer, hold down the Alt key before clicking the arrow.
13. This pulls up a list of all objects, in all layers. Select the DM-24. This automatically routes this cable to the DM-24 on its layer.

You're done! Moving faders on the DM-24 environment layer, should cause the faders on the DM-24 itself to react. Inversely, if you move the DM-24 controls, the environment should reflect it.
If you want to automate these controls, create a sequencer track in Logic, and select the DM-24 as the track destination.
With regards to the effect processors on the DM-24, you can only recall effects that have been mapped via the MIDI mapping function located in the MIDI section of the DM-24.

***Please Note*** The default DM24 mixer setup is for the second fader layer (17-32) to have channel 25-32 set up as four stereo pairs. In this case channels 26, 28, 30, & 32 on the Logic mixer will have no corresponding function with the DM-24. If these channels are unlinked, you must manually reassign proper MIDI channel assignments for faders, pans, and mutes on the DM-24 for those channels, in order for them to respond to the Logic mixer. This is done in the MIDI control setup page of the DM-24.

DM-24 HYPER EDIT SET

The second tool this file provides you with is a predefined Hyper Edit set. This allows for the graphical representation of all DM-24 functions you automate into Logic. There is no import function for Hyper Edit Sets from within Logic, however you can copy a set from one Logic session to another. Follow the procedure below.

1. Assuming you're already in your autoload session, go to the File heading and select "Open". Logic asks if you want to close the existing file. Select "Don't Close".
2. Select the "DM-24 Template PC" file from your drive.
3. Go to Windows, and select "Open Hyper Edit". This will display the Hyper Edit Set.
4. Under the Hyper menu option, select "Select All Event Definitions".

5. Then select under the Hyper menu, "Copy Even Definition".
6. Now Go to the Windows menu, and at the bottom it will list both active sessions. Select the original autoload session.
7. Go back to Windows, and select "Open Hyper Edit".
8. If asked whether or not you want to "Open selected Folder or to Create a new Sequence", select "Create"
9. Once Hyper Edit window appears, go to the Hyper menu, and select "Create Hyper Set". A new set with a "Volume" event definition will appear.
10. Under the Hyper menu, select Paste. The copied event definition will appear.
11. Select the original event definition labeled "Volume" and delete it.
12. Double click the event definition name that says "MIDI Controls" (under the tool bar) and rename it "DM-24"

Your done! This Hyper edit set can be used with any DM-24 objects you create while automating. It's a great tool for manipulating automation data in a non real time time time time fashion.
Event Definitions that begin with the letter "v" refer to fader volume, with the respective channel number following. Letter "m" is for mutes, and letter "p" is for panning. Refer to Logic's manual for the details in how to use the Hyper Edit functions.
Save the changes to your autoload file, so your new DM-24 tools will be available with each new session.




**DM-24 LOGIC ENVIRONMENT**
**Instructions for Mac OS**

This DM-24 Template file provides you with two powerful tools for integrating Emagic's Logic sequencing software with Tascam's DM-24 digital console. It requires Logic 4.5 or higher.

DM-24 MIXER MACRO

The first tool is a Logic environment macro that appears as a visual representation of various DM-24 functions. Macros are a single Logic environment object, that are actually comprised of many different objects that are packed together. Ultimately this allows you to view things such as fader position, mute status, panning, and preset recall of effects and snapshots. Also, the status of these functions will automatically update on screen as you change setting on the DM-24. You can also grab controls on Logic's environment screen, and watch the DM-24 immediately respond as well. All though this looks cool, and is sure to impress your friends, the real power is in being able to automate these functions within Logic's sequencer. The advantage of getting the DM-24 macro installed into your Logic session requires a few steps. Logic has to be made aware that the DM-24 exists in your system, and this is accomplished by simply copying the macro from this downloaded session file, and pasting it into your Logic session. You'll probably want to paste the macro into your autoload session, so that the DM-24 will be present in any new session you create.

1. It is necessary to have bi-directional MIDI communication between Logic and the DM-24. Connect a MIDI cables from an output of your MIDI interface to the MIDI IN of the DM-24, and from the MIDI OUT of the DM-24 to an input of your MIDI interface.
2. Launch Logic. This should automatically create a new session from your autoload template.
3. Go to the windows heading, and select "Open Environment".
4. In the Environment window, select "options", and go down to where it says "Import Environment", and then select "Layer...".
5. Logic now asks you to locate the file from which you want to import the environment layer. Locate and select the "DM-24 template" file on your drive.
6. It now asks you to choose the layer you want to import. Select the

"DM-24" layer, and press "Import". Now select "Exit".
7. You should now see the DM-24 macro on your screen, along with a small object name "DM-24 Output" Click on the DM-24 Output object, and select the MIDI port output you have the DM-24 connected to.
8. Now we need to split the signal coming from the "Physical Input" in Logic's environment to go to both the "Sequencer Input" and to the "DM-24". The Physical Input object is most likely in the "Click & Ports" Environment layer. Under the Environment Tools box, you will see a pull down menu that currently says "DM-24". Click and hold down the mouse button, and scroll to the "Click & Ports" option. The environment screen will now change.
9. Under the New heading, select the "Monitor" option. These creates a new object that we are going to use to split the output of the "Physical Input".
10. A long object called "Physical Input" will have a virtual cable connecting it to another object (most likely the sequencer input). Click and hold this cable, and then reconnect it to the Monitor object you just created.
11. The monitor has a small arrow in the upper right hand corner. Click and hold down the mouse, this creates another virtual patch cable. Connect this cable to the object that the Physical Input used to be connected to. Do this by dragging the cable to that object.
12. The monitor object should now have a second small arrow in the upper right hand corner. You'll use this to split the signal to the DM-24 macro. Because the DM-24 is on a different environment layer, hold down the option key before clicking the arrow.
13. This pulls up a list of all the environment layers. Select the DM-24 layer, in which it now shows the DM-24 itself. Select it. This automatically routes this cable to the DM-24 on its layer.

You're done! Moving faders on the DM-24 environment layer, should cause the faders on the DM-24 itself to react. Inversely, If you move the DM-24 controls, the environment should reflect it.
If you want to automate these controls, create a sequencer track in Logic, and select the DM-24 as the track destination.
With regards to the effect processors on the DM-24, you can only recall effects that have been mapped via the MIDI mapping function located in the MIDI section of the DM-24.
***Please Note*** The default DM24 setup is for the second fader layer (17-32) to have channel 25-32 set up as four stereo pairs. In this case channels 26, 28, 30, & 32 on the Logic mixer will have no corresponding function with the DM-24. If these channels are unlinked, you must manually reassign proper MIDI channel assignments for faders, pans, and mutes on the DM-24 for those channels, in order for them to respond to the Logic mixer. This is done in the MIDI control setup page of the DM-24.

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The second tool this file provides you with is a predefined Hyper Edit set. This allows for the graphical representation of all DM-24 functions you automate into Logic. There is no import function for Hyper Edit Sets from within Logic, however you can copy a set from one Logic session to another. Follow the procedure below.

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2. Select the "DM-24 Template" file from your drive.
3. Go to Windows, and select "Open Hyper Edit". This will display the Hyper Edit Set.
4. Under the Hyper menu option, select "Select All Event Definitions".
5. Then select under the Hyper menu, "Copy Even Definition".
6. Now Go to the Windows menu, and at the bottom it will list both active sessions. Select the original autoload session.
7. Go back to Windows, and select "Open Hyper Edit".
8. If asked whether or not you want to "Open selected Folder or to Create a new Sequence", select "Create"
9. Once Hyper Edit window appears, go to the Hyper menu, and select "Create Hyper Set". A new set with a "Volume" event definition will appear.
10. Under the Hyper menu, select Paste. The copied event definition will appear.
11. Select the original event definition labeled "Volume" and delete it.
12. Double click the event definition name that says "MIDI Controls" (under the tool bar) and rename it "DM-24"

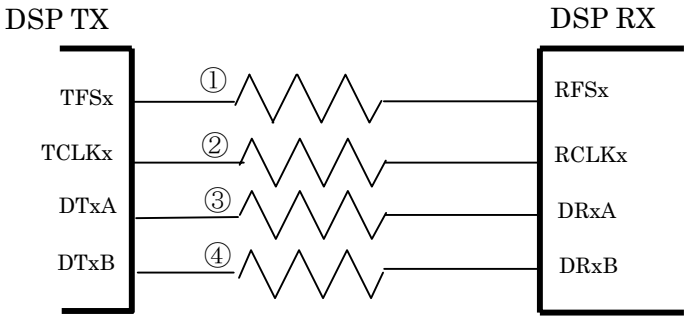
Your done! This Hyper edit set can be used with any DM-24 objects you create while automating. It's a great tool for manipulating automation data in a non real-time fashion.
Event Definitions that begin with the letter "v" refer to fader volume, with the respective channel number following. Letter "m" is for mutes, and letter "p" is for panning. Refer to Logic's manual for the details in how to use the Hyper Edit functions.
Save the changes to your autoload file, so your new DM-24 tools will be available with each new session.

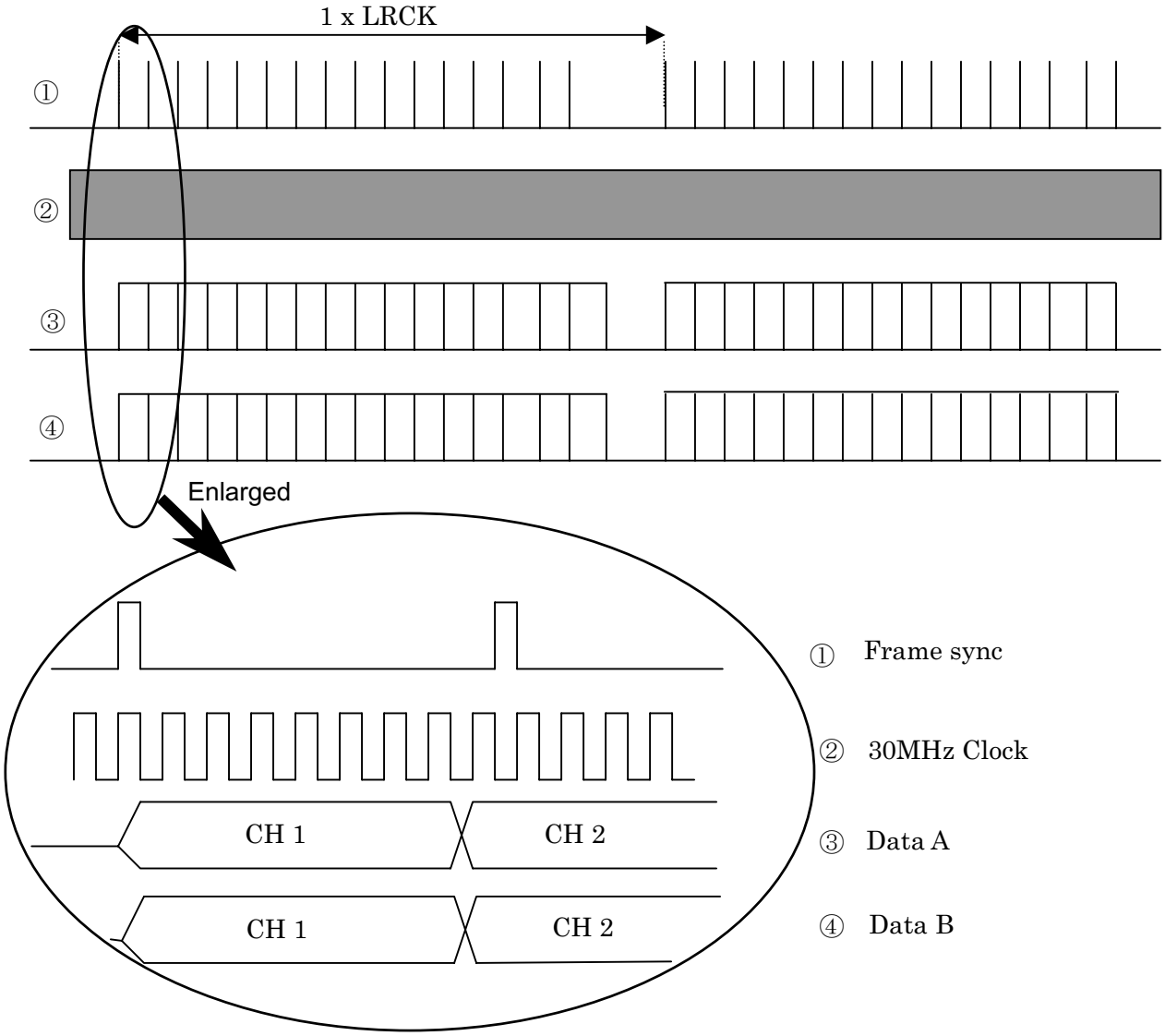
## DM-24, DSP Architecture

| | | |
|---|---|---|
| IOX | U71 | MTR1 (TDIF1 or SLOT1) in/out<br>MTR2 (TDIF2 or SLOT2) in/out |
| | U72 | MTR3 (TDIF3 or Adat) in/out<br>AK4527: Assignable RTN in/Assignable SENDN out |
| | U73 | AK5383: MIC/LINE in<br>AK4527: Stereo OUT / CROOM OUT / Studio OUT |
| DSP1 | U77 | IOX data in/out processor<br>Stereo fader<br>C. ROOM / Studio processor |
| DSP2 | U78 | Input Select processor<br>TRIM, Phase processor<br>Noise GATE/EXPANDER processor |
| DSP3 | U87 | Equalizer processor, Compressor processor<br>Digital input processor<br>Digital output processor |
| DSP4 | U88 | Equalizer processor, Compressor processor<br>C. ROOM (METER data) input processor, TB data in/out processor<br>Digital output processor |
| DSP5 | U94 | CH FADER processor<br>CH DELAY processor<br>AUX assign processor<br>SOLO assign processor<br>CH insert processor |
| DSP6 | U95 | BUSS assign processor<br>Stereo assign processor<br>TONE/SLATE processor<br>MASTER COMP processor<br>BUSS, AUX FADER processor |
| DSP7 | U106 | Effect processor |

Cascade DSP (IF-CS/DM)
In case the optional card, IF-CS/DM is installed, MASTER COMP processor and BUSS, AUX FADER processor of DSP6 are moved to this card.

## Operation of the Audio Serial Port



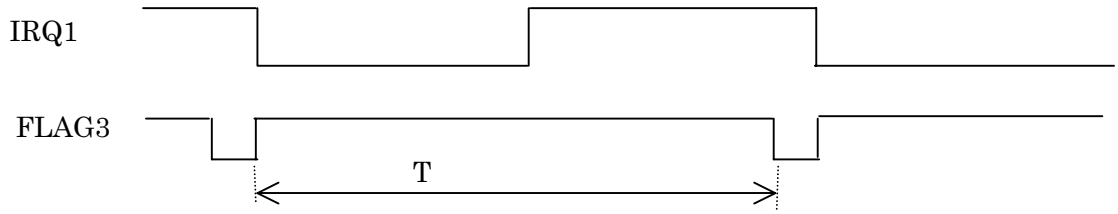
Audio serial port of the DSP consists of 4 data lines.
1. Frame sync
2. Clcok (30 MHz)
3. Data
4. Data

Each signal lines have a dumping resistor so that the signals can be measured by measured by the oscilloscope.

* DR1A/B, DT1A of U87/88 are the $I^2S$ format.

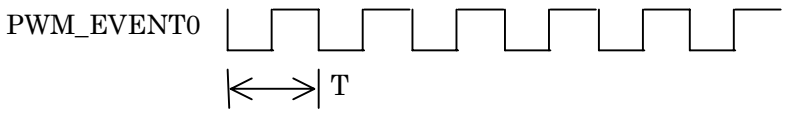
Other way to check the DSP

FLAG3 (pin 201) can be used to confirm the operation of the DSP.
Each DSP's runs the mixer program with a trigger of the IRQ1 falling down edge.
Mixer program is operated during "T" that starts at rising edge and finishes at falling down edge of the FLAG3. IRQ1 signal is equaled to inverted signal of LRCK.

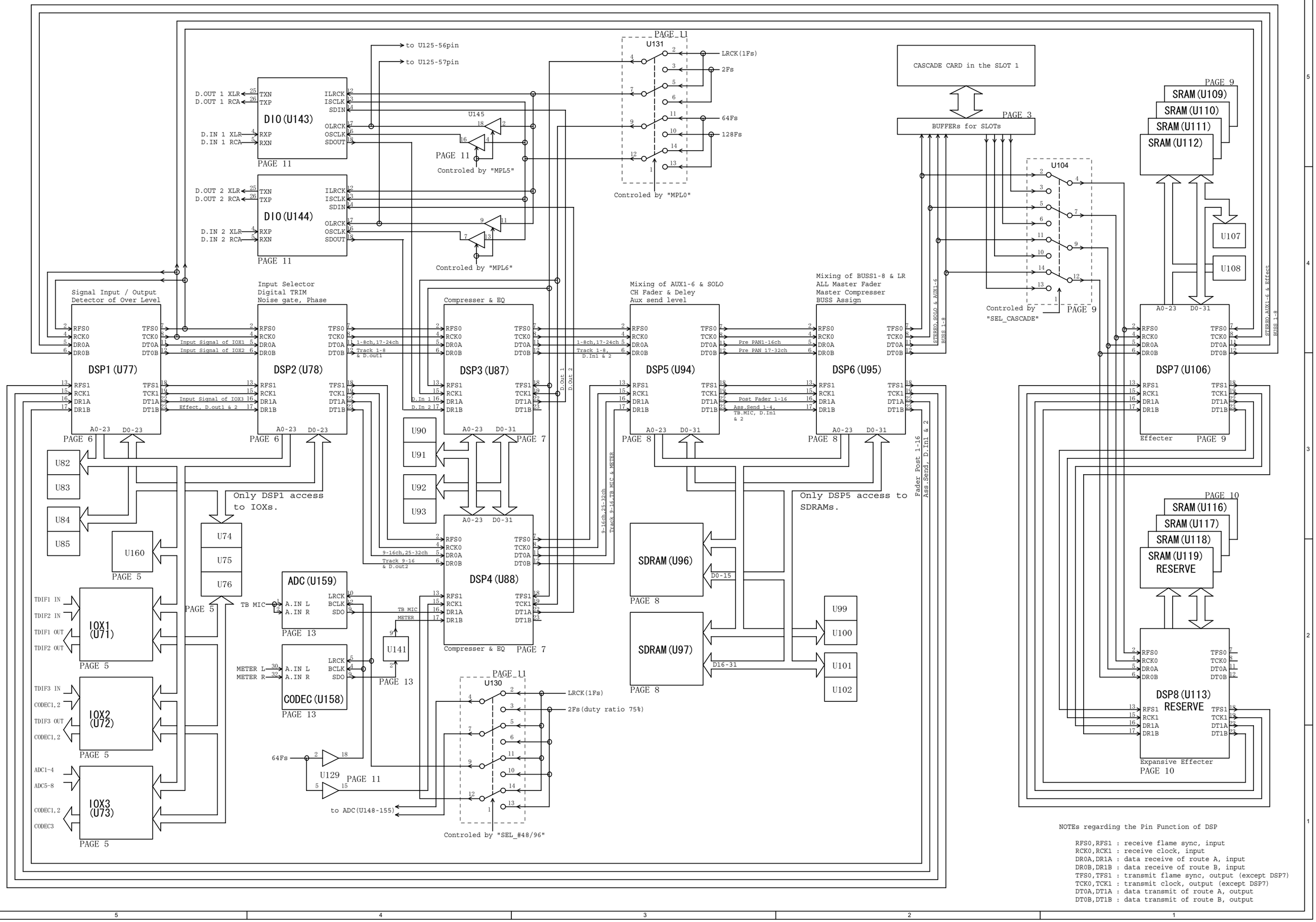



* U87 outputs the Fader touch sense clock when the fader is touched by a finger.

At PWM_EVENT0 (pin 26) or R160, there is a pulse waveform observed.
Interval of "T" is a reciprocal number of the frequency defined at OPTION/SET UP/FADER SENSITIVITY



# DM-24 DSP BLOCK DIAGRAM




NOTEs regarding the Pin Function of DSP

RFS0,RFS1 : receive flame sync, input
RCK0,RCK1 : receive clock, input
DR0A,DR1A : data receive of route A, input
DR0B,DR1B : data receive of route B, input
TFS0,TFS1 : transmit flame sync, output (except DSP7)
TCK0,TCK1 : transmit clock, output (except DSP7)
DT0A,DT1A : data transmit of route A, output
DT0B,DT1B : data transmit of route B, output

**TASCAM digital MIXER DM-24 DSP architecture** 2001/01/10

