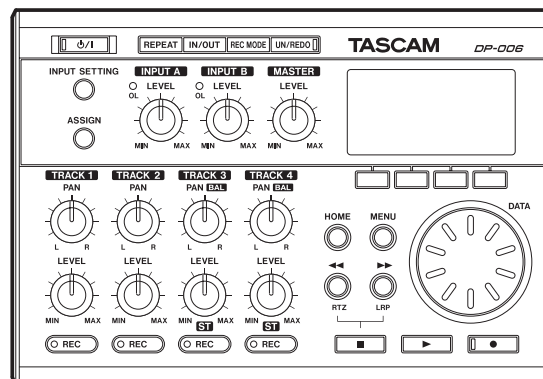
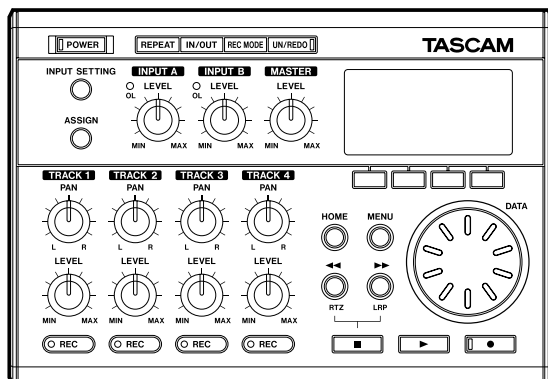


# TASCAM



## SERVICE MANUAL

# DP-004

Portable 4-Track Digital Pocketstudio

# DP-006

Digital Multitrack Recorder

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### INSTRUCTIONS FOR SERVICE PERSONNEL

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

# 1. Specifications

## 仕様

### Audio input/output ratings

#### INPUT A

Terminal:	Standard phone jack, Unbalanced
Input impedance:	10k $\Omega$ min. (with INPUT A selectable switch set to MIC/LINE) 1M $\Omega$ (with INPUT A selectable switch set to GUITAR)
Standard input level:	-10 dBV
Maximum input level:	+6 dBV
Headroom:	16 dB

#### INPUT B

Terminal:	Standard phone jack, Unbalanced
Input impedance:	10k $\Omega$ min.
Standard input level:	-10 dBV
Maximum input level:	+6 dBV
Headroom:	16dB

### Head Phone/LINE OUT output

Terminal:	3.5 mm mini-phone jack (stereo)
-----------	---------------------------------

#### When line is connected

Standard output level:	-16 dBV
Maximum output level:	0 dBV

#### When headphone is connected

Maximum output level:	15 mW + 15 mW (when 32 $\Omega$ headphone is connected)
-----------------------	--

### Audio performance

Frequency response:	INPUT (MIC/LINE) $\rightarrow$ LINE OUT: 20 Hz to 20 kHz
Distortion:	INPUT (LINE) $\rightarrow$ LINE OUT: 0.05% max.
S/N ratio:	INPUT (MIC/LINE) $\rightarrow$ LINE OUT: 75 dBV max.

### General

Recording media:	SD card (512 MB - 2 GB) or SDHC card (4 GB - 32 GB)
File system	
MTR partition:	TASCAM original
FAT partition:	FAT32
Battery life:	About 8 hours (Record mode) About 8.5 hours (Music playback mode) (when measured with alkaline batteries. Battery life may vary depending on the operating conditions)
Operating temperature range:	5 - 35 $^{\circ}$ C
Power consumption:	1 W

### オーディオ入出力定格

#### INPUT A

端子:	標準ホンジャック・不平衡
入力インピーダンス:	10k $\Omega$ 以上 (INPUT A 切換スイッチを "MIC/LINE" に設定時) 1M $\Omega$ (INPUT A 切換スイッチを "GUITAR" に設定時)
基準入力レベル:	- 10dBV
最大入力レベル:	+ 6dBV
ヘッドルーム:	16dB

#### INPUT B

端子:	標準ホンジャック・不平衡
入力インピーダンス:	10k $\Omega$ 以上
基準入力レベル:	- 10dBV
最大入力レベル:	+ 6dBV
ヘッドルーム:	16dB

### Head Phone/LINE OUT 出力

端子:	3.5mm ミニホンジャック (ステレオ)
-----	-----------------------

#### ライン接続時

基準出力レベル:	- 16dBV
最大出力レベル:	0dBV

#### ヘッドホン接続時

最大出力レベル:	15mW + 15mW (32 $\Omega$ ヘッドホン接続時)
----------	---------------------------------------

### オーディオ性能

周波数特製:	INPUT (MIC/LINE) $\rightarrow$ LINE OUT: 20Hz $\sim$ 20kHz
歪率:	INPUT (LINE) $\rightarrow$ LINE OUT : 0.05% 以下
S/N 比:	INPUT (MIC/LINE) $\rightarrow$ LINE OUT: 75dBV 以下

### 一般

記録媒体:	SD カード (512M バイト $\sim$ 2G バイト) および SDHC カード (4G バイト $\sim$ 32G バイト)
ファイルシステム	
MTR パーティション:	TASCAM オリジナル
FAT パーティション:	FAT32
電池持続時間:	約 8 時間 (JEITA 録音時) 約 8.5 時間 (JEITA 音楽再生時) (アルカリ乾電池使用時。使用状況により変動することがあります。)
使用温度範囲:	5 $\sim$ 35 $^{\circ}$ C
消費電力:	1W

Dimensions: 155.0 (W) x 33.5 (H) x 107.0 (D)mm  
(w/o projections)

Weight: 360 g (w/o batteries)

外形寸法： 155.0(幅)× 33.5(高さ)× 107.0(奥行)mm  
(突起部含まず)

質量： 360g (電池を含まず)

### Optional accessories

AC adapter: PS-P520

### 別売アクセサリ

ACアダプター： PS-P520

### Computer requirements

Windows Pentium 300 MHz or faster  
128 MB or more memory  
USB (USB 2.0 recommended)

Macintosh: Power PC, iMac, G3, G4 266 MHz or faster  
64 MB or more memory  
USB port (USB 2.0 recommended)

Recommended USB host controller  
Intel chipset

### Supported OS

Windows: Windows 2000 SP4 or later, Windows XP, Windows Vista and Windows 7 (DP-006)

Macintosh: Mac OS X 10.2 or later (DP-004)  
Mac OS X 10.4.6 or later (DP-006)

### 接続するパソコンの条件

Windows マシン： Pentium 300MHz 以上  
128MB 以上の Memory  
USB ポート (推奨：USB2.0)

Macintosh マシン： Power PC、iMac、G3、G4  
266MHz 以上  
64MB 以上の Memory  
USB ポート (推奨：USB2.0)

推奨 USB ホストコントローラー：

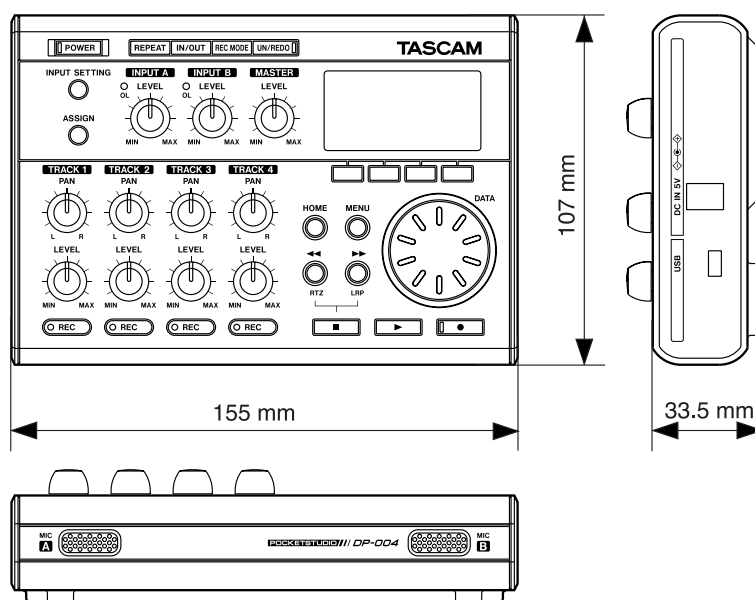
Intel 製チップセット

サポート OS

Windows: Windows 2000 SP4 以上、  
Windows XP、Windows Vista、  
Windows 7 (DP-006)

Macintosh: Mac OS X 10.2 以上 (DP-004)  
Mac OS X 10.4.6 以上 (DP-006)

### Dimensions(寸法図)



## 2. Test Mode

### テストモード

The DP-004/006 is provided with a test mode that lets you run diagnostic checks on the hardware.

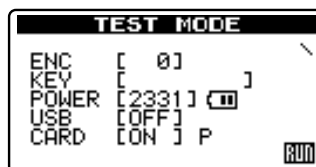
This mode is for use in factory and servicing and is not accessible by users.

#### 1. How to enter test mode

While holding down the **REC1+REC3+STOP** keys, switch the power on.

#### 2. Displays explained

When the test mode starts up, the following are displayed:



- |            |  |            |  |
|------------|--|------------|--|
| •ENC [ 0]: | DATA encoder (0-999)<br>You can determine whether or not each of the three encoders is in order.                               | •ENC[ 0] : | DATA エンコーダ (0～999)<br>エンコーダが正常に動作しているかを<br>確認可能            |
| •KEY [ ]:  | Shows the name of a key pressed.<br>You can determine whether or not a switch pressed is in order.                             | •KEY[ ] :  | 押されたキーの名称を表示<br>押されたキーが正常に認識されている<br>かを確認可能                |
| •POWER :   | Power supply voltage (4095 steps)<br>"BAT" shown when powered on battery;<br>"AC" shown when connected to an AC outlet.        | •POWER :   | 電源供給電圧 (4095 段階)<br>バッテリー時: <b>BAT</b> / AC 接続時: <b>AC</b> |
| •USB :     | USB connection   | •USB :     | USB 接続認識   |
| •CARD :    | Card detection   | •CARD :    | カード検出 ("P": カードプロテクトが<br>ON の時のみ表示)                        |
| •"/":      | This is an event acceptance indicator.<br>Normally, this indicator is still and rotates<br>when a key is operated for example. | •"/":      | イベント受付インジケータ<br>通常は停止、キーなど操作すると回転                          |

#### 3. Checking LEDs

When a key is pressed, its name is displayed in "KEY [ ]" and, at the same time, the associated LED turns on solid or blinks on the PANEL PCB, allowing you to check whether they work dependably.

##### 1) General

- |            |                          |
|------------|--------------------------|
| <b>F1:</b> | all on                   |
| <b>F2:</b> | blinking at higher speed |
| <b>F3:</b> | blinking at normal speed |
| <b>F4:</b> | all off                  |

For the LED associated with a key, it turns on solid when a key is pressed and starts blinking when holding down the key for a certain time.

\*Use care when pressing the **POWER** key, for holding it down for a certain time switches off the power of the unit.

##### 2) Others

- |              |  |
|--------------|--|
| <b>OL A:</b> | turns on when the <b>REPEAT</b> key is pressed.  |
| <b>OL B:</b> | turns on when the <b>UN/REDO</b> key is pressed. |

DP-004/006 ではハードウェアの自己診断が可能なテストモードを備えています。

このモードは生産、サービス用モードであり一般公開はしません。

#### 1. TEST MODE の起動方法

「**REC1+REC3+STOP**」キーを 3 個同時に押しながら電源を投入します。

#### 2. 画面の説明

起動画面後に下記の LCD 表示となります。

#### 3. LED 確認

**KEY [ ]** で押されたキーの名称を表示すると同時に PANEL PCB 上の LED も点灯もしくは点滅し、正常に点灯するか否かの確認が可能となります。

##### 1) 一般

- |             |      |
|-------------|------|
| <b>F1 :</b> | 全灯   |
| <b>F2 :</b> | 早い点滅 |
| <b>F3 :</b> | 通常点滅 |
| <b>F4 :</b> | 全消灯  |

キーとセットで設置してある LED に関してはキーを押すと LED が点灯し、一定時間以上押し続けると点滅します。

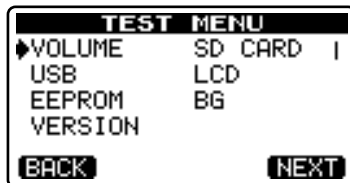
※ **POWER** キーは押し続けると本体の電源が切れますので注意してください。

##### 2) その他

- |               |                      |
|---------------|----------------------|
| <b>OL A :</b> | <b>REPEAT</b> キーで点灯  |
| <b>OL B :</b> | <b>UN/REDO</b> キーで点灯 |

## 4. Menu

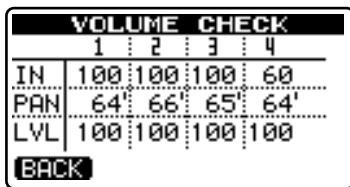
Pressing the **MENU** key reveals the following menu.



- **REW/FF** KEY: cursor movement
- **F4(NEXT)** KEY: mode selection
- **F1(BACK)** KEY: back to the TOP screen

### 1) VOLUME

Select "**VOLUME**" and press **F4(NEXT)** key and the following are displayed:

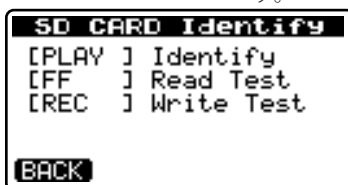


When rotating a potentiometer, the number display changes, allowing you to check whether the potentiometer is operating correctly.

- **IN-1, IN-2:** INPUT A, B
- **IN-3:** MASTER
- **IN-4:** HEADPHONE VOLUME
- **PAN:** PAN
- **LVL:** LEVEL

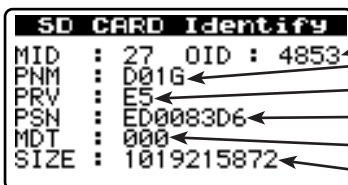
### 2) SD CARD

Select "**SD**" and press **F4(NEXT)** key and the following are displayed:



**Identify:** Read in data from the card.

Pressing the **PLAY** key indicates the following information:



Pressing the **F1** key returns the display to the previous screen.

## 4. MENU

**MENU** キーを押すと下記メニューを表示します。

- **REW/FF** キー: 項目の移動。
- **F4(NEXT)** キー: 項目の選択。
- **F1(BACK)** キー: TOP 画面へ。

### 1) VOLUME

"**VOLUME**" を選択して **F4(NEXT)** キーを押すと下記画面を表示します。

各対応 VR を回すとその数値が変化して、VR が正常に読み取り出来ているかを確認できます。

- **IN-1, IN-2:** INPUT A, B
- **IN-3:** MASTER
- **IN-4:** HEADPHONE VOLUME
- **PAN:** PAN
- **LVL:** LEVEL

### 2) SD CARD

"**SD**" を選択して **F4(NEXT)** キーを押すと下記画面を表示します。

**Identify:** カードから情報の読み込み

**PLAY** キーを押すと下記の情報を表示します。

- Manufacturer ID
- OID : OEM/Application ID
- Product name
- Product revision
- Product serial number
- Manufacturing date
- Raw Size

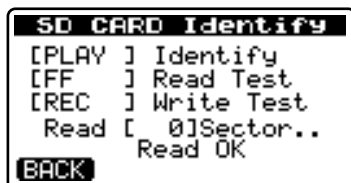
**F1** キーを押すと元の画面に戻ります。

**Read Test:** Read in data from the card per sector

At each press of the **FWD** key, data is read in from the card per sector.

**Read Test :** カードから 1 セクタ読み込み

**FWD** キーを押すと、押すたびにカードから 1 セクタ毎のデータの読み込みを行ないます。



**Write Test: Card write test.**

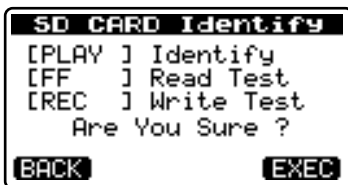
Press the **REC** key to advance to the following screen.

Press the **F4 (EXEC)** key to execute the Write Test.

**Write Test :** カードへの書き込みテスト

**REC** キーを押すと、下記画面を表示します。

**F4(EXEC)** キーを押すと書き込みテストが実行されます。

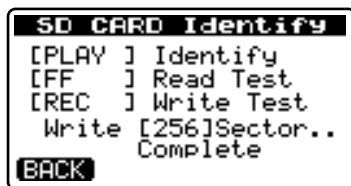


The following screen is displayed when the write test completes successfully.

書込テストが正常終了すると下記画面が表示されます。

\*Note that executing the Write Test results in clearing the data on the SD card as well as the format.

※ Write Test を実行しますと SD CARD 上のデータは消去され、フォーマットもクリアされますので注意してください。



**3) USB Check**

Select "**USB**" and press **F4(NEXT)** key and the following are displayed:

Each time the **ENTER** key is pressed, the indication alternates between ON and OFF.

ON indicates that USB connected, and OFF indicates that USB is disconnected.

**3) USB チェック**

"**USB**" を選択して **F4(NEXT)** キーを押すと下記画面を表示します。

**ENTER** キーを押すたびに ON/OFF を繰り返します。

ON 表示で USB 接続、OFF 表示で USB 切断となります。



**4) LCD Check**

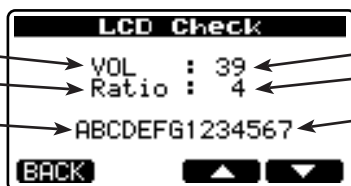
Select "**LCD**" and press **F4(NEXT)** key and the following are displayed:

Contrast adjustment (**F3**: +; **F4**: -)  
 adjustment(**FWD**(▶▶): +; **REW**(◀◀): -)  
 Characters for after-image check

**4) LCD チェック**

"**LCD**" を選択して **F4(NEXT)** キーを押すと下記画面を表示します。

コントラスト調整 (**F3** : + , **F4** : -)  
 コントラスト調整傾き  
 ( **REW** : - , **FF** : + )  
 残像確認用キャラクタ



**STOP** key : Reverse

**STOP** キー : 反転

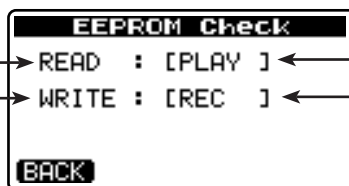
## 5) EEPROM Check

Select "**EEPROM**" and press **F4(NEXT)** key and the following are displayed:

Read in from the ROM

Writing all zeros to the ROM

The writing process starts at a press of the **F4(EXEC)** key in response to "**Are you sure?**" To cancel the process, press the **F1(BACK)** key.



PLAY :ROM の読み込み実行。

REC :ROM のオールゼロ書き込み。

"Are you sure?" 後に **F4(EXEC)** で書き込み。 **F1(BACK)** でキャンセル。

If errors occur during either the read or the write, the following are displayed:

- Timeout Err :** No response from the EEPROM
- Error :** Errors at data send/receive time
- Verify Err :** Errors in verification during the write process

## 6) BG

Select "**BG**" and press **F4(NEXT)** key, and the background sample screen is displayed.

The screen contains four pictures.

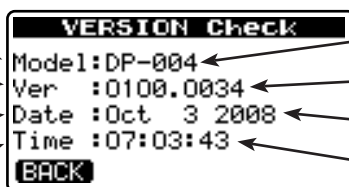
- FWD** key: To move forward.
- REW** key: To move backward.

Pressing **F1** key returns the display to the MENU screen.

## 7) VERSION Check

Select "**VERSION**" and press **F4(NEXT)** key, and the following are displayed, in which the detailed version information on the firmware can be confirmed.

Model Name(DP-004 or DP-006)  
Version of the system firmware.  
The last 4 digits indicate a build number  
on which the system firmware was built.  
which the system firmware was built



モデル名 (DP-004 or DP-006)

システムファームのバージョン

後半の4桁はビルド番号  
ファームビルド日付

ファームビルド時刻

## 5) EEPROM チェック

"EEPROM" を選択して **F4(NEXT)** キーを押すと下記画面を表示します。

READ/WRITE 共に、エラーの場合には下記を表示する。

- Timeout Err :** EEPROM の応答なし
- Error :** データ送信 / 受信時のエラー
- Verify Err :** Write 時のペリファイエラー

## 6) BG

"BG" を選択して **F4(NEXT)** キーを押すと背景サンプル画面を表示します。

4 枚の絵があります。

- FWD** キー: 進む
- REW** キー: 戻る

**F1** キーで MENU 画面に戻ります。

## 7) VERSION チェック

"VERSION" を選択して **F4(NEXT)** キーを押すと下記画面を表示され、ファームウェアの詳細 Version 確認が可能となります。

## 3. Updating Firmware

### ファームウェアのアップデート

#### 1. Preparations

- 1) Make the connection between this unit and the PC using a USB cable.
- 2) Place the update file in the **UTILITY** folder in the unit.
- 3) Perform the USB device "**remove**" action on the PC, and then switch off the power to the unit.

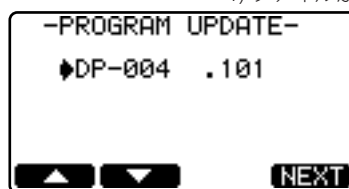
#### 2. START-UP

While holding down the **REPEAT** and **UN/REDO** keys, switch the power on.

#### 3. Displays explained

The following screen is displayed initially after start-up.

- 1) When only a single file is available:



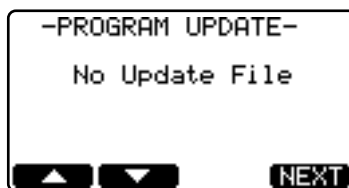
- 2) When multiple files are available:



The maximum number of display lines is 4.

If a file contains a larger number of lines than the maximum number of displayable lines, the cursor can be moved using **F1/F2** keys or the dial.

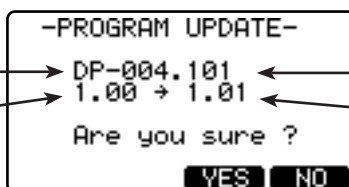
- 3) When no update file is available:  
Nothing can be done.



#### 4. File confirmation

Press the **F4(NEXT)** key .

Name of the file selected  
Current version at left and  
New version at right



選択したファイル名  
左：現バージョン 右：新バージョン

#### 5. Getting update started

Press the **F3 (YES)** or **F4 (NO)** key.

- 1) When **F3 (YES)** key is pressed:  
Updating is started.

#### 1. 準備

- 1) 本体と PC を USB ケーブルで接続します。
- 2) アップデートファイルを本体の「UTILITY」フォルダに置きます。
- 3) PC で USB デバイスの「取り外し」を行い、PC から切り離れた後、本体の電源を落とします。

#### 2. 起動

**REPEAT + UN/REDO** キーを押しながら電源を投入します。

#### 3. 画面の説明

起動後に下記の表示となります。

- 1) ファイルが一つの場合

- 2) ファイルが複数の場合

表示行は最大 4 行です。

表示最大行を超えるファイルがある場合は **F1** キーと **F2** キーまたはダイヤルでカーソルが移動します。

- 3) ファイルが無い場合  
何も操作できません。

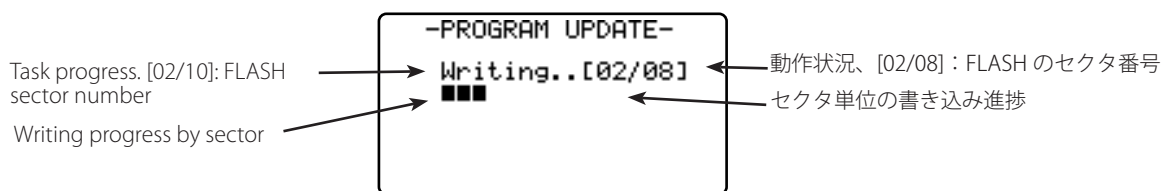
#### 4. ファイルの確認

**F4(NEXT)** キーを押します。

#### 5. アップデート実行

**F3(YES)** キーか **F4(NO)** キーを押します。

- 1) **F3(YES)** キーを押した場合  
アップデートを実行します。

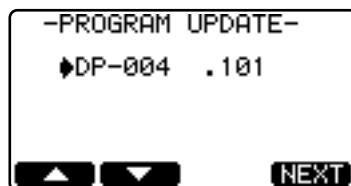


2) When **F4 (NO)** key is pressed:

Update is not started and the display returns to the file selection screen shown above.

2) **F4(NO)** キーを押した場合。

アップデートを実行せず、ファイル選択画面へ戻ります。



## 6. Completion

After "**Complete**" and "**POWER OFF**" are displayed, the unit switches OFF automatically.

Switch the power of the unit again and confirm the version.

## 7. Error messages

1) If an error occurs when selecting a file, the following messages appear:

Messages(メッセージ)	Meaning(内容)
<b>Product</b>	The product ID of the file does not match (the file may be for other products).
	ファイルのプロダクト ID が一致しない (別製品のファイルの可能性もある)。
<b>Old Version</b>	The file version is older than the current one.
	現バージョンよりもファイルのバージョンが古い。
<b>Checksum</b>	The checksum does not match.
	ファイルのチェックサムが一致しない。
<b>Update File</b>	Error in file reading.
	ファイル読み込みエラー。

2) If an error occurs in the data rewriting process, the following messages appear:

2) 書き換え時にエラーが発生した場合のメッセージ

Messages(メッセージ)	Meaning(内容)
<b>Flash Erase</b>	Error in erasing
	消去エラー
<b>Flash Blank</b>	Blank error as a result of data erasure.
	消去後のブランクエラー
<b>Flash Write</b>	Error in writing.
	書き込みエラー
<b>Flash Verify</b>	Error in verification after data has been written.
	書き込み後のベリファイエラー

## 4. How to initialize SD CARD

### SD カードの初期化方法

When an SD card malfunctions, for example if the MOUNT ERROR occurs immediately after start-up, the SD card can be initialized as described below.

Initialization can also be executed on a normal SD card.

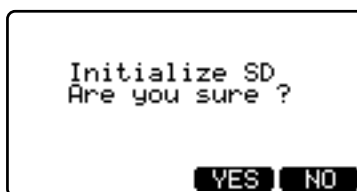
\*Initializing an SD card erases all of the data in it.

#### 1. Start-up

While holding down the **REPEAT+INPUT SETTING** keys, switch the power on.

#### 2. Confirmation

The screen for confirming the initialization is displayed.



#### 3. Getting Initialization Started

Press the **F3 (YES)** or **F4 (NO)** key.

1) When **F3 (YES)** key is pressed:

The normal startup screen is displayed, and the SD card initialization is executed.

\*The screen is displayed for a relatively long period due execution of the SD card initialization.



When the SD card initialization completes, the home screen is displayed.



2) When **F4 (NO)** key is pressed:

The normal start up screen is displayed, and then the home screen is displayed without initializing the SD card.



起動時に MOUNT ERROR になってしまうなど、正常に動作できなくなった SD CARD を強制的に初期化する方法です。

正常な SD CARD に対して実行することもできます。

※この操作を行うと SD CARD 内のデータはすべて消去されます。

#### 1. 起動方法

**REPEAT** キー + **INPUT SETTING** キーを押しながら電源を投入します。

#### 2. 確認画面

Initialize をするかどうか確認する画面が表示されます。

#### 3. 実行

**F3(YES)** キーか **F4(NO)** キーを押します。

1) **F3(YES)** キーの場合

通常起動画面となり、SD CARD 初期化処理を実行します。

※ SD CARD 初期化処理実行のため、この画面表示時間がやや長くなります。

SD CARD 初期化処理を終了すると、HOME 画面が立ち上がります。

2) **F4(NO)** キーの場合

通常起動画面となり、SD CARD 初期化処理をしないで HOME 画面が立ち上がります。

## 5. Messages Explained

### メッセージ一覧

The following popup messages alert you to conditions that may arise while you are using the unit. Consult this table if you see something you do not understand.

以下のポップアップメッセージの一覧表を示します。  
DP-004/006 では状況に応じたポップアップメッセージが表示されますが、それぞれのメッセージの内容を知りたいとき、および対処方法を知りたいときにこの表をご覧ください。

#### 1. General Error (一般的エラー)

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>Empty Export Track</b>	You are trying to export a track which does not have anything recorded on it. Pick another track to export.
	「エクスポートトラックが空っぽです。」 何も録音されていないトラックをエクスポートしようすると表示されます。別のトラックをエクスポートしてください。
<b>File Not Found</b>	You are trying to restore a song when there are no backed-up songs on the FAT partition.
	「ファイルが見つかりません。」 FATパーティションにバックアップされたソングがないときに、ソングをリストアしようすると表示されます。
<b>I/O Too Short</b>	You are trying to enter repeat mode, but the time between the IN and OUT points is too short. Make the time longer.
	「IN ポイントと OUT ポイントが近すぎます。」 リピートモードに入ろうとするとときに IN ポイントと OUT ポイントが近すぎると表示されます。 IN ポイントと OUT ポイントを 2 フレーム以上離してください。
<b>Import File Not Found</b>	You are trying to import a WAV file from the FAT partition when there are no WAV files there. Connect the unit to a PC and transfer some files to the FAT partition for import.
	「インポートするファイルが見つかりません。」 WAV ファイルのない FAT パーティションから WAV ファイルをインポートしようとしています。 本機をパソコンに接続して、インポートするファイルをパソコンから本機の FAT パーティションに転送してください。
<b>Import File Too Large</b>	You are trying to import a WAV file from the FAT partition that is too large for the remaining space on the partition. Free up some space on the (native) partition and try again.
	「インポートするファイルが大きすぎます。」 アクティブパーティションの空きスペースより容量の大きい WAV ファイルを FAT パーティションからインポートしようとしています。アクティブパーティション内の不要なファイルを削除して空きスペースを増やしてから再度インポートを試みてください。
<b>In Bounce Mode</b>	You tried to perform an action that cannot be done while in Bounce mode.
	「バウンスモード中です。」 バウンスモード中に禁止操作をしようとしたときに表示されます。
<b>In Master Mode</b>	You tried to perform an action that cannot be done while in Master mode.
	「マスタリングモード中です。」 マスタリングモード中に禁止操作をしようとしたときに表示されます。
<b>In Repeat Mode</b>	You tried to perform an action that cannot be done while in Repeat mode.
	「リピートモード中です。」 リピートモード中に禁止操作をしようとしたときに表示されます。
<b>Master Track Not Found</b>	You have tried to export a mastered mix track when the song does not have one. Master the song and then export the mix.
	「マスタートラックが見つかりません。」 ステレオマスターがソング内に録音されていないときにステレオマスターをエクスポートしようすると表示されます。 ソングをマスタリングしてから、ステレオマスターをエクスポートしてください。

Messages( メッセージ )	Meaning and response( 内容と対処方法 )
<b>Master Track Too Large</b>	You tried to export a master track which was too large for the remaining space on the FAT partition . Connect the unit to a computer and free up some space on the FAT partition.
	「マスタートラックが大きすぎます。」 FATパーティションの空き容量より大きなステレオマスターをエクスポートしようとしています。 本機をパソコンに接続して、FATパーティションの空きスペースを拡げてください。
<b>No Disk Space</b>	You tried to create a song, but there is not enough space on the partition to create a song. Free up some space and try again.
	「ディスクスペースがありません。」 パーティションパーティションに十分な空きスペースがないときにソングを作成しようとすると、このメッセージが表示されます。 スペースを拡げてからソングを作成してください。
<b>No Master Trk</b>	You have tried to use a non-existent master track as the source in a track cloning operation. Select another source or master the song and try again.
	「マスタートラックが存在しません。」 トラックのクローンを作るとき、存在しないマスタートラックをソースとして選択しようとする则表示されます。 マスタートラックを作るか、または別のソースを選択してください。
<b>No Song</b>	You are trying to load a song from a partition that has no songs on it. Change partitions.
	「ソングがありません。」 ソングが存在しないパーティションからソングをロードしようとしています。 パーティションを変更してください。
<b>No Undo Histroy</b>	There are no actions to be undone.
	「アンドゥのヒストリーがありません」 アンドゥするような操作が存在しません。
<b>History 900!!</b>	The number of items in the Undo History has exceeded 900. Clear the Undo History because the Work Memory is about to become full.
	Undo History が 900 個を越えたときに警告として表示されます。 Work Memory Full になる寸前ですので、History クリアを実行してください。
<b>Not Stopped</b>	The transport is moving (not stopped, but playing back, recording, etc.) and you have pressed a key such as the UN/REDO key which cannot be used until you press STOP.
	「レコーダーが停止していません。」 レコーダーが停止していないとき、たとえば UN/REDO キーのように停止中でないと受け付けられないキーを押すと、このメッセージが表示されます。
<b>Now Recording</b>	You are trying to perform an action which cannot be done while recording.
	「レコーディング中です。」 レコーディングを行っているときにメニュー操作を行おうとすると表示されます。他にもレコーディング中に受け付けられない操作があります。
<b>Same Track</b>	You cannot clone a track to itself.
	「同じトラックを指定しています。」 クローントラック設定で、"Src Trk" と "Dst Trk" とで同じトラックを指定すると表示されます。
<b>Song Protected</b>	The song is protected and you are trying to change it (record or edit, etc.). Unprotect the song.
	「ソングがプロテクトされています。」 プロテクトされているソングに変更（録音、編集など）を加えようとする则表示されます。変更を加える前にプロテクトを解除してください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>Too Many songs</b>	You have 250 songs on one partition. You must delete some before you can create another song.
	「これ以上ソングを作成できません。」 一つのパーティションが持つことができるソングの数は最大 250 です。不要なソングを削除してから、新しいソングを作成してください。
<b>Track Full</b>	You are trying to import a file from the FAT partition to a track that has already been recorded to . You can only import to a blank track.
	「トラックが録音済みです。」 FAT パーティションからすでに録音されているトラックにファイルをインポートしようとする则表示されます。
<b>Trk Too Short</b>	You are trying to master with the OUT point at the zero position. Set the OUT point and try again.
	「トラックが短すぎです。」 ゼロポジションを OUT ポイントに設定してマスタリングを行おうとすると表示されます。 OUT ポイントを設定し直してください。
<b>No SD Card! Please set a SD</b>	Insert an SD card after turning off the unit.
	「SD カードが挿入されておりません。」 電源をオフにしてから SD カードを挿入してください。
<b>Not Continued</b>	This error occurs during SONG BACKUP or SONG RESTORE. The song data is destroyed or normal access to the FAT area failed.
	SONG BACKUP または SONG RESTORE 中のエラーです。 SONG データが壊れているか、FAT エリアに正常アクセスができなかった場合に表示されます。
<b>It's Too Lage</b>	The FAT area does not have enough remaining space for SONG BACKUP. Move the files in the FAT area to the PC using the USB connection or save the files in the FAT area and then reformat it.
	SONG BACKUP 時に FAT 空き容量が足りない場合に表示されます。 USB 接続して FAT エリアにあるファイルを PC へ移動するか、FAT 上のファイル保存後 FAT REFORMAT してください。
<b>Invalid Card</b>	Insert another SD card after turning off the unit, or format the card by MENU → CARD → FORMAT.
	「挿入されている SD カードは DP-004 (or DP-006) で使用できないフォーマットです。」 電源をオフにしてから別の SD カードを挿入するか、MENU → CARD から FORMAT してください。
<b>Protected Card</b>	To record or edit, turn off the unit and un-protect the SD card.
	「挿入されている SD CARD はプロテクトされています。」 録音や編集を行いたい場合は、電源を OFF して SD カードのプロテクトを解除してください。
<b>Card Full</b>	The SD card is full during recording. Erase the unnecessary songs or use another SD card.
	「録音中に SD カードがいっぱいになりました。」 不要な SONG を ERASE するか、SD カードを交換してください。
<b>Trk Edit Fail</b>	Save the song and turn the unit off and then on, and perform track edit again.
	「トラックエディットに失敗しました。」 ソングを保存してから本体の電源を入れ直して再度トラックエディットを実行してください。
<b>Battery Empty</b>	Replace the batteries with new ones or use a PS-P520 AC adapter (sold separately).
	「電池が空です。」 電池がほとんど空の状態の時に表示されます。 新しい電池に交換するか、別売の AC アダプター (PS-P520) を接続してご使用ください。
<b>Battery Low</b>	Replace the batteries with new ones or use a PS-P520 AC adapter (sold separately).
	「電池が空に近いです。」 電池が空に近い状態で録音しようとする则表示されます。 新しい電池に交換するか、別売の AC アダプター (PS-P520) を接続してご使用ください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>SD Size Error</b>	Use an SD card larger than 512 MB.
	「DP-004 (or DP-006) では使用できない小さいサイズのSDカードが挿入されています。」 512Mバイト以上のSDカードをご使用ください。
<b>Work Memory Full</b>	Even if the card has enough remaining memory space, this error may occur when you record a long song or edit a lot. You may be able to continue the work if you clear the history which may increase the open work memory. You may also be able to continue work by turning the unit off and then on again, which may inclears the open work memory.
	「ソングの録音や編集のために必要なワークメモリがいっぱいになりました。」 SDカードの空き容量が残っていても、1ソングでの長時間録音を行ったり、編集作業を多く行うと発生する場合があります。 ヒストリのクリアを実行すると空きワークメモリが増え、作業が継続できる場合があります。 電源をオフすることでも空きワークメモリが増え、作業が継続できる場合があります。

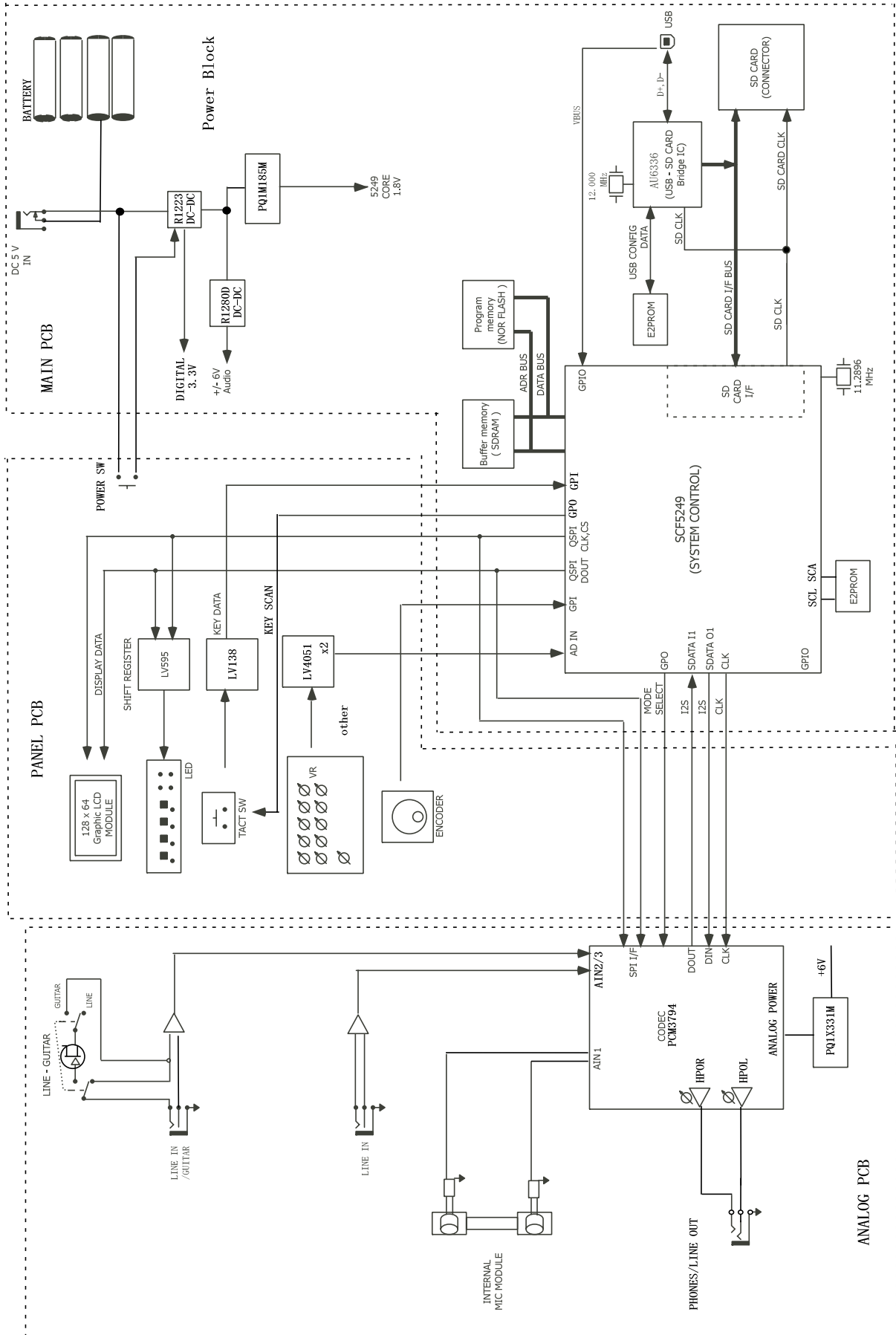
## 2. Fatal Error (致命的エラー)

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>SD Not Found</b>	The SD card cannot be recognized. Ensure that a normal card is inserted correctly and switch the power off then on again.
	SDカードが認識できませんでした。正常なSDカードが正しく挿入されていることを確認し、電源を入れ直してください。
<b>SD Read Busy</b>	The SD card read operation is delayed for the required processing. The card may be defective. Re-format it or use another SD card.
	SDカードからの読み込み時、処理が間に合わないなどのエラー。SDカード不良の可能性があります。カードフォーマットし直すか、別のSDカードを使用してください。
<b>SD Write Busy</b>	The SD card write operation is delayed for the required processing. The SD card may be defective. Re-format it or use another card.
	SDカードへの書き込み時、処理が間に合わないなどのエラー。SDカード不良の可能性があります。カードフォーマットし直すか、別のSDカードを使用してください。
<b>I/F Error</b>	The card does not respond or there is an error on the SD interface. The hardware or SD card may be defective.
	カードから応答が無いか、もしくはSDインターフェース上のエラー。 ハードウェア不具合、あるいはカード不良の可能性があります。
<b>No Memory Left</b>	An error occurred during the Track Edit operation. The song data is destroyed or normal access is impossible.
	Track Editでエラーが発生しました。 SONGデータが壊れているか正常にアクセスできない可能性があります。
<b>FileErr:XXXXXX</b>	Other irrecoverable error. "XXXXXX" is the number of the current step and indicates how far the processing has advanced till the error. The SD card may be defective. Re-format it or use another card.
	「その他の修復不可能なエラー」XXXXXXは処理がどこまで進んだかのステップを表す番号です。 SDカード不良の可能性があります。カードフォーマットし直すか、別のSDカードを使用してください。
<b>Audio Rst Fail</b>	Audio file system initialization error. The format in the SD card is destroyed or the card is defective. Re-format the SD card or use another card.
	Audio File System初期化エラー。SDカード内のフォーマットが壊れている、またはSDカード不良の可能性があります。 カードフォーマットし直すか、別のSDカードを使用してください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>SaveParam Fail</b>	Parameter save error. Check the card insertion and card protection status. Otherwise, the SD card may be defective.
	パラメータセーブエラー。SD カード挿入、カードプロテクトを確認してください。 SD カード不良の可能性もあります。
<b>Mount Error:XX</b>	Mount processing error. "XX" is the number of the current step indicating how far the processing has advanced till the error. The format in the SD card is destroyed or the card is defective. Re-format the SD card or use another card.
	マウントプロセスでのエラー。XX は処理がどこまで進んだかのステップを表す番号です。 SD カード内のフォーマットが壊れている、または SD カード不良の可能性もあります。 カードフォーマットし直すか、別の SD カードを使用してください。
<b>SD-Card Error!</b>	The SD card was ejected in the middle of recording or playback.
	録音・再生動作中に SD カードがイジェクトされた場合に表示されます。
<b>System Error code 1</b>	CPU access error. The firmware may be defective.
	CPU のアクセスエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 2</b>	CPU address error. The firmware may be defective.
	CPU のアドレスエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 3</b>	CPU instruction error. The firmware may be defective.
	CPU のインストラクションエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 4</b>	CPU zero division error. The firmware may be defective.
	CPU のゼロ除算エラー。ファームウェア不具合の可能性もあります。
<b>System Error code 5</b>	CPU Privilege Violation error. The firmware may be defective.
	CPU の Privilege Violation エラー。ファームウェア不具合の可能性もあります。
<b>System Error code 6</b>	CPU Unimplemented line-a opcode error. The firmware may be defective.
	CPU の Unimplemented line-a opcode エラー。ファームウェア不具合の可能性もあります。
<b>System Error code 7</b>	CPU Unimplemented line-f opcode error The firmware may be defective.
	CPU の Unimplemented line-f opcode エラー。ファームウェア不具合の可能性もあります。
<b>System Error code 8</b>	CPU format error. The firmware may be defective.
	CPU のフォーマットエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 9</b>	CPU Uninitialized Interrupt error. The firmware may be defective.
	CPU の Uninitialized Interrupt エラー。ファームウェア不具合の可能性もあります。
<b>Device Error</b>	An error occurred during the SD Identification. The hardware or SD card may be defective.
	SD カードの認識コマンドが失敗しました。ハードウェア不具合、あるいはカード不良の可能性もあります。

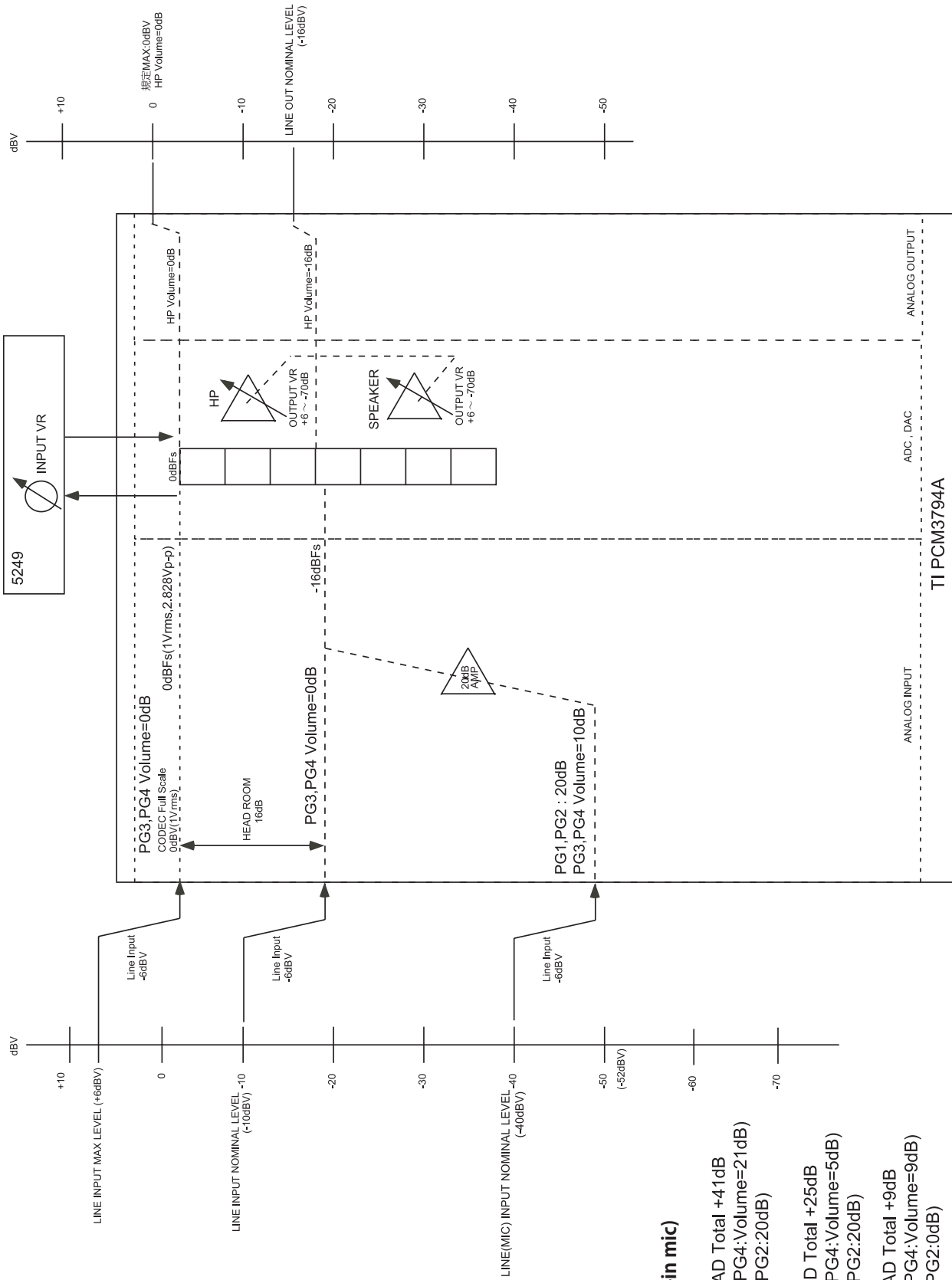
# 6. Block Diagram

## ブロックダイアグラム



# 7. Level Diagram

## レベルダイアグラム



**(The built-in mic)**

HIGH PAD Total +41dB  
 (PG3,PG4:Volume=21dB)  
 (PG1,PG2:20dB)

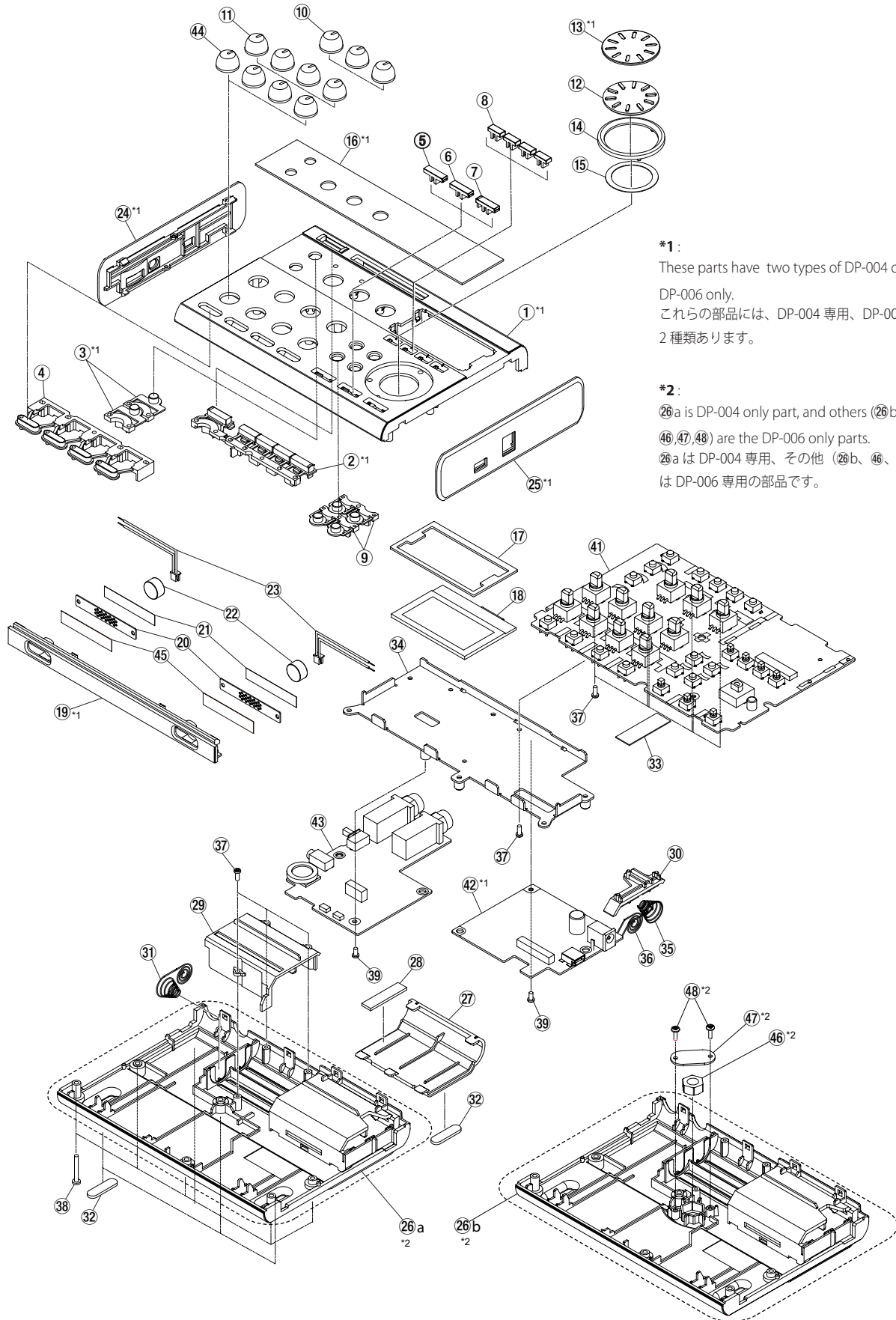
MID PAD Total +25dB  
 (PG3,PG4:Volume=5dB)  
 (PG1,PG2:20dB)

LOW PAD Total +9dB  
 (PG3,PG4:Volume=9dB)  
 (PG1,PG2:0dB)

# 8. Exploded Views and Parts List

## 分解図とパーツリスト

### Exploded View



**\*1:**  
These parts have two types of DP-004 only and DP-006 only.  
これらの部品には、DP-004専用、DP-006専用の2種類あります。

**\*2:**  
②6 a is DP-004 only part, and others (②6 b, ④6 ④7 ④8) are the DP-006 only parts.  
②6 aはDP-004専用、その他(②6 b、④6、④7、④8)はDP-006専用の部品です。

**CAUTION** Part with numbers in parentheses ( ) cannot be ordered.**注意** "()"付き品番は、発注できません。**Exploded View Parts List**

REF.NO.	PARTS NO.	DESCRIPTION	QTY	REMARKS
1-1	M02876900B	PANEL, TOP DP004 G	1	DP-004 only
	M02876950B	PANEL, TOP DP006 G	1	DP-006 only
1-2	M02877500A	BUTTON, A DP004 G	1	DP-004 only
	M02877510A	BUTTON, A DP006 G	1	DP-006 only
1-3	M02877600B	BUTTON, B DP004 G	2	DP-004 only
	M02877610A	BUTTON, B DP006 G	2	DP-006 only
1-4	M02877700A	BUTTON, C DP004 G	1	
1-5	M02877810C	BUTTON, D STOP DP004 G	1	
1-6	M02877820C	BUTTON, D PLAY DP004 G	1	
1-7	M02877900C	BUTTON, E DP004 G	1	
1-8	M02878000C	BUTTON, F DP004 G	4	
1-9	M02878100A	BUTTON, G DP004 G	2	
1-10	M02878500C	KNOB, VR DP004 ORG G	3	
1-11	M02878510C	KNOB, VR DP004 WHT G	4	
1-12	M02878600A	KNOB, JOG BASE DP004 G	1	
1-13	M02878700A	KNOB, JOG COVER DP004 G	1	DP-004 only
	M02878710A	KNOB, JOG COVER DP006 G	1	DP-006 only
1-14	M02878800A	KNOB, JOG RING DP004 G	1	
1-15	M02587500A	POLYEST SHEET, JOG MPGT1 G	1	
1-16	M02878900B	WINDOW, DP004 G	1	DP-004 only
	M02878910A	WINDOW, DP004 G	1	DP-006 only
1-17	M02879000A	CUSHION, LCD DP004 G	1	
1-18	E01381200A	LCD, KMC12864AC-00-SP A G	1	
1-19	M02877300B	ESCUTCHEON, DP004 G	1	DP-004 only
	M02877350B	ESCUTCHEON, DP006 G	1	DP-006 only
1-20	M02880600B	PLATE, MIC DP004 G	2	
1-21	M02880700A	SHEET, MIC DP004 G	2	
1-22	3E038410	MIC CONDENSER ECM-100 G	2	
1-23	E01534000A	HARN ASSY, MIC DP004 G	2	
1-24	M02877100B	PANEL, SIDE L DP004 G	1	DP-004 only
	M02877150B	PANEL, SIDE L DP006 G	1	DP-006 only
1-25	M02877200B	PANEL, SIDE R DP004 G	1	DP-004 only
	M02877250B	PANEL, SIDE R DP006 G	1	DP-006 only
1-26	M02877000B	PANEL, BOTTOM DP004 G	1	DP-004 only
	M02877050B	PANEL, BOTTOM DP006 G	1	DP-006 only
1-27	M02879100A	COVER, BATTERY A DP004 G	1	
1-28	M02904300A	CUSHION, BATTERY DP004 G	1	
1-29	M02879200A	COVER, BATTERY B DP004 G	1	
1-30	M02880200A	COVER, BATTERY C DP004 G	1	
1-31	M02666400A	SPRING, BATT CDXT2 G	1	
1-32	M02880800A	FOOT, DP004 G	4	
1-33	M02931700A	SHEET, PCB PANEL DP004 G	1	

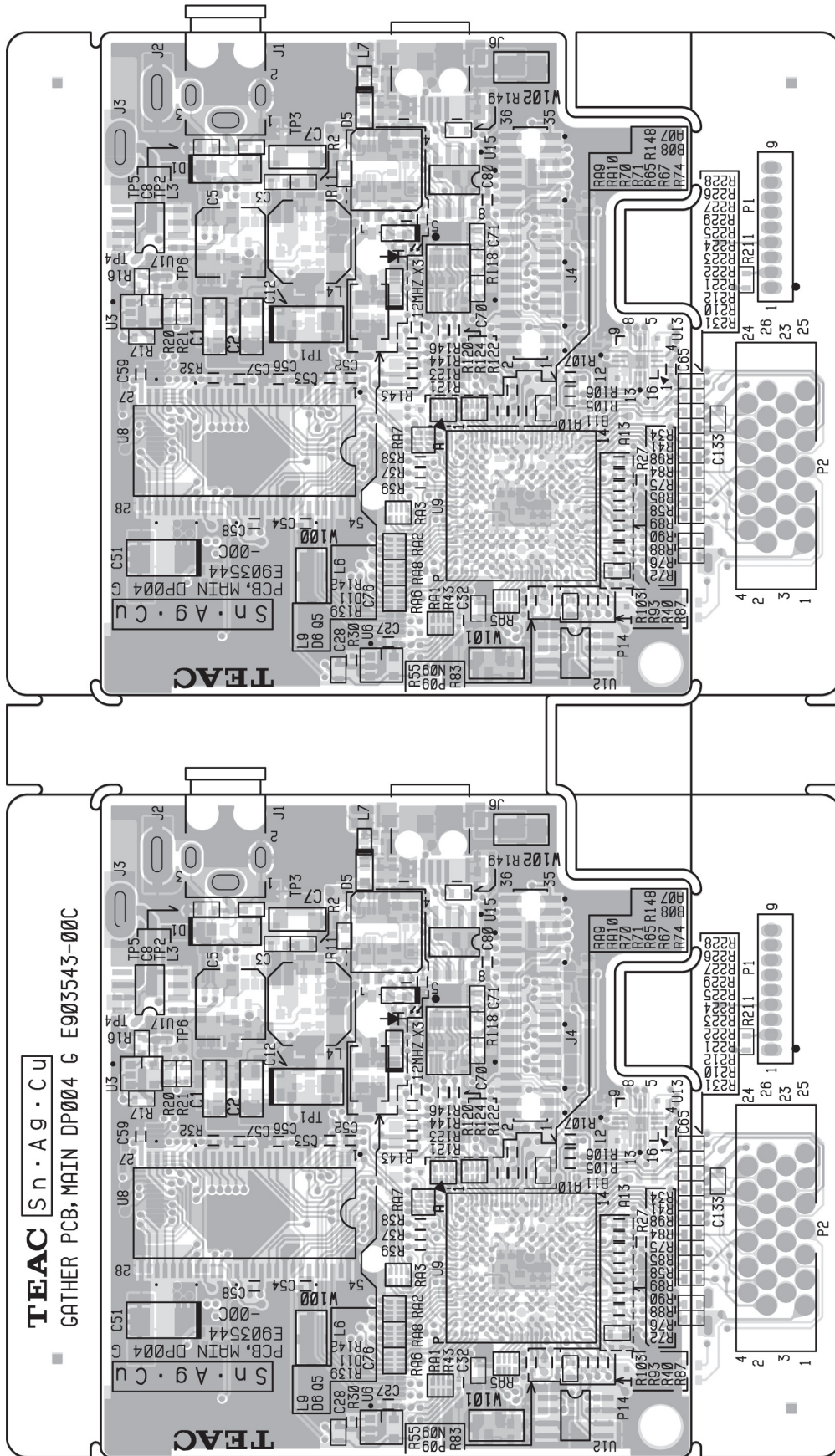
**CAUTION** Part with numbers in parentheses ( ) cannot be ordered.**注意** "()"付き品番は、発注できません。**Exploded View Parts List**

REF.NO.	PARTS NO.	DESCRIPTION	QTY	REMARKS
1-34	M02877400C	FRAME,MAIN DP004 G	1	
1-35	M02880300A	SPRING,BATTERY A DP004 G	1	
1-36	M02880400A	SPRING,BATTERY B DP004 G	1	
1-37	B00302606A	SCREW,BPB M2*6 FNI G	10	
1-38	B00311316A	SCREW,BPP 2*16 FZC G	6	
1-39	B00311704A	SCREW,BPA 2*4 FNI G	2	
1-39	B00311704A	SCREW,BPA 2*4 FNI G	2	
1-41	E95354000A	PCB ASSY,PANEL DP004 G	1	(See "GATHER PCB,PANEL DP004 G " on page 28.)
1-42	E95354400A	PCB ASSY,MAIN DP004 G	1	(See "GATHER PCB,MAIN DP004 G " on page 28.)
	E95466900A	PCB ASSY,MAIN DP006 G	1	(See "GATHER PCB,MAIN DP006 G " on page 28.)
1-43	E95354200A	PCB ASSY,ANA DP004 G	1	(See "GATHER PCB,ANA DP004 G " on page 28.)
1-44	M02878500C	KNOB,VR DP004 ORG G	4	DP-004 only
	M02878530B	KNOB,VR DP004 BLU G	4	DP-006 only
1-45	M03482900A	MESH,MIC DP006 G	2	DP-006 only
1-46	M02812600A	NUT,UNC 1/4-20 FNI G	1	DP-006 only
1-47	M03477700A	BRACKET,TRIPOD NUT G	1	DP-006 only
1-48	B00302606A	SCREW,BPB M2*6 FNI G	2	DP-006 only

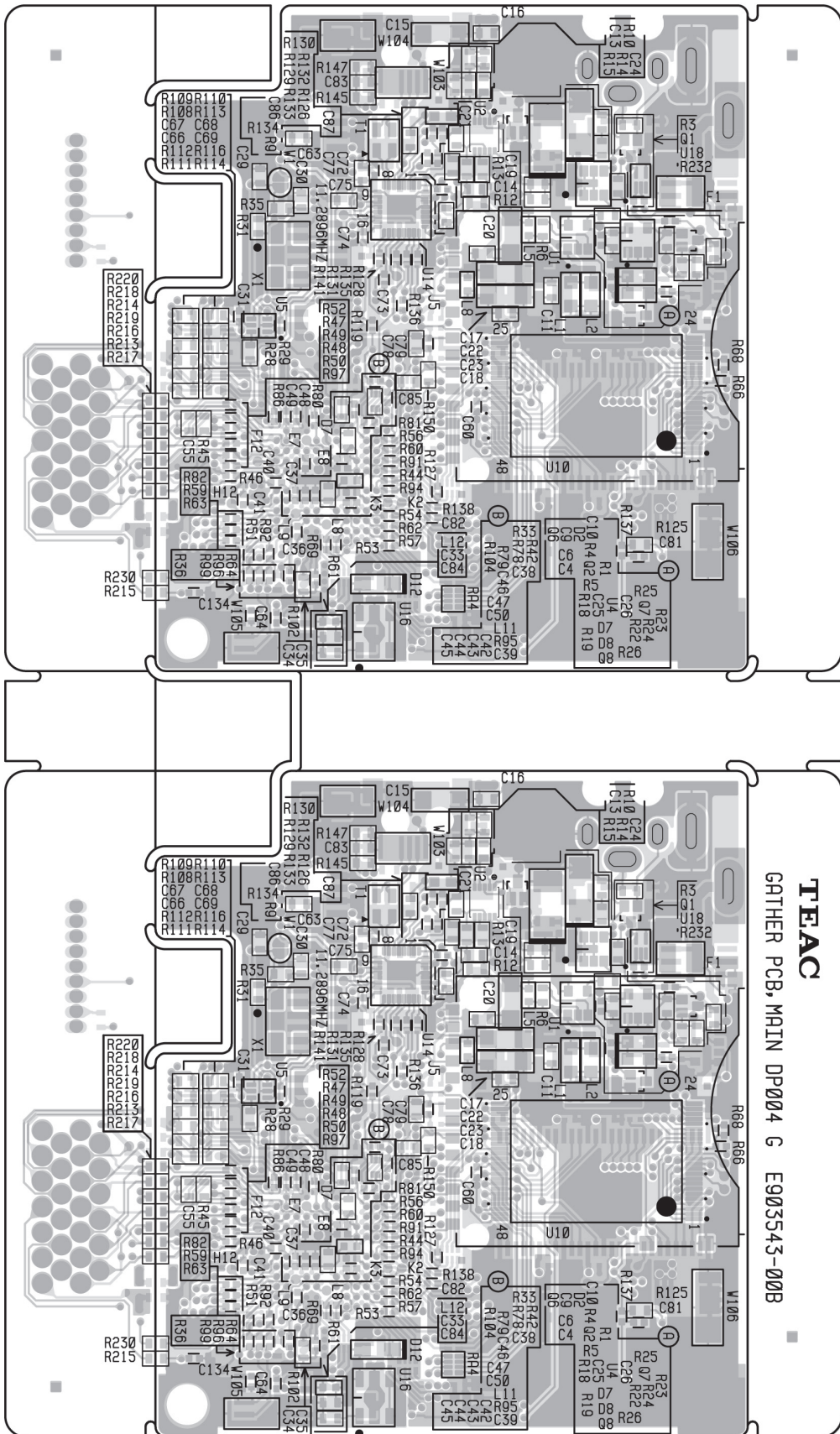
# 9. PC Boards and Parts List

基板図とパーツリスト

## MAIN PCB (Side A) DP004



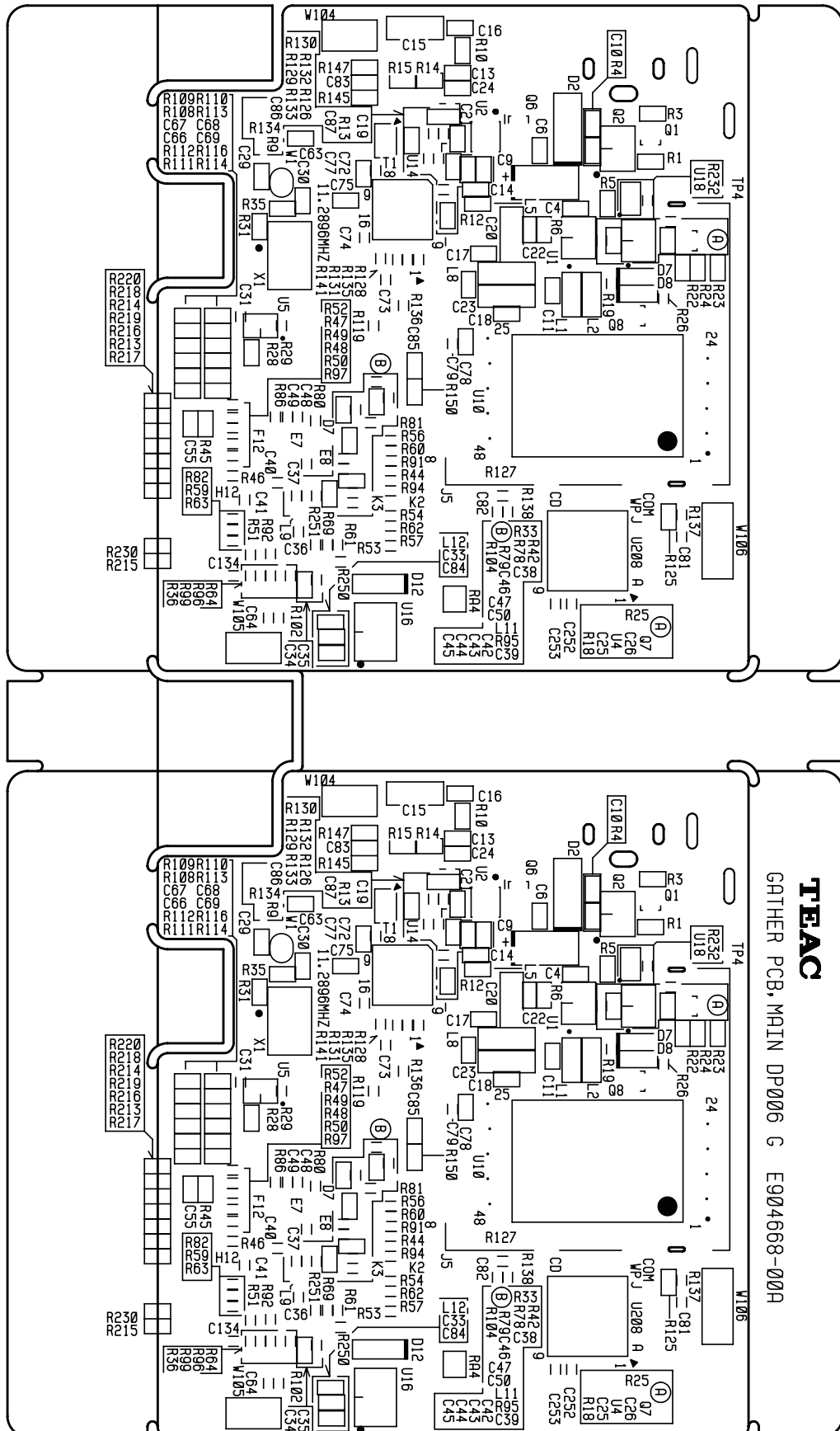
MAIN PCB (Side B) DP004



**TEAC**  
GATHER PCB, MAIN DP004 G E903543-00B



MAIN PCB (Side B) DP006

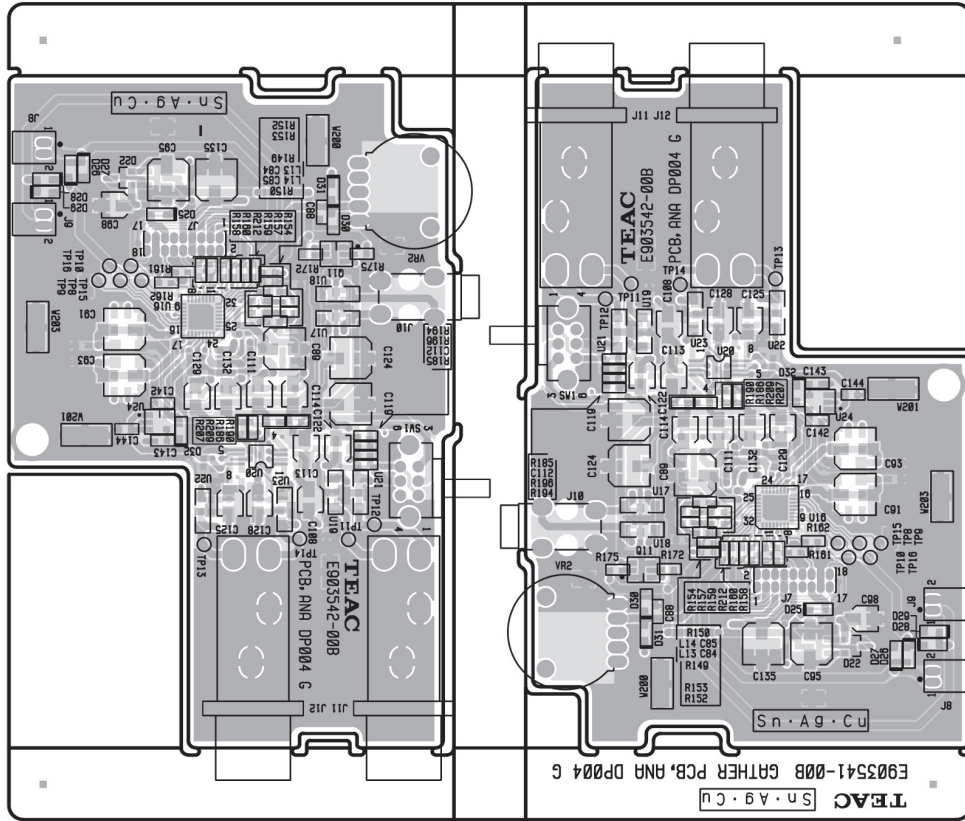


**TEAC**  
GATHER PCB, MAIN DP006 G E904668-00A

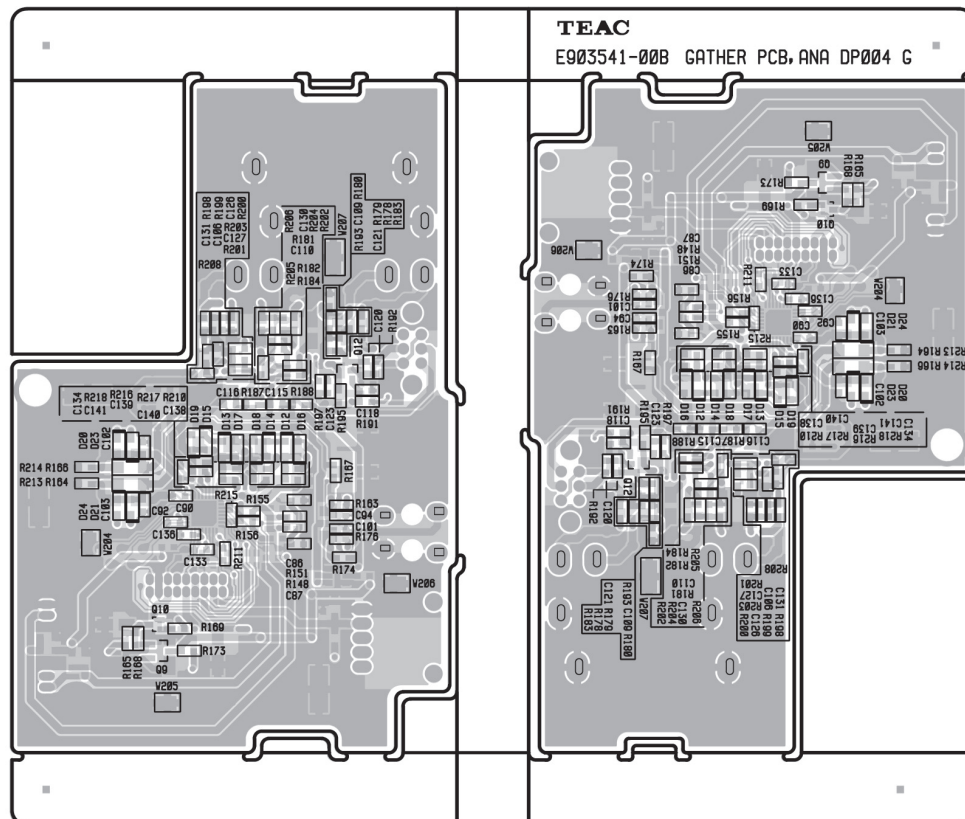




ANA PCB (Side A)



ANA PCB (Side B)



**CAUTION**

Part with numbers in parentheses ( ) cannot be ordered. If you want to order service parts, be sure to use "Child" part numbers (numbers in Bold), which refer to individual parts of a parent part.

**注意**

"()"付き品番は、発注できません。補修部品を発注する際は、太字品番で発注してください。

**GATHER PCB,MAIN DP004 G (DP-004 only)**

## メイン基板

PARTS NO.	DESCRIPTION	REMARKS
<b>E95354300A</b>	GATHER PCBA,MAIN DP004 G	[ JPN ] [ EUR ] [ T/C ]
(E95354400A)	PCB ASSY,MAIN DP004 G	[ JPN ] [ EUR ] [ T/C ]

**GATHER PCB,MAIN DP006 G (DP-006 only)**

## メイン基板

PARTS NO.	DESCRIPTION	REMARKS
<b>E95466800A</b>	GATHER PCBA,MAIN DP006 G	[ JPN ] [ EUR ] [ T/C ] [ CHI ]
(E95466900A)	PCB ASSY,MAIN DP006 G	[ JPN ] [ EUR ] [ T/C ] [ CHI ]

**GATHER PCB,ANA DP004 G (Common to DP-004 and DP-006)**

## アナログ基板

PARTS NO.	DESCRIPTION	REMARKS
<b>E95354100A</b>	GATHER PCBA,ANA DP004 G	[ JPN ] [ EUR ] [ T/C ] [ CHI ] ( [ CHI ]:DP-006 only )
(E95354200A)	PCB ASSY,ANA DP004 G	[ JPN ] [ EUR ] [ T/C ] [ CHI ] ( [ CHI ]:DP-006 only )

**GATHER PCB,PANEL DP004 G (Common to DP-004 and DP-006)**

## パネル基板

PARTS NO.	DESCRIPTION	REMARKS
<b>E95353900A</b>	GATHER PCBA,PANEL DP004 G	[ JPN ] [ EUR ] [ T/C ] [ CHI ] ( [ CHI ]:DP-006 only )
(E95354000A)	PCB ASSY,PANEL DP004 G	[ JPN ] [ EUR ] [ T/C ] [ CHI ] ( [ CHI ]:DP-006 only )

**WIRE Section (Common to DP-004 and DP-006)**

## ワイヤーセクション

PARTS NO.	DESCRIPTION	REMARKS
(E01534000A)	HARN ASSY,MIC DP004 G	[ JPN ] [ EUR ] [ T/C ]

# 10. Safety Parts

安全部品

## Safety Parts List

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
F1	E0017804	FUSE, ICP-S2.3 (-TN)	⚠

# 11. Included Accessories

付属品

## Included Accessories (DP-004)

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	D01054901B	OWNERS MNL,(J) DP004 G	[ JPN ]
	D01054920A	OWNERS MNL,(E) DP004 G	[ T/C ] [ EUR ]
	D01055980A	OWNERS MNL,QSG(D)DP004 G	[ EUR ]
	D01055981A	OWNERS MNL,QSG(F)DP004 G	[ EUR ]
	D01055982A	OWNERS MNL,QSG(I)DP004 G	[ EUR ]
	D01055983A	OWNERS MNL,QSG(S)DP004 G	[ EUR ]
	D00729700E	WARR CARD,(JPN) G	[ JPN ]
	D00822001C	WARR CARD,ENG/FRE C A G	[ EUR ]
	D01059900A	CARD,REGISTRATION T/C G	[ T/C ]
	D00819901B	DISTRIBUTOR LIST,WLD CA G	[ T/C ] [ EUR ]
	T0017950	SD CARD,SP002GSD045HMPC G	[ JPN ] [ T/C ] [ EUR ]
	E01892100A	USB CABLE,FMT-11-054 0.8M	[ JPN ] [ T/C ] [ EUR ]

## Included Accessories (DP-006)

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	D01175201A	OWNERS MNL,DP006 J G	[JPN]
	D01175220A	OWNERS MNL,DP006 E G	[T/C][EUR]
	D01175380A	OWNERS MNL,QSG DP006 G G	[EUR]
	D01175381A	OWNERS MNL,QSG DP006 F G	[EUR]
	D01175382A	OWNERS MNL,QSG DP006 I G	[EUR]
	D01175383A	OWNERS MNL,QSG DP006 S G	[EUR]
	D0118500A	SHEET,INSERTION ERP2 G	[JPN][T/C][EUR][CHI]
	D01173700A	WARR CARD,TASCAM G	[JPN][T/C][EUR][CHI]
	T0019950	MICROSD,PTA02045 G	[JPN][T/C][EUR][CHI]
	T0019840	MICROSD ADAPTER,PTA02041G	[JPN][T/C][EUR][CHI]
	E01892100A	USB CABLE,FMT-11-054 0.8M	[JPN][T/C][EUR][CHI]

## NOTES

- PC boards shown are viewed from parts side.
- Parts marked with \* require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in this manual.
- ⚠ Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.

[JPN]: JAPAN [T/C]: U.S.A./CANADA [KOR]: KOREA

[EUR]: EUROPE [UK]: U.K.

[AUS]: AUSTRALIA [TM]: TAIWAN

[CHI]: CHINA [EX/BR]: BRAZIL

## 注意

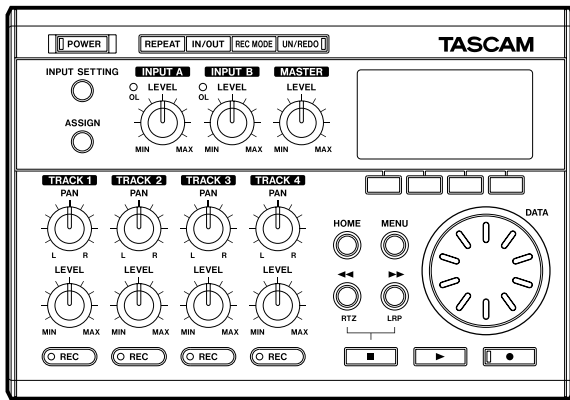
- プリント基板図は部品面を示しています。
- \*印の部品は納期が若干かかります。あらかじめご了承ください。
- 分解図に部番のない部品および品番のない部品は供給できません。
- 標準の抵抗、コンデンサーは省略してあります。回路図を参照してください。
- ⚠印は安全重要部品です。交換する時は必ず指定の部品を使用してください。
- 仕向先

[JPN]: JAPAN [T/C]: U.S.A./CANADA [KOR]: KOREA

[EUR]: EUROPE [UK]: U.K.

[AUS]: AUSTRALIA [TM]: TAIWAN

[CHI]: CHINA [EX/BR]: BRAZIL



**TASCAM**<sup>®</sup>  
TEAC PROFESSIONAL

## SERVICE MANUAL

# DP-004

## Portable 4-Track Digital Pocketstudio

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# 1. Specifications

## 仕様

### Audio input/output ratings

#### INPUT A

Terminal:	Standard phone jack, Unbalanced
Input impedance:	10k $\Omega$ min. (with INPUT A selectable switch set to MIC/LINE) 1M $\Omega$ (with INPUT A selectable switch set to GUITAR)
Standard input level:	-10 dBV
Maximum input level:	+6 dBV
Headroom:	16 dB

#### INPUT B

Terminal:	Standard phone jack, Unbalanced
Input impedance:	10k $\Omega$ min.
Standard input level:	-10 dBV
Maximum input level:	+6 dBV
Headroom:	16dB

### Head Phone/LINE OUT output

Terminal:	3.5 mm mini-phone jack (stereo)
• When line is connected	Standard output level: -16 dBV Maximum output level: 0 dBV
• When headphone is connected	Maximum output level: 15 mW + 15 mW (when 32 $\Omega$ headphone is connected)

### Audio performance

• Frequency response:	INPUT (MIC/LINE) $\rightarrow$ LINE OUT: 20 Hz to 20 kHz
• Distortion:	INPUT (LINE) $\rightarrow$ LINE OUT: 0.05% max.
• S/N ratio:	INPUT (MIC/LINE) $\rightarrow$ LINE OUT: 75 dBV max.

### General

• Recording media:	SD card (512 MB - 2 GB) or SDHC card (4 GB - 32 GB)
• File system	MTR partition: TASCAM original FAT partition: FAT32
• Battery life:	About 8 hours (Record mode) About 8.5 hours (Music playback mode)
	(when measured with alkaline batteries. Battery life may vary depending on the operating conditions)
• Operating temperature range	5 - 35 $^{\circ}$ C
• Power consumption:	1 W

### オーディオ入出力定格

#### INPUT A

端子:	標準ホンジャック・不平衡
入力インピーダンス:	10k $\Omega$ 以上 (INPUT A 切換スイッチを"MIC/LINE" に設定時) 1M $\Omega$ (INPUT A 切換スイッチを"GUITAR" に設定時)
基準入力レベル:	-10dBV
最大入力レベル:	+ 6dBV
ヘッドルーム:	16dB

#### INPUT B

端子:	標準ホンジャック・不平衡
入力インピーダンス:	10k $\Omega$ 以上
基準入力レベル:	-10dBV
最大入力レベル:	+6dBV
ヘッドルーム:	16dB

### Head Phone/LINE OUT 出力

端子:	3.5mm ミニホンジャック (ステレオ)
• ライン接続時	基準出力レベル: -16dBV 最大出力レベル: 0dBV
• ヘッドホン接続時	最大出力レベル: 15mW + 15mW (32 $\Omega$ ヘッドホン接続時)

### オーディオ性能

• 周波数特製:	INPUT (MIC/LINE) $\rightarrow$ LINE OUT: 20Hz ~ 20kHz
• 歪率:	INPUT (LINE) $\rightarrow$ LINE OUT: 0.05%以下
• S/N 比:	INPUT (MIC/LINE) $\rightarrow$ LINE OUT: 75dBV 以下

### 一般

• 記録媒体:	SD カード (512M バイト ~ 2G バイト) およびSDHC カード (4G バイト ~ 32G バイト)
• ファイルシステム	MTR/パーティション: TASCAM オリジナル FAT パーティション: FAT32
• 電池持続時間:	約8 時間 (JEITA 録音時) 約8.5 時間 (JEITA 音楽再生時)
	(アルカリ乾電池使用時。使用状況により変動することがあります。)
• 使用温度範囲:	5 ~ 35 $^{\circ}$ C
• 消費電力:	1W

- Dimensions: 155.0 (W) x 33.5 (H) x 107.0 (D) mm (w/o projections)
- Weight: 360 g (w/o batteries)

### Optional accessories

- AC adapter: PS-P520

### Computer requirements

- Windows Pentium 300 MHz or faster  
128 MB or more memory  
USB (USB 2.0 recommended)
- Macintosh: Power PC, iMac, G3, G4 266 MHz or faster  
64 MB or more memory  
USB port (USB 2.0 recommended)
- Recommended USB host controller  
Intel chipset
- Supported OS  
Windows: Windows 2000 SP4 or later, Windows XP and Windows Vista  
Macintosh: Mac OS X 10.2 or later

- 外形寸法: 155.0 (幅) × 33.5 (高さ) × 107.0 (奥行) mm (突起部含まず)
- 質量: 360g (電池を含まず)

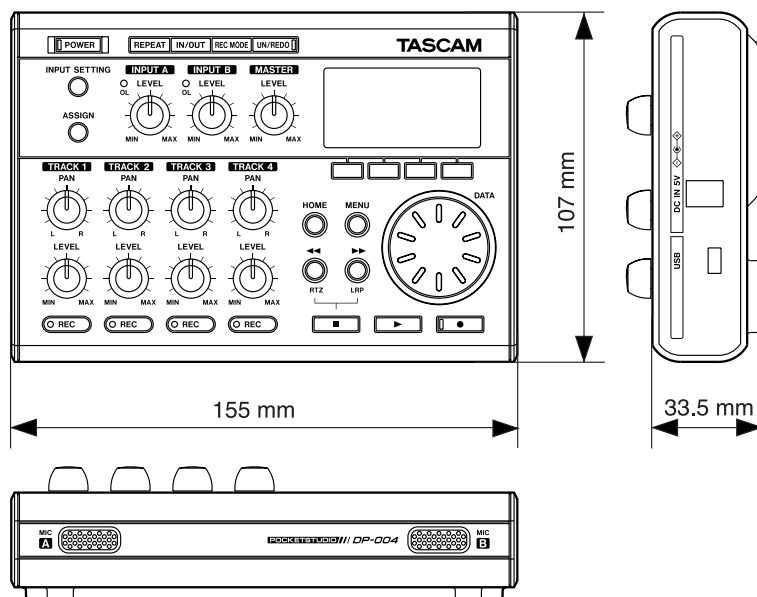
### 別売アクセサリ

- AC アダプター: PS-P520

### 接続するパソコンの条件

- Windows マシン: Pentium 300MHz 以上  
128MB 以上のMemory  
USB ポート (推奨: USB2.0)
- Macintosh マシン: Power PC、iMac、G3、G4 266MHz 以上  
64MB 以上のMemory  
USB ポート (推奨: USB2.0)
- 推奨USB ホストコントローラー:  
Intel 製チップセット
- サポートOS  
Windows: Windows 2000SP4 以上、Windows XP、Windows Vista  
Macintosh: Mac OS X 10.2 以上

### Dimensions(寸法図)



## 2. TEST MODE

### テストモード

The DP-004 is provided with a test mode that lets you run diagnostic checks on the hardware.

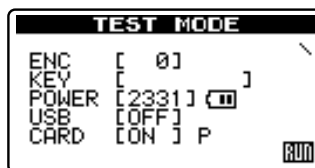
This mode is for use in factory and servicing and is not accessible by users.

#### 1. How to enter test mode

While holding down the REC1+REC3+STOP keys, switch the power on.

#### 2. Displays explained

When the test mode starts up, the following are displayed:



- ENC [ 0]: DATA encoder (0-999)  
You can determine whether or not each of the three encoders is in order.
- KEY [ ]: Shows the name of a key pressed.  
You can determine whether or not a switch pressed is in order.
- POWER: Power supply voltage (4095 steps)  
"BAT" shown when powered on battery; "AC" shown when connected to an AC outlet.
- USB: USB connection
- CARD: Card detection
- " / ": This is an event acceptance indicator.  
Normally, this indicator is still and rotates when a key is operated for example.

#### 3. Checking LEDs

When a key is pressed, its name is displayed in "KEY [ ]" and, at the same time, the associated LED turns on solid or blinks on the PANEL PCB, allowing you to check whether they work dependably.

##### 1) General

- F1: all on
- F2: blinking at higher speed
- F3: blinking at normal speed
- F4: all off

For the LED associated with a key, it turns on solid when a key is pressed and starts blinking when holding down the key for a certain time.

※ Use care when pressing the POWER key, for holding it down for a certain time switches off the power of the unit.

##### 2) Others

- OL A: turns on when the REPEAT key is pressed.
- OL B: turns on when the UN/REDO key is pressed.

DP-004ではハードウェアの自己診断が可能なテストモードを備えています。

このモードは生産、サービス用モードであり一般公開はしません。

#### 1. TEST MODEの起動方法

「REC1+REC3+STOP」キーを3個同時に押しながら電源を投入します。

#### 2. 画面の説明

起動画面後に下記のLCD表示となります。

- ENC [ 0 ]: DATAエンコーダ (0~999)  
エンコーダが正常に動作しているかを確認可能
- KEY [ ]: 押されたキーの名称を表示  
押されたキーが正常に認識されているかを確認可能
- POWER: 電源供給電圧(4095段階)  
バッテリー時: BAT / AC接続時: AC
- USB: USB接続認識
- CARD: カード検出 ("P": カードプロテクトがONの時のみ表示)
- " / ": イベント受付インジケータ。通常は停止、キーなど操作すると回転

#### 3. LED確認

KEY [ ]で押されたキーの名称を表示すると同時にPANEL PCB上のLEDも点灯もしくは点滅し、正常に点灯するか否かの確認が可能となります。

##### 1)一般

- F1: 全灯
- F2: 早い点滅
- F3: 通常点滅
- F4: 全消灯

キーとセットで設置してあるLEDに関してはキーを押すとLEDが点灯し、一定時間以上押し続けると点滅します。

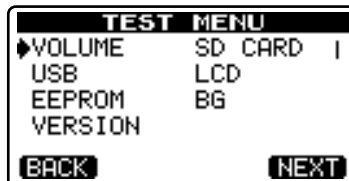
※ POWERキーは押し続けると本体の電源が切れますので注意してください。

##### 2)その他

- OL A: REPEATキーで点灯
- OL B: UN/REDOキーで点灯

## 4. Menu

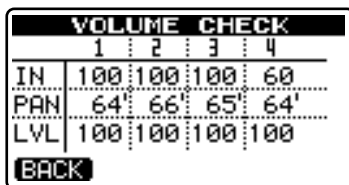
Pressing the MENU key reveals the following menu.



- REW/FF KEY: cursor movement
- F4(NEXT) KEY: mode selection
- F1(BACK) KEY: back to the TOP screen

### 1) VOLUME

Select "VOLUME" and press F4(NEXT) key and the following are displayed:

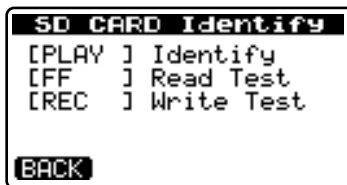


When rotating a potentiometer, the number display changes, allowing you to check whether the potentiometer is operating correctly.

- IN-1, IN-2 : INPUT A, B
- IN-3 : MASTER
- IN-4 : HEADPHONE VOLUME
- PAN : PAN
- LVL : LEVEL

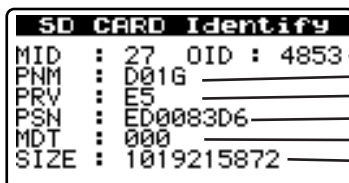
### 2) SD CARD

Select "SD" and press F4(NEXT) key and the following are displayed:



**Identify: Read in data from the card.**

Pressing the PLAY key indicates the following information:



Pressing the F1 key returns the display to the previous screen.

## 4. MENU

MENUキーを押すと下記メニューを表示します。

- REWキー/FFキー： 項目の移動。
- F4(NEXT)キー： 項目の選択。
- F1(BACK)キー： TOP画面へ。

### 1) VOLUME

"VOLUME"を選択してF4(NEXT)キーを押すと下記画面を表示します。

各対応VRを回すとその数値が変化して、VRが正常に読み取り出来ているかを確認できます。

- IN-1, IN-2 : INPUT A, B
- IN-3 : MASTER
- IN-4 : HEADPHONE VOLUME
- PAN : PAN
- LVL : LEVEL

### 2) SD CARD

"SD"を選択してF4(NEXT)キーを押すと下記画面を表示します。

**Identify : カードから情報の読み込み**

PLAYキーを押すと下記の情報を表示します。

MID : 27    OID : 4853    → Manufacturer ID    OID : OEM/Application ID  
 PNM : D01G    → Product name  
 PRV : E5    → Product revision  
 PSN : ED0083D6    → Product serial number  
 MDT : 000    → Manufacturing date  
 SIZE : 1019215872    → Raw Size

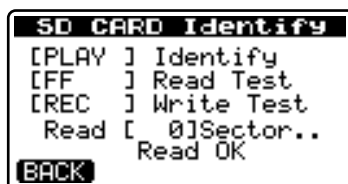
F1キーを押すと元の画面に戻ります。

**Read Test: Read in data from the card per sector**

At each press of the FWD key, data is read in from the card per sector.

**Read Test : カードから1セクタ読み込み**

FWDキーを押すと、押すたびにカードから1セクタ毎のデータの読み込みを行ないます。

**Write Test: Card write test.**

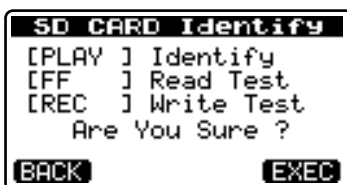
Press the REC key to advance to the following screen.

Press the F4 (EXEC) key to execute the Write Test.

**Write Test : カードへの書き込みテスト**

RECキーを押すと、下記画面を表示します。

F4(EXEC)キーを押すと書き込みテストが実行されます。



The following screen is displayed when the write test completes successfully.

※ Note that executing the Write Test results in clearing the data on the SD card as well as the format.

書込テストが正常終了すると下記画面が表示されます。

※ Write Testを実行しますとSD CARD上のデータは消去され、フォーマットもクリアされますので注意してください。

**3) USB Check**

Select "USB" and press F4(NEXT) key and the following are displayed:

Each time the ENTER key is pressed, the indication alternates between ON and OFF.

ON indicates that USB connected, and OFF indicates that USB is disconnected.

**3)USBチェック**

"USB"を選択してF4(NEXT)キーを押すと下記画面を表示します。

ENTERキーを押すたびにON/OFFを繰り返します。

ON表示でUSB接続、OFF表示でUSB切断となります。

**4) LCD Check**

Select "LCD" and press F4(NEXT) key and the following are displayed:

Contrast adjustment (F3: +; F4: -)

adjustment(FWD(▶▶): +; REW(◀◀): -)

Characters for after-image check

STOP key : Reverse

**4)LCDチェック**

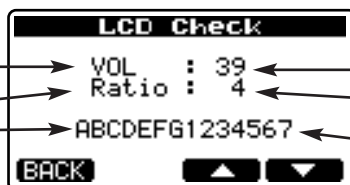
"LCD"を選択してF4(NEXT)キーを押すと下記画面を表示します。

コントラスト調整 (F3 : +, F4 : -)

コントラスト調整傾き ( REW : -, FF : + )

残像確認用キャラクタ

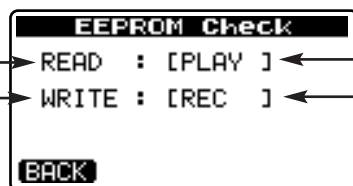
STOPキー: 反転



### 5) EEPROM Check

Select "**EEPROM**" and press F4(NEXT) key and the following are displayed:

Read in from the ROM  
 Writing all zeros to the ROM  
 The writing process starts at a press of the F4(EXEC) key in response to "**Are you sure?**" To cancel the process, press the F1(BACK) key.



PLAY :ROMの読み込み実行。  
 REC :ROMのオールゼロ書き込み。  
 "**Are you sure?**"後にF4(EXEC)で書き込み。F1(BACK)でキャンセル。

If errors occur during either the read or the write, the following are displayed:

**Timeout Err :** No response from the EEPROM  
**Error :** Errors at data send/receive time  
**Verify Err :** Errors in verification during the write process

### 5)EEPROMチェック

"**EEPROM**"を選択してF4(NEXT)キーを押すと下記画面を表示します。

READ/WRITE共に、エラーの場合には下記を表示する。

**Timeout Err :** EEPROMの応答なし  
**Error :** データ送信/受信時のエラー  
**Verify Err :** Write時のベリファイエラー

### 6)BG

Select "**BG**" and press F4 (NEXT) key, and the background sample screen is displayed.

The screen contains four pictures.

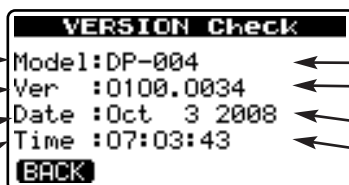
- FWD key: To move forward.
- REW key: To move backward.

Pressing F1 key returns the display to the MENU screen.

### 7) VERSION Check

Select "**VERSION**" and press F4 (NEXT) key, and the following are displayed, in which the detailed version information on the firmware can be confirmed.

Model Name  
 Version of the system firmware. The last 4 digits indicate a build number on which the system firmware was built.  
 which the system firmware was built



モデル名 (DP-004)  
 システムファームのバージョン。  
 後半の4桁はビルド番号  
 ファームビルド日付  
 ファームビルド時刻

### 6)BG

"**BG**"を選択してF4(NEXT)キーを押すと背景サンプル画面を表示します。

4枚の絵があります。

- FWDキー：進む
- REWキー：戻る

F1キーでMENU画面に戻ります。

### 7)VERSIONチェック

"**VERSION**"を選択してF4(NEXT)キーを押すと下記画面を表示され、ファームウェアの詳細Version確認が可能となります。

## 3. Updating Firmware

### ファームウェアのアップデート

#### 1. Preparations

- 1) Make the connection between this unit and the PC using a USB cable.
- 2) Place the update file in the UTILITY folder in the unit.
- 3) Perform the USB device "remove" action on the PC, and then switch off the power to the unit.

#### 2. START-UP

While holding down the REPEAT and UN/REDO keys, switch the power on.

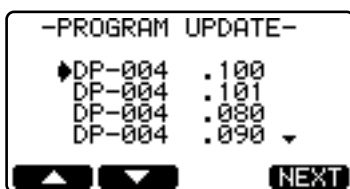
#### 3. Displays explained

The following screen is displayed initially after start-up.

- 1) When only a single file is available:



- 2) When multiple files are available:

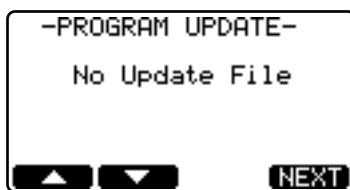


The maximum number of display lines is 4.

If a file contains a larger number of lines than the maximum number of displayable lines, the cursor can be moved using F1/F2 keys or the dial.

- 3) When no update file is available:

Nothing can be done.

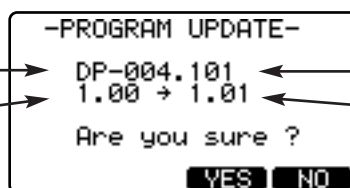


#### 4. File confirmation

Press the F4(NEXT) key .

Name of the file selected

Current version at left and New version at right



選択したファイル名

左：現バージョン 右：新バージョン

#### 5. Getting update started

Press the F3 (YES) or F4 (NO) key.

- 1) When F3 (YES) key is pressed:  
Updating is started.

#### 1. 準備

- 1) 本体とPCをUSBケーブルで接続します。
- 2) アップデートファイルを本体の「UTILITY」フォルダに置きます。
- 3) PCでUSBデバイスの「取り外し」を行い、PCから切り離れた後、本体の電源を落とします。

#### 2. 起動

REPEAT + UN/REDO キーを押しながら電源を投入します。

#### 3. 画面の説明

起動後に下記の表示となります。

- 1) ファイルが一つの場合

- 2) ファイルが複数の場合

表示行は最大4行です。

表示最大行を超えるファイルがある場合はF1キーとF2キーまたはダイヤルでカーソルが移動します。

- 3) ファイルが無い場合

何も操作できません。

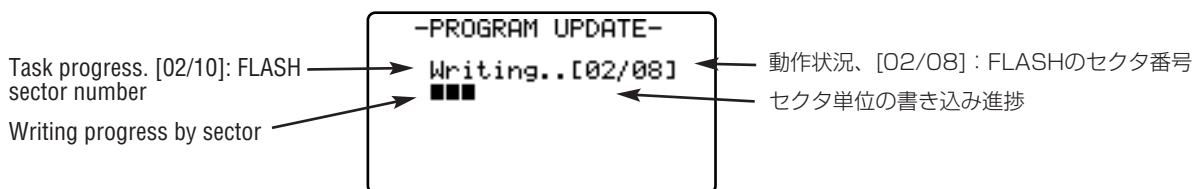
#### 4. ファイルの確認

F4(NEXT)キーを押します。

#### 5. アップデート実行

F3(YES)キーかF4(NO)キーを押します。

- 1) F3(YES)キーを押した場合  
アップデートを実行します。



2) When F4 (NO) key is pressed:

Update is not started and the display returns to the file selection screen shown above.

2) F4(NO)キーを押した場合。

アップデートを実行せず、ファイル選択画面へ戻ります。



## 6. Completion

After "Complete" and "POWER OFF" are displayed, the unit switches OFF automatically.

Switch the power of the unit again and confirm the version.

## 7. Error messages

1) If an error occurs when selecting a file, the following messages appear:

Messages(メッセージ)	Meaning (内容)
Product	The product ID of the file does not match (the file may be for other products).
	ファイルのプロダクトIDが一致しない (別製品のファイルの可能性はある)。
Old Version	The file version is older than the current one.
	現バージョンよりもファイルのバージョンが古い。
Checksum	The checksum does not match.
	ファイルのチェックサムが一致しない。
Update File	Error in file reading.
	ファイル読み込みエラー。

2) If an error occurs in the data rewriting process, the following messages appear:

2) 書き換え時にエラーが発生した場合のメッセージ

Messages(メッセージ)	Meaning (内容)
Flash Erase	Error in erasing
	消去エラー
Flash Blank	Blank error as a result of data erasure.
	消去後のブランクエラー
Flash Write	Error in writing.
	書き込みエラー
Flash Verify	Error in verification after data has been written.
	書き込み後のベリファイエラー

## 4. How to initialize SD CARD

### SDカードの初期化方法

When an SD card malfunctions, for example if the MOUNT ERROR occurs immediately after start-up, the SD card can be initialized as described below.

Initialization can also be executed on a normal SD card.

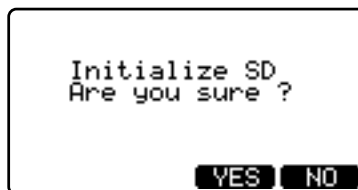
※ Initializing an SD card erases all of the data in it.

#### 1. Start-up

While holding down the REPEAT+INPUT SETTING keys, switch the power on.

#### 2, Confirmation

The screen for confirming the initialization is displayed.



#### 3. Getting Initialization Started

Press the F3 (YES) or F4 (NO) key.

1) When F3 (YES) key is pressed:

The normal startup screen is displayed, and the SD card initialization is executed.

※ The screen is displayed for a relatively long period due execution of the SD card initialization.

When the SD card initialization completes, the home screen is displayed.



2) When F4 (NO) key is pressed:

The normal start up screen is displayed, and then the home screen is displayed without initializing the SD card.



起動時にMOUNT ERRORになってしまうなど、正常に動作できなくなったSD CARDを強制的に初期化する方法です。

正常なSD CARDに対して実行することもできます。

※ この操作を行うとSD CARD内のデータはすべて消去されます。

#### 1. 起動方法

REPEATキー+INPUT SETTINGキーを押しながら電源を投入します。

#### 2. 確認画面

Initializeをするかどうか確認する画面が表示されます。

#### 3. 実行

F3(YES)キーかF4(NO)キーを押します。

1) F3(YES)キーの場合

通常起動画面となり、SD CARD初期化処理を実行します。

※ SD CARD初期化処理実行のため、この画面表示時間がやや長くなります。

SD CARD初期化処理を終了すると、HOME画面が立ち上がります。

2) F4(NO)キーの場合

通常起動画面となり、SD CARD初期化処理をしないでHOME画面が立ち上がります。

## 5. Messages Explained

### メッセージ一覧

The following popup messages alert you to conditions that may arise while you are using the unit. Consult this table if you see something you do not understand.

以下のポップアップメッセージの一覧表を示します。DP-004では状況に応じたポップアップメッセージが表示されますが、それぞれのメッセージの内容を知りたいとき、および対処方法を知りたいときにこの表をご覧ください。

#### 1. General Error (一般的エラー)

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>Empty Export Track</b>	You are trying to export a track which does not have anything recorded on it. Pick another track to export.
	「エクスポートトラックが空っぽです。」 何も録音されていないトラックをエクスポートしようとする则表示されます。別のトラックをエクスポートしてください。
<b>File Not Found</b>	You are trying to restore a song when there are no backed-up songs on the FAT partition.
	「ファイルが見つかりません。」 FAT パーティションにバックアップされたソングがないときに、ソングをリストアしようとする则表示されます。
<b>I/O Too Short</b>	You are trying to enter repeat mode, but the time between the IN and OUT points is too short. Make the time longer.
	「IN ポイントとOUT ポイントが近すぎます。」 リピートモードに入ろうとするときにIN ポイントとOUT ポイントが近すぎると表示されます。 IN ポイントとOUT ポイントを2 フレーム以上離してください。
<b>Import File Not Found</b>	You are trying to import a WAV file from the FAT partition when there are no WAV files there. Connect the unit to a PC and transfer some files to the FAT partition for import..
	「インポートするファイルが見つかりません。」 WAV ファイルのないFAT パーティションからWAV ファイルをインポートしようとしています。 本機をパソコンに接続して、インポートするファイルをパソコンから本機のFAT パーティションに転送してください。
<b>Import File Too Large</b>	You are trying to import a WAV file from the FAT partition that is too large for the remaining space on the partition. Free up some space on the (native) partition and try again.
	「インポートするファイルが大きすぎます。」 アクティブパーティションの空きスペースより容量の大きいWAV ファイルをFAT パーティションからインポートしようとしています。アクティブパーティション内の不要なファイルを削除して空きスペースを増やしてから再度インポートを試みてください。
<b>In Bounce Mode</b>	You tried to perform an action that cannot be done while in Bounce mode.
	「バウンスモード中です。」 バウンスモード中に禁止操作をしようとしたときに表示されます。
<b>In Master Mode</b>	You tried to perform an action that cannot be done while in Master mode.
	「マスタリングモード中です。」 マスタリングモード中に禁止操作をしようとしたときに表示されます。
<b>In Repeat Mode</b>	You tried to perform an action that cannot be done while in Repeat mode.
	「リピートモード中です。」 リピートモード中に禁止操作をしようとしたときに表示されます。
<b>Master Track Not Found</b>	You have tried to export a mastered mix track when the song does not have one. Master the song and then export the mix.
	「マスタートラックが見つかりません。」 ステレオマスターがソング内に録音されていないときにステレオマスターをエクスポートしようとする则表示されます。 ソングをマスタリングしてから、ステレオマスターをエクスポートしてください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>Master Track Too Large</b>	You tried to export a master track which was too large for the remaining space on the FAT partition . Connect the unit to a computer and free up some space on the FAT partition.
	「マスタートラックが大きすぎます。」 FAT パーティションの空き容量より大きなステレオマスターをエクスポートしようとしています。 本機をパソコンに接続して、FAT パーティションの空きスペースを拡げてください。
<b>No Disk Space</b>	You tried to create a song, but there is not enough space on the partition to create a song. Free up some space and try again.
	「ディスクスペースがありません。」 パーティションパーティションに十分な空きスペースがないときにソングを作成しようとすると、こ のメッセージが表示されます。 スペースを拡げてからソングを作成してください。
<b>No Master Trk</b>	You have tried to use a non-existent master track as the source in a track cloning operation. Select another source or master the song and try again.
	「マスタートラックが存在しません。」 トラックのクローンを作るとき、存在しないマスタートラックをソースとして選択しようとする と表示されます。 マスタートラックを作るか、または別のソースを選択してください。
<b>No Song</b>	You are trying to load a song from a partition that has no songs on it. Change partitions.
	「ソングがありません。」 ソングが存在しないパーティションからソングをロードしようとしています。 パーティションを変更してください。
<b>No Undo Histry</b>	There are no actions to be undone.
	「アンドゥのヒストリーがありません」 アンドゥするような操作が存在しません。
<b>History 900!!</b>	The number of items in the Undo History has exceeded 900. Clear the Undo History because the Work Memory is about to become full.
	Undo Historyが900個を越えたときに警告として表示されます。 Work Memory Fullになる寸前ですので、Historyクリアを実行してください。
<b>Not Stopped</b>	The transport is moving (not stopped, but playing back, recording, etc.) and you have pressed a key such as the UN/REDO key which cannot be used until you press STOP.
	「レコーダーが停止していません。」 レコーダーが停止していないとき、たとえばUN/REDO キーのように停止中でないと受け付け ないキーを押すと、このメッセージが表示されます。
<b>Now Recording</b>	You are trying to perform an action which cannot be done while recording.
	「レコーディング中です。」 レコーディングを行っているときにメニュー操作を行おうとすると表示されます。他にもレコー ディング中に受け付けられない操作があります。
<b>Same Track</b>	You cannot clone a track to itself.
	「同じトラックを指定しています。」 クローントラック設定で、"Src Trk" と"Dst Trk" とで同じトラックを指定すると表示されま す。
<b>Song Protected</b>	The song is protected and you are trying to change it (record or edit, etc.). Unprotect the song.
	「ソングがプロテクトされています。」 プロテクトされているソングに変更(録音、編集など)を加えようとする と表示されます。変更を加える前にプロテクトを解除してください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>Too Many songs</b>	You have 250 songs on one partition. You must delete some before you can create another song.
	「これ以上ソングを作成できません。」 一つのパーティションが持つことができるソングの数は最大250です。不要なソングを削除してから、新しいソングを作成してください。
<b>Track Full</b>	You are trying to import a file from the FAT partition to a track that has already been recorded to . You can only import to a blank track.
	「トラックが録音済みです。」 FAT パーティションからすでに録音されているトラックにファイルをインポートしようとすると表示されます。
<b>Trk Too Short</b>	You are trying to master with the OUT point at the zero position. Set the OUT point and try again.
	「トラックが短すぎです。」 ゼロポジションをOUTポイントに設定してマスタリングを行おうとすると表示されます。OUTポイントを設定し直してください。
<b>No SD Card! Please set a SD</b>	Insert an SD card after turning off the unit.
	「SDカードが挿入されておりません。」 電源をオフにしてからSDカードを挿入してください。
<b>Not Continued</b>	This error occurs during SONG BACKUP or SONG RESTORE. The song data is destroyed or normal access to the FAT area failed.
	SONG BACKUP または SONG RESTORE中のエラーです。 SONGデータが壊れているか、FATエリアに正常アクセスができなかった場合に表示されます。
<b>It's Too Lage</b>	The FAT area does not have enough remaining space for SONG BACKUP. Move the files in the FAT area to the PC using the USB connection or save the files in the FAT area and then reformat it.
	SONG BACKUP時にFAT空き容量が足りない場合に表示されます。 USB接続してFATエリアにあるファイルをPCへ移動するか、FAT上のファイル保存後FAT REFORMATしてください。
<b>Invalid Card</b>	Insert another SD card after turning off the unit, or format the card by MENU → CARD → FORMAT.
	「挿入されているSDカードはDP-004で使用できないフォーマットです。」 電源をオフにしてから別のSDカードを挿入するか、MENU → CARD からFORMAT してください。
<b>Protected Card</b>	To record or edit, turn off the unit and un-protect the SD card.
	「挿入されているSD CARD はプロテクトされています。」 録音や編集を行いたい場合は、電源をOFF してSD カードのプロテクトを解除してください。
<b>Card Full</b>	The SD card is full during recording. Erase the unnecessary songs or use another SD card.
	「録音中にSD カードがいっぱいになりました。」 不要なSONGをERASEするか、SDカードを交換してください。
<b>Trk Edit Fail</b>	Save the song and turn the unit off and then on, and perform track edit again.
	「トラックエディットに失敗しました。」 ソングを保存してから本体の電源を入れ直して再度トラックエディットを実行してください。
<b>Battery Empty</b>	Replace the batteries with new ones or use a PS-P520 AC adapter (sold separately).
	「電池が空です。」 電池がほとんど空の状態の時に表示されます。 新しい電池に交換するか、別売のAC アダプター (PS-P520) を接続してご使用ください。
<b>Battery Low</b>	Replace the batteries with new ones or use a PS-P520 AC adapter (sold separately).
	「電池が空に近いです。」 電池が空に近い状態で録音しようとすると表示されます。 新しい電池に交換するか、別売のAC アダプター (PS-P520) を接続してご使用ください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>SD Size Error</b>	Use an SD card larger than 512 MB.
	「DP-004 では使用できない小さいサイズのSD カードが挿入されています。」 512M バイト以上のSD カードをご使用ください。
<b>Work Memory Full</b>	Even if the card has enough remaining memory space, this error may occur when you record a long song or edit a lot. You may be able to continue the work if you clear the history which may increase the open work memory. You may also be able to continue work by turning the unit off and then on again, which may inclears the open work memory.
	「ソングの録音や編集のために必要なワークメモリがいっぱいになりました。」 SDカードの空き容量が残っていても、1 ソングでの長時間録音を行ったり、編集作業を多く行うと発生する場合があります。 ヒストリのクリアを実行すると空きワークメモリが増え、作業が継続できる場合があります。 電源をオフすることでも空きワークメモリが増え、作業が継続できる場合があります。

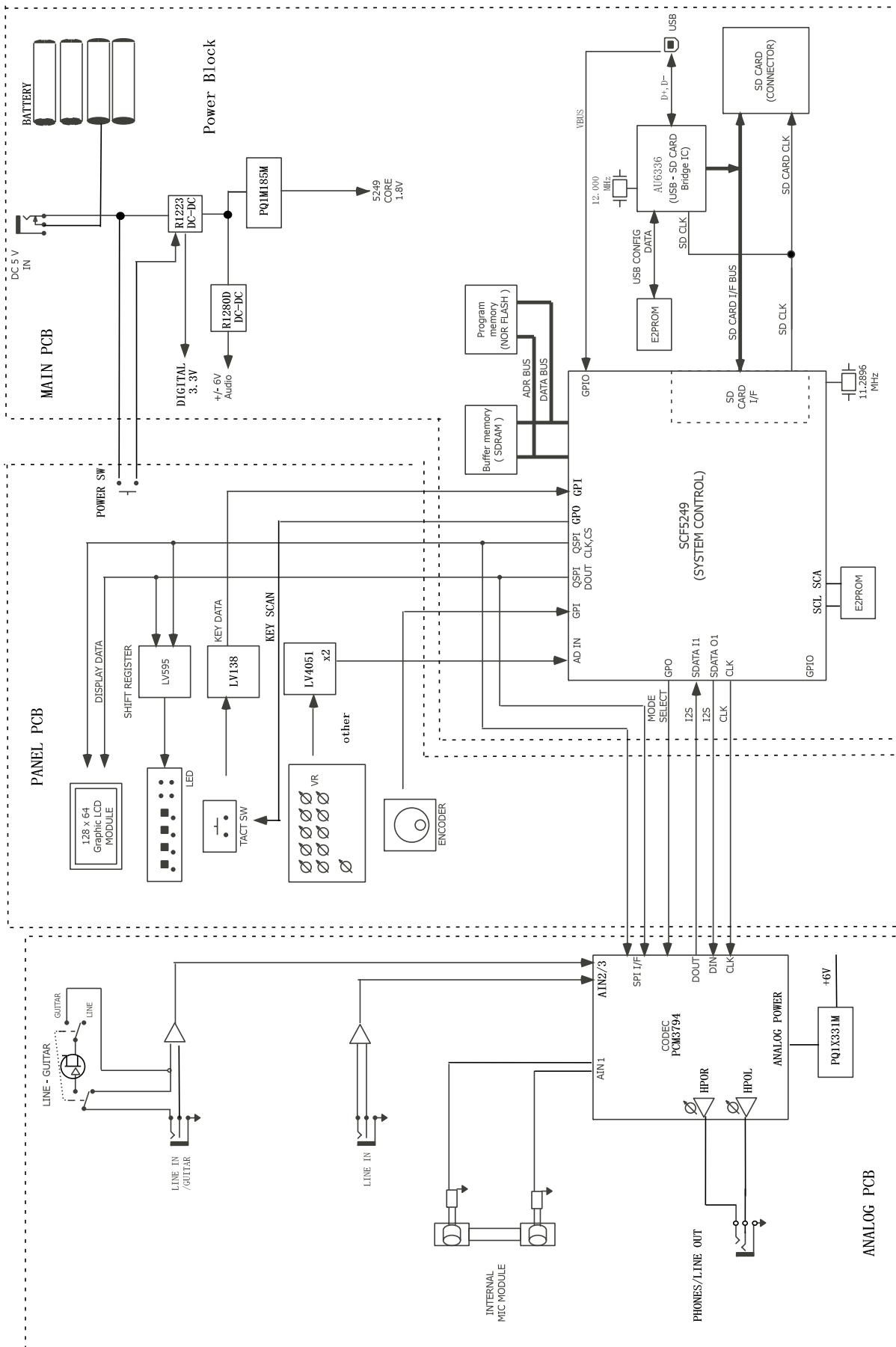
## 2. Fatal Error (致命的エラー)

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>SD Not Found</b>	The SD card cannot be recognized. Ensure that a normal card is inserted correctly and switch the power off then on again.
	SDカードが認識できませんでした。正常なSDカードが正しく挿入されていることを確認し、電源を入れ直してください。
<b>SD Read Busy</b>	The SD card read operation is delayed for the required processing. The card may be defective. Re-format it or use another SD card.
	SDカードからの読み込み時、処理が間に合わないなどのエラー。SDカード不良の可能性があります。カードフォーマットし直すか、別のSDカードを使用してください。
<b>SD Write Busy</b>	The SD card write operation is delayed for the required processing. The SD card may be defective. Re-format it or use another card.
	SDカードへの書き込み時、処理が間に合わないなどのエラー。SDカード不良の可能性があります。カードフォーマットし直すか、別のSDカードを使用してください。
<b>I/F Error</b>	The card does not respond or there is an error on the SD interface. The hardware or SD card may be defective.
	カードから応答が無いか、もしくはSDインターフェース上のエラー。 ハードウェア不具合、あるいはカード不良の可能性があります。
<b>No Memory Left</b>	An error occurred during the Track Edit operation. The song data is destroyed or normal access is impossible.
	Track Editでエラーが発生しました。 SONGデータが壊れているか正常にアクセスできない可能性があります。
<b>FileErr:XXXXXX</b>	Other irrecoverable error. "XXXXXX" is the number of the current step and indicates how far the processing has advanced till the error. The SD card may be defective. Re-format it or use another card.
	「その他の修復不可能なエラー」 XXXXXXは処理がどこまで進んだかのステップを表す番号です。 SDカード不良の可能性があります。カードフォーマットし直すか、別のSDカードを使用してください。
<b>Audio Rst Fail</b>	Audio file system initialization error. The format in the SD card is destroyed or the card is defective. Re-format the SD card or use another card.
	Audio File System 初期化エラー。SDカード内のフォーマットが壊れている、またはSDカード不良の可能性があります。 カードフォーマットし直すか、別のSDカードを使用してください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
<b>SaveParam Fail</b>	Parameter save error. Check the card insertion and card protection status. Otherwise, the SD card may be defective.
	パラメータセーブエラー。SDカード挿入、カードプロテクトを確認してください。 SDカード不良の可能性もあります。
<b>Mount Error:XX</b>	Mount processing error. "XX" is the number of the current step indicating how far the processing has advanced till the error. The format in the SD card is destroyed or the card is defective. Re-format the SD card or use another card.
	マウントプロセスでのエラー。XXは処理がどこまで進んだかのステップを表す番号です。 SDカード内のフォーマットが壊れている、またはSDカード不良の可能性もあります。 カードフォーマットし直すか、別のSDカードを使用してください。
<b>SD-Card Error!</b>	The SD card was ejected in the middle of recording or playback.
	録音・再生動作中にSDカードがイジェクトされた場合に表示されます。
<b>System Error code 1</b>	CPU access error. The firmware may be defective.
	CPUのアクセスエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 2</b>	CPU address error. The firmware may be defective.
	CPUのアドレスエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 3</b>	CPU instruction error. The firmware may be defective.
	CPUのインストラクションエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 4</b>	CPU zero division error. The firmware may be defective.
	CPUのゼロ除算エラー。ファームウェア不具合の可能性もあります。
<b>System Error code 5</b>	CPU Privilege Violation error. The firmware may be defective.
	CPUのPrivilege Violationエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 6</b>	CPU Unimplemented line-a opcode error. The firmware may be defective.
	CPUのUnimplemented line-a opcodeエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 7</b>	CPU Unimplemented line-f opcode error The firmware may be defective.
	CPUのUnimplemented line-f opcodeエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 8</b>	CPU format error. The firmware may be defective.
	CPUのフォーマットエラー。ファームウェア不具合の可能性もあります。
<b>System Error code 9</b>	CPU Uninitialized Interrupt error. The firmware may be defective.
	CPUのUninitialized Interruptエラー。ファームウェア不具合の可能性もあります。

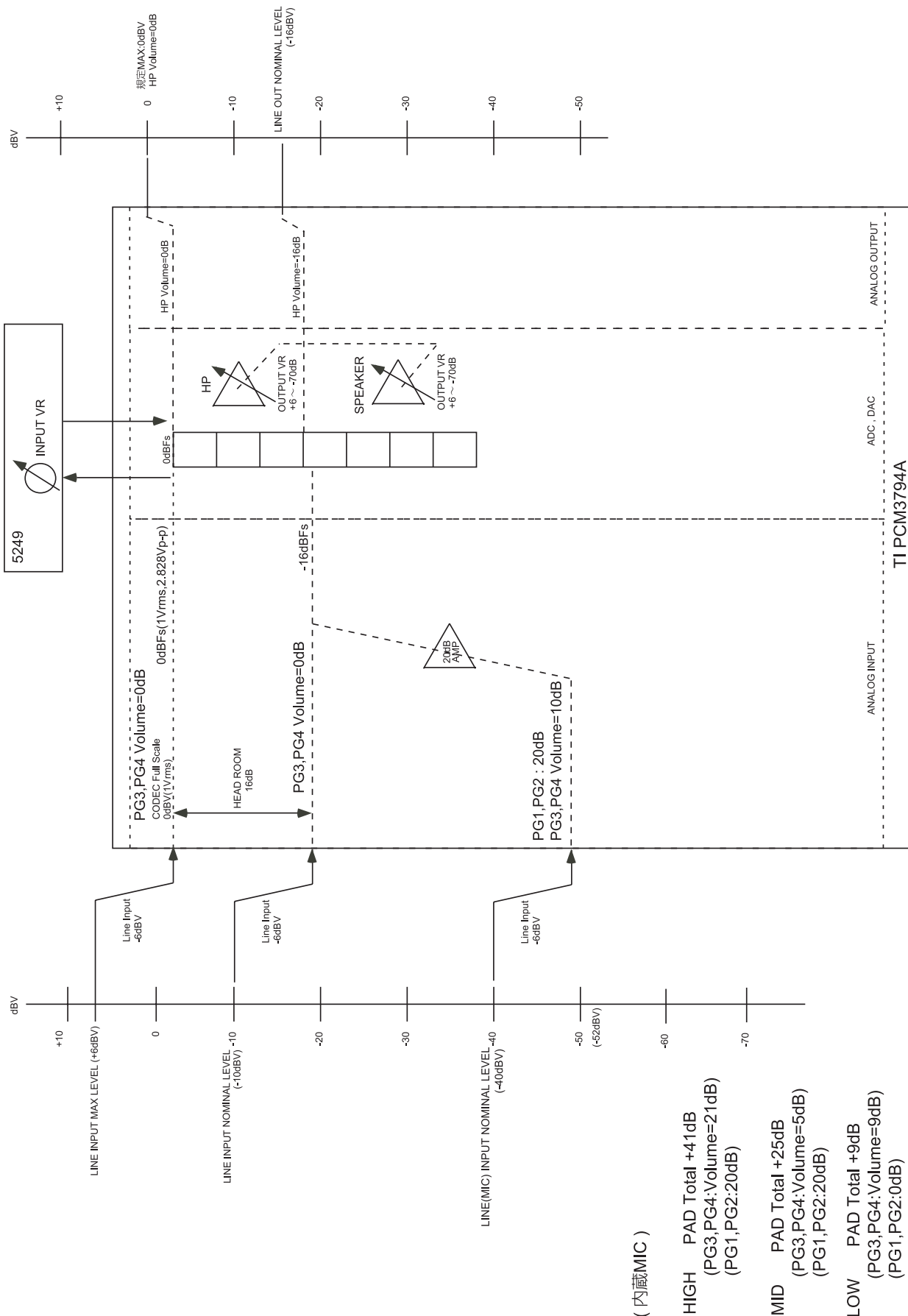
# 6. Block Diagram

## ブロックダイアグラム



# 7. Level Diagram

## レベルダイアグラム



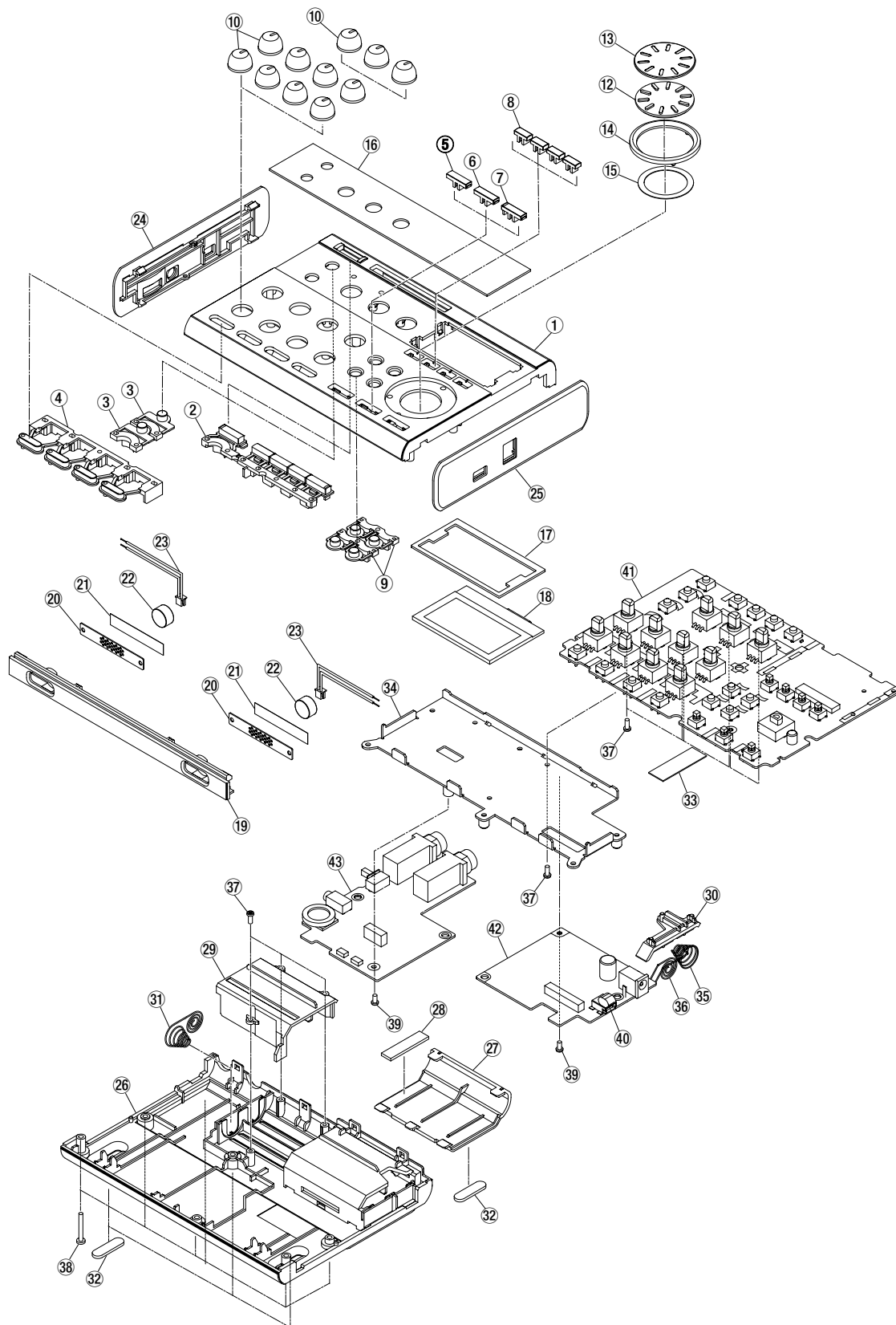
DP-004 LEVEL DIAGRAM

- ( 内蔵MIC )
- HIGH PAD Total +41dB  
(PG3,PG4:Volume=21dB)  
(PG1,PG2:20dB)
- MID PAD Total +25dB  
(PG3,PG4:Volume=5dB)  
(PG1,PG2:20dB)
- LOW PAD Total +9dB  
(PG3,PG4:Volume=9dB)  
(PG1,PG2:0dB)

# 8. Exploded Views and Parts List

## 分解図とパーツリスト

### Exploded View-1



#### ●CAUTION

Danger of explosion if battery is incorrectly replaced.  
Replace only with the same or equivalent type.

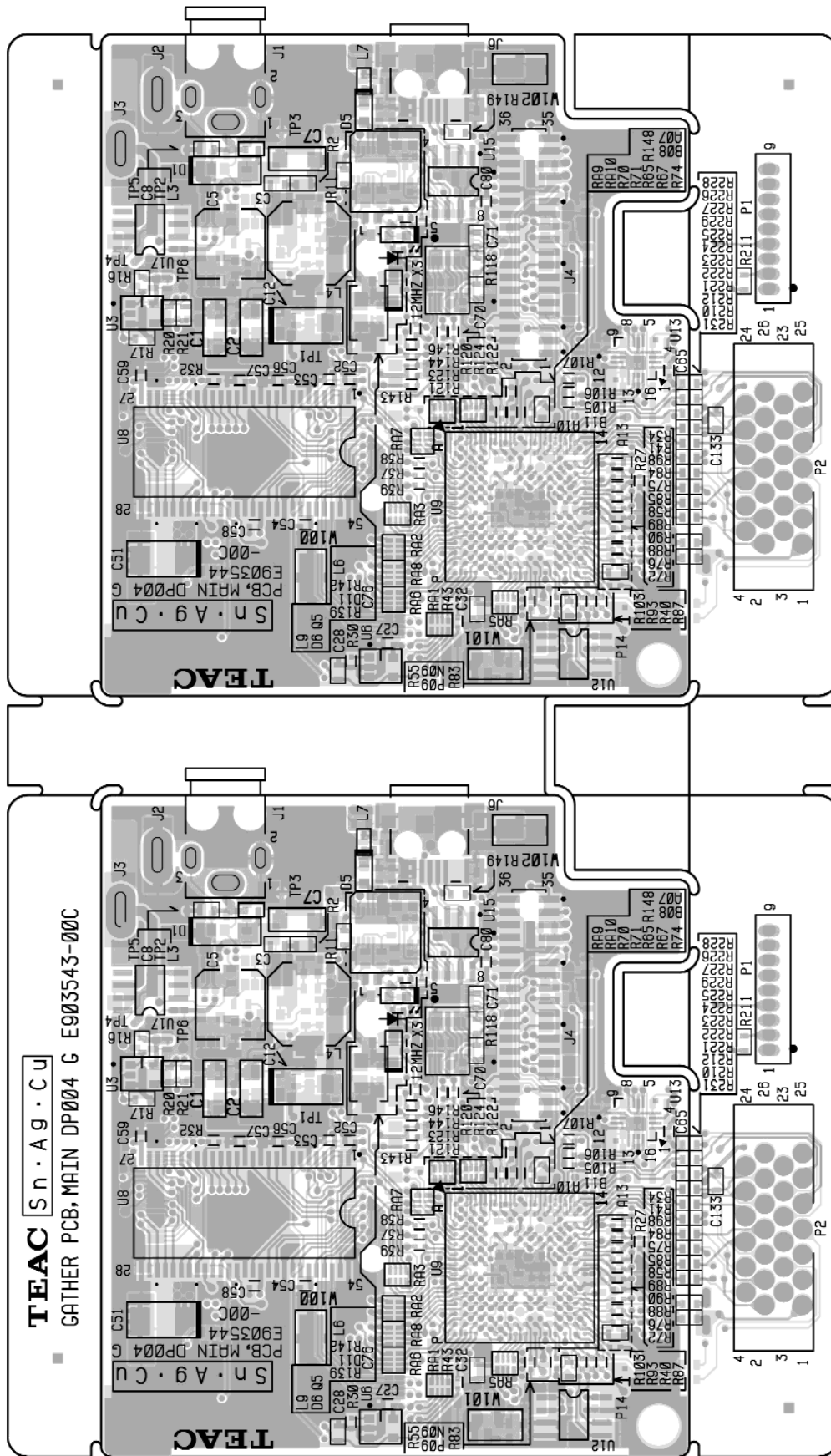
**Exploded View-1**

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	M02876900B	PANEL, TOP DP004 G	
1- 2	M02877500A	BUTTON,A DP004 G	
1- 3	M02877600A	BUTTON,B DP004 G	
1- 4	M02877700A	BUTTON,C DP004 G	
1- 5	M02877810C	BUTTON,D STOP DP004 G	
1- 6	M02877820C	BUTTON,D PLAY DP004 G	
1- 7	M02877900C	BUTTON,E DP004 G	
1- 8	M02878000B	BUTTON,F DP004 G	
1- 9	M02878100A	BUTTON,G DP004 G	
1-10	M02878500B	KNOB,VR DP004 ORG G	
1-11	M02878510B	KNOB,VR DP004 WHT G	
1-12	M02878600A	KNOB,JOG BASE DP004 G	
1-13	M02878700A	KNOB,JOG COVER DP004 G	
1-14	M02878800A	KNOB,JOG RING DP004 G	
1-15	M02882200A	POLYEST SHEET,JOG DP004 G	
1-16	M02878900A	WINDOW,DP004 G	
1-17	M02879000A	CUSHION,LCD DP004 G	
1-18	E01381200A	LCD,KMC12864AC-00-SP A G	
1-19	M02877300B	ESCUTCHEON,DP004 G	
1-20	M02880600B	PLATE,MIC DP004 G	
1-21	M02880700A	SHEET,MIC DP004 G	
1-22	3E038410	MIC CONDENSER ECM-100 G	
1-23	E01534000A	HARN ASSY,MIC DP004 G	
1-24	M02877100B	PANEL,SIDE L DP004 G	
1-25	M02877200B	PANEL,SIDE R DP004 G	
1-26	M02877000B	PANEL,BOTTOM DP004 G	
1-27	M02879100A	COVER,BATTERY A DP004 G	
1-28	M02904300A	CUSHION,BATTERY DP004 G	
1-29	M02879200A	COVER,BATTERY B DP004 G	
1-30	M02880200A	COVER,BATTERY C DP004 G	
1-31	M02666400A	SPRING,BATT CDXT2 G	
1-32	M02880800A	FOOT,DP004 G	
1-33	M02931700A	SHEET,PCB PANEL DP004 G	
1-34	M02877400B	FRAME,MAIN DP004 G	
1-35	M02880300A	SPRING,BATTERY A DP004 G	
1-36	M02880400A	SPRING,BATTERY B DP004 G	
1-37	B00302606A	SCREW,BPB M2*6 FNI G	
1-38	B00311316A	SCREW,BPP 2*16 FZC G	
1-39	B00311704A	SCREW,BPA 2*4 FNI G	
1-40	M02931400A	CUSHION,50*55*70 G	
1-41	E95354000A	PCB ASSY,PANEL DP004 G.....	GATHER PCBA,PANEL DP004 G(Refer to page 22/23)
1-42	E95354400A	PCB ASSY,MAIN DP004 G.....	GATHER PCBA,MAIN DP004 G(Refer to page 20/21)
1-43	E95354200A	PCB ASSY,ANA DP004 G.....	GATHER PCBA,ANA DP004 G(Refer to page 24)

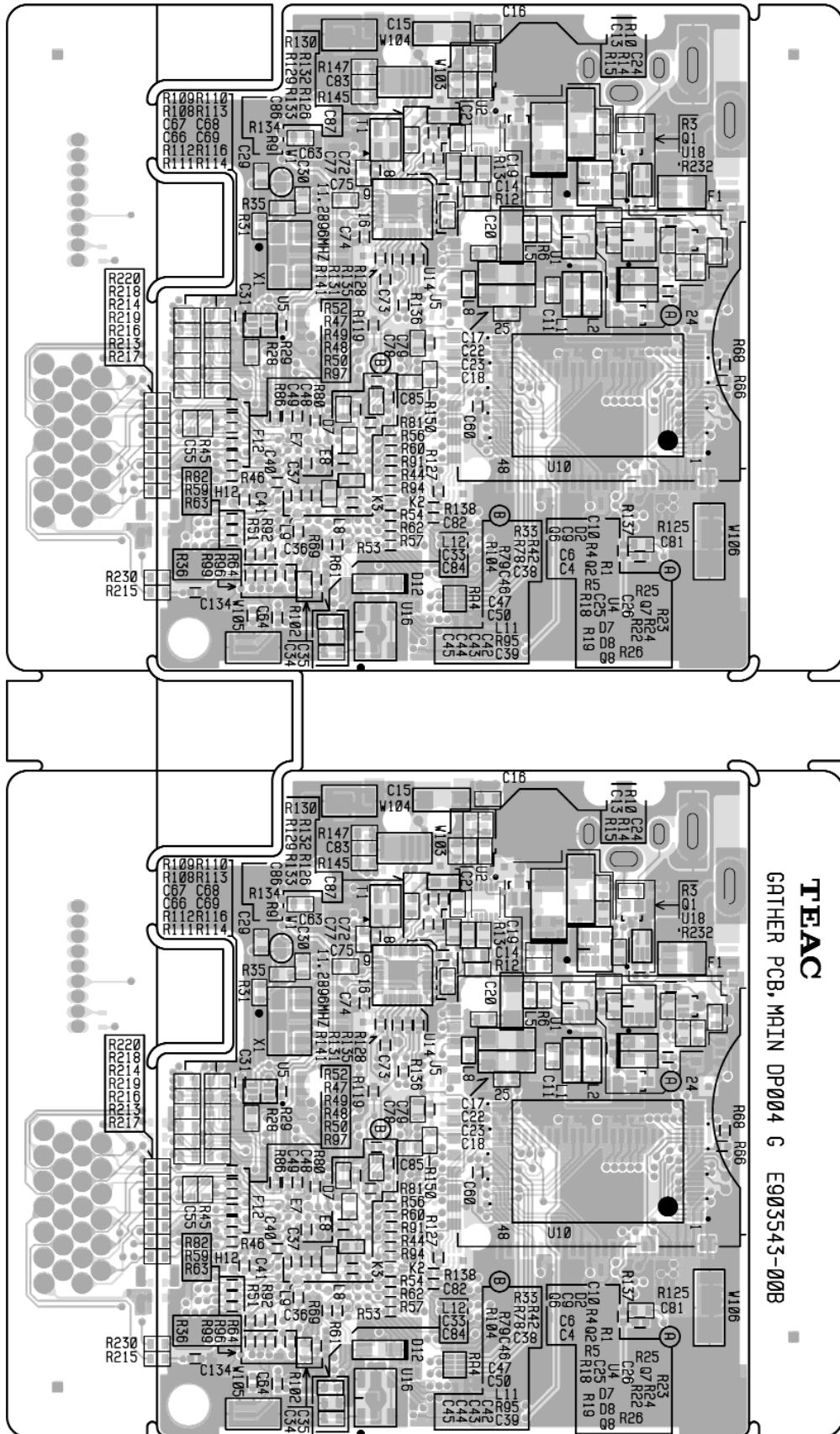
# 9. PC Boards and Parts List

基板図とパーツリスト

## MAIN PCB (Side A)



MAIN PCB (Side B)









**GATHER PCBA,MAIN DP004 G**

REF.NO.	PARTS NO.	DESCRIPTION
	E95354300A	GATHER PCBA,MAIN DP004 G PCB,MAIN DP004 G
		PCB ASSY,MAIN DP004 G
C12	C0069934	CNIOB,NOJC107M004R G
C51	C0069934	CNIOB,NOJC107M004R G
C9	C0069954	CNIOB,NOJC336M010R G
D1	S0021344	DIODE,RB160L-40
D2	S0042404	DIODE,RB161L-40 G
D5	S0075354	DIODE,RB551V-30 TE17 G
D6	S0075354	DIODE,RB551V-30 TE17 G
D7	S0022094	DIODE,1SS355
D8	S0022094	DIODE,1SS355
D12	S0071644	DIODE,RB161M-20 G
F1	E0017804	FUSE,ICP-S2.3 (-TN)
J1	E0138210	JACK,DC POWER KM02006P G
J4	E0152743	CONN,2199SBDI36GSM4060 G
J5	E0143773	CONNECTOR,SCDA4A0400 G
J6	E0143954	CONNECTOR,USB MINI-5B G
L1	R0177384	RD,1/8W 0 OHM F0805 G
L2	R0177384	RD,1/8W 0 OHM F0805 G
L3	R0157394	RD,1/10W 0 OHM J0603G
L4	E0138204	COIL,CDRH8D28-330NC 33UHG
L5	E0126164	BEAD COIL,BLM18PG471SN1D G
L6	E0128494	COIL,CDRH5D28NP101NC 100U G
L7	E0126164	BEAD COIL,BLM18PG471SN1D G
L8	E0126164	BEAD COIL,BLM18PG471SN1D G
L9	E0101174	COIL,LQH43CN100K03L G
L11	E0126164	BEAD COIL,BLM18PG471SN1D G
L12	E0126164	BEAD COIL,BLM18PG471SN1D G
Q1	S0065074	TRANSISTOR,DTC124EUA TP G
Q2	S0050404	FET,RTQ035P02
Q5	S0073014	FET,RTF020P02 TL G
Q6	S0075374	FET,RTF025N03 G
Q7	S0042944	TRANSISTOR,DTC143TUA T106
Q8	S0042944	TRANSISTOR,DTC143TUA T106
RA1	R0181584	RES ARRAY,82*4 1005 G
RA2	R0181584	RES ARRAY,82*4 1005 G
RA3	R0181584	RES ARRAY,82*4 1005 G
RA4	R0181584	RES ARRAY,82*4 1005 G
RA5	R0181584	RES ARRAY,82*4 1005 G
RA6	R0181594	RES ARRAY,47*4 1005 G
RA7	R0181594	RES ARRAY,47*4 1005 G
RA8	R0181594	RES ARRAY,47*4 1005 G
RA9	R0181594	RES ARRAY,47*4 1005 G
RA10	R0181594	RES ARRAY,47*4 1005 G
T1	E0128484	FILTER,956BP-1002=P2 G
U1	S0072964	IC,R1223N332H-TR-F G
U2	S0075384	IC,R1280D002B-TR-F G
U3	S0072934	IC,BU4S66G2-TR G
U4	S0080064	IC,BD46361G-TR G
U4	S0079724	IC,BD46362G-TR G
U5	S0065014	IC,SN74LVC2GU04DCKR G
U6	S0065024	IC,BD46285G G

**GATHER PCBA,MAIN DP004 G**

REF.NO.	PARTS NO.	DESCRIPTION
U8	S0055053	IC,M12L64164A-7T-G
U9	S0060143	IC,SCF5249VM140
U10	S00804500A	IC,,ROM ASSY MAIN DP004 G IC,S29AL008D70TFI020 G LABEL,ROM VER M100 G SOFTWARE SPEC,MAINDP004 G
U12	S0071694	IC,CAT24C04WI-GT3 G
U13	S0079734	IC,BA2901KN-E2 G
U14	S0079744	IC,AU6336-MOF G
U15	S00804600A	IC,ROM ASSY USB DP004 G IC,CAT24C04WI-GT3 G SOFTWARE SPEC,USB DP004 G
U16	S0063964	IC,PQ1M185M2SPQ G
U17	S0079754	IC,AIC1526-0PSTR
U18	S0080024	IC,BD4944FVE-TR G
W100	M0293230	LEAF SPR,B5G-25*45*060 G
W101	M0293230	LEAF SPR,B5G-25*45*060 G
W102	M0293230	LEAF SPR,B5G-25*45*060 G
X1	E0141174	RESONATOR,11.2896MHZ G
X3	E0141184	RESONATOR,12.0000MHZ G

**GATHER PCBA,PANEL DP004 G**

REF.NO.	PARTS NO.	DESCRIPTION
	E95353900A	GATHER PCBA,PANEL DP004 G PCB,PANEL DP004 G
		PCB ASSY,PANEL DP004 G
BZD14	S0080034	ZENER DIO,RSB5.6S TE61 G
BZD15	S0080034	ZENER DIO,RSB5.6S TE61 G
BZD16	S0080034	ZENER DIO,RSB5.6S TE61 G
BZD17	S0080034	ZENER DIO,RSB5.6S TE61 G
BZD18	S0080034	ZENER DIO,RSB5.6S TE61 G
BZD19	S0080034	ZENER DIO,RSB5.6S TE61 G
BZD20	S0080034	ZENER DIO,RSB5.6S TE61 G
D501	S0079784	LED,LNJ326W83RAC G
D502	S0079774	LED,LNJ826W83RAA G
D503	S0079774	LED,LNJ826W83RAA G
D504	S0079774	LED,LNJ826W83RAA G
D505	S0079774	LED,LNJ826W83RAA G
D506	S0079774	LED,LNJ826W83RAA G
D507	S0079774	LED,LNJ826W83RAA G
D508	S0079774	LED,LNJ826W83RAA G
D509	S0022094	DIODE,1SS355
D510	S0022094	DIODE,1SS355
D511	S0022094	DIODE,1SS355
D512	S0022094	DIODE,1SS355
D513	S0022094	DIODE,1SS355
D514	S0022094	DIODE,1SS355
D515	S0022094	DIODE,1SS355
D517	S0022094	DIODE,1SS355
D518	S0022094	DIODE,1SS355
D519	S0022094	DIODE,1SS355
D520	S0022094	DIODE,1SS355
D521	S0022094	DIODE,1SS355
D522	S0022094	DIODE,1SS355
D523	S0022094	DIODE,1SS355
D530	S0022094	DIODE,1SS355
D531	S0022094	DIODE,1SS355
D532	S0022094	DIODE,1SS355
D533	S0022094	DIODE,1SS355
D534	S0022094	DIODE,1SS355
D540	S0022094	DIODE,1SS355
D541	S0022094	DIODE,1SS355
D542	S0079794	LED,LNJ826W86RA G
EC501	E0140844	ENCODER,EC12E2440301 G
J501	E0134523	CONNECTOR,2200SB36GSM45 G
J502	E0152773	CONN,2200SB18GSM45 G
J503	E0152834	CONN,F1003WRS18PT G
Q502	S0041574	TRANSISTER,DTA124EUA G
S501	E0127100	SW,TACT SKHHAM2520 G
S503	E0125781	SW,TACT SKHHDA010 G
S504	E0125781	SW,TACT SKHHDA010 G
S505	E0125781	SW,TACT SKHHDA010 G
S506	E0125781	SW,TACT SKHHDA010 G
S507	E0127100	SW,TACT SKHHAM2520 G
S508	E0127100	SW,TACT SKHHAM2520 G

**GATHER PCBA,PANEL DP004 G**

REF.NO.	PARTS NO.	DESCRIPTION
S509	E0127100	SW,TACT SKHHAM2520 G
S510	E0127100	SW,TACT SKHHAM2520 G
S511	E0125781	SW,TACT SKHHDA010 G
S512	E0125781	SW,TACT SKHHDA010 G
S513	E0125781	SW,TACT SKHHDA010 G
S514	E0127100	SW,TACT SKHHAM2520 G
S515	E0127100	SW,TACT SKHHAM2520 G
S516	E0127100	SW,TACT SKHHAM2520 G
S518	E0127100	SW,TACT SKHHAM2520 G
S519	E0127100	SW,TACT SKHHAM2520 G
S520	E0127100	SW,TACT SKHHAM2520 G
S521	E0127100	SW,TACT SKHHAM2520 G
S522	E0127100	SW,TACT SKHHAM2520 G
S523	E0127100	SW,TACT SKHHAM2520 G
S524	E0127100	SW,TACT SKHHAM2520 G
U501	S0065394	IC,SN74LV595APWR G
U502	S0037264	IC,SN74LV4051APWR
U503	S0037264	IC,SN74LV4051APWR
U504	S0051154	IC,SN74LV138APW G
VR501	R0193080	VR,XV09211YNPV15F1B10KC G
VR502	R0193090	VR,XV09211YNPV15F1B10K G
VR503	R0193080	VR,XV09211YNPV15F1B10KC G
VR504	R0193090	VR,XV09211YNPV15F1B10K G
VR505	R0193080	VR,XV09211YNPV15F1B10KC G
VR506	R0193090	VR,XV09211YNPV15F1B10K G
VR507	R0193080	VR,XV09211YNPV15F1B10KC G
VR508	R0193090	VR,XV09211YNPV15F1B10K G
VR509	R0193090	VR,XV09211YNPV15F1B10K G
VR510	R0193090	VR,XV09211YNPV15F1B10K G
VR511	R0193090	VR,XV09211YNPV15F1B10K G
W500	M0293230	LEAF SPR,B5G-25*45*060 G
W501	M0293230	LEAF SPR,B5G-25*45*060 G
W502	M0293230	LEAF SPR,B5G-25*45*060 G
W503	M0293230	LEAF SPR,B5G-25*45*060 G
W504	M0293230	LEAF SPR,B5G-25*45*060 G
W505	M0293230	LEAF SPR,B5G-25*45*060 G
W508	M0293230	LEAF SPR,B5G-25*45*060 G
W509	M0293230	LEAF SPR,B5G-25*45*060 G
ZD1	S0074914	ZENER DIO,RSAG.1U5 T108 G

**GATHER PCBA,ANA DP004 G**

REF.NO.	PARTS NO.	DESCRIPTION
	E95354100A	GATHER PCBA,ANA DP004 G PCB,ANA DP004 G
		PCB ASSY,ANA DP004 G
D12	S0022094	DIODE,1SS355
D13	S0022094	DIODE,1SS355
D16	S0022094	DIODE,1SS355
D17	S0022094	DIODE,1SS355
D20	S0022094	DIODE,1SS355
D21	S0022094	DIODE,1SS355
D22	S0023224	DIODE,DAN217 T146 G
D23	S0022094	DIODE,1SS355
D24	S0022094	DIODE,1SS355
D25	S0022094	DIODE,1SS355
D26	S0022094	DIODE,1SS355
D27	S0022094	DIODE,1SS355
D28	S0022094	DIODE,1SS355
D29	S0022094	DIODE,1SS355
D30	S0022094	DIODE,1SS355
D31	S0022094	DIODE,1SS355
D32	S0022094	DIODE,1SS355
J7	E0152760	CONN,2199SBDI18G1380 G
J8	E0113560	CONNECTOR,S 2B-ZR G
J9	E0113560	CONNECTOR,S 2B-ZR G
J10	E0136530	JACK,JY-3530-01-030 G
J11	E0139410	JACK,JY-6314-01-340 G
J12	E0139410	JACK,JY-6314-01-340 G
L13	E0126164	BEAD COIL,BLM18PG471SN1D G
L14	E0126164	BEAD COIL,BLM18PG471SN1D G
Q9	S0066984	TRANSISTOR,2SA1037AK TP G
Q10	S0073024	TRANSISTOR,2SC4081 TP G
Q11	S0078604	TRANSISTOR,IMX25 T110 G
Q12	S0070354	FET,2SK208GR TP G
SW1	E0140930	SW,SLIDE SSAA120200 G
U16	S0079803	IC,PCM3794ARHBR G
U17	E0124074	FILTER,EXCCET101U G
U18	E0124074	FILTER,EXCCET101U G
U19	E0124074	FILTER,EXCCET101U G
U20	S0064634	IC,NJM4580V-TE2 G
U21	E0124074	FILTER,EXCCET101U G
U22	E0124074	FILTER,EXCCET101U G
U23	E0124074	FILTER,EXCCET101U G
U24	S0064184	IC,PQ1X331M2ZPH G
VR2	R0193310	VAR RES,K1010GBV1B203BF G
W200	M0293240	LEAF SPR,BSG-25*65*080 G
W201	M0293240	LEAF SPR,BSG-25*65*080 G
W203	M0293240	LEAF SPR,BSG-25*65*080 G

REF.NO.	PARTS NO.	DESCRIPTION
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# 10. Included Accessories

## 付属品

### Included Accessories

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	D01054901B	OWNERS MNL,(J) DP004 G [ JEX ]	
	D01054920A	OWNERS MNL,(E) DP004 G	
	D01054920A	OWNERS MNL,(E) DP004 G	
	D01055980A	OWNERS MNL,QSG(D)DP004 G [ E ]	
	D01055981A	OWNERS MNL,QSG(F)DP004 G [ E ]	
	D01055982A	OWNERS MNL,QSG(I)DP004 G [ E ]	
	D01055983A	OWNERS MNL,QSG(S)DP004 G [ E ]	
	T0015810	SD CARD,PS8005 1GB G [ Except US/C ]	
	T0016350	SD CARD,AF1GSD TEAC01 G [ US/C ]	
	E01536100A	BAT,LR6(GD)2P(E)O NF D G	
	E0135680	USBB CABLE,CA3096080A37 G	

### NOTES

- PC boards shown are viewed from parts side.
- Parts marked with \* require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in this manual.
- △ Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.  
[ J ]: JAPAN [ US/C ]: U.S.A./CANADA [ K ]: KOREA [ E ]: EUROPE  
[ UK ]: U.K. [ A ]: AUSTRALIA [ T ]: TAIWAN [ JEX ]: JAPAN & ASIA  
[ CH ]: CHINA

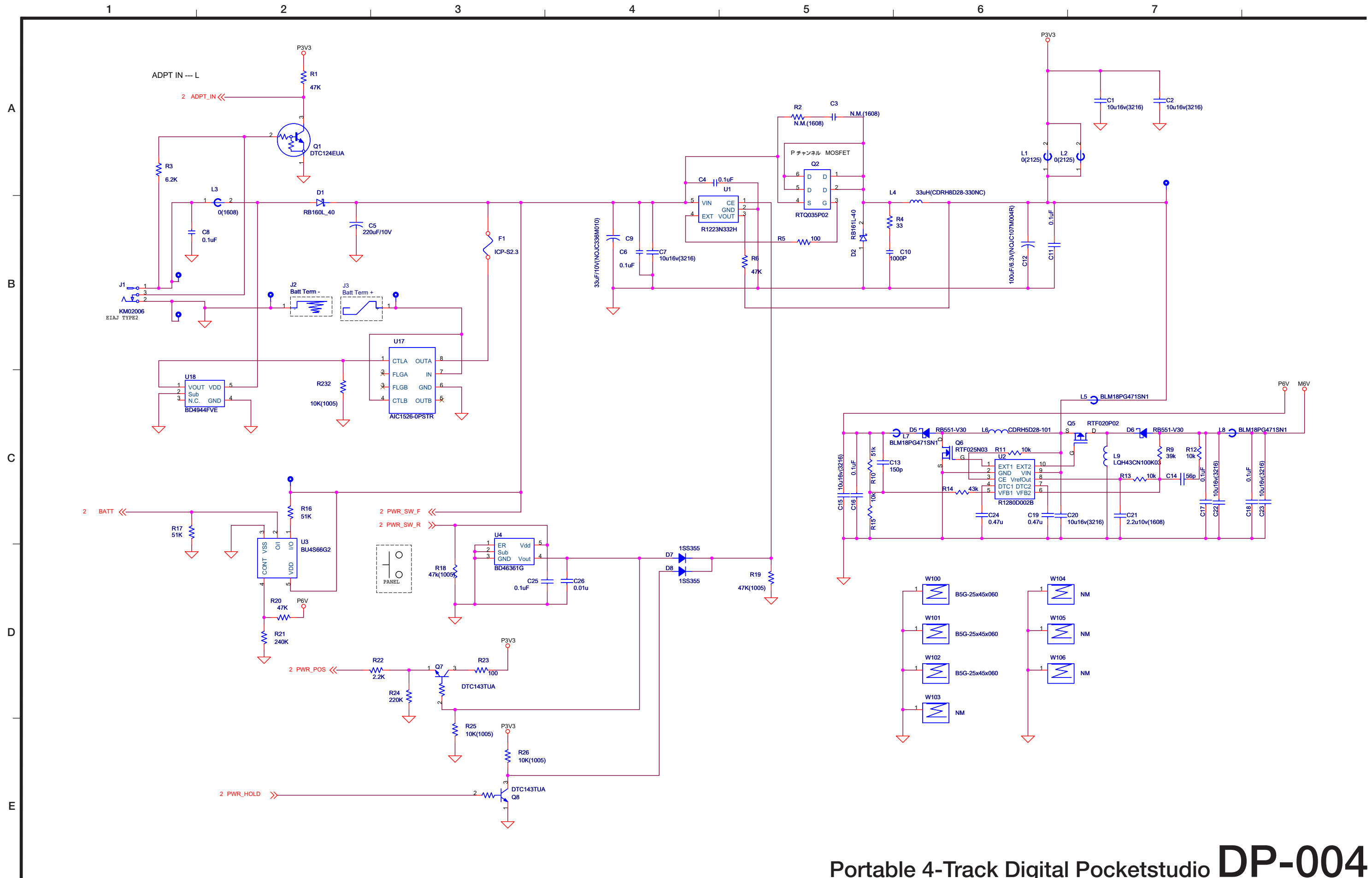
### 注意

- プリント基板図は部品面を示しています。
- \*印の部品は納期が若干かかります。  
あらかじめご了承ください。
- 分解図に部番のない部品および品番のない部品は供給できません。
- 標準の抵抗、コンデンサーは省略してあります。  
回路図を参照してください。
- △印は安全重要部品です。  
交換する時は必ず指定の部品を使用してください。
- 仕向先  
[ J ]: JAPAN [ US/C ]: U.S.A./CANADA [ K ]: KOREA  
[ E ]: EUROPE [ UK ]: U.K. [ A ]: AUSTRALIA  
[ T ]: TAIWAN [ JEX ]: JAPAN & ASIA [ CH ]: CHINA

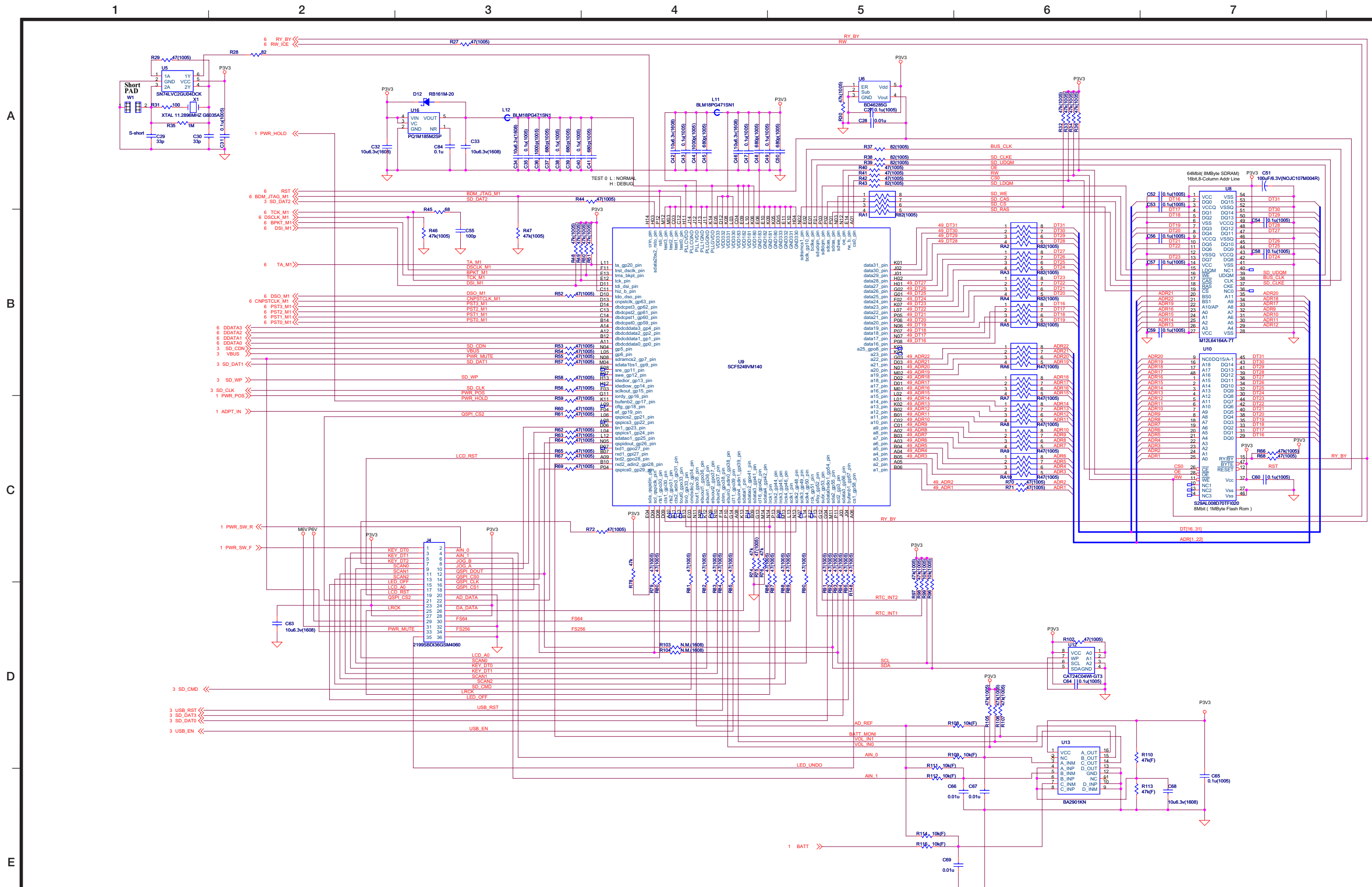
**SCHEMATIC DIAGRAM**  
**回路図**

**CONTENTS 目次**

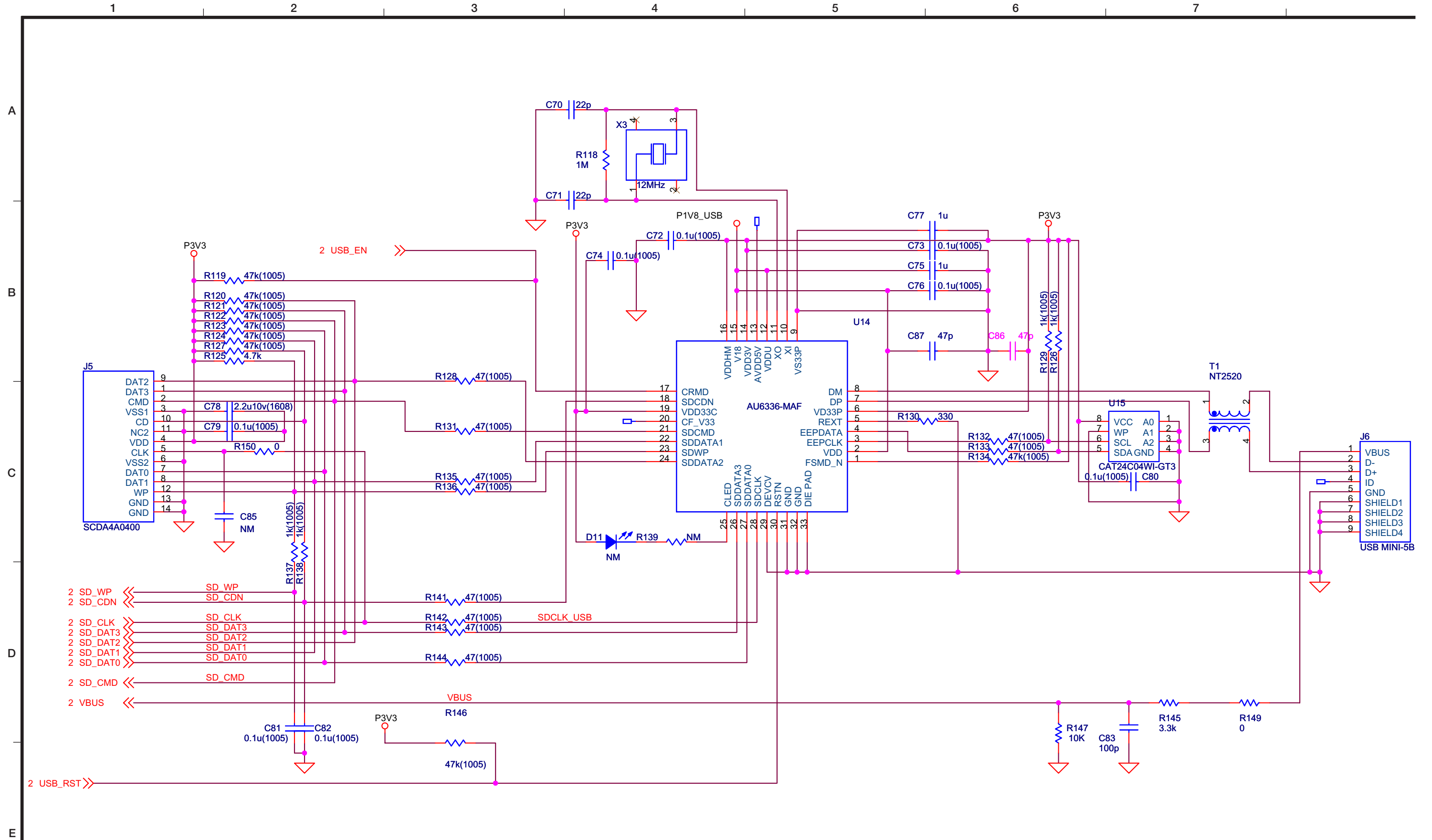
MAIN (1/4) .....	2
MAIN (2/4) .....	3
MAIN (3/4) .....	4
MAIN (4/4) .....	5
ANALOG (1/2) .....	6
ANALOG (2/2) .....	7
PANEL .....	8



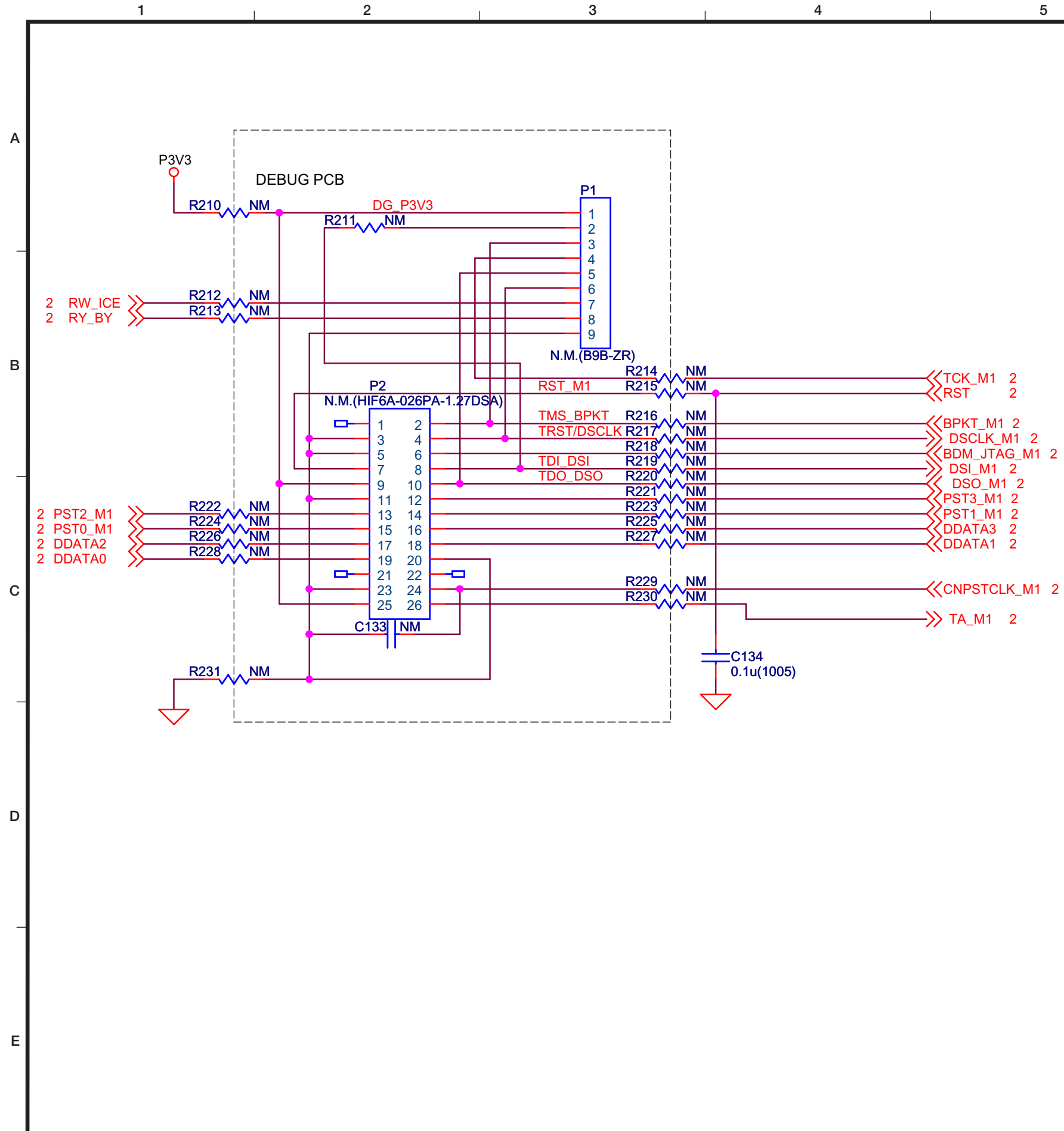
Portable 4-Track Digital Pocketstudio **DP-004**

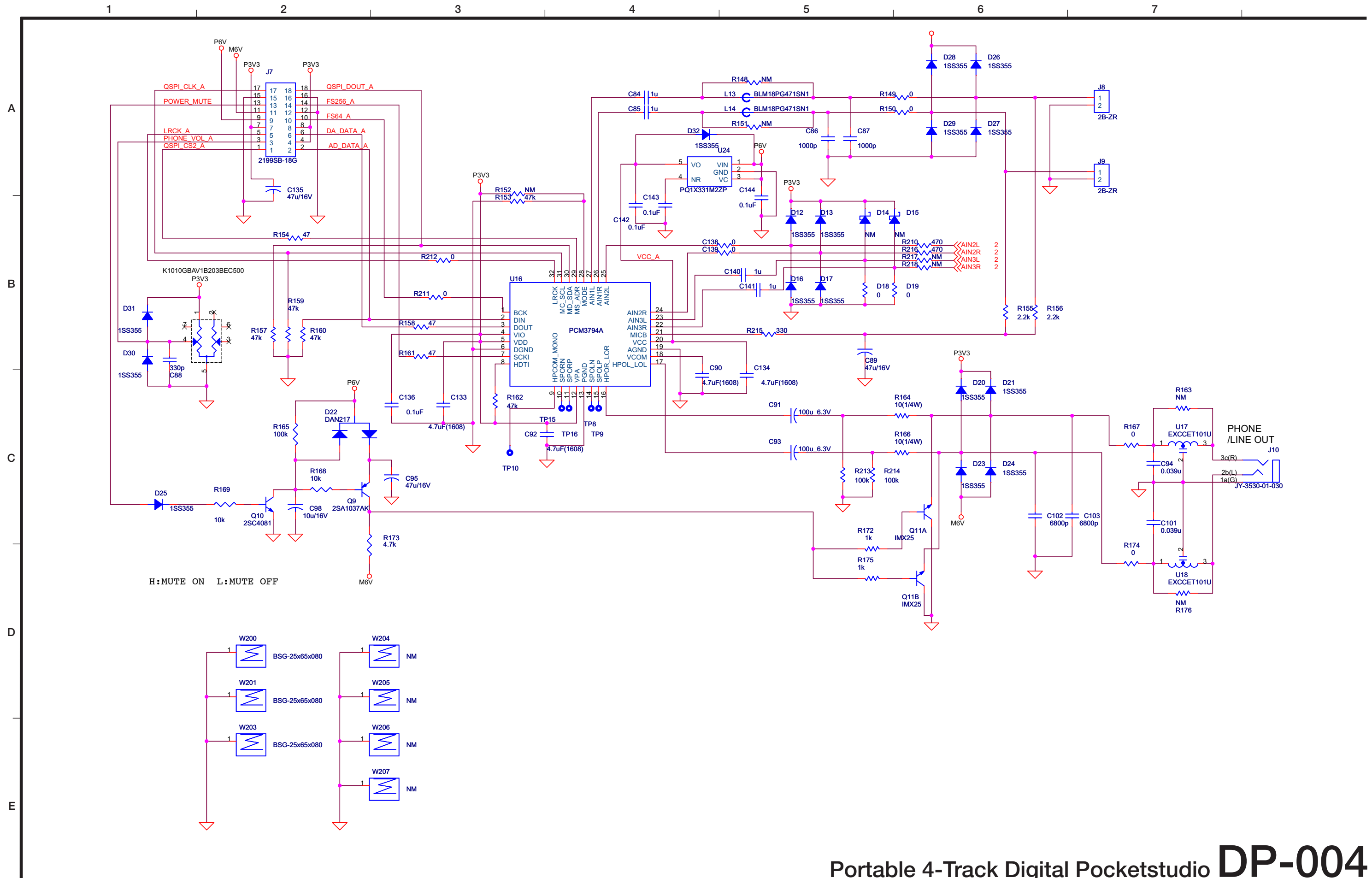


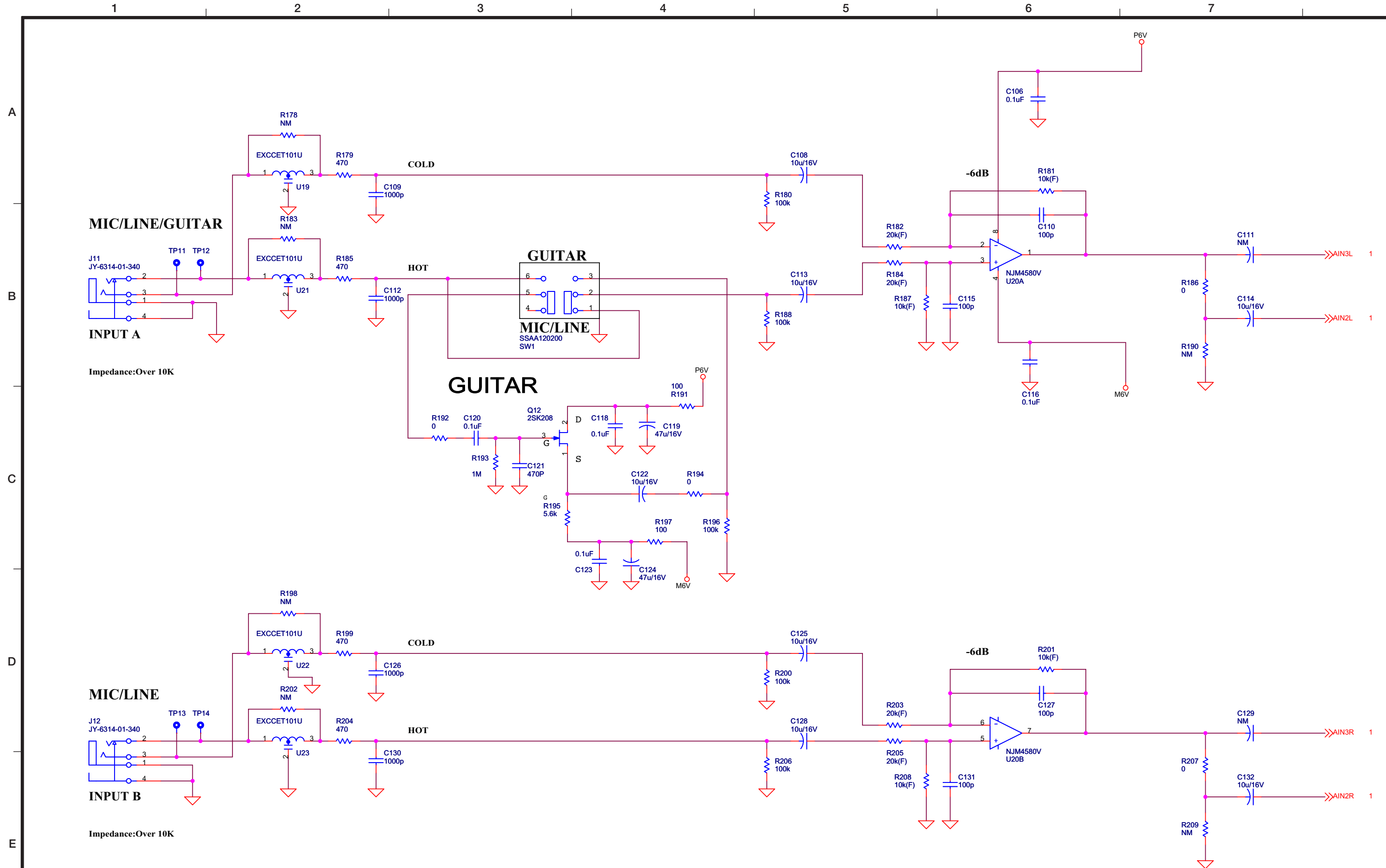
# Portable 4-Track Digital Pocketstudio DP-004



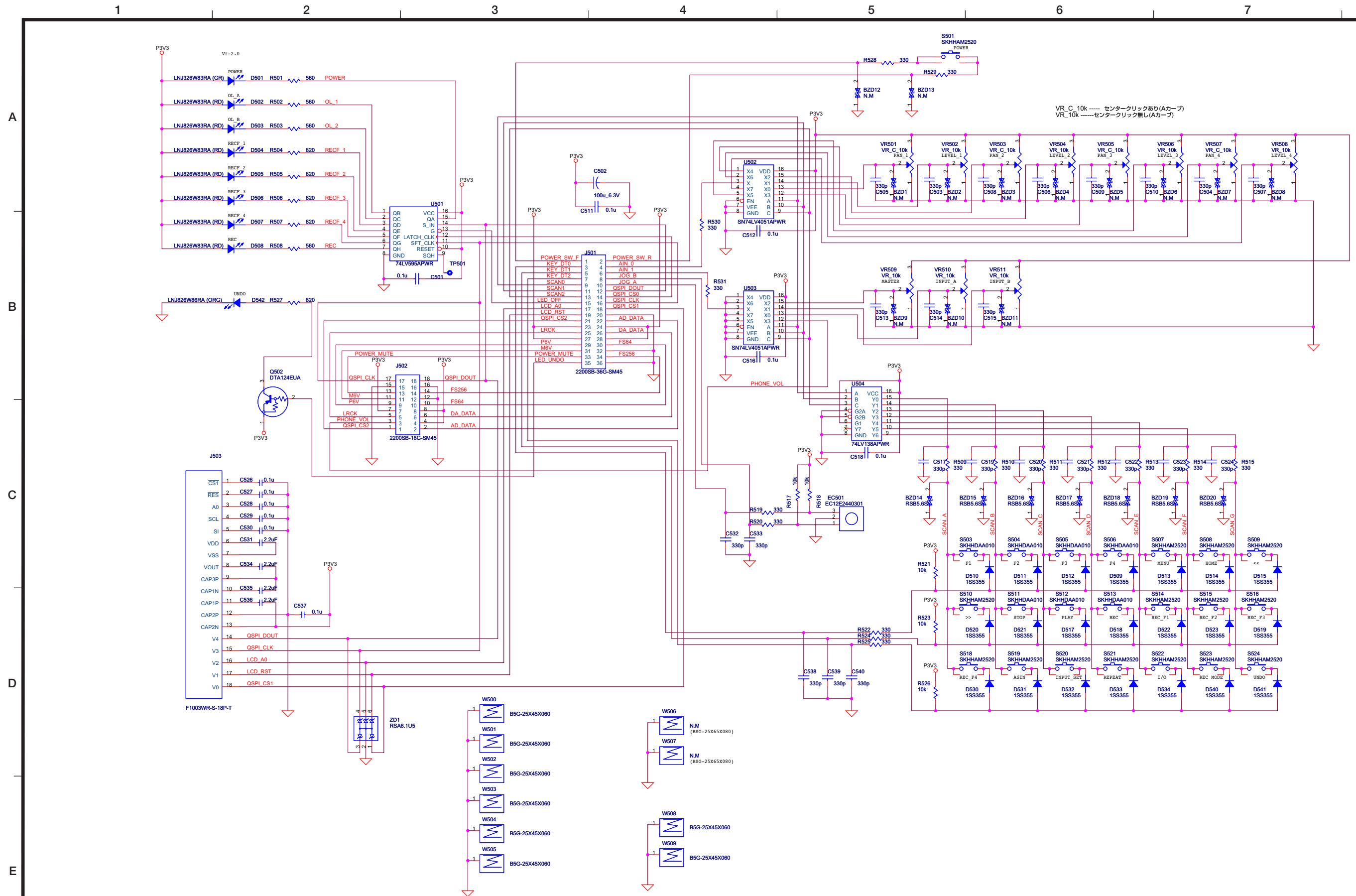
Portable 4-Track Digital Pocketstudio **DP-004**



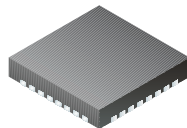




Portable 4-Track Digital Pocketstudio **DP-004**



Portable 4-Track Digital Pocketstudio **DP-004**



## 16-Bit, Low-Power Stereo Audio CODEC With Microphone Bias, Headphone, and Digital Speaker Amplifier

### FEATURES

- **Analog Front End:**
  - Stereo Single-Ended Input With Multiplexer
  - Mono Differential Input
  - Stereo Programmable Gain Amplifier
  - Microphone Amplifier (20 dB) and Bias
- **Analog Back End:**
  - Stereo/Mono Line Output With Volume
  - Stereo/Mono Headphone Amplifier With Volume and Capless Mode
  - Stereo/Mono Digital Speaker Amplifier (BTL) With Volume
- **Analog Performance:**
  - Dynamic Range: 93 dB (DAC)
  - Dynamic Range: 90 dB (ADC)
  - 40-mW + 40-mW Headphone Output at  $R_L = 16 \Omega$
  - 700-mW + 700-mW Speaker Output at  $R_L = 8 \Omega$
- **Power Supply Voltage**
  - 1.71 V to 3.6 V for Digital I/O Section
  - 1.71 V to 3.6 V for Digital Core Section
  - 2.4 V to 3.6 V for Analog Section
  - 2.4 V to 3.6 V for Power Amplifier Section
- **Low Power Dissipation:**
  - 7 mW in Playback, 1.8 V/2.4 V, 48 kHz
  - 13 mW in Record, 1.8 V/2.4 V, 48 kHz
  - 3.3  $\mu$ W in Power Down
- **Sampling Frequency: 5 kHz to 50 kHz**
- **Automatic Level Control for Recording**
- **Operation From a Single Clock Input Without PLL**
- **System Clock:**
  - Common-Audio Clock (256  $f_s$ /384  $f_s$ ), 12/24, 13/26, 13.5/27, 19.2/38.4, 19.68/39.36 MHz
- **Headphone Plug Insert Detection**
- **2 (I<sup>2</sup>C) or 3 (SPI) Wire Serial Control**
- **Programmable Function by Register Control:**
  - Digital Attenuation of DAC: 0 dB to –62 dB
  - Digital Gain of DAC: 0, 6, 12, 18 dB
  - Power Up/Down Control for Each Module
  - 6-dB to –70-dB Gain for Analog Outputs
  - 30-dB to –12-dB Gain for Analog Inputs
  - 0/20 dB Selectable for Microphone Input
  - 0-dB to –21-dB Gain for Analog Mixing
  - Parameter Settings for ALC
  - Three-Band Tone Control and 3D Sound
  - High-Pass Filter: 4-, 120-, 240-Hz
  - Two-Stage Programmable Notch Filter
  - Analog Mixing Control
- **Pop-Noise Reduction Circuit**
- **Short and Thermal Protection Circuit**
- **Package: 5-mm × 5-mm QFN Package**
- **Operation Temperature Range: –40°C to 85°C**

### APPLICATIONS

- Portable Audio Player, Cellular Phone
- Video Camcorder, Digital Movie/Still Camera
- PMP/DMB

### DESCRIPTION

The PCM3793A/94A is a low-power stereo CODEC designed for portable digital audio applications. The device integrates stereo digital speaker amplifier, headphone amplifier, line amplifier, line input, boost amplifier, microphone bias, programmable gain control, analog mixing, sound effects, and automatic level control (ALC). It is available in a small-footprint, 5-mm × 5-mm QFN package. The PCM3793A/94A supports right-justified, left-justified, I<sup>2</sup>S, and DSP formats, providing easy interfacing to audio DSP and decoder/encoder chips. Sampling rates up to 50 kHz are supported. The user-programmable functions are accessible through a two- or three-wire serial control port.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MAX	UNIT
Supply voltage	$V_{DD}, V_{IO}, V_{CC}, V_{PA}$	-0.3 to 4	V
Ground voltage differences: DGND, AGND, PGND		±0.1	V
Input voltage		-0.3 to 4	V
Input current (any pins except supplies and SPK out)		±10	mA
Ambient temperature under bias		-40 to 110	°C
Storage temperature		-55 to 150	°C
Junction temperature		150	°C
Lead temperature (soldering)		260	°C, 5 s
Package temperature (reflow, peak)		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC}, V_{PA}$	Analog supply voltage	2.4	3.3	3.6	V
$V_{DD}, V_{IO}$	Digital supply voltage	1.71	3.3	3.6	V
Digital input logic family		CMOS			
Digital input clock frequency	SCKI system clock	3.072		18.432	MHz
	LRCK sampling clock	8		48	kHz
Analog output load resistance	LOL and LOR	10			k $\Omega$
	HPOL and HPOR	16			$\Omega$
	SPOLP, SPOLN, SPORP and SPORN	8			$\Omega$
Analog output load capacitance				30	pF
Digital output load capacitance				10	pF
$T_A$	Operating free-air temperature	-40		85	°C

## ELECTRICAL CHARACTERISTICS

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , and 16-bit data (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PCM3793ARHB, PCM3794ARHB			UNIT
			MIN	TYP	MAX	
<b>Audio Data Characteristics</b>						
<b>DATA FORMAT</b>						
Resolution			16			Bits
Audio data interface format			I <sup>2</sup> S, left-, right-justified, DSP			
Audio data bit length			16			Bits
Audio data format			MSB first, 2s complement			
Sampling frequency ( $f_S$ )			5		50	kHz
System clock		$V_{DD} < 2\text{ V}$			27	MHz
		$V_{DD} > 2\text{ V}$			40	
<b>Digital Input/Output</b>						
Logic family			CMOS compatible			
$V_{IH}$	Input logic level		0.7 $V_{IO}$			VDC
$V_{IL}$			0.3 $V_{IO}$			
$I_{IH}$	Input logic current	$V_{IN} = 3.3\text{ V}$			10	$\mu\text{A}$
$I_{IL}$		$V_{IN} = 0\text{ V}$			-10	
$V_{OH}$	Output logic level	$I_{OH} = -2\text{ mA}$	0.75 $V_{IO}$			VDC
$V_{OL}$		$I_{OL} = 2\text{ mA}$			0.25 $V_{IO}$	
<b>Digital Input to Line Output Through DAC (LOL, LOR, and MONO)</b>						
$R_L = 10\text{ k}\Omega$ , ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = disabled						
<b>DYNAMIC PERFORMANCE</b>						
Full-scale output voltage		0 dB	2.828			Vp-p
			1			Vrms
Dynamic range		EIAJ, A-weighted	93			dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted	86	93		dB
Channel separation			91			dB
THD+N	Total harmonic distortion + noise	0 dB	0.008%			
Load resistance			10			k $\Omega$
<b>Line Input to Line Output Through Mixing Path (LOL, LOR, and MONO)</b>						
$R_L = 10\text{ k}\Omega$ , ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = enabled						
<b>DYNAMIC PERFORMANCE</b>						
Full-scale input and output voltage		0 dB	2.828			Vp-p
			1			Vrms
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93		dB

**ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $256\text{ f}_S$ , and 16-bit data (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PCM3793ARHB, PCM3794ARHB			UNIT
			MIN	TYP	MAX	
<b>Digital Input to Headphone Output Through DAC (HPOL and HPOR)</b>						
$R_L = 16\ \Omega$ or $32\ \Omega$ , ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = disabled, not capless mode						
<b>DYNAMIC PERFORMANCE</b>						
Full-scale output voltage		0 dB	2.828		Vp-p	
			1		Vrms	
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93	dB	
THD+N	Total harmonic distortion + noise	30 mW, $R_L = 32\ \Omega$ , volume = 0 dB	0.1%			
		40 mW, $R_L = 16\ \Omega$ , volume = -1 dB	0.03%			
Load resistance			16		$\Omega$	
PSRR	Power-supply rejection ratio	200 Hz, 140 mVp-p	-40		dB	
		1 kHz, 140 mVp-p	-45			
		20 kHz, 140 mVp-p	-32			
<b>Line Input to Headphone Output Through Mixing Path (HPOL and HPOR)</b>						
$R_L = 16\ \Omega$ or $32\ \Omega$ , ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = enabled, not capless mode						
<b>DYNAMIC PERFORMANCE</b>						
Full-scale output voltage		0 dB	2.828		Vp-p	
			1		Vrms	
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93	dB	
Load resistance			16		$\Omega$	
<b>Digital Input to Speaker Output Through DAC (SPOLP, SPOLN, SPORP, and SPORN): PCM3793A</b>						
$R_L = 8\ \Omega$ , ALC = OFF, volume = 0 dB, headphone = powered down, analog mixing = disabled						
<b>DYNAMIC PERFORMANCE</b>						
Full-scale output voltage		0 dB	2.52		Vp-p	
			0.9		Vrms	
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	93	dB	
THD+N	Total harmonic distortion + noise	400 mW, $R_L = 8\ \Omega$ , volume = 0 dB	0.3%			
Load resistance			8		$\Omega$	
PSRR	Power-supply rejection ratio	200 Hz, 140 mVp-p	-50		dB	
		1 kHz, 140 mVp-p	-45			
		20 kHz, 140 mVp-p	-25			
<b>Line Input to Speaker Output Through Mixing Path (SPOLP, SPOLN, SPORP, and SPORN): PCM3793A</b>						
$R_L = 8\ \Omega$ , ALC = OFF, volume = 0 dB, headphone = powered down, analog mixing = enabled						
<b>DYNAMIC PERFORMANCE</b>						
Full-scale output voltage		0 dB	2.52		Vp-p	
			0.9		Vrms	
SNR	Signal-to-noise ratio	EIAJ, A-Weighted	84	93	dB	

## ELECTRICAL CHARACTERISTICS (continued)

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , and 16-bit data (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PCM3793ARHB, PCM3794ARHB			UNIT	
		MIN	TYP	MAX		
<b>Line Input to Digital Output Through ADC (AIN1L/R, AIN2L/R, AIN3L, and AIN3L/R)</b>						
ALC = OFF, microphone boost = 0 dB, PGA = 0 dB, speaker and headphone = powered down, analog mixing = disabled						
<b>DYNAMIC PERFORMANCE</b>						
Full-scale input voltage	0 dB	2.828			Vp-p	
		1			Vrms	
Dynamic range	EIAJ, A-weighted	90			dB	
SNR	Signal-to-noise ratio	EIAJ, A-weighted	83	90	dB	
	Channel separation		87			dB
THD+N	Total harmonic distortion + noise	-1 dB	0.009%			
<b>ANALOG INPUT</b>						
Center voltage		0.5 $V_{CC}$			V	
Input impedance		10	20	k $\Omega$		
<b>Microphone Bias</b>						
ALC = OFF, microphone boost = 0 dB, PGA = 0 dB, speaker and headphone = powered down, analog mixing = disabled						
Bias voltage		0.75 $V_{CC}$			V	
Bias source current		2			mA	
Output noise		6.5			$\mu\text{V}$	
<b>Filter Characteristics</b>						
<b>INTERPOLATION FILTER FOR DAC</b>						
Pass band		0.454 $f_S$				
Stop band		0.546 $f_S$				
Pass-band ripple		$\pm 0.04$			dB	
Stop-band attenuation		-50			dB	
Group delay		19/ $f_S$			s	
De-emphasis error		$\pm 0.1$			dB	
<b>ANALOG FILTER FOR DAC</b>						
Frequency response	$f = 20\text{ kHz}$	$\pm 0.2$			dB	
<b>DECIMATION FILTER FOR ADC</b>						
Pass band		0.408 $f_S$				
Stop band		0.591 $f_S$				
Pass-band ripple		$\pm 0.02$			dB	
Stop-band attenuation	$f < 3.268 f_S$	-60			dB	
Group delay		17/ $f_S$			s	
<b>HIGH-PASS FILTER FOR ADC</b>						
Frequency response	-3 dB, $f_c = 4\text{ Hz}$	3.74			Hz	
	-0.5 dB, $f_c = 4\text{ Hz}$	10.66				
	-0.1 dB, $f_c = 4\text{ Hz}$	24.2				
	-3 dB, $f_c = 240\text{ Hz}$	235.68				
	-0.5 dB, $f_c = 240\text{ Hz}$	609.95				
	-0.1 dB, $f_c = 240\text{ Hz}$	2601.2				

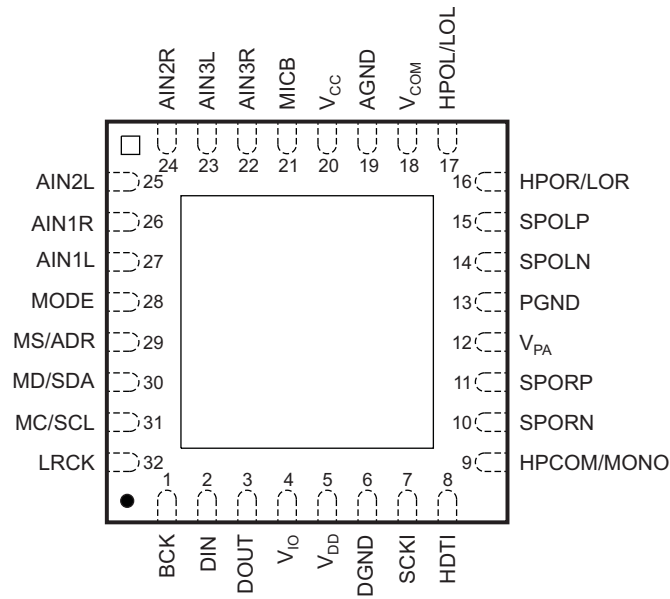
**ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock = 256  $f_S$ , and 16-bit data (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PCM3793ARHB, PCM3794ARHB			UNIT
			MIN	TYP	MAX	
<b>Power Supply and Supply Current</b>						
$V_{IO}$	Voltage range		1.71	3.3	3.6	VDC
$V_{DD}$			1.71	3.3	3.6	
$V_{CC}$			2.4	3.3	3.6	
$V_{PA}$			2.4	3.3	3.6	
Supply current		BPZ input, all active, no load		24.3	35	mA
		All inputs are held static		1	10	$\mu\text{A}$
Power dissipation		BPZ input		80.2	115.5	mW
		All inputs are held static		3.3	33	$\mu\text{W}$
<b>Temperature Condition</b>						
Operation temperature			-40		85	$^\circ\text{C}$
$\theta_{JA}$	Thermal resistance			30		$^\circ\text{C/W}$

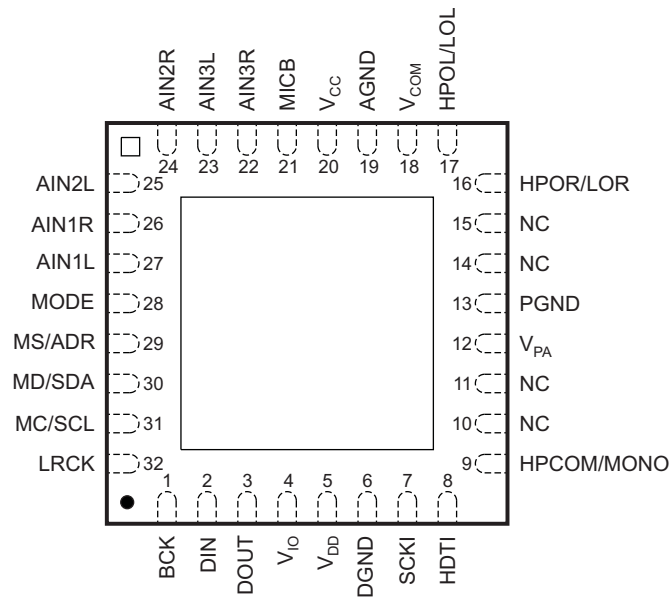
**PIN ASSIGNMENTS**

**PCM3793ARHB  
(TOP VIEW)**



P0048-05

**PCM3794ARHB  
(TOP VIEW)**

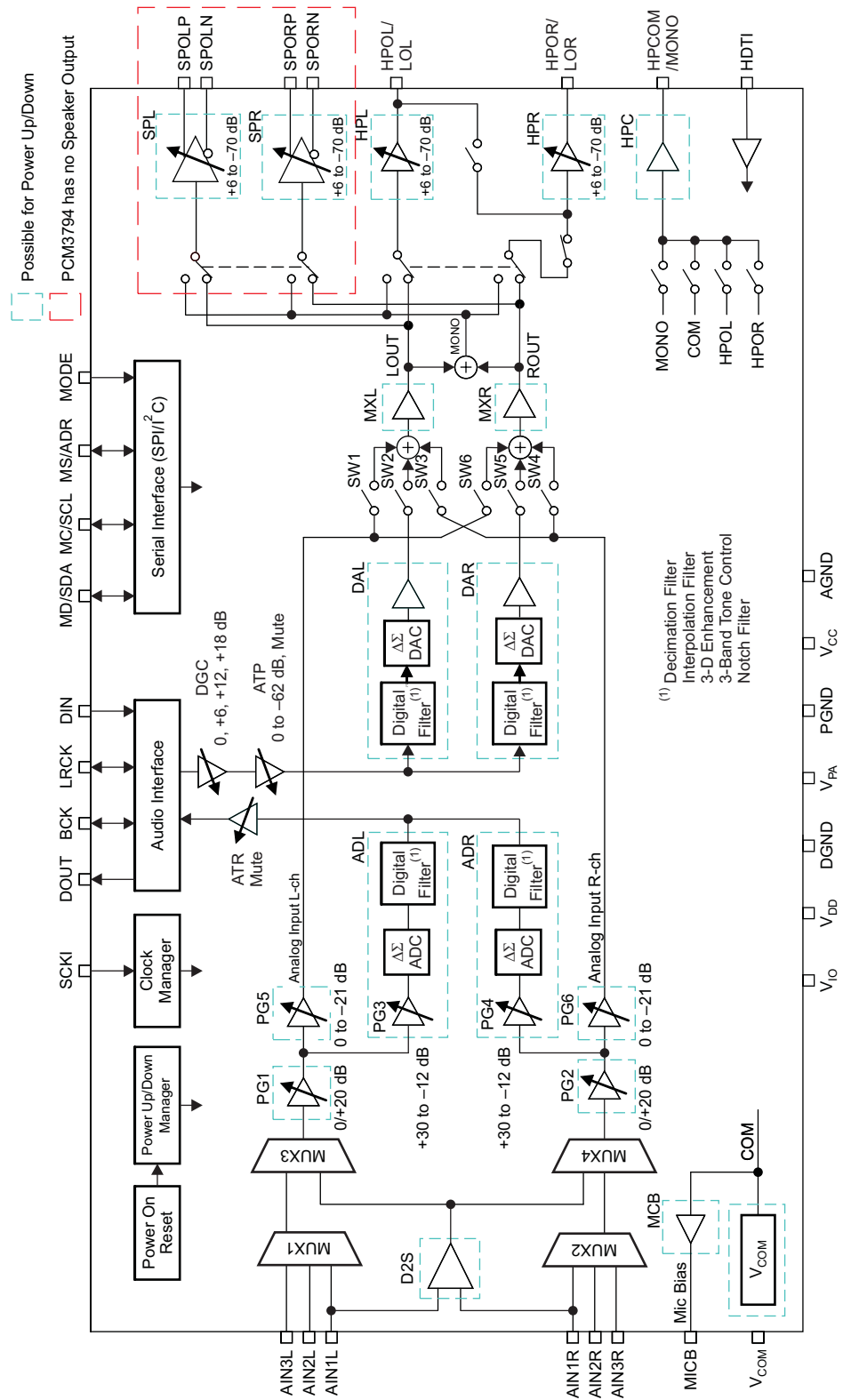


P0048-06

**Table 1. TERMINAL FUNCTIONS**

TERMINAL			I/O	DESCRIPTION
NAME	PCM3793ARHB	PCM3794ARHB		
AGND	19	19	–	Ground for analog
AIN1L	27	27	I	Analog input 1 for L-channel
AIN1R	26	26	I	Analog input 1 for R-channel
AIN2L	25	25	I	Analog input 2 for L-channel
AIN2R	24	24	I	Analog input 2 for R-channel
AIN3L	23	23	I	Analog input 3 for L-channel
AIN3R	22	22	I	Analog input 3 for R-channel
BCK	1	1	I/O	Serial bit clock
DGND	6	6	–	Digital ground
DIN	2	2	I	Serial audio data input
DOUT	3	3	O	Serial audio data output
HDTI	8	8	I	Headphone plug insertion detection
HPCOM/MONO	9	9	O	Headphone common/mono line output
HPOL/LOL	17	17	O	Headphone/lineout for R-channel
HPOR/LOR	16	16	O	Headphone/lineout for L-channel
LRCK	32	32	I/O	Left and right channel clock
MC/SCL	31	31	I	Mode control clock for three-wire/two-wire interface
MD/SDA	30	30	I/O	Mode control data for three-wire/two-wire interface
MICB	21	21	O	Microphone bias source output
MODE	28	28	I	Two- or three-wire interface selection (LOW: SPI, HIGH: I <sup>2</sup> C)
MS/ADR	29	29	I	Mode control select for three-wire/two-wire interface
PGND	13	13	–	Ground for speaker power amplifier
SCKI	7	7	I	System clock
SPOLN	14	–	O	Speaker output L-channel for negative (PCM3793A)
SPOLP	15	–	O	Speaker output L-channel for positive (PCM3793A)
SPORN	10	–	O	Speaker output R-channel for negative (PCM3793A)
SPORP	11	–	O	Speaker output R-channel for positive (PCM3793A)
V <sub>CC</sub>	20	20	–	Analog power supply
V <sub>COM</sub>	18	18	–	Analog common voltage
V <sub>DD</sub>	5	5	–	Power supply for digital core
V <sub>IO</sub>	4	4	–	Power supply for digital I/O
V <sub>PA</sub>	12	12	–	Power supply for power amplifier

FUNCTIONAL BLOCK DIAGRAM



B0181-02

### TYPICAL PERFORMANCE CURVES

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 8\text{ to }48\text{ kHz}$ , system clock =  $256 f_S$ , and 16-bit data, unless otherwise noted.

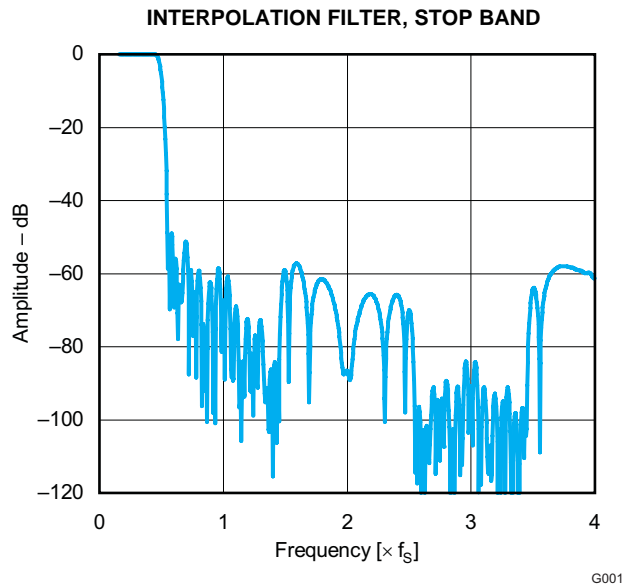


Figure 1.

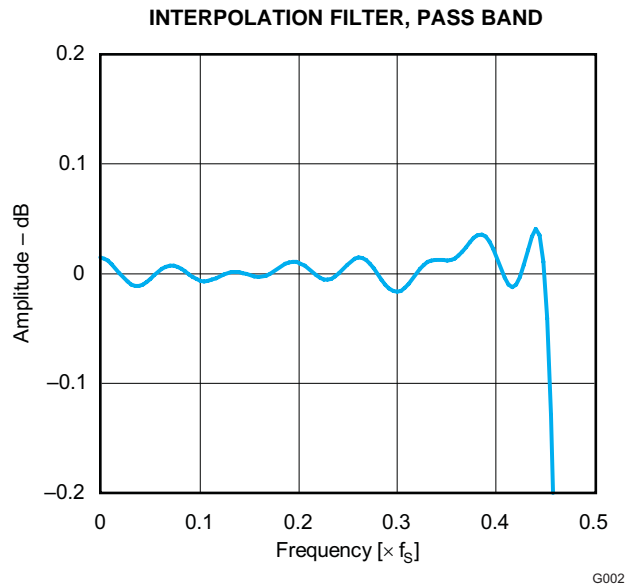


Figure 2.

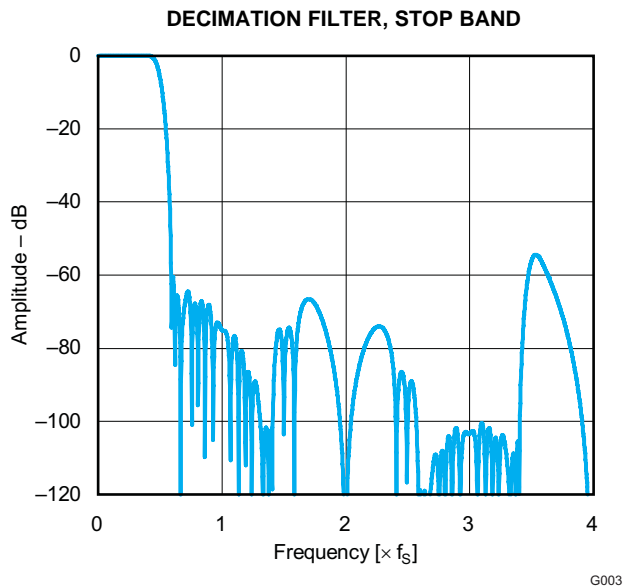


Figure 3.

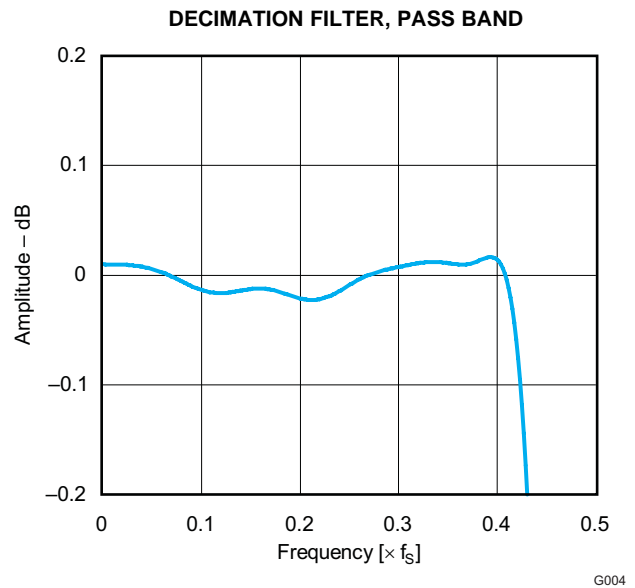


Figure 4.

**TYPICAL PERFORMANCE CURVES (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 8\text{ to }48\text{ kHz}$ , system clock =  $256 f_S$ , and 16-bit data, unless otherwise noted.

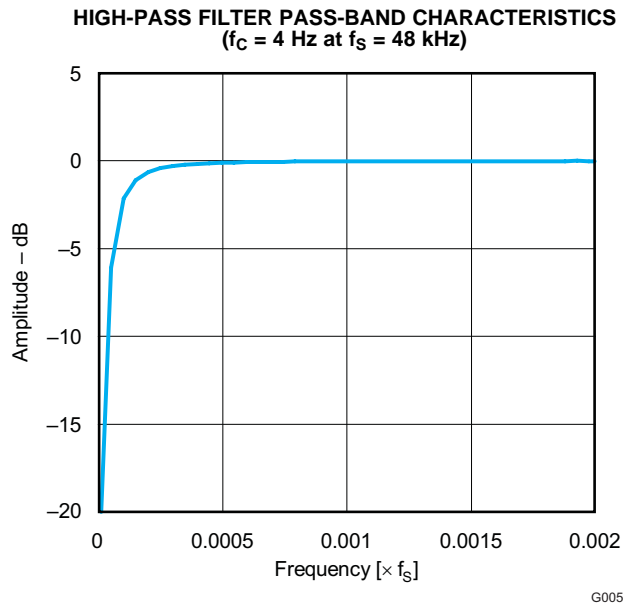


Figure 5.

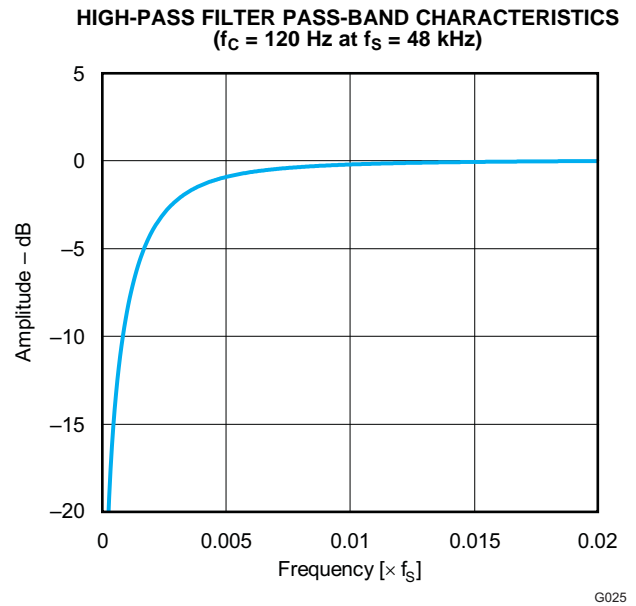


Figure 6.

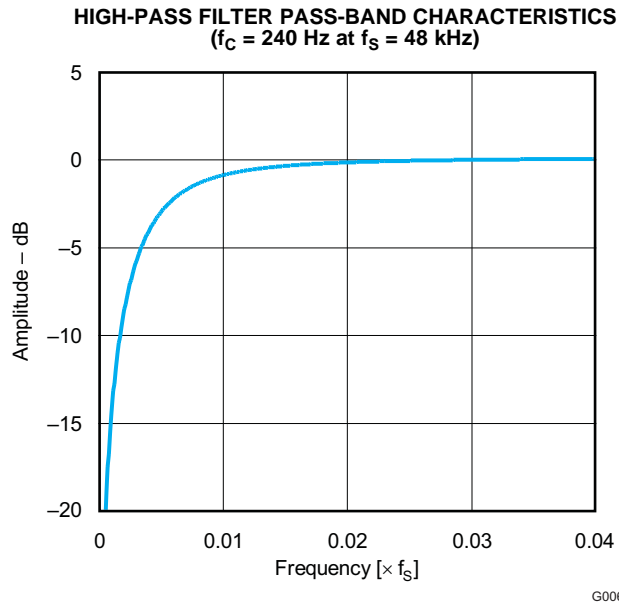
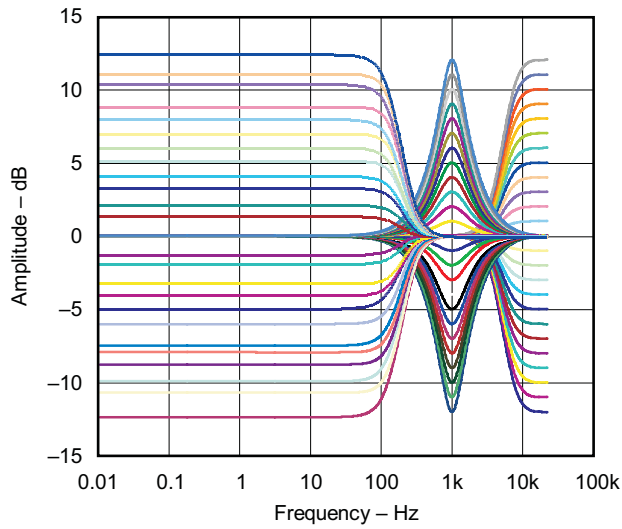


Figure 7.

**TYPICAL PERFORMANCE CURVES (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 44.1\text{ kHz}$ , system clock =  $256 f_S$ , and 16-bit data, unless otherwise noted.

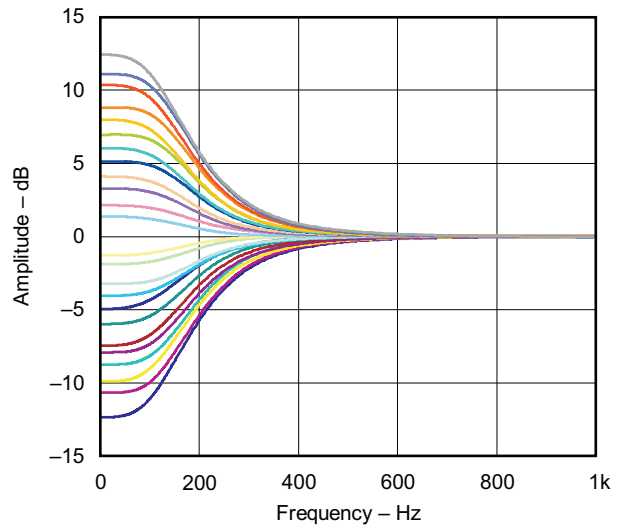
**THREE-BAND TONE CONTROL (BASS, MIDRANGE, TREBLE)**



**Figure 8.**

G007

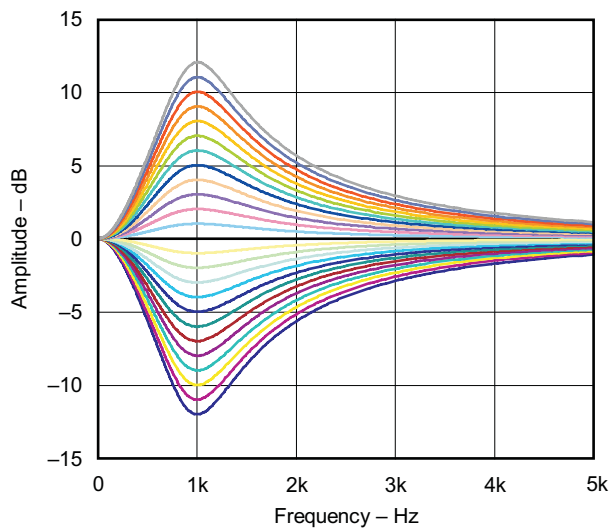
**THREE-BAND TONE CONTROL (BASS)**



**Figure 9.**

G008

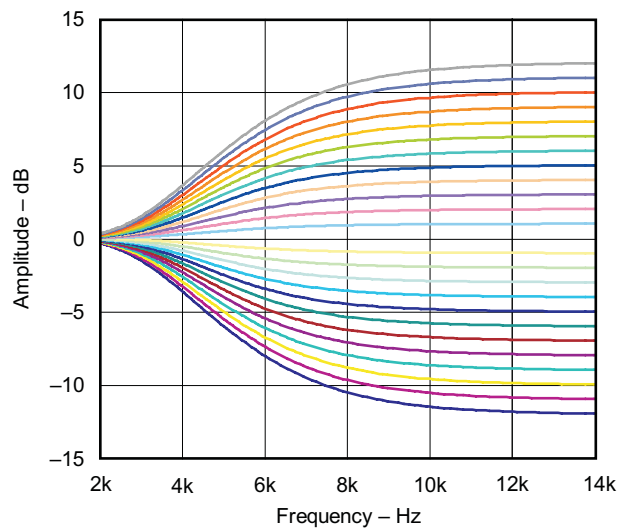
**THREE-BAND TONE CONTROL (MIDRANGE)**



**Figure 10.**

G009

**THREE-BAND TONE CONTROL (TREBLE)**

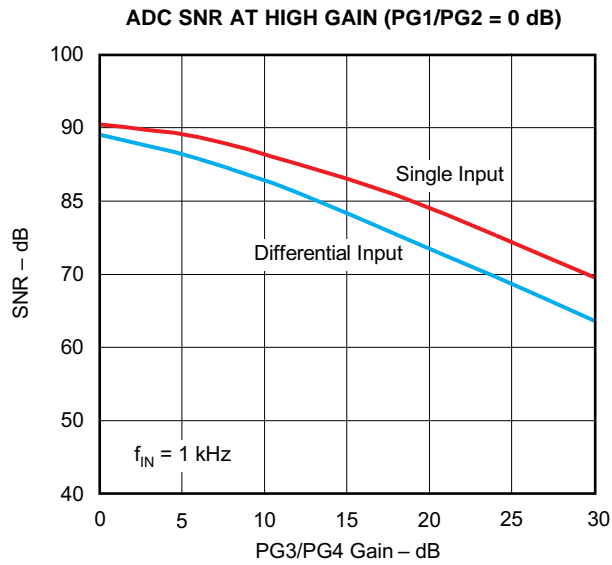


**Figure 11.**

G010

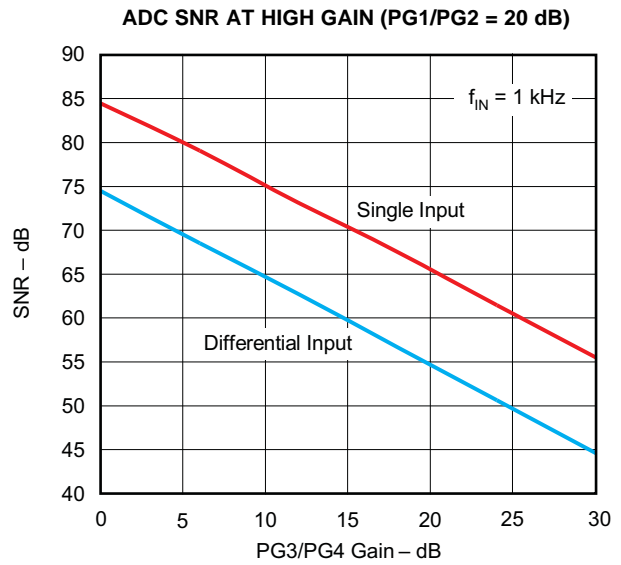
**TYPICAL PERFORMANCE CURVES (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , and 16-bit data, unless otherwise noted.



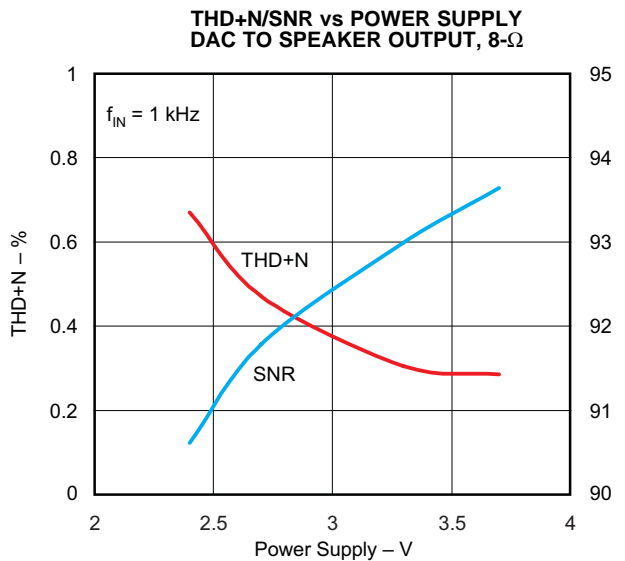
G011

Figure 12.



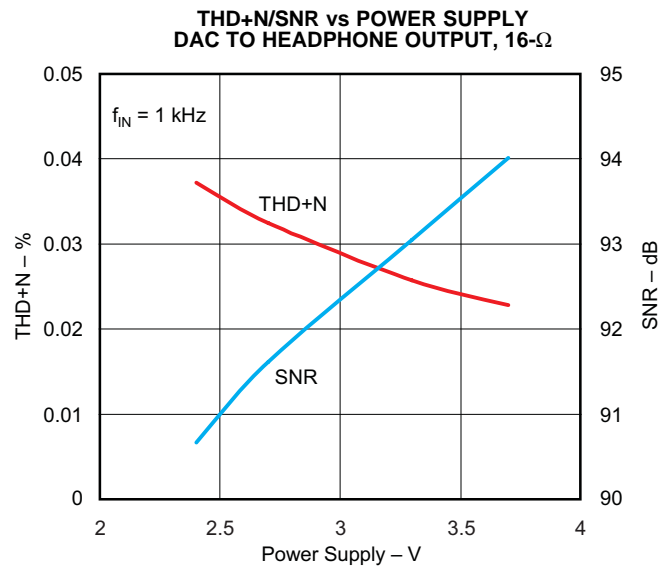
G012

Figure 13.



G013

Figure 14.



G014

Figure 15.

**TYPICAL PERFORMANCE CURVES (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , and 16-bit data, unless otherwise noted.

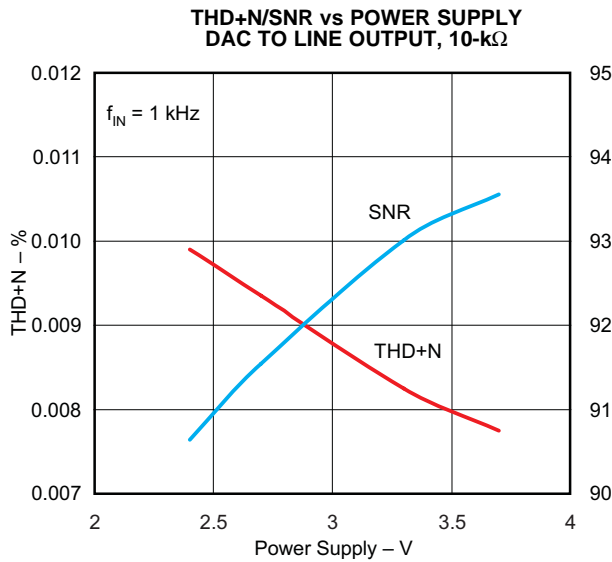


Figure 16.

G015

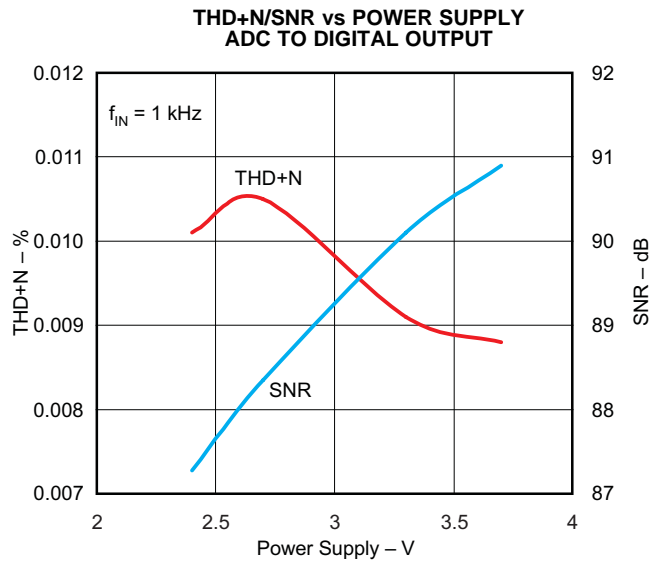


Figure 17.

G016

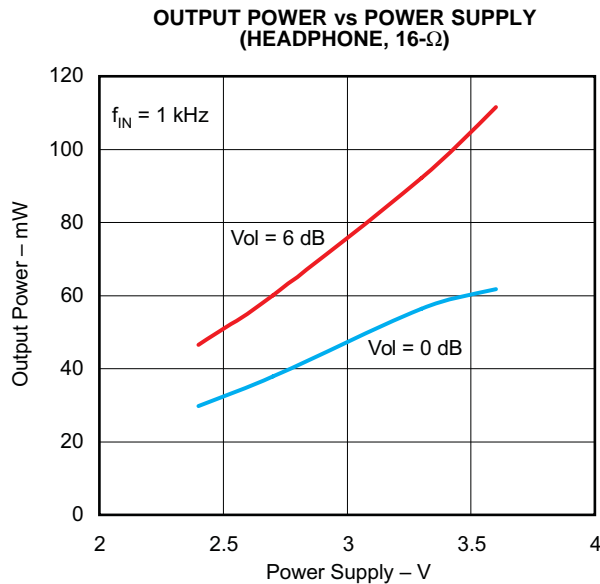


Figure 18.

G017

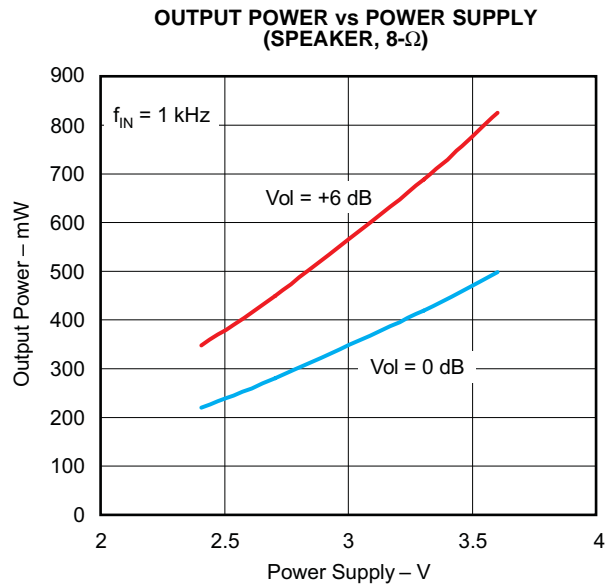


Figure 19.

G018

**TYPICAL PERFORMANCE CURVES (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_s = 48\text{ kHz}$ , system clock =  $256 f_s$ , and 16-bit data, unless otherwise noted.

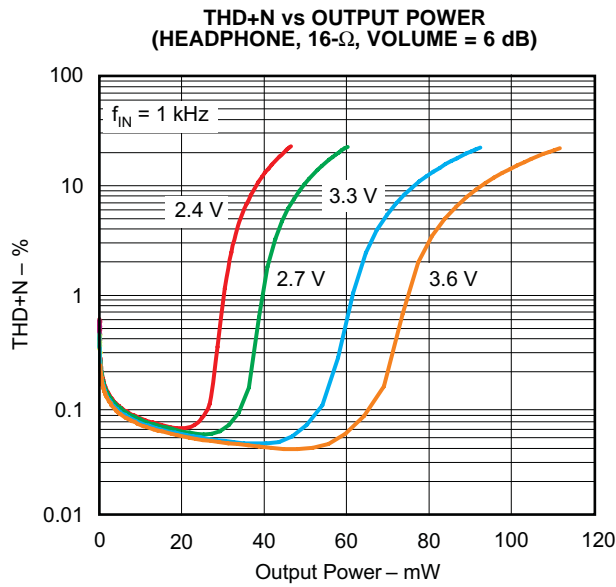


Figure 20.

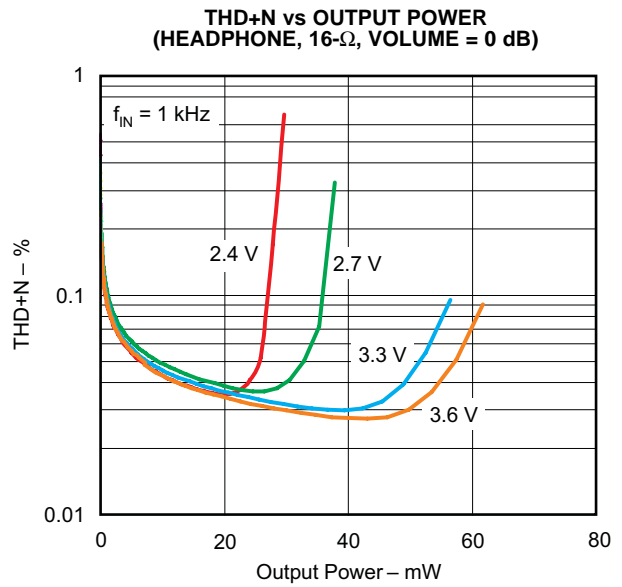


Figure 21.

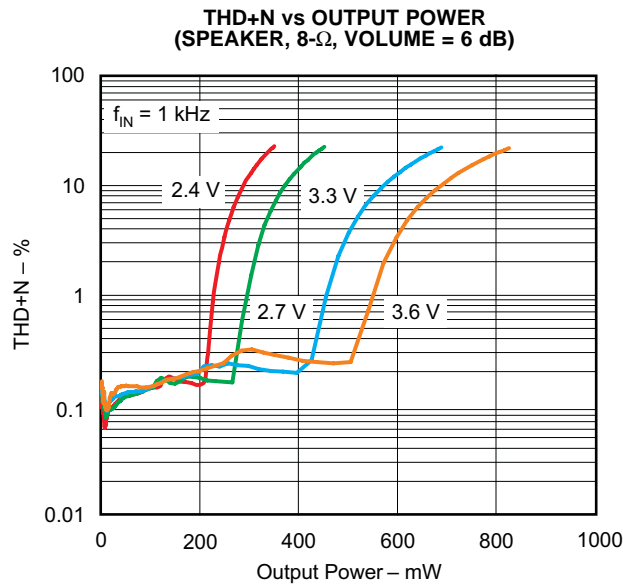


Figure 22.

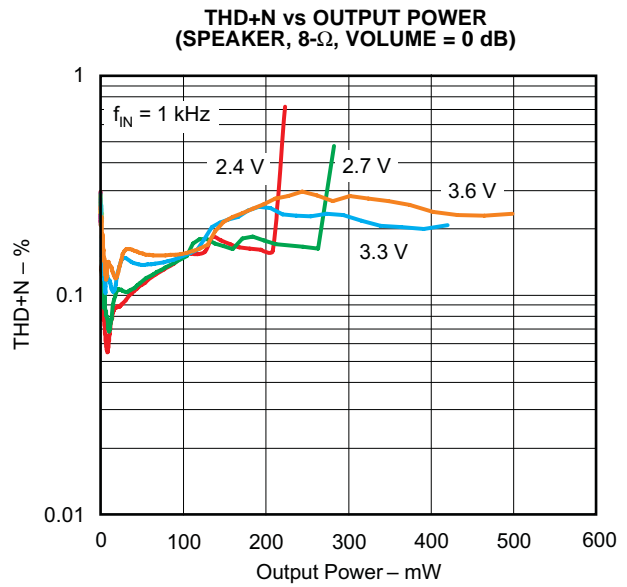
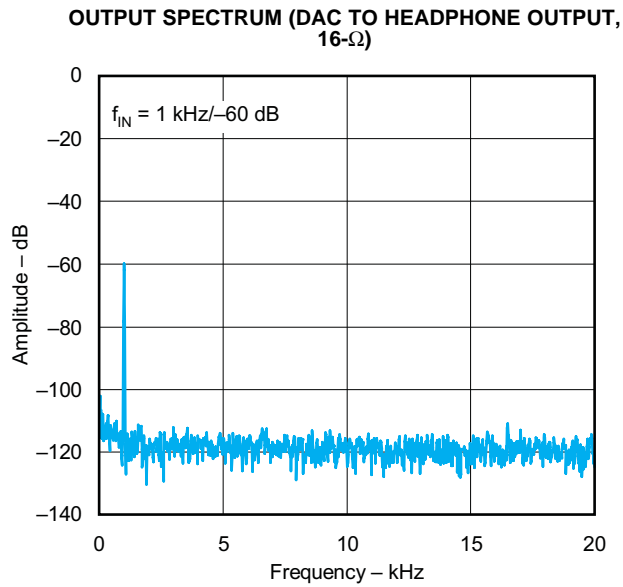


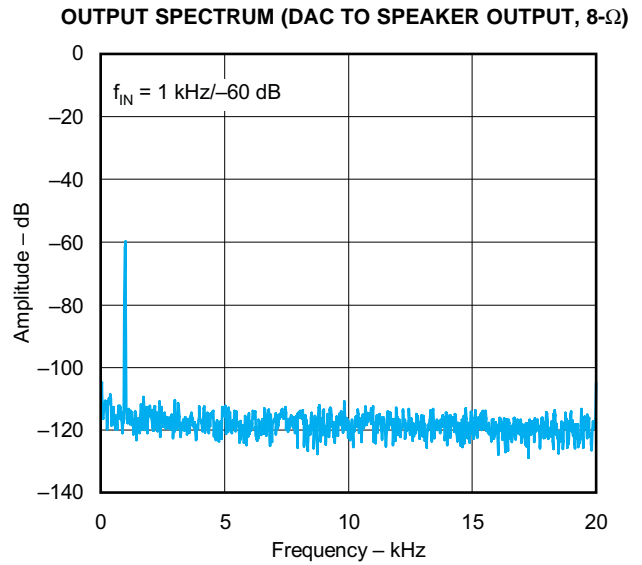
Figure 23.

**TYPICAL PERFORMANCE CURVES (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$ ,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , and 16-bit data, unless otherwise noted.



**Figure 24.**



**Figure 25.**

## PCM3793A/94A DESCRIPTION

### Analog Input

The AIN1L, AIN1R, AIN2L, AIN2R, AIN3L, and AIN3R pins can be used as microphone or line inputs with selectable 0- or 20-dB boost and 1-V<sub>rms</sub> input. All of these analog inputs have high input impedance (20 kΩ), which is not changed by gain settings. One pair of inputs is selected by register 87 (AIL[1:0], AIR[1:0]). AIN1L and AIN1R can be used as a monaural differential input.

### Gain Settings for Analog Input

The gain of the analog signals can be adjusted from 30 dB to –12 dB in 1-dB steps following the 0- or 20-dB boost amplifier. The gain level can be set for each channel by registers 79 and 80 (ALV[5:0], ARV[5:0]).

### A/D Converter

The ADC includes a multilevel delta-sigma modulator, aliasing filter, decimation filter, high-pass filter, and notch filter and can accept a 1-V<sub>rms</sub> full-scale voltage input. The decimation filter has a digital soft mute controlled by register 81 (RMUL, RMUR). The high-pass filter can be disabled by register 81 (HPF[1:0]), and the notch filter can be disabled by registers 96 to 104 if it is not necessary to cancel a dc offset or compensate for wind noise.

### D/A Converter

The DAC includes a multilevel delta-sigma modulator and an interpolation filter. These can be used to obtain high PSRR, low jitter sensitivity, and low out-of-band noise quickly and easily. The interpolation filter includes digital attenuator, digital soft mute, three-band tone control (bass, midrange and treble), and 3-D sound controlled by registers 92 to 95. The de-emphasis filter (32, 44.1 and 48 kHz) is controlled by registers 68 to 70 (ATL[5:0], ATR[5:0], PMUL, PMUR, DEM[1:0]). Oversampling rate control can reduce out-of-band noise when operating at low sampling rates by using register 70 (OVER).

### Common Voltage

The V<sub>COM</sub> pin is normally biased to 0.5 V<sub>CC</sub>, and it provides the common voltage to internal circuitry. It is recommended that a 4.7-μF capacitor be connected between this pin and AGND to provide clean voltage and avoid pop noise. The PCM3793A/94A may have a little pop noise on each analog output if a capacitor smaller than 4.7 μF is used.

### Line Output

The HPOL/LOL, HPOR/LOR, and HPCOM/MONO pins can drive a 10-kΩ load and be configured by register 74 (HPS[1:0]) as a monaural single-ended, monaural differential, or stereo single-line output with 1-V<sub>rms</sub> output. These outputs, except for the HPCOM/MONO pin, include an analog volume amplifier that can be set from 6 dB to –70 dB and mute in steps of 0.5-, 1-, 2- or 4-dB. Each output is controlled by registers 64 and 65 (HLV[5:0], HRV[5:0], HMUL, HMUR). No dc blocking capacitor is required when connecting an external speaker amplifier with monaural differential input. The center voltage is 0.5 V<sub>CC</sub> with zero data input.

### Headphone Output

The HPOL/LOL, HPOR/LOR, and HPCOM/MONO pins can be configured as a stereo, monaural, or monaural differential headphone output by register 74 (HPS[1:0]). These pins have more than 30 or 40 mW<sub>rms</sub> output power into a 32- or 16-Ω load, either through a dc blocking capacitor or without a capacitor. These outputs, except for the HPCOM/MONO pin, include an analog volume amplifier that can be set from 6 dB to –70 dB in steps of 0.5, 1, 2, or 4 dB. Each is controlled by registers 64 and 65 (HLV[5:0], HRV[5:0], HMUL, HMUR). The center voltage is 0.5 V<sub>CC</sub> with zero data input.

### Headphone Plug Insertion Detection

The HDTI pin detects the insertion status of headphone plug and writes the status to register 77 (HPDS), which can be read by the I<sup>2</sup>C interface. The polarity of the status indication can be inverted by register 75 (HPDP). The headphone and speaker amplifiers are disabled or enabled automatically by headphone plug insertion/extraction if register 75, HPDE = 1. They follow the register settings if register 75, HPDE = 0. HPCOM/MONO is not affected by the status when register 74, CMS[0] = 1.

### Speaker Output (Class-D, PCM3793A)

The SPOLP/SPOLN and SPORP/SPORN pins are stereo or mono speaker differential outputs (BTL) pairs with a maximum of 700 mWrms ( $V_{PA} = 3.6$  V, volume = 6 dB) into an 8- $\Omega$  load. The digital speaker amplifier offers maximum battery life, minimum heat, and elimination of LC low-pass filtering. The speaker amplifier includes an analog volume control with 6 dB to –70 dB in steps of 0.5, 1, 2 or 4 dB steps for each output, which can be set by registers 66 (SLV[5:0] and 67 SRV[5:0]). Spectrum spreading technology and selectable switching frequency to reduce EMI noise are controlled by register 71 (DFQ[2:0], SPS[1:0] and SPSE). This digital amplifier has a thermal shutdown circuit that detects when the device temperature reaches approximately 150°C; then the speaker amplifier is shut down.

### Analog Mixing and Bypass

Mixing amplifiers (MXL, MXR) mix inputs from the AIN pins. The analog inputs are selected by register 87 (AD2S, AIR[1:0],AIL[1:0]) and can bypass the ADC/DAC and connect the mixed signal to the headphone or speaker outputs by register 88 (MXR[2:0], MXL[2:0]). The gain of the analog inputs is controlled by register 89 (GMR[2:0], GML[2:0]). These functions are suitable for FM radio, headset, and other analog sources without an ADC.

### Microphone Bias

The MICB pin is the microphone bias source for an external microphone. MICB can provide 2 mA (typical) of bias current.

### Digital Gain Control

A portable application with small speakers may require a high sound level when playing back audio data recorded at low level. Digital gain control (DGC) can be used to amplify the digital input data by 0, 6, 12 or 18 dB by setting register 70 (SPX[1:0]).

### Automatic Level Control (ALC) for Recording

The sound for microphone recording should be expanded to a suitable level without saturation. The digitally controlled automatic level control (ALC) provides automatic expansion for small input signals and compression for large input signals while recording. The expansion level, compression level, attack time, and recovery time can be selected by register 83. The register 83 description explains the details of these settings.

### 3-D Sound

A 3-D sound effect is provided by mixing L-channel and R-channel data with a band-pass filter with two parameters, mixing ratio and band pass filter characteristic, that can be controlled by register 95 (3DP[3:0], 3FLO). The 3-D sound effect uses the DAC digital input or ADC digital output selected by register 95 (SDAS).

### Three-Band Tone Control

Tone control has bass, midrange, and treble controls that can be adjusted from 12 dB to –12 dB in 1-dB steps by registers 92 to 94 (LGA[4:0], MGA[4:0] and HGA[4:0]). Register 92 (LPAE) attenuates the digital input signal automatically to prevent clipping of the output signal at settings above 0 dB for bass control. LPAE has no effect on midrange and treble controls.

### High-Pass Filter and Two-Stage Programmable Notch Filter

The high-pass filter eliminates the dc offset of the ADC analog signal and can be set for a cutoff frequency of 4 Hz, 120 Hz, or 240 Hz at the 48-kHz sampling frequency by register 81 (HPF[1:0]). A register 95 (SDAS) selection applies the filter to either the DAC digital input or the ADC digital output.

Notch filters are provided to remove noise of a particular frequency, such as CCD noise, motor noise, or other mechanical noise in a particular application. The PCM3793A/94A has two notch filters for which the center frequency and frequency bandwidth can be programmed by registers 96 to 104. A register 95 (SDAS) selection applies the filter to either the DAC digital input or the ADC digital output.

## Digital Monaural Mixing

The audio data can be converted from stereo digital data to mixed monaural digital data. The conversion occurs in the internal audio interface section and is controlled by register 96 (MXEN).

## Zero-Cross Detection

Zero-cross detection minimizes audible zipper noise while changing analog volume and digital attenuation. This function applies to the digital input or digital output as defined by register 86 (ZCRS).

## Short Protection

The short-circuit protection on each headphone output prevents damage to the device while an output is shorted to  $V_{PA}$ , an output is shorted to PGND, or any two outputs are shorted together. When the short circuit is detected on the outputs, the PCM3793A/94A powers down the shorted amplifier immediately. The short-protection status can be monitored by reading register 77 (STHC, STHL, SCHR) through the I<sup>2</sup>C interface. Short-circuit protection operates in any enabled headphone amplifier.

## Thermal Protection

The thermal protection on the speaker amplifier prevents damage to the device when the internal die temperature exceeds approximately 150°C. Once the die temperature exceeds the thermal set point, all analog outputs are powered down. This status can be reset by setting register 76 (RLSR, RLSL) and can be watched by reading register 77 (STSR, STSL) through the two-wire (I<sup>2</sup>C) interface. Thermal protection operates in any enabled speaker amplifier.

## Pop-Noise Reduction Circuit

The pop-noise reduction circuit prevents audible noise when turning the power supply on/off and powering the device up/down in portable applications. It is recommended to establish the register settings in the sequence that is shown in [Table 3](#) and [Table 4](#). No particular external parts are required.

## Power Up/Down for Each Module

Using register 72 (PMXL, PMXR), register 73 (PBIS, PDAR, PDAL, PHPC, PHPR, PHPL, PSPR, PSPL), register 82 (PAIR, PAIL, PADS, PMCB, PADR, PADL), and register 90 (PCOM), unused modules can be powered down to minimize power consumption (7 mW during playback only and 13 mW when recording only).

## Digital Audio Interface

The PCM3793A/94A can receive I<sup>2</sup>S, right-justified, left-justified, and DSP formats in both master and slave modes. These options can be selected in register 70 (PFM[1:0]), register 81 (RFM[1:0]) and register 84 (MSTR).

## Digital Interface

All digital I/O pins can interface at various power supply voltages.  $V_{IO}$  pin can be connected to a 1.71-V to 3.6-V power supply.

## Power Supply

The  $V_{CC}$  pin and the  $V_{PA}$  pin can be connected to 2.4 V to 3.6 V. The same voltage must be applied to both pins. The  $V_{DD}$  pin and the  $V_{IO}$  pin can be connected to 1.71 V to 3.6 V. A different voltage can be applied to each of these pins (for example,  $V_{DD} = 1.8$  V,  $V_{IO} = 3.3$  V).

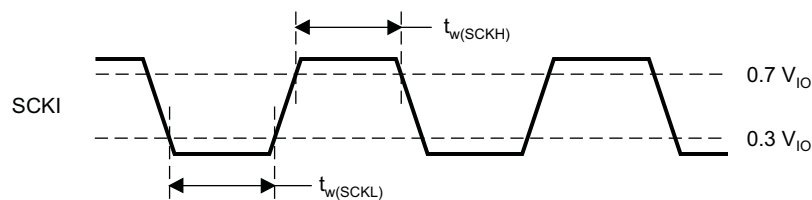
## DESCRIPTION OF OPERATION

### System Clock Input

The PCM3793A/94A can accept clocks of various frequencies without a PLL. They are used for clocking the digital filters and automatic level control and delta-sigma modulators and are classified as common-audio and application-specific clocks. [Table 2](#) shows frequencies of the common-audio clock and application-specific clock. [Figure 26](#) shows the timing requirements for system clock inputs. The sampling rate and frequency of the system clocks are determined by the settings of register 86 (MSR[2:0]) and register 85 (NPR[5:0]). Note that the sampling rate of the application-specific clock has a little sampling error. The details are shown in [Table 12](#).

**Table 2. System Clock Frequencies**

CLOCK	FREQUENCIES
Common-audio clock	11.2896, 12.288, 16.9344, 18.432 MHz
Application-specific clock	12, 13, 13.5, 24, 26, 27, 19.2, 19.68, 38.4, 39.36 MHz



T0005-12

PARAMETERS	SYMBOL	MIN	UNITS
System-clock pulse duration, high	t <sub>w</sub> (SCKH)	7	ns
System-clock pulse duration, low	t <sub>w</sub> (SCKL)	7	ns

**Figure 26. System Clock Timing**

### Power-On Reset and System Reset

The power-on-reset circuit outputs a reset signal, typically at V<sub>DD</sub> = 1.2 V, and this circuit does not depend on the voltage of other power supplies (V<sub>CC</sub>, V<sub>PA</sub>, and V<sub>IO</sub>). Internal circuits are cleared to default status, then signals are removed from all analog and digital outputs. The PCM3793A/94A does not require any power supply sequencing. Register data must be written after turning all power supplies on.

System reset is enabled by setting register 85 (SRST = 1). After the reset sequence, the register data is reset to SRST = 0 automatically. All circuits are cleared to their default status at once by the system reset. Note that the PCM3793A/94A has audible pop noise on the analog outputs when enabling SRST.

### Power On/Off Sequence

To reduce audible pop noise, a sequence of register settings is required after turning all power supplies on when powering up, or before turning the power supplies off when powering down. If some modules are not required for a particular application or operation, they should be placed in the power-down state after performing the power-on sequence. The recommended power-on and power-off sequences are shown in [Table 3](#) and [Table 4](#), respectively.

**Table 3. Recommended Power-On Sequence**

STEP	REGISTER SETTINGS	NOTE
1	–	Turn on all power supplies <sup>(1)</sup>
2	4027h	Headphone amplifier L-ch volume (–6 dB) <sup>(2)</sup>
3	4127h	Headphone amplifier R-ch volume (–6 dB) <sup>(2)</sup>
4	4227h	Speaker amplifier L-ch volume (–6 dB) <sup>(2)</sup>
5	4327h	Speaker amplifier R-ch volume (–6 dB) <sup>(2)</sup>
6	4427h	Digital attenuator L-ch (–24 dB) <sup>(2)</sup>
7	4527h	Digital attenuator R-ch (–24 dB) <sup>(2)</sup>
8	4620h	DAC audio interface format (left-justified) <sup>(3)</sup>
9	4BC0h	Headphone detection enable and inverting polarity. Short and thermal detection enable
10	5102h	ADC audio interface format (left-justified) <sup>(3)</sup>
11	5A10h	V <sub>COM</sub> ramp up/down time control. PG1, PG2 gain control (0 dB)
12	49E0h	DAC (DAL, DAR) and analog bias power up
13	5601h	Zero-cross detection enable
14	4803h	Analog mixer (MXL, MXR) power up
15	5811h	Analog mixer input (SW2, SW5) select
16	49FCh	Headphone amplifier (HPL, HPR, HPC) power up
17	4C03h	Speaker amplifier shut down release
18	4A01h	V <sub>COM</sub> power up
19	523Fh	Analog front end (ADL, ADR, D2S, MCB, PG1, 2, 5, 6) power up
20	5711h	Analog input (MUX3, MUX4) select. Analog input (MUX1, MUX2) select
21	4F0Ch	Analog input L-ch (PG3) volume (0 dB) <sup>(2)</sup>
22	500Ch	Analog input R-ch (PG4) volume (0 dB) <sup>(2)</sup>
23	–	Any settings for other devices or wait time, 450 ms <sup>(4)(5)</sup>
24	49FFh	Speaker amplifier (SPL, SPR) power up <sup>(5)</sup>

- (1) V<sub>DD</sub> should be turn on prior to or simultaneously with the other power supplies. It is recommended to set register data with the system clock input after turning all power supplies on.
- (2) Any level is acceptable for volume or attenuation. Level should be resumed by register data recorded when system power off.
- (3) Audio interface format should be set to match the DSP or decoder being used.
- (4) The PCM3793A requires time for V<sub>COM</sub> to reach the common level from GND level. The delay depends on the capacitor value for V<sub>COM</sub> and the setting of register 125 PTM[1:0], RES[4:0]. The default setting is 450 ms at V<sub>COM</sub> = 4.7 μs.
- (5) The PCM3794A does not require this setting because it has no speaker output.

**Table 4. Recommended Power-Off Sequence**

STEP	REGISTER SETTINGS	NOTE
1	447Fh	DAC L-ch digital soft-mute enable <sup>(1)</sup>
2	457Fh	DAC R-ch digital soft-mute enable <sup>(1)</sup>
3	5132h	ADC L-ch/R-ch digital soft-mute enable, ADC audio interface format (left-justified) <sup>(2)</sup>
4	5811h	Analog mixer input (SW2, SW5) select
5	49FCh	Headphone amplifier (HPL, HPR, HPC) power up <sup>(3)(4)</sup>
6	5200h	Analog front end (ADL, ADR, D2S, MCB, PG1, 2, 5, 6) power down
7	5A00h	PG1, PG2 gain control (0 dB)
8	4A00h	V <sub>COM</sub> power down
9	–	Wait time (750 ms) <sup>(5)</sup>
10	49E0h	Headphone amplifier (HPL, HPR, HPC) power down, speaker amplifier (SPL, SPR) power down
11	4800h	Analog mixer (MXL, MXR) power down
12	4900h	DAC (DAL, DAR) and analog bias power down
13	–	Turn off all power supplies. <sup>(6)</sup>

- (1) Any level is acceptable for volume or attenuation.
- (2) Audio interface format should be set to match the DSP or decoder in the application.
- (3) The PCM3794A has no speaker amplifier.
- (4) The headphone amplifier must be operating during the power-off sequence.
- (5) PCM3793A requires time for V<sub>COM</sub> to reach the ground level from the common level. The wait time allowed depends on the settings of register 125 PTM[1:0], RES[4:0]. The default setting is 750 ms for V<sub>COM</sub> = 4.7 μF.
- (6) Power supply sequencing is not required. It is recommended to turn off all power supplies after setting the registers with the system clock input.

### Power-Supply Current

The current consumption of the PCM3793A/94A depends on power up/down status of each circuit module. In order to reduce the power consumption, disabling each module is recommended when it is not used in an application or operation. [Table 5](#) shows the current consumption in some states.

Table 5. Power Consumption Table

OPERATION MODE	POWER SUPPLY CURRENT [mA]					PD [mW]	PD [mW]
	V <sub>DD</sub> (1.8 V)	V <sub>DD</sub> (3.3 V)	V <sub>CC</sub> (3.3 V)	V <sub>PA</sub> (3.3 V)	V <sub>IO</sub> (3.3 V)	TOTAL (V <sub>DD</sub> = 1.8 V)	TOTAL (V <sub>DD</sub> = 3.3 V)
All Power Down	0	0	0.007	0.002	0	0.03	0.03
All Active	2.5	5.1	7.5	11.6	0.1	67.7	80.2
<b>PLAYBACK WITH DIGITAL INPUT</b>							
Line output and headphone output	1.18	2.51	1.79	0.54	0.09	10.1	16.3
Headphone output with sound effect	1.81	3.84	1.79	0.54	0.09	11.2	20.7
Capless headphone output	1.18	2.51	1.8	0.75	0.09	10.8	17.0
Headphone output with line input (AIN2L/AIN2R)	1.18	2.52	2.09	0.54	0.09	11.1	17.3
Headphone output with mono microphone input (AIN1L, 20 dB)	1.18	2.52	2.5	0.54	0.09	12.5	18.6
Headphone output with mono differential microphone input (AIN1L/AIN1R, 20 dB)	1.18	2.52	2.8	0.54	0.09	13.4	19.6
Stereo speaker output	1.21	2.58	2.18	10.94	0.09	45.8	52.1
Mono speaker output	1.2	2.57	2.01	5.61	0.09	27.6	33.9
Speaker output with line input (AIN2L/AIN2R)	1.21	2.57	2.48	10.95	0.09	46.8	53.1
Speaker output with mono microphone input (AIN1L, 20 dB)	1.21	2.58	2.89	10.96	0.09	48.2	54.5
Speaker output with mono differential microphone input (AIN1L/AIN1R, 20 dB)	1.2	2.58	3.2	10.98	0.09	49.3	55.6
<b>PLAYBACK WITHOUT DIGITAL INPUT</b>							
Line input (AIN2L/AIN2R) to headphone output	0	0	0.76	0.53	0	4.3	4.3
Mono line input (AIN2L) to headphone output	0	0	0.61	0.53	0	3.8	3.8
Mono microphone Input (AIN1L, 20 dB) to headphone output	0	0	1.18	0.53	0	5.6	5.6
Mono differential microphone input (AIN1L/AIN1R, 20 dB) to headphone output	0	0	1.48	0.53	0	6.6	6.6
Mono microphone input (AIN1L, 20 dB) to speaker output	0	0	1.57	10.92	0	41.2	41.2
<b>RECORDING</b>							
Line input (AIN3L/AIN3R)	1.86	3.89	4.58	0.13	0.1	19.1	28.7
Microphone input (AIN1L/AIN1R, 20 dB)	1.86	3.91	5.14	0.13	0.1	21.1	30.6
Microphone input (AIN1L/AIN1R, 20 dB) with ALC	2.78	5.77	5.14	0.13	0.1	22.7	36.8
Mono microphone input (AIN1L, 20 dB)	1.4	2.93	3.6	0.13	0.1	15.2	22.3
Mono microphone input (AIN1L, 20 dB) with ALC	2.2	4.74	3.6	0.13	0.1	16.6	28.3
Mono differential microphone input (AIN1L/AIN1R, 20 dB)	1.4	2.94	3.96	0.13	0.1	16.3	23.5
Mono differential microphone input (AIN1L/AIN1R, 20 dB) with ALC	2.2	4.74	3.96	0.13	0.1	17.8	29.5
<b>Conditions:</b> 48 kHz/256 f <sub>s</sub> , 16 bits, slave mode, zero data input, no load							

## Audio Serial Interface

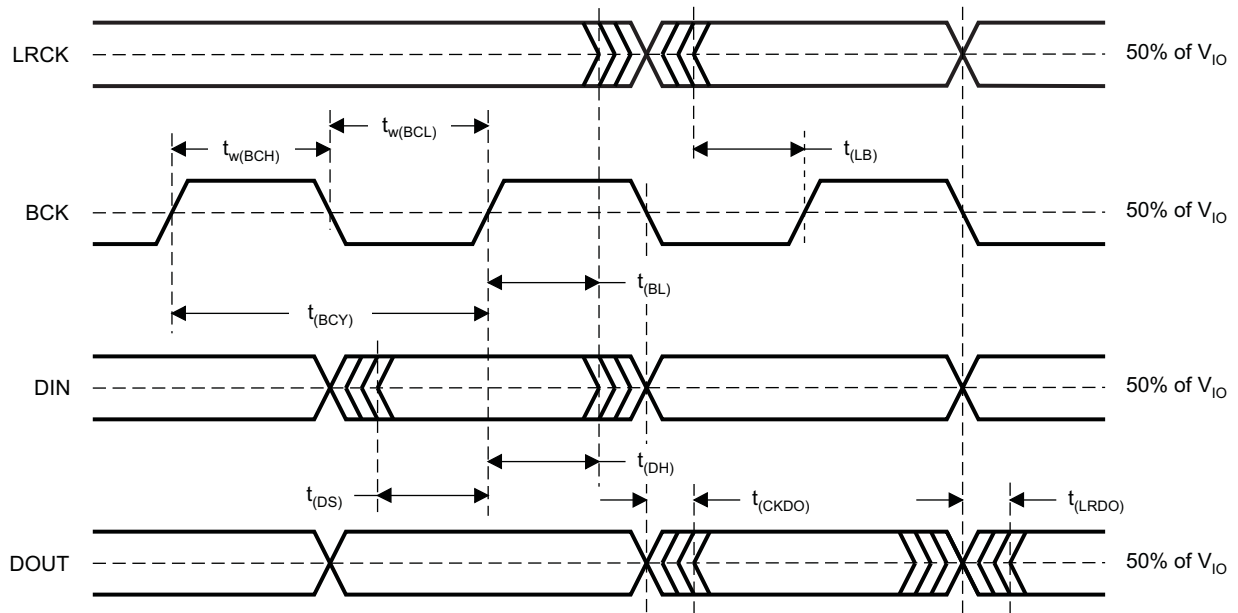
The audio serial interface for the PCM3793A/94A comprises LRCK, BCK, DIN, and DOUT. Sampling rate (f<sub>s</sub>), left and right channel are present on LRCK. DIN receives the serial data for the DAC interpolation filter, and DOUT transmits the serial data from the ADC decimation filter. BCK clocks the transfer of serial audio data on DIN and DOUT in its high-to-low transition. BCK and LRCK should be synchronized with audio system clock. Ideally, it is recommended that they be derived from it.

The PCM3793A/94A requires LRCK to be synchronized with the system clock. The PCM3793A/94A does not require a specific phase relationship between LRCK and the system clock.

The PCM3793A/94A has both master mode and slave mode interface formats, which can be selected by register 84 (MSTR). In master mode, the PCM3793A/94A generates LRCK and BCK from the system clock.

## Audio Data Formats and Timing

The PCM3793A/94A supports I<sup>2</sup>S, right-justified, left-justified, and DSP formats. The data formats are shown in [Figure 29](#) and are selected using registers 70 and 81 (RFM[1:0], PFM[1:0]). All formats require binary 2s-complement, MSB-first audio data. The default format is I<sup>2</sup>S. [Figure 27](#) shows a detailed timing diagram.

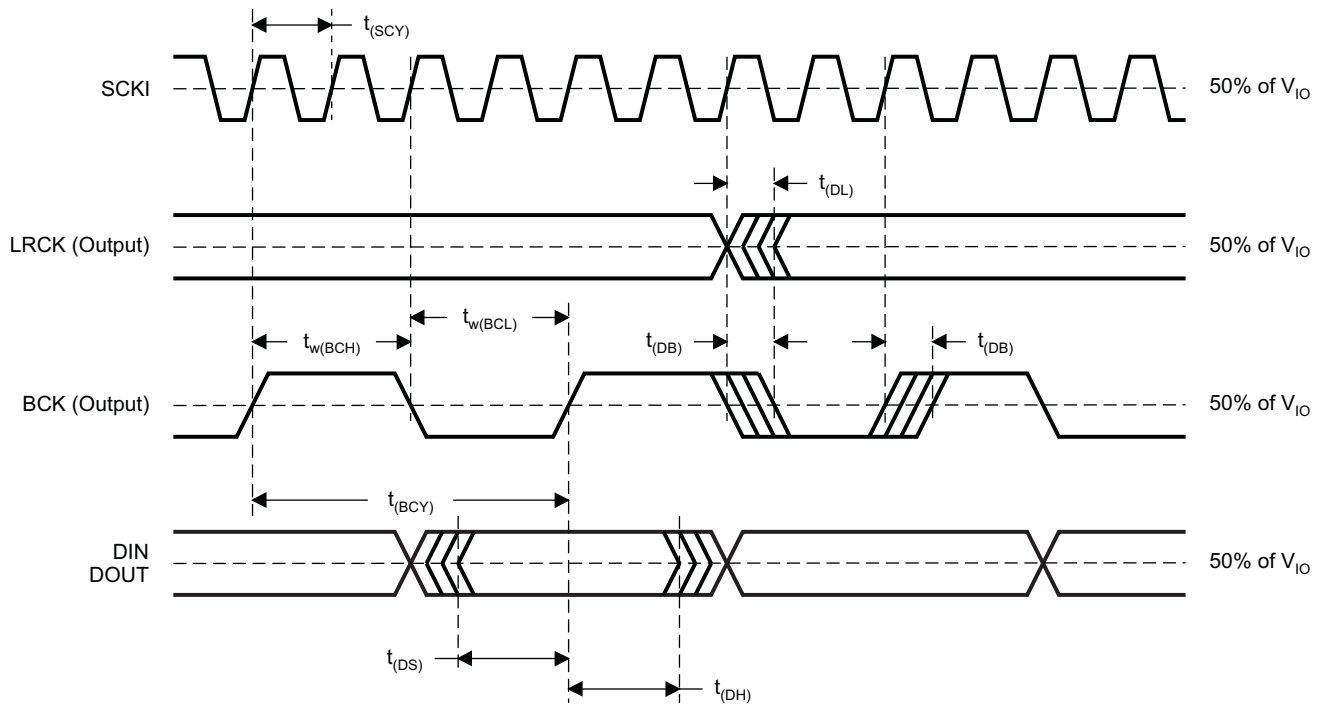


T0010-09

PARAMETERS		MIN	MAX	UNITS
$t_{(BCY)}$	BCK pulse cycle time (I <sup>2</sup> S, left- and right-justified formats)	$1/(64 f_s)^{(1)}$		
	BCK pulse cycle time (DSP format)	$1/(256 f_s)^{(1)}$		
$t_{w(BCH)}$	BCK high-level time	35		ns
$t_{w(BCL)}$	BCK low-level time	35		ns
$t_{(BL)}$	BCK rising edge to LRCK edge	10		ns
$t_{(LB)}$	LRCK edge to BCK rising edge	10		ns
$t_{(DS)}$	DIN set up time	10		ns
$t_{(DH)}$	DIN hold time	10		ns
$t_{(CKDO)}$	DOUT delay time from BCK falling edge		15	ns
$t_{(LRDO)}$	DOUT delay time from LRCK falling edge		15	ns
$t_r$	Rising time of all signals		10	ns
$t_f$	Falling time of all signals		10	ns

(1)  $f_s$  is the sampling frequency.

Figure 27. Audio Interface Timing (Slave Mode)



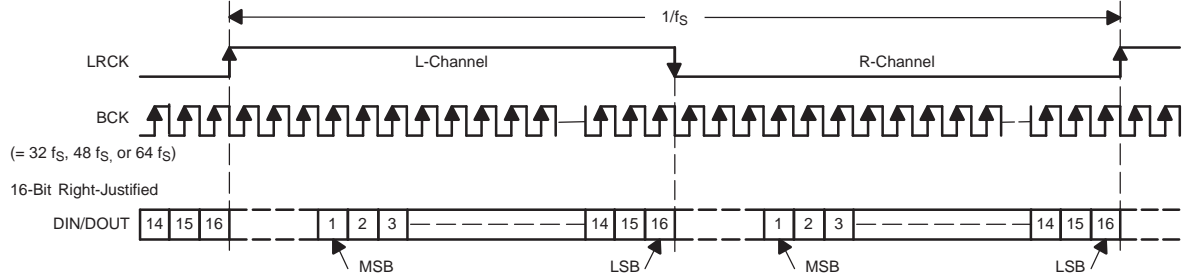
T0011-04

PARAMETERS		MIN	MAX	UNIT
$t_{(SCY)}$	SCKI pulse cycle time	$1/(256 f_s)^{(1)}$		
$t_{(DL)}$	LRCK edge from SCKI rising edge	0	40	ns
$t_{(DB)}$	BCK edge from SCKI rising edge	0	40	ns
$t_{(BCY)}$	BCK pulse cycle time	$1/(64 f_s)^{(1)}$		
$t_{w(BCH)}$	BCK high level time	146		ns
$t_{w(BCL)}$	BCK low level time	146		ns
$t_{(DS)}$	DATA setup time	10		ns
$t_{(DH)}$	DATA hold time	10		ns

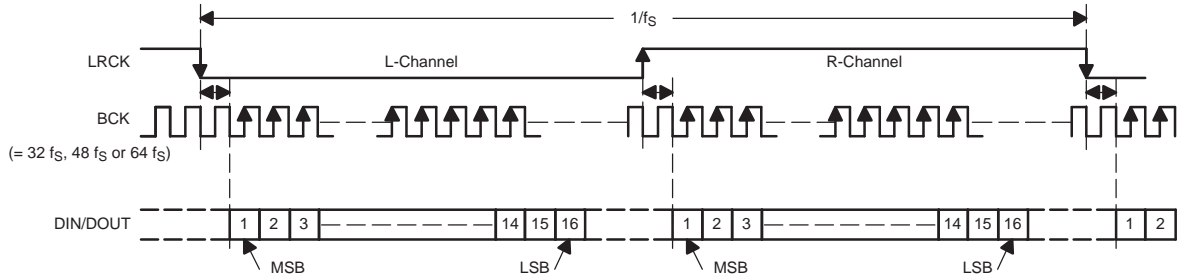
(1)  $f_s$  is up to 48 kHz.  $f_s$  is the sampling frequency.

**Figure 28. Audio Interface Timing (Master Mode)**

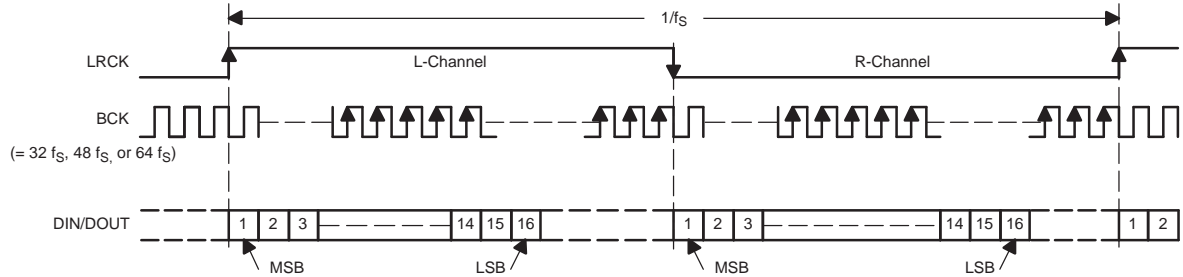
(a) Right-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



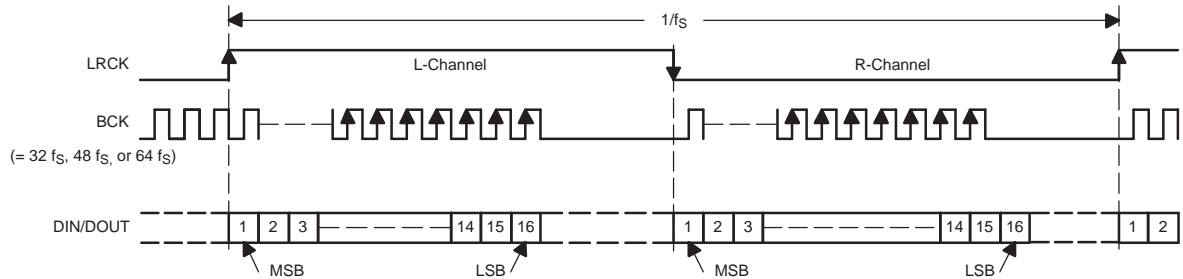
(b) I<sup>2</sup>S Data Format; L-Channel = LOW, R-Channel = HIGH



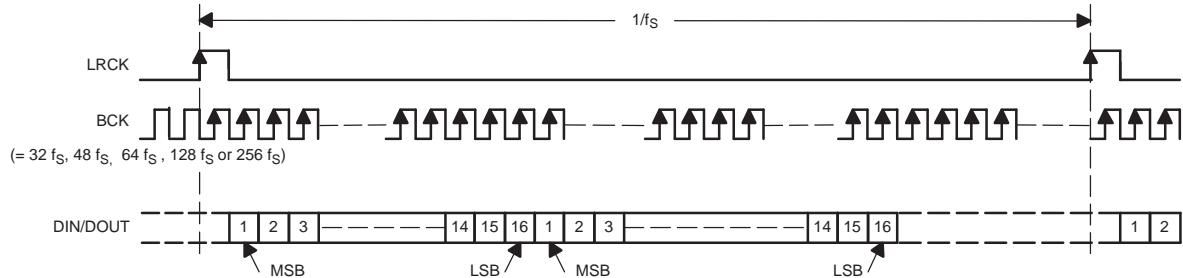
(c) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(d) Burst BCK Interface Format at Master Mode; L-Channel = HIGH, R-Channel = LOW



(e) DSP Format



T0009-07

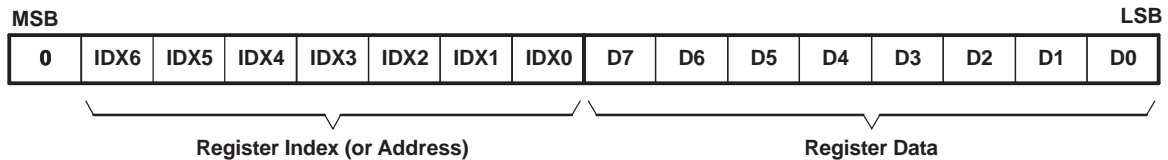
NOTE: All audio interface formats support BCK = 64 f<sub>s</sub> in master mode (register 69, MSTR = 1). When setting the multisampling rate, the f<sub>s</sub> of BCK is set to half the rate of the DSP operation frequency.

Figure 29. Audio Data Input and Output Formats

### THREE-WIRE INTERFACE (SPI, MODE (PIN 28) = LOW)

All write operations for the serial control port use 16-bit data words. [Figure 30](#) shows the control data word format. The most-significant bit must be 0. There are seven bits, labeled  $IDX[6:0]$ , that set the register address for the write operation. The least-significant eight bits,  $D[7:0]$ , contain the data to be written to the register specified by  $IDX[6:0]$ .

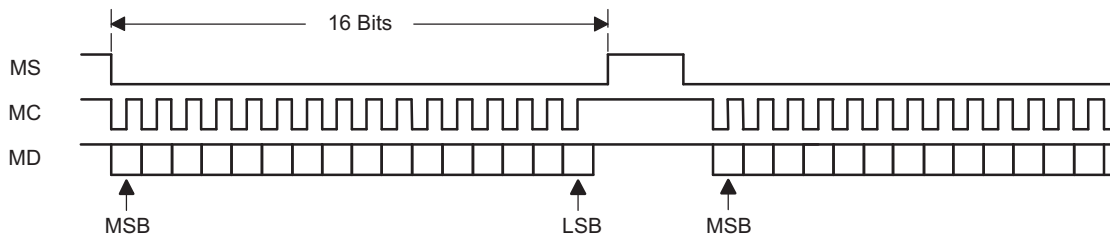
[Figure 31](#) shows the functional timing diagram for writing to the serial control port. To write the data into the mode register, the data is clocked into an internal shift register on the rising edge of the MC clock. The serial data should change on the falling edge of the MC clock, and MS should be LOW during write mode. The rising edge of MS should be aligned with the falling edge of the last MC clock pulse in the 16-bit frame. MC can run continuously between transactions while MS is in the LOW state.



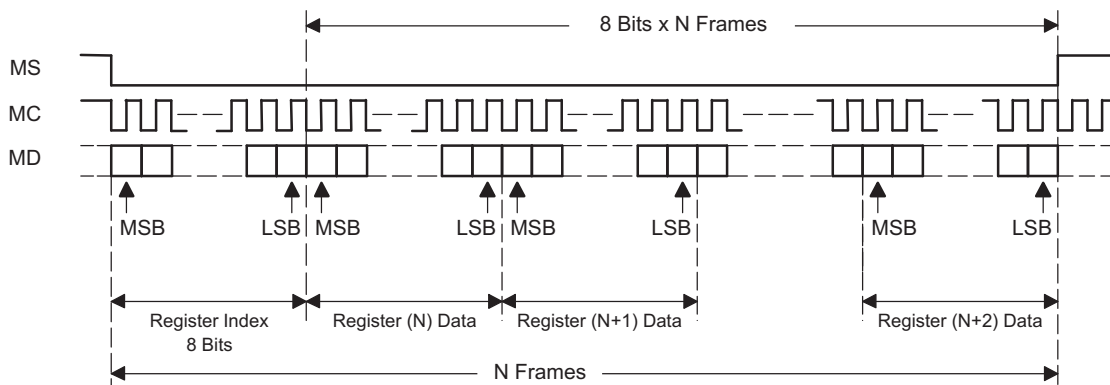
R0001-01

**Figure 30. Control Data Word Format for MD**

(1) Single Write Operation



(2) Continuous Write Operation

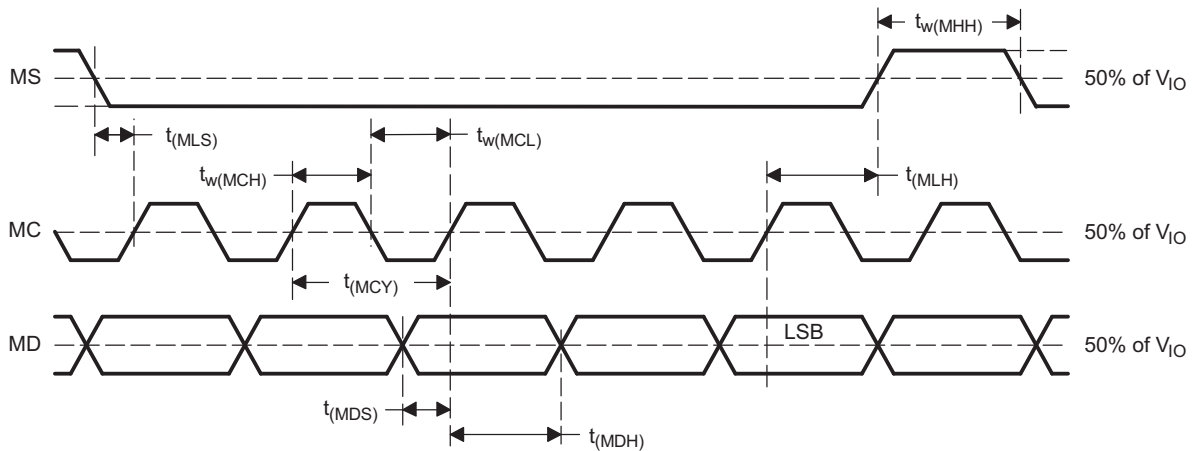


T0012-03

**Figure 31. Register Write Operation**

### Three-Wire Interface (SPI) Timing Requirements

Figure 32 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



T0013-08

PARAMETERS		MIN	TYP	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	500 <sup>(1)</sup>			ns
$t_w(MCL)$	MC low level time	50			ns
$t_w(MCH)$	MC high level time	50			ns
$t_w(MHH)$	MS high level time	(1)			ns
$t_{(MLS)}$	MS falling edge to MC rising edge	20			ns
$t_{(MLH)}$	MS hold time	20			ns
$t_{(MDH)}$	MD hold time	15			ns
$t_{(MDS)}$	MD setup time	20			ns

(1)  $3/(128 f_s)$  s (min), where  $f_s$  is sampling rate.

**Figure 32. SPI Interface Timing**

### TWO-WIRE INTERFACE [I<sup>2</sup>C, MODE (PIN 28) = HIGH]

The PCM3793A/94A supports the I<sup>2</sup>C serial bus and the data transmission protocol for the I<sup>2</sup>C standard as a slave device. This protocol is explained in I<sup>2</sup>C specification 2.0.

In I<sup>2</sup>C mode, the control terminals are changed as follows.

TERMINAL NAME	PROPERTY	DESCRIPTION
MS/ADR	Input	I <sup>2</sup> C address
MD/SDA	Input/output	I <sup>2</sup> C data
MC/SCL	Input	I <sup>2</sup> C clock

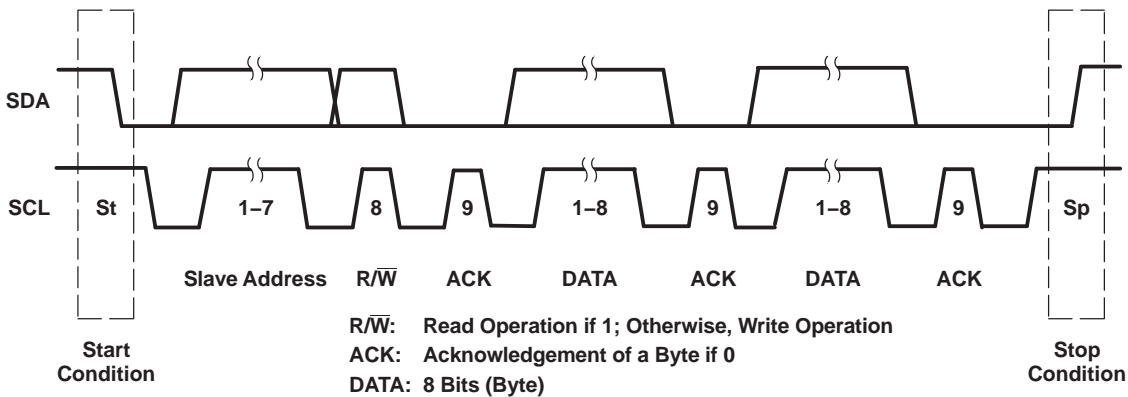
### SLAVE ADDRESS

MSB						LSB	
1	0	0	0	1	1	ADR	R/W

The PCM3793A/94A has its own 7-bit slave address. The first six bits (MSBs) of the slave address are factory preset to 100011. The last bit of the address byte is the device select bit, which can be user-defined by the ADR terminal. A maximum of two PCM3793A/94As can be connected on the same bus at one time. Each PCM3793A/94A responds when it receives its own slave address.

## Packet Protocol

The master device must control packet protocol, which consists of start condition, slave address with read/write bit, data (if write) or acknowledgement (if read), and stop condition. The PCM3793A/94A supports only slave receiver and slave transmitter.



### Write Operation

Transmitter	M	M	M	S	M	S	M	S	M
Data Type	St	Slave Address	R/W	ACK	DATA	ACK	DATA	ACK	Sp

### Read Operation

Transmitter	M	M	M	S	S	M	S	M	M
Data Type	St	Slave Address	R/W	ACK	DATA	ACK	DATA	NACK	Sp

M: Master Device      S: Slave Device  
St: Start Condition    Sp: Stop Condition

T0049-03

Figure 33. Basic I<sup>2</sup>C Framework

## WRITE OPERATION

The master can write any PCM3793A/94A registers in a single access. The master sends a PCM3793A/94A slave address with a write bit, a register address, and data. When undefined registers are accessed, the PCM3793A/94A does not send any acknowledgement. [Figure 34](#) shows a diagram of the write operation.

Transmitter	M	M	M	S	M	S	M	S	M
Data Type	St	Slave Address	W	ACK	Reg Address	ACK	Write Data	ACK	Sp

M: Master Device      S: Slave Device  
St: Start Condition    W: Write    ACK: Acknowledge    Sp: Stop Condition

R0002-01

Figure 34. Framework for Write Operation

## READ OPERATION

The master can read PCM3793A/94A register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM3793A/94A slave address with a read bit after storing the register address. Then the PCM3793A/94A transfers the data which the index register specifies. [Figure 35](#) shows a diagram of the read operation.

Transmitter	M	M	M	S	M	S	M	M	M	S	S	M	M
Data Type	St	Slave Address	$\bar{W}$	ACK	Reg Address	ACK	Sr	Slave Address	R	ACK	Read Data	NACK	Sp

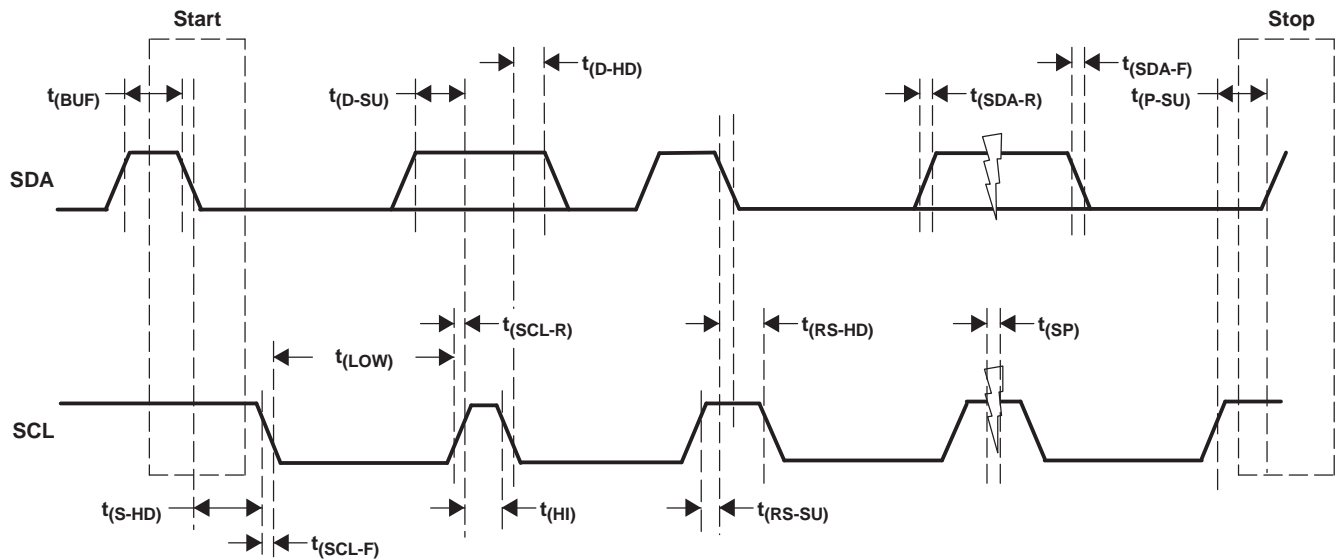
M: Master Device S: Slave Device St: Start Condition  
Sr: Repeated Start Condition ACK: Acknowledge Sp: Stop Condition NACK: Not Acknowledge  
W: Write R: Read

R0002-02

NOTE: The slave address after the repeated start condition must be the same as the previous slave address.

Figure 35. Read Operation

Timing Diagram



T0050-03

PARAMETERS		CONDITIONS	MIN	MAX	UNIT
$f_{SCL}$	SCL clock frequency	Standard		100	kHz
$t_{(BUF)}$	Bus free time between a STOP and START condition	Standard	4.7		$\mu$ s
$t_{(LOW)}$	Low period of the SCL clock	Standard	4.7		$\mu$ s
$t_{(HI)}$	High period of the SCL clock	Standard	4		$\mu$ s
$t_{(RS-SU)}$	Setup time for START condition	Standard	4.7		$\mu$ s
$t_{(S-HD)}$	Hold time for START condition	Standard	4		$\mu$ s
$t_{(D-SU)}$	Data setup time	Standard	250		ns
$t_{(D-HD)}$	Data hold time	Standard	0	900	ns
$t_{(SCL-R)}$	Rise time of SCL signal	Standard	$20 + 0.1 C_B$	1000	ns
$t_{(SCL-R1)}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard	$20 + 0.1 C_B$	1000	ns
$t_{(SCL-F)}$	Fall time of SCL signal	Standard	$20 + 0.1 C_B$	1000	ns
$t_{(SDA-R)}$	Rise time of SDA signal	Standard	$20 + 0.1 C_B$	1000	ns
$t_{(SDA-F)}$	Fall time of SDA signal	Standard	$20 + 0.1 C_B$	1000	ns
$t_{(P-SU)}$	Setup time for STOP condition	Standard	4		$\mu$ s
$C_B$	Capacitive load for SDA and SCL line			400	pF
$t_{(SP)}$	Pulse duration of suppressed spike			25	ns

Figure 36. I<sup>2</sup>C Interface Timing

## USER-PROGRAMMABLE MODE CONTROLS

### Register Map

The mode control register map is shown in [Table 6](#). Each register includes an index (or address) indicated by the IDX[6:0] bits.

**Table 6. Mode Control Register Map**

REGISTER	IDX[6:0] (B14–B8)	DESCRIPTION	B7	B6	B5	B4	B3	B2	B1	B0
Register 64	40h	Volume for HPA (L-ch)	RSV	HMUL	HLV5	HLV4	HLV3	HLV2	HLV1	HLV0
Register 65	41h	Volume for HPA (R-ch)	RSV	HMUR	HRV5	HRV4	HRV3	HRV2	HRV1	HRV0
Register 66	42h	Volume for SPA (L-ch)	RSV	SMUL	SLV5	SLV4	SLV3	SLV2	SLV1	SLV0
Register 67	43h	Volume for SPA (R-ch)	RSV	SMUR	SRV5	SRV4	SRV3	SRV2	SRV1	SRV0
Register 68	44h	DAC digital attenuation and soft mute (L-ch)	RSV	PMUL	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 69	45h	DAC digital attenuation and soft mute (R-ch)	RSV	PMUR	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Register 70	46h	DAC over sampling, de-emphasis, audio interface	DEM1	DEM0	PFM1	PFM0	SPX1	SPX0	RSV	OVER
Register 71	47h	SPA (class-D) switching frequency	RSV	RSV	RSV	SPSE	SPS1	SPS0	DFQ1	DFQ0
Register 72	48h	Analog mixer power up/down	RSV	RSV	RSV	RSV	RSV	RSV	PMXR	PMXL
Register 73	49h	DAC, SPA and HPA power up/down	PBIS	PDAR	PDAL	PHPC	PHPR	PHPL	PSPR	PSPL
Register 74	4Ah	Analog output configuration select	RSV	CMS2	CMS1	CMS0	HPS1	HPS0	SPKS	PCOM
Register 75	4Bh	HPA insertion detection, short/thermal protection	HPDP	HPDE	RSV	SDHC	SDHR	SDHL	SDSR	SDSL
Register 76	4Ch	SPA shutdown release	RSV	RSV	RSV	RSV	RSV	RSV	RLSR	RLSL
Register 77	4Dh	Shut down status read back	HPDS	RSV	RSV	STHC	STHR	STHL	STSR	STSL
Register 79	4Fh	Volume for ADC input (L-ch)	RSV	RSV	ALV5	ALV4	ALV3	ALV2	ALV1	ALV0
Register 80	50h	Volume for ADC input (R-ch)	RSV	RSV	ARV5	ARV4	ARV3	ARV2	ARV1	ARV0
Register 81	51h	ADC high-pass filter, soft mute, audio interface	HPF1	HPF0	RMUL	RMUR	RSV	DSMC	RFM1	RFM0
Register 82	52h	ADC, MCB, PG1, 2, 5, 6, D2S power up/down	RSV	RSV	PAIR	PAIL	PADS	PMCB	PADR	PADL
Register 83	53h	Automatic level control for recording	RALC	RSV	RRTC	RATC	RCP1	RCP0	RLV1	RLV0
Register 84	54h	Master mode	RSV	RSV	RSV	RSV	RSV	MSTR	RSV	BIT0
Register 85	55h	System reset, sampling rate control	SRST	RSV	NPR5	NPR4	NPR3	NPR2	NPR1	NPR0
Register 86	56h	BCK configuration, sampling rate control, zero-cross	MBST	MSR2	MSR1	MSR0	ATOD	RSV	RSV	ZCRS
Register 87	57h	Analog input select (MUX1, 2, 3, 4)	AD2S	RSV	AIR1	AIR0	RSV	RSV	AIL1	AIL0
Register 88	58h	Analog mixing switch (SW1, 2, 3, 4, 5, 6)	RSV	MXR2	MXR1	MXR0	RSV	MXL2	MXL1	MXL0
Register 89	59h	Analog to analog path (PG5, 6) gain	RSV	GMR2	GMR1	GMR0	RSV	GML2	GML1	GML0
Register 90	5Ah	Microphone boost	RSV	RSV	RSV	RSV	RSV	RSV	G20R	G20L
Register 92	5Ch	Bass boost gain level	LPAE	RSV	RSV	LGA4	LGA3	LGA2	LGA1	LGA0
Register 93	5Dh	Middle boost gain level	RSV	RSV	RSV	MGA4	MGA3	MGA2	MGA1	MGA0
Register 94	5Eh	Treble boost gain level	RSV	RSV	RSV	HGA4	HGA3	HGA2	HGA1	HGA0
Register 95	5Fh	Sound effect source select, 3D sound	SDAS	3DEN	RSV	3FL0	3DP3	3DP2	3DP1	3DP0
Register 96	60h	2-stage notch filter, digital monaural mixing	NEN2	NEN1	NUP2	NUP1	RSV	RSV	RSV	MXEN
Register 97	61h	1st stage notch filter lower coefficient (a1)	F107	F106	F105	F104	F103	F102	F101	F100
Register 98	62h	1st stage notch filter upper coefficient (a1)	F115	F114	F113	F112	F111	F110	F109	F108
Register 99	63h	1st stage notch filter lower coefficient (a2)	F207	F206	F205	F204	F203	F202	F201	F200
Register 100	64h	1st stage notch filter upper coefficient (a2)	F215	F214	F213	F212	F211	F210	F209	F208
Register 101	65h	2nd stage notch filter lower coefficient (a1)	S107	S106	S105	S104	S103	S102	S101	S100
Register 102	66h	2nd stage notch filter upper coefficient (a1)	S115	S114	S113	S112	S111	S110	S109	S108
Register 103	67h	2nd stage notch filter lower coefficient (a2)	S207	S206	S205	S204	S203	S202	S201	S200
Register 104	68h	2nd stage notch filter upper coefficient (a2)	S215	S214	S213	S212	S211	S210	S209	S208
Register 125	7Dh	Power up/down time control	RSV	PTM1	PTM0	RES4	RES3	RES2	RES1	RES0

HPA: Headphone amplifier single-ended amplifier SPA: Speaker amplifier DAC: D/A converter ADC: A/D converter MCB: Microphone bias PGx: Analog input buffer D2S: Differential to

**Register Definitions**

**Registers 64 and 65**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 64	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	HMUL	HLV5	HLV4	HLV3	HLV2	HLV1	HLV0
Register 65	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	HMUR	HRV5	HRV4	HRV3	HRV2	HRV1	HRV0

**IDX[6:0]:** 100 0000b (40h): Register 64

**IDX[6:0]:** 100 0001b (41h): Register 65

**HMUL: Analog Mute Control for HPL (Line or Headphone L-Channel)**

**HMUR: Analog Mute Control for HPR (Line or Headphone R-Channel)**

Default value: 1

HPOL/LOL and HPOR/LOR can be independently muted to zero level when HMUL and HMUR = 1. These settings take precedence over analog volume level settings.

HMUL, HMUR = 0	Mute disabled
HMUL, HMUR = 1	Mute enabled (default)

**HLV[5:0]: Analog Volume for HPL (Headphone L-Channel)**

**HRV[5:0]: Analog Volume for HPR (Headphone R-Channel)**

Default value: 00 0000.

HPOL/LOL and HPOR/LOR can be independently controlled between 6 dB and –70 dB, with step size depending on the gain level as shown in [Table 7](#). Outputs may have zipper noise while changing levels. This noise can be reduced by selecting zero-cross detection (register 86, ZCRS).

**Table 7. Headphone Gain Level Setting**

HLV[5:0], HRV[5:0]	STEP	GAIN LEVEL SETTING	HLV[5:0], HRV[5:0]	STEP	GAIN LEVEL SETTING	HLV[5:0], HRV[5:0]	STEP	GAIN LEVEL SETTING
11 1111	3F	6 dB	10 1001	29	–5 dB	01 0011	13	–21 dB
11 1110	3E	5.5 dB	10 1000	28	–5.5 dB	01 0010	12	–22 dB
11 1101	3D	5 dB	10 0111	27	–6 dB	01 0001	11	–23 dB
11 1100	3C	4.5 dB	10 0110	26	–6.5 dB	01 0000	10	–24 dB
11 1011	3B	4 dB	10 0101	25	–7 dB	00 1111	0F	–26 dB
11 1010	3A	3.5 dB	10 0100	24	–7.5 dB	00 1110	0E	–28 dB
11 1001	39	3 dB	10 0011	23	–8 dB	00 1101	0D	–30 dB
11 1000	38	2.5 dB	10 0010	22	–8.5 dB	00 1100	0C	–32 dB
11 0111	37	2 dB	10 0001	21	–9 dB	00 1011	0B	–34 dB
11 0110	36	1.5 dB	10 0000	20	–9.5 dB	00 1010	0A	–36 dB
11 0101	35	1 dB	01 1111	1F	–10 dB	00 1001	09	–38 dB
11 0100	34	0.5 dB	01 1110	1E	–10.5 dB	00 1000	08	–40 dB
11 0011	33	0 dB	01 1101	1D	–11 dB	00 0111	07	–42 dB
11 0010	32	–0.5 dB	01 1100	1C	–12 dB	00 0110	06	–46 dB
11 0001	31	–1 dB	01 1011	1B	–13 dB	00 0101	05	–50 dB
11 0000	30	–1.5 dB	01 1010	1A	–14 dB	00 0100	04	–54 dB
10 1111	2F	–2 dB	01 1001	19	–15 dB	00 0011	03	–58 dB
10 1110	2E	–2.5 dB	01 1000	18	–16 dB	00 0010	02	–62 dB
10 1101	2D	–3 dB	01 0111	17	–17 dB	00 0001	01	–66 dB
10 1100	2C	–3.5 dB	01 0110	16	–18 dB	00 0000	00	–70 dB
10 1011	2B	–4 dB	01 0101	15	–19 dB			
10 1010	2A	–4.5 dB	01 0100	14	–20 dB			

**Registers 66 and 67**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 66	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	SMUL	SLV5	SLV4	SLV3	SLV2	SLV1	SLV0
Register 67	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	SMUR	SRV5	SRV4	SRV3	SRV2	SRV1	SRV0

**IDX[6:0]:** 100 0010b (42h): Register 66

**IDX[6:0]:** 100 0011b (43h): Register 67

**SMUL: Digital Soft Mute Control for SPL (Speaker Output, L-Channel)**

**SMUR: Digital Soft Mute Control for SPR (Speaker Output R-Channel)**

Default value: 1

SPOLP/SPOLN and SPORP/SPORN can be independently muted to the zero level when SMUL and SMUR = 1. These settings have precedence over analog volume level settings.

SMUL, SMUR = 0	Mute disabled
SMUL, SMUR = 1	Mute enabled (default)

**SLV[5:0]: Gain Setting for SPL (Speaker Output L-Channel)**

**SRV[5:0]: Gain Setting for SPR (Speaker Output R-Channel)**

Default value: 00 0000.

SPOLP/SPOLN and SPORP/SPORN can be independently controlled between 6 dB and –70 dB, with step size depending on the gain level as shown in [Table 8](#). Outputs may have zipper noise while changing levels. This noise can be reduced by selecting zero-cross detection (register 86, ZCRS).

**Table 8. Speaker Gain Level Setting**

SLV[5:0], SRV[5:0]	STEP	GAIN LEVEL SETTING	SLV[5:0], SRV[5:0]	STEP	GAIN LEVEL SETTING	SLV[5:0], SRV[5:0]	STEP	GAIN LEVEL SETTING
11 1111	3F	6 dB	10 1001	29	–5 dB	01 0011	13	–21 dB
11 1110	3E	5.5 dB	10 1000	28	–5.5 dB	01 0010	12	–22 dB
11 1101	3D	5 dB	10 0111	27	–6 dB	01 0001	11	–23 dB
11 1100	3C	4.5 dB	10 0110	26	–6.5 dB	01 0000	10	–24 dB
11 1011	3B	4 dB	10 0101	25	–7 dB	00 1111	0F	–26 dB
11 1010	3A	3.5 dB	10 0100	24	–7.5 dB	00 1110	0E	–28 dB
11 1001	39	3 dB	10 0011	23	–8 dB	00 1101	0D	–30 dB
11 1000	38	2.5 dB	10 0010	22	–8.5 dB	00 1100	0C	–32 dB
11 0111	37	2 dB	10 0001	21	–9 dB	00 1011	0B	–34 dB
11 0110	36	1.5 dB	10 0000	20	–9.5 dB	00 1010	0A	–36 dB
11 0101	35	1 dB	01 1111	1F	–10 dB	00 1001	09	–38 dB
11 0100	34	0.5 dB	01 1110	1E	–10.5 dB	00 1000	08	–40 dB
11 0011	33	0 dB	01 1101	1D	–11 dB	00 0111	07	–42 dB
11 0010	32	–0.5 dB	01 1100	1C	–12 dB	00 0110	06	–46 dB
11 0001	31	–1 dB	01 1011	1B	–13 dB	00 0101	05	–50 dB
11 0000	30	–1.5 dB	01 1010	1A	–14 dB	00 0100	04	–54 dB
10 1111	2F	–2 dB	01 1001	19	–15 dB	00 0011	03	–58 dB
10 1110	2E	–2.5 dB	01 1000	18	–16 dB	00 0010	02	–62 dB
10 1101	2D	–3 dB	01 0111	17	–17 dB	00 0001	01	–66 dB
10 1100	2C	–3.5 dB	01 0110	16	–18 dB	00 0000	00	–70 dB
10 1011	2B	–4 dB	01 0101	15	–19 dB			
10 1010	2A	–4.5 dB	01 0100	14	–20 dB			

**Registers 68 and 69**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 68	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	PMUL	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 69	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	PMUR	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

**IDX[6:0]:** 100 0100b (44h): Register 68

**IDX[6:0]:** 100 0101b (45h): Register 69

**PMUL: Digital Soft Mute Control for DAL (DAC, L-Channel)**

**PMUR: Digital Soft Mute Control for DAR (DAC R-Channel)**

Default value: 0

The digital inputs of the DAC can be independently muted by setting PMUL and PMUR = 1. The digital data is changed from the current attenuation level to mute level by a 1-dB step for every  $8/f_s$  time period. When PMUL and PMUR are set to 0, the digital data is changed from the mute level to the current attenuation level by a 1-dB step for every  $8/f_s$  time period. In the PCM3793A/94A, audible zipper noise can be reduced by selecting zero-cross detection (register 86, ZCRS).

PMUL, PMUR = 0	Mute disabled (default)
PMUL, PMUR = 1	Mute enabled

**ATL[5:0]: Digital Attenuation Setting for DAL (L-Channel DAC)**

**ATR[5:0]: Digital Attenuation Setting for DAR (R-Channel DAC)**

Default value: 11 1111b

The digital inputs of the DAC can be independently attenuated. The attenuation of the digital input is changed by a 1-dB step for every  $8/f_s$  time period. Audible zipper noise in the PCM3793A/94A can be reduced by selecting zero-cross detection (register 86, ZCRS).

**Table 9. Digital Attenuation Setting**

ATL[5:0], ATR[5:0]	ATTENUATION LEVEL SETTING	ATL[5:0], ATR[5:0]	ATTENUATION LEVEL SETTING	ATL[5:0], ATR[5:0]	ATTENUATION LEVEL SETTING
11 1111	3F	0 dB (default)	10 1001	29	-22 dB
11 1110	3E	-1 dB	10 1000	28	-23 dB
11 1101	3D	-2 dB	10 0111	27	-24 dB
11 1100	3C	-3 dB	10 0110	26	-25 dB
11 1011	3B	-4 dB	10 0101	25	-26 dB
11 1010	3A	-5 dB	10 0100	24	-27 dB
11 1001	39	-6 dB	10 0011	23	-28 dB
11 1000	38	-7 dB	10 0010	22	-29 dB
11 0111	37	-8 dB	10 0001	21	-30 dB
11 0110	36	-9 dB	10 0000	20	-31 dB
11 0101	35	-10 dB	01 1111	1F	-32 dB
11 0100	34	-11 dB	01 1110	1E	-33 dB
11 0011	33	-12 dB	01 1101	1D	-34 dB
11 0010	32	-13 dB	01 1100	1C	-35 dB
11 0001	31	-14 dB	01 1011	1B	-36 dB
11 0000	30	-15 dB	01 1010	1A	-37 dB
10 1111	2F	-16 dB	01 1001	19	-38 dB
10 1110	2E	-17 dB	01 1000	18	-39 dB
10 1101	2D	-18 dB	01 0111	17	-40 dB
10 1100	2C	-19 dB	01 0110	16	-41 dB
10 1011	2B	-20 dB	01 0101	15	-42 dB
10 1010	2A	-21 dB	01 0100	14	-43 dB
					Mute

## Register 70

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 70	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	DEM1	DEM0	PFM1	PFM0	SPX1	SPX0	RSV	OVER

**IDX[6:0]:** 100 0110b (46h): Register 70

### DEM[1:0]: De-Emphasis Filter Selection

Default value: 00

A digital de-emphasis filter is in front of the interpolation filter. One of three de-emphasis filters can be selected corresponding to the sampling rate, 32 kHz, 44.1 kHz, or 48 kHz.

DEM[1:0]	De-Emphasis Filter Selection
00	OFF (default)
01	32 kHz
10	44.1 kHz
11	48 kHz

### PFM[1:0]: Audio Interface Selection for DAC (Digital Input)

Default value: 00

The audio interface for the DAC digital input has I<sup>2</sup>S, right-justified, left-justified, and DSP formats.

PFM[1:0]	Audio Interface Selection for DAC Digital Input
00	I <sup>2</sup> S format (default)
01	Right-justified format
10	Left-justified format
11	DSP format

### SPX[1:0]: Digital Gain Control for DAC Input

Default value: 00

These bits are used to gain up the digital input data.

SPX[1:0]	Digital Gain Control for DAC input
00	0 dB (default)
01	6 dB
10	12 dB
11	18 dB

### OVER: Oversampling Control for Delta-Sigma DAC

Default value: 0

This bit is used to control the oversampling rate of delta-sigma DAC. When the PCM3793A/94A operates at low sampling rates (less than 24 kHz) and the SCK1 frequency is less than 12.5 MHz, OVER = 1 is recommended.

OVER = 0	128 f <sub>S</sub> (default)
OVER = 1	192 f <sub>S</sub> , 256 f <sub>S</sub> , 384 f <sub>S</sub>

**Register 71**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 71	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	SPSE	SPS1	SPS0	DFQ1	DFQ0

**IDX[6:0]:** 100 0111b (47h): Register 71

**SPSE: Enable of Spectrum Spreading**

Default value: 0

The class-D speaker amplifier output can cause RF interference due to switching noise. The PCM3793A can reduce peak noise by the use of spectrum spreading technology when SPSE = 1.

SPSE = 0	Disable (default)
SPSE = 1	Enable

**SPS[1:0]: Spectrum Spreading Efficiency**

Default value: 00

The spectrum-spreading efficiency of can be selected from low, medium, and high.

<b>SPS[1:0]</b>	<b>Spectrum Spreading Efficiency</b>
00	Low (default)
01	Medium
10	High
11	Reserved

**DFQ[1:0]: Switching Frequency for Speaker Amplifier (Class-D)**

Default value: 00

The switching frequency of the class-D speaker amplifier can be selected to avoid interference with other equipment.

<b>DFQ[1:0]</b>	<b>Class D Amplifier Switching Frequency</b>
00	1.5 MHz (default)
01	2.25 MHz
10	2.65 MHz
11	3 MHz

**Register 72**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 72	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	PMXR	PMXL

**IDX[6:0]:** 100 1000b (48h) Register 72

**PMXR: Power Up/Down for MXR (Mixer R-Channel)**

**PMXL: Power Up/Down for MXL (Mixer L-Channel)**

Default value: 0

These bits are used to control power up/down for the analog mixer.

PMXL, PMXR = 0	Power down (default)
PMXL, PMXR = 1	Power up

### Register 73

Register 73	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	PBIS	PDAR	PDAL	PHPC	PHPR	PHPL	PSPR	PSPL

**IDX[6:0]:** 100 1001b (49h): Register 73

#### **PBIS: Power Up/Down Control for Bias**

Default value: 0

This bit is used to control power up/down for the analog bias circuit.

PBIS = 0	Power down (default)
PBIS = 1	Power up

#### **PDAR: Power Up/Down Control for DAR (DAC and R-Channel Digital Filter)**

#### **PDAL: Power Up/Down Control for DAL (DAC and L-Channel Digital Filter)**

Default value: 0

These bits are used to control power up/down for the DAC and interpolation filter.

PDAR, PDAL = 0	Power down (default)
PDAR, PDAL = 1	Power up

#### **PHPC: Power Up/Down Control for HPC (Headphone COM/Monaural Output)**

Default value: 0

This bit is used to control power up/down for the headphone COM or monaural line amplifier.

PHPC = 0	Power down (default)
PHPC = 1	Power up

#### **PHPR: Power Up/Down Control for HPR (Line or R-Channel Headphone Output)**

#### **PHPL: Power Up/Down Control for HPL (Line or L-Channel Headphone Output)**

Default value: 0

These bits are used to control power up/down for the headphone amplifier.

PHPR, PHPL = 0	Power down (default)
PHPR, PHPL = 1	Power up

#### **PSPR: Power Up/Down Control for SPR (R-Channel Speaker Output, PCM3793A)**

#### **PSPL: Power Up/Down Control for SPL (L-Channel Speaker Output, PCM3793A)**

Default value: 0

These bits are used to control power up/down for the PCM3793A speaker amplifier. These bits should be set to 0 for the PCM3794A, because it has no speaker outputs.

PSPR, PSPL = 0	Power down (default)
PSPR, PSPL = 1	Power up

## Register 74

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 74	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	CMS2	CMS1	CMS0	HPS1	HPS0	SPKS	PCOM

**IDX[6:0]:** 100 1010b (4Ah): Register 74

### **CMS[2:0]: Output Selection for HPC (Headphone COM/Monaural Output)**

Default value: 000

The HPCOM/MONO output can be selected from several input analog sources, including inverted HPOR output, inverted HPOL output, and monaural output.

<b>CMS[2:0]</b>	<b>HPCOM/MONO Output Selection</b>
0 0 0	Common voltage (0.5 V <sub>CC</sub> ) output for capless mode (default)
0 0 1	Monaural output
0 1 0	Inverted HPOL output
1 0 0	Inverted HPOR output
Others	Reserved

### **HPS[1:0]: Line or Headphone Output Configuration**

Default value: 00

HPOL/LOL and HPOR/LOR can be configured selected as follows.

<b>HPS[1:0]</b>	<b>Line or Headphone Output Configuration</b>
0 0	Stereo output (default)
0 1	Single monaural output
1 0	Differential monaural output
1 1	Reserved

### **SPKS: Speaker Output Configuration**

Default value: 00

SPOLP/SPOLN and SPORP/SPORN can be configured as follows.

SPKS = 0	Stereo output (default)
SPKS = 1	Monaural output

### **PCOM: Power Up/Down Control for V<sub>COM</sub>**

Default value: 0

This bit is used to control power up/down for V<sub>COM</sub>.

PCOM = 0	Power down (default)
PCOM = 1	Power up

**Register 75**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 75	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	HPDP	HPDE	RSV	SDHC	SDHR	SDHL	SDSR	SDSL

**IDX[6:0]:** 1001011b (4Bh): Register 75

**HPDP: Headphone Insertion Detection Polarity**

**HPDE: Enable for Headphone Insertion Detection**

Default value: 0

**Table 10. Headphone Insertion Detection**

HPDE	HPDP	HDTI (PIN 8)	HP OUTPUT	SP OUTPUT
1	0	0	Down	Up
1	0	1	Up	Down
1	1	0	Up	Down
1	1	1	Down	Up
0	X	X	Headphone insertion detection disabled	

**SDHC: Short Protection Disable for HPC (Headphone COM/Monaural Output)**

**SDHR: Short Protection Disable for HPR (R-Channel Headphone)**

**SDHL: Short Protection Disable for HPL (L-Channel Headphone)**

Default value: 0

Short-circuit protection can be disabled if this function is not needed in an application.

SDHC, SDHR, SDHL = 0	Enabled (default)
SDHC, SDHR, SDHL = 1	Disabled

**SDSR: Thermal Protection Disable for SPR (Speaker Amplifier R-Channel)**

**SDSL: Thermal Protection Disable for SPL (Speaker Amplifier L-Channel)**

Default value: 0

The thermal protection circuit can be disabled if this function is not needed in an application.

SDSR, SDSL = 0	Enabled (default)
SDSR, SDSL = 1	Disabled

**Register 76**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 76	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	RLSR	RLSL

**IDX[6:0]:** 100 1100b (4Ch): Register 76

**RLSR: Reset Thermal Protection Circuit for SPR (R-Channel Speaker Amplifier)**

**RLSL: Reset Thermal Protection Circuit for SPL (L-Channel Speaker Amplifier)**

Default value: 0

A thermal protection circuit puts the device in power-down status after it detects a temperature of approximately 150°C on the die. These bits must be set to 1 to restore power to the speaker amplifier.

RLSR, RLSL = 0	Operation (default)
RLSR, RLSL = 1	Reset (set to 0 automatically after being set to 1)

**Register 77**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 77	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	HPDS	RSV	RSV	STHC	STHR	STHL	STSR	STSL

**IDX[6:0]:** 100 1101b (4Dh): Register 77

**HPDS: Headphone Detection Status**

Default value: 0

The HPDS bit shows the status of insertion detection for the headphone. This is a read-only bit. The polarity depends on the register 75 (HPDP) setting.

HPDS = 0	HDTI input (when HPDP = 0) (default)
HPDS = 1	Inverted HDTI input (When HPDP = 1)

**STHC: Short Protection Status for HPC (Headphone COM/Monaural Output)**

**STHR: Short Protection Status for HPR (R-Channel Headphone)**

**STHL: Short Protection Status for HPL (L-Channel Headphone)**

These bits can be used to read short protection status through the I<sup>2</sup>C interface.

STHC, STHR, STHL = 0	Detect short circuit
STHC, STHR, STHL = 1	Not detect short circuit

**STSR: Thermal Protection Status for SPR (R-Channel Speaker)**

**STSL: Thermal Protection Status for SPL (L-Channel Speaker)**

These bits can be used to read thermal protection status through the I<sup>2</sup>C interface.

STSR, STSL = 0	Detect thermal protection
STSR, STSL = 1	Not detect thermal protection

**Registers 79 and 80**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 79	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	ALV5	ALV4	ALV3	ALV2	ALV1	ALV0
Register 80	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	ARV5	ARV4	ARV3	ARV2	ARV1	ARV0

**IDX[6:0]:** 100 1111b (4Fh): Register 79

**IDX[6:0]:** 101 0000b (50h): Register 80

**ALV[5:0]: Gain Control for PG3 (R-Channel ADC Analog Input)**

**ARV[5:0]: Gain Control for PG4 (L-Channel ADC Analog Input)**

Default value: 00

The gain of the PG3 and PG4 inputs to the ADC can be independently controlled from 30 dB to –12 dB in 1-dB steps. The ADC output may have zipper noise while changing the level. This noise can be reduced by using zero-cross detection (register 86, ZCRS).

**Table 11. Gain Level Setting**

ALV[5:0], ARV[5:0]		GAIN LEVEL SETTING	ALV[5:0], ARV[5:0]		GAIN LEVEL SETTING
10 1010	2A	30 dB	01 0100	14	8 dB
10 1001	29	29 dB	01 0011	13	7 dB
10 1000	28	28 dB	01 0010	12	6 dB
10 0111	27	27 dB	01 0001	11	5 dB
10 0110	26	26 dB	01 0000	10	4 dB
10 0101	25	25 dB	00 1111	0F	3 dB
10 0100	24	24 dB	00 1110	0E	2 dB
10 0011	23	23 dB	00 1101	0D	1 dB
10 0010	22	22 dB	00 1100	0C	0 dB
10 0001	21	21 dB	00 1011	0B	–1 dB
10 0000	20	20 dB	00 1010	0A	–2 dB
01 1111	1F	19 dB	00 1001	09	–3 dB
01 1110	1E	18 dB	00 1000	08	–4 dB
01 1101	1D	17 dB	00 0111	07	–5 dB
01 1100	1C	16 dB	00 0110	06	–6 dB
01 1011	1B	15 dB	00 0101	05	–7 dB
01 1010	1A	14 dB	00 0100	04	–8 dB
01 1001	19	13 dB	00 0011	03	–9 dB
01 1000	18	12 dB	00 0010	02	–10 dB
01 0111	17	11 dB	00 0001	01	–11 dB
01 0110	16	10 dB	00 0000	00	–12 dB (default)
01 0101	15	9 dB			

**Register 81**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 81	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	HPF1	HPF0	RMUL	RMUR	RSV	DSMC	RFM1	RFM0

**IDX[6:0]:** 101 0001b (51h): Register 81

**HPF[1:0]: High-Pass Filter Selection**

Default value: 00

The PCM3793A/94A has a digital high-pass filter to remove dc voltage at the input of the ADC. The cutoff frequency of the high-pass filter can be selected.

HPF [1:0]	High-Pass Filter Selection
0 0	$f_C = 4$ Hz at 48 kHz (default)
0 1	$f_C = 240$ Hz at 48 kHz
1 0	$f_C = 120$ Hz at 48 kHz
1 1	High-pass filter disabled

**RMUL: Digital Soft Mute Control for L-Channel ADC**

**RMUR: Digital Soft Mute Control for R-Channel ADC**

Default value: 1

The digital output of the ADC can be independently muted by setting RMUL and RMUR = 1. The digital data is changed from the current attenuation level to mute level by a 1-dB step for every  $8/f_S$  time period. When PMUL and PMUR are set to 0, the digital data is changed from the mute level to the current attenuation level by a 1-dB step for every  $8/f_S$  time period. In the PCM3793A/94A, audible zipper noise can be reduced by selecting zero-cross detection (register 86, ZCRS).

RMUL, RMUR = 0	Mute disabled
RMUL, RMUR = 1	Mute enabled (default)

**DSMC: Waiting Time for ADC Mute Off at Power Up**

Default value: 0

The ADC digital output has an optional delay after power up when DSMC = 0. It is recommended to set DSMC = 0.

DSMC = 0	10 ms at 48 kHz (default)
DSMC = 1	No delay

**RFM[1:0]: Audio Interface Selection for ADC (Digital Output)**

Default value: 00

The audio interface for the ADC digital input supports I<sup>2</sup>S, right-justified, left-justified, and DSP formats.

RFM [1:0]	Audio Interface Selection for ADC Digital Output
0 0	I <sup>2</sup> S format (default)
0 1	Right-justified format
1 0	Left-justified format
1 1	DSP format

**Register 82**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 82	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	PAIR	PAIL	PADS	PMCB	PADR	PADL

**IDX[6:0]:** 101 0010b (52h): Register 82

**PAIR: Power Up/Down for PG2 and PG6 (Gain Amplifier for R-Channel Analog Input)**

**PAIL: Power Up/Down for PG1 and PG5 (Gain Amplifier for L-Channel Analog Input)**

Default value: 0

These bits are used to control power up/down for PG2 and PG6 (gain amplifier for analog input).

PAIR, PAIL = 0	Power down (default)
PAIR, PAIL = 1	Power up

**PADS: Power Up/Down for D2S (Differential Amplifier) of AIN1L and AIN1R**

Default value: 0

This bit is used to control power up/down for D2S (differential-to-single amplifier).

PADS = 0	Power down (default)
PADS = 1	Power up

**PMCB: Power Up/Down Control for Microphone Bias Source**

Default value: 0

This bit is used to control power up/down for the microphone bias source.

PMCB = 0	Power down (default)
PMCB = 1	Power up

**PADR: Power Up/Down Control for ADR (ADC and R-Channel Digital Filter)**

**PADL: Power Up/Down Control for ADL (ADC and L-Channel Digital Filter)**

Default value: 0

These bits are used to control power up/down for the ADC and decimation filter.

PADR, PADL = 0	Power down (default)
PADR, PADL = 1	Power up

**Register 83**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 83	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RALC	RSV	RRTC	RATC	RCP1	RCP0	RLV1	RLV0

**IDX[6:0]:** 101 0011b (53h): Register 83

**RALC: Automatic Level Control (ALC) Enable for Recording**

Default value: 0

Automatic level control can be enabled with some parameters for microphone input or lower analog source level.

RALC = 0	Disable (default)
RALC = 1	Enable

**RRTC: ALC Recovery Time Control for Recording**

Default value: 0

This bit is used to select the recovery time for the ALC. The response is shown in [Figure 37](#).

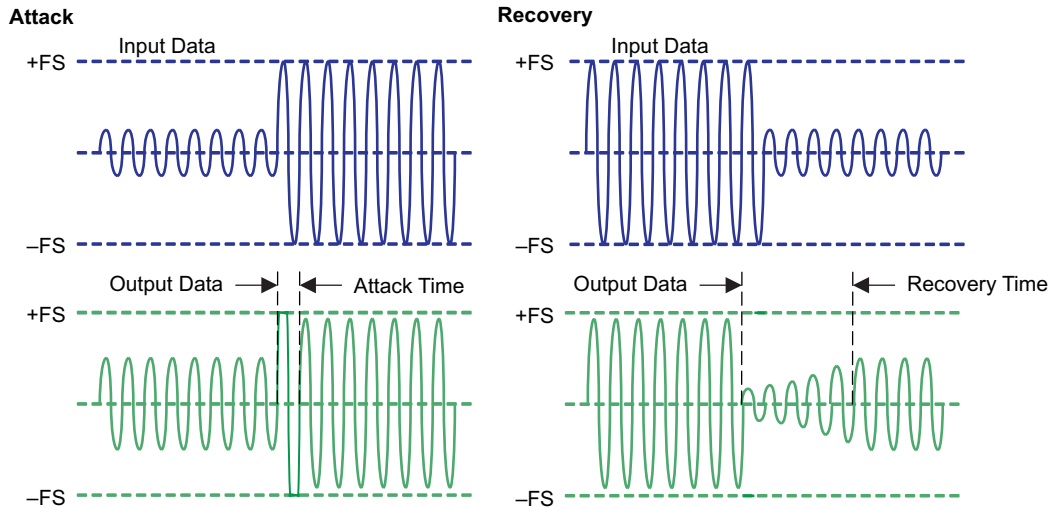
RRTC = 0	3.4 s (default)
RRTC = 1	13.6 s

**RATC: ALC Attack Time Control for Recording**

Default value: 0

This bit is used to select the attack time for the ALC. The response is shown in [Figure 37](#).

RATC = 0	1 ms (default)
RATC = 1	2 ms



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**Figure 37. Attack and Recovery Time Response**

### RCP[1:0]: ALC Compression Level Control for Recording

Default value: 00

These bits are used to set the compression level for the ALC. The characteristic is shown in [Figure 38](#).

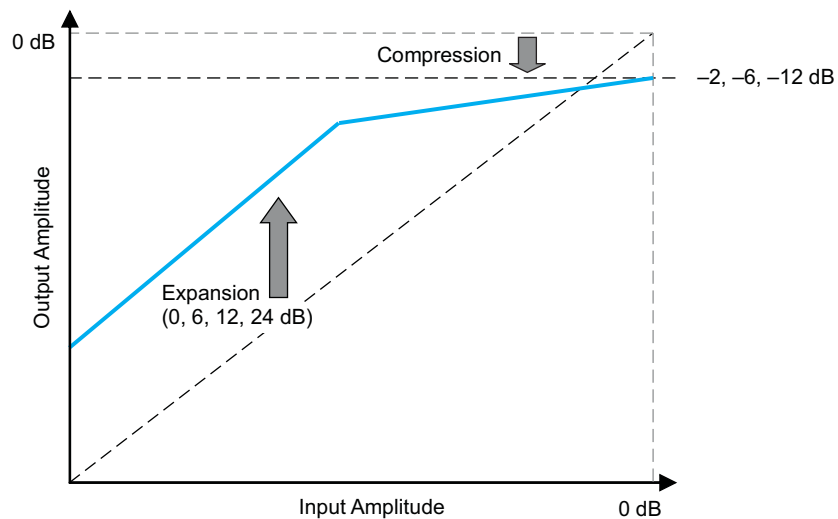
RCP[1:0]	ALC Compression Level Control for Recording
0 0	-2 dB (default)
0 1	-6 dB
1 0	-12 dB
1 1	Reserved

### RLV[1:0]: ALC Expansion Level Control for Recording

Default value: 00

These bits are used to set the expansion level for the ALC. The characteristic is shown in [Figure 38](#).

RLV[1:0]	ALC Gain Level Control for Recording
0 0	0 dB (default)
0 1	6 dB
1 0	14 dB
1 1	24 dB



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**Figure 38. Compression and Expansion Characteristics**

**Registers 84–86**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 84	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	MSTR	RSV	BIT0
Register 85	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	RSV	NPR5	NPR4	NPR3	NPR2	NPR1	NPR0
Register 86	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	MBST	MSR2	MSR1	MSR0	ATOD	RSV	RSV	ZCRS

**IDX[6:0]:** 101 0100b (54h): Register 84

**IDX[6:0]:** 101 0101b (55h): Register 85

**IDX[6:0]:** 101 0110b (56h): Register 86

**MSTR: Master or Slave Selection for Audio Interface**

Default value: 0

This bit is used to select either master or slave mode for the audio interface. In master mode, the PCM3793A/94A generates LRCK and BCK from the system clock. In slave mode, it receives LRCK and BCK from another device.

MSTR = 0	Slave interface (default)
MSTR = 1	Master interface

**BIT0: Bit Length Selection for Audio Interface**

Default value: 1

This bit is used to select the data bit length for DAC input.

BIT0 = 0	Reserved
BIT0 = 1	16 bits (default)

**SRST: System Reset**

Default value: 0

This bit is used to enable system reset. All circuits are reset by setting SRST = 1. After completing the reset sequence, SRST is set to 0 automatically.

SRST = 0	Reset disabled (default)
SRST = 1	Reset enabled

**NPR[5:0]: System Clock Rate Selection**

Default value: 000000

**MSR[2:0]: System Clock Dividing Rate Selection in Master Mode (Register 70)**

Default value: 000

These bits are used to select the system clock rate and the dividing rate of the input system clock. See [Table 12](#) for the details.

**Table 12. System Clock Frequency for Common-Audio Clock**

SYSTEM CLOCK SCK (MHz)	ADC SAMPLING RATE ADC $f_s$ (kHz)	DAC SAMPLING RATE DAC $f_s$ (kHz)	REGISTER SETTINGS <sup>(1)</sup>		BIT CLOCK BCK ( $f_s$ )
			MSR[2:0]	NPR[5:0]	
6.144	24 (SCK/256)		010	00 0000	64
	16 (SCK/384)		011	00 0000	64
	12 (SCK/512)		100	00 0000	64
	8 (SCK/768)		101	00 0000	64
	6 (SCK/1024)		110	00 0000	64
	4 (SCK/1536)		111	00 0000	64
8.192	32 (SCK/256)		010	00 0000	64
	16 (SCK/512)		100	00 0000	64
	8 (SCK/1024)		110	00 0000	64
12.288	48 (SCK/256)		010	00 0000	64
	32 (SCK/384)		011	00 0000	64
	24 (SCK/512)		100	00 0000	64
	16 (SCK/768)		101	00 0000	64
	12 (SCK/1024)		110	00 0000	64
	8 (SCK/1536)		111	00 0000	64
18.432	48 (SCK/384)		011	00 0000	64
	24 (SCK/768)		101	00 0000	64
	12 (SCK/1536)		111	00 0000	64
5.6448	22.05 (SCK/256)		010	00 0000	64
	14.7 (SCK/384)		011	00 0000	64
	11.025 (SCK/512)		100	00 0000	64
	7.35 (SCK/768)		101	00 0000	64
	5.5125 (SCK/1024)		110	00 0000	64
	3.675 (SCK/1536)		111	00 0000	64
11.2896	44.1 (SCK/256)		010	00 0000	64
	29.4 (SCK/384)		011	00 0000	64
	22.05 (SCK/512)		100	00 0000	64
	14.7 (SCK/768)		101	00 0000	64
	11.025 (SCK/1024)		110	00 0000	64
	7.35 (SCK/1536)		111	00 0000	64

(1) Other settings are reserved.

**Table 13. System Clock Frequency for Application-Specific Clock**

SYSTEM CLOCK SCK (MHz)	ADC SAMPLING RATE ADC $f_s$ (kHz)	DAC SAMPLING RATE DAC $f_s$ (kHz)	REGISTER SETTINGS		BIT CLOCK BCK ( $f_s$ )
			MSR[2:0]	NPR[5:0]	
13.5	48.214 (SCK/280)		010	00 0010	70
	44.407 (SCK/304)		010	00 0001	76
	32.142 (SCK/420)		010	10 0010	70
	24.107 (SCK/560)		100	00 0010	70
	22.203 (SCK/608)		100	00 0001	76
	16.071 (SCK/840)		100	10 0010	70
	12.053 (SCK/1120)		110	00 0010	70
	8.035 (SCK/1680)		110	10 0010	70
27	48.214 (SCK/560)		010	01 0010	70
	44.407 (SCK/608)		010	01 0001	76
	32.142 (SCK/840)		010	11 0010	70
	24.107 (SCK/1120)		100	01 0010	70
	22.203 (SCK/1216)		100	01 0001	76
	16.071 (SCK/1680)		100	11 0010	70
	12.053 (SCK/2240)		110	01 0010	70
	8.035 (SCK/3360)		110	11 0010	70
12	48.387 (SCK/248)		010	00 0100	62
	44.117 (SCK/272)		010	00 0011	68
	32.258 (SCK/372)		010	10 0100	62
	24.193 (SCK/496)		100	00 0100	62
	22.058 (SCK/544)		100	00 0011	68
	16.129 (SCK/744)		100	10 0100	62
	12.096 (SCK/992)		110	00 0100	62
	8.064 (SCK/1488)		110	10 0100	62
24	48.387 (SCK/496)		010	01 0100	62
	44.117 (SCK/544)		010	01 0011	68
	32.258 (SCK/744)		010	11 0100	62
	24.193 (SCK/992)		100	01 0100	62
	22.058 (SCK/1088)		100	01 0011	68
	16.129 (SCK/1488)		100	11 0100	62
	12.096 (SCK/1984)		110	01 0100	62
	8.064 (SCK/2976)		110	11 0100	62
19.2	48.484 (SCK/396)		011	00 0110	66
	44.444 (SCK/432)		011	00 0101	72
	32.323 (SCK/594)		011	10 0110	66
	24.242 (SCK/792)		101	00 0110	66
	22.222 (SCK/864)		101	00 0101	72
	16.161 (SCK/1188)		101	10 0110	66
	12.121 (SCK/1584)		111	00 0110	66
	8.080 (SCK/2376)		111	10 0110	66

**Table 13. System Clock Frequency for Application-Specific Clock (continued)**

SYSTEM CLOCK SCK (MHz)	ADC SAMPLING RATE ADC $f_s$ (kHz)	DAC SAMPLING RATE DAC $f_s$ (kHz)	REGISTER SETTINGS		BIT CLOCK BCK ( $f_s$ )
			MSR[2:0]	NPR[5:0]	
38.4	48.484 (SCK/792)		011	01 0110	66
	44.444 (SCK/864)		011	01 0101	72
	32.323 (SCK/1188)		011	11 0110	66
	24.242 (SCK/1584)		101	01 0110	66
	22.222 (SCK/1728)		101	01 0101	72
	16.161 (SCK/2376)		101	11 0110	66
	12.121 (SCK/3168)		111	01 0110	66
	8.080 (SCK/4752)		111	11 0110	66
13	47.794 (SCK/272)		010	00 1000	68
	43.918 (SCK/296)		010	00 0111	74
	31.862 (SCK/408)		010	10 1000	68
	23.897 (SCK/544)		100	00 1000	68
	21.959 (SCK/592)		100	00 0111	74
	15.931 (SCK/816)		100	10 1000	68
	11.948 (SCK/1088)		110	00 1000	68
	7.965 (SCK/1632)		110	10 1000	68
26	47.794 (SCK/544)		010	01 1000	68
	43.918 (SCK/592)		010	01 0111	74
	31.862 (SCK/816)		010	11 1000	68
	23.897 (SCK/1088)		100	01 1000	68
	21.959 (SCK/1184)		100	01 0111	74
	15.931 (SCK/1632)		100	11 1000	68
	11.948 (SCK/2176)		110	01 1000	68
	7.965 (SCK/3264)		110	11 1000	68
19.68	48.235 (SCK/408)		011	00 1010	68
	44.324 (SCK/444)		011	00 1001	74
	32.156 (SCK/612)		011	10 1010	68
	24.117 (SCK/816)		101	00 1010	68
	22.162 (SCK/888)		101	00 1001	74
	16.078 (SCK/1224)		101	10 1010	68
	12.058 (SCK/1632)		111	00 1010	68
	8.039 (SCK/2448)		111	10 1010	68
39.36	48.235 (SCK/816)		011	01 1010	68
	44.324 (SCK/888)		011	01 1001	74
	32.156 (SCK/1224)		011	11 1010	68
	24.117 (SCK/1632)		101	01 1010	68
	22.162 (SCK/1776)		101	01 1001	74
	16.078 (SCK/2448)		101	11 1010	68
	12.058 (SCK/3264)		111	01 1010	68
	8.039 (SCK/4896)		111	11 1010	68

### **MBST: BCK Output Configuration in Master Mode**

Default value: 0

This bit is used to control the BCK output configuration in master mode. In master mode, this bit sets the BCK output configuration to normal mode or burst mode. In normal mode (MBST = 0), the BCK clock runs continuously. In burst mode (MBST = 1), the BCK clock runs intermittently, and the number of clock cycles per LRCK period is reduced to equal the number of bits of audio data being transmitted. Operating in burst mode reduces the power consumption of  $V_{IO}$  (I/O cell power supply). This is effective in master mode (register 69 MSTR = 1).

MBST = 0	Normal mode (default)
MBST = 1	Burst mode

### **ATOD: ADC Digital Output to DAC Digital Input (Loopback)**

Default value: 0

The ADC digital output is internally connected to the DAC digital input by setting ATOD = 1. This setting can be used to debug ADC functions or to monitor a recording.

ATOD= 0	Disabled (default)
ATOD= 1	Enabled

### **ZCRS: Zero-Cross for Digital Attenuation/Mute and Analog Gain Setting**

Default value: 0

This bit is used to enable the zero-cross detector, which reduces zipper noise while the digital soft mute, digital attenuation analog gain setting, or analog volume setting is being changed. If no zero-cross data is input for a  $512/f_s$  period (10.6 ms at a 48-kHz sampling rate), then a time-out occurs and the PCM3793A/94A starts changing the attenuation, gain, or volume level. The zero-cross detector cannot be used with continuous-zero and dc data.

ZCRS = 0	Zero-cross disabled (default)
ZCRS = 1	Zero-cross enabled

**Register 87**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 87	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AD2S	RSV	AIR1	AIR0	RSV	RSV	AIL1	AIL0

**IDX[6:0]:** 101 0111b (57h): Register 87

**AD2S: Differential Amplifier Selector (MUX3 and MUX4)**

Default value: 0

The PCM3793A/94A has stereo single-input amplifiers (PG1, PG2) and a monaural differential-input amplifier (D2S) which can output signals to the ADC. MUX3 and MUX4 can be selected as the monaural differential input by setting AD2S = 1.

AD2S = 0	Single-input amplifiers (default)
AD2S = 1	Differential-input amplifier

**AIL[1:0]: AIN1L, AIN2L, and AIN3L Selector (MUX1)**

Default value: 00

These bits are used to select one of the three analog inputs, AIN1L, AIN2L, or AIN3L.

AIL[1:0]	AIN L-channel Select
0 0	Disconnect (default)
0 1	AIN1L
1 0	AIN2L
1 1	AIN3L

**AIR[1:0]: AIN1R, AIN2R, and AIN3R Selector (MUX2)**

Default value: 00

These bits are used to select one of the three stereo analog inputs, AIN1R, AIN2R, or AIN3R.

AIR[1:0]	AIN R-channel Select
0 0	Disconnect (default)
0 1	AIN1R
1 0	AIN2R
1 1	AIN3R

**Register 88**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 88	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	MXR2	MXR1	MXR0	RSV	MXL2	MXL1	MXL0

**IDX[6:0]:** 101 1000b (58h): Register 88

**MXR2: Mixing SW6 to MXR (R-Channel Mixing Amplifier) From L-Channel Analog Input**

Default value: 0

This bit is used to mix the analog source into MXR (R-ch mixing amplifier) from the L-ch analog input.

MXR2 = 0	Disable (default)
MXR2 = 1	Enable

**MXR1: Mixing SW4 to MXR (R-Channel Mixing Amplifier) From R-Channel Analog Input**

Default value: 0

This bit is used to mix the analog source into MXR (R-ch mixing amplifier) from the R-ch analog input.

MXR1 = 0	Disable (default)
MXR1 = 1	Enable

**MXR0: Mixing SW5 to MXR (R-Channel Mixing Amplifier) From R-Channel DAC**

Default value: 0

This bit is used to mix the analog source into MXR (R-ch mixing amplifier) from the R-ch DAC.

MXR0 = 0	Disable (default)
MXR0 = 1	Enable

**MXL2: Mixing SW3 to MXL (L-Channel Mixing Amplifier) From R-Channel Analog Input**

Default value: 0

This bit is used to mix the analog source into MXL (L-ch mixing amplifier) from the R-ch analog input.

MXL2 = 0	Disable (default)
MXL2 = 1	Enable

**MXL1: Mixing SW1 to MXL (L-Channel Mixing Amplifier) From L-Channel Analog Input**

Default value: 0

This bit is used to mix the analog source into MXL (L-ch mixing amplifier) from the L-ch analog input.

MXL1 = 0	Disable (default)
MXL1 = 1	Enable

**MXL0: Mixing SW2 to MXL (L-Channel Mixing Amplifier) From L-Channel DAC**

Default value: 0

This bit is used to mix the analog source into MXL (L-ch mixing amplifier) from the L-ch DAC.

MXL0 = 0	Disable (default)
MXL0 = 1	Enable

**Register 89**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 89	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	GMR2	GMR1	GMR0	RSV	GML2	GML1	GML0

**IDX[6:0]:** 101 1001b (59h): Register 89

**GMR[2:0]: Gain Level Control for PG6 (Gain Amplifier for Analog Input or R-Channel Bypass)**

**GML[2:0]: Gain Level Control for PG5 (Gain Amplifier for Analog Input or L-Channel Bypass)**

Default value: 111

These bits are used for setting the gain level of the analog source to the mixing amplifier. It is recommended to set the gain level to avoid saturation in the analog mixer.

<b>GMR[2:0]</b> <b>GML[2:0]</b>	<b>Gain Level Control for PG6</b> <b>Gain Level Control for PG5</b>
0 0 0	-21 dB
0 0 1	-18 dB
0 1 0	-15 dB
0 1 1	-12 dB
1 0 0	-9 dB
1 0 1	-6 dB
1 1 0	-3 dB
1 1 1	0 dB (default)

**Register 90**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 90	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	G20R	G20L

**IDX[6:0]:** 1011010b (5Ah): Register 90

**G20R: 20-dB Boost for PG2 (Gain Amplifier for AIN1R, AIN2R, and AIN3R)**

Default value: 0

This bit is used to boost the microphone signal when the analog input is small.

G20R = 0	0 dB (default)
G20R = 1	20-dB boost

**G20L: 20-dB Boost for PG1 (Gain Amplifier for AIN1L, AIN2L, and AIN3L)**

Default value: 0

This bit is used to boost the microphone signal when the analog input is small.

G20L = 0	0 dB (default)
G20L = 1	20-dB boost

**Register 92**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 92	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	LPAE	RSV	RSV	LGA4	LGA3	LGA2	LGA1	LGA0

**IDX[6:0]:** 101 1100b (5Ch): Register 92

**LPAE: Gain Adjustment for Bass Boost Gain Control**

Default value: 0

A gain setting for bass boost may cause digital data may saturation, depending on the input data level. Where this could occur, LPAE can be used to set the same attenuation level as the bass boost gain level for the digital input data.

LPAE = 0	Disable (default)
LPAE = 1	Enable

**LGA[4:0]: Bass Boost Gain Control**

Default value: 0 0000

These bits are used to set the bass boost gain level for the digital data. The detailed characteristics are shown in the [Typical Performance Curves](#).

LGA[4:0]	TONE CONTROL GAIN (BASS)	LGA[4:0]	TONE CONTROL GAIN (BASS)
0 0000	0 dB (default)	0 1111	0 dB
0 0011	12 dB	1 0000	-1 dB
0 0100	11 dB	1 0001	-2 dB
0 0101	10 dB	1 0010	-3 dB
0 0110	9 dB	1 0011	-4 dB
0 0111	8 dB	1 0100	-5 dB
0 1000	7 dB	1 0101	-6 dB
0 1001	6 dB	1 0110	-7 dB
0 1010	5 dB	1 0111	-8 dB
0 1011	4 dB	1 1000	-9 dB
0 1100	3 dB	1 1001	-10 dB
0 1101	2 dB	1 1010	-11 dB
0 1110	1 dB	1 1011	-12 dB

### Register 93

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 93	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	MGA4	MGA3	MGA2	MGA1	MGA0

**IDX[6:0]:** 101 1101b (5Dh): Register 93

**MGA[4:0]: Middle Boost Gain Control**

Default value: 0 0000

These bits are used to set the midrange boost gain level for the digital data. The detailed characteristics are shown in the [Typical Performance Curves](#).

MGA[4:0]	TONE CONTROL GAIN (MIDRANGE)	MGA[4:0]	TONE CONTROL GAIN (MIDRANGE)
0 0000	0 dB (default)	0 1111	0 dB
0 0011	12 dB	1 0000	-1 dB
0 0100	11 dB	1 0001	-2 dB
0 0101	10 dB	1 0010	-3 dB
0 0110	9 dB	1 0011	-4 dB
0 0111	8 dB	1 0100	-5 dB
0 1000	7 dB	1 0101	-6 dB
0 1001	6 dB	1 0110	-7 dB
0 1010	5 dB	1 0111	-8 dB
0 1011	4 dB	1 1000	-9 dB
0 1100	3 dB	1 1001	-10 dB
0 1101	2 dB	1 1010	-11 dB
0 1110	1 dB	1 1011	-12 dB

### Register 94

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 94	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	HGA4	HGA3	HGA2	HGA1	HGA0

**IDX[6:0]:** 101 1110b (5Eh): Register 94

**HGA[4:0]: Treble Boost Gain Control ( $f_c = 5$  kHz)**

Default value: 0 0000

These bits are used to set the treble boost gain level for the digital data. The detailed characteristics are shown in the [Typical Performance Curves](#).

HGA[4:0]	TONE CONTROL GAIN (TREBLE)	HGA[4:0]	TONE CONTROL GAIN (TREBLE)
0 0000	0 dB (default)	0 1111	0 dB
0 0011	12 dB	1 0000	-1 dB
0 0100	11 dB	1 0001	-2 dB
0 0101	10 dB	1 0010	-3 dB
0 0110	9 dB	1 0011	-4 dB
0 0111	8 dB	1 0100	-5 dB
0 1000	7 dB	1 0101	-6 dB
0 1001	6 dB	1 0110	-7 dB
0 1010	5 dB	1 0111	-8 dB
0 1011	4 dB	1 1000	-9 dB
0 1100	3 dB	1 1001	-10 dB
0 1101	2 dB	1 1010	-11 dB
0 1110	1 dB	1 1011	-12 dB

**Register 95**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 95	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SDAS	3DEN	RSV	3FL0	3DP3	3DP2	3DP1	3DP0

**IDX[6:0]:** 101 1111b (5Fh): Register 95

**SDAS: Source Select for Sound Effect (Tone Control, 3-D Sound, Notch Filter, Mono Mix)**

Default value: 0

The PCM3793A/94A includes sound effect circuits (tone control, 3-D sound, notch filter, mono mix) which can be used to filter either the digital input to the DAC or the digital output from the ADC. This bit selects the signal source of the sound effect circuit.

SDAS = 0	DAC digital input (default)
SDAS = 1	ADC digital output

**3DEN: 3-D Sound Effect Enable**

Default value: 0

This bit is used for enabling the 3-D sound effect filter. This filter has two independently controlled parameters.

3DEN = 0	Disable (default)
3DEN = 1	Enable

**3FL0: Filter Selection for 3-D Sound**

Default value: 0

This bit is used for selecting from two types of filter, narrow and wide. These filters have a different 3-D performance effect.

3FL0 = 0	Narrow (default)
3FL0 = 1	Wide

**3DP[3:0]: Efficiency for 3-D Sound Effects**

Default value: 0000

These bits are used for adjusting the 3-D sound efficiency. Higher percentages have greater efficiency.

<b>3DP[3:0]</b>	<b>3D Sound Effect Efficiency</b>
0 0 0 0	0% (default)
0 0 0 1	10%
0 0 1 0	20%
0 0 1 1	30%
0 1 0 0	40%
0 1 0 1	50%
0 1 1 0	60%
0 1 1 1	70%
1 0 0 0	80%
1 0 0 1	90%
1 0 1 0	100%
1 0 1 1	Reserved
:	:
1 1 1 1	Reserved

## Register 96

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 96	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	NEN2	NEN1	NUP2	NUP1	RSV	RSV	RSV	MXEN

**IDX[6:0]:** 110 0000b (60h): Register 96

### **NEN2: Second-Stage Notch Filter Enable**

Default value: 0

PCM3793A/94A has two notch filters with characteristics that can be set separately. This bit is used to enable the second stage.

NEN2 = 0	Disable (default)
NEN2 = 1	Enable

### **NEN1: First-Stage Notch Filter Enable**

Default value: 0

PCM3793A/94A has two notch filters with characteristics that can be set separately. This bit is used to enable the first stage.

NEN1 = 0	Disable (default)
NEN1 = 1	Enable

### **NUP2: Second-Stage Notch Filter Coefficients Update**

Default value: 0

This bit is used to update the coefficients for the second-stage notch filter. The coefficients set by registers 101, 102, 103, and 104 are updated when NUP2 = 1.

NUP2 = 0	No Update (default)
NUP2 = 1	Update (set to 0 automatically after set to 1)

### **NUP1: First-Stage Notch Filter Coefficients Update**

Default value: 0

This bit is used to update the coefficients for the first-stage notch filter. The coefficients set by registers 97, 98, 99, and 100 are updated when NUP1 = 1.

NUP1 = 0	No Update (default)
NUP1 = 1	Update (set to 0 automatically after being set to 1)

### **MXEN: Digital Monaural Mixing**

Default value: 0

This bit is used to enable or disable monaural mixing in the section that combines L-ch data and R-ch data.

MXEN = 0	Stereo (default)
MXEN = 1	Monaural Mixing

**Registers 97–100**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 97	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	F107	F106	F105	F104	F103	F102	F101	F100
Register 98	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	F115	F114	F113	F112	F111	F110	F109	F108
Register 99	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	F207	F206	F205	F204	F203	F202	F201	F200
Register 100	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	F215	F214	F213	F212	F211	F210	F209	F208

**IDX[6:0]:** 110 0001b (61h): Register 97

**IDX[6:0]:** 110 0010b (62h): Register 98

**IDX[6:0]:** 110 0011b (63h): Register 99

**IDX[6:0]:** 110 0100b (64h): Register 100

**F[107:100]:** Lower 8 Bits of Coefficient  $a_1$  for First-Stage Notch Filter

**F[115:108]:** Upper 8 Bits of Coefficient  $a_1$  for First-Stage Notch Filter

**F[207:200]:** Lower 8 Bits of Coefficient  $a_2$  for First-Stage Notch Filter

**F[215:208]:** Upper 8 Bits of Coefficient  $a_2$  for First-Stage Notch Filter

Default value: 0000 0000

These bits are used to change the characteristics of the first-stage notch filter. See [Figure 39](#) for details.

## Registers 101–104

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 101	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	S107	S106	S105	S104	S103	S102	S101	S100
Register 102	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	S115	S114	S113	S112	S111	S110	S109	S108
Register 103	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	S207	S206	S205	S204	S203	S202	S201	S200
Register 104	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	S215	S214	S213	S212	S211	S210	S209	S208

**IDX[6:0]:** 110 0101b (65h): Register 101

**IDX[6:0]:** 110 0110b (66h): Register 102

**IDX[6:0]:** 110 0111b (67h): Register 103

**IDX[6:0]:** 110 1000b (68h): Register 104

**S[107:100]:** Lower 8 Bits of Coefficient  $a_1$  for Second-Stage Notch Filter

**S[115:108]:** Upper 8 Bits of Coefficient  $a_1$  for Second-Stage Notch Filter

**S[207:200]:** Lower 8 Bits of Coefficient  $a_2$  for Second-Stage Notch Filter

**S[215:208]:** Upper 8 Bits of Coefficient  $a_2$  for Second-Stage Notch Filter

Default value: 0000 0000

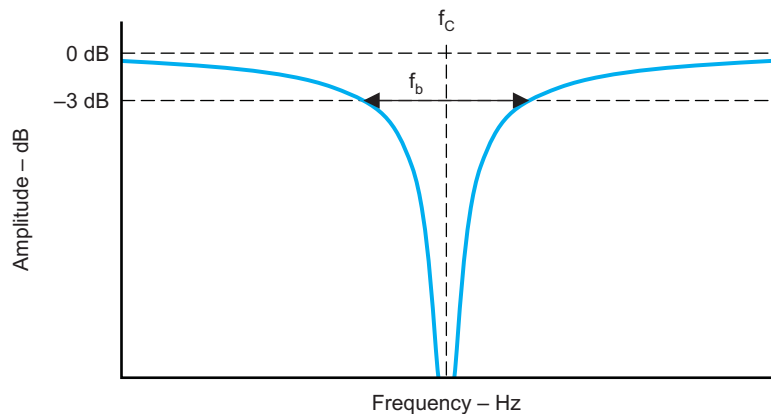
These bits are used to change the characteristics of the second-stage notch filter. See [Figure 39](#) for details.

The PCM3793A/94A provides two notch filters for the digital input to the DAC or the digital output from the ADC. The optional filter characteristics of each filter are programmable. The characteristics are given by calculating the coefficients for three parameters, sampling frequency, center frequency, and bandwidth, as shown in [Figure 39](#). All coefficients must be written as 2s-complement binary data into registers 97, 98, 99, 100, 101, 102, 103, and 104.

$f_s$ : Sampling Frequency [Hz]  
 $f_c$ : Center Frequency [Hz]  
 $f_b$ : Band Width [Hz]

$$a_1 = -(1 + a_2) \cos\left(\frac{2\pi f_c}{f_s}\right) \quad (\text{Equation 1})$$

$$a_2 = \frac{1 - \tan\left(\frac{2\pi f_b/f_s}{2}\right)}{1 + \tan\left(\frac{2\pi f_b/f_s}{2}\right)} \quad (\text{Equation 2})$$



M0058-01

**Figure 39. Parameter Settings for Notch Filter**

The coefficients are calculated using Equation 1 and Equation 2 in [Figure 39](#). An example follows:

$f_s = 16$  kHz,  $f_c = 0.5$  kHz,  $f_b = 0.2$  kHz  
 $a_2 = 0.924390492 \rightarrow$  Decimal to Hex  $\rightarrow$  3B29h  
 $a_1 = -1.887413868 \rightarrow$  Decimal to Hex  $\rightarrow$  8735h  
 $a_2$ : F[215:208] = 3Bh, F[207:200] = 29h  
 $a_1$ : F[115:108] = 87h, F[107:100] = 35h

**Register 125**

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 125	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	PTM1	PTM0	RES4	RES3	RES2	RES1	RES0

**IDX[6:0]:** 111 1101b (7Dh): Register 125

**PTM[1:0]:** Power-Up/Down Time Control

Default value: 00

**Table 14. Power Up/Down Time Control**

V <sub>COM</sub> CAPACITOR [μF]	RES[4:0]	PTM[1:0]	POWER-UP TIME [ms]	POWER-DOWN TIME [ms]	NOTE
10	1 1110	00	450	750	
	1 1100	11	900	1500	
	1 1000	Do not set.	–	–	
	1 0000	Do not set.	–	–	
4.7	1 1110	01	250	400	
	1 1100	00	450	750	Default
	1 1000	11	900	1500	
	1 0000	Do not set.	–	–	
2.2	1 1110	10	100	300	
	1 1100	01	250	400	
	1 1000	00	450	750	
	1 0000	11	900	1500	
1	1 1110	Do not set.	–	–	
	1 1100	10	100	300	
	1 1000	01	250	400	
	1 0000	00	450	750	

**RES[4:0]:** Resistor Value Control

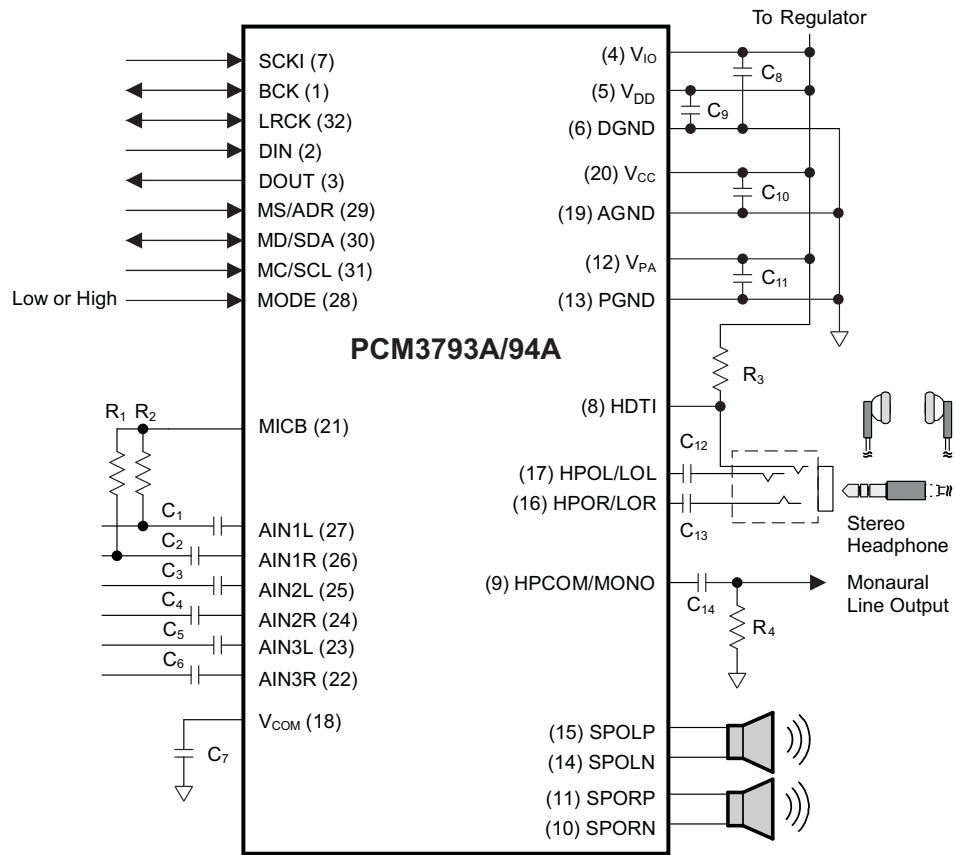
Default value: 1 1100

These bits are used to optimize audible pop noise and ramp-up time for the headphone output when powering the device on/off.

**Table 15. Resistor Value Control**

RES [4:0]	V <sub>COM</sub> RESISTOR VALUE
1 0000	60 kΩ
1 1000	24 kΩ
1 1100	12 kΩ
1 1110	6 kΩ
Others	Reserved

CONNECTION DIAGRAMS

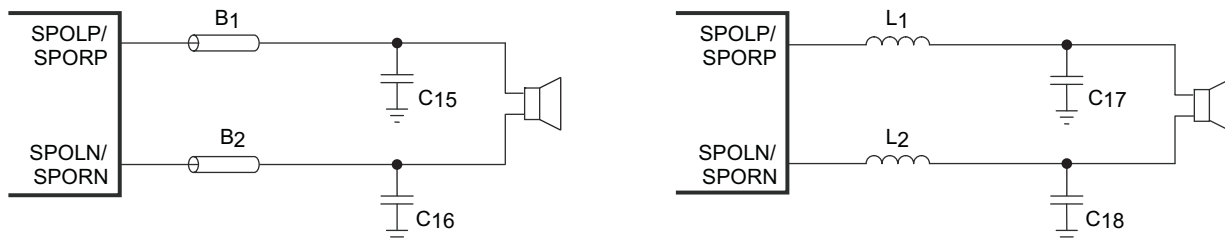


S0220-02

Figure 40. Connection Diagram

Table 16. Recommended External Parts

C <sub>1</sub> –C <sub>6</sub>	1 μF	C <sub>12</sub> , C <sub>13</sub>	10 μF–220 μF
C <sub>7</sub>	4.7 μF	C <sub>14</sub>	1 μF–10 μF
C <sub>8</sub>	0.1 μF	R <sub>1</sub> , R <sub>2</sub>	2.2 kΩ
C <sub>9</sub> , C <sub>10</sub>	1 μF–4.7 μF	R <sub>3</sub>	33 kΩ
C <sub>11</sub>	4.7 μF–10 μF	R <sub>4</sub>	10 kΩ

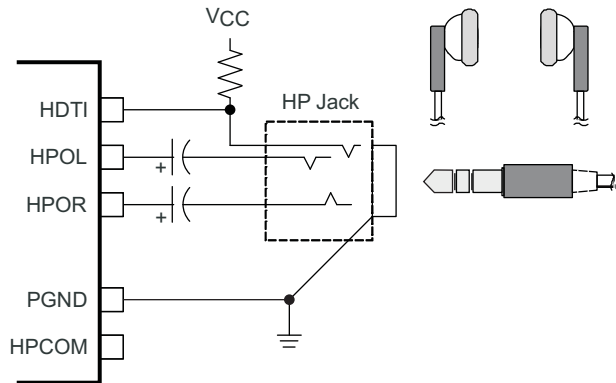


S0221-01

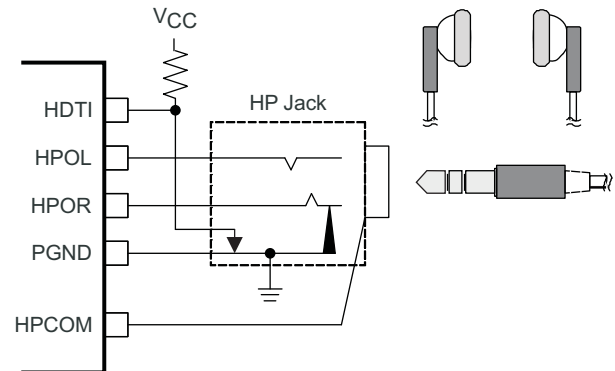
NOTE: C<sub>15</sub>, C<sub>16</sub> = 1 nF; C<sub>17</sub>, C<sub>18</sub> = 1 μF; B<sub>1</sub>, B<sub>2</sub>: NEC/Tokin N2012ZPS121; L<sub>1</sub>, L<sub>2</sub> = 22 μH to 33 μH

Figure 41. Filter Consideration for Speaker Output

Conventional Mode

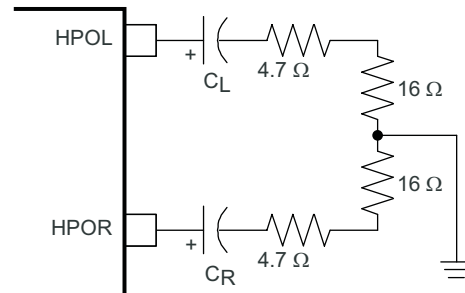
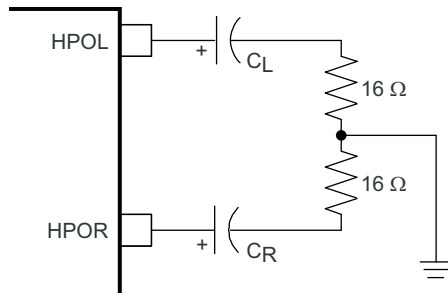


Capless Mode



S0222-01

Figure 42. Connection for Headphone Output and Insertion Detection



$C_L, C_R - \mu F$	$f_C - Hz$
10	995
47	212
100	100
220	45

$C_L, C_R - \mu F$	$f_C - Hz$
10	770
47	163
100	77
220	35

S0223-01

Figure 43. High-Pass Filter for Headphone Output

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PCM3793ARHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCM3793ARHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCM3793ARHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCM3793ARHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCM3794ARHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCM3794ARHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCM3794ARHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCM3794ARHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

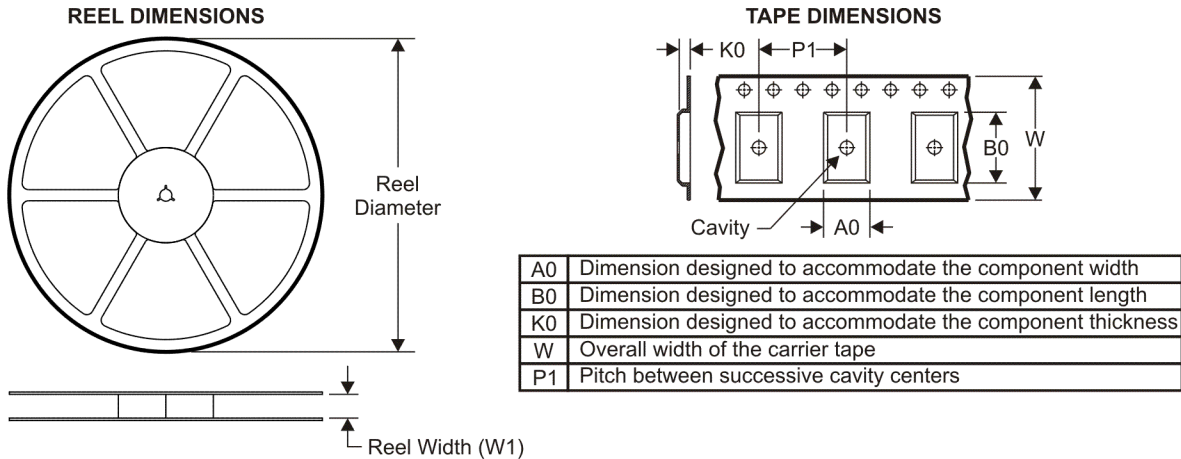
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

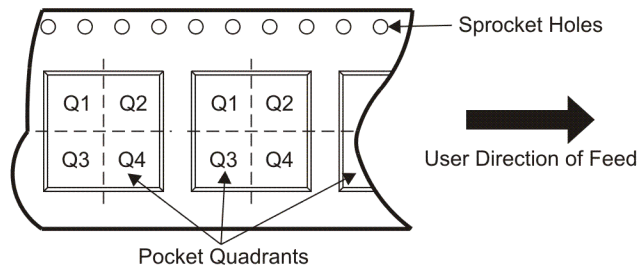
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**TAPE AND REEL INFORMATION**



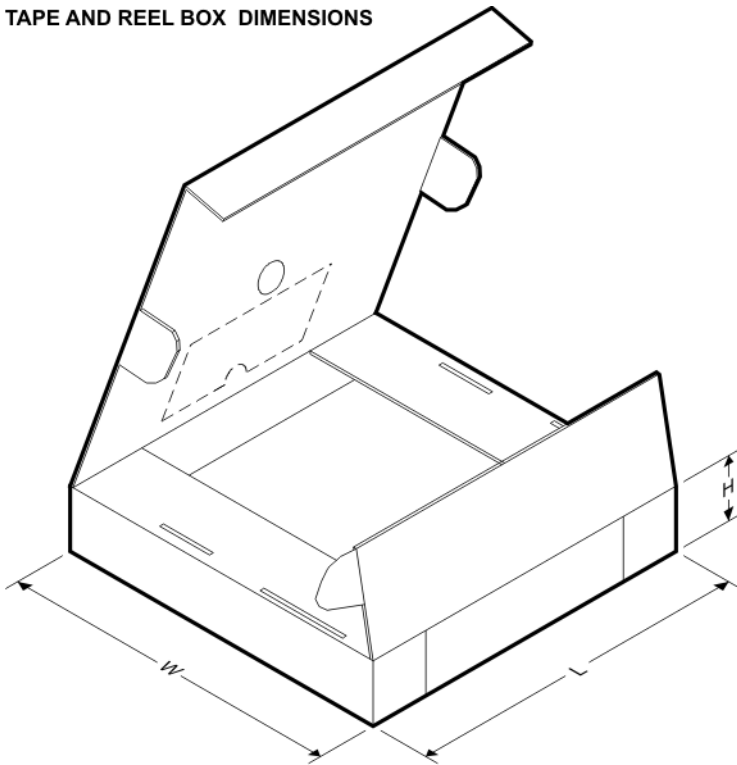
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM3793ARHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
PCM3793ARHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
PCM3794ARHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
PCM3794ARHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM3793ARHBR	QFN	RHB	32	3000	346.0	346.0	29.0
PCM3793ARHBT	QFN	RHB	32	250	190.5	212.7	31.8
PCM3794ARHBR	QFN	RHB	32	3000	346.0	346.0	29.0
PCM3794ARHBT	QFN	RHB	32	250	190.5	212.7	31.8



## THERMAL PAD MECHANICAL DATA

RHB (S-PVQFN-N32)

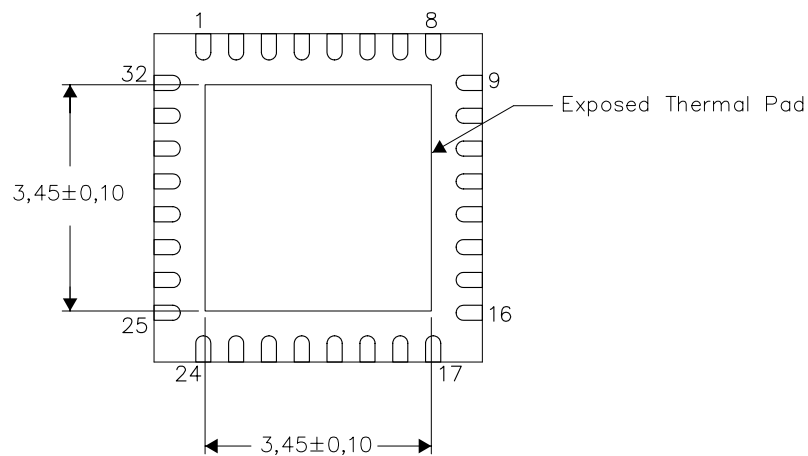
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206356-2/N 03/10



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Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>

## Updates

Always use the most recent firmware for this device. Please visit the TASCAM web site at <http://tascam.com/> to check for the latest firmware.

## Maintenance items

### V1.04 fixes

If recording was conducted until the capacity of the SD card was filled, I/F Error appeared and recording did not complete correctly in some cases. This has been fixed.

### V1.03 fixes

Operation reliability has been improved.

### V1.02 fixes

- The following selection items are added to the INPUT SETTING screen so you can record a low output guitar with the most suitable level.

#### IN A

GUITAR/LINE M: Guitar or Line (Middle sensitivity)

GUITAR/LINE H: Guitar or Line (High sensitivity)

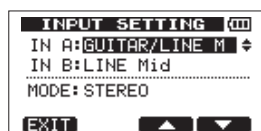
#### IN B

LINE Mid: Line (Middle sensitivity)

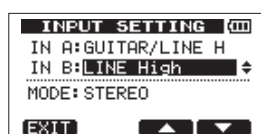
LINE High: Line (High sensitivity)

If you feel the input level is low when you select GUITAR/LINE or LINE as an input source, select GUITAR/LINE M or GUITAR/LINE H for IN A or LINE Mid or LINE High for IN B.

NOTE: If the **OL** indicator of the selected input lights by selecting the above setting, the sensitivity is too high. Turn down the volume of the input source or use the previous selection item.



[Inputs set to GUITAR/LINE M and LINE Mid]



[Inputs set to GUITAR/LINE H and LINE High]

- When using an SD card of 2GB or larger, EXPORT TRACK, EXPORT MASTER and SONG BACKUP are executed about 20% faster.

## V1.01 fixes

A bug that caused the tuner not to function has been fixed.

## Confirmation of firmware version

Confirm the firmware version of your DP-004 before conducting a firmware update.

- Turn the unit's power ON.
- When the Home Screen is open, press the MENU key to open the MENU screen.
- Use the DATA wheel to select INFORMATION item and press the F4 (▶) key to open the INFORMATION screen SONG (1/4) page.
- Use the F3 (PREV) and F4 (NEXT) keys to open the F/W (4/4) page.

If the System Version shown here is the same or newer than the firmware version that you planned to update to, then there is no need to update it.

## Firmware update procedures

### CAUTION

When updating the firmware, be sure that the batteries have sufficient charge or power the unit using a TASCAM PS-P520 AC adaptor (sold separately).

The program has been set so that the update will not be conducted if battery power is insufficient.

- Download the most recent firmware from the TASCAM web site (<http://tascam.com/>). If the file that you have downloaded is compressed in ZIP format, for example, decompress it.
- Turn the unit's power ON and use the included USB cable to connect it with a computer. This unit will be recognized as an external drive (external storage device) by the computer.
- Copy the downloaded firmware (DP004-41.101 for V1.01) to the UTILITY folder on the DP-004.
- After copying has completed, disconnect the unit from the computer following the correct procedures, remove the USB cable and turn the unit power OFF.
- While pressing and holding both the REPEAT and UN/REDO keys, turn the unit power ON.

The unit starts up in update mode, and the update file appears on the screen.



**CAUTION**

- If this screen does not appear, turn the power OFF. Then while pressing and holding both the **REPEAT** and **UN/REDO** keys, turn the unit's power ON again. Continue to press and hold the **REPEAT** and **UN/REDO** keys firmly until this screen appears.
- When firmware has been copied to this unit's *UTILITY* folder from a Mac, in addition to the firmware file itself, another file with "\_" added to the beginning of the firmware name is also shown. Use the file without the "\_" at the beginning of the name.

**NOTE**

- This screen shows a list of the firmware update files inside the *UTILITY* folder of the unit. Also, the screen shows the firmware copied at Step 3 above. No Update File appears if there is no update file in the *UTILITY* folder.
  - The screen shown is an example. The actual display differs.
- 6 Select the firmware (highlight the item) using F1 (▲) and F2 (▼), then press F4 (NEXT). The following screen appears.**



The current version appears on the left and the updated version appears on the right.

**NOTE**

The screen shown is an example. The actual display differs.

- 7 Press the F3 (YES) key to start the update.**
- 8 When the update is complete, the power turns OFF automatically. Turn the power ON again.**
- 9 Follow the "Confirmation of firmware version" instructions above to check that the "System Version" is now the most recent version of the firmware.**

This completes the procedure for updating this unit.

- 10 Connect to a computer with USB and delete the firmware update from the unit's *UTILITY* folder.**

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## Updates

Always use the most recent firmware for this device.  
Please visit the TASCAM web site at <http://www.tascam.com> to check for the latest firmware.

## Maintenance items

### Changes in Version 1.02

- The following selection items are added to the INPUT SETTING screen so you can record a low output guitar with the most suitable level.

#### IN A

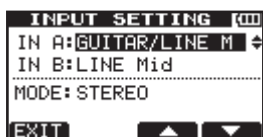
GUITAR/LINE M: Guitar or Line (Middle sensitivity)  
GUITAR/LINE H: Guitar or Line (High sensitivity)

#### IN B

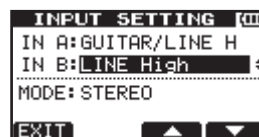
LINE Mid: Line (Middle sensitivity)  
LINE High: Line (High sensitivity)

If you feel the input level is low when you select GUITAR/LINE or LINE as an input source, select GUITAR/LINE M or GUITAR/LINE H for IN A or LINE Mid or LINE High for IN B.

NOTE: If the OL indicator of the selected input lights by selecting the above setting, the sensitivity is too high. Turn down the volume of the input source or use the previous selection item.



[Inputs set to GUITAR/LINE M and LINE Mid]



[Inputs set to GUITAR/LINE H and LINE High]

- When using an SD card of 2GB or larger, EXPORT TRACK, EXPORT MASTER and SONG BACKUP are executed about 20% faster.

### Changes in Version 1.01

A bug that caused the tuner not to function has been fixed.

## Confirmation of firmware version

Confirm the firmware version of your DP-004 before conducting a firmware update.

- 1 Turn the unit's power ON.
- 2 Press the MENU key to open the MENU screen, select "INFORMATION" and press the F4 (▶) key.
- 3 When the INFORMATION screen appears, press F4 (NEXT) three times so the screen changes to F/W (4/4) to confirm the "System Version".

You do not need to update the unit's firmware if the version shown is the same as or newer than the version that you intend to use for the update.

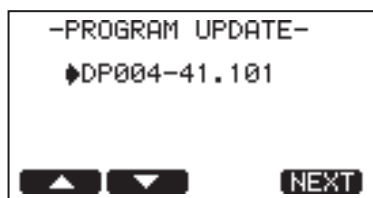
## Firmware update procedures

### CAUTION

When you updated the firmware, make sure that the batteries have enough remaining power or use an optional AC adapter (PS-P520). The program has been set so that the update will not be conducted if battery power is insufficient.

- 1 Download the most recent firmware from the TASCAM web site (<http://www.tascam.com>).
- 2 Turn the unit's power ON and use the included USB cable to connect it with a computer. This unit will be recognized as an external drive (external storage device) by the computer.
- 3 Copy the downloaded firmware to the UTILITY folder on the DP-004.
- 4 After copying has completed, disconnect the unit from the computer following the correct procedures, remove the USB cable and turn the unit power OFF.
- 5 While pressing and holding both the REPEAT and UN/REDO keys, turn the unit power ON.

The unit starts up in update mode, and the update file appears on the screen.



### NOTE

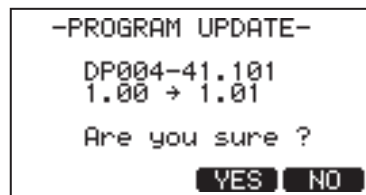
- This screen shows a list of the firmware update files inside the UTILITY folder of the unit. "No Update File" appears if there is no update file in the UTILITY folder.

- The screen shown is an example. The actual display differs.

### CAUTION

If this screen does not appear, turn the power OFF. Then while pressing and holding both the REPEAT and UNIREDO keys, turn the unit's power ON again. Continue to press and hold the REPEAT and UNIREDO keys firmly until this screen appears.

- 6 Select the firmware (highlight the item) using F1 (▲) and F2 (▼), then press F4 (NEXT). The following screen appears.



The current version appears on the left and the updated version appears on the right.

### NOTE

The screen shown is an example. The actual display differs.

- 7 Press the F3 (YES) key to start the update.
- 8 When the update is complete, the power turns OFF automatically. Turn the power ON again.
- 9 Follow the "Confirmation of firmware version" instructions above to check that the "System Version" is now the most recent version of the firmware.

This completes the procedure for updating this unit.

- 10 Connect to a computer with USB and delete the firmware update from the unit's UTILITY folder.

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## Maintenance items

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### Changes in Version 1.01 0041

With this version, the problem that the tuner function did not operate in the previous firmware version has been corrected.

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## Confirmation of firmware version

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Confirm the firmware version of your DP-004 before conducting a firmware update.

- 1 Turn the unit's power ON.**
- 2 Press the MENU key to open the MENU screen, select "INFORMATION" and press the F4 (▶) key.**
- 3 When the INFORMATION screen appears, press F4 (NEXT) three times so the screen changes to F/W (4/4) to confirm the "System Version".**

You do not need to update the unit's firmware if the version shown is the same as or newer than the version that you intend to use for the update.

## Firmware update procedures

### CAUTION

When you updated the firmware, make sure that the batteries have enough remaining power or use an optional AC adapter (PS-P520). The program has been set so that the update will not be conducted if battery power is insufficient.

- 1 **Download the most recent firmware from the TASCAM web site (<http://www.tascam.com>).**
- 2 **Turn the unit's power ON and use the included USB cable to connect it with a computer. This unit will be recognized as an external drive (external storage device) by the computer.**
- 3 **Copy the downloaded firmware to the UTILITY folder on the DP-004.**
- 4 **After copying has completed, disconnect the unit from the computer following the correct procedures, remove the USB cable and turn the unit power OFF.**
- 5 **While pressing and holding both the REPEAT and UN/REDO keys, turn the unit power ON.**

The unit starts up in update mode, and the update file appears on the screen.



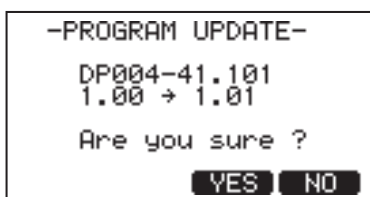
### NOTE

This screen shows a list of the firmware update files inside the UTILITY folder of the unit. "No Update File" appears if there is no update file in the UTILITY folder.

### CAUTION

If this screen does not appear, turn the power OFF. Then while pressing and holding both the REPEAT and UN/REDO keys, turn the unit's power ON again. Continue to press and hold the REPEAT and UN/REDO keys firmly until this screen appears.

- 6 **Select the firmware (highlight the item) using F1 (▲) and F2 (▼), then press F4 (NEXT). The following screen appears.**



The current version appears on the left and the updated version appears on the right.

- 7 **Press the F3 (YES) key to start the update.**
- 8 **When the update is complete, the power turns OFF automatically. Turn the power ON again.**
- 9 **Follow the "Confirmation of firmware version" instructions above to check that the "System Version" is now the most recent version of the firmware.**

This completes the procedure for updating this unit.

- 10 **Connect to a computer with USB and delete the firmware update from the unit's UTILITY folder.**



# TECHNICAL INFORMATION

## TASCAM DR Series, OS Operation check

No. 1305

DATE 17th April. 2013

### OS operation check result

■ Operation check had been done. The result is shown below.

### OS operation check: Mac Mountain Lion/Windows8

April 15th, 2013

	Model name	Mac Mountain Lion	Windows8	Note
1	DP-03	ok	ok	
2	DR-05	ok	ok	
3	DR-07MK2	ok	ok	
4	DR-2d	ok	ok	
5	DR-100MK2	ok	ok	
6	DR-40	ok	ok	
7	DR-08	ok	ok	
8	DR-60D	ok	ok	
9	DR-680	ok	ok	
10	DR-V1HD	ok	ok	Playback sound isn't output because WindowsMediaPlayer doesn't support 24bit sound on movie playback. OK on QuickTime.
11	DP-24	ok	ok	
12	DP-32	ok	ok	
13	DP-004	ok	ok	
14	DP-008	ok	ok	
15	DP-006	ok	ok	
16	DP-008EX	ok	ok	



## TECHNICAL INFORMATION

### TASCAM DP-004 V1.01 Firmware Update

No. **0828**

DATE 2nd December 2008

The firmware V1.01 for DP-004 has been released with bug fix from V1.00. V1.01 on the products with S/N 003001 and higher:

**Bug fixes:**

1. The tuner function did not operate. – fixed–

Visit the [ROM Data Library](#) in the TASCAM Service HP website to download firmware.



## TECHNICAL INFORMATION

### TASCAM DP-004, V1.02 Firmware Update

No. **0910**

DATE 16th March 2009

The firmware V1.02 for DP-004 has been released with a new features and some improvements from V1.01.

V1.02 on DP-0041 has been installed since SN 0060001.

#### **New Feature:**

Some new INPUT settings are added as follows.

IN A: GUITAR/LINE M, Guitar or Line (Middle sensitivity: +6dB)

IN A: GUITAR/LINE H, Guitar or Line (High sensitivity: +12dB)

IN B: LINE Mid, Line (Middle sensitivity: +6dB)

IN B: LINE High, Line (High sensitivity: +12dB)

#### **Improvement:**

1. Some SD card performance has been improved ,  
e.g. Export Track, Export Master, and Song Master are executed about 20% faster,  
when using an SD card of 2GB or larger.

#### **How to Firmware Update**

Refer to Service Manual “3.Updating Firmware” page 8.

Visit the [ROM Data Library](#) in the TASCAM Service HP website to download firmware and refer to DP-004 Release Note for further details..



## TECHNICAL INFORMATION

### TASCAM DP-004, V1.03 Firmware Update

No. **0925**

DATE 17th July 2009

The firmware V1.03 for DP-004 has been released with some improvement from V1.02. V1.03 on DP-004 has been installed since SN 0090001.

#### **Improvement and Bug fixes:**

1. It might power off automatically some time later when it is powered on while it is connected to PC with USB cable. – fixed –
2. The Input signal did not become to REC source signal after the Input source is changed from OFF to ON (e.g. selecting INT.MIC or LINE, etc) while Track REC is ON. – fixed-

#### **How to Firmware Update**

Refer to DP-004 Service Manual “3.Updating Firmware ” page 8.

Visit the [ROM Data Library](#) in the TASCAM Service HP website to download firmware.



## TECHNICAL INFORMATION

### TASCAM DP-004 V1.04 Firmware Update

No. 1111

DATE 20th Apr. 2011

The firmware V1.04 for DP-004 has been released with some improvement from V1.03.

**Improvement:**

1. If recording was conducted until the capacity of the SD card was filled, I/F Error appeared and recording did not complete correctly in some cases. –fixed–

**How to Firmware Update:**

Refer to DP-004 Release Note “Firmware update procedures” for details of it.  
The firmware file for V1.04 is “dp004-46.104” (303KB)

Visit the [ROM Data Library](#) in the TASCAM Service HP website to download firmware.