

TASCAM[®]
TEAC PROFESSIONAL

SERVICE MANUAL

DR-07

Portable Digital Recorder

CONTENTS

1. Specifications	2
2. Test Mode	4
3. Updating of Firmware	8
4. Messages Explained	11
5. Block Diagram	16
6. Level Diagram	17
7. Exploded Views and Parts List	18
8. PC Boards and Parts List	20
9. Included Accessories	26

目次

1. 仕様	2
2. テストモード	4
3. ファームウェアアップデート方法	8
4. メッセージ一覧	11
5. ブロックダイアグラム	16
6. レベルダイアグラム	17
7. 分解図とパーツリスト	18
8. 基板図とパーツリスト	20
9. 付属品	26

1. Specifications

仕様

Audio Input and Output

- MIC IN input

Jack	3.5-mm stereo phone (with plug-in power)
Input impedance	30 k Ω
Nominal input level	-64 dBV (GAIN set to HIGH) -48 dBV (GAIN set to MID) -32 dBV (GAIN set to LOW)
Maximum input level	-48 dBV (GAIN set to HIGH) -32 dBV (GAIN set to MID) -16 dBV (GAIN set to LOW)
- LINE IN input

Jack	3.5-mm phone (stereo)
Input impedance	23 k Ω
Nominal input level	-10 dBV
Maximum input level	+6 dBV
- Ω /LINE OUT output

Jack	3.5-mm phone (stereo)
Nominal line output	-14 dBV
Maximum line output	+2 dBV
Maximum headphones output	15 mW + 15 mW (with 32 Ω impedance headphones)

Audio performance

- Frequency response (LINE IN \rightarrow Ω /LINE OUT)
20 Hz–20 kHz, +1/-3 dB
- Distortion (LINE IN \rightarrow Ω /LINE OUT)
0.015 % or less (at 1kHz, +6dBV input)
- S/N ratio (LINE IN \rightarrow Ω /LINE OUT)
87 dB or more

Other specifications

- Audio file compatibility

MP3 files	32–320 kbps 44.1/48 kHz sampling frequency VBR (playback only) ID3 tag support up to Ver 2.4
WAV files	44.1/48 kHz sampling frequency 16/24-bit rate
Recording medium	SD card (64 MB–2 GB) or SD HC card (4–32 GB)
File system	FAT16/32
- Physical

Battery life	About 7.5 hours when recording About 8.5 hours when playing (using alkaline batteries, no back light, MP3 128 kbps, varies with operating conditions)
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オーディオ入出力定格

- MIC IN入力

端子：	3.5mmミニホンジャック (ステレオ) (プラグインパワー対応)
入カインピーダンス：	30K Ω
基準入力レベル：	-64dBV(GAIN HIGH時) -48dBV(GAIN MID時) -32dBV(GAIN LOW時)
最大入力レベル：	-48dBV(GAIN HIGH時) -32dBV(GAIN MID時) -16dBV(GAIN LOW時)
- LINE IN入力

端子：	3.5mmミニホンジャック (ステレオ)
入カインピーダンス：	23K Ω
基準入力レベル：	-10dBV
最大入力レベル：	+6dBV
- Ω /LINE OUT 出力

端子：	3.5mmミニホンジャック (ステレオ)
基準出力レベル：	-14dBV(ライン接続時)
最大出力レベル：	+2dBV(ライン接続時)
ヘッドホン最大出力：	15mW + 15mW (32 Ω ヘッドホン接続時)

オーディオ性能

- 周波数特性 (LINE IN \rightarrow Ω /LINE OUT) :
20Hz ~ 20kHz, + 1/- 3dB
- 歪率 (LINE IN \rightarrow Ω /LINE OUT) :
0.015%以下
- S/N 比 (LINE IN \rightarrow Ω /LINE OUT) :
87dB 以上

一般

- 対応オーディオファイル：

MP3 ファイル：	32kbps ~ 320kbps、サンプリング周波数44.1kHz / 48kHz、VBR 再生対応、Ver ~ 2.4のID3TAG をサポート
WAV ファイル：	サンプリング周波数44.1kHz / 48kHz、ビット長：16 / 24 ビット
記録媒体：	SDカード (64Mバイト~2Gバイト) およびSDHCカード (4Gバイト~32Gバイト)
ファイルシステム：	FAT16/32
- 電池持続時間 (連続再生時) :

約7.5時間 (JEITA録音時間)
約8.5時間 (JEITA音楽再生時間)
(アルカリ乾電池使用、バックライト消灯、MP3 128kbps時。使用状況により変動することがあります。)

- Operating temperature 5 to 35°C
- Power consumption 0.7 W (during MP3 playback)
- Dimensions 55 (W) x 137 (H) x 27 (D) (mm)
(not including protrusions) 2.2 (W) x 5.4 (H) x 1.1 (D) (inches)
- Weight 130 g (without batteries)

Accessories available for purchase

- AC adapter PS-P520

Computer requirements

- Windows: Pentium 300 MHz or faster
128 MB or more memory
USB port (USB 2.0 recommended)
- Macintosh: Power PC, iMac, G3, G4 266 MHz
or faster 64 MB or more memory
USB port (USB 2.0 recommended)
- Recommended USB host controller
Intel chipset
- Supported OS
Windows: Windows 2000 SP4 or later,
Windows XP and Windows Vista
Macintosh: Mac OS X 10.2 or later

- 使用温度範囲： 5～35°C
- 消費電力： 0.7W (MP3再生時)
- 外形寸法： 55 (幅) × 137 (高さ) × 27 (奥行)
mm (突起部含まず)
- 質量： 130g (電池を含まず)

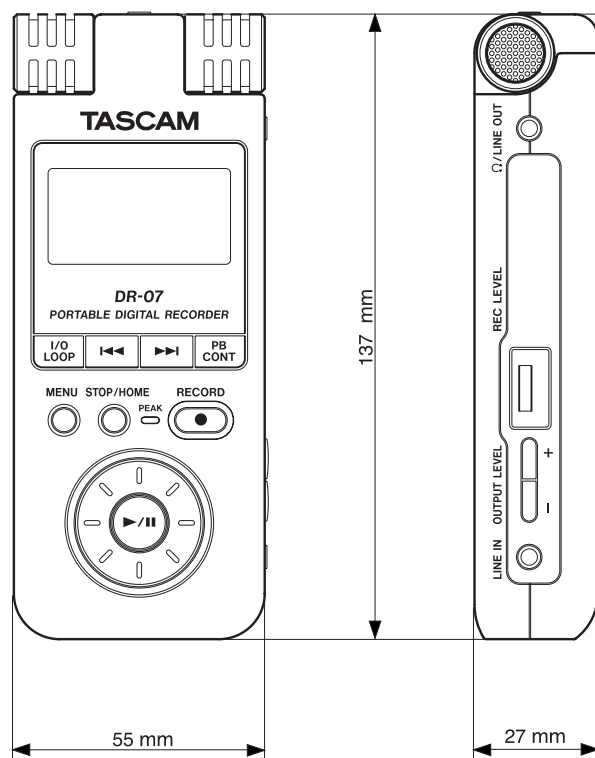
別売アクセサリ

- AC アダプター PS-P520

接続するパソコンの条件

- Windows マシン： Pentium 300MHz 以上
128MB 以上のMemory
USB ポート(推奨： USB2.0)
- Macintosh マシン： Power PC、iMac、G3、G4
266MHz 以上
64MB 以上のMemory
USB ポート(推奨： USB2.0)
- 推奨USB ホストコントローラー：
Intel 製チップセット
- サポートOS
Windows： Windows 2000 SP4以上、
Windows XP、Windows Vista
Macintosh： Mac OS 10.2 以上

Dimensional drawings (寸法図)



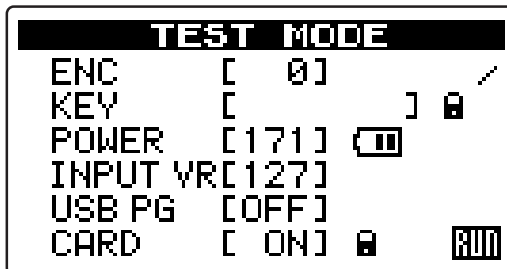
2. Test Mode

テストモード

1. How to enter test mode

While holding down the PLAY+MENU+STOP keys, switch the power on.

The LCD shows the following message: The LCD backlight is lit.



1. テストモードの起動方法

「PLAY+MENU+STOP」キーを押しながら電源を投入する。



LCDに下記を表示する。バックライトは点灯。

2. Displays explained

DATA encoder (0-999)

Shows the name of a key pressed

Power supply voltage (255 steps)

"  " shown when powered on battery; "  " shown when connected to an AC outlet.

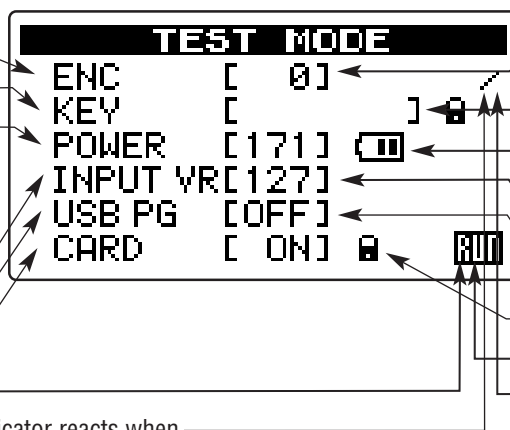
Read in input volume value

USB connection

Card detection

Operation indicator

Event acceptance indicator. This indicator reacts when keys are operated for example



2. 画面の説明

3. Checking LEDs

REC LED: turns on when the REC key is pressed.

PEAK LED: turns on when the STOP key is pressed.

They turn off when the keys are held pressed for a certain time.

3. LED確認

REC LED : RECキーで点灯する。

PEAK LED : STOPキーで点灯する。

全て、キーを長押しすると点滅する。

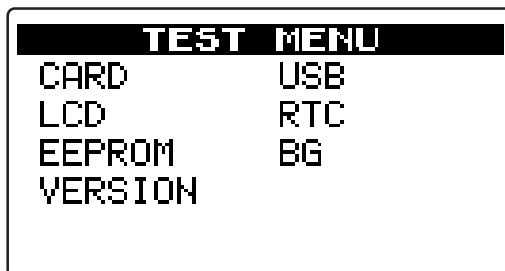
4. Menu

Pressing the MENU key reveals the following menu.

Options are selectable using the encoder.

ENTER (▶/||) : mode selection

MENU: back to the TOP screen



エンコーダ操作で項目の移動。

ENTER (▶/||) : 項目の選択。

MENU : TOP画面へ。

4. MENU

MENUキーを押すと下記メニューを表示する。

1) CARD

Selecting "CARD" and pressing the ENTER(▶/■) key gets you to the following menu:

```

CARD
[ENTER] Identify
[FWD  ] Read One
[REC  ] Format

```

1) CARD

"CARD" を選択してENTER(▶/■)キーを押すと下記メニューを表示する。

Identify: Read in data from the card.

Pressing the ENTER(▶/■) key indicates the following information:

Manufacturer ID
 OID : OEM/Application ID
 Product name
 Product revision
 Product serial number
 Manufacturing date
 Raw Size

```

CARD
MID  : 02  OID : 544D
PRN  : SD02G
PRV  : 32
PSN  : AD2B8D21
MDT  : 088
SIZE : 2013265920

```

Manufacturer ID
 OID : OEM/Application ID
 Product name
 Product revision
 Product serial number
 Manufacturing date
 Raw Size

Identify : カードから情報の読み込み

ENTER(▶/■)キーを押すと下記の情報を表示する。

Read One: Read in data from the card per sector

At each press of the FWD(▶▶) key, data is read in from the card per sector.

```

CARD
[ENTER] Identify
[FWD  ] Read One
[REC  ] Format
  Read [ 1]Sector..
    Read OK

```

Read One : カードから1セクタ読み込み

FWD(▶▶)キーを押すと、押すたびにカードから1セクター毎のデータの読み込みを行なう。

Format: Card formatting

At a press of the REC key, the following screen appears:

```

CARD
[ENTER] Identify
[FWD  ] Read One
[REC  ] Format
  Are You Sure ?

```

Format : カードフォーマット

RECキーを押すと下記画面を表示する。

If ENTER(▶/⏏) key is pressed at this screen, the card starts being formatted. Upon completion of the formatting process, "Complete" is displayed. Pressing MENU brings you back to the top screen.

ここでENTER(▶/⏏)キーを押すとFormatを実行し、実行後、"Complete"を表示して終了する。MENUでTop画面へ戻る。

2) USB Check

Select "USB" and press the ENTER(▶/⏏) key. Each time the ENTER(▶/⏏) key is pressed, the indication alternates between ON and OFF.

2) USB Check

"USB"を選択してENTER(▶/⏏)キーを押す。ENTER(▶/⏏)キーを押すたびにON/OFFを繰り返す。



3) LCD Check

Select "LCD" and press ENTER(▶/⏏) key and the following are displayed:

3) LCD Check

"LCD"を選択してENTER(▶/⏏)キーを押すと下記画面を表示する。

The screenshot shows a menu titled "LCD Check" with the following settings and labels:

- VOL : 44**: Contrast adjustment (IO: +; LOP: -) adjustment. Labels: "コントラスト調整 IO: + LOOP: -" and "コントラスト調整傾き FWD(▶▶): + REW(◀◀): -".
- Ratio : 4**: Contrast adjustment slope.
- ABCDEFGH1234567 35**: Characters for after-image check. Label: "残像確認用キャラクタ".
- STOP/HOME key : Reverse**: Label: "STOP/HOME : 反転".

4) RTC Check

Select "RTC" and press ENTER(▶/⏏) key and the following are displayed: Real-time clock indication Date and time indication only

4) RTC Check

"RTC"を選択してENTER(▶/⏏)キーを押すと下記画面を表示する。リアルタイムクロック表示 日時の表示のみ

The screenshot shows a menu titled "RTC Check" with the following information and labels:

- TIME: 21 12 50**: Time. Label: "時刻".
- DATE: 00 01 01**: Date (yy/mm/dd). Label: "日付 (年月日)".
- 0001**: The year of 2000 is indicated as "00". Label: "年は2000年を00と表示".

5) EEPROM Check

Select "**EEPROM**" and press ENTER(▶/■) key and the following are displayed:

Read in from the ROM

"Reading..." is displayed at a press of the ENTER(▶/■) key.

Writing all zeros to the ROM

The writing process starts at a press of the ENTER(▶/■) key in response to "Are you sure?"

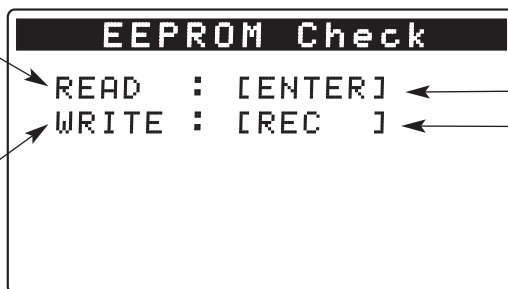
To cancel the process, press the MENU key.

If errors occur during either the read or the write, the following are displayed:

Timeout Err: No response from the EEPROM

Error: Errors at data send/receive time

Verify Err: Errors in verification during the write process



ROMの読み込み実行。

ENTER(▶/■)キーで「Reading...」を表示。

ROMのオールゼロ書き込み。

「Are you sure?」後に ENTER(▶/■)キーで書き込み。MENUでキャンセル。

5) EEPROM Check

"EEPROM"を選択してENTER(▶/■)キーを押すと下記画面を表示する。

READ/WRITE共にエラーの場合には下記を表示する。

Timeout Err : EEPROMの応答なし

Error : データ送信/受信時のエラー

Verify Err : Write時のベリファイエラー

6) BG

Select "**BG**" and press ENTER(▶/■) key:

Background samples

FWD(▶▶): Previous; REW(◀◀): Next

6) BG

"BG"を選択してENTER(▶/■)キーを押す。

背景サンプル

FWD(▶▶): 後 REW(◀◀): 前

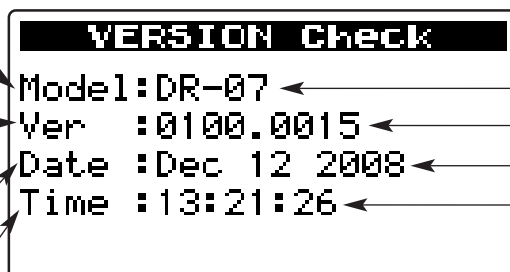
7) VERSION Check

Select "**VERSION**" and press ENTER(▶/■) key and the following are displayed:

Model Name

Version of the system firmware. The last 4 digits indicate a build number on which the system firmware was built.

which the system firmware was built.



モデル名

システムファームのバージョン。後半の4桁はビルド番号

ファームビルド日付

ファームビルド時刻

7) VERSION Check

"VERSION"を選択してENTER(▶/■)キーを押すと下記画面を表示する。

3. Updating of Firmware

ファームウェアアップデート方法

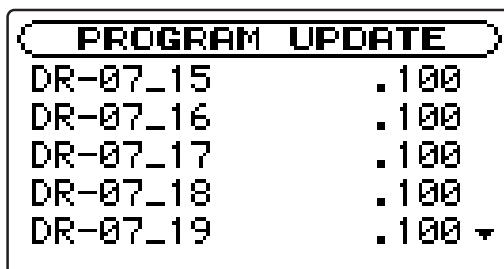
1. Preparations

- 1) Make the connection between this unit and the PC using a USB cable.
- 2) Place the update file in the UTILITY folder in the unit.
- 3) Perform the USB device "remove" action on the PC, and then switch off the power to the unit.

2. START-UP

While holding down the PLAY and MENU keys, switch the power on.

The LCD looks like this:



Update files are shown with extensions.

The USB connection can be made at this point.

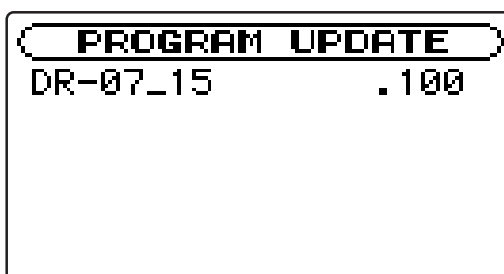
When USB connected, the normal USB screen appears.

When unplugging the USB cable, the unit shifts to the normal start-up.

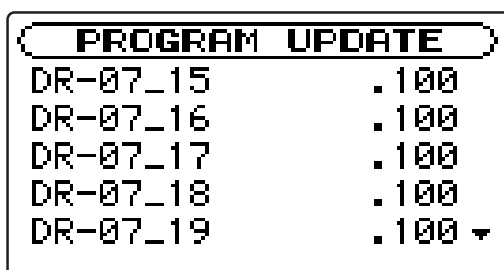
That is to say, the update screen reappears when unplugging the USB cable while holding down the PLAY and MENU keys.

3. Displays explained

- 1) When only a single file is available:



- 2) When multiple files are available:



When there are 6 or more files, use the dial to move the cursor over them.

1. 準備

- 1) 本体とPCをUSBケーブルで接続する。
- 2) アップデートファイルを本体の「UTILITY」フォルダに置く。
- 3) PCでUSBデバイスの「取り外し」を行い、本体の電源を落とす。

2. 起動

PLAY+MENUキーを押しながら電源を投入する。

LCDに下記を表示する。

アップデートファイルを拡張子付きで表示する。

この時点でUSB接続することが可能です。

接続すると通常と同じUSB画面となり、USBケーブルを抜くと通常起動する。

従って、PLAY+MENUキーを押しながらUSBケーブルを抜けば再びアップデート画面となる。

3. 画面の説明

- 1) ファイルが一つの場合

- 2) ファイルが複数の場合

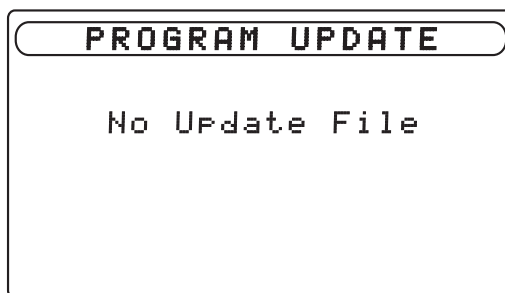
5つ以上の場合はダイヤルでカーソル移動する。

3) When no update file is available:

Nothing can be done.

3) ファイルが無い場合

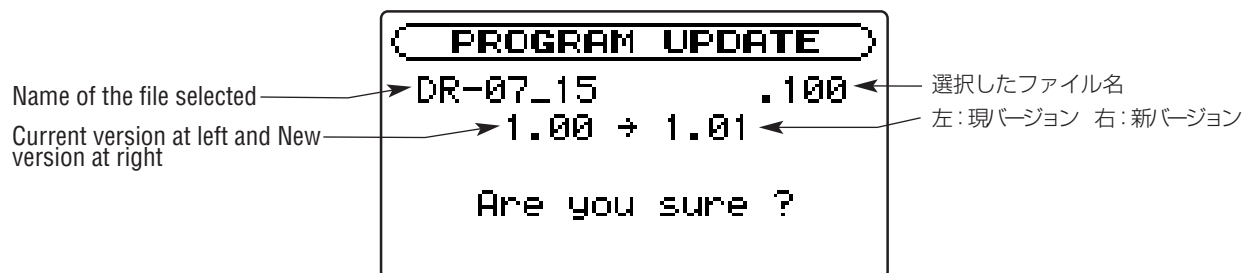
何も操作できません。

**4. File confirmation**

Select a target file and press the ENTER(▶/■) key .

4. ファイルの確認

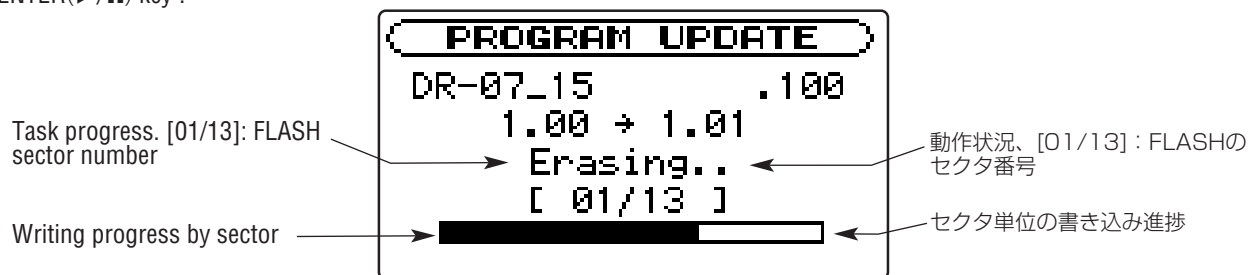
対象のファイルを選択し、ENTER(▶/■)キーを押す。

**5. Getting update started**

The update process starts when pressing the ENTER(▶/■) key .

5. アップデート実行

ENTER(▶/■)キーを押すとアップデートを実行する。



Pressing the MENU key brings you back to the file selection screen, as at step 2, without performing the update.

アップデートを実行せず、2.のファイル選択画面へ戻るにはMENUキーを押す。

6. Completion**6. 完了**

Upon completion of the update process, "Complete" is displayed and the unit automatically switched off.

アップデートが完了すると "Complete" と表示して自動的に電源が切れる。

7. Error messages

1) If an error occurs when selecting a file, the following messages appear:

Messages(メッセージ)	Meaning (内容)
Product	The product ID of the file does not match (the file may be for other products).
	ファイルのプロダクトIDが一致しない (別製品のファイルの可能性はある)。
Old Version	The file version is older than the current one.
	現バージョンよりもファイルのバージョンが古い。
Checksum	The checksum does not match.
	ファイルのチェックサムが一致しない。
Update File	Error in file reading.
	ファイル読み込みエラー。

7.エラー

1) ファイル選択時にエラーが発生した場合のメッセージ

2) If an error occurs in the data rewriting process, the following messages appear:

2) 書き換え時にエラーが発生した場合のメッセージ

Messages(メッセージ)	Meaning (内容)
Flash Erase	Error in erasing.
	消去エラー
Flash Blank	Blank error as a result of data erasure.
	消去後のブランクエラー
Flash Write	Error in writing.
	書き込みエラー
Flash Verify	Error in verification after data has been written.
	書き込み後のバリファイエラー

4. Messages Explained

メッセージ一覧

The following is a list of the popup messages that might appear on the DR-07 under certain conditions.

Refer to this list if one of these popup messages appears and you want to check the meaning or determine a proper response.

以下にポップアップメッセージの一覧表を示します。

DR-07では状況に応じてポップアップメッセージが表示されますが、それぞれのメッセージの内容を知りたいとき、および対処方法を知りたいときにこの表をご覧ください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
File Name ERR	The length of the file name is longer than 200 characters when the Divide is used.
	「ファイル名が不正です。」 Divideでファイル名の長さが200文字を超えた場合に表示されます。
Dup File Name	The same file name already exists when a new file is created when the Divide is used.
	「同じフォルダ内で、そのファイル名は既に使用されています。」 Divide時に作成されるファイル名と同じファイルが既に存在する場合に表示されます。
File not found	The audio file cannot be found or is corrupted. Check the file (using a computer).
	「ファイルが見つかりません。」 対象の音楽ファイルが見つからないかファイル内容が壊れている場合に表示されます。 対象の音楽ファイルを確認してください。
Non-Supported	The audio file is not a supported format. Check the file format (using a computer).
	「ファイルの形式がサポート対象外です。」 対象の音楽ファイルの形式が対象外である場合に表示されます。 対象ファイルのエンコード形式を確認してください。
Battery Empty	The batteries are almost out of power. Replace the batteries or use an AC adapter (sold separately).
	「電池が空です。」 バッテリーが殆ど空の状態の時に表示されます。 ACアダプタを接続するか、または電池を交換してご使用下さい。
I/O Too Short	When using the I/O LOOP key, the IN and OUT points are too close together to start loop playback. Set the interval to at least one second. Reset the IN and OUT points and try again.
	「IN ポイントとOUTポイントが近すぎます。」 I/O LOOPキーでループ再生に入ろうとするとINポイントとOUTポイントが非常に近すぎると表示されます。一秒以上の間隔を空けて下さい。 INポイントとOUTポイントを再度設定し直して見てください。
File Not Found PLAYLIST	The file in the Playlist cannot be found. Please confirm that the file is still in the Music Folder.
	「プレイリスト上のファイルが見つかりません。」 プレイリストに登録されているファイルが見つかりません。 MUSICフォルダに対象のファイルがあるか確認してください。
No PLAYLIST	No files are in the Play list. This appears when the PLAY MODE is set to PLAYLIST, but no files have been added to the Playlist. Add a file to the Playlist.
	「プレイリストがありません。」 プレイモードを「PLAYLIST」にした場合、プレイリストにファイルが一つも登録されていない場合に表示されます。プレイリストへファイルを登録してください。
PLAYLIST FULL	You cannot add more than 99 tracks to the Playlist. Erase an unneeded file from the Playlist and then add the new file.
	「プレイリストが一杯です。」 プレイリストに99曲登録された状態で新たにファイルを登録しようとしたとき表示されます。 プレイリストから不要なファイルを削除してください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
MBR Error Init CARD	There is a problem with the Master Boot Record. The card is not formatted properly or the formatting is broken. When “Are you Sure?” appears, press the ENTER(▶/■) key to format the entire card in FAT format. CAUTION Execution of FAT formatting erases all data currently on the card.
	「カードの初期化が不正です。」 カードのフォーマットが異常、もしくは壊れています。 “Are you Sure?” 表示の状態ですENTER(▶/■)キーを押すことでカード全域がFATでフォーマットされます。 注意 : FATフォーマットが実行されるとカード内のデータはすべて消去されます。
Format Error Format CARD	The FAT formatting of the card is abnormal or broken. This message also appears if you FAT formatted the card using a computer connected by USB (or by card reader). This message also appears when a new card is inserted in the unit. Always use the DR-07 to conduct FAT formatting of cards to be used with it. When “Are you Sure?” appears, press ENTER(▶/■) key to FAT format the entire card. CAUTION Execution of FAT formatting erases all data currently on the card.
	「カードのフォーマットが不正です。」 カードのFATフォーマットが異常、もしくは壊れています。 このメッセージはUSB接続したパソコンからFATでフォーマットした場合や新規購入のカードを挿入した場合でも表示されます。FATフォーマットは必ず製品本体で行う必要があります。 “Are you Sure?” 表示の状態ですENTER(▶/■)キーを押すことでカード全域がFATでフォーマットされます。 注意 : FATフォーマットが実行されるとフラッシュメモリ内のデータはすべて消去されます。
File Not Found Make Sys File	The system file is missing. This unit requires a system file for operation. When “Are you Sure?” appears, press ENTER(▶/■) key to automatically create a system file.
	「システムファイルがありません。」 本機を使用するために必要なシステムファイルが無い場合に表示されます。 “Are you Sure?” 表示の状態ですENTER(▶/■)キーを押すことでシステムファイルが自動的に作られます。
Invalid SysFile Make Sys File	The system file is invalid. The system file required to operate this unit has become abnormal or broken. When “Are you Sure?” appears, press the ENTER(▶/■) key to automatically create a valid system file.
	「システムファイルが不正です。」 本機を使用するために必要なシステムファイルが異常、もしくは壊れています。 “Are you Sure?” 表示の状態ですENTER(▶/■)キーを押すことで現在のファイルは破棄され、正常なシステムファイルで自動的に上書きされます。
Invalid Card Change Card	This appears when there is some type of error with the card.
	カードが何らかのエラーとなってしまう場合に表示されます。
Protected Card Change Card	This appears when the card in the unit during startup is a protected card without the necessary Music Folder and other folders and files.
	MUSICフォルダなど所定のフォルダ、ファイルが無い状態でカードにプロテクトが掛かっていると起動時に表示します。
Write Timeout	Writing to the card timed out. Backup files on the card to your computer, and format the card using the DR-07.
	カードへの書き込みが間に合いませんでした。 ファイルをPCへバックアップの上、フォーマットを実行してください。
Card Full	Erase unnecessary files or move them to your computer to make open space.
	カードの残容量がありません。 不要なファイルを削除するかPCへ移動してください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
Layer too Deep	A folder cannot be created below this level.
	これ以上深い階層のフォルダを作成する事はできません。
Can't Divide	The position set for division is not suitable (song beginning or end).
	Divide実行時に分割位置が適切ではありません。(曲の先頭、曲の最後)
Max File Size	The file is larger than the designated size or the recording time exceeds 24 hours.
	ファイルのサイズが指定のサイズを超えました。 あるいは録音時間が24時間を超えました。
File Full	The total number of folders and files is already 999. Erase unnecessary files or move them to your computer.
	フォルダとファイルの総数がすでに999個です。 不要なファイルを削除するかPCへ移動してください。
Card Error	There was some sort of error with the card. Turn off the power and replace the card with a working card.
	カードによる何かしらのエラー 一旦電源を切り、カードを正常なものと差し替える必要があります。
Current File MP3	You cannot divide a recording that has been made as an MP3 file.
	MP3ファイルの分割はできません。
File Protected	The file is protected. You cannot delete a "read only" file.
	リードオンリーファイルの為、削除できません。
No Card	Can't record because there is no card in the slot.
	カードが無いため、録音できません。
No MUSIC File	Can't divide because no music file exists.
	再生ファイルが無いため、DIVIDEを実行できません。

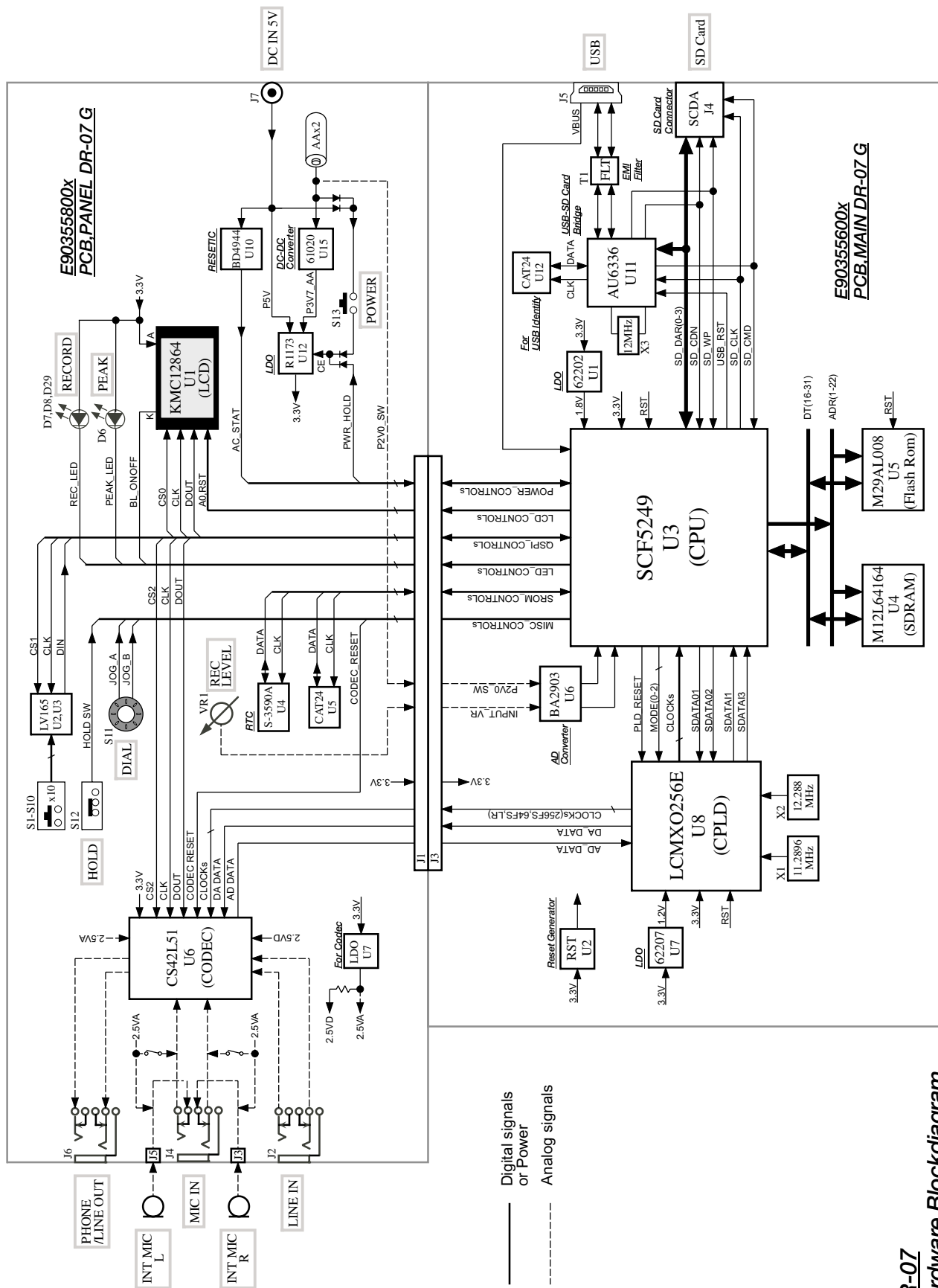
System Error Messages (システムエラーメッセージ)

Messages(メッセージ)	Description(説明)	Cause(原因)
Not Continued	Playback not stopped, or card unmounted error.	The card or firmware may be defective.
	再生系の停止が未完了、あるいはカードのアンマウント時のエラー	カード不良もしくはF/Wの不具合の可能性有り。
File Error	File system error or recording/playback circuitry error.	The card or firmware may be defective.
	ファイルシステム上でエラー、あるいは録再系でのエラー	カード不良もしくはF/Wの不具合の可能性有り。
Can't Save Data	Write in the EEPROM or system file failed during shutdown or switching to USB (this error occurs for example when the card is write protected).	Check that the card is inserted and it is not protected. The card may be defective. If the error occurs with the EEPROM, the PCB may be defective.
	シャットダウン時やUSB切り替え時にEEPROMあるいはシステムファイルへの書き込みが出来なかった。(カードがライトプロテクトに設定されているなどで。)	カードの挿入、カードプロテクトを確認。 カード不良の可能性有り。 EEPROMの場合はPCB不良の可能性有り。
Player Error	Internal error in recording/playback.	The firmware may be defective.
	記録再生の内部的エラー	F/Wの不具合の可能性有り。
Device Error	Device Error 2: RTC initialization error.	The PCB may be defective.
	Device Error 2 : RTC初期化エラー	PCB不良の可能性有り。
Writing Failed	File creation error at the start of recording or file close error at the end of recording.	Confirm whether the error occurred during start or end of recording. The card may be defective.
	記録開始時のファイル作成エラー、あるいは記録終了時のファイルクローズエラー	録音開始時か記録終了時かの確認。 カード不良の可能性有り。
Sys Rom Err	EEPROM read error	The PCB may be defective.
	EEPROMの読み込みエラー	PCB不良の可能性有り。
System Err 50	Other fatal error	The firmware may be defective.
	その他の致命的エラー	F/Wの不具合の可能性有り。
System Error 1	CPU access error	The firmware may be defective.
	CPUのアクセスエラー	F/Wの不具合の可能性有り。
System Error 2	CPU address error	The firmware may be defective.
	CPUのアドレスエラー	F/Wの不具合の可能性有り。
System Error 3	CPU instruction error	The firmware may be defective.
	CPUのインストラクションエラー	F/Wの不具合の可能性有り。

Messages(メッセージ)	Description(説明)	Cause(原因)
System Error 4	CPU zero division error	The firmware may be defective.
	CPUのゼロ除算エラー	F/Wの不具合の可能性有り。
System Error 5	CPU Privilege Violation error	The firmware may be defective.
	CPUのPrivilege Violationエラー	F/Wの不具合の可能性有り。
System Error 6	CPU Unimplemented line-a opcode error	The firmware may be defective.
	CPUのUnimplemented line-a opcodeエラー	F/Wの不具合の可能性有り。
System Error 7	CPU Unimplemented line-f opcode error	The firmware may be defective.
	CPUのUnimplemented line-f opcodeエラー	F/Wの不具合の可能性有り。
System Error 8	CPU format error	The firmware may be defective.
	CPUのフォーマットエラー	F/Wの不具合の可能性有り。
System Error 9	CPU Uninitialized Interrupt error	The firmware may be defective.
	CPUのUninitialized Interruptエラー	F/Wの不具合の可能性有り。

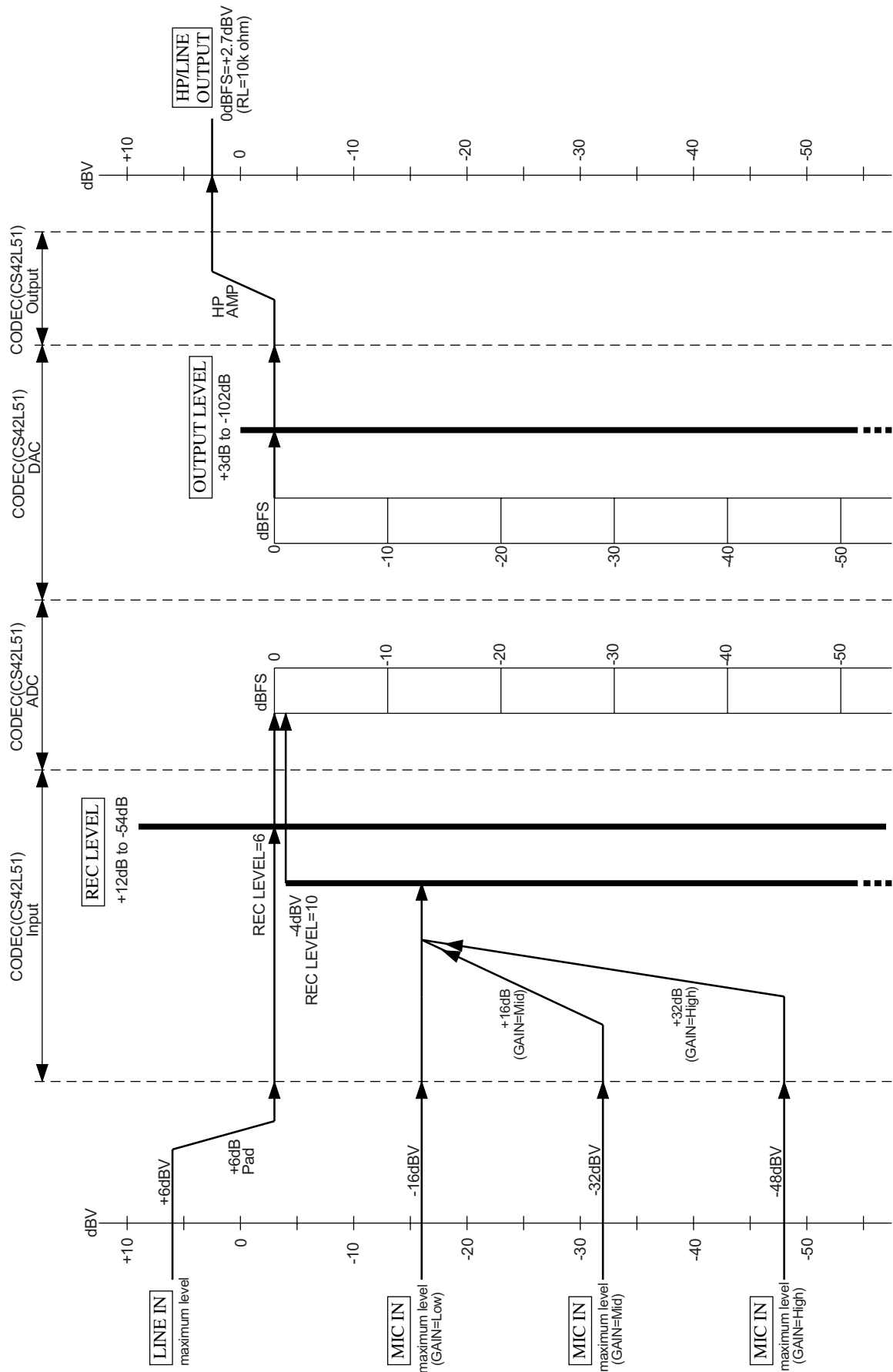
5. Block Diagram

ブロックダイアグラム



6. Level Diagram

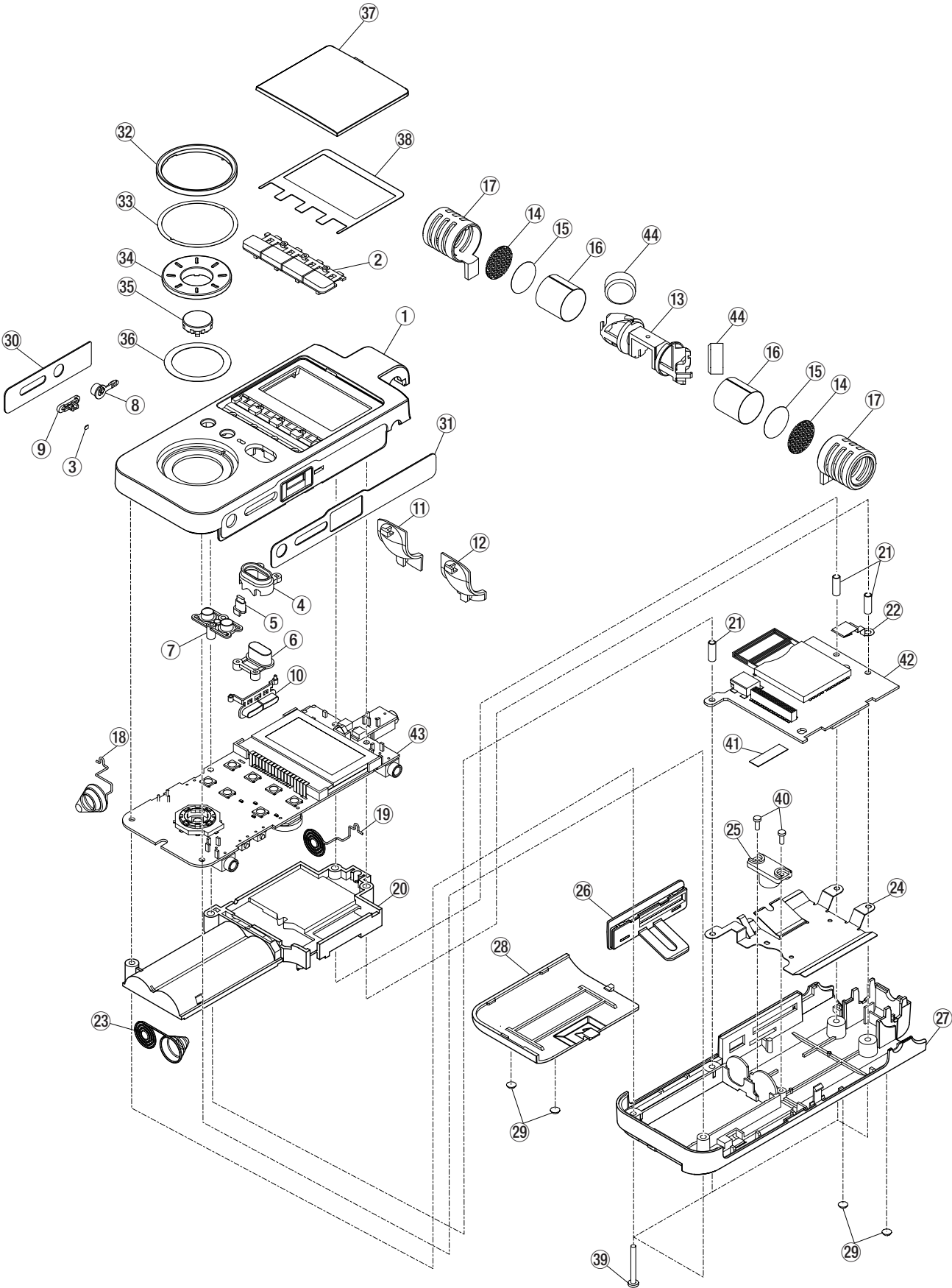
レベルダイアグラム



7. Exploded Views and Parts List

分解図とパーツリスト

Exploded View-1



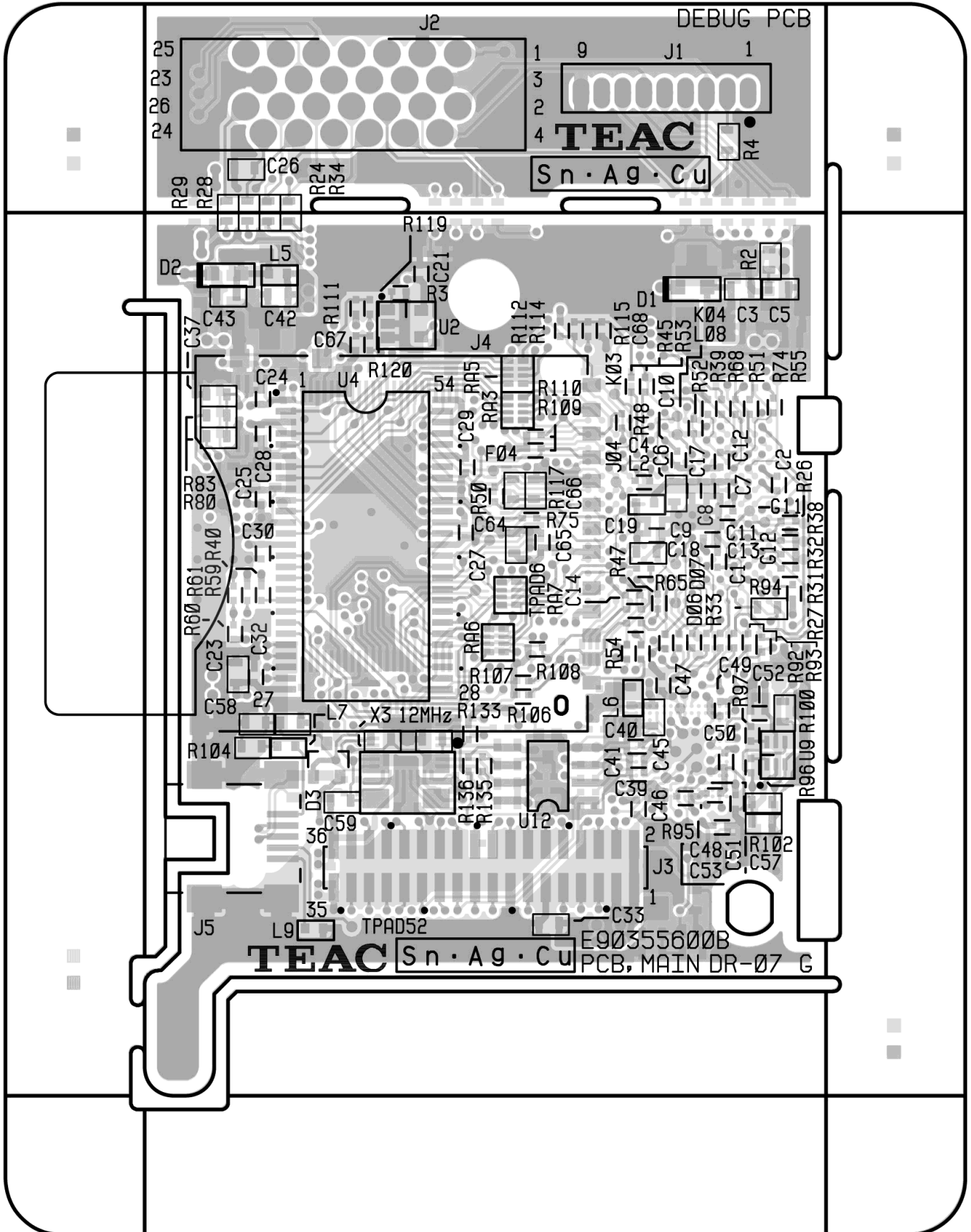
Exploded View-1

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	M02908100E	CASE, TOP DR07 G	
1- 2	M02908900B	BUTTON, TRANSPORT DR07 G	
1- 3	M02968200A	SHEET, HOLD DR07 G	
1- 4	M02909600A	LENS, REC DR07 G	
1- 5	M02909700B	LENS, PEAK DR07 G	
1- 6	M02909000B	BUTTON, REC DR07 G	
1- 7	M02909100C	BUTTON, STOP DR07 G	
1- 8	M02909200A	BUTTON, POWER DR07 G	
1- 9	M02909400B	KNOB, SLIDE DR07 G	
1-10	M02909300A	BUTTON, LE DR07 G	
1-11	M02908300B	COVER, MIC L DR07 G	
1-12	M02908400B	COVER, MIC R DR07 G	
1-13	M02910200D	HOLDER, MIC MARGE DR07 G	
1-14	M02756700B	SHEET, TOP MESH DR1 G	
1-15	M02756800A	SHEET, TOP SCREEN DR1 G	
1-16	M02910100B	SHEET, SIDE MESH DR07 G	
1-17	M02910000B	CASE, MIC DR07 G	
1-18	M02929600A	SPRING, MINUS DR07 G	
1-19	M02929700A	SPRING, PLUS DR07 G	
1-20	M02909800B	HOLDER, PCBA DR07 G	
1-21	M02599700A	COLLAR, BUSH 2.4*3*L8.5 G	
1-22	M02968100A	SHIELD SHEET, MAIN DR07 G	
1-23	M02666400A	SPRING, BATT CDXT2 G	
1-24	M02909900A	CHASSIS, MAIN DR07 G	
1-25	M02910300A	JOINT, TRIPOD DR07 G	
1-26	M02908500D	COVER, SD DR07 G	
1-27	M02908200C	CASE, BOTTOM DR07 G	
1-28	M02908600D	COVER, BATTERY DR07 G	
1-29	M02757700B	FOOT, D40*H15 DR1 G	
1-30	M02908700B	SIDE PANEL, L DR07 G	
1-31	M02908800A	SIDE PANEL, R DR07 G	
1-32	M02933000B	RING, BASE DR07 G	
1-33	M02933100A	SHEET, RING DR07 G	
1-34	M02755400C	KNOB, JOG DR1 G	
1-35	M02755500B	BUTTON, ENTER DR1 G	
1-36	M02587500A	POLYEST SHEET, JOG MPGT1 G	
1-37	M02909500A	WINDOW, DR07 G	
1-38	M02930400A	SHEET, WIN DR07 G	
1-39	B00311318A	SCREW, BPP 2*18 FZB G	
1-40	B00312500A	SCREW, MPPR 1.7*4.5 FZB G	
1-41	M02931900A	SHEET, PCB MAIN DR07 G	
1-42	E95355600A	PCBA, MAIN DR-07 G.....	Refer to page 20 & 21
1-43		PCBA, PANEL DR-07 G.....	GATHER PCBA, PANEL DR-07 G (Refer to page 22 & 23)
1-44	E01502000A	MIC, EM135-M2S7H55B1-E G	

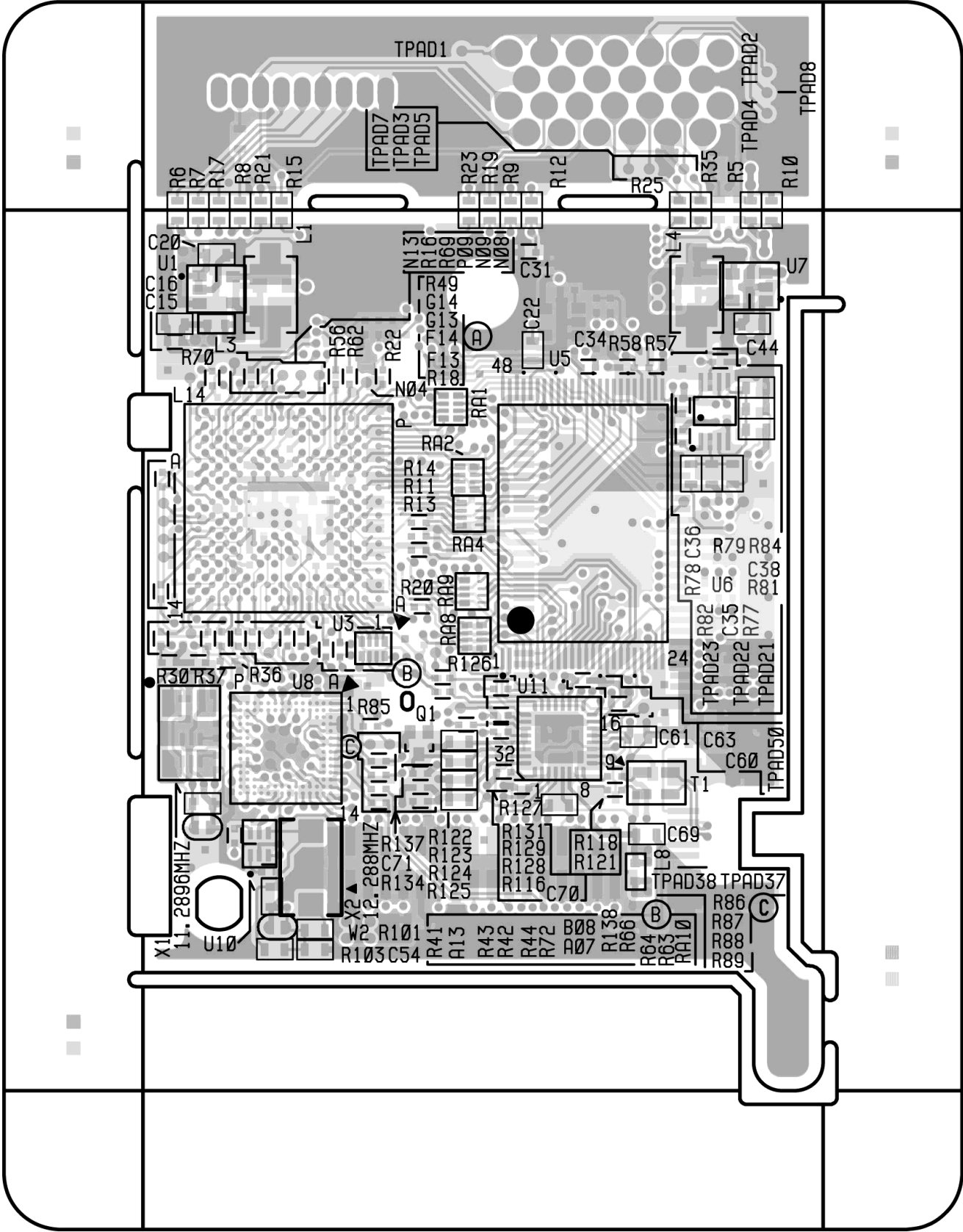
8. PC Boards and Parts List

基板図とパーツリスト

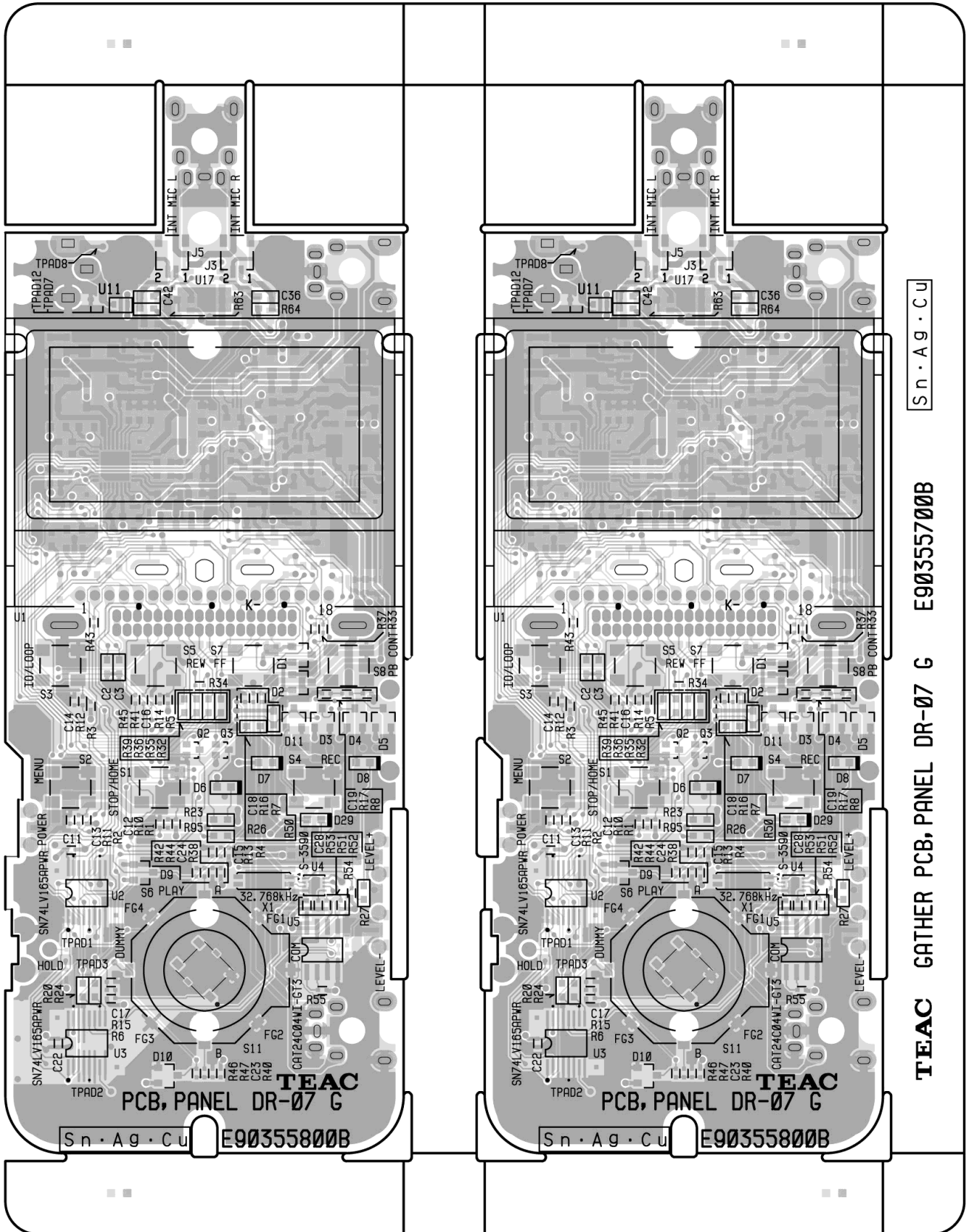
PCB A, MAIN DR-07 G (SIDE A)



PCB A, MAIN DR-07 G (SIDE B)



GATHER PCBA,PANEL DR-07 G (SIDE A)



Sn · Ag · Cu

E90355700B

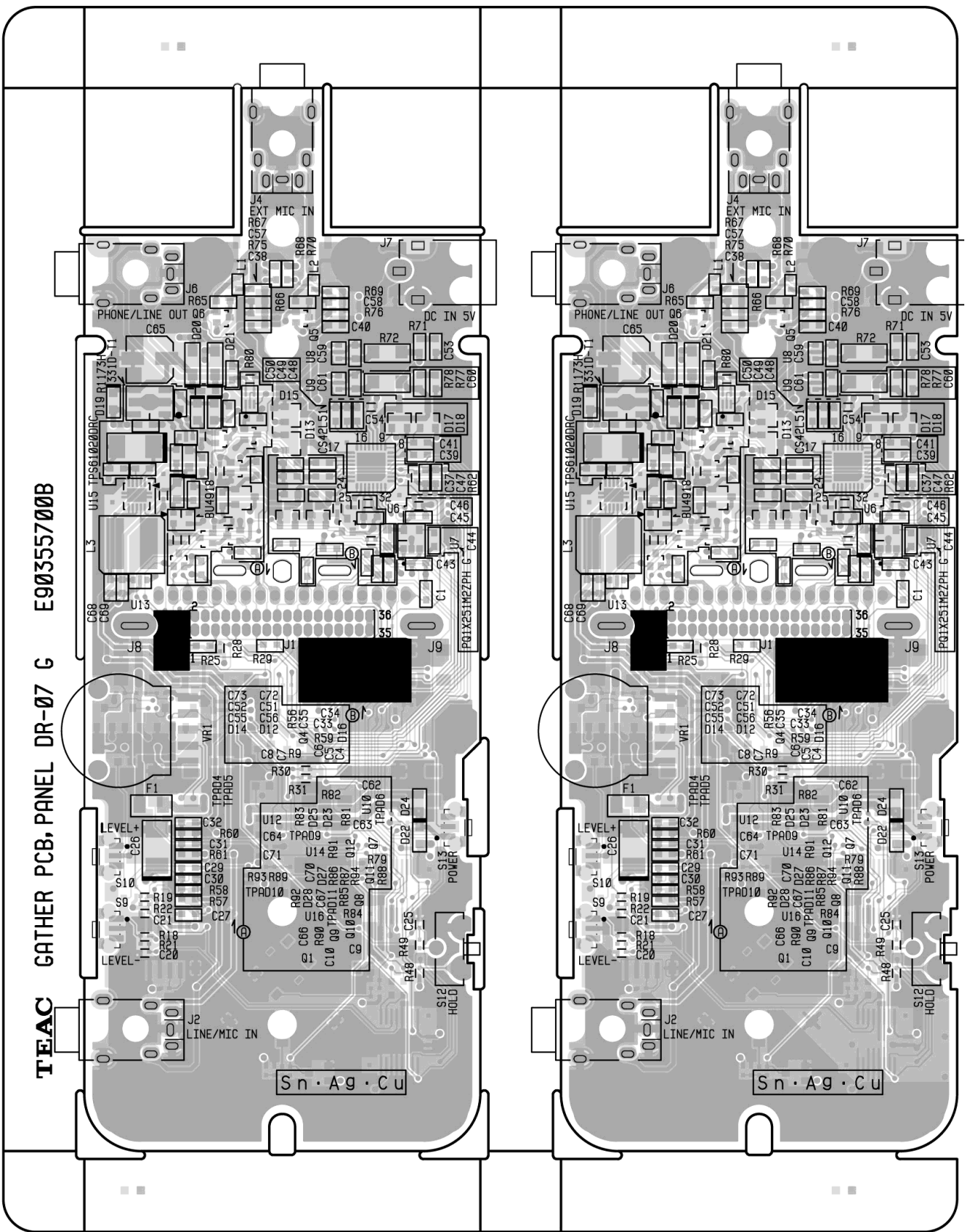
PCB, PANEL DR-07 G

TEAC

Sn · Ag · Cu E90355800B

Sn · Ag · Cu E90355800B

GATHER PCBA,PANEL DR-07 G (SIDE B)



PCBA,MAIN DR-07 G

REF.NO.	PARTS NO.	DESCRIPTION
	E95355600A	PCBA,MAIN DR-07 G PCB,MAIN DR-07 G
D1 D2	S0022094	DIODE,1SS355
D3	S0023224	DIODE,DAN217 T146 G
J3	E0134523	CONNECTOR,2200SB36GSM45 G
J4	E0143773	CONNECTOR,SCDA4A0400 G
J5	E0143954	CONNECTOR,USB MINI-5B G
L1 L4	E0101174	COIL,LQH43CN100K03L G
L2 L3	E0126164	BEAD COIL,BLM18PG471SN1D G
L5	E0126164	BEAD COIL,BLM18PG471SN1D G
L6	E0126164	BEAD COIL,BLM18PG471SN1D G
L7 L9	E0126164	BEAD COIL,BLM18PG471SN1D G
L8	E0126164	BEAD COIL,BLM18PG471SN1D G
Q1	S0065074	TRANSISTOR,DTC124EUA TP G
RA1	R0181584	RES ARRAY,82*4 1005 G
RA2-RA5	R0181584	RES ARRAY,82*4 1005 G
RA6-RA10	R0181594	RES ARRAY,47*4 1005 G
T1	E0128484	FILTER,956BP-1002=P2 G
U1	S0079894	IC,TPS62202DBVR G
U2	S0065024	IC,BD46285G G
U3	S0060143	IC,SCF5249VM140
U4	S0055053	IC,M12L64164A-7T-G
U5	S00798700A	IC,ROM ASSY SYS DR-07 G
U5	S0059093	@IC,S29AL008D70TFI020 G
U5	D01054700B	SOFTWARE SPEC,SYS DR-07 G
U5	M02930000A	LABEL,ROM SYS DR07 G
U6	S0066994	IC,BA2903FVM G
U7	S0079904	IC,TPS62207DBVR G
U8	S0075183	IC,LCMX0256E-3MN100C G
U9	S0065014	IC,SN74LVC2GU04DCKR G
U10	S0065014	IC,SN74LVC2GU04DCKR G
U11	S0079744	IC,AU6336-MOF G
U12	S00798800A	IC,ROM ASSY USB DR-07 G
U12	S0071694	IC,CAT24C04WI-GT3 G
U12	D01054800A	SOFTWARE SPEC,USB DR-07 G
X1	E0141174	RESONATOR,11.2896MHZ G
X2	E0143413	XTAL,LAP55A 12.288MHZ G
X3	E0141184	RESONATOR,12.0000MHZ G

REF.NO.	PARTS NO.	DESCRIPTION
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GATHER PCBA,PANEL DR-07 G

REF.NO.	PARTS NO.	DESCRIPTION
	E95355700A	GATHER PCBA,PANEL DR-07 G PCB,PANEL DR-07 G
		PCBA,PANEL DR-07 G
	E01502000A	MIC,EM135-M2S7H55B1-E G
D1-D5	S0023224	DIODE,DAN217 T146 G
D6	S0075754	LED,SML-512UW(RED) G
D7 D8	S0075754	LED,SML-512UW(RED) G
D9-D11	S0023224	DIODE,DAN217 T146 G
D12-D15	S0023224	DIODE,DAN217 T146 G
D16 D24	S0075354	DIODE,RB551V-30 TE17 G
D17 D18	S0023224	DIODE,DAN217 T146 G
D19 D22	S0022094	DIODE,1SS355
D20 D21	S0071644	DIODE,RB161M-20 G
D23	S0022094	DIODE,1SS355
D25 D28	S0075354	DIODE,RB551V-30 TE17 G
D27	S0022094	DIODE,1SS355
D29	S0075754	LED,SML-512UW(RED) G
F1	E0017804	FUSE,ICP-S2.3 (-TN)
J1	E0134530	CONNECTOR,2199SB36G6122 G
J2 J4	E0143793	JACK,LGY3009-0200F G
J3 J5	E0154204	CONNECTOR,SM02B-SRSS-TB G
J6	E0143793	JACK,LGY3009-0200F G
J7	E0146132	JACK,DC YKB31-0023A G
L1 L2	E0126164	BEAD COIL,BLM18PG471SN1D G
L3	E0153004	COIL,CDRH5D18NP-6R2NC G
Q1	S0029814	TRANSISTOR,DTC123EUA G
Q2	S0065074	TRANSISTOR,DTC124EUA TP G
Q3	S0065074	TRANSISTOR,DTC124EUA TP G
Q4 Q7	S0065074	TRANSISTOR,DTC124EUA TP G
Q5	S0041574	TRANSISTER,DTA124EUA G
Q6 Q9	S0041574	TRANSISTER,DTA124EUA G
Q8	S0066984	TRANSISTOR,2SA1037AK TP G
Q10 Q11	S0065074	TRANSISTOR,DTC124EUA TP G
Q12	S0065074	TRANSISTOR,DTC124EUA TP G
S1-S5	E00683600B	SW,TSW-6A-2-16-T50
S6	E0134644	SW,TACT TS050W1F43FK4 G
S7 S8	E00683600B	SW,TSW-6A-2-16-T50
S9 S10	E0143813	SW,TACT SKRTLAE010 G
S11	E0143823	ENCODER,SRE-2431ST G
S12	E0144730	SW,S5SS213100 G
S13	E0143813	SW,TACT SKRTLAE010 G
U1	E01536200A	LCD,KMC12864 DR-07 G
U2 U3	S0065384	IC,SN74LV165APWR G
U4	S0075164	IC,S-35390A-I8T1G G
U5	S0071694	IC,CAT24C04WI-GT3 G
U6	S0075283	IC,CS42L51-CNZR G
U7	S0064174	IC,PQ1X251M2ZPH G
U8 U9	E0153634	FILTER,MCF182CN473M04AK G
U10	S0080024	IC,BD4944FVE-TR G
U11 U13	E0153634	FILTER,MCF182CN473M04AK G
U12	S0075293	IC,R1173H331D-T1-F G
U14	E0153634	FILTER,MCF182CN473M04AK G

GATHER PCBA,PANEL DR-07 G

REF.NO.	PARTS NO.	DESCRIPTION
U15	S0080104	IC,TPS61020DRCR G
U16	S0079934	IC,BU4918F-TR G
VR1	R0186553	VR,XV010702G15C20K-3979 G
X1	E0143374	XTAL,SSP-T7-F 32.768K 7P G

9. Included Accessories

付属品

Included Accessories

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	D01055601A	OWNERS MNL,PRT(J) DR07 G [JEX]	
	D01055620A	OWNERS MNL,PRT(E) DR07 G	
	D01055881A	OWNERS MNL,QSG(F) DR07 G [E]	
	D01055880A	OWNERS MNL,QSG(G) DR07 G [E]	
	D01055882A	OWNERS MNL,QSG(I) DR07 G [E]	
	D01055883A	OWNERS MNL,QSG(S) DR07 G [E]	
	D01068600A	SHEET,INSERTION DIVIDE G	
	E01545400A	SD CARD ASSY,XXXX 1GB G OWNERS MNL,PRT(J) DR07 G OWNERS MNL,PRT(E) DR07 G	
		OWNERS MNL,DAT(F) DR07 G OWNERS MNL,DAT(G) DR07 G OWNERS MNL,DAT(I) DR07 G OWNERS MNL,DAT(S) DR07 G SD CARD,SD-M02G7R5W G	
	E0135680	USBB CABLE,CA3096080A37 G	
	E01536100A	BAT,LR6(GD)2P(E)O NF D G	
	M02930100A	COVER,WINDSCREEN DR07 G	

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with * require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in this manual.
- △ Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [] mark can be used only with the version designated.
[J]: JAPAN [US/C]: U.S.A./CANADA [K]: KOREA [E]: EUROPE
[UK]: U.K. [A]: AUSTRALIA [T]: TAIWAN [JEX]: JAPAN & ASIA
[CH]: CHINA [ETC]: U.S.A./CANADA/SOUTH AMERICA

注 意

- プリント基板図は部品面を示しています。
- *印の部品は納期が若干かかります。
あらかじめご了承ください。
- 分解図に部番のない部品および品番のない部品は供給できません。
- 標準の抵抗、コンデンサーは省略してあります。
回路図を参照してください。
- △印は安全重要部品です。
交換する時は必ず指定の部品を使用してください。
- 仕向先
[J]: JAPAN [US/C]: U.S.A./CANADA [K]: KOREA
[E]: EUROPE [UK]: U.K. [A]: AUSTRALIA
[T]: TAIWAN [JEX]: JAPAN & ASIA [CH]: CHINA
[ETC]: U.S.A./CANADA/SOUTH AMERICA

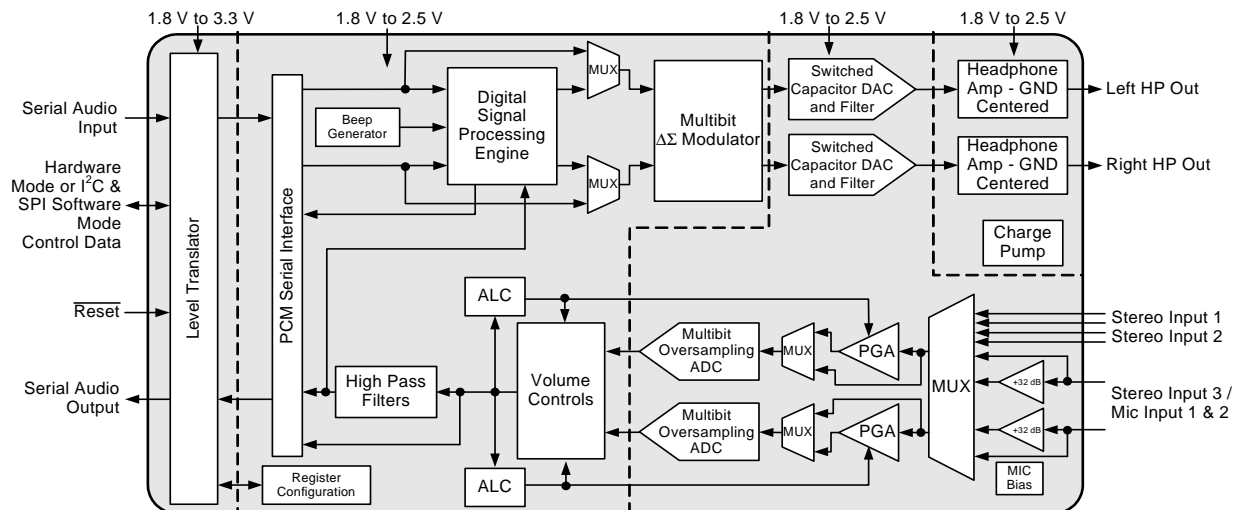
Low Power, Stereo CODEC with Headphone Amp

DIGITAL to ANALOG FEATURES

- ◆ 98 dB Dynamic Range (A-wtd)
- ◆ -86 dB THD+N
- ◆ Headphone Amplifier - GND Centered
 - On-Chip Charge Pump Provides -VA_HP
 - No DC-Blocking Capacitor Required
 - 46 mW Power Into Stereo 16 Ω @ 1.8 V
 - 88 mW Power Into Stereo 16 Ω @ 2.5 V
 - -75 dB THD+N
- ◆ Digital Signal Processing Engine
 - Bass & Treble Tone Control, De-Emphasis
 - PCM + ADC Mix w/Independent Vol Control
 - Master Digital Volume Control
 - Soft Ramp & Zero Cross Transitions
- ◆ Beep Generator
 - Tone Selections Across Two Octaves
 - Separate Volume Control
 - Programmable On & Off Time Intervals
 - Continuous, Periodic or One-Shot Beep Selections
- ◆ Programmable Peak-Detect and Limiter
- ◆ Pop and Click Suppression

ANALOG to DIGITAL FEATURES

- ◆ 98 dB Dynamic Range (A-wtd)
- ◆ -88 dB THD+N
- ◆ Analog Gain Controls
 - +32 dB or +16 dB MIC Pre-Amplifiers
 - Analog Programmable Gain Amplifier (PGA)
- ◆ +20 dB Digital Boost
- ◆ Programmable Automatic Level Control (ALC)
 - Noise Gate for Noise Suppression
 - Programmable Threshold and Attack/Release Rates
- ◆ Independent Channel Control
- ◆ Digital Volume Control
- ◆ High-Pass Filter Disable for DC Measurements
- ◆ Stereo 3:1 Analog Input MUX
- ◆ Dual MIC Inputs
 - Programmable, Low Noise MIC Bias Levels
 - Differential MIC Mix for Common Mode Noise Rejection
- ◆ Very Low 64 Fs Oversampling Clock Reduces Power Consumption



SYSTEM FEATURES

- ◆ 24-bit Converters
- ◆ 4 kHz to 96 kHz Sample Rate
- ◆ Multi-bit Delta Sigma Architecture
- ◆ Low Power Operation
 - Stereo Playback: 12.93 mW @ 1.8 V
 - Stereo Record and Playback: 20.18 mW @ 1.8 V
- ◆ Variable Power Supplies
 - 1.8 V to 2.5 V Digital & Analog
 - 1.8 V to 3.3 V Interface Logic
- ◆ Power Down Management
 - ADC, DAC, CODEC, MIC Pre-Amplifier, PGA
- ◆ Software Mode (I²C® & SPI™ Control)
- ◆ Hardware Mode (Stand-Alone Control)
- ◆ Digital Routing/Mixes:
 - Analog Out = ADC + Digital In
 - Digital Out = ADC + Digital In
 - Internal Digital Loopback
 - Mono Mixes
- ◆ Flexible Clocking Options
 - Master or Slave Operation
 - High-Impedance Digital Output Option (for easy MUXing between CODEC and Other Data Sources)
 - Quarter-Speed Mode - (i.e. Allows 8 kHz F_s while maintaining a flat noise floor up to 16 kHz)

APPLICATIONS

- ◆ HDD & Flash-Based Portable Audio Players
- ◆ MD Players/Recorders
- ◆ PDAs
- ◆ Personal Media Players
- ◆ Portable Game Consoles
- ◆ Digital Voice Recorders
- ◆ Digital Camcorders
- ◆ Digital Cameras
- ◆ Smart Phones

GENERAL DESCRIPTION

The CS42L51 is a highly integrated, 24-bit, 96 kHz, low power stereo CODEC. Based on multi-bit, delta-sigma modulation, it allows infinite sample rate adjustment between 4 kHz and 96 kHz. Both the ADC and DAC offer many features suitable for low power, portable system applications.

The ADC input path allows independent channel control of a number of features. An input multiplexer selects between line-level or microphone level inputs for each channel. The microphone input path includes a selectable programmable-gain pre-amplifier stage and a low noise MIC bias voltage supply. A PGA is available for line or microphone inputs and provides analog gain with soft ramp and zero cross transitions. The ADC also features a digital volume attenuator with soft ramp transitions. A programmable ALC and Noise Gate monitor the input signals and adjust the volume levels appropriately.

The DAC output path includes a digital signal processing engine. Tone Control provides bass and treble adjustment of four selectable corner frequencies. The Mixer allows independent volume control for both the ADC mix and the PCM mix, as well as a master digital volume control for the analog output. All volume level changes may be configured to occur on soft ramp and zero cross transitions. The DAC also includes de-emphasis, limiting functions and a beep generator delivering tones selectable across a range of two full octaves.

The stereo headphone amplifier is powered from a separate positive supply and the integrated charge pump provides a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates external DC-blocking capacitors.

In addition to its many features, the CS42L51 operates from a low-voltage analog and digital core, making this CODEC ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS42L51 is available in a 32-pin QFN package in both Commercial (-10 to +70° C) and Automotive grades (-40 to +85° C). The CDB42L51 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see [“Ordering Information” on page 85](#) for complete details.

TABLE OF CONTENTS

1. PIN DESCRIPTIONS - SOFTWARE (HARDWARE) MODE	7
1.1 Digital I/O Pin Characteristics	9
2. TYPICAL CONNECTION DIAGRAMS	10
3. CHARACTERISTIC AND SPECIFICATION TABLES	12
SPECIFIED OPERATING CONDITIONS	12
ABSOLUTE MAXIMUM RATINGS	12
ANALOG INPUT CHARACTERISTICS (COMMERCIAL - CNZ)	13
ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)	14
ADC DIGITAL FILTER CHARACTERISTICS	15
ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL - CNZ)	16
ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)	17
LINE OUTPUT VOLTAGE CHARACTERISTICS	18
HEADPHONE OUTPUT POWER CHARACTERISTICS	19
COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE	20
SWITCHING SPECIFICATIONS - SERIAL PORT	20
SWITCHING SPECIFICATIONS - I ² C® CONTROL PORT	22
SWITCHING CHARACTERISTICS - SPI™ CONTROL PORT	23
DC ELECTRICAL CHARACTERISTICS	24
DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS	24
POWER CONSUMPTION	25
4. APPLICATIONS	26
4.1 Overview	26
4.1.1 Architecture	26
4.1.2 Line & MIC Inputs	26
4.1.3 Line & Headphone Outputs	26
4.1.4 Signal Processing Engine	26
4.1.5 Beep Generator	26
4.1.6 Device Control (Hardware or Software Mode)	26
4.1.7 Power Management	26
4.2 Hardware Mode	27
4.3 Analog Inputs	28
4.3.1 Digital Code, Offset & DC Measurement	28
4.3.2 High-Pass Filter and DC Offset Calibration	29
4.3.3 Digital Routing	29
4.3.4 Differential Inputs	29
4.3.4.1 External Passive Components	29
4.3.5 Analog Input Multiplexer	31
4.3.6 MIC & PGA Gain	31
4.3.7 Automatic Level Control (ALC)	32
4.3.8 Noise Gate	33
4.4 Analog Outputs	34
4.4.1 De-Emphasis Filter	34
4.4.2 Volume Controls	35
4.4.3 Mono Channel Mixer	35
4.4.4 Beep Generator	35
4.4.5 Tone Control	36
4.4.6 Limiter	36
4.4.7 Line-Level Outputs and Filtering	37
4.4.8 On-Chip Charge Pump	38
4.5 Serial Port Clocking	38
4.5.1 Slave	39
4.5.2 Master	39

4.5.3 High-Impedance Digital Output	40
4.5.4 Quarter- and Half-Speed Mode	40
4.6 Digital Interface Formats	40
4.7 Initialization	41
4.8 Recommended Power-Up Sequence	41
4.9 Recommended Power-Down Sequence	42
4.10 Software Mode	43
4.10.1 SPI Control	43
4.10.2 I ² C Control	43
4.10.3 Memory Address Pointer (MAP)	45
4.10.3.1 Map Increment (INCR)	45
5. REGISTER QUICK REFERENCE	46
6. REGISTER DESCRIPTION	49
6.1 Chip I.D. and Revision Register (Address 01h) (Read Only)	49
6.2 Power Control 1 (Address 02h)	49
6.3 MIC Power Control & Speed Control (Address 03h)	50
6.4 Interface Control (Address 04h)	52
6.5 MIC Control (Address 05h)	53
6.6 ADC Control (Address 06h)	54
6.7 ADCx Input Select, Invert & Mute (Address 07h)	56
6.8 DAC Output Control (Address 08h)	57
6.9 DAC Control (Address 09h)	58
6.10 ALCX & PGAX Control: ALCA, PGAA (Address 0Ah) & ALCB, PGAB (Address 0Bh)	59
6.11 ADCx Attenuator: ADCA (Address 0Ch) & ADCB (Address 0Dh)	60
6.12 ADCx Mixer Volume Control: ADCA (Address 0Eh) & ADCB (Address 0Fh)	61
6.13 PCMX Mixer Volume Control:	
PCMA (Address 10h) & PCMB (Address 11h)	62
6.14 Beep Frequency & Timing Configuration (Address 12h)	62
6.15 Beep Off Time & Volume (Address 13h)	63
6.16 Beep Configuration & Tone Configuration (Address 14h)	64
6.17 Tone Control (Address 15h)	65
6.18 AOOUTx Volume Control:	
AOUTA (Address 16h) & AOOUTB (Address 17h)	66
6.19 PCM Channel Mixer (Address 18h)	67
6.20 Limiter Threshold SZC Disable (Address 19h)	67
6.21 Limiter Release Rate Register (Address 1Ah)	69
6.22 Limiter Attack Rate Register (Address 1Bh)	70
6.23 ALC Enable & Attack Rate (Address 1Ch)	70
6.24 ALC Release Rate (Address 1Dh)	71
6.25 ALC Threshold (Address 1Eh)	71
6.26 Noise Gate Configuration & Misc. (Address 1Fh)	72
6.27 Status (Address 20h) (Read Only)	73
6.28 Charge Pump Frequency (Address 21h)	74
7. ANALOG PERFORMANCE PLOTS	75
7.1 Headphone THD+N versus Output Power Plots	75
7.2 Headphone Amplifier Efficiency	77
7.3 ADC_FILT+ Capacitor Effects on THD+N	78
8. EXAMPLE SYSTEM CLOCK FREQUENCIES	79
8.1 Auto Detect Enabled	79
8.2 Auto Detect Disabled	80
9. PCB LAYOUT CONSIDERATIONS	81
9.1 Power Supply, Grounding	81
9.2 QFN Thermal Pad	81
10. ADC & DAC DIGITAL FILTERS	82

11. PARAMETER DEFINITIONS	83
12. PACKAGE DIMENSIONS	84
THERMAL CHARACTERISTICS	84
13. ORDERING INFORMATION	85
14. REFERENCES	85
15. REVISION HISTORY	86

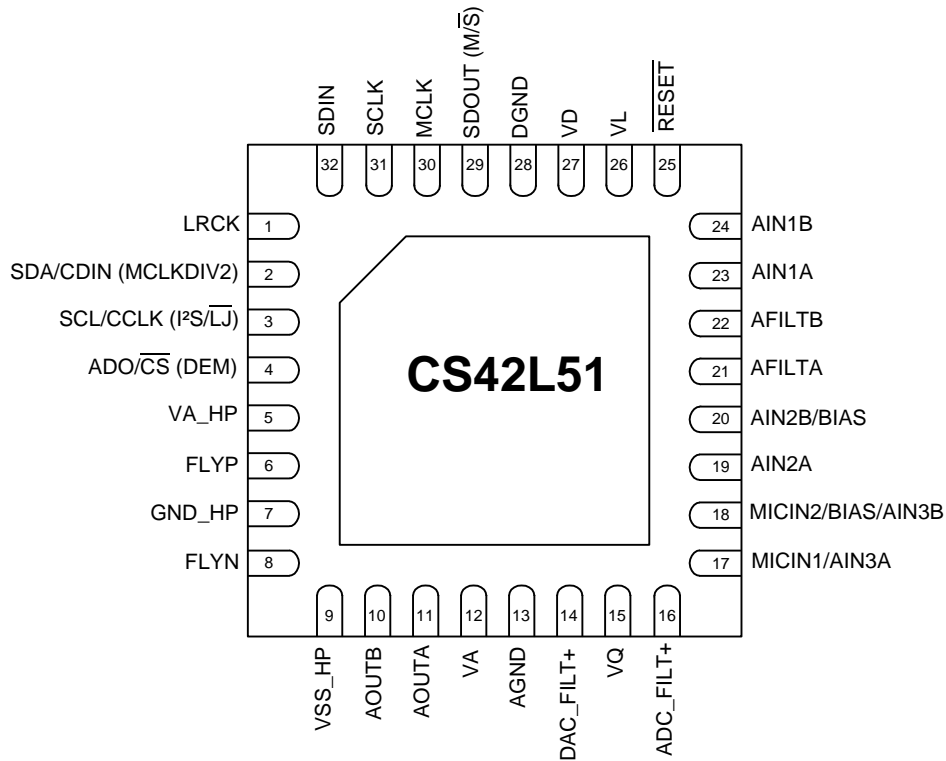
LIST OF FIGURES

Figure 1. Typical Connection Diagram (Software Mode)	10
Figure 2. Typical Connection Diagram (Hardware Mode)	11
Figure 3. Headphone Output Test Load	19
Figure 4. Serial Audio Interface Slave Mode Timing	21
Figure 5. Serial Audio Interface Master Mode Timing	21
Figure 6. Control Port Timing - I ² C	22
Figure 7. Control Port Timing - SPI Format	23
Figure 8. Analog Input Architecture	28
Figure 9. MIC Input Mix w/Common Mode Rejection	30
Figure 10. Differential Input	30
Figure 11. ALC	32
Figure 12. Noise Gate Attenuation	33
Figure 13. Output Architecture	34
Figure 14. De-Emphasis Curve	35
Figure 15. Beep Configuration Options	36
Figure 16. Peak Detect & Limiter	37
Figure 17. Master Mode Timing	39
Figure 18. Tri-State Serial Port	40
Figure 19. I ² S Format	40
Figure 20. Left-Justified Format	41
Figure 21. Right-Justified Format (DAC only)	41
Figure 22. Initialization Flowchart	42
Figure 23. Control Port Timing in SPI Mode	43
Figure 24. Control Port Timing, I ² C Write	44
Figure 25. Control Port Timing, I ² C Read	44
Figure 26. AIN & PGA Selection	56
Figure 27. THD+N vs. Output Power per Channel at 1.8 V (16 Ω load)	75
Figure 28. THD+N vs. Output Power per Channel at 2.5 V (16 Ω load)	75
Figure 29. THD+N vs. Output Power per Channel at 1.8 V (32 Ω load)	76
Figure 30. THD+N vs. Output Power per Channel at 2.5 V (32 Ω load)	76
Figure 31. Power Dissipation vs. Output Power into Stereo 16 Ω	77
Figure 32. Power Dissipation vs. Output Power into Stereo 16 Ω (Log Detail)	77
Figure 33. ADC THD+N vs. Frequency w/Capacitor Effects	78
Figure 34. ADC Passband Ripple	82
Figure 35. ADC Stopband Rejection	82
Figure 36. ADC Transition Band	82
Figure 37. ADC Transition Band Detail	82
Figure 38. DAC Passband Ripple	82
Figure 39. DAC Stopband	82
Figure 40. DAC Transition Band	82
Figure 41. DAC Transition Band (Detail)	82

LIST OF TABLES

Table 1. I/O Power Rails	9
Table 2. Hardware Mode Feature Summary	27
Table 3. MCLK/LRCK Ratios	39

1. PIN DESCRIPTIONS - SOFTWARE (HARDWARE) MODE



Pin Name	#	Pin Description
LRCK	1	Left Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SDA/CDIN (MCLKDIV2)	2	Serial Control Data (Input/Output) - SDA is a data I/O in I ² C Mode. CDIN is the input data line for the control port interface in SPI Mode. MCLK Divide by 2 (Input) - Hardware Mode: Divides the MCLK by 2 prior to all internal circuitry.
SCL/CCLK (I ² S/LJ)	3	Serial Control Port Clock (Input) - Serial clock for the serial control port. Interface Format Selection (Input) - Hardware Mode: Selects between I ² S & Left-Justified interface formats for the ADC & DAC.
AD0/CS (DEM)	4	Address Bit 0 (I²C) / Control Port Chip Select (SPI) (Input) - AD0 is a chip address pin in I ² C Mode; CS is the chip-select signal for SPI format. De-Emphasis (Input) - Hardware Mode: Enables/disables the de-emphasis filter.
VA_HP	5	Analog Power For Headphone (Input) - Positive power for the internal analog headphone section.
FLYP	6	Charge Pump Cap Positive Node (Input) - Positive node for the external charge pump capacitor.
GND_HP	7	Analog Ground (Input) - Ground reference for the internal headphone/charge pump section.
FLYN	8	Charge Pump Cap Negative Node (Input) - Negative node for the external charge pump capacitor.
VSS_HP	9	Negative Voltage From Charge Pump (Output) - Negative voltage rail for the internal analog headphone section.

AOUTB	10	Analog Audio Output (<i>Output</i>) - The full-scale output level is specified in the DAC Analog Characteristics specification table
AOUTA	11	
VA	12	Analog Power (<i>Input</i>) - Positive power for the internal analog section.
AGND	13	Analog Ground (<i>Input</i>) - Ground reference for the internal analog section.
DAC_FILT+	14	Positive Voltage Reference (<i>Output</i>) - Positive reference voltage for the internal sampling circuits.
VQ	15	Quiescent Voltage (<i>Output</i>) - Filter connection for internal quiescent voltage.
ADC_FILT+	16	Positive Voltage Reference (<i>Output</i>) - Positive reference voltage for the internal sampling circuits.
MICIN1/ AIN3A	17	Microphone Input 1 (<i>Input</i>) - The full-scale level is specified in the ADC Analog Characteristics specification table.
MICIN2/ BIAS/AIN3B	18	Microphone Input 2 (<i>Input/Output</i>) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AIN2A	19	Analog Input (<i>Input</i>) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN2B/BIAS	20	Analog Input (<i>Input/Output</i>) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AFILTA	21	
AFILTB	22	Filter Connection (<i>Output</i>) - Filter connection for the ADC inputs.
AIN1A	23	Analog Input (<i>Input</i>) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN1B	24	
RESET	25	Reset (<i>Input</i>) - The device enters a low power mode when this pin is driven low.
VL	26	Digital Interface Power (<i>Input</i>) - Determines the required signal level for the serial audio interface and host control port. Refer to the Recommended Operating Conditions for appropriate voltages.
VD	27	Digital Power (<i>Input</i>) - Positive power for the internal digital section.
DGND	28	Digital Ground (<i>Input</i>) - Ground reference for the internal digital section.
SDOUT (M/S)	29	Serial Audio Data Output (<i>Output</i>) - Output for two's complement serial audio data. Serial Port Master/Slave (<i>Input/Output</i>) - Hardware Mode Startup Option: Selects between Master and Slave Mode for the serial port.
MCLK	30	Master Clock (<i>Input</i>) - Clock source for the delta-sigma modulators.
SCLK	31	Serial Clock (<i>Input/Output</i>) - Serial clock for the serial audio interface.
SDIN	32	Serial Audio Data Input (<i>Input</i>) - Input for two's complement serial audio data.
Thermal Pad	-	Thermal relief pad for optimized heat dissipation. See "QFN Thermal Pad" on page 81.

1.1 Digital I/O Pin Characteristics

The logic level for each input should not exceed the maximum ratings for the VL power supply.

Pin Name SW/(HW)	I/O	Driver	Receiver
RESET	Input	-	1.8 V - 3.3 V
SCL/CCLK (I ² S/LJ)	Input	-	1.8 V - 3.3 V, with Hysteresis
SDA/CDIN (MCLKDIV2)	Input/Output	1.8 V - 3.3 V, CMOS/Open Drain	1.8 V - 3.3 V, with Hysteresis
AD0/ $\overline{\text{CS}}$ (DEM)	Input	-	1.8 V - 3.3 V
MCLK	Input	-	1.8 V - 3.3 V
LRCK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SCLK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SDOUT (M/S)	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SDIN	Input	-	1.8 V - 3.3 V

Table 1. I/O Power Rails

2. TYPICAL CONNECTION DIAGRAMS

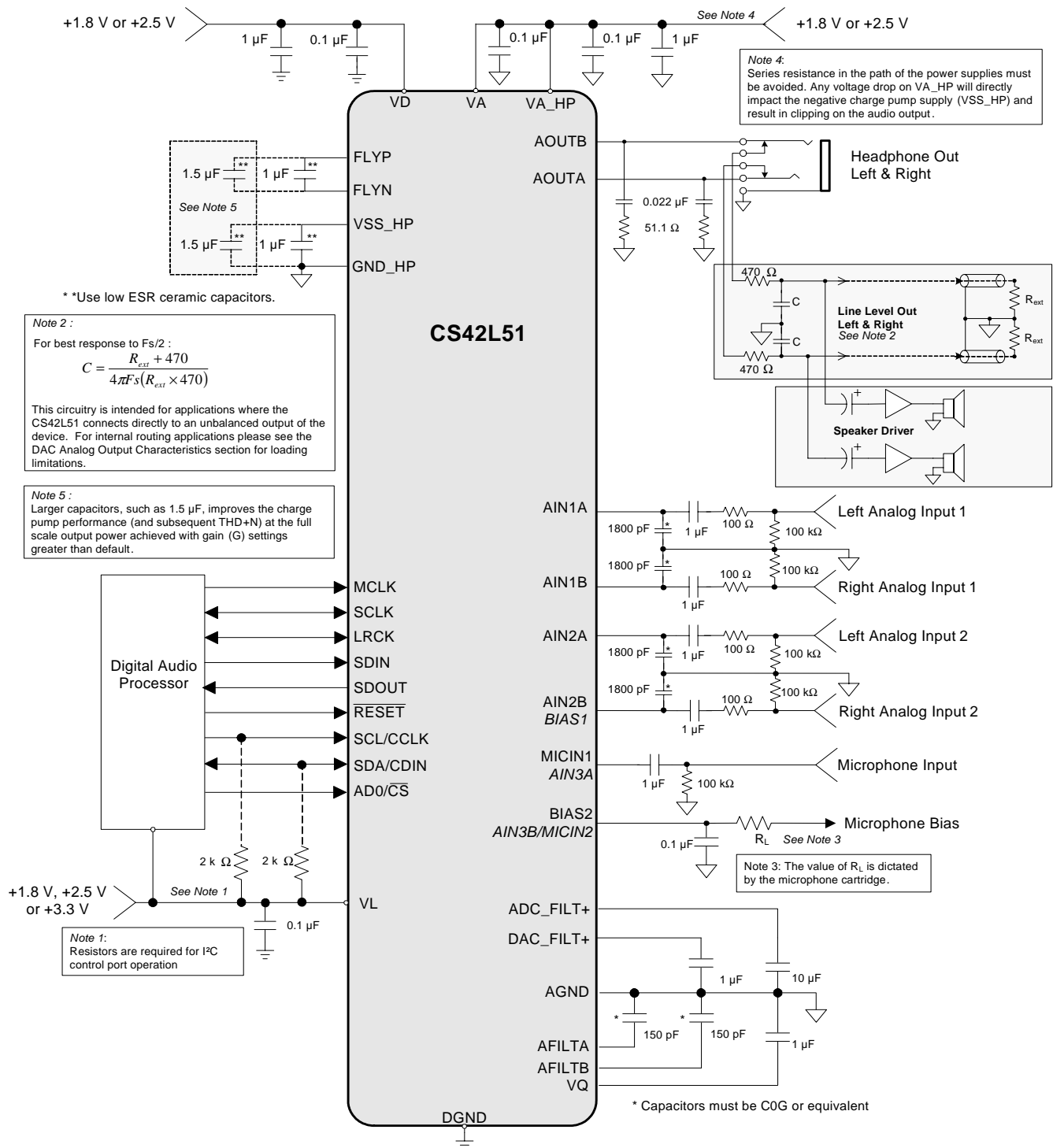


Figure 1. Typical Connection Diagram (Software Mode)

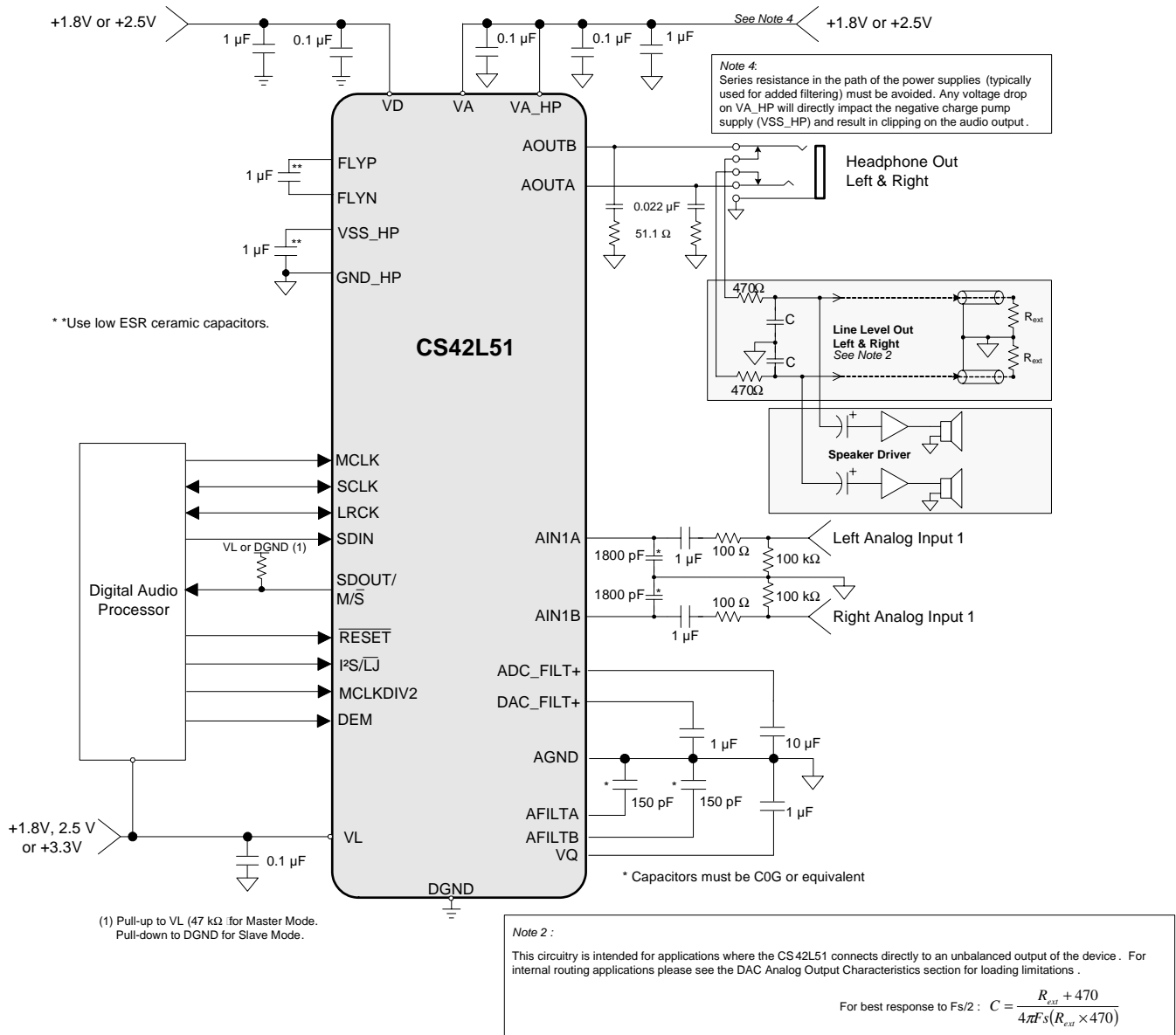


Figure 2. Typical Connection Diagram (Hardware Mode)

3. CHARACTERISTIC AND SPECIFICATION TABLES

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and $T_A = 25^\circ \text{C}$.)

SPECIFIED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters	Symbol	Min	Nom	Max	Units	
DC Power Supply (Note 1)						
Analog Core	VA	1.65	1.8	1.89	V	
		2.37	2.5	2.63	V	
Headphone Amplifier	VA_HP	1.65	1.8	1.89	V	
		2.37	2.5	2.63	V	
Digital Core	VD	1.65	1.8	1.89	V	
		2.37	2.5	2.63	V	
Serial/Control Port Interface	VL	1.65	1.8	1.89	V	
		2.37	2.5	2.63	V	
		3.14	3.3	3.47	V	
Ambient Temperature	Commercial - CNZ Automotive - DNZ	T_A	-10	-	+70	$^\circ\text{C}$
			-40	-	+85	$^\circ\text{C}$

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	Analog	-0.3	3.0	V
	Digital			V
	Serial/Control Port Interface			V
Input Current (Note 2)	I_{in}	-	± 10	mA
Analog Input Voltage	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage (Note 3)	V_{IND}	-0.3	VL+ 0.4	V
Ambient Operating Temperature (power applied)	T_A	-50	+115	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65	+150	$^\circ\text{C}$

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. The device will operate properly over the full range of the analog, headphone amplifier, digital core and serial/control port interface supplies.
2. Any pin except supplies. Transient currents of up to ± 100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to digital full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 5)		VA = 2.5 V (nominal)			VA = 1.8 V (nominal)			Unit	
		Min	Typ	Max	Min	Typ	Max		
Analog In to ADC (PGA bypassed)									
Dynamic Range	A-weighted	93	99	-	90	96	-	dB	
	unweighted	90	96	-	87	93	-	dB	
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-80	-	-84	-78	dB	
	-20 dBFS	-	-76	-	-	-73	-	dB	
	-60 dBFS	-	-36	-	-	-33	-	dB	
Analog In to PGA to ADC									
Dynamic Range									
PGA Setting: 0 dB	A-weighted	92	98	-	89	95	-	dB	
	unweighted	89	95	-	86	92	-	dB	
PGA Setting: +12 dB	A-weighted	85	91	-	82	88	-	dB	
	unweighted	82	88	-	79	85	-	dB	
Total Harmonic Distortion + Noise	PGA Setting: 0 dB	-1 dBFS	-	-88	-81	-	-86	-80	dB
		-60 dBFS	-	-35	-	-	-32	-	dB
	PGA Setting: +12 dB	-1 dBFS	-	-85	-79	-	-83	-77	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC									
Dynamic Range									
PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB	
	unweighted	-	83	-	-	80	-	dB	
Total Harmonic Distortion + Noise	PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC									
Dynamic Range									
PGA Setting: 0 dB	A-weighted	-	78	-	-	75	-	dB	
	unweighted	-	74	-	-	71	-	dB	
Total Harmonic Distortion + Noise	PGA Setting: 0 dB	-1 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics									
DC Accuracy									
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB	
Gain Drift		-	±100	-	-	±100	-	ppm/°C	
Offset Error		SDOUT Code with HPF On		-	352	-	-	352	LSB
Input									
Interchannel Isolation		-	90	-	-	90	-	dB	
DAC Isolation (Note 4)		-	70	-	-	70	-	dB	
Full-scale Input Voltage	ADC	0.74•VA	0.78•VA	0.82•VA	0.74•VA	0.78•VA	0.82•VA	Vpp	
	PGA (0 dB)	0.75•VA	0.794•VA	0.83•VA	0.75•VA	0.794•VA	0.83•VA	Vpp	
	MIC (+16 dB)		0.129•VA			0.129•VA		Vpp	
	MIC (+32 dB)		0.022•VA			0.022•VA		Vpp	
Input Impedance (Note 6)	ADC	-	20	-	-	20	-	kΩ	
	PGA	-	39	-	-	39	-	kΩ	
	MIC	-	50	-	-	50	-	kΩ	

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 5)		VA = 2.5 V (nominal)			VA = 1.8 V (nominal)			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog In to ADC								
Dynamic Range	A-weighted	91	99	-	88	96	-	dB
	unweighted	78	96	-	85	93	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-78	-	-84	-76	dB
	-20 dBFS	-	-76	-	-	-73	-	dB
	-60 dBFS	-	-36	-	-	-33	-	dB
Analog In to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
PGA Setting: +12 dB	A-weighted	83	91	-	80	88	-	dB
	unweighted	80	88	-	77	85	-	dB
Total Harmonic Distortion + Noise	PGA Setting: 0 dB	-1 dBFS	-88	-80	-	-86	-78	dB
		-60 dBFS	-35	-	-	-32	-	dB
	PGA Setting: +12 dB	-1 dBFS	-85	-77	-	-83	-75	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
	unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise	PGA Setting: 0 dB	-1 dBFS	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	78	-	-	75	-	dB
	unweighted	-	74	-	-	71	-	dB
Total Harmonic Distortion + Noise	PGA Setting: 0 dB	-1 dBFS	-74	-	-	-71	-	dB
Other Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error		SDOUT Code with HPF On	352	-	-	352	-	LSB
Input								
Interchannel Isolation		-	90	-	-	90	-	dB
DAC Isolation (Note 4)		-	70	-	-	70	-	dB
Full-scale Input Voltage	ADC	0.74•VA	0.78•VA	0.82•VA	0.74•VA	0.78•VA	0.82•VA	Vpp
	PGA (0 dB)	0.75•VA	0.794•VA	0.83•VA	0.75•VA	0.794•VA	0.83•VA	Vpp
	MIC (+16 dB)		0.129•VA			0.129•VA		Vpp
	MIC (+32 dB)		0.022•VA			0.022•VA		Vpp
Input Impedance (Note 6)	ADC	18	-	-	18	-	-	kΩ
	PGA	40	-	-	40	-	-	kΩ
	MIC	50	-	-	50	-	-	kΩ

4. Measured with DAC delivering full-scale output power into 16 Ω.

5. Referred to the typical full-scale voltage. Applies to all THD+N and Dynamic Range values in the table.
6. Measured between AINxx and AGND.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 7)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4948	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Group Delay		-	7.6/Fs	-	s
High-Pass Filter Characteristics (48 kHz Fs)					
Frequency Response	-3.0 dB	-	3.7	-	Hz
	-0.13 dB	-	24.2	-	Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	10 ⁵ /Fs	0	s

7. Response is clock-dependent and will scale with Fs. Note that the response plots (Figure 33 to Figure 41) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs. HPF parameters are for Fs = 48 kHz.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$ for the line output (see [Figure 3](#)), and test load $R_L = 16\ \Omega$, $C_L = 10\text{ pF}$ (see [Figure 3](#)) for the headphone output. HP_GAIN[2:0] = 011.)

Parameter (Note 8)		VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
		Min	Typ	Max	Min	Typ	Max	
$R_L = 10\text{ k}\Omega$								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-78	-	-88	-82	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
$R_L = 16\ \Omega$								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-69	-	-75	-69	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for $R_L = 16\ \Omega$ or $10\text{ k}\Omega$								
Output Parameters (Note 9)	Modulation Index (MI) Analog Gain Multiplier (G)	-	0.6787 0.6047	-	-	0.6787 0.6047	-	
Full-scale Output Voltage ($2 \cdot G \cdot MI \cdot VA$) (Note 9)		Refer to Table "Line Output Voltage Characteristics" on page 18						Vpp
Full-scale Output Power (Note 9)		Refer to Table "Headphone Output Power Characteristics" on page 19						mW
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 k Ω	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	± 100	-	-	± 100	-	ppm/ $^\circ\text{C}$
AC-Load Resistance (R_L) (Note 10)		16	-	-	16	-	-	Ω
Load Capacitance (C_L) (Note 10)		-	-	150	-	-	150	pF

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz and 96 kHz; test load $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$ for the line output (see [Figure 3](#)), and test load $R_L = 16\ \Omega$, $C_L = 10\text{ pF}$ (see [Figure 3](#)) for the headphone output.
HP_GAIN[2:0] = 011.)

Parameter (Note 8)	VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit	
	Min	Typ	Max	Min	Typ	Max		
$R_L = 10\text{ k}\Omega$								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-73	-	-88	-80	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
$R_L = 16\ \Omega$								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-67	-	-75	-67	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for $R_L = 16\ \Omega$ or $10\text{ k}\Omega$								
Output Parameters (Note 9)	Modulation Index (MI) Analog Gain Multiplier (G)	-	0.6787 0.6047	-	-	0.6787 0.6047	-	
Full-scale Output Voltage ($2 \cdot G \cdot MI \cdot VA$) (Note 9)		Refer to Table "Line Output Voltage Characteristics" on page 18						Vpp
Full-scale Output Power (Note 9)		Refer to Table "Headphone Output Power Characteristics" on page 19						mW
Interchannel Isolation (1 kHz)	16 Ω 10 k Ω	-	80 95	-	-	80 93	-	dB dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	± 100	-	-	± 100	-	ppm/ $^{\circ}$ C
AC-Load Resistance (R_L) (Note 10)		16	-	-	16	-	-	Ω
Load Capacitance (C_L) (Note 10)		-	-	150	-	-	150	pF

LINE OUTPUT VOLTAGE CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$ (see [Figure 3](#)).

Parameter			VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Voltage Into $R_L = 10\text{ k}\Omega$									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	1.34	-	-	0.97	-	V_{pp}
		2.5 V	-	1.34	-	-	0.97	-	V_{pp}
001	0.4571	1.8 V	-	1.55	-	-	1.12	-	V_{pp}
		2.5 V	-	1.55	-	-	1.12	-	V_{pp}
010	0.5111	1.8 V	-	1.73	-	-	1.25	-	V_{pp}
		2.5 V	-	1.73	-	-	1.25	-	V_{pp}
011 (default)	0.6047	1.8 V	-	2.05	-	1.41	1.48	1.55	V_{pp}
		2.5 V	1.95	2.05	2.15	-	1.48	-	V_{pp}
100	0.7099	1.8 V	-	2.41	-	-	1.73	-	V_{pp}
		2.5 V	-	2.41	-	-	1.73	-	V_{pp}
101	0.8399	1.8 V	-	2.85	-	-	2.05	-	V_{pp}
		2.5 V	-	2.85	-	-	2.05	-	V_{pp}
110	1.0000	1.8 V	-	3.39	-	-	2.44	-	V_{pp}
		2.5 V	-	3.39	-	-	2.44	-	V_{pp}
111	1.1430	1.8 V	(See Note 11)			-	2.79	-	V_{pp}
		2.5 V	-	3.88	-	-	2.79	-	V_{pp}

HEADPHONE OUTPUT POWER CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load $R_L = 16 \Omega$, $C_L = 10 \text{ pF}$ (see [Figure 3](#)).

Parameter			VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Power Into $R_L = 16 \Omega$									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	14	-	-	7	-	mW_{rms}
		2.5 V	-	14	-	-	7	-	mW_{rms}
001	0.4571	1.8 V	-	19	-	-	10	-	mW_{rms}
		2.5 V	-	19	-	-	10	-	mW_{rms}
010	0.5111	1.8 V	-	23	-	-	12	-	mW_{rms}
		2.5 V	-	23	-	-	12	-	mW_{rms}
011 (default)	0.6047	1.8 V	(Note 11)			-	17	-	mW_{rms}
		2.5 V	-	32	-	-	17	-	mW_{rms}
100	0.7099	1.8 V	(Note 11)			-	23	-	mW_{rms}
		2.5 V	-	44	-	-	23	-	mW_{rms}
101	0.8399	1.8 V	(Note 9, 11)			(Note 9)		mW_{rms}	
		2.5 V				-	32	-	mW_{rms}
110	1.0000	1.8 V	(Note 9, 11)					mW_{rms}	
		2.5 V						mW_{rms}	
111	1.1430	1.8 V	(Note 9, 11)					mW_{rms}	
		2.5 V						mW_{rms}	

8. One-half LSB of triangular PDF dither is added to data.
9. Full-scale output voltage and power is determined by the gain setting, G, in register “[Headphone Analog Gain \(HP_GAIN\[2:0\]\)](#)” on [page 57](#). High gain settings at certain VA and VA_HP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output, as shown in [Figures 27 - 30 on page 76](#).
10. See [Figure 3](#). R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.
11. VA_HP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the DAC may not achieve the full THD+N performance at full-scale output voltage and power.

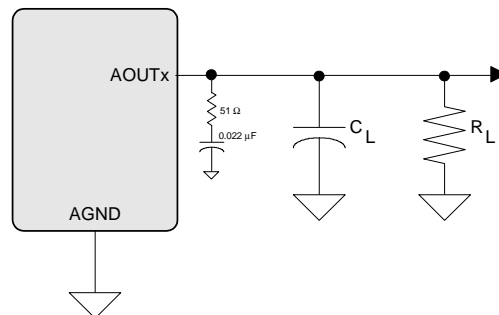


Figure 3. Headphone Output Test Load

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 12)	Min	Typ	Max	Unit	
Frequency Response 10 Hz to 20 kHz	-0.01	-	+0.08	dB	
Passband	to -0.05 dB corner	0	-	0.4780	Fs
	to -3 dB corner	0	-	0.4996	Fs
StopBand	0.5465	-	-	Fs	
StopBand Attenuation (Note 13)	50	-	-	dB	
Group Delay	-	10.4/Fs	-	s	
De-emphasis Error	Fs = 32 kHz	-	-	+1.5/+0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.25	dB
	Fs = 48 kHz	-	-	-0.2/-0.4	dB

Notes:

12. Response is clock dependent and will scale with Fs. Note that the response plots (Figure 38 to Figure 41 on page 82) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
13. Measurement Bandwidth is from Stopband to 3 Fs.

SWITCHING SPECIFICATIONS - SERIAL PORT

 (Inputs: Logic 0 = DGND, Logic 1 = VL, SDOUT C_{LOAD} = 15 pF.)

Parameters	Symbol	Min	Max	Units	
RESET pin Low Pulse Width (Note 14)		1	-	ms	
MCLK Frequency		1.024	38.4	MHz	
MCLK Duty Cycle (Note 15)		45	55	%	
Slave Mode					
Input Sample Rate (LRCK)	Quarter-Speed Mode	F _s	4	12.5	kHz
	Half-Speed Mode	F _s	8	25	kHz
	Single-Speed Mode	F _s	4	50	kHz
	Double-Speed Mode	F _s	50	100	kHz
LRCK Duty Cycle		45	55	%	
SCLK Frequency	1/t _p	-	64•F _s	Hz	
SCLK Duty Cycle		45	55	%	
LRCK Setup Time Before SCLK Rising Edge	t _{s(LK-SK)}	40	-	ns	
LRCK Edge to SDOUT MSB Output Delay	t _{d(MSB)}	-	52	ns	
SDOUT Setup Time Before SCLK Rising Edge	t _{s(SDO-SK)}	20	-	ns	
SDOUT Hold Time After SCLK Rising Edge	t _{h(SK-SDO)}	30	-	ns	
SDIN Setup Time Before SCLK Rising Edge	t _{s(SD-SK)}	20	-	ns	
SDIN Hold Time After SCLK Rising Edge	t _h	20	-	ns	

Parameters	Symbol	Min	Max	Units
Master Mode (Note 17)				
Output Sample Rate (LRCK)	All Speed Modes (Note 17) F_s	-	$\frac{MCLK}{128}$	Hz
LRCK Duty Cycle		45	55	%
SCLK Frequency	$1/t_p$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle		45	55	%
LRCK Edge to SDOUT MSB Output Delay	$t_{d(MSB)}$	-	52	ns
SDOUT Setup Time Before SCLK Rising Edge	$t_{s(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge	$t_{h(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge	$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge	t_h	20	-	ns

14. After powering up the CS42L51, \overline{RESET} should be held low after the power supplies and clocks are settled.
15. See “[Example System Clock Frequencies](#)” on page 79 for typical MCLK frequencies.
16. See
17. “[Master](#)” on page 39
18. “MCLK” refers to the external master clock applied.

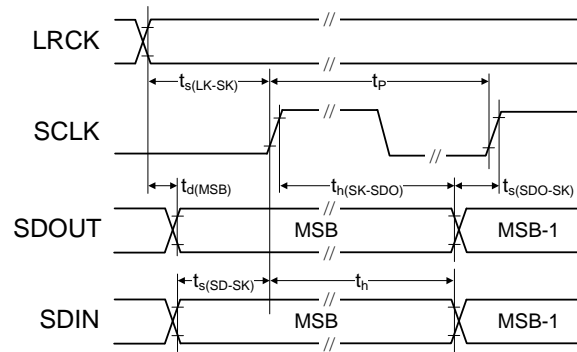


Figure 4. Serial Audio Interface Slave Mode Timing

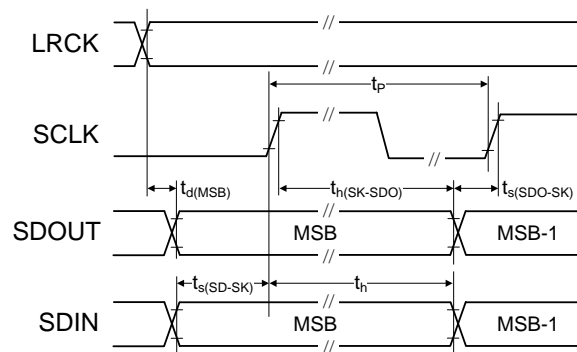


Figure 5. Serial Audio Interface Master Mode Timing

SWITCHING SPECIFICATIONS - I²C® CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDA C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
RESET Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	μ s
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	μ s
Clock Low time	t_{low}	4.7	-	μ s
Clock High Time	t_{high}	4.0	-	μ s
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	μ s
SDA Hold Time from SCL Falling	(Note 19) t_{hdd}	0	-	μ s
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	μ s
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	μ s
Acknowledge Delay from SCL Falling	t_{ack}	300	3450	ns

19. Data must be held for sufficient time to bridge the transition time, t_{fc} , of SCL.

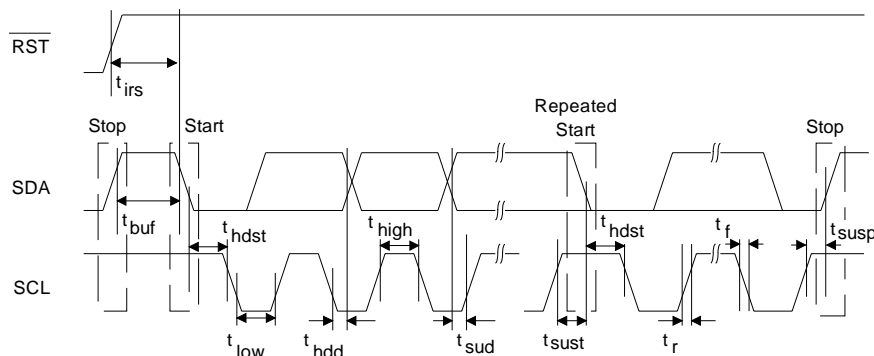


Figure 6. Control Port Timing - I²C

SWITCHING CHARACTERISTICS - SPI™ CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL)

Parameter	Symbol	Min	Max	Units
CCLK Clock Frequency	f_{sck}	0	6.0	MHz
RESET Rising Edge to CS Falling	t_{srs}	20	-	ns
CS Falling to CCLK Edge	t_{css}	20	-	ns
CS High Time Between Transmissions	t_{csh}	1.0	-	μ s
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	t_{f2}	-	100	ns

20. Data must be held for sufficient time to bridge the transition time of CCLK.

21. For $f_{sck} < 1$ MHz.

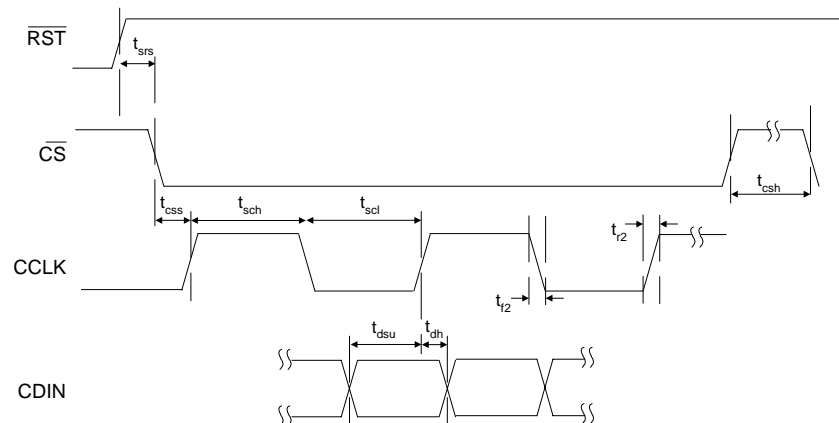


Figure 7. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters	Min	Typ	Max	Units	
VQ Characteristics					
Nominal Voltage	-	0.5•VA	-	V	
Output Impedance	-	23	-	kΩ	
DC Current Source/Sink (Note 22)	-	-	10	μA	
DAC_FILT+ Nominal Voltage	-	VA	-	V	
ADC_FILT+ Nominal Voltage	-	VA	-	V	
VSS_HP Characteristics					
Nominal Voltage	-	-0.8•(VA_HP)	-	V	
DC Current Source	-	-	10	μA	
MIC BIAS Characteristics					
Nominal Voltage	MICBIAS_LVL[1:0] = 00	-	0.8•VA	-	V
	MICBIAS_LVL[1:0] = 01	-	0.7•VA	-	V
	MICBIAS_LVL[1:0] = 10	-	0.6•VA	-	V
	MICBIAS_LVL[1:0] = 11	-	0.5•VA	-	V
DC Current Source	-	-	1	mA	
Power Supply Rejection Ratio (PSRR)	1 kHz	-	50	-	dB
Power Supply Rejection Ratio (PSRR) (Note 23)	1 kHz	-	60	-	dB

22. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through electrolytic de-coupling capacitors.

23. Valid with the recommended capacitor values on DAC_FILT+, ADC_FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 24)	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	μA
Input Capacitance		-	10	pF
1.8 V - 3.3 V Logic				
High-Level Output Voltage ($I_{OH} = -100 \mu A$)	V_{OH}	$V_L - 0.2$	-	V
Low-Level Output Voltage ($I_{OL} = 100 \mu A$)	V_{OL}	-	0.2	V
High-Level Input Voltage	V_{IH}	0.68•VL	-	V
Low-Level Input Voltage	V_{IL}	-	0.32•VL	V

24. See “Digital I/O Pin Characteristics” on page 9 for serial and control port power rails.

POWER CONSUMPTION

See (Note 25)

	Operation	Power Ctl. Registers							Typical Current (mA)				Total Power (mW _{rms})					
		02h				03h			V	i _{VA_HP}	i _{VA}	i _{VD}		i _{VL} (Note 28)				
		PDN_DACB	PDN_DACA	PDN_PGAB	PDN_PGAA	PDN_ADCB	PDN_ADCA	PDN_PDN							PDN_MICB	PDN_MICA	PDN_MICBIAS	
1	Off (Note 26)	x	x	x	x	x	x	x	x	x	x	1.8	0	0	0	0	0	
												2.5	0	0	0	0	0	
2	Standby (Note 27)	x	x	x	x	x	x	1	x	x	x	1.8	0	0.01	0.02	0	0.05	
												2.5	0	0.01	0.03	0	0.10	
3	Mono Record	ADC	1	1	1	1	1	0	0	1	1	1	1.8	0	1.85	2.03	0.03	7.05
													2.5	0	2.07	3.05	0.05	12.94
		PGA to ADC	1	1	1	0	1	0	0	1	1	1	1.8	0	2.35	2.03	0.03	7.95
												2.5	0	2.58	3.08	0.05	14.29	
			MIC to PGA to ADC (with Bias)	1	1	1	0	1	0	0	1	0	0	1.8	0	3.67	2.05	0.03
											2.5	0	3.95	3.09	0.05	17.71		
		MIC to PGA to ADC (no Bias)	1	1	1	0	1	0	0	1	0	1	1.8	0	3.27	2.03	0.03	9.61
												2.5	0	3.52	3.08	0.05	16.62	
4	Stereo Record	ADC	1	1	1	1	0	0	0	1	1	1	1.8	0	2.69	2.12	0.03	8.72
													2.5	0	2.93	3.18	0.04	15.40
		PGA to ADC	1	1	0	0	0	0	0	1	1	1	1.8	0	3.65	2.12	0.03	10.45
												2.5	0	3.91	3.17	0.04	17.84	
		MIC to PGA to ADC (no Bias)	1	1	0	0	0	0	0	0	0	1	1.8	0	5.48	2.11	0.03	13.73
												2.5	0	5.76	3.17	0.04	22.45	
5	Mono Playback		1	0	1	1	1	1	0	1	1	1	1.8	1.66	1.40	2.35	0.01	9.74
													2.5	2.03	1.71	3.48	0.02	18.08
6	Stereo Playback		0	0	1	1	1	1	0	1	1	1	1.8	2.77	2.05	2.35	0.01	12.93
													2.5	3.21	2.50	3.49	0.02	23.02
7	Mono Record & Playback PGA in (no MIC) to Mono Out		1	0	1	0	1	0	0	1	1	1	1.8	1.66	3.63	2.73	0.03	14.49
													2.5	2.03	4.16	4.08	0.05	25.79
8	Phone Monitor MIC (w/bias) in to Mono Out		1	0	1	0	1	0	0	1	0	0	1.8	1.66	4.95	2.75	0.03	16.90
													2.5	2.03	5.52	4.08	0.05	29.20
9	Stereo Record & Playback PGA in (no MIC) to Stereo Out		0	0	0	0	0	0	0	1	1	1	1.8	2.77	5.59	2.82	0.03	20.18
													2.5	3.21	6.28	4.19	0.04	34.30

25. Unless otherwise noted, test conditions are as follows: All zeros input, slave mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation.

26. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.

27. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.

28. VL current will slightly increase in master mode.

4. APPLICATIONS

4.1 Overview

4.1.1 Architecture

The CS42L51 is a highly integrated, low power, 24-bit audio CODEC comprised of stereo analog-to-digital converters (ADC), and stereo digital-to-analog converters (DAC) designed using multi-bit delta-sigma techniques. The DAC operates at an oversampling ratio of 128Fs and the ADC operates at 64Fs, where Fs is equal to the system sample rate. The different clock rates maximize power savings while maintaining high performance. The CODEC operates in one of four sample rate speed modes: Quarter, Half, Single and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

4.1.2 Line & MIC Inputs

The analog input portion of the CODEC allows selection from and configuration of multiple combinations of stereo and microphone (MIC) sources. Six line inputs with configuration for two MIC inputs (or one MIC input with common mode rejection), two MIC bias outputs and independent channel control (including a high-pass filter disable function) are available. A Programmable Gain Amplifier (PGA), MIC boost, and Automatic Level Control (ALC), with noise gate settings, provide analog gain and adjustment. Digital volume controls, including gain, boost, attenuation and inversion are also available.

4.1.3 Line & Headphone Outputs

The analog output portion of the D/A includes a headphone amplifier capable of driving headphone and line-level loads. An on-chip charge pump creates a negative headphone supply allowing a full-scale output swing centered around ground. This eliminates the need for large DC-Blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages. Eight gain settings for the headphone amplifier are available.

4.1.4 Signal Processing Engine

A signal processing engine is available to process serial input D/A data before output to the DAC. The D/A data has independent volume controls and mixing functions such as mono mixes and left/right channel swaps. A Tone Control provides bass and treble at four selectable corner frequencies. An automatic level control provides limiting capabilities at programmable attack and release rates, maximum thresholds and soft ramping. A 15/50 μ s de-emphasis filter is also available at a 44.1 kHz sample rate.

4.1.5 Beep Generator

A beep may be generated internally at select frequencies across approximately two octave major scales and configured to occur continuously, periodically or at single time intervals controlled by the user. Volume may be controlled independently.

4.1.6 Device Control (Hardware or Software Mode)

In Software Mode, all functions and features may be controlled via a two-wire I²C or three-wire SPI control port interface. In Hardware Mode, a limited feature set may be controlled via stand-alone control pins.

4.1.7 Power Management

Two Software Mode control registers provide independent power-down control of the ADC, DAC, PGA, MIC pre-amp and MIC bias, allowing operation in select applications with minimal power consumption.

4.2 Hardware Mode

A limited feature-set is available when the CODEC powers up in Hardware Mode (see [“Recommended Power-Up Sequence” on page 41](#)) and may be controlled via stand-alone control pins. [Table 2](#) shows a list of functions/features, the default configuration and the associated stand-alone control available.

Hardware Mode Feature/Function Summary				
Feature/Function		Default Configuration	Stand-Alone Control	Note
Power Control	CODEC PGAx ADCx DACx MIC Bias MICx Pre-amplifier	Powered Up Powered Up Powered Up Powered Up Powered Down Powered Down	-	-
Auto-Detect		Enabled	-	-
Speed Mode	Serial Port Slave Serial Port Master	Auto-Detect Speed Mode Single-Speed Mode	-	-
MCLK Divide		(Selectable)	“MCLKDIV2” pin 2	see Section 4.5 on page 38
Serial Port Master / Slave Selection		(Selectable)	“M/S” pin 29	see Section 4.5 on page 38
Interface Control	ADC DAC	(Selectable)	“I ² S/LJ” pin 3	see Section 4.6 on page 40
ADC Volume & Gain	Digital Boost Soft Ramp Zero Cross Invert PGAx Attenuator ALC Noise Gate	Disabled Disabled Disabled Disabled 0 dB 0 dB Disabled Disabled	-	-
ADCx High-Pass Filter ADCx High-Pass Filter Freeze		Enabled Continuous DC Subtraction	-	-
Line/MIC Input Select		AIN1A to PGAA AIN1B to PGAB	-	-
DAC Volume & Gain	HP Gain AOUTx Volume Invert Soft Ramp Zero Cross	G = 0.6047 0 dB Disabled Enabled Disabled	-	-
DAC De-Emphasis		(Selectable)	“DEM” pin 4	see Section on page 34
Signal Processing Engine (SPE)	Mix Beep Tone Control Peak Detect and Limiter	Disabled Disabled Disabled Disabled	-	-
Data Selection		Data Input (PCM) to DAC	-	-
Channel Mix	ADC DAC	ADCA = L; ADCB = R PCMA = L; PCMB = R	-	-
Charge Pump Frequency		(64xFs)/7	-	-

Table 2. Hardware Mode Feature Summary

4.3 Analog Inputs

AINxA and AINxB are the analog inputs, internally biased to VQ, that accepts line-level and MIC-level signals, allowing various gain and signal adjustments for each channel.

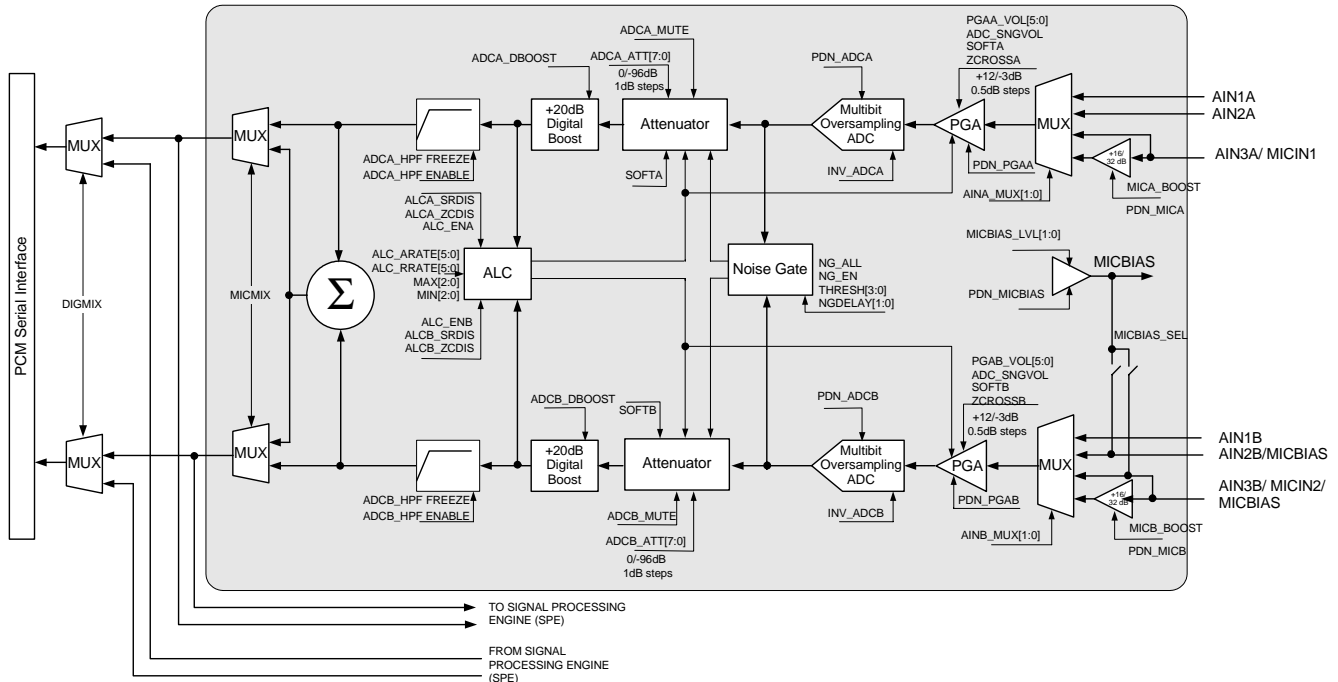


Figure 8. Analog Input Architecture

4.3.1 Digital Code, Offset & DC Measurement

The ADC output data is in two's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFFH or 800000H, respectively and cause the ADC overflow bit to be set to a '1'.

Given the two's complement format, low-level signals may cause the MSB of the serial data to periodically toggle between '1' and '0', possibly introducing noise into the system as the bit switches back and forth. To prevent this phenomena, a constant DC offset is added to the serial data bringing the low-level signal just above the point at which the MSB would normally toggle, thus reducing the noise introduced. Note that this offset is not removed (refer to "Analog Input Characteristics (Commercial - CNZ)" on page 13 and/or "Analog Input Characteristics (Automotive - DNZ)" on page 14 for the specified offset level).

The CODEC may be used to measure DC voltages by disabling the high-pass filter for the designated channel. DC levels are measured relative to VQ and will be decoded as positive two's complement binary numbers above VQ and negative two's complement binary numbers below VQ.

Software Controls:	"Status (Address 20h) (Read Only)" on page 73, "ADC Control (Address 06h)" on page 54.
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4.3.2 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the high-pass filter is “frozen” during normal operation, the current value of the DC offset for the corresponding channel is held. It is this DC offset that will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CODEC with the high-pass filter enabled and the DC offset not “frozen” until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Freezing the DC offset.

The high-pass filters are controlled using the ADCx_HPFRZ and ADCx_HPFEN bits.

If a particular ADC channel is used to measure DC voltages, the high-pass filter may be disabled using the ADCx_HPFEN bit.

Software Controls:	“ADC Control (Address 06h)” on page 54.
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4.3.3 Digital Routing

The digital output of the ADC may be internally routed to the signal processing engine (SPE) for playback of analog input signals. Volume to the DAC may be controlled using the ADCMIX[6:0] bits. The serial input data may also be routed to the ADC serial interface using the DIGMIX bit. This is useful for recording a digital mix along with the analog input.

Software Controls:	“ADCx Mixer Volume Control: ADCA (Address 0Eh) & ADCB (Address 0Fh)” on page 61, “Interface Control (Address 04h)” on page 52.
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4.3.4 Differential Inputs

The stereo pair inputs act as a single differential input when the MICMIX bit is enabled. This provides common mode rejection of noise in digitally intense PCB’s where the microphone signal traverses long traces, or across long microphone cables as illustrated in [Figure 9](#).

Since the mixer provides a differential combination of the two signals, the potential input mix may exceed the maximum full-scale input and result in clipping. The level out of the mixer, therefore, is automatically attenuated 6 dB. Gain may be applied using either the analog PGA or MIC Pre-amp or the digital ADCMIX volume control to re-adjust a small signal to desired levels.

The analog inputs may also be used as a differential input pair as illustrated in [Figure 10](#). The two channels are differentially combined when the MICMIX bit is enabled.

4.3.4.1 External Passive Components

The microphone input is internally biased to VQ. Input signals must be AC coupled using external capacitors with values consistent with the desired high-pass filter design. The MICINx input resistance of 50 kΩ may be combined with an external capacitor of 1 μF to achieve the cutoff frequency defined by the equation,

An electrolytic capacitor must be placed such that the positive terminal is positioned relative to the side with the greater bias voltage. The MICBIAS voltage level is controlled by the MICBIAS_LVL[1:0] bits.

$$f_c = \frac{1}{2\pi(50 \text{ k}\Omega)(1 \text{ }\mu\text{F})} = 3.18 \text{ Hz}$$

The MICBIAS series resistor must be selected based on the requirements of the particular microphone used. The MICBIAS output pin is selected using the MICBIAS_SEL bit.

Software Controls:	"Interface Control (Address 04h)" on page 52, "MIC Control (Address 05h)" on page 53.
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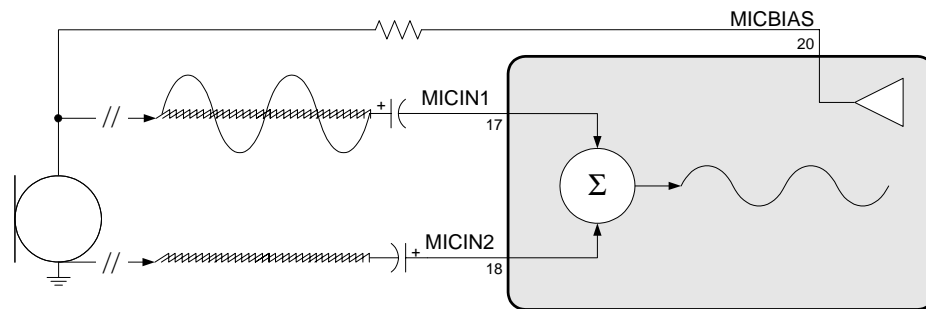


Figure 9. MIC Input Mix w/Common Mode Rejection

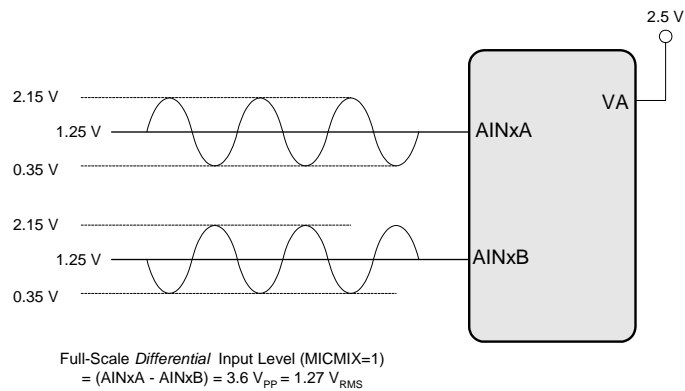


Figure 10. Differential Input

4.3.5 Analog Input Multiplexer

A stereo 4-to-1 analog input multiplexer selects between a line-level input source, or a mic-level input source, depending on the PDN_PGAX and AINx_MUX[1:0] bit settings. Signals may be routed to or bypassed around the PGA. To conserve power, the PGA's may be powered down allowing the user to select from multiple line-level sources and route the stereo signal directly to the ADC. When using the MIC pre-amp, however, the PGA must be powered up.

Analog input channel B may also be used as an output for the MIC bias voltage. The MICBIAS_SEL bit routes the bias voltage to either of two pins. The multiplexer must then select from the remainder of the two input channels.

The ADC, PGA and MIC pre-amplifier each has an associated input resistance. When selecting between these paths, the input resistance to the CODEC will change accordingly. Refer to the input resistance characteristics in the [Characteristic and Specification Tables](#) for the input resistance of each path.

Software Controls:	“Power Control 1 (Address 02h)” on page 49, “MIC Control (Address 05h)” on page 53 “ADCx Input Select, Invert & Mute (Address 07h)” on page 56.
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4.3.6 MIC & PGA Gain

The MIC-level input passes through a +16 dB or +32 dB analog gain stage prior to the input multiplexer, allowing it to be used for microphone level signals without the need for any external gain. The PGA must be powered up when using the MIC pre-amp.

The PGA stage provides an additional +12 dB to -3 dB of analog gain in 0.5 dB steps.

Software Controls:	“Power Control 1 (Address 02h)” on page 49, “ADCx Input Select, Invert & Mute (Address 07h)” on page 56, “ALCX & PGAX Control: ALCA, PGAA (Address 0Ah) & ALCB, PGAB (Address 0Bh)” on page 59, “MIC Control (Address 05h)” on page 53.
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4.3.7 Automatic Level Control (ALC)

When enabled, the ALC monitors the analog input signal after the digital attenuator, detects when peak levels exceed the maximum threshold settings and lowers, first, the PGA gain settings and then increases the digital attenuation levels at a programmable attack rate and maintains the resulting level below the maximum threshold.

When input signal levels fall below the minimum threshold, digital attenuation levels are decreased first and the PGA gain is then increased at a programmable release rate and maintains the resulting level above the minimum threshold.

Attack and release rates are affected by the ADC soft ramp/zero cross settings and sample rate, Fs. ALC soft ramp and zero cross dependency may be independently enabled/disabled.

Recommended settings: Best level control may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. **Note: 1.)** The maximum realized gain must be set in the PGAx_VOL register. The ALC will only apply the gain set in the PGAx_VOL. **2.)** The ALC maintains the output signal between the MIN and MAX thresholds. As the input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds.

Software Controls:	“ALC Enable & Attack Rate (Address 1Ch)” on page 70 , “ALC Release Rate (Address 1Dh)” on page 71 , “ALC Threshold (Address 1Eh)” on page 71 , “ALCX & PGAX Control: ALCA, PGAA (Address 0Ah) & ALCB, PGAB (Address 0Bh)” on page 59 .
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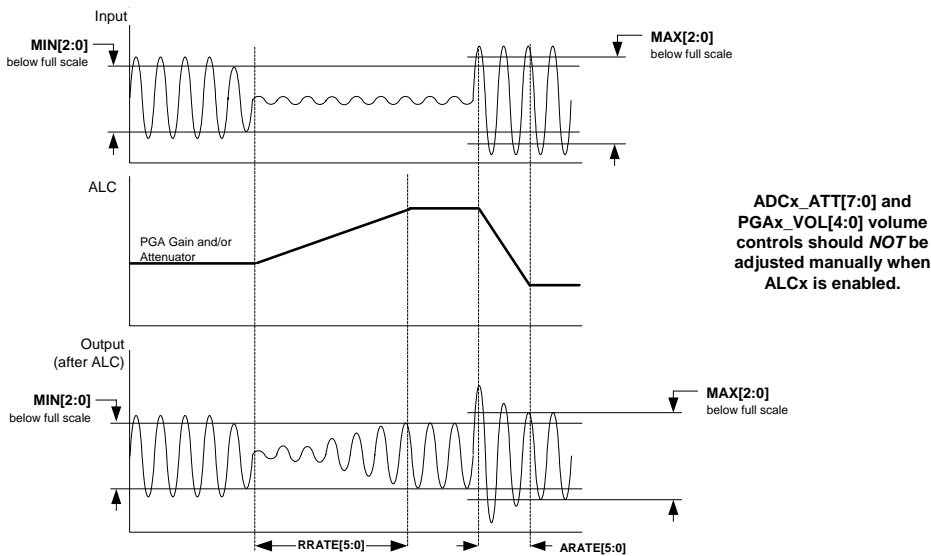


Figure 11. ALC

4.3.8 Noise Gate

The noise gate may be used to mute signal levels that fall below a programmable threshold. This prevents the ALC from applying gain to noise. A programmable delay may be used to set the minimum time before the noise gate attacks the signal.

Maximum noise gate attenuation levels will depend on the gain applied in either the PGA or MIC pre-amplifier. For example: If both +32 dB pre-amplification and +12 dB programmable gain is applied, the maximum attenuation that the noise gate achieves will be 52 dB (-96 + 32 + 12) below full-scale.

Ramp-down time to the maximum setting is affected by the SOFTx bit.

Recommended settings: For best results, enable soft ramp for the digital attenuator. When the analog inputs are configured for differential signals (see “Differential Inputs” on page 29), enable the NG_ALL bit to trigger the noise gate only when *both* inputs fall below the threshold.

Software Controls:	“Noise Gate Configuration & Misc. (Address 1Fh)” on page 72, “ADC Control (Address 06h)” on page 54.
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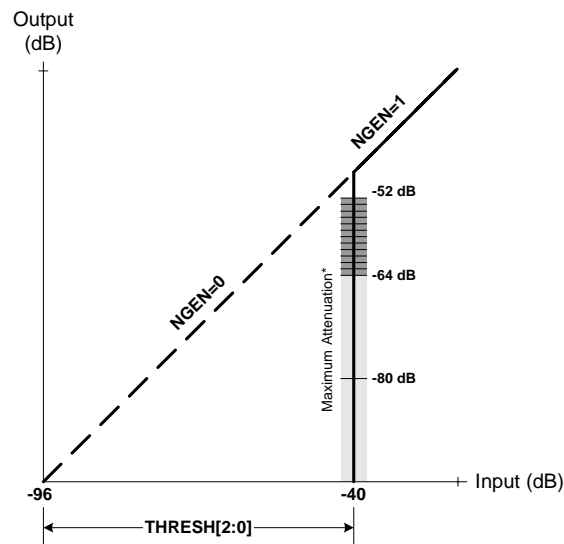


Figure 12. Noise Gate Attenuation

4.4 Analog Outputs

AOUTA and AOUTB are the ground-centered line or headphone outputs. Various signal processing options are available, including digital mixes with the ADC signal and an internal Beep Generator. The desired path to the DAC must be selected using the DATA_SEL[1:0] bits.

Software Controls:	“DAC Control (Address 09h)” on page 58.
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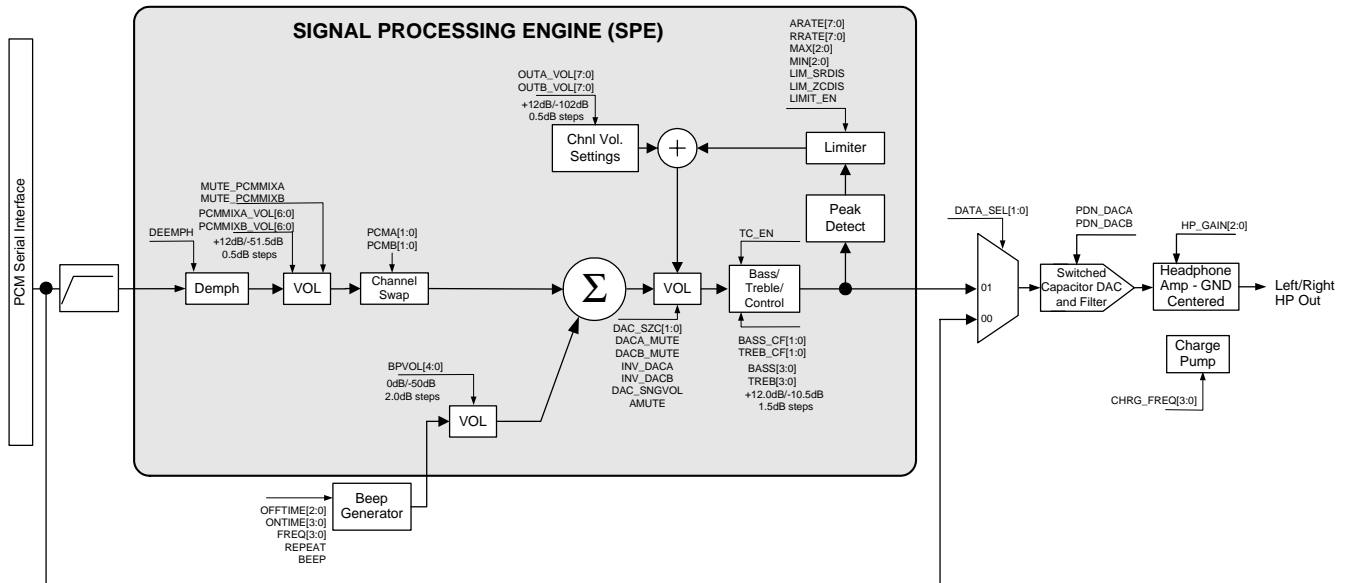


Figure 13. Output Architecture

4.4.1 De-Emphasis Filter

The CODEC includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in Figure 14. The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 μ s pre-emphasis equalization as a means of noise reduction. De-emphasis is only available in Single-Speed Mode.

Software Controls:	“DAC Control (Address 09h)” on page 58.		
Hardware Control:	Pin	Setting	Selection
	“DEM” pin 4.	LO	No De-Emphasis
		HI	De-Emphasis Applied

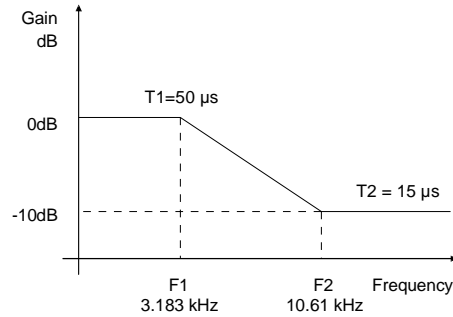


Figure 14. De-Emphasis Curve

4.4.2 Volume Controls

Three digital volume control functions are implemented, offering independent control over the ADC and PCM signal paths into the mixer as well as a combined control over the mixed signals. All volume controls are programmable to ramp in increments of 0.125 dB at a rate controlled by the DAC soft ramp/zero cross settings.

All signal paths may also be independently muted via mute control bits. When enabled, each bit attenuates the signal to its maximum value. When the mute bit is disabled, the signal returns to the attenuation level set in the respective volume control register. The attenuation is ramped up and down at the rate specified by the DAC_SZC[1:0] bits.

Software Controls:	“ADCx Mixer Volume Control: ADCA (Address 0Eh) & ADCB (Address 0Fh)” on page 61 , “PCMX Mixer Volume Control: PCMA (Address 10h) & PCMB (Address 11h)” on page 62 , “AOUTx Volume Control: AOUTA (Address 16h) & AOUTB (Address 17h)” on page 66 , “DAC Output Control (Address 08h)” on page 57 .
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4.4.3 Mono Channel Mixer

A channel mixer may be used to create a mix of the left and right channels for either the PCM or ADC signals. This mix allows the user to produce a MONO signal from a stereo source. The mixer may also be used to implement a left/right channel swap.

Software Controls:	“PCM Channel Mixer (Address 18h)” on page 67 .
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4.4.4 Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple and single (one-shot) beeps. Sixteen on and eight off times are available.

Note: The Beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be required to set the Beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, AOUTx_VOL[7:0], will affect the Beep volume, DAC volume may alternatively be controlled using the PCMMIXx_VOL[6:0] bits.

Software Controls:	“Beep Frequency & Timing Configuration (Address 12h)” on page 62 , “Beep Off Time & Volume (Address 13h)” on page 63 , “Beep Configuration & Tone Configuration (Address 14h)” on page 64
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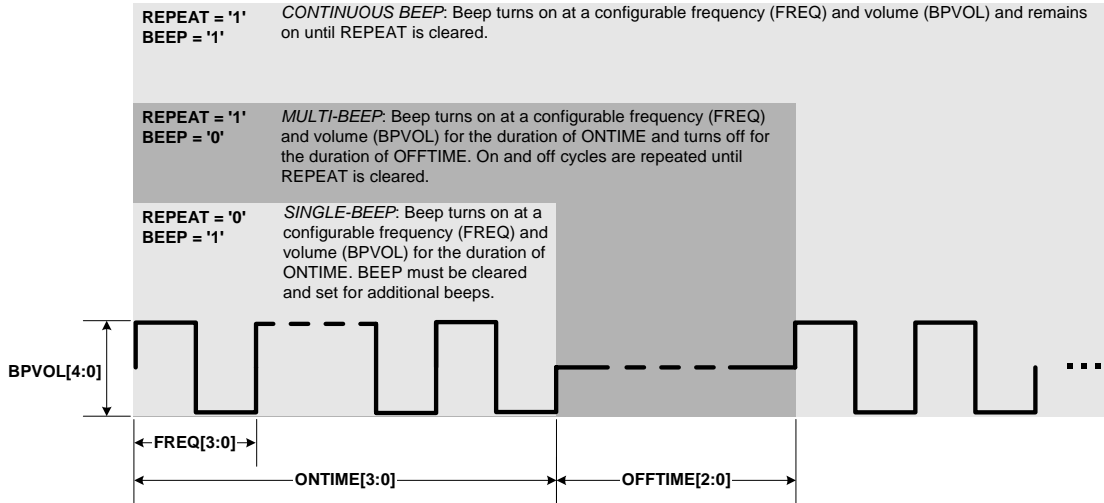


Figure 15. Beep Configuration Options

4.4.5 Tone Control

Shelving filters are used to implement bass and treble (boost and cut) with four selectable corner frequencies. Boosting will affect peak detect and limiting when levels exceed the maximum threshold settings.

Software Controls:	"Tone Control (Address 15h)" on page 65.
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4.4.6 Limiter

When enabled, the limiter monitors the digital input signal before the DAC modulator, detects when levels exceed the maximum threshold settings and lowers the AOUT volume at a programmable attack rate below the maximum threshold. When the input signal level falls below the maximum threshold, the AOUT volume returns to its original level set in the Volume Control register at a programmable release rate. Attack and release rates are affected by the DAC soft ramp/zero cross settings and sample rate, Fs. Limiter soft ramp and zero cross dependency may be independently enabled/disabled.

Recommended settings: Best limiting performance may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. The "cushion" bits allow the user to set a threshold slightly below the maximum threshold for hysteresis control - this cushions the sound as the limiter attacks and releases.

Note:

1. When the Limiter is enabled, the AOUT Volume is automatically controlled and should not be adjusted manually. Alternative volume control may be realized using the PCMMIXx_VOL[6:0] bits.
2. The Limiter maintains the output signal between the CUSH and MAX thresholds. As the digital input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds.

Software Controls:	"Limiter Release Rate Register (Address 1Ah)" on page 69, "Limiter Attack Rate Register (Address 1Bh)" on page 70, "DAC Control (Address 09h)" on page 58
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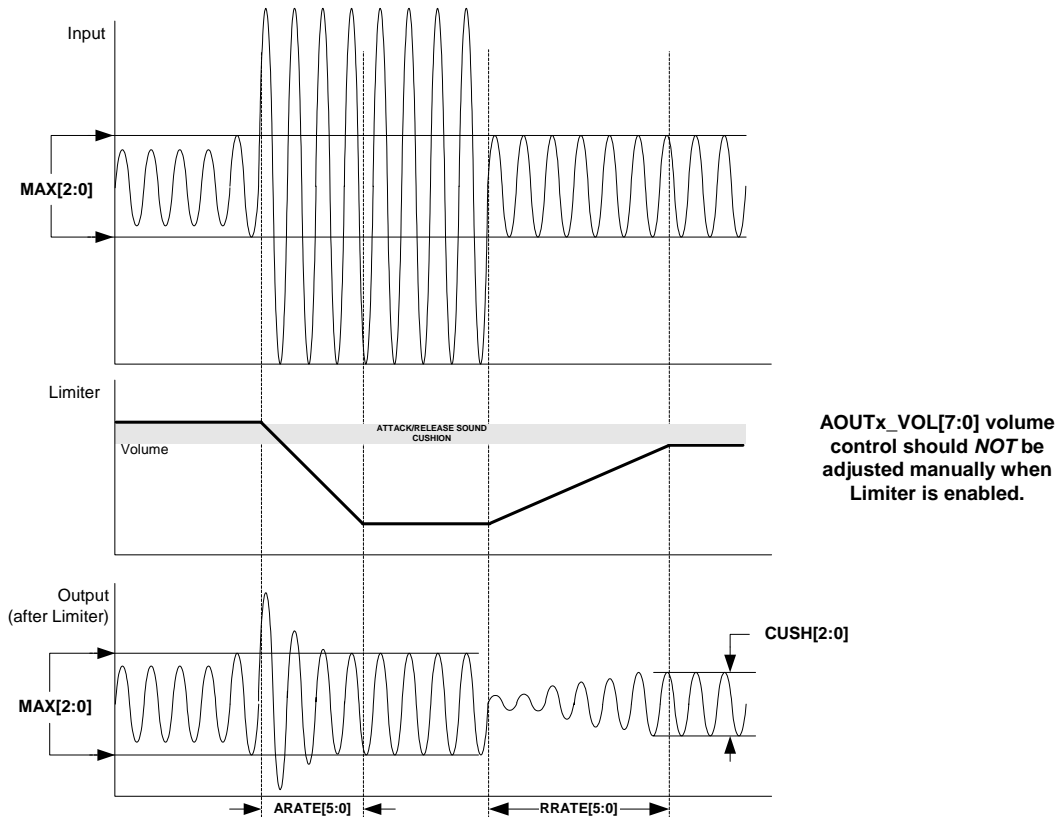


Figure 16. Peak Detect & Limiter

4.4.7 Line-Level Outputs and Filtering

The CODEC contains on-chip buffer amplifiers capable of producing line level single-ended outputs on AOUTA and AOUTB. These amplifiers are ground centered and do not have any DC offset. A load stabilizer circuit, shown in the [“Typical Connection Diagram \(Software Mode\)”](#) on page 10 and the [“Typical Connection Diagram \(Hardware Mode\)”](#) on page 11, is required on the analog outputs. This allows the DAC amplifiers to drive line or headphone outputs.

Also shown in the Typical Connection diagrams is the recommended passive output filter to support higher impedances such as those found on the inputs to operational amplifiers. “Rext”, shown in the typical connection diagrams, is the input impedance of the receiving device.

The invert and digital gain controls may be used to provide phase and/or amplitude compensation for an external filter.

The delta-sigma conversion process produces high frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low pass filter.

Software Controls:	“DAC Output Control (Address 08h)” on page 57, “AOUTx Volume Control: AOUTA (Address 16h) & AOUTB (Address 17h)” on page 66.
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4.4.8 On-Chip Charge Pump

An on-chip charge pump derives a negative supply voltage from the VA_HP supply. This provides dual rail supplies allowing a full-scale output swing centered around ground and eliminates the need for large, DC-blocking capacitors. Added benefits include greater pop suppression and improved low frequency (bass) response. **Note:** Series resistance in the path of the power supplies must be avoided. Any voltage drop on the VA_HP supply will directly impact the derived negative voltage on the charge pump supply, VSS_HP, and may result in clipping.

The FLYN and FLYP pins connect to internal switches that charges and discharges the external capacitor attached, at a default switching frequency. This frequency may be adjusted in the control port registers. Increasing the charge-pumping capacitor will slightly decrease the pumping frequency. The capacitor connected to VSS_HP acts as a charge reservoir for the negative supply as well as a filter for the ripple induced by the charge pump. Increasing this capacitor will decrease the ripple on VSS_HP. Refer to the typical connection diagrams in [Figure 1 on page 10](#) or [Figure 2 on page 11](#) for the recommended capacitor values for the charge pump circuitry.

Software Controls:	"Charge Pump Frequency (Address 21h)" on page 74.
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4.5 Serial Port Clocking

The CODEC serial audio interface port operates either as a slave or master. It accepts externally generated clocks in slave mode and will generate synchronous clocks derived from an input master clock (MCLK) in master mode.

The frequency of the MCLK must be an integer multiple of, and synchronous with, the system sample rate, Fs. The LRCK frequency is equal to Fs, the frequency at which audio samples for each channel are clocked into or out of the device.

The SPEED and MCLKDIV2 software control bits or the SDOUT/(M \bar{S}) and MCLKDIV2 stand-alone control pins, configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. The value on the SDOUT pin is latched immediately after powering up in Hardware Mode.

Software Control:	"MIC Power Control & Speed Control (Address 03h)" on page 50, "DAC Control (Address 09h)" on page 58.		
Hardware Control:	Pin	Setting	Selection
	"SDOUT, M \bar{S} " pin 29	47 k Ω Pull-down	Slave
		47 k Ω Pull-up	Master
	"MCLKDIV2" pin 2	LO	No Divide
HI		MCLK is divided by 2 prior to all internal circuitry.	

4.5.1 Slave

LRCK and SCLK are inputs in Slave Mode. The speed of the CODEC is automatically determined based on the input MCLK/LRCK ratio when the Auto-Detect function is enabled. Certain input clock ratios will then require an internal divide-by-two of MCLK* using either the MCLKDIV2 bit or the MCLKDIV2 stand-alone control pin.

Additional clock ratios are allowed when the Auto-Detect function is disabled; but the appropriate speed mode must be selected using the SPEED[1:0] bits.

Auto-Detect	QSM	HSM	SSM	DSM
Disabled (Software Mode only)	512, 768, 1024, 1536, 2048, 3072	256, 384, 512, 768, 1024, 1536	128, 192, 256, 384, 512, 768	128, 192, 256, 384
Enabled	1024, 1536, 2048*, 3072*	512, 768, 1024*, 1536*	256, 384, 512*, 768*	128, 192, 256*, 384*

*MCLKDIV2 must be enabled.

Table 3. MCLK/LRCK Ratios

4.5.2 Master

LRCK and SCLK are internally derived from the internal MCLK (after the divide, if MCLKDIV2 is enabled). In Hardware Mode the CODEC operates in single-speed only. In Software Mode, the CODEC operates in either quarter-, half-, single- or double-speed depending on the setting of the SPEED[1:0] bits.

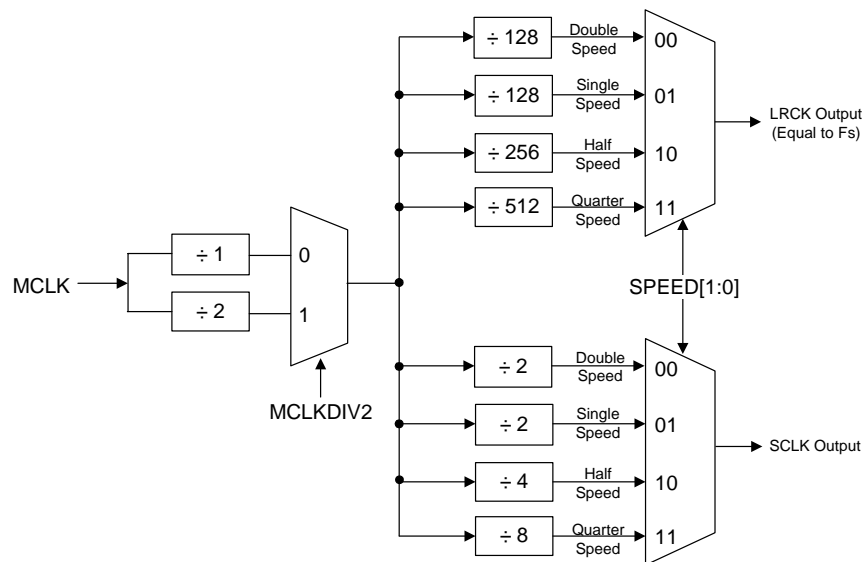


Figure 17. Master Mode Timing

4.5.3 High-Impedance Digital Output

The serial port may be placed on a clock/data bus that allows multiple masters for the serial port I/O without the need for external buffers. The 3ST_SP bit places the internal buffers for these I/O in a high-impedance state, allowing another device to transmit serial port data without bus contention.

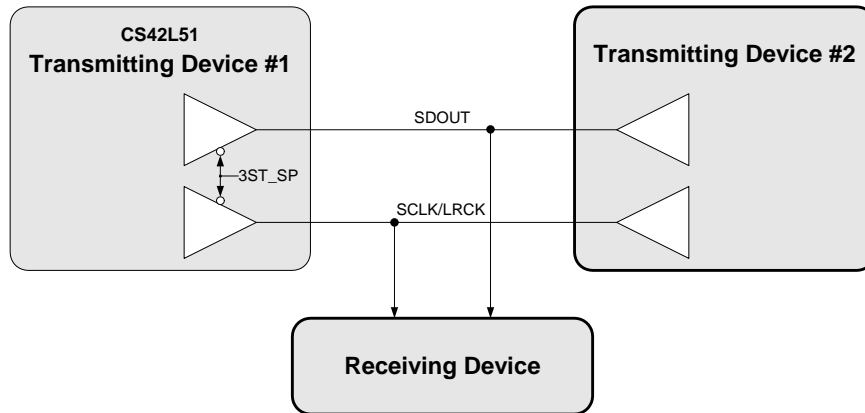


Figure 18. Tri-State Serial Port

4.5.4 Quarter- and Half-Speed Mode

Quarter-Speed Mode (QSM) and Half-Speed Mode (HSM) allow lower sample rates while maintaining a relatively flat noise floor in the typical audio band of 20 Hz - 20 kHz. Single-Speed Mode (SSM) will allow lower frequency sample rates; however, the DAC's noise floor, that normally rises out-of-band, will scale with the lower sample rate and begin to rise within the audio band. QSM and HSM corrects for most of this scaling, effectively increasing the dynamic range of the CODEC at lower sample rates, relative to SSM.

4.6 Digital Interface Formats

The serial port operates in standard I²S, Left-Justified or Right-Justified (DAC only) digital interface formats with varying bit depths from 16 to 24. Data is clocked out of the ADC or into the DAC on the rising edge of SCLK. Figures 19-21 illustrate the general structure of each format. Refer to “Switching Specifications - Serial Port” on page 20 for exact timing relationship between clocks and data.

Software Control:	“Interface Control (Address 04h)” on page 52.		
Hardware Control:	Pin	Setting	Selection
	“I ² S/LJ” pin 3	LO	Left-Justified Interface
		HI	I ² S Interface

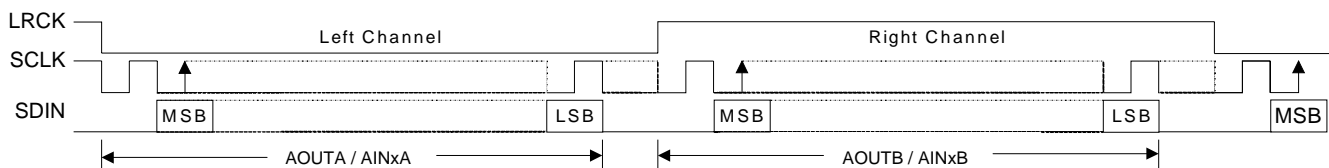


Figure 19. I²S Format

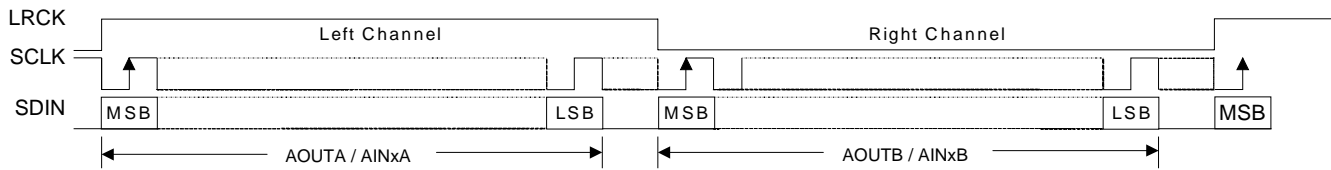


Figure 20. Left-Justified Format

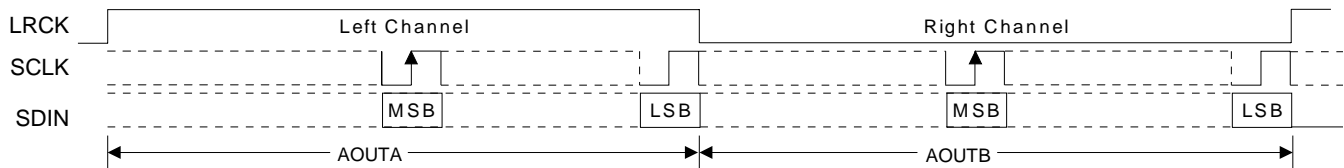


Figure 21. Right-Justified Format (DAC only)

4.7 Initialization

The initialization and Power-Down sequence flowchart is shown in [Figure 22 on page 42](#). The CODEC enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma modulators and control port registers are reset. The internal voltage reference, multi-bit DAC and ADC and switched-capacitor low-pass filters are powered down.

The device will remain in the Power-Down state until the $\overline{\text{RESET}}$ pin is brought high. The control port is accessible once $\overline{\text{RESET}}$ is high and the desired register settings can be loaded per the interface descriptions in [“Software Mode” on page 43](#). If a valid write sequence to the control port is not made within approximately 10 ms, the CODEC will enter Hardware Mode.

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage references, DAC_FILT+ and ADC_FILT+ will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

4.8 Recommended Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable.
2. Bring $\overline{\text{RESET}}$ high. After approximately 10 ms, the device will enter Hardware Mode.
3. For Software Mode operation, set the PDN bit to ‘1’b in under 10 ms. This will place the device in “stand-by”.
4. Load the desired register settings while keeping the PDN bit set to ‘1’b.
5. Start MCLK to the appropriate frequency, as discussed in [Section 4.5](#).
6. Set the PDN bit to ‘0’b.
7. Apply LRCK, SCLK and SDIN for normal operation to begin.
8. Bring $\overline{\text{RESET}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.9 Recommended Power-Down Sequence

To minimize audible pops when turning off or placing the CODEC in standby,

1. Mute the DAC's and ADC's.
2. Set the PDN bit in the power control register to '1'b. The CODEC will not power down until it reaches a fully muted state. Do not remove MCLK until after the part has fully muted. Note that it may be necessary to disable the soft ramp and/or zero cross volume transitions to achieve faster muting/power down.
3. Bring $\overline{\text{RESET}}$ low.

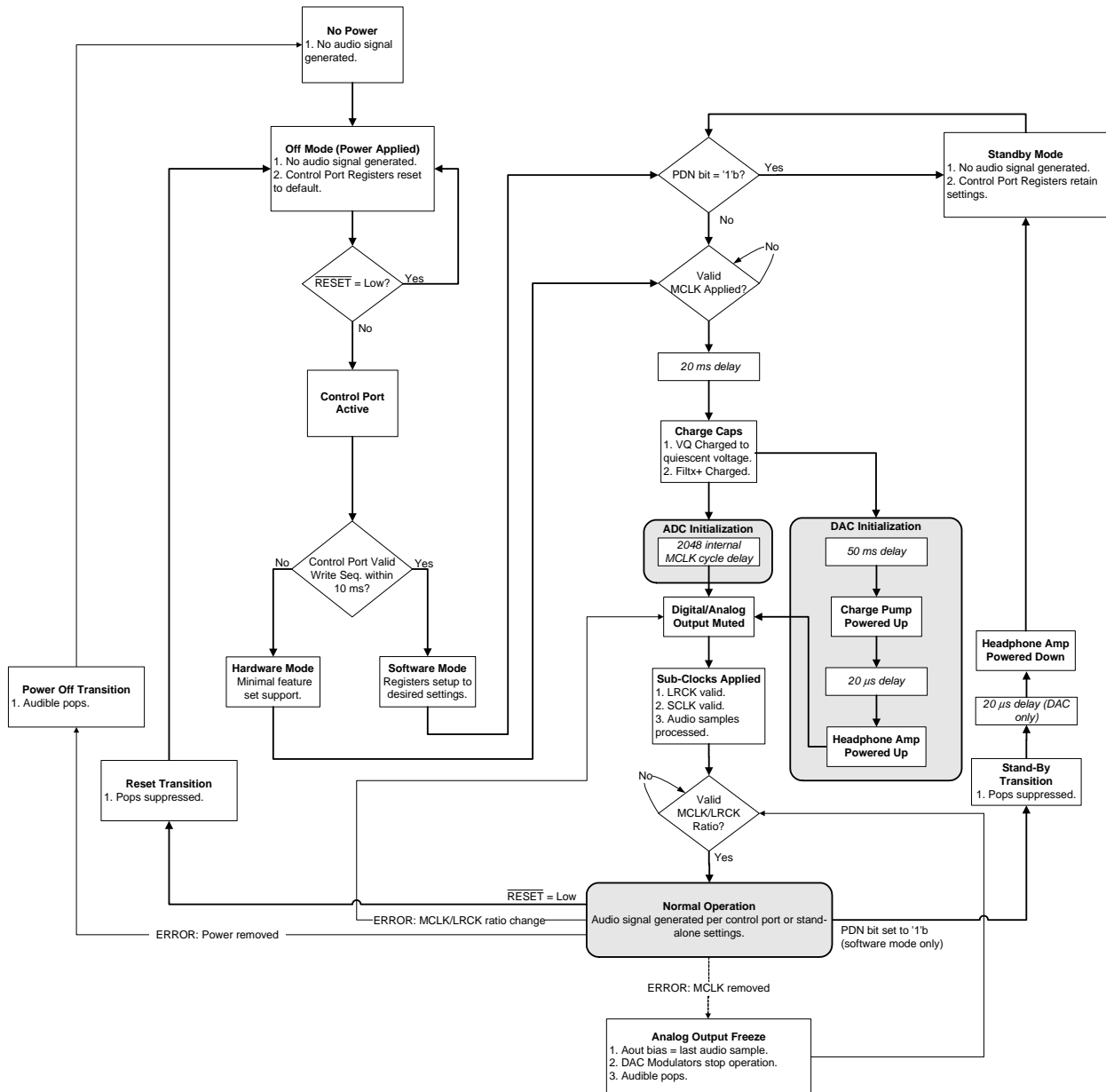


Figure 22. Initialization Flowchart

4.10 Software Mode

The control port is used to access the registers allowing the CODEC to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in two modes: SPI and I²C, with the CODEC acting as a slave device. Software Mode is selected if there is a high-to-low transition on the AD0/ $\overline{\text{CS}}$ pin after the $\overline{\text{RESET}}$ pin has been brought high. I²C Mode is selected by connecting the AD0/ $\overline{\text{CS}}$ pin through a resistor to VL or DGND, thereby permanently selecting the desired AD0 bit address state.

4.10.1 SPI Control

In Software Mode, $\overline{\text{CS}}$ is the CS42L51 chip-select signal, CCLK is the control port bit clock (input into the CS42L51 from the microcontroller), CDIN is the input data line from the microcontroller. Data is clocked in on the rising edge of CCLK. The CODEC will only support write operations. Read request will be ignored.

Figure 23 shows the operation of the control port in Software Mode. To write to a register, bring $\overline{\text{CS}}$ low. The first seven bits on CDIN form the chip address and must be 1001010. The eighth bit is a read/write indicator (R/W), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP.

There is MAP auto-increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

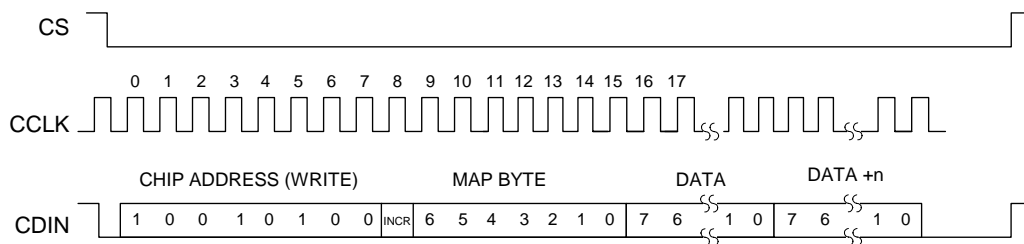


Figure 23. Control Port Timing in SPI Mode

4.10.2 I²C Control

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{\text{CS}}$ pin. Pin AD0 forms the least significant bit of the chip address and should be connected through a resistor to VL or DGND as desired. The state of the pin is sensed while the CS42L51 is being reset.

The signal timings for a read and write cycle are shown in Figure 24 and Figure 25. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42L51 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write). The upper 6 bits of the 7-bit address field are fixed at 100101. To communicate with a CS42L51, the chip address field, which is the first byte sent to the CS42L51, should match 100101 followed by the setting of the AD0 pin. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read,

the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42L51 after each input byte is read and is input to the CS42L51 from the microcontroller after each transmitted byte.

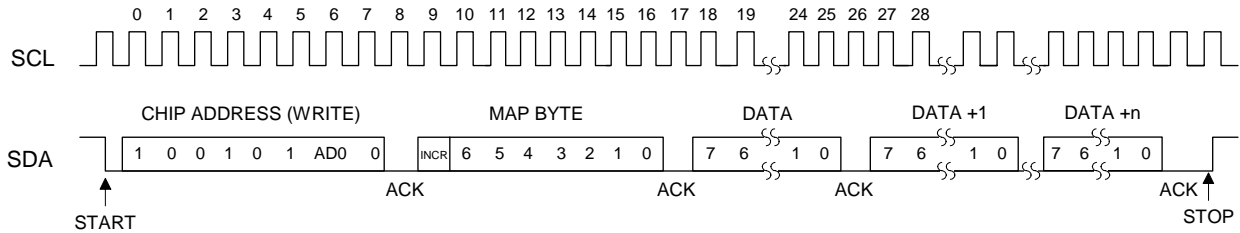


Figure 24. Control Port Timing, I²C Write

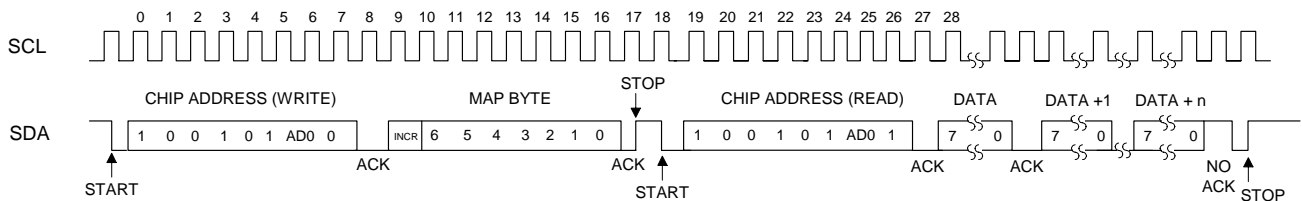


Figure 25. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in [Figure 25](#), the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

- Send start condition.
- Send 100101x0 (chip address & write operation).
- Receive acknowledge bit.
- Send MAP byte, auto-increment off.
- Receive acknowledge bit.
- Send stop condition, aborting write.
- Send start condition.
- Send 100101x1 (chip address & read operation).
- Receive acknowledge bit.
- Receive byte, contents of selected register.
- Send acknowledge bit.
- Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.10.3 Memory Address Pointer (MAP)

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudo code above for implementation details.

4.10.3.1 Map Increment (INCR)

The device has MAP auto-increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

5. REGISTER QUICK REFERENCE

Software mode register defaults are as shown. "Reserved" registers must maintain their default state.

Addr	Function	7	6	5	4	3	2	1	0
01h	ID p 49 default	Chip_ID4 1	Chip_ID3 1	Chip_ID2 0	Chip_ID1 1	Chip_ID0 1	Rev_ID2 0	Rev_ID1 0	Rev_ID0 1
02h	Power Ctl. 1 p 49 default	Reserved 0	PDN_DACB 0	PDN_DACA 0	dPDN_PGAB 0	PDN_PGAA 0	PDN_ADCB 0	PDN_ADCA 0	PDN 0
03h	Speed Ctl. & Power Ctl. 2 p 50 default	AUTO 1	SPEED1 0	SPEED0 1	3-ST_SP 0	PDN_MICB 1	PDN_MICA 1	PDN_ MICBIAS 1	MCLKDIV2 0
04h	Interface Ctl. p 52 default	SDOUT->SDIN 0	M/S 0	DAC_DIF2 0	DAC_DIF1 0	DAC_DIF0 0	ADC_I ² S/LJ 0	DIGMIX 0	MICMIX 0
05h	MIC Control & Misc. p 53 default	ADC_SNGVOL 0	ADCB_ DBOOST 0	ADCA_ DBOOST 0	MICBIAS_ SEL 0	MICBIAS_ LVL1 0	MICBIAS_ LVL0 0	MICB_ BOOST 0	MICA_ BOOST 0
06h	ADC Control p 54 default	ADCB_HPF EN 1	ADCB_HP FRZ 0	ADCA_HPF EN 1	ADCA_HP FRZ 0	SOFTB 0	ZCROSSB 0	SOFTA 0	ZCROSSA 0
07h	ADC Input Select , Invert, Mute p 56 default	AINB_MUX1 0	AINB_MUX 0	AINA_MUX1 0	AINA_MUX0 0	INV_ADCB 0	INV_ADCA 0	ADCB_ MUTE 0	ADCA_ MUTE 0
08h	DAC Output Control p 57 default	HP_GAIN2 0	HP_GAIN1 1	HP_GAIN0 1	DAC_SNG VOL 0	INV_PCMB 0	INV_PCMA 0	DACB_ MUTE 0	DACA_ MUTE 0
09h	DAC Control p 58 default	DATA_SEL1 0	DATA_SEL0 0	FREEZE 0	Reserved 0	DEEMPH 0	AMUTE 1	DAC_SZC1 1	DAC_SZC0 0
0Ah	ALCA SZC & PGAA Vol- ume p 59 default	ALCA_SR DIS 0	ALCA_ZC DIS 0	Reserved 0	PGAA VOL4 0	PGAA VOL3 0	PGAA VOL2 0	PGAA VOL1 0	PGAA VOL0 0
0Bh	ALCB SZC & PGAB Vol- ume p 59 default	ALCB_SR DIS 0	ALCB_ZC DIS 0	Reserved 0	PGAB VOL4 0	PGAB VOL3 0	PGAB VOL2 0	PGAB VOL1 0	PGAB VOL0 0
0Ch	ADCA Atten- uator p 60 default	ADCA_ ATT7 0	ADCA_ ATT6 0	ADCA_ ATT5 0	ADCA_ ATT4 0	ADCA_ ATT3 0	ADCA_ ATT2 0	ADCA_ ATT1 0	ADCA_ ATT0 0
0Dh	ADCB Atten- uator	ADCB_ ATT7	ADCB_ ATT6	ADCB_ ATT5	ADCB_ ATT4	ADCB_ ATT3	ADCB_ ATT2	ADCB_ ATT1	ADCB_ ATT0

Addr	Function	7	6	5	4	3	2	1	0
	p 60 default	0	0	0	0	0	0	0	0
0Eh	Vol. Control ADCMIXA p 61 default	MUTE_ADC MIXA 1	ADCMIXA VOL6 0	ADCMIXA VOL5 0	ADCMIXA VOL4 0	ADCMIXA VOL3 0	ADCMIXA VOL2 0	ADCMIXA VOL1 0	ADCMIXA VOL0 0
0Fh	Vol. Control ADCMIXB p 61 default	MUTE_ADC MIXB 1	ADCMIXB VOL6 0	ADCMIXB VOL5 0	ADCMIXB VOL4 0	ADCMIXB VOL3 0	ADCMIXB VOL2 0	ADCMIXB VOL1 0	ADCMIXB VOL0 0
10h	Vol. Control PCMMIXA p 62 default	MUTE_PCM MIXA 1	PCMMIXA VOL6 0	PCMMIXA VOL5 0	PCMMIXA VOL4 0	PCMMIXA VOL3 0	PCMMIXA VOL2 0	PCMMIXA VOL1 0	PCMMIXA VOL0 0
11h	Vol. Control PCMMIXB p 62 default	MUTE_PCM MIXB 1	PCMMIXB VOL6 0	PCMMIXB VOL5 0	PCMMIXB VOL4 0	PCMMIXB VOL3 0	PCMMIXB VOL2 0	PCMMIXB VOL1 0	PCMMIXB VOL0 0
12h	BEEP Freq. & OnTime p 62 default	FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0
		0	0	0	0	0	0	0	0
13h	BEEP Off Time & Vol. p 63 default	OFFTIME2	OFFTIME1	OFFTIME0	BPVOL4	BPVOL3	BPVOL2	BPVOL1	BPVOL0
		0	0	0	0	0	0	0	0
14h	BEEP Control & Tone Config p 64 default	REPEAT	BEEP	Reserved	TREB_CF1	TREB_CF0	BASS_CF1	BASS_CF0	TC_EN
		0	0	0	0	0	0	0	0
15h	Tone Control p 65 default	TREB3	TREB2	TREB1	TREB0	BASS3	BASS2	BASS1	BASS0
		1	0	0	0	1	0	0	0
16h	Vol. Control AOUTA p 66 default	AOUTA_ VOL7	AOUTA_ VOL6	AOUTA_ VOL5	AOUTA_ VOL4	AOUTA_ VOL3	AOUTA_ VOL2	AOUTA_ VOL1	AOUTA_ VOL0
		0	0	0	0	0	0	0	0
17h	Vol. Control AOUTB p 66 default	AOUTB_ VOL7	AOUTB_ VOL6	AOUTB_ VOL5	AOUTB_ VOL4	AOUTB_ VOL3	AOUTB_ VOL2	AOUTB_ VOL1	AOUTB_ VOL0
		0	0	0	0	0	0	0	0
18h	PCM & ADC Channel Mixer p 67 default	PCMA1	PCMA0	PCMB1	PCMB0	ADCA1	ADCA0	ADCB1	ADCB0
		0	0	0	0	0	0	0	0
19h	Limiter Threshold & SZC Disable p 67 default	MAX2	MAX1	MAX0	CUSH2	CUSH1	CUSH0	LIM_SRDIS	LIM_ZCDIS
		0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
1Ah	Limiter Config & Release Rate p 69 default	LIMIT_EN 0	LIMIT_ALL 1	LIM_RRATE 5 1	LIM_RRATE 4 1	LIM_RRATE 3 1	LIM_RRATE 2 1	LIM_RRATE 1 1	LIM_RRATE 0 1
1Bh	Limiter Attack Rate p 70 default	Reserved 0	Reserved 0	LIM_ARATE5 0	LIM_ARATE4 0	LIM_ARATE3 0	LIM_ARATE2 0	LIM_ARATE1 0	LIM_ARATE0 0
1Ch	ALC Enable & Attack Rate p 70 default	ALC_ENB 0	ALC_ENA 0	ALC_ARATE 5 0	AALC_RATE 4 0	ALC_ARATE 3 0	ALC_ARATE 2 0	ALC_ARATE 1 0	ALC_ARATE 0 0
1Dh	ALC Release Rate p 71 default	Reserved 0	Reserved 0	ALC_RRATE 5 1	ALC_RRATE 4 1	ALC_RRATE 3 1	ALC_RRATE 2 1	ALC_RRATE 1 1	ALC_RRATE 0 1
1Eh	ALC Threshold p 71 default	MAX2 0	MAX1 0	MAX0 0	MIN2 0	MIN1 0	MIN0 0	Reserved 0	Reserved 0
1Fh	Noise Gate Config p 72 default	NG_ALL 0	NG_EN 0	NG_BOOST 0	THRESH2 0	THRESH1 0	THRESH0 0	NGDELAY1 0	NGDELAY0 0
20h	Status p 73 default	Reserved 0	SP_CLKER R 0	SPEB_OVFL 0	SPEA_OVFL 0	PCMA_OVFL 0	PCMB_OVFL 0	ADCA_OVFL 0	ADCB_OVFL 0
21h	Charge Pump Frequency p 74 default	CHRG_ FREQ3 0	CHRG_ FREQ2 1	CHRG_ FREQ1 0	CHRG_ FREQ0 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0

6. REGISTER DESCRIPTION

All registers are read/write except for the chip I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.

All “Reserved” registers must maintain their default state.

Note: Certain functions are only available when the “Signal Processing Engine to DAC” option is selected using the DATA_SEL[1:0] bits, as described in section [“DAC Data Selection \(DATA_SEL\[1:0\]\)” on page 58](#).

6.1 Chip I.D. and Revision Register (Address 01h) (Read Only)

7	6	5	4	3	2	1	0
Chip_ID4	Chip_ID3	Chip_ID2	Chip_ID1	Chip_ID0	Rev_ID2	Rev_ID1	Rev_ID0

Chip I.D. (Chip_ID[4:0])

Default: 11011

Function:

I.D. code for the CS42L51. Permanently set to 11011.

Chip Revision (Rev_ID[2:0])

Default: 001

Function:

CS42L51 revision level. Revision B is coded as 001. Revision A is coded as 000.

6.2 Power Control 1 (Address 02h)

7	6	5	4	3	2	1	0
Reserved	PDN_DACB	PDN_DACA	PDN_PGAB	PDN_PGAA	PDN_ADCB	PDN_ADCA	PDN

Notes:

- To activate the power-down sequence for individual channels (A or B,) *both* channels must first be powered down either by enabling the PDN bit or by enabling the power-down bits for both channels. Enabling the power-down bit on an individual channel basis after the CODEC has fully powered up will mute the selected channel without achieving any power savings.

Recommended channel power-down sequence: 1.) Enable the PDN bit, 2.) enable power-down for the select channels, 3.) disable the PDN bit.

Power Down DAC X (PDN_DACX)

Default: 0

0 - Disable

1 - Enable

Function:

DAC channel x will either enter a power-down or muted state when this bit is enabled. See [Note 1](#) above.

Power Down PGA X (PDN_PGAX)

Default: 0

- 0 - Disable
- 1 - Enable

Function:

PGA channel x will either enter a power-down or muted state when this bit is enabled. See [Power Control 1 \(Address 02h\)](#) on [page 49](#) above.

This bit is used in conjunction with AINx_MUX bits to determine the analog input path to the ADC. Refer to [“ADCX Input Select Bits \(AINX_MUX\[1:0\]\)”](#) on [page 56](#) for the required settings.

Power Down ADC X (PDN_ADCX)

Default: 0

- 0 - Disable
- 1 - Enable

Function:

ADC channel x will either enter a power-down or muted state when this bit is enabled. See [Note 1 on page 49](#).

Power Down (PDN)

Default: 0

- 0 - Disable
- 1 - Enable

Function:

The entire CODEC will enter a low-power state when this function is enabled. The contents of the control port registers are retained in this mode.

6.3 MIC Power Control & Speed Control (Address 03h)

7	6	5	4	3	2	1	0
AUTO	SPEED1	SPEED0	3-ST_SP	PDN_MICB	PDN_MICA	PDN_MICBIAS	MCLKDIV2

Auto-Detect Speed Mode (AUTO)

Default: 1

- 0 - Disable
- 1 - Enable

Function:

Enables the auto-detect circuitry for detecting the speed mode of the CODEC when operating as a slave. When AUTO is enabled, the MCLK/LRCK ratio must be implemented according to [Table 3 on page 39](#). The SPEED[1:0] bits are ignored when this bit is enabled. Speed is determined by the MCLK/LRCK ratio.

Speed Mode (SPEED[1:0])

Default: 01

- 11 - Quarter-Speed Mode (QSM) - 4 to 12.5 kHz sample rates
- 10 - Half-Speed Mode (HSM) - 12.5 to 25 kHz sample rates
- 01 - Single-Speed Mode (SSM) - 4 to 50 kHz sample rates
- 00 - Double-Speed Mode (DSM) - 50 to 100 kHz sample rates

Function:

Sets the appropriate speed mode for the CODEC in Master or Slave Mode. QSM is optimized for 8 kHz sample rate and HSM is optimized for 16 kHz sample rate. These bits are ignored when the AUTO bit is enabled (see [Auto-Detect Speed Mode \(AUTO\)](#) above).

Tri-State Serial Port Interface (3ST_SP)

Default: 0

- 0 - Disable
- 1 - Enable

Function:

When enabled and the device is configured as a master, all serial port outputs are placed in a high impedance state. If the serial port is configured as a slave, only the SDOOUT pin will be placed in a high-impedance state. The other signals will remain as inputs.

Power Down MIC X (PDN_MICX)

Default: 1

- 0 - Disable
- 1 - Enable

Function:

When enabled, the microphone pre-amplifier for channel x will be in a power-down state.

Power Down MIC BIAS (PDN_MICBIAS)

Default: 1

- 0 - Disable
- 1 - Enable

Function:

When enabled, the microphone bias circuit will be in a power-down state.

MCLK Divide By 2 (MCLKDIV2)

Default: 0

- 0 - Disabled
- 1 - Divide by 2

Function:

Divides the input MCLK by 2 prior to all internal circuitry. This bit is ignored when the AUTO bit is disabled in Slave Mode.

6.4 Interface Control (Address 04h)

7	6	5	4	3	2	1	0
SDOUT->SDIN	M/S	DAC_DIF2	DAC_DIF1	DAC_DIF0	ADC_I ² S/LJ	DIGMIX	MICMIX

SDOUT to SDIN Loopback (SDOUT->SDIN)

Default: 0

- 0 - Disabled; SDOUT internally disconnected from SDIN
- 1 - Enabled; SDOUT internally connected to SDIN

Function:

Internally loops the signal on the SDOUT pin to SDIN.

Master/Slave Mode (M/ \bar{S})

Default: 0

- 0 - Slave
- 1 - Master

Function:

Selects either master or slave operation for the serial port.

DAC Digital Interface Format (DAC_DIF[2:0])

Default = 000

DAC_DIF[2:0]	Description	Figure
000	Left-Justified, up to 24-bit data	20 on page 41
001	I ² S, up to 24-bit data	19 on page 40
010	Right-Justified, 24-bit data	21 on page 41
011	Right-Justified, 20-bit data	21 on page 41
100	Right-Justified, 18-bit data	21 on page 41
101	Right-Justified, 16-bit data	21 on page 41
110	Reserved	-
100	Reserved	-

Function:

Selects the digital interface format used for the data in on SDIN. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in the section [“Digital Interface Formats” on page 40](#).

ADC I²S or Left-Justified (ADC_I²S/LJ)

Default: 0

- 0 - Left-Justified
- 1 - I²S

Function:

Selects either the I²S or Left-Justified digital interface format for the data on SDOOUT. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in this section .

Digital Mix (DIGMIX)

Default: 0

DIGMIX	DATA_SEL[1:0]	Mix Selected
0	xx	No Mix: ADC to ADC serial port, SDOOUT data.
1	00	No Mix: SDIN data to ADC serial port, SDOOUT data.
	01	Mix: ADC + SDIN data to ADC serial port, SDOOUT data.
	10	No Mix: ADC to ADC serial port, SDOOUT data.
	11	Reserved

Function:

Selects between the ADC or a digital mix of the ADC and DAC into the serial port to the SDOOUT pin. This mix function is affected by the data select bits DATA_SEL[1:0].

Microphone Mix (MICMIX)

Default: 0

- 0 - Disabled; No Mix: Left/Right Channel to ADC serial port, SDOOUT.
- 1 - Enabled; Mix: Differential mix ((A-B)/2)to ADC serial port, SDOOUT.

Function:

Selects between the ADC stereo mix or a differential mix of analog inputs A and B.

6.5 MIC Control (Address 05h)

7	6	5	4	3	2	1	0
ADC_SNGVOL	ADCB_DBOOST	ADCA_DBOOST	MICBIAS_SEL	MICBIAS_LVL1	MICBIAS_LVL0	MICB_BOOST	MICA_BOOST

ADC Single Volume Control (ADC_SNGVOL)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

The individual PGA Volume (PGA_x_VOL_x) and ADC channel attenuation (ADC_x_ATT_x) levels as well as the ALC A and B enable (ALC_EN_x) are independently controlled by their respective control registers when this function is disabled. When enabled, the volume on both channels is determined by the ADCA Attenuator Control register, or the PGAA Control register, and the ADCB Attenuator and PGAB Control registers are ignored. The ALC enable control for channel B is controlled by the ALC A enable when the ADC_SNGVOL bit is enabled and the ALC_ENB control register is ignored.

ADCx 20 dB Digital Boost (ADCx_DBOOST)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

Applies a 20 dB digital gain to the input signal on ADC channel x, regardless of the input path.

MIC Bias Select (MICBIAS_SEL)

Default: 0

- 0 - MICBIAS on AIN3B/MICIN2 pin
- 1 - MICBIAS on AIN2B pin

Function:

Determines the output pin for the internally generated MICBIAS signal. If set to '0'b, the MICBIAS is output on the AIN3B/MICIN2 pin. If set to '1'b, the MICBIAS is output on the AIN2B pin.

MIC Bias Level (MICBIAS_LVL[1:0])

Default: 00

- 00 - 0.8 x VA
- 01 - 0.7 x VA
- 10 - 0.6 x VA
- 11 - 0.5 x VA

Function:

Determines the output voltage level of the MICBIAS output.

MIC X Preamplifier Boost (MICX_BOOST)

Default: 0

- 0 - +16 dB Gain
- 1 - +32 dB Gain

Function:

Determines the amount of gain applied to the microphone preamplifier for channel x.

6.6 ADC Control (Address 06h)

7	6	5	4	3	2	1	0
ADCB_HPFEN	ADCB_HPFRZ	ADCA_HPFEN	ADCA_HPFRZ	SOFTB	ZCROSSB	SOFTA	ZCROSSA

ADCX High-Pass Filter Enable (ADCX_HPFEN)

Default: 1

- 0 - High-pass filter is disabled
- 1 - High-pass filter is enabled

Function:

When this bit is set, the internal high-pass filter will be enabled for ADCx. When set to '0', the high-pass filter will be disabled. For DC measurements, this bit must be cleared to '0'. See ["ADC Digital Filter Characteristics" on page 15](#).

ADCX High-Pass Filter Freeze (ADCX_HPFRZ)

Default: 0

- 0 - Continuous DC Subtraction
- 1 - Frozen DC Subtraction

Function:

The high-pass filter works by continuously subtracting a measure of the DC offset from the output of the decimation filter. If the ADCx_HPFRZ bit is taken high during normal operation, the current value of the DC offset is frozen, and this DC offset will continue to be subtracted from the conversion result. For DC measurements, this bit must be set to '1'. See [“ADC Digital Filter Characteristics” on page 15](#).

Soft Ramp CHX Control (SOFTX)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

Soft Ramp allows level changes to be implemented via an incremental ramp. ADCx_ATT[7:0] digital attenuation changes are ramped from the current level to the new level at a rate of 0.125 dB per LRCK period. PGAx_VOL[4:0] gain changes are ramped in 0.5 dB steps every 16 LRCK periods.

Soft Ramp & Zero Cross Enabled

When used in conjunction with the ZCROSSx bit, the PGAx_VOL[4:0] gain changes will occur in 0.5 dB steps and be implemented on a signal zero crossing.

Zero Cross CHX Control (ZCROSSX)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

Zero Cross Enable dictates that signal level changes will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period of 1024 sample periods (approximately 10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp & Zero Cross Enabled

When used in conjunction with the SOFTx bit, the PGAx_VOL[4:0] gain changes will occur in 0.5 dB steps and be implemented on a signal zero crossing.

The ADC Attenuator ADCx_ATT[7:0] is not affected by the ZCROSSx bit.

SOFTx	ZCROSSx	Analog PGA Volume (PGAx_VOL[4:0])	Digital Attenuator (ADCx_ATT[7:0])
0	0	Volume changes immediately.	Volume changes immediately.
0	1	Volume changes at next zero cross time.	Volume changes immediately.
1	0	Volume changes in 0.5 dB steps.	Change volume in 0.125 dB steps.
1	1	Volume changes in 0.5 dB steps at every signal zero-cross.	Change volume in 0.125 dB steps.

6.7 ADCx Input Select, Invert & Mute (Address 07h)

7	6	5	4	3	2	1	0
AINB_MUX1	AINB_MUX0	AINA_MUX1	AINA_MUX0	INV_ADCB	INV_ADCA	ADCB_MUTE	ADCA_MUTE

ADCX Input Select Bits (AINX_MUX[1:0])

Default: 00

PDN_PGAx	AINx_MUX[1:0]	Selected Path to ADC
0	00	AIN1x-->PGAx
0	01	AIN2x-->PGAx
0	10	AIN3x/MICINx-->PGAx
0	11	AIN3x/MICINx-->Pre-Amp(+16/+32 dB Gain)-->PGAx
1	00	AIN1x
1	01	AIN2x
1	10	AIN3x/MICINx
1	11	Reserved

Function:

Selects the specified analog input signal into ADCx. The microphone pre-amplifier is only available when PDN_PGAx is disabled. See [Figure 26](#).

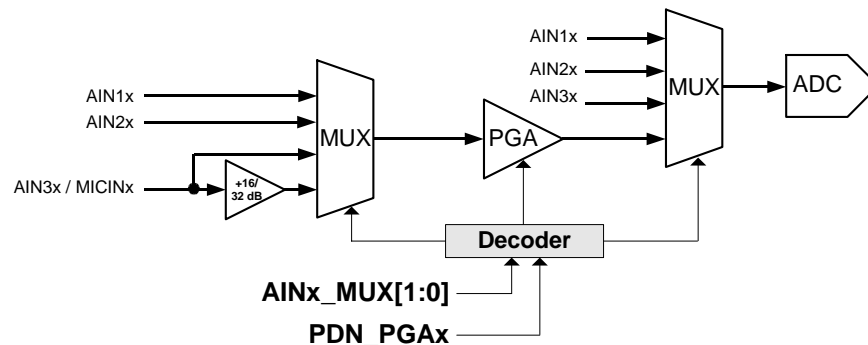


Figure 26. AIN & PGA Selection

ADCX Invert Signal Polarity (INV_ADCX)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

When enabled, this bit will invert the signal polarity of the ADC x channel.

ADCX Channel Mute (ADCX_MUTE)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

The output of channel x ADC will mute when enabled. The muting function is affected by the ADCx Soft bit (SOFT).

6.8 DAC Output Control (Address 08h)

7	6	5	4	3	2	1	0
HP_GAIN2	HP_GAIN1	HP_GAIN0	DAC_SNGVOL	INV_PCMB	INV_PCMA	DACB_MUTE	DACA_MUTE

Headphone Analog Gain (HP_GAIN[2:0])

Default: 011

HP_GAIN[2:0]	Gain Setting
000	0.3959
001	0.4571
010	0.5111
011	0.6047
100	0.7099
101	0.8399
110	1.0000
111	1.1430

Function:

These bits select the gain multiplier for the headphone/line outputs. See [“Line Output Voltage Characteristics” on page 18](#) and [“Headphone Output Power Characteristics” on page 19](#).

DAC Single Volume Control (DAC_SNGVOL)

Default: 0

Function:

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on all channels is determined by the AOUTA Volume Control register and the AOUTB Volume Control register is ignored.

PCMX Invert Signal Polarity (INV_PCMX)

Default: 0

0 - Disabled
1 - Enabled

Function:

When enabled, this bit will invert the signal polarity of the PCM x channel.

DACX Channel Mute (DACX_MUTE)

Default: 0

0 - Disabled
1 - Enabled

Function:

The output of channel x DAC will mute when enabled. The muting function is affected by the DACx Soft and Zero Cross bits (DACx_SZC[1:0]).

6.9 DAC Control (Address 09h)

7	6	5	4	3	2	1	0
DATA_SEL1	DATA_SEL0	FREEZE	Reserved	DEEMPH	AMUTE	DAC_SZC1	DAC_SZC0

DAC Data Selection (DATA_SEL[1:0])

Default: 00

- 00 - PCM Serial Port to DAC
- 01 - Signal Processing Engine to DAC
- 10 - ADC Serial Port to DAC
- 11 - Reserved

Function:

Selects the digital signal source for the DAC. **Note:** Certain functions are only available when the “Signal Processing Engine to DAC” option is selected using these bits.

Freeze Controls (FREEZE)

Default: 0

Function:

This function will freeze the previous settings of, and allow modifications to be made to all control port registers without the changes taking effect until the FREEZE is disabled. To have multiple changes in the control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

DAC De-Emphasis Control (DEEMPH)

Default: 0

- 0 - No De-Emphasis
- 1 - De-Emphasis Enabled

Function:

Note: The DATA_SEL[1:0] bits in reg09h must be set to ‘01’b to enable function control.

Enables the digital filter to apply the standard 15µs/50µs digital de-emphasis filter response for a sample rate of 44.1 kHz.

Analog Output Auto MUTE (AMUTE)

Default: 0

- 0 - Auto Mute Disabled
- 1 - Auto Mute Enabled

Function:

Enables (or disables) Automatic Mute of the analog outputs after 8192 “0” samples on each digital input channel.

DAC Soft Ramp and Zero Cross Control (DAC_SZC[1:0])

Default = 10

- 00 - Immediate Change
- 01 - Zero Cross
- 10 - Soft Ramp
- 11 - Soft Ramp on Zero Crossings

Function:

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control

Immediate Change

When Immediate Change is selected all volume-level changes will take effect immediately in one step.

Zero Cross

This setting dictates that signal-level changes, either by gain changes, attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 1024 and 2048 sample periods (21.3 ms to 42.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. **Note:** The LIM_SRDIS bit is ignored.

Soft Ramp

Soft Ramp allows level changes, either by gain changes, attenuation changes or muting, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 0.5 dB per 4 left/right clock periods.

Soft Ramp on Zero Crossing

This setting dictates that signal-level changes, either by gain changes, attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. **Note:** The LIM_SRDIS bit is ignored.

6.10 ALCX & PGAX Control: ALCA, PGAA (Address 0Ah) & ALCB, PGAB (Address 0Bh)

7	6	5	4	3	2	1	0
ALCX_SRDIS	ALCX_ZCDIS	Reserved	PGAX_VOL4	PGAX_VOL3	PGAX_VOL2	PGAX_VOL1	PGAX_VOL0

ALCX Soft Ramp Disable (ALCX_SRDIS)

Default: 0

- 0 - Off
- 1 - On

Function:

Overrides the SOFTx bit setting for the ADC. When this bit is set, the ALC attack rate in the PGA will not be dictated by the soft ramp setting. ALC volume-level changes will take effect in one step.

ALCX Zero Cross Disable (ALCX_ZCDIS)

Default: 0

- 0 - Off
- 1 - On

Function:

Overrides the ZCROSSx bit setting for the ADC. When this bit is set, the ALC attack rate in the PGA will not be dictated by the zero cross setting. ALC volume-level changes will take effect immediately in one step.

PGA X Gain Control (PGAX_VOL[4:0])

Default: 00000

Binary Code	Volume Setting
11000	+12 dB
...	...
01010	+5 dB
...	...
00000	0 dB
11111	-0.5 dB
11110	-1 dB
...	...
11001	-3 dB
11010	-3 dB

Function:

The PGAX Gain Control register allows independent setting of the signal levels in 0.5 dB increments as dictated by the ADCx Soft and Zero Cross bits (SOFTx & ZCROSSx) from +12 dB to -3 dB. Gain settings are decoded as shown in the table above. The gain changes are implemented as dictated by the ALCX Soft & Zero Cross bits (ALCX_SZC). Levels are decoded as described in the table above.

Note: When the ALC is enabled, the PGA is automatically controlled and should not be adjusted manually.

6.11 ADCx Attenuator: ADCA (Address 0Ch) & ADCB (Address 0Dh)

7	6	5	4	3	2	1	0
ADCx_ATT7	ADCx_ATT6	ADCx_ATT5	ADCx_ATT4	ADCx_ATT3	ADCx_ATT2	ADCx_ATT1	ADCx_ATT0

ADCX Attenuation Control (ADCX_ATT[7:0])

Default: 00h

Binary Code	Volume Setting
0111 1111	0 dB
...	...
0000 0000	0 dB
1111 1111	-1 dB
1111 1110	-2 dB
...	...
1010 0000	-96 dB
...	...
1000 0000	-96 dB

Function:

The level of ADCX can be adjusted in 1.0 dB increments as dictated by the ADCx Soft and Zero Cross bits (SOFTx & ZCROSSx) from 0 to -96 dB. Levels are decoded in two's complement, as shown in the table above.

Note: When the ALC is enabled, the Attenuator and PGA volume is automatically controlled and should not be adjusted manually.

6.12 ADCx Mixer Volume Control: ADCA (Address 0Eh) & ADCB (Address 0Fh)

7	6	5	4	3	2	1	0
MUTE_ADCMIXx	ADCMIXx_VOL6	ADCMIXx_VOL5	ADCMIXx_VOL4	ADCMIXx_VOL3	ADCMIXx_VOL2	ADCMIXx_VOL1	ADCMIXx_VOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

ADCX Mixer Channel Mute (MUTE_ADCMIXX)

Default: 1

- 0 - Disabled
- 1 - Enabled

Function:

The ADC channel X input to the output mixer will mute when enabled. The muting function is affected by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]).

ADCX Mixer Volume Control (ADCMIXX_VOL[6:0])

Default = 000 0000

Binary Code	Volume Setting
001 1000	+12.0 dB
...	...
000 0000	0 dB
111 1111	-0.5 dB
111 1110	-1.0 dB
...	...
001 1001	-51.5 dB

Function:

The level of the ADCX input to the output mixer can be adjusted in 0.5 dB increments as dictated by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]) from +12 to -51.5 dB. Levels are decoded as shown in the table above.

6.13 PCMX Mixer Volume Control: PCMA (Address 10h) & PCMB (Address 11h)

7	6	5	4	3	2	1	0
MUTE_ PCMMIXx	PCMMIXx_ VOL6	PCMMIXx_ VOL5	PCMMIXx_ VOL4	PCMMIXx_ VOL3	PCMMIXx_ VOL2	PCMMIXx_ VOL1	PCMMIXx_ VOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

PCMX Mixer Channel Mute (MUTE_PCMMIXX)

Default = 1

0 - Disabled
1 - Enabled

Function:

The PCM channel X input to the output mixer will mute when enabled. The muting function is affected by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]).

PCMX Mixer Volume Control (PCMMIXX_VOL[6:0])

Default: 000 0000

Binary Code	Volume Setting
001 1000	+12.0 dB
...	...
000 0000	0 dB
111 1111	-0.5 dB
111 1110	-1.0 dB
...	...
001 1001	-51.5 dB

Function:

The level of the PCMX input to the output mixer can be adjusted in 0.5 dB increments as dictated by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]) from +12 to -51.5 dB. Levels are decoded as described in the table above.

6.14 Beep Frequency & Timing Configuration (Address 12h)

7	6	5	4	3	2	1	0
FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Beep Frequency (FREQ[3:0])

Default: 0000

FREQ[3:0]	Frequency Fs = 12, 24, 48 or 96 kHz	Pitch
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5

FREQ[3:0]	Frequency Fs = 12, 24, 48 or 96 kHz	Pitch
0101	774.19 Hz	G5
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7

Function:

The frequency of the beep signal can be adjusted from 260.87 Hz to 2181.82 Hz. Beep frequency will scale directly with sample rate, Fs, but is fixed at the nominal Fs within each speed mode. Refer to [Figure 15 on page 36](#) for single, multiple and continuous beep configurations using the REPEAT and BEEP bits.

Beep On Time Duration (ONTIME[3:0])

Default: 0000

TIME[3:0]	On Time Fs = 12, 24, 48 or 96 kHz
0000	86 ms
...	...
1111	5.2 s

Function:

The on-duration of the beep signal can be adjusted from approximately 86 ms to 5.2 s. The on-duration will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode. Refer to [Figure 15 on page 36](#) for single-, multiple- and continuous-beep configurations using the REPEAT and BEEP bits.

6.15 Beep Off Time & Volume (Address 13h)

7	6	5	4	3	2	1	0
OFFTIME2	OFFTIME1	OFFTIME0	BPVOL4	BPVOL3	BPVOL2	BPVOL1	BPVOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Beep Off Time (OFFTIME[2:0])

Default: 000

OFFTIME[2:0]	Off Time Fs = 12, 24, 48 or 96 kHz
000	1.23 s
001	2.58 s
010	3.90 s
011	5.20 s
100	6.60 s
101	8.05 s

OFFTIME[2:0]	Off Time Fs = 12, 24, 48 or 96 kHz
110	9.35 s
111	10.80 s

Function:

The off-duration of the beep signal can be adjusted from approximately 75 ms to 680 ms. The off-duration will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode. Refer to [Figure 15 on page 36](#) for single-, multiple- and continuous-beep configurations using the REPEAT and BEEP bits.

Beep Volume (BPVOL[4:0])

Default: 00000

Binary Code	Volume Setting
00110	+12.0 dB
...	...
00000	0 dB
11111	-2 dB
11110	-4 dB
...	...
00111	-50 dB

Function:

The level of the beep into the output mixer can be adjusted in 2.0 dB increments from +12 dB to -50 dB. Refer to [Figure 15 on page 36](#) for single-, multiple- and continuous-beep configurations using the REPEAT and BEEP bits. Levels are decoded as described in the table above.

6.16 Beep Configuration & Tone Configuration (Address 14h)

7	6	5	4	3	2	1	0
REPEAT	BEEP	Reserved	TREB_CF1	TREB_CF0	BASS_CF1	BASS_CF0	TC_EN

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Repeat Beep (REPEAT)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

This bit is used in conjunction with the BEEP bit to mix a continuous or periodic beep with the analog output. Refer to [Figure 15 on page 36](#) for a description of each configuration option.

Beep (BEEP)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

This bit is used in conjunction with the REPEAT bit to mix a continuous or periodic beep with the analog output. **Note:** Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration. Refer to [Figure 15 on page 36](#) for a description of each configuration option.

Treble Corner Frequency (TREB_CF[1:0])

Default: 00

- 00 - 5 kHz
- 01 - 7 kHz
- 10 - 10 kHz
- 11 - 15 kHz

Function:

The treble corner frequency is user selectable as shown above.

Bass Corner Frequency (BASS_CF[1:0])

Default: 00

- 00 - 50 Hz
- 01 - 100 Hz
- 10 - 200 Hz
- 11 - 250 Hz

Function:

The bass corner frequency is user-selectable as shown above.

Tone Control Enable (TC_EN)

Default = 0

- 0 - Disabled
- 1 - Enabled

Function:

The Bass and Treble tone control features are active when this bit is enabled.

6.17 Tone Control (Address 15h)

7	6	5	4	3	2	1	0
TREB3	TREB2	TREB1	TREB0	BASS3	BASS2	BASS1	BASS0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Treble Gain Level (TREB[3:0])

Default: 1000 dB (No Treble Gain)

Binary Code	Gain Setting
0000	+12.0 dB
...	...
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
...	...
1111	-10.5 dB

Function:

The level of the shelving treble gain filter is set by Treble Gain Level. The level can be adjusted in 1.5 dB increments from +12.0 to -10.5 dB.

Bass Gain Level (BASS[3:0])

Default: 1000 dB (No Bass Gain)

Binary Code	Gain Setting
0000	+12.0 dB
...	...
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
...	...
1111	-10.5 dB

Function:

The level of the shelving bass gain filter is set by Bass Gain Level. The level can be adjusted in 1.5 dB increments from +10.5 to -10.5 dB.

**6.18 AOUTx Volume Control:
AOUTA (Address 16h) & AOUTB (Address 17h)**

7	6	5	4	3	2	1	0
AOUTx_VOL7	AOUTx_VOL6	AOUTx_VOL5	AOUTx_VOL4	AOUTx_VOL3	AOUTx_VOL2	AOUTx_VOL1	AOUTx_VOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

AOUTX Volume Control (AOUTX_VOL[7:0])

Default = 00h

Binary Code	Volume Setting
0001 1000	+12.0 dB
...	...
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-102 dB
...	...
0001 1001	-102 dB

Function:

The analog output levels can be adjusted in 0.5 dB increments from +12 to -102 dB as dictated by the DAC Soft and Zero Cross bits (DACX_SZC[1:0]). Levels are decoded in unsigned binary as described in the table above.

Note: When the limiter is enabled, the AOUT Volume is automatically controlled and should not be adjusted manually. Alternative volume control may be achieved using the PCMMIXx_VOL[6:0] bits.

6.19 PCM Channel Mixer (Address 18h)

7	6	5	4	3	2	1	0
PCMA1	PCMA0	PCMB1	PCMB0	ADCA1	ADCA0	ADCB1	ADCB0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Channel Mixer (PCMx[1:0] & ADCx[1:0])

Default: 00

PCMA[1:0] and/or ADCA[1:0]	AOUTA	PCMB[1:0] and/or ADCB[1:0]	AOUTB
00	L	00	R
01	$\frac{L+R}{2}$	01	$\frac{L+R}{2}$
10	$\frac{L+R}{2}$	10	$\frac{L+R}{2}$
11	R	11	L

Function:

Implements mono mixes of the left and right channels as well as a left/right channel swap.

6.20 Limiter Threshold SZC Disable (Address 19h)

7	6	5	4	3	2	1	0
MAX2	MAX1	MAX0	CUSH2	CUSH1	CUSH0	LIM_SRDIS	LIM_ZCDIS

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Maximum Threshold (MAX[2:0])

Default: 000

MAX[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6
011	-9
101	-12
101	-18
110	-24
111	-30

Function:

Sets the maximum level, below full scale, at which to limit and attenuate the output signal at the attack rate. Bass, Treble and digital gain settings that boost the signal beyond the maximum threshold may trigger an attack.

Cushion Threshold (CUSH[2:0])

Default: 000

CUSH[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6
011	-9
101	-12
101	-18
110	-24
111	-30

Function:

Sets a cushion level below full scale. This setting is usually set slightly below the maximum (MAX[2:0]) threshold. The Limiter uses this cushion as a hysteresis point for the input signal as it maintains the signal below the maximum as well as below the cushion setting. This provides a more natural sound as the limiter attacks and releases.

Limiter Soft Ramp Disable (LIM_SRDIS)

Default: 0

0 - Off
1 - On

Function:

Overrides the DAC_SZC setting. When this bit is set, the Limiter attack and release rate will not be dictated by the soft ramp setting. **Note:** This bit is ignored when the zero-cross function is enabled (i.e. when DAC_SZC[1:0] = '01'b or '11'b.)

Limiter Zero Cross Disable (LIM_ZCDIS)

Default: 0

0 - Off
1 - On

Function:

Overrides the DAC_SZC setting. When this bit is set, the Limiter attack and release rate will not be dictated by the zero-cross setting.

6.21 Limiter Release Rate Register (Address 1Ah)

7	6	5	4	3	2	1	0
LIMIT_EN	LIMIT_ALL	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Peak Detect and Limiter Enable (LIMIT_EN)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

Limits the maximum signal amplitude to prevent clipping when this function is enabled. Peak Signal Limiting is performed by digital attenuation. **Note:** When the limiter is enabled, the AOUT Volume is automatically controlled and should not be adjusted manually. Alternative volume control may be realized using the PCMMIXx_VOL[6:0] bits.

Peak Signal Limit All Channels (LIMIT_ALL)

Default: 1

- 0 - Individual Channel
- 1 - Both channel A & B

Function:

When set to 0, the peak signal limiter will limit the maximum signal amplitude to prevent clipping on the specific channel indicating clipping. The other channels will not be affected.

When set to 1, the peak signal limiter will limit the maximum signal amplitude to prevent clipping on both channels in response to any single channel indicating clipping.

Limiter RELEASE Rate (RRATE[5:0])

Default: 111111

Binary Code	Release Time
000000	Fastest Release
...	...
111111	Slowest Release

Function:

Sets the rate at which the limiter releases the digital attenuation from levels below the minimum setting in the limiter threshold register, and returns the analog output level to the AOUTx_VOL[7:0] setting.

The limiter release rate is user selectable but is also a function of the sampling frequency, F_s , and the DAC_SZC setting unless the disable bit is enabled.

6.22 Limiter Attack Rate Register (Address 1Bh)

7	6	5	4	3	2	1	0
Reserved	Reserved	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Limiter Attack Rate (ARATE[5:0])

Default: 000000

Binary Code	Attack Time
000000	Fastest Attack
...	...
111111	Slowest Attack

Function:

Sets the rate at which the limiter attenuates the analog output from levels above the maximum setting in the limiter threshold register.

The limiter attack rate is user-selectable but is also a function of the sampling frequency, F_s , and the DAC_SZC setting unless the disable bit is enabled.

6.23 ALC Enable & Attack Rate (Address 1Ch)

7	6	5	4	3	2	1	0
ALC_ENB	ALC_ENA	ALC_ARATE5	ALC_ARATE4	ALC_ARATE3	ALC_ARATE2	ALC_ARATE1	ALC_ARATE0

ALC Enable (ALC_ENX)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

Enables automatic level control for ADC channel x.

Note: When the ALC is enabled, the Attenuator and PGA volume is automatically controlled and should not be adjusted manually.

ALC Attack Rate (ARATE[5:0])

Default: 000000

Binary Code	Attack Time
000000	Fastest Attack
...	...
111111	Slowest Attack

Function:

Sets the rate at which the ALC attenuates the analog input from levels above the maximum setting in the ALC threshold register.

The limiter attack rate is user-selectable but is also a function of the sampling frequency, F_s , and the SOFTx & ZCROSSx bit settings unless the disable bit for each function is enabled.

6.24 ALC Release Rate (Address 1Dh)

7	6	5	4	3	2	1	0
Reserved	Reserved	ALC_RRATE5	ALC_RRATE4	ALC_RRATE3	ALC_RRATE2	ALC_RRATE1	ALC_RRATE0

ALC Release Rate (RRATE[5:0])

Default: 111111

Binary Code	Release Time
000000	Fastest Release
...	...
111111	Slowest Release

Function:

Sets the rate at which the ALC releases the PGA & digital attenuation from levels below the minimum setting in the ALC threshold register, and returns the input level to the PGA_VOL[4:0] & ADCx_ATT[7:0] setting. The ALC release rate is user selectable, but is also a function of the sampling frequency, Fs, and the SOFTx & ZCROSS bit settings unless the disable bit for each function is enabled.

6.25 ALC Threshold (Address 1Eh)

7	6	5	4	3	2	1	0
MAX2	MAX1	MAX0	MIN2	MIN1	MIN0	Reserved	Reserved

Maximum Threshold (MAX[2:0])

Default: 000

MAX[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6
011	-9
100	-12
101	-18
110	-24
111	-30

Function:

Sets the maximum level, relative to full scale, at which to limit and attenuate the input signal at the attack rate.

Minimum Threshold (MIN[2:0])

Default: 000

MIN[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6

MIN[2:0]	Threshold Setting (dB)
011	-9
100	-12
101	-18
110	-24
111	-30

Function:

Sets the minimum level at which to disengage the ALC's attenuation or amplify the input signal at a rate set in the release rate register until levels again reach this minimum threshold. The ALC uses this minimum as a hysteresis point for the input signal as it maintains the signal below the maximum as well as below the minimum setting. This provides a more natural sound as the ALC attacks and releases.

6.26 Noise Gate Configuration & Misc. (Address 1Fh)

7	6	5	4	3	2	1	0
NG_ALL	NG_EN	NG_BOOST	THRESH2	THRESH1	THRESH0	NGDELAY1	NGDELAY0

Noise Gate Channel Gang (NG_ALL)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

Gangs the noise gate function for channel A and B. When enabled, both channels must fall below the threshold setting for the noise gate attenuation to take effect.

Noise Gate Enable (NG_EN)

Default: 0

- 0 - Disabled
- 1 - Enabled

Function:

Enables the noise gate. Maximum attenuation is relative to all gain settings applied.

Noise Gate Boost (NG_BOOST) and Threshold (THRESH[3:0])

Default: 000

THRESH[2:0]	Minimum Setting (NG_BOOST = '0'b)	Minimum Setting (NG_BOOST = '1'b)
000	-64 dB	-34 dB
001	-67 dB	-37 dB
010	-70 dB	-40 dB
011	-73 dB	-43 dB
100	-76 dB	-46 dB
101	-82 dB	-52 dB
110	Reserved	-58 dB
111	Reserved	-64 dB

Function:

Sets the threshold level of the noise gate. Input signals below the threshold level will be attenuated to -96 dB. NG_BOOST = '1'b adds 30 dB to the threshold settings.

Noise Gate Delay Timing (NGDELAY[1:0])

Default: 00

00 - 50 ms

01 - 100 ms

10 - 150 ms

11 - 200 ms

Function:

Sets the delay time before the noise gate attacks. Noise gate attenuation is dictated by the SOFTx & ZCROSS bit settings unless the disable bit for each function is enabled.

6.27 Status (Address 20h) (Read Only)

7	6	5	4	3	2	1	0
Reserved	SP_CLKERR	SPEA_OVFL	SPEB_OVFL	PCMA_OVFL	PCMB_OVFL	ADCA_OVFL	ADCB_OVFL

For all bits in this register, a "1" means the associated error condition has occurred at least once since the register was last read. A "0" means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0.

Serial Port Clock Error (SP_CLK Error)

Default: 0

Function:

Indicates an invalid MCLK to LRCK ratio. See ["Serial Port Clocking" on page 38](#) for valid clock ratios.

Note: On initial power up and application of clocks, this bit will be high as the serial port re-synchronizes.

Signal Processing Engine Overflow (SPEX_OVFL)

Default: 0

Function:

Indicates a digital overflow condition within the data path after the signal processing engine.

PCMX Overflow (PCMX_OVFL)

Default: 0

Function:

Indicates a digital overflow condition within the data path of the PCM mix.

ADC Overflow (ADCX_OVFL)

Default = 0

Function:

Indicates that there is an over-range condition anywhere in the CS42L51 ADC signal path of each of the associated ADC's.

6.28 Charge Pump Frequency (Address 21h)

7	6	5	4	3	2	1	0
CHRG_FREQ	CHRG_FREQ	CHRG_FREQ	CHRG_FREQ	Reserved	Reserved	Reserved	Reserved
3	2	1	0				

Charge Pump Frequency (CHRG_FREQ[3:0])

Default: 0101

N	CHRG_FREQ[3:0]	Frequency
0	0000	$\frac{64xF_s}{N + 2}$
...	...	
15	1111	

Function:

Alters the clocking frequency of the charge pump in $1/(N+2)$ fractions of the DAC oversampling rate, $128F_s$, should the switching frequency interfere with other system frequencies such as those in the AM radio band.

Note: Distortion performance may be affected.

7. ANALOG PERFORMANCE PLOTS

7.1 Headphone THD+N versus Output Power Plots

Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; $F_s = 48$ kHz. Plots were taken from the CDB42L51 using an Audio Precision analyzer.

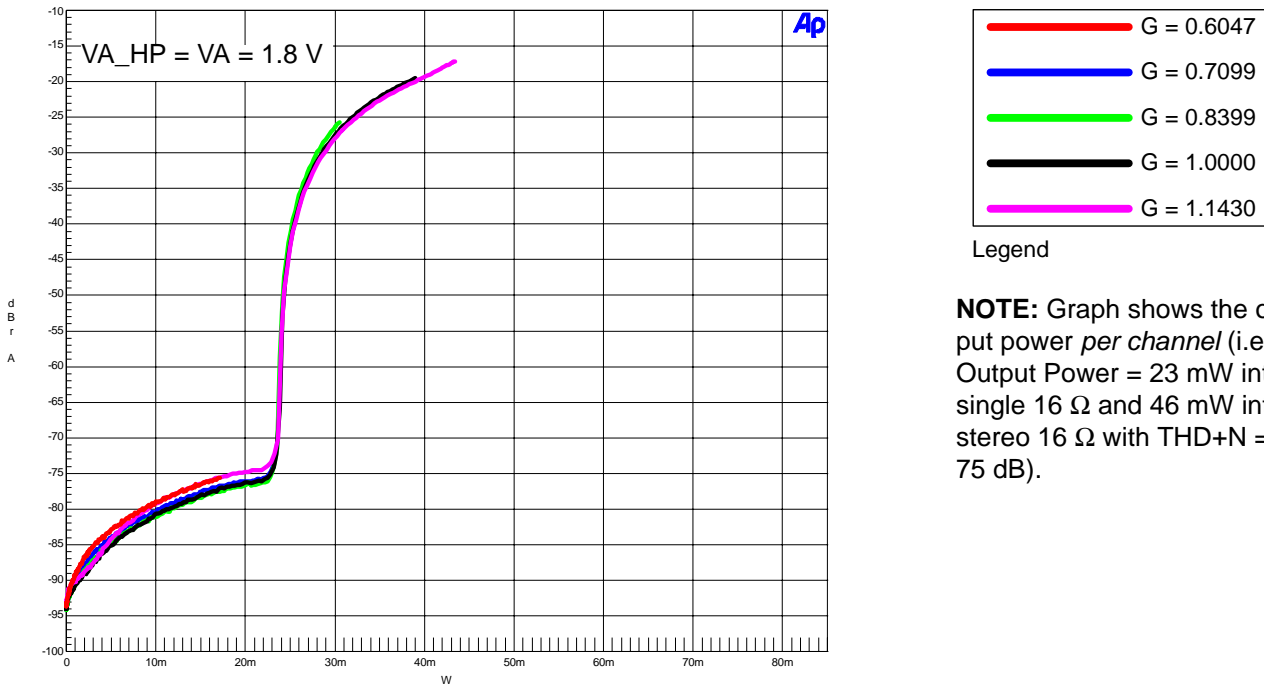


Figure 27. THD+N vs. Output Power per Channel at 1.8 V (16 Ω load)

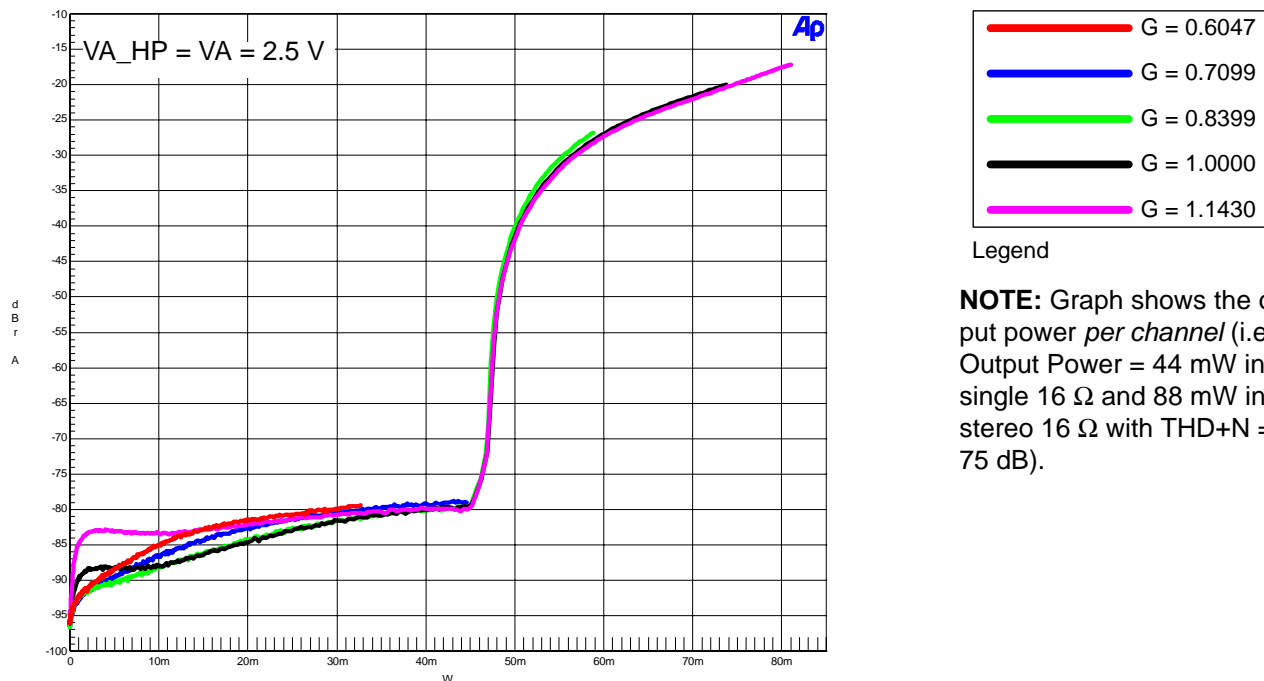


Figure 28. THD+N vs. Output Power per Channel at 2.5 V (16 Ω load)

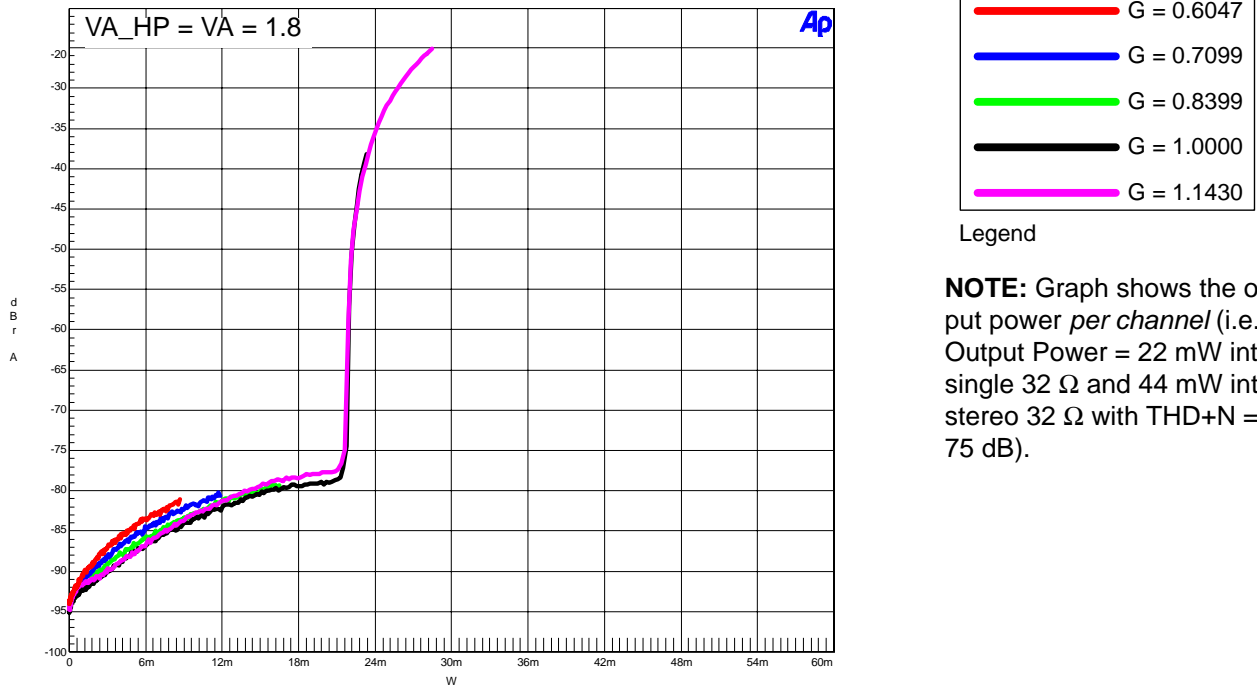


Figure 29. THD+N vs. Output Power per Channel at 1.8 V (32 Ω load)

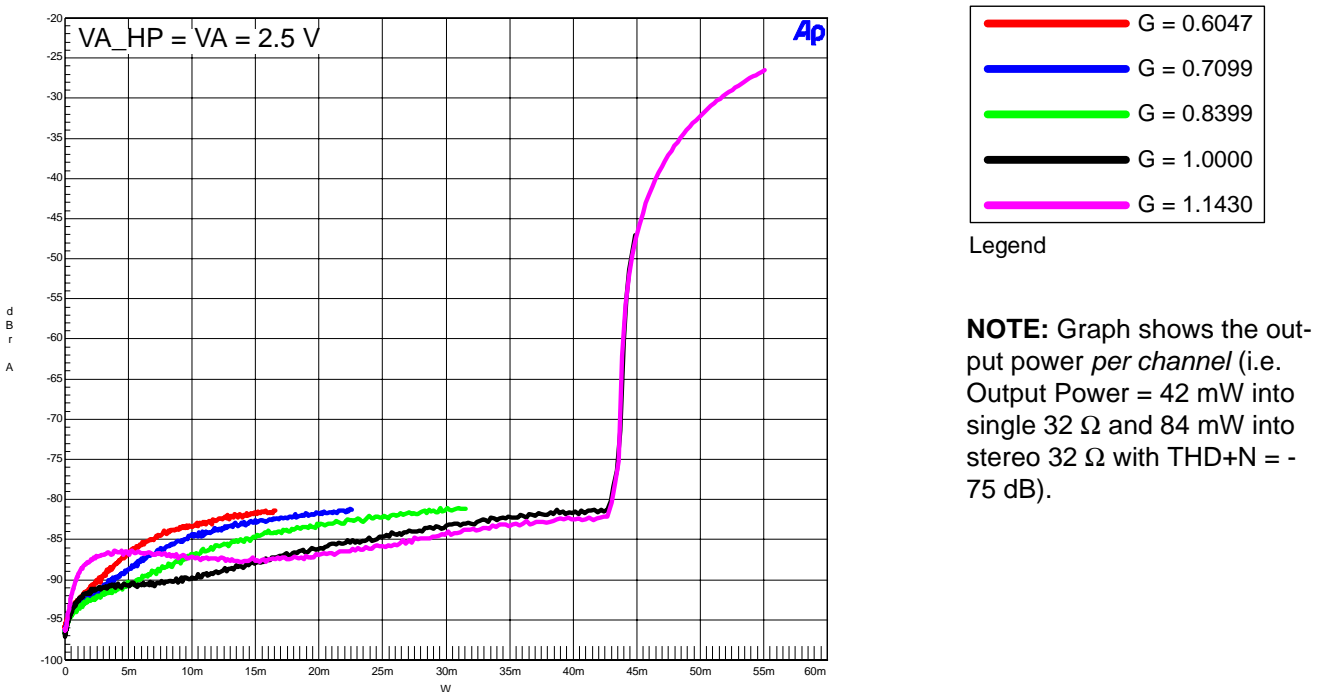


Figure 30. THD+N vs. Output Power per Channel at 2.5 V (32 Ω load)

7.2 Headphone Amplifier Efficiency

The architecture of the headphone amplifier is that of typical class AB amplifiers. Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; Power Consumption Mode 6 - Stereo Playback w/16 Ω load. HP_GAIN = 1.1430. Best efficiency is realized when the amplifier outputs maximum power.

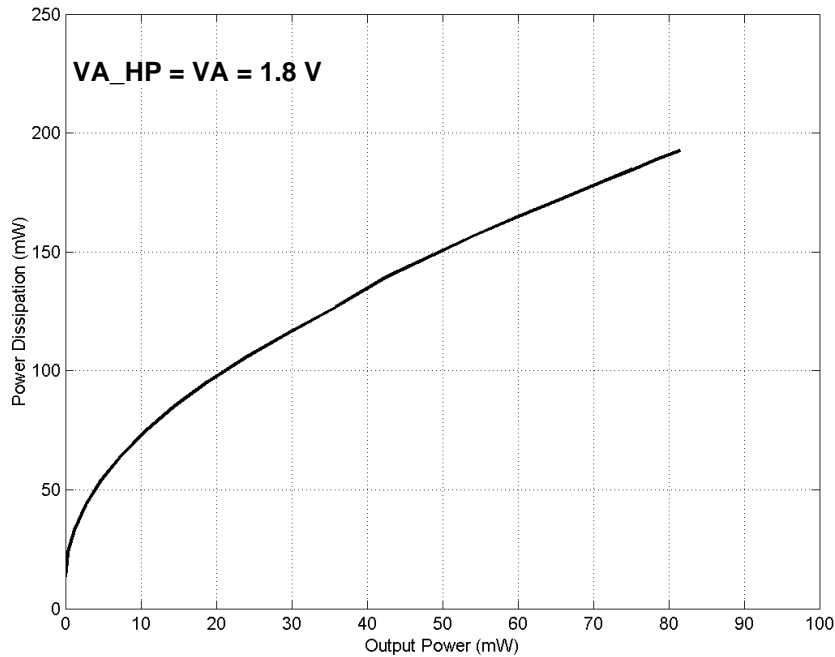


Figure 31. Power Dissipation vs. Output Power into Stereo 16 Ω

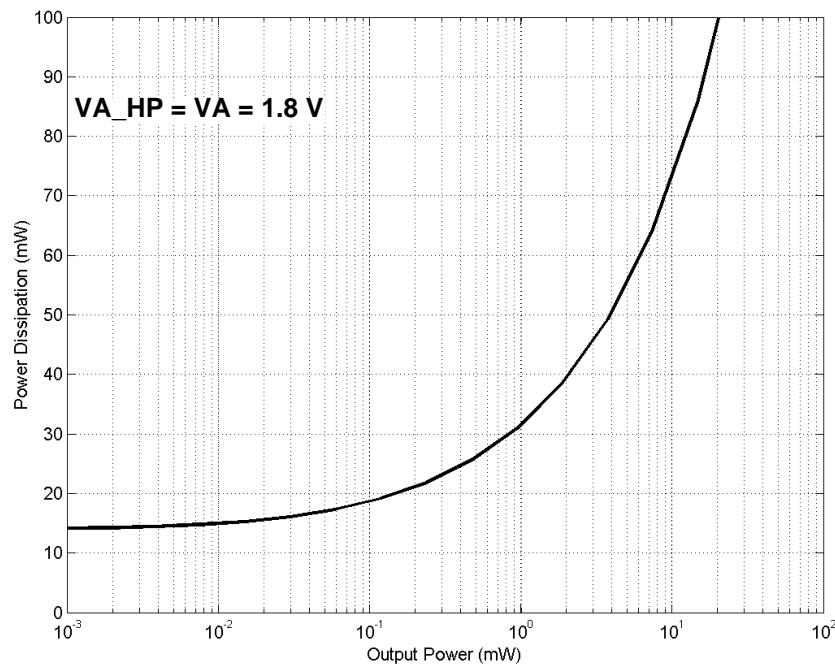


Figure 32. Power Dissipation vs. Output Power into Stereo 16 Ω (Log Detail)

7.3 ADC_FILT+ Capacitor Effects on THD+N

The value of the capacitor on the ADC_FILT+ pin, 16, affects the low frequency total harmonic distortion + noise (THD+N) performance of the ADC. Larger capacitor values yield significant improvement in THD+N at low frequencies. Figure 33 shows the THD+N versus frequency for the ADC analog input. Plots were taken from the CDB42L51 using an Audio Precision analyzer.

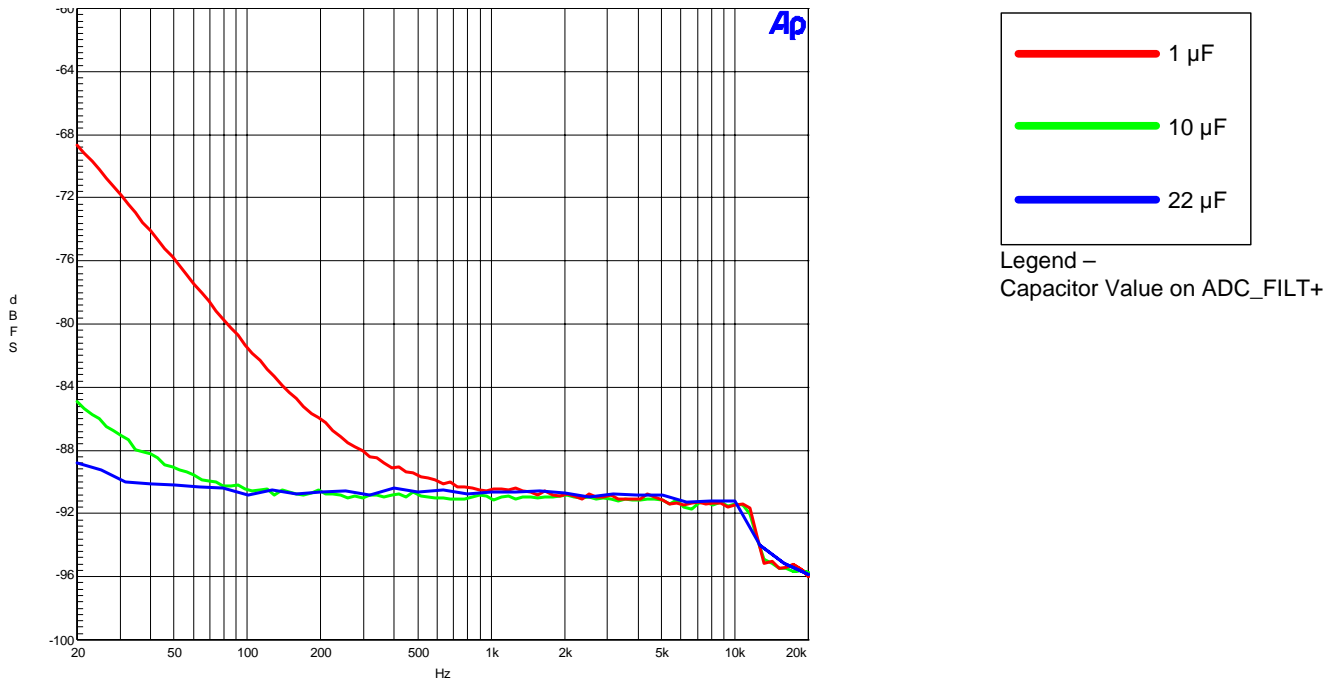


Figure 33. ADC THD+N vs. Frequency w/Capacitor Effects

8. EXAMPLE SYSTEM CLOCK FREQUENCIES

8.1 Auto Detect Enabled

Sample Rate LRCK (kHz)	MCLK (MHz)			
	1024x	1536x	2048x*	3072x*
8	8.1920	12.2880	16.3840	24.5760
11.025	11.2896	16.9344	22.5792	33.8688
12	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	512x	768x	1024x*	1536x*
16	8.1920	12.2880	16.3840	24.5760
22.05	11.2896	16.9344	22.5792	33.8688
24	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	256x	384x	512x*	768x*
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	128x	192x	256x*	384x*
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

*The "MCLKDIV2" pin 4 must be set HI.

8.2 Auto Detect Disabled

Sample Rate LRCK (kHz)	MCLK (MHz)					
	512x	768x	1024x	1536x	2048x	3072x
8	-	6.1440	8.1920	12.2880	16.3840	24.5760
11.025	-	8.4672	11.2896	16.9344	22.5792	33.8688
12	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)					
	256x	384x	512x	768x	1024x	1536x
16	-	6.1440	8.1920	12.2880	16.3840	24.5760
22.05	-	8.4672	11.2896	16.9344	22.5792	33.8688
24	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	256x	384x	512x	768x
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	128x	192x	256x	384x
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

9. PCB LAYOUT CONSIDERATIONS

9.1 Power Supply, Grounding

As with any high-resolution converter, the CS42L51 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. [Figure 1 on page 10](#) shows the recommended power arrangements, with VA and VA_HP connected to clean supplies. VD, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VD may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS42L51 as possible. The low value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS42L51 to minimize inductance effects. All signals, especially clocks, should be kept away from the DAC_FILTER+/ADC_FILTER+ and VQ pins in order to avoid unwanted coupling into the modulators. The DAC_FILTER+/ADC_FILTER+ and VQ decoupling capacitors, particularly the 0.1 μ F, must be positioned to minimize the electrical path from DAC_FILTER+/ADC_FILTER+ and AGND. The CDB42L51 evaluation board demonstrates the optimum layout and power supply arrangements.

9.2 QFN Thermal Pad

The CS42L51 is available in a compact QFN package. The under side of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. In split ground systems, it is recommended that this thermal pad be connected to AGND for best performance. The CS42L51 evaluation board demonstrates the optimum thermal pad and via configuration.

10.ADC & DAC DIGITAL FILTERS

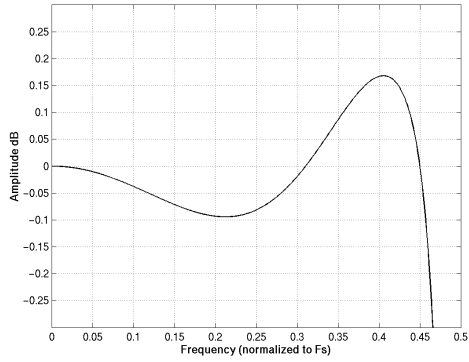


Figure 34. ADC Passband Ripple

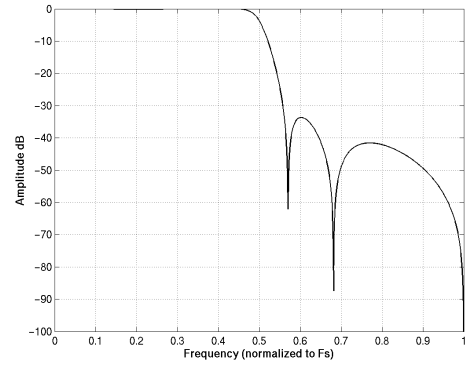


Figure 35. ADC Stopband Rejection

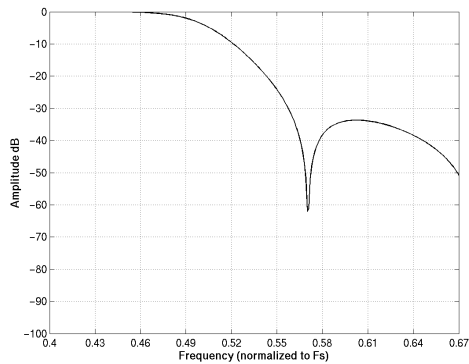


Figure 36. ADC Transition Band

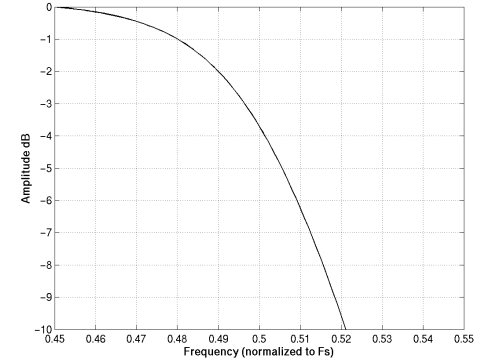


Figure 37. ADC Transition Band Detail

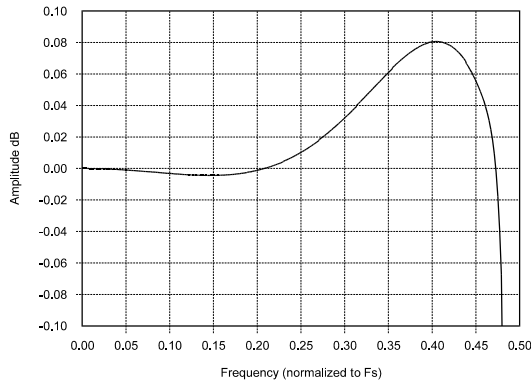


Figure 38. DAC Passband Ripple

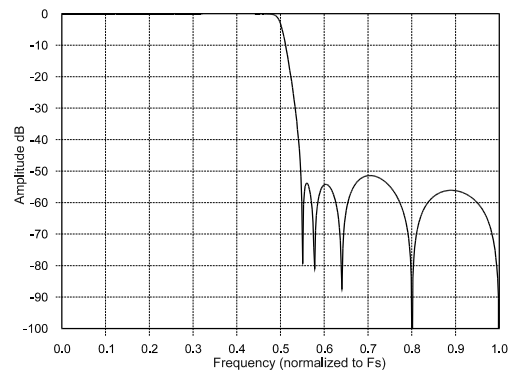


Figure 39. DAC Stopband

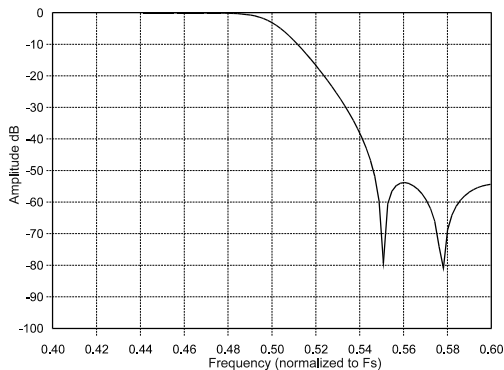


Figure 40. DAC Transition Band

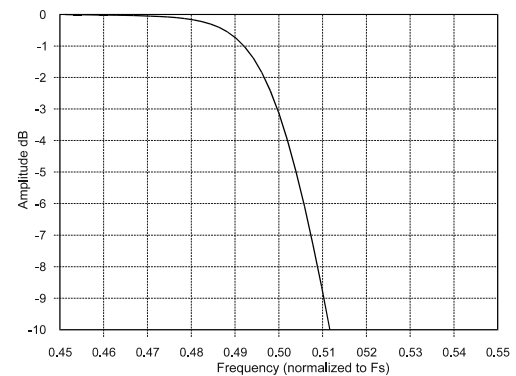


Figure 41. DAC Transition Band (Detail)

11.PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channel pairs. Units in decibels.

Gain Error

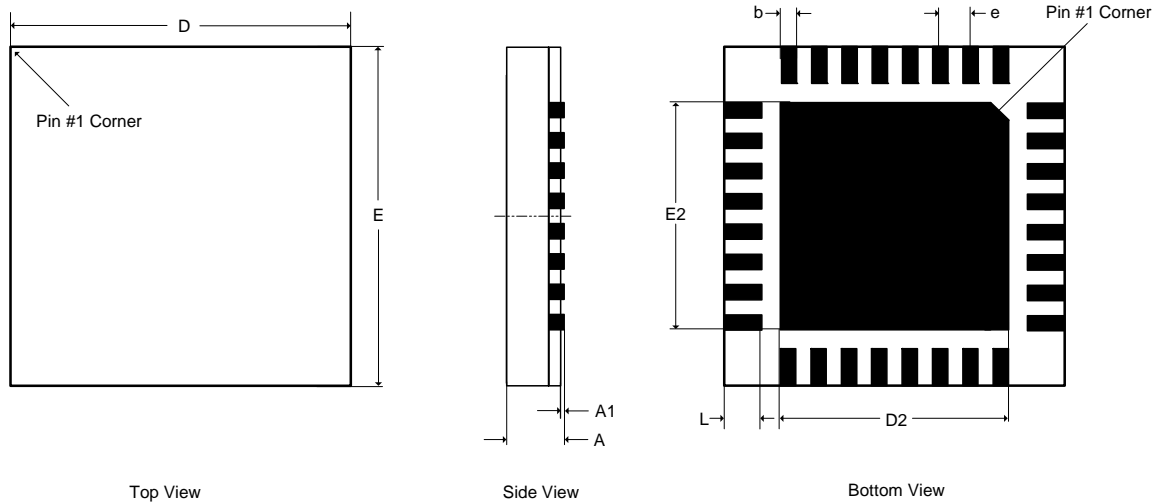
The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

12.PACKAGE DIMENSIONS
32L QFN (5 X 5 mm BODY) PACKAGE DRAWING


DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0394	--	--	1.00	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0071	0.0091	0.0110	0.18	0.23	0.28	1,2
D	0.1969 BSC			5.00 BSC			1
D2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
E	0.1969 BSC			5.00 BSC			1
E2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
e	0.0197 BSC			0.50 BSC			1
L	0.0118	0.0157	0.0197	0.30	0.40	0.50	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

1. Dimensioning and tolerance per ASME Y 14.5M-1995.
2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	θ_{JA}	-	52	-	°C/Watt
2 Layer Board 4 Layer Board		-	38	-	

13. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42L51	Low-Power Stereo CODEC w/HP Amp for Portable Apps	32L-QFN	Yes	Commercial	-10 to +70° C	Rail	CS42L51-CNZ
						Tape & Reel	CS42L51-CNZR
				Automotive	-40 to +85° C	Rail	CS42L51-DNZ
						Tape & Reel	CS42L51-DNZR
CDB42L51	CS42L51 Evaluation Board	-	No	-	-	-	CDB42L51
CRD42L51	CS42L51 Reference Design	-	No	-	-	-	CRD42L51

14. REFERENCES

1. Cirrus Logic, *AN18: Layout and Design Rules for Data Converters and Other Mixed Signal Devices*, Version 6.0, February 1998.
2. Cirrus Logic, *Techniques to Measure and Maximize the Performance of a 120 dB, 96 kHz A/D Converter Integrated Circuit*, by Steven Harris, Steven Green and Ka Leung. Presented at the 103rd Convention of the Audio Engineering Society, September 1997.
3. Cirrus Logic, *A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio*, by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.
4. Cirrus Logic, *The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's*, by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
5. Cirrus Logic, *An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example*, by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
6. Cirrus Logic, *How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters*, by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.
7. Cirrus Logic, *A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range*, by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
8. Philips Semiconductor, *The I²C-Bus Specification: Version 2.1*, January 2000.
<http://www.semiconductors.philips.com>

15. REVISION HISTORY

Revision	Changes
A1	Initial Release
A2	<p>Renamed pin 14, FILT1+, to DAC_FILT+ and pin 16, FILT2+, to ADC_FILT+.</p> <p>Added 1.5 μF capacitor recommendation to figure “Typical Connection Diagram (Software Mode)” on page 10.</p> <p>Removed the 0.1μF capacitors from pins DAC_FILT+, ADC_FILT+ and VQ on the figures “Typical Connection Diagram (Software Mode)” on page 10 and “Typical Connection Diagram (Hardware Mode)” on page 11.</p> <p>Added DAC Isolation specification to “Analog Input Characteristics (Commercial - CNZ)” on page 13 and “Analog Input Characteristics (Automotive - DNZ)” on page 14.</p> <p>Corrected specification table “Headphone Output Power Characteristics” on page 19.</p> <p>Removed t_d timing specification from table in section “Switching Specifications - Serial Port” on page 20.</p> <p>Added $t_{s(SDO-SK)}$ and $t_{h(SK-SDO)}$ timing specification to table in section “Switching Specifications - Serial Port” on page 20.</p> <p>Adjusted timing specifications $t_{s(SD-SK)}$ from 0 ns to 20 ns and t_h from 50 ns to 20 ns in table in section “Switching Specifications - Serial Port” on page 20.</p> <p>Added MIC Bias PSRR specification to “DC Electrical Characteristics” on page 24.</p> <p>Adjusted specification table “Power Consumption” on page 25.</p> <p>Removed QSM clock ratios 128, 192, 256, 384 and HSM ratios 128, 192 from Table 3 on page 39.</p> <p>Modified Digital Mix description in section “Digital Mix (DIGMIX)” on page 53.</p> <p>Corrected DAC Zero Cross timeout period in section “Zero Cross” on page 59.</p> <p>Adjusted BEEP off time settings in section “Beep Off Time (OFFTIME[2:0])” on page 63.</p> <p>Modified BEEP description in section “Beep (BEEP)” on page 64.</p> <p>Adjusted the minimum settings for the “Noise Gate Boost (NG_BOOST) and Threshold (THRESH[3:0])” on page 72.</p> <p>Swapped bits PCMA_OVFL w/PCMB_OVFL and ADCA_OVFL w/ADCB_OVFL in register “Status (Address 20h) (Read Only)” on page 73.</p> <p>Corrected Charge Pump Frequency setting in section “Charge Pump Frequency (CHRG_FREQ[3:0])” on page 74.</p> <p>Added sections “Headphone THD+N versus Output Power Plots” on page 75 and “ADC_FILT+ Capacitor Effects on THD+N” on page 78.</p>

Revision	Changes
PP1	<p>Adjusted the minimum voltage specification in “Specified Operating Conditions” section on page 12.</p> <p>Adjusted Ambient Operating Temp. specification in “Absolute Maximum Ratings” section on page 12.</p> <p>Adjusted maximum “Analog In to PGA to ADC” THD+N performance specification in “Analog Input Characteristics (Commercial - CNZ)” on page 13.</p> <p>Added Offset Error specification to “Analog Input Characteristics (Commercial - CNZ)” on page 13 and “Analog Input Characteristics (Automotive - DNZ)” on page 14.</p> <p>Corrected Interchannel Gain Mismatch specification in “Analog Input Characteristics (Commercial - CNZ)” on page 13 and “Analog Input Characteristics (Automotive - DNZ)” on page 14.</p> <p>Adjusted ADC full scale input voltage specification in “Analog Input Characteristics (Commercial - CNZ)” on page 13 and “Analog Input Characteristics (Automotive - DNZ)” on page 14.</p> <p>Corrected Group Delay characteristic in table in section “ADC Digital Filter Characteristics” on page 15.</p> <p>Adjusted maximum “$R_L = 10k\Omega$” THD+N performance specification in “Analog Output Characteristics (Commercial - CNZ)” on page 16 and “Analog Output Characteristics (Automotive - DNZ)” on page 17.</p> <p>Corrected Group Delay characteristic in table in section “Combined DAC Interpolation & on-Chip Analog Filter Response” on page 20.</p> <p>Adjusted timing specifications $t_{d(MSB)}$ from 40 ns to 52 ns and $t_{s(SDO-SK)}$ from 30 ns to 20 ns in table in section “Switching Specifications - Serial Port” on page 20.</p> <p>Adjusted I²C timing specification t_{ack} from 1000 ns to 3450 ns in table in section “” on page 21.</p> <p>Adjusted High-Level Input Voltage specifications V_{IH} from 0.65VL to 0.68VL and V_{IL} from 0.35VL to 0.32VL in table in section “Digital Interface Specifications & Characteristics” on page 24.</p> <p>Adjusted the +20 dB Digital Boost block before the ALC feedback path in Figure 8 on page 28.</p> <p>Modified ALC Recommended Settings in section “Automatic Level Control (ALC)” on page 32.</p> <p>Modified step 2 of the “Recommended Power-Down Sequence” on page 42.</p> <p>Corrected default values for ALC and Limiter Release Rates shown in “Register Quick Reference” on page 46.</p> <p>Corrected default value for the DAC_SZC bits and Added AMUTE bit and description in “DAC Control (Address 09h)” on page 58.</p> <p>Added section “Headphone Amplifier Efficiency” on page 77.</p> <p>Corrected ADC Filter Response shown in Figures 34, 35, 36, and 37 on page 82.</p> <p>Corrected ADC_SNGVOL description in “MIC Control (Address 05h)” on page 53.</p>
F1	Final Release

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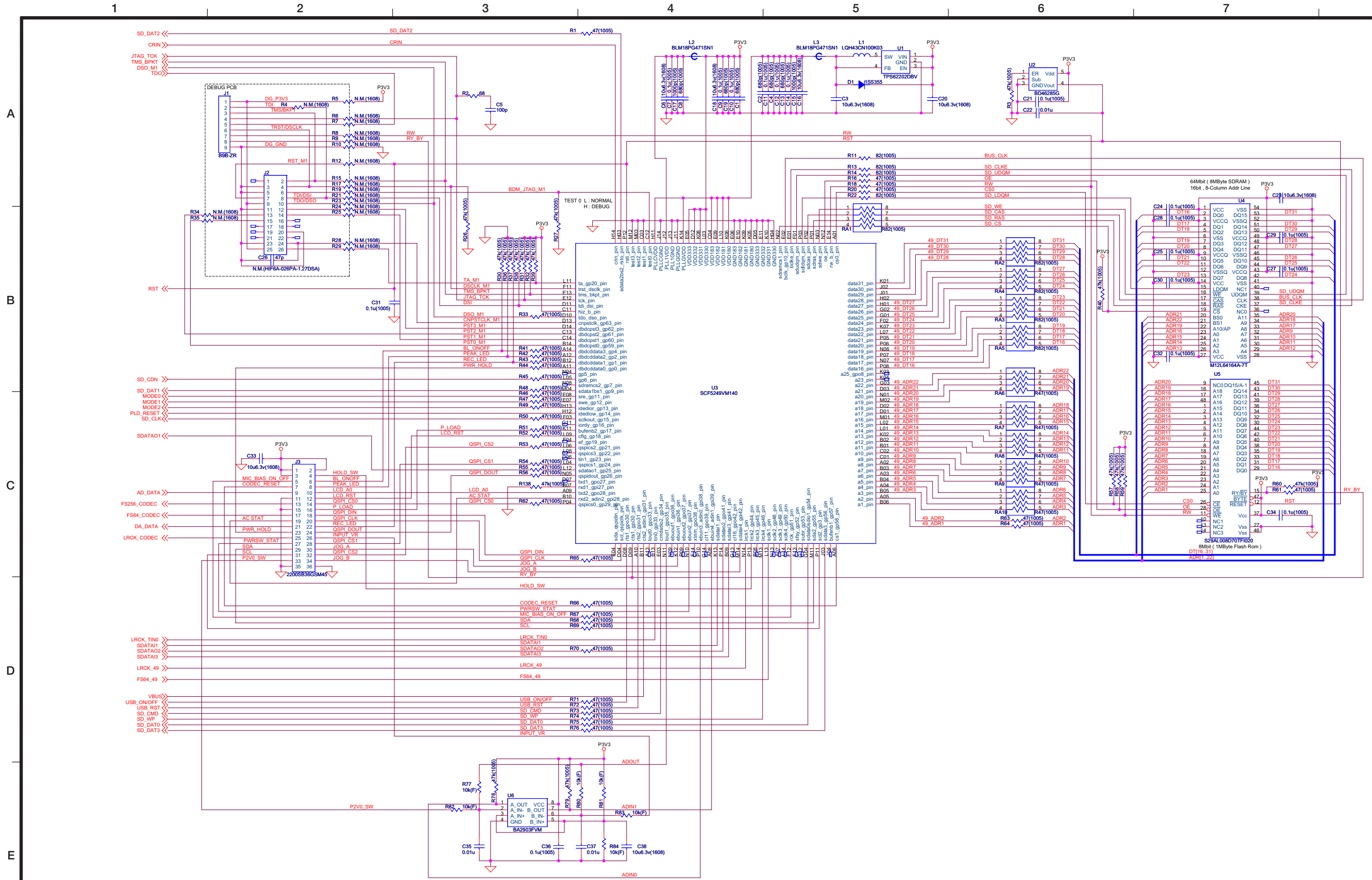
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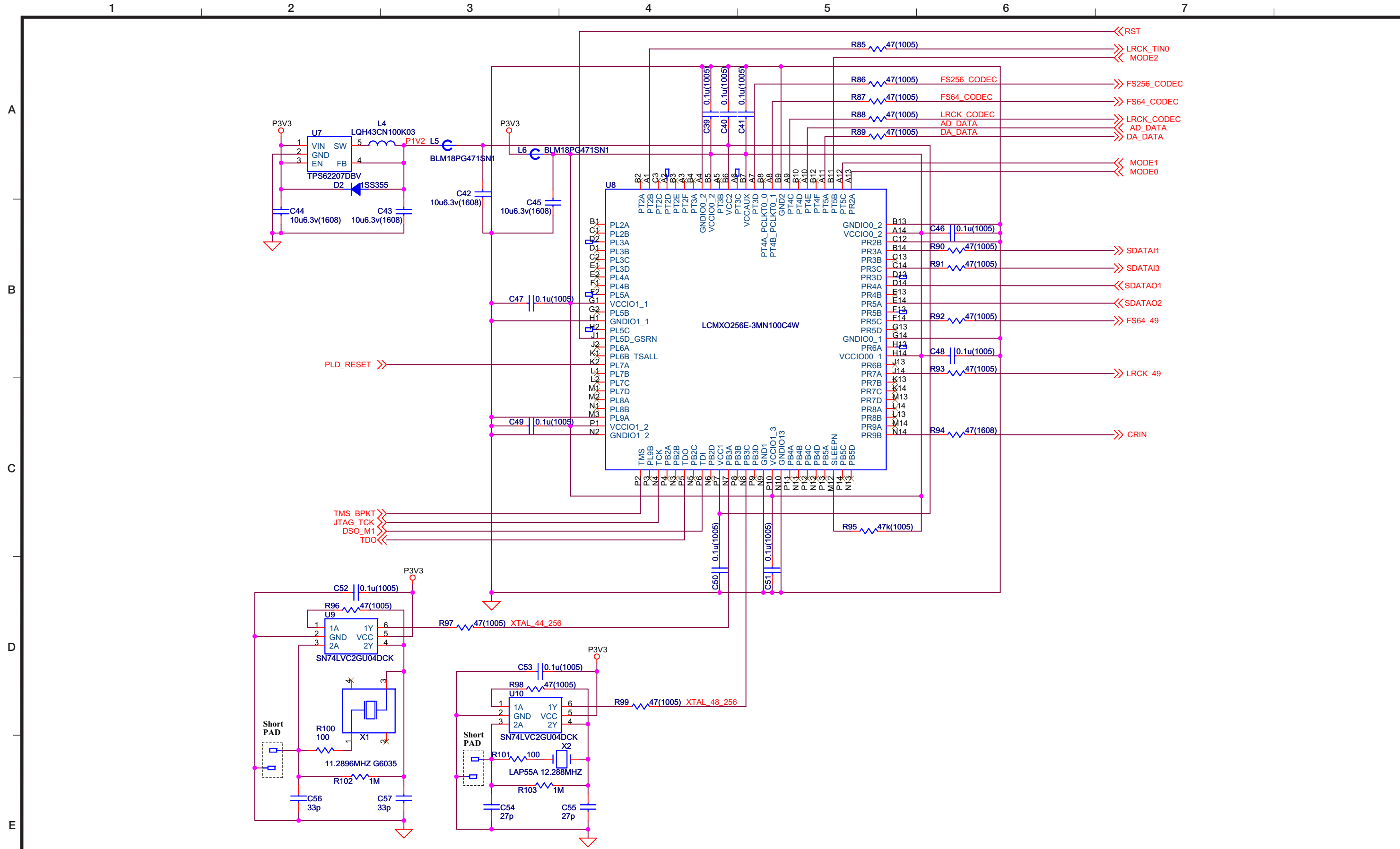
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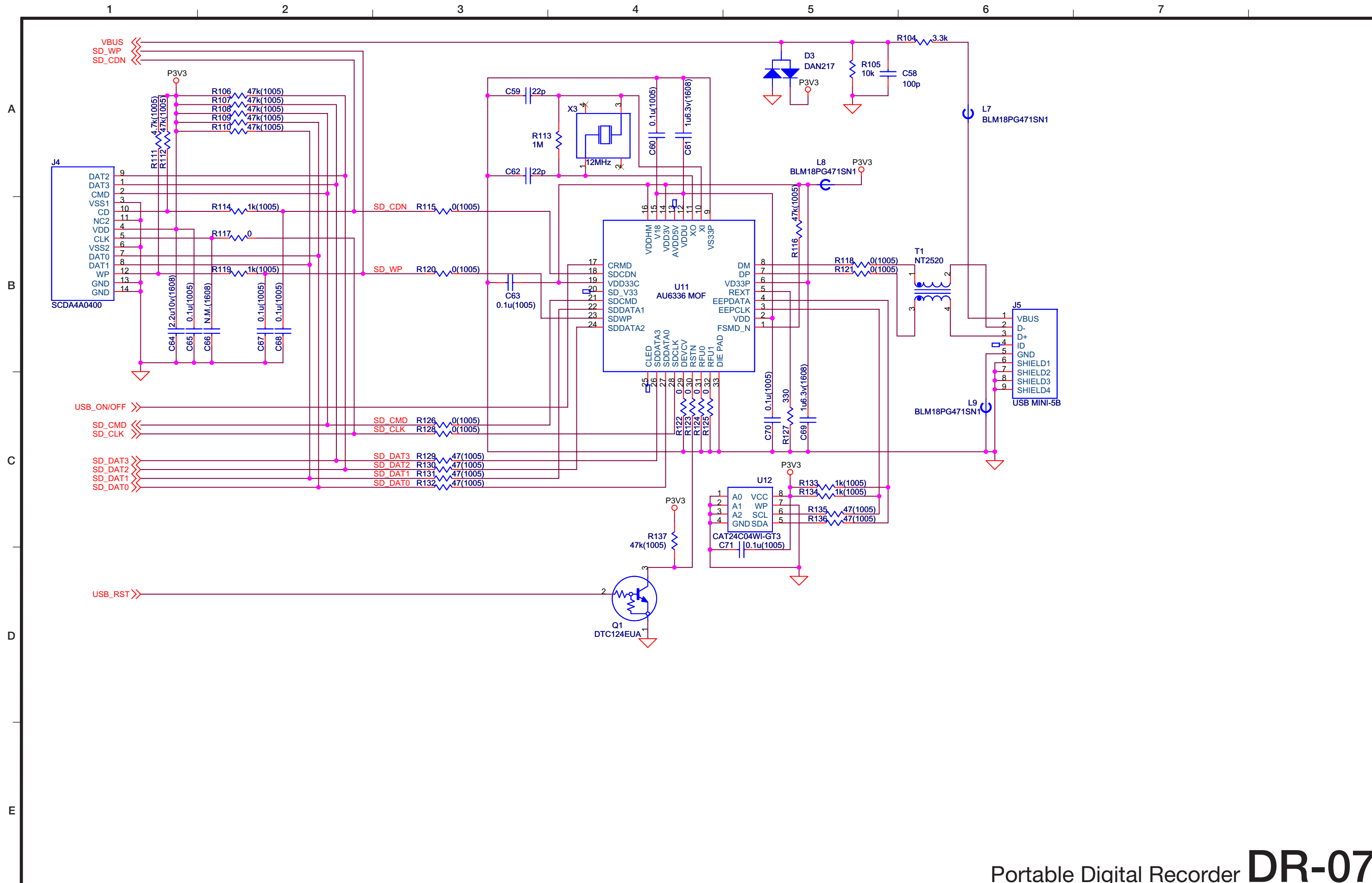
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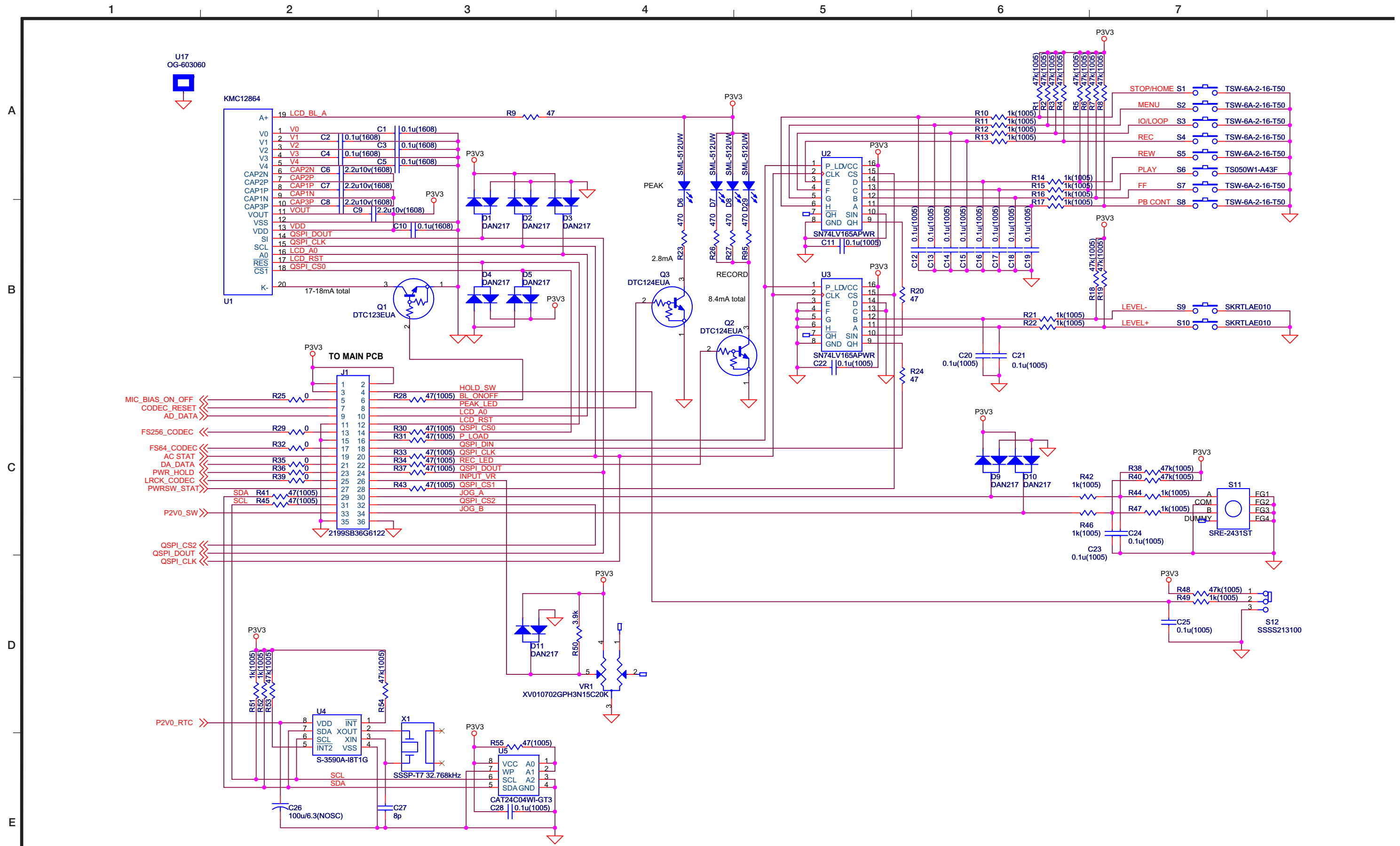
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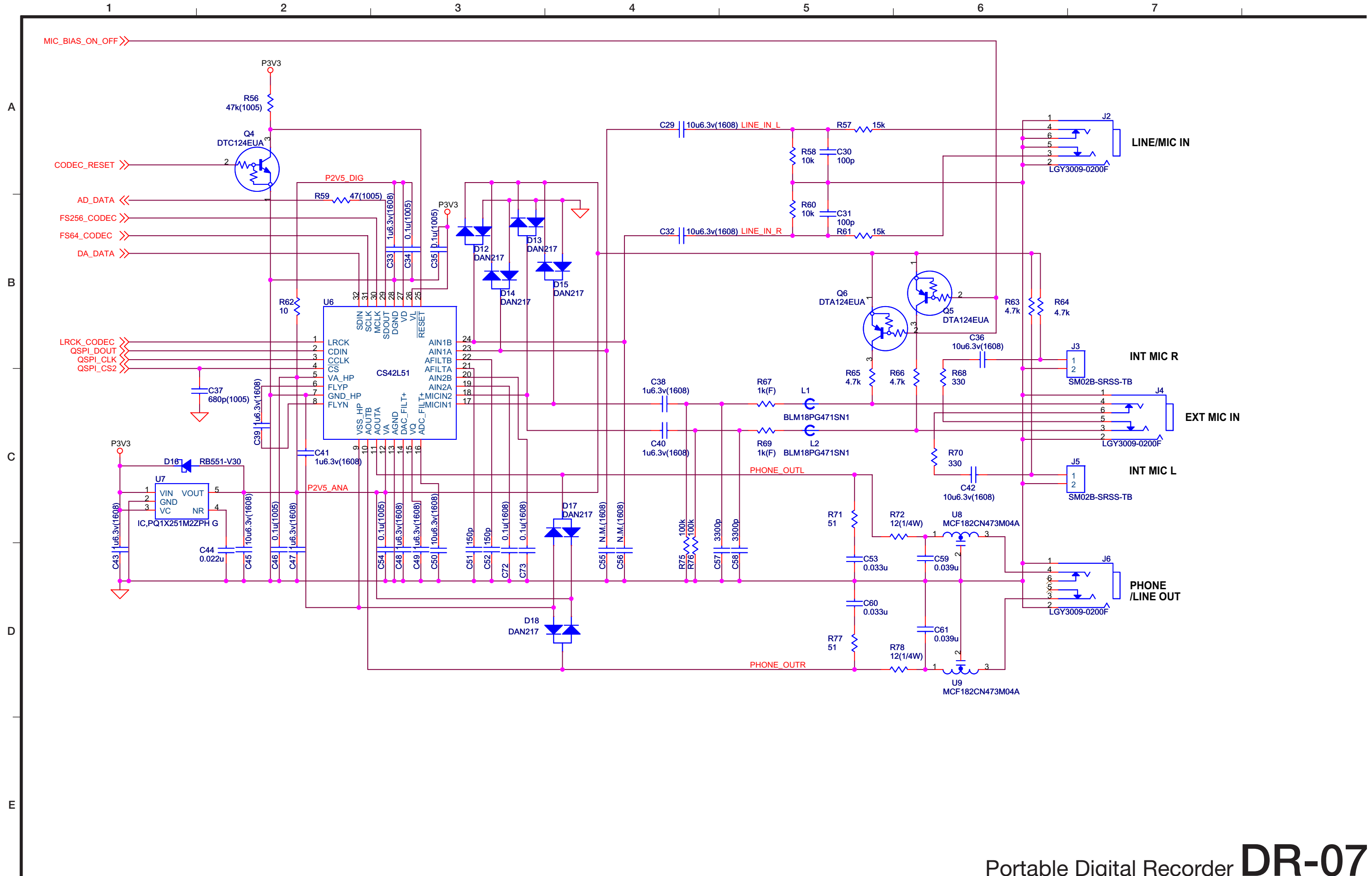
MAIN (1/3)	2
MAIN (2/3)	3
MAIN (3/3)	4
PANEL (1/3)	5
PANEL (2/3)	6
PANEL (3/3)	7

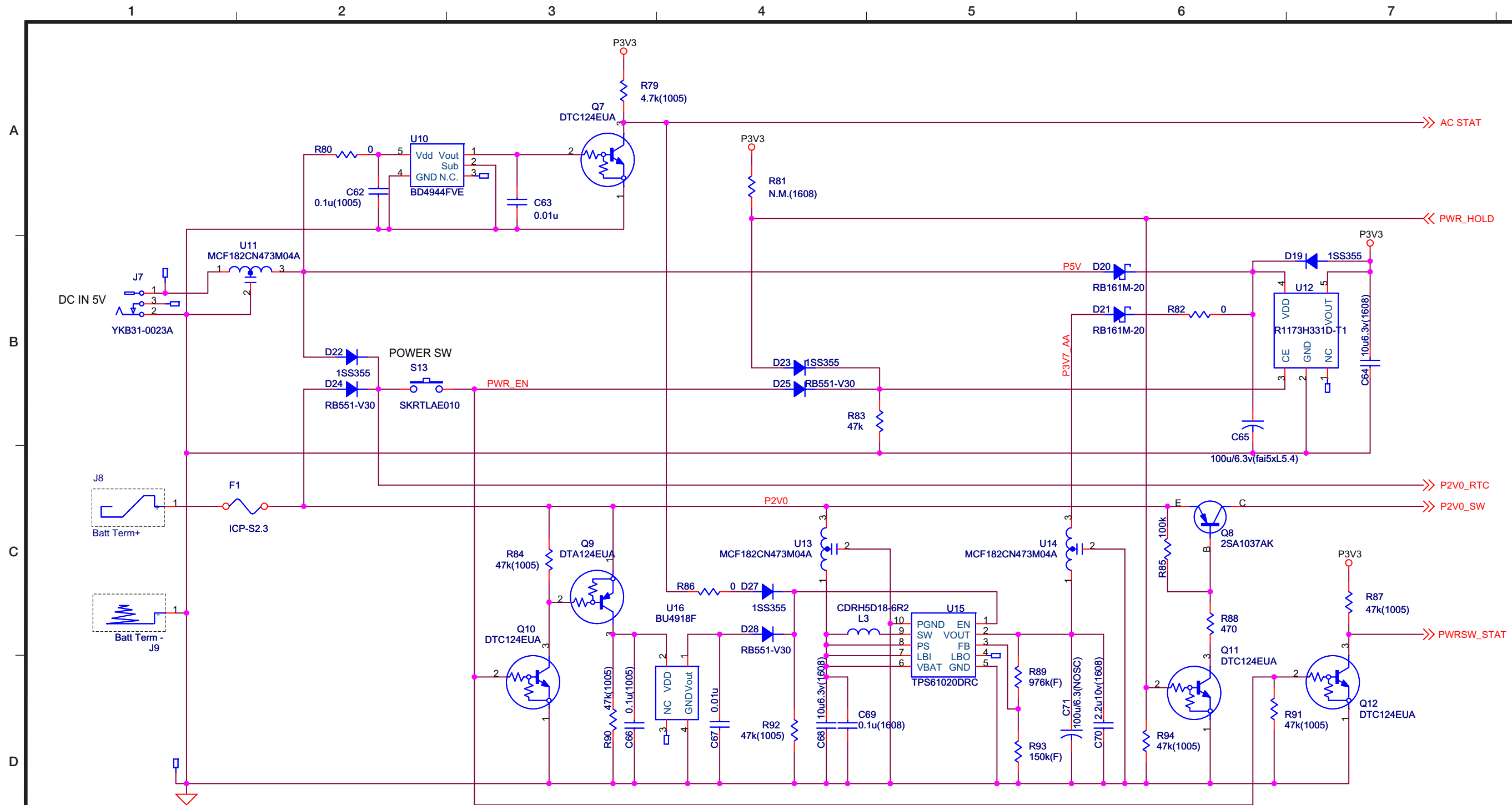












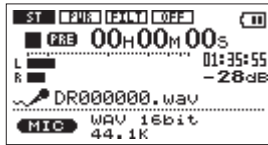
取扱説明書・追補

ファームウェア V1.02 より下記の機能が追加されました。

- マイク入力の音質補正を目的としたフィルター機能を追加しました。

400Hz 以下の音をブーストする機能を追加しました。この機能により、さらに豊かな低域の録音を行うことができます。この機能追加により、以下の点が変更になります。

- 録音画面の上部にある 4 つのアイコンのうち、“LCF” が “FILT” に変わります。



- INPUT SETTING 画面において、“LOW CUT” (LOW CUT FILTER) 項目が “FILTER” に変わります。
- INPUT SETTING 画面の “FILTER” の設定パラメーターの表示が OFF、+ 400Hz、- 40Hz、- 80Hz、- 120Hz になります。



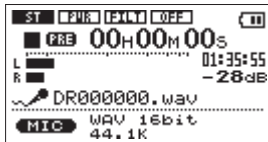
メモ

従来の、低域をカットするローカットフィルター機能の設定は、- 40Hz、- 80Hz、- 120Hz になります。

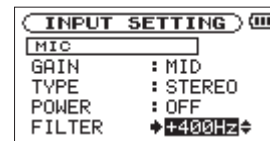
Owner's Manual Addendum

A new filter function has been added from firmware V1.02 for the purpose of enhancing the sound quality of the mic inputs. This new function allows you to boost sound frequencies of 400 Hz and below. By using this function, you can record low frequencies with greater richness. The following changes have been made with the addition of this function.

- The “LCF” icon (third from left) at the top of the Record Screen has been changed to “FILT.”



- On the INPUT SETTING screen, the “LOW CUT” (LOW CUT FILTER) item has been changed to “FILTER.”
- On the INPUT SETTING screen, the “FILTER” item setting parameters now include OFF, +400Hz, -40Hz, -80Hz and -120Hz.



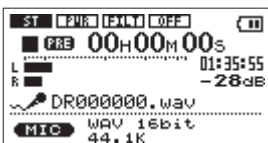
NOTE

The -40Hz, -80Hz and -120Hz still function as before, cutting frequencies below 40, 80 and 120 Hz, respectively.

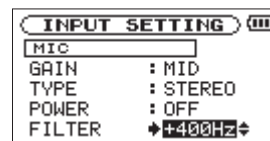
Addendum au mode d'emploi

Une nouvelle fonction de filtre a été ajoutée depuis le firmware V1.02, dans le but d'améliorer la qualité sonore des entrées micro. Cette nouvelle fonction vous permet de renforcer les fréquences audio égales ou inférieures à 400 Hz. Grâce à cette fonction, vous pouvez enregistrer des basses fréquences d'une plus grande richesse. Les changements suivants ont été apportés en plus de cette fonction.

- L'icône “LCF” (troisième à partir de la gauche) a été changée en “FILT” en haut de l'écran d'enregistrement.



- En écran INPUT SETTING, le paramètre “LOW CUT” (FILTRE COUPE-BAS) a été changé en “FILTER” (FILTRE).
- En écran INPUT SETTING, les valeurs de réglage du paramètre “FILTER” sont maintenant OFF, +400Hz, -40Hz, -80Hz et -120Hz.



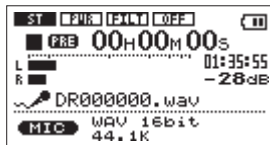
NOTE

Les valeurs -40Hz, -80Hz et -120Hz fonctionnent comme précédemment, coupant les fréquences respectivement sous 40, 80 et 120 Hz.

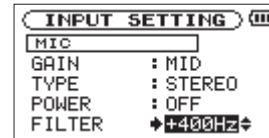
Ergänzung zum Benutzerhandbuch

Die Firmware in der Version 1.02 erweitert den DR-07 um ein neues Filter, das dabei hilft, die Klangqualität der Mikrofoneingänge zu verbessern. Mit dem Filter können Sie Frequenzen unterhalb von 400 Hz anheben und so Ihren Aufnahmen einen satteren Klang im unteren Frequenzbereich verleihen. Mit der Ergänzung dieses Merkmals wurden folgende Änderungen am DR-07 vorgenommen:

- Auf der Aufnahmeseite oben wurde das Displayzeichen LCF (das dritte von links) in FILT. umbenannt.



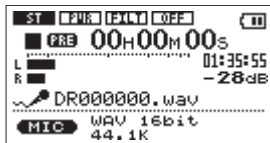
- Auf der INPUT SETTING-Seite wurde der Eintrag LOW CUT (Tiefenabsenkung) in FILTER umbenannt.
- Auf der INPUT SETTING-Seite sind unter FILTER nun die folgenden Einstellungen verfügbar:
 - o OFF (keine Filterung)
 - o +400Hz (Anhebung unterhalb von 400 Hz)
 - o -40Hz (Absenkung unterhalb von 40 Hz)
 - o -80Hz (Absenkung unterhalb von 80 Hz)
 - o -120Hz (Absenkung unterhalb von 120 Hz)



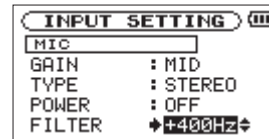
Aggiunta al Manuale di istruzioni

Una nuova funzione del filtro è stata aggiunta con la versione del firmware V1.02, allo scopo di migliorare la qualità del suono all'ingresso microfonico. Questa nuova funzione permette di rinforzare le frequenze del suono di 400 Hz o inferiori. Usando questa funzione è possibile registrare suoni ricchi di basse frequenze. Grazie a questa funzione sono stati apportati i seguenti cambiamenti.

- L'icona "LCF" (la terza da sinistra) nella parte superiore della schermata Record è stata cambiata in "FILT".



- Nella schermata INPUT SETTING, la voce "LOW CUT" (FILTRO TAGLIA BASSI) è stato cambiata in "FILTER".
- Nella schermata INPUT SETTING, la voce "FILTER" ora include i parametri di impostazione OFF, +400Hz, -40Hz, -80Hz e -120Hz.



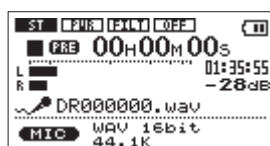
NOTA

I valori -40Hz, -80Hz e -120Hz funzionano come in precedenza, ovvero tagliando le frequenze rispettivamente a 40, 80 e 120 Hz.

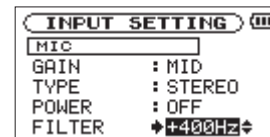
Anexo al manual de instrucciones

Ha sido añadida una nueva función de filtro con respecto al firmware V1.02 con el fin de mejorar la calidad de sonido de las entradas de micro. Esta nueva función también le permite realzar las frecuencias sonoras hasta los 400 Hz. Gracias a esta función, puede grabar bajas frecuencias con una mayor riqueza. La adición de esta función ha dado lugar a los siguientes cambios.

- El icono "LCF" (tercero desde la izquierda) de la parte superior de la pantalla de grabación, ha cambiado ahora a "FILT."



- En la pantalla INPUT SETTING, el elemento "LOW CUT" (FILTRO DE CORTE DE GRAVES) ha sido modificado a "FILTER."
- En la pantalla INPUT SETTING, los parámetros de ajuste del elemento "FILTER" incluyen ahora los valores OFF, +400Hz, -40Hz, -80Hz y -120Hz.



NOTA

Los valores -40Hz, -80Hz y -120Hz siguen funcionando como antes, cortando las frecuencias que están por debajo de los 40, 80 y 120 Hz, respectivamente.

Contents

Updates	1
Maintenance items	1
V1.01 changes	1
Confirmation of firmware version	2
Firmware update procedures	2

Updates

Always use the most recent firmware for this device. Please visit the TASCAM web site at <http://www.tascam.com> to check for the latest firmware.

Maintenance items

V1.01 changes

- A bug that caused the LINE input level to be fixed and prevented **REC LEVEL** volume changes when level control was set to “**AUTO**” has been fixed.
- A bug that caused “**Write Timeout**” to appear when recording an MP3 file at 48-kHz sampling frequency has been fixed.
- A bug that prevented recording from continuing correctly after using the track increment function when **PRE REC** was set to **ON** has been fixed.
- A bug that prevented recording an MP3 file from continuing correctly after pausing and resuming recording has been fixed.

Confirmation of firmware version

Confirm the firmware version of your DR-07 before conducting a firmware update.

- 1 Turn the unit's power ON.
- 2 Press the MENU key to open the MENU screen, select "INFORMATION" and press the ►/|| key.
- 3 Turn the wheel right to confirm the "System Ver." displayed at the bottom.

You do not need to update the unit's firmware if the version shown is the same as or newer than the version that you intend to use for the update.

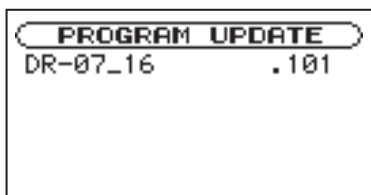
Firmware update procedures

CAUTION

When you updated the firmware, make sure that the batteries have enough remaining power or use an optional AC adapter (PS-P520). The program has been set so that the update will not be conducted if battery power is insufficient.

- 1 Download the most recent firmware from the TASCAM web site (<http://www.tascam.com>).
- 2 Turn the unit's power ON and use the included USB cable to connect it with a computer. This unit will be recognized as an external drive (external storage device) by the computer.
- 3 Copy the downloaded firmware to the UTILITY folder on the DR-07.
- 4 After copying has completed, disconnect the unit from the computer following the correct procedures, remove the USB cable. The unit automatically restarts. Then, turn its power OFF.
- 5 While pressing and holding both the MENU and ►/|| keys, turn the unit power ON.

The unit starts up in update mode, and the update file appears on the screen.



NOTE

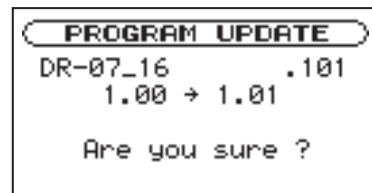
- This screen shows a list of the firmware update files inside the UTILITY folder of the unit. Also, the screen shows the firmware copied at Step 3 above. "No Update File" appears if there is no update file in the UTILITY folder.

- The screen shown is an example. The actual display differs.

CAUTION

If this screen does not appear, turn the power OFF. Then while pressing and holding both the MENU and ►/|| keys, turn the unit's power ON again. Continue to press and hold the MENU and ►/|| keys firmly until this screen appears.

- 6 Select the firmware (highlight the item) then press ►/||. The following screen appears.



The current version appears on the left and the updated version appears on the right.

NOTE

- The screen shown is an example. The actual display differs.

- 7 Press the ►/|| key to start the update.
- 8 When the update is complete, the power turns OFF automatically. Turn the power ON again.
- 9 Follow the "Confirmation of firmware version" instructions above to check that the "System Vers." is now the most recent version of the firmware.

This completes the procedure for updating this unit.

- 10 Connect to a computer with USB and delete the firmware update from the unit's UTILITY folder.

Contents

Updates	1
New function.....	1
V1.02 addition	1
Maintenance items	1
V1.01 changes	1
Confirmation of firmware version	2
Firmware update procedures	2

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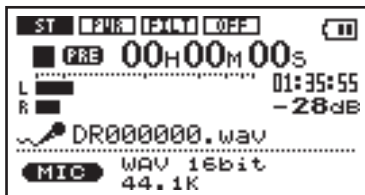
New function

V1.02 addition

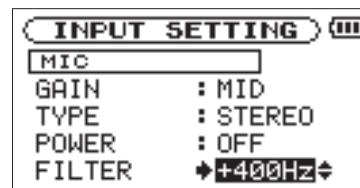
- A new filter function has been added for the purpose of enhancing the sound quality of the mic inputs.

This new function allows you to boost sound frequencies of 400 Hz and below. By using this function, you can record low frequencies with greater richness. The following changes have been made with the addition of this function.

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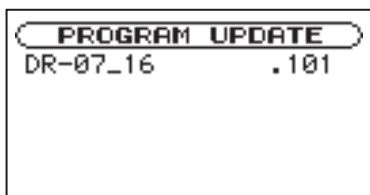
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CAUTION

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- 5 While pressing and holding both the MENU and ►/|| keys, turn the unit power ON.

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NOTE

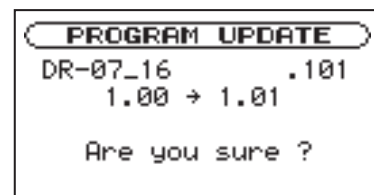
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CAUTION

If this screen does not appear, turn the power OFF. Then while pressing and holding both the MENU and ►/|| keys, turn the unit's power ON again. Continue to press and hold the MENU and ►/|| keys firmly until this screen appears.

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- 8 When the update is complete, the power turns OFF automatically. Turn the power ON again.
- 9 Follow the "Confirmation of firmware version" instructions above to check that the "System Vers." is now the most recent version of the firmware.

This completes the procedure for updating this unit.

- 10 Connect to a computer with USB and delete the firmware update from the unit's UTILITY folder.



TECHNICAL INFORMATION

TASCAM DR-07, V1.02 Firmware Update

No. **0926**

DATE 5th Aug 2009

The firmware V1.02 for DR-07 has been released with some improvements from V1.01. V1.02 on DR-07 has been installed since SN 0080001.

New feature

A new filter function has been added for the purpose of enhancing the sound quality of the mic inputs. This new function allows you to boost the sound frequencies of 400Hz and below.

Improvement and Bug fixes:

1. The very low level noise (-85dbV) of high-pitch (approx. 1kHz) occurred in the input sound during recording, when record ready, or when input monitoring was ON. – fixed –

How to Firmware Update

Refer to DR-07 Release Notes “Firmware Update Procedures”.

Visit the [ROM Data Library](#) in the TASCAM Service HP website to download firmware and refer to DR-07 Release Note for further details.



TECHNICAL INFORMATION

TASCAM DR-07, V1.01 Firmware Update

No. 0911

DATE 27th March 2009

The firmware V1.01 for DR-07 has been released with some improvements from V1.00. V1.01 on DR-07 has been installed since SN 0030001.

Improvement and Bug fixes:

1. The LINE input level was fixed and REC LEVEL could not be changed when Level Control was set to "AUTO". –fixed-
2. "Write Timeout" might be appeared when recording an MP3 file at 48kHz sampling frequency. –fixed-
3. The recording could not be done correctly after using the track increment when PRE REC was set to ON. – fixed-
4. The recording an MP3 file could not be done correctly after pausing and resuming recording when PRE REC was set to ON. – fixed –

How to Firmware Update:

Refer to Service Manual "3.Updating of Firmware" page 8.

Visit the [ROM Data Library](#) in the TASCAM Service HP website to download firmware and refer to DR-07 Release Note for further details..



TECHNICAL INFORMATION

No. 0921

TASCAM DR-07, Countermeasure for No Boot up

DATE 5th June 2009

The countermeasure for No Boot up on DR-07 has been found.
The modification for it has been applied since SN 0050001.

Symptom:

DR-07 might not boot up after Power On with Batteries power. This trouble was likely to happen with using a kind of 8GB SD card.

Cause:

The U15 (TPS61020DRC the first internal DC-DC convertor for 3.7V) might not boot up with some circumstance of the mixing of battery's voltage and the overload of the next stage.

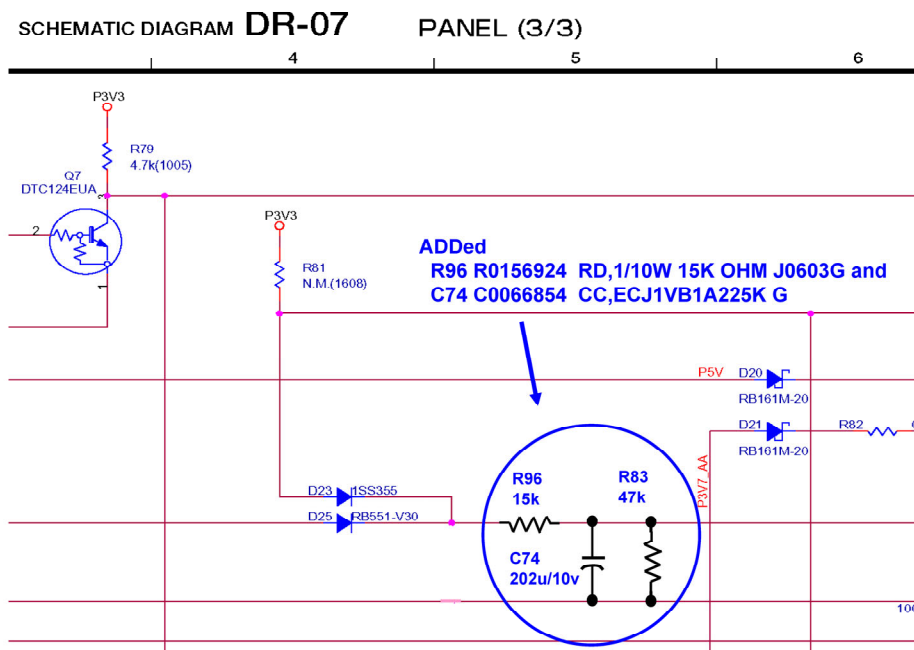
Remedy:

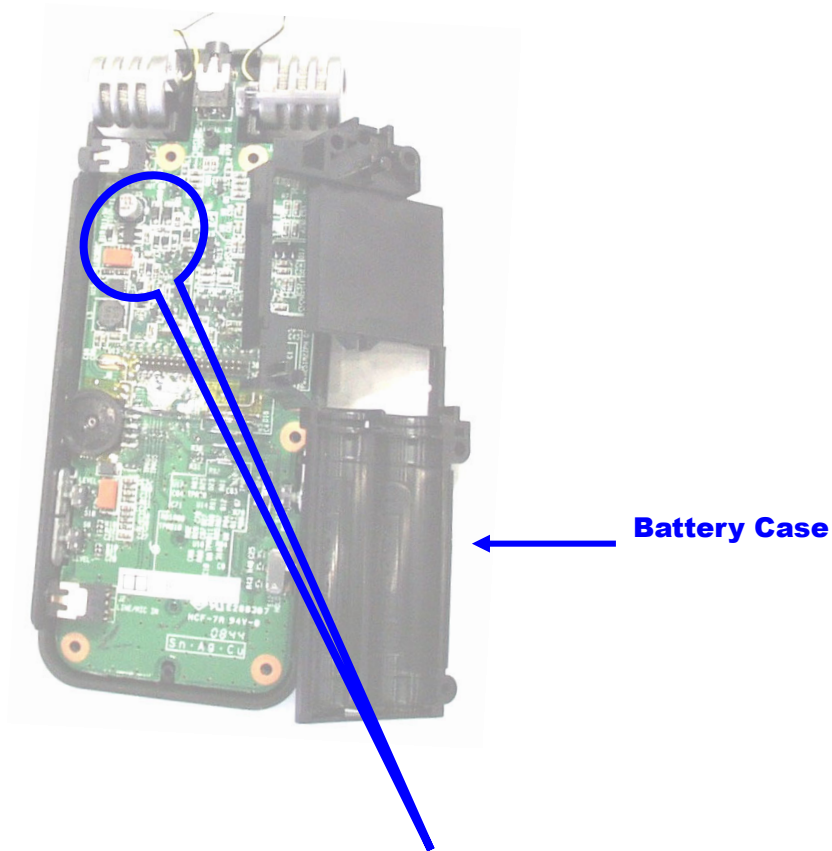
Adding a ceramic capacitor (2.2uF) and a resister (15kohm) makes the delay circuit for U12 (R1173H331D-T1 the internal 3.3V LDO), and makes U15 boot up surely with low overload.

Modification:

Cut one pattern and add a ceramic capacitor C0066854 2.2uF CC, EC J1 VB1A225K and a resister 15kohm R0156924 RD,1/10W 15K OHM J0603G on Panel PCBA.

Refer to the following figures for details of the modification.





Panel PCB Assy

