

TASCAM[®]
TEAC PROFESSIONAL

SERVICE MANUAL

DR-07MKII

Linear PCM Recorder

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1. Specifications

仕様

Ratings

Recording media

microSD card (64 MB - 2 GB)
microSDHC card (4 GB - 32 GB)

Recording/playback format

WAV: 44.1/48/96 kHz, 16/24-bit
MP3: 44.1/48 kHz, 32/64/96/128/192/256/
320 kbps

Number of channels

2 channels (stereo)

Input/output ratings

Analog audio input/output ratings

MIC/EXT IN jacks (supporting plug-in power)

Connector: 1/8" (3.5 mm) stereo mini
Input impedance: 25 k Ω
Nominal input level: -20 dBV
Maximum input level: -4 dBV

/LINE OUT

Connector: 1/8" (3.5 mm) stereo mini
Output impedance: 12 Ω
Nominal output level: -14 dBV (10 k Ω load)
Maximum output level:
+2 dBV (10 k Ω load)
Maximum output: 20 mW + 20 mW (32 Ω load)

Built-in speaker 0.3 W (monaural)

Control input/output ratings

USB jack

Connector: Mini-B type
Format: USB 2.0 HIGH SPEED mass storage class

Audio performance

Frequency response

20 - 20 kHz +1/-3 dB (44.1 kHz, EXT IN to LINE
OUT) (JEITA)
20 - 22 kHz +1/-3 dB (48 kHz, EXT IN to LINE OUT)
(JEITA)
20 - 40 kHz +1/-3 dB (96 kHz, EXT IN to LINE
OUT) (JEITA)

Total harmonic distortion

0.05% or lower (EXT IN to LINE OUT,
Fs 44.1/48/96kHz) (JEITA)

S/N ratio

92dB or higher (EXT IN to LINE OUT,
Fs 44.1/48/96kHz) (JEITA)

Note) JEITA: Conforming to JEITA CP-2150

定格

記録メディア

microSDカード (64MB~2GB)
microSDHCカード (4GB~32GB)

録音再生フォーマット

WAV: 44.1/48/96 kHz, 16/24ビット
MP3: 44.1/48 kHz, 32/64/96/128/
192/256/320 kbps

チャンネル数

2チャンネル (ステレオ)

入出力定格

アナログオーディオ入出力定格

MIC/EXT IN 端子 (プラグインパワー対応)

コネクター: 1/8" (3.5mm) ステレオミニジャック
入力インピーダンス: 25k Ω
基準入力レベル: -20dBV
最大入力レベル: -4dBV

/LINE OUT 端子

コネクター: 1/8" (3.5mm) ステレオミニジャック
出力インピーダンス: 12 Ω
基準出力レベル: -14dBV (10k Ω 負荷時)
最大出力レベル: +2dBV (10k Ω 負荷時)
最大出力: 20mW+20mW (32 Ω 負荷時)

内蔵スピーカー

0.3W (モノラル)

コントロール入出力定格

USB 端子

コネクター: Mini-B タイプ
フォーマット: USB2.0 HIGH SPEED マスストレージ
クラス

オーディオ性能

周波数特性

20-20kHz +1/-3dB (EXT IN to LINEOUT,
Fs44.1kHz, JEITA)
20-22kHz +1/-3dB (EXT IN to LINEOUT,
Fs48kHz, JEITA)
20-40kHz +1/-3dB (EXT IN to LINEOUT,
Fs96kHz, JEITA)

歪率

0.05%以下 (EXT IN to LINE OUT,
Fs44.1k/48k/96 kHz, JEITA)

S/N 比

92dB以上 (EXT IN to LINE OUT,
Fs44.1k/48k/96 kHz, JEITA)

注) JEITA: JEITA CP-2150準拠

Computer compatibility

Windows Pentium 300 MHz or faster
128 MB or more memory
USB port (USB 2.0 recommended)

Macintosh Power PC, iMac, G3, G4 266 MHz or faster
64 MB or more memory
USB port (USB 2.0 recommended)

Recommended USB host controller

Intel chipset

Supported OS

Windows XP, Windows Vista,
Windows 7
Macintosh Mac OS X 10.2 or later

Other specifications

Power Two AA batteries (Alkaline or Ni-MH)
USB bus power supplied from a computer
AC adaptor (TASCAM PS-P515U, sold separately)

Power consumption

1.7 W (maximum)

Battery operation time (continuous operation)

● Alkaline type battery (EVOLTA)

Recording / playback	Format	Operation time	Note
Recording	WAV, 96kHz, 24bit	About 10,5 hours	Built-in microphone
Recording	WAV, 44.1kHz, 16bit	About 17,5 hours	Built-in microphone
Recording	MP3, 44.1kHz, 128Kbps	About 16 hours	Built-in microphone
Recording	MP3, 48kHz, 320Kbps	About 11 hours	Built-in microphone
Playback	WAV, 96kHz, 24bit	About 17 hours	Headphone
Playback	WAV, 96kHz, 24bit	About 17 hours	Built-in speaker
Playback	WAV, 44.1kHz, 16bit	About 19,5 hours	Headphone
Playback	WAV, 44.1kHz, 16bit	About 19,5 hours	Built-in speaker
Playback	MP3, 44.1kHz, 128Kbps	About 19,5 hours	Headphone
Playback	MP3, 44.1kHz, 128Kbps	About 18,5 hours	Built-in speaker

接続するパソコンの動作条件

Windowsマシン Pentium 300MHz以上
128MB 以上のMemory
USBポート (推奨 : USB2.0)

Macintoshマシン Power PC、iMac、G3、G4
266MHz以上
64MB以上のMemory
USBポート (推奨 : USB2.0)

推奨USBホストコントローラー

Intel製チップセット

サポートOS

Windows : Windows XP、Windows Vista、
Windows 7
Macintosh : Mac OS X 10.2以上

一般

電源 単3形電池2本 (アルカリ乾電池またはニッケル水素電池)
パソコンからのUSBバスパワー
専用ACアダプター
(TASCAM PS-P515U、別売)

消費電力 1.7W(最大時)

電池持続時間 (連続使用時)

● アルカリ乾電池 (EVOLTA) 使用時

録音/再生	フォーマット	持続時間	備考
録音時	WAV, 96kHz, 24ビット	約10.5時間	内蔵ステレオマイク入力時
録音時	WAV, 44.1kHz, 16ビット	約17.5時間	内蔵ステレオマイク入力時
録音時	MP3, 44.1kHz, 128kbps	約16時間	内蔵ステレオマイク入力時
録音時	MP3, 48kHz, 320kbps	約11時間	内蔵ステレオマイク入力時
再生時	WAV, 96kHz, 24ビット	約17時間	ヘッドホン使用時
再生時	WAV, 96kHz, 24ビット	約17時間	内蔵素スピーカー使用時
再生時	WAV, 44.1kHz, 16ビット	約19.5時間	ヘッドホン使用時
再生時	WAV, 44.1kHz, 16ビット	約19.5時間	内蔵素スピーカー使用時
再生時	MP3, 44.1kHz, 128kbps	約19.5時間	ヘッドホン使用時
再生時	MP3, 44.1kHz, 128kbps	約18.5時間	内蔵素スピーカー使用時

Recording / playback	Format	Operation time	Note
Playback	MP3,48kHz, 320Kbps	About 19,5 houes	Headphone
Playback	MP3,48kHz, 320Kbps	About 18,5 houes	Built-in speaker

● Ni-MH type battery (eneloop)

Recording / playback	Format	Operation time	Note
Recording	WAV,96kHz, 24bit	About 10 houes	Built-in microphone
Recording	WAV,44.1kHz, 16bit	About 15,5 houes	Built-in microphone
Recording	MP3,44.1kHz, 128Kbps	About 13 houes	Built-in microphone
Recording	MP3,48kHz, 320Kbps	About 11 houes	Built-in microphone
Playback	WAV,96kHz, 24bit	About 15 houes	Headphone
Playback	WAV,96kHz, 24bit	About 14 houes	Built-in speaker
Playback	WAV,44.1kHz, 16bit	About 16,5 houes	Headphone
Playback	WAV,44.1kHz, 16bit	About 16,5 houes	Built-in speaker
Playback	MP3,44.1kHz, 128Kbps	About 16 houes	Headphone
Playback	MP3,44.1kHz, 128Kbps	About 15 houes	Built-in speaker
Playback	MP3,48kHz, 320Kbps	About 16 houes	Headphone
Playback	MP3,48kHz, 320Kbps	About 15 houes	Built-in speaker

Dimensions (W x H x D)

68 x 158 x 26 mm
(25/8" x 63/16" x 1")
(when the microphone pair is close)
90 x 158 x 26 mm
(31/2" x 63/16" x 1")
(when the microphone pair is open)

Weight 127g (47/16 oz)
(not including batteries)

Operating temperature range
0 - 40°C (32°F - 104°F)

録音／再生	フォーマット	持続時間	備考
再生時	MP3,48kHz, 320kbps	約19.5時間	ヘッドホン使用時
再生時	MP3,48kHz, 320kbps	約18.5時間	内蔵素スピーカー使用時

録音時：JEITA録音時、再生時：JEITA音楽再生時

● ニッケル水素電池 (eneloop) 使用時

録音／再生	フォーマット	持続時間	備考
録音時	WAV,96kHz, 24ビット	約10.時間	内蔵ステレオマイク入力時
録音時	WAV,44.1kHz, 16ビット	約15.5時間	内蔵ステレオマイク入力時
録音時	MP3,44.1kHz, 128kbps	約13時間	内蔵ステレオマイク入力時
録音時	MP3,48kHz, 320kbps	約11時間	内蔵ステレオマイク入力時
再生時	WAV,96kHz, 24ビット	約15時間	ヘッドホン使用時
再生時	WAV,96kHz, 24ビット	約14時間	内蔵素スピーカー使用時
再生時	WAV,44.1kHz, 16ビット	約16.5時間	ヘッドホン使用時
再生時	WAV,44.1kHz, 16ビット	約16.5時間	内蔵素スピーカー使用時
再生時	MP3,44.1kHz, 128kbps	約16時間	ヘッドホン使用時
再生時	MP3,44.1kHz, 128kbps	約15時間	内蔵素スピーカー使用時
再生時	MP3,48kHz, 320kbps	約16時間	ヘッドホン使用時
再生時	MP3,48kHz, 320kbps	約15時間	内蔵素スピーカー使用時

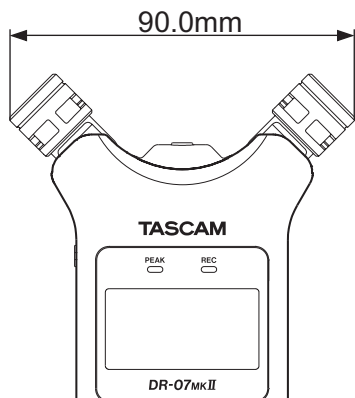
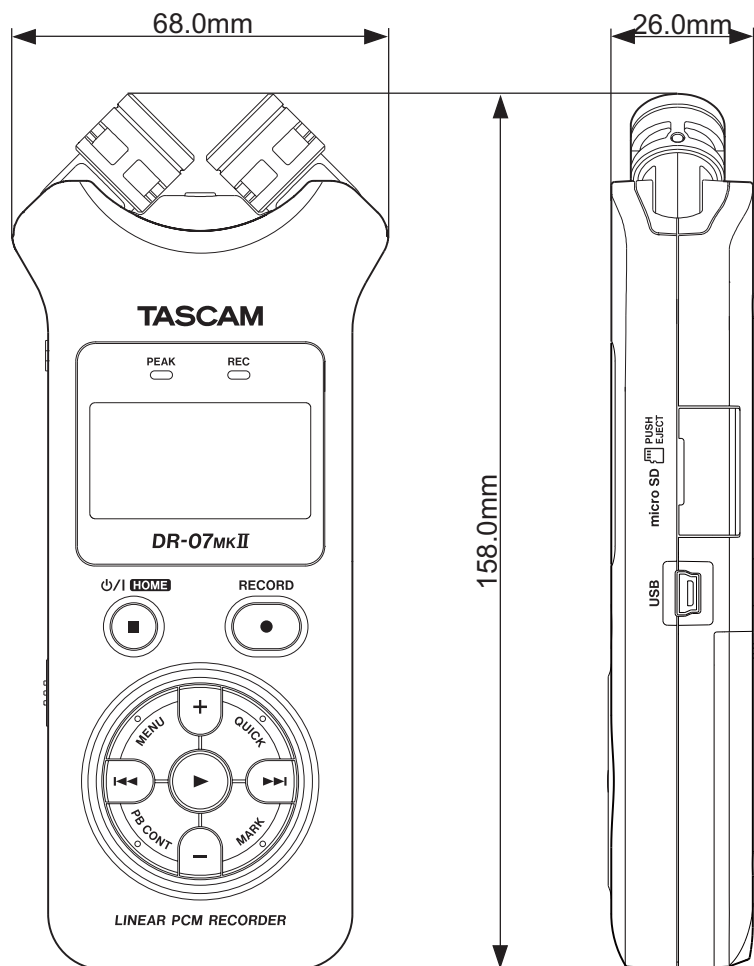
録音時：JEITA録音時、再生時：JEITA音楽再生時

外形寸法 68 x 158 x 26mm
(幅x高さx奥行き、マイク閉状態)
90 x 158 x 26mm
(幅x高さx奥行き、マイク開状態)

質量 127g (電池を含まず)

動作温度 0~40°C

Dimensional drawings(寸法図)



[Dimension of the microphone opened]
[マイク開状態の寸法]

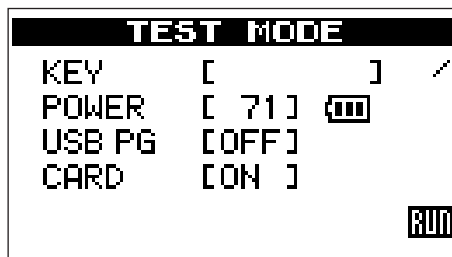
2. Test Mode

テストモード

1. How to enter test mode

While holding down the **QUICK+REW** keys, switch the power on.

The LCD shows the following message.



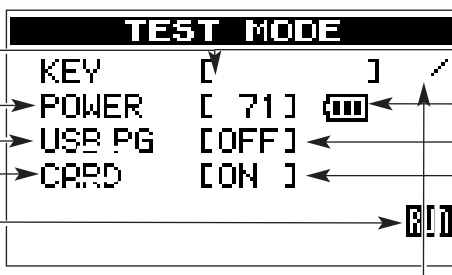
1. テストモードの起動方法

QUICK+REWキーを押しながら電源を投入する。

LCDに下記を表示する。

2. Displays explained

- Shows the name of a key pressed
- Power supply voltage (255 steps)
“” shown when powered on battery; “” shown when connected to an AC outlet.
- USB connection
- Card detection
- Operation indicator
- Event acceptance indicator. This indicator reacts when keys are operated for example



- 押されたキーを表示。
- 電源供給電圧（255段階）
バッテリー時： AC接続時：
- USB接続
- カード検出
- 動作インジケータ
- イベント受付インジケータ。キーなど操作すると反応。

2. 画面の説明

3. Checking LEDs

REC LED: turns on when the **REC** key is pressed.

PEAK LED: turns on when the **MARK** key is pressed.

They turn off when the keys are held pressed for a certain time.

3. LED

REC LED: **REC**キーで点灯する。

PEAK LED: **MARK**キーで点灯する。

全てキーを長押しすると点滅する。

4. Menu

Pressing the **MENU** key reveals the following menu.

Options are selectable using the **◀◀**, **▶▶**, **+** and **-** key.

PLAY: mode selection

MENU: back to the TOP screen

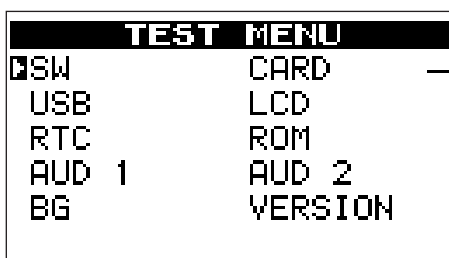
4. MENU

MENUキーを押すと下記メニューを表示する。

◀◀, **▶▶**, **+**, **-** キー操作で項目の移動をする。

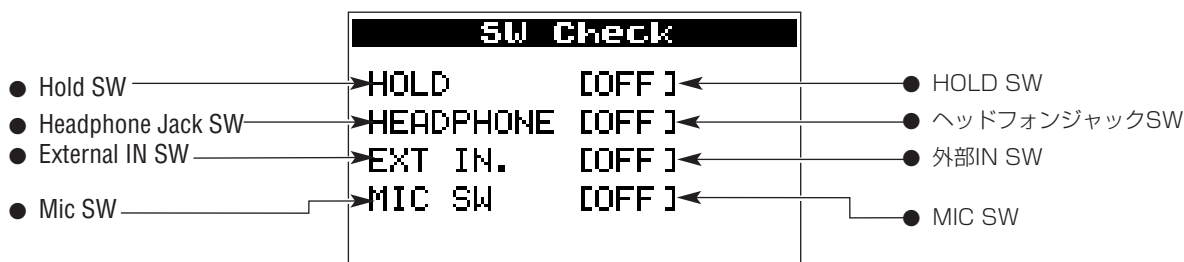
PLAY: 項目の選択。

MENU: TOP画面へ。



1) SW

Selecting "SW" and pressing the **PLAY** key gets you to the following menu:

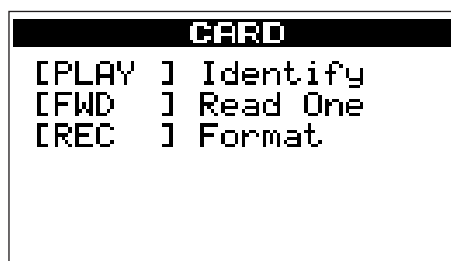


1)SW

"SW"を選択して**PLAY**キーを押すと下記メニューを表示する。

2) CARD

Selecting "CARD" and pressing the **PLAY** key gets you to the following menu:

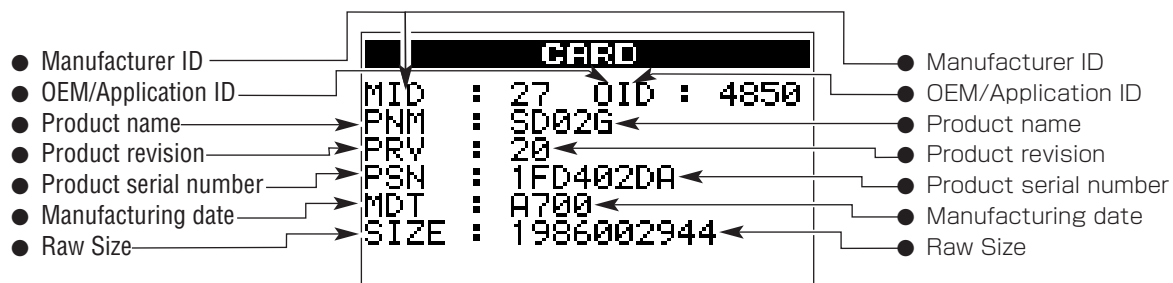


2)CARD

"CARD"を選択して**PLAY**キーを押すと下記メニューを表示する。

Identify: Read in data

Pressing the **PLAY** key indicates the following information:



Identify : カードから情報の読み込み

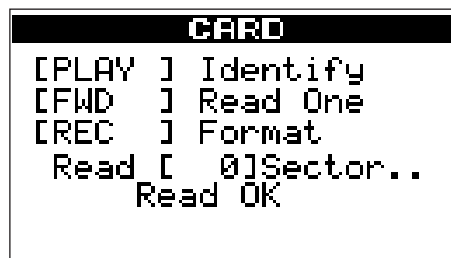
PLAYキーを押すと下記の情報を表示する。

Read One: Read in data from the card per sector

At each press of the **▶▶** key, data is read in from the card per sector.

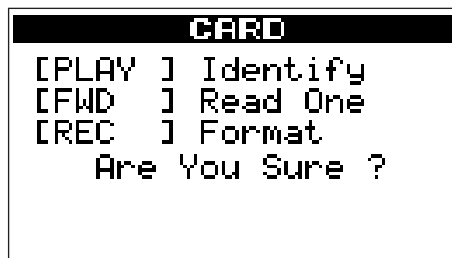
Read One : カードから1セクタ読み込み

▶▶キーを押すと、押すたびにカードから1セクター毎のデータの読み込みを行なう。



Format: Card formatting

At a press of the **REC** key, the following screen appears:



If **PLAY** key is pressed at this screen, the card starts being formatted. Upon completion of the formatting process, "**Complete**" is displayed.

Pressing **MENU** key brings you back to the top screen.

Format : カードフォーマット

RECキーを押すと下記画面を表示する。

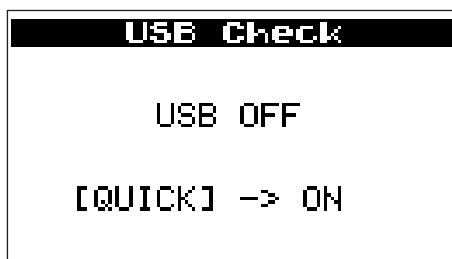
ここで**PLAY**キーを押すとFormatを実行し、実行後、"**Complete**"を表示して終了する。

MENUキーでTop画面へ戻る。

3) USB Check

Select "**USB**" and press the **QUICK** key.

Each time the **QUICK** key is pressed, the indication alternates between ON and OFF.

**3) USB Check**

"**USB**"を選択して**QUICK**キーを押す。

QUICKキーを押すたびにON/OFFを繰り返す。

4) LCD Check

Select "**LCD**" and press **PLAY** key and the following are displayed:

● Contrast adjustment
(+ : up; - : down)

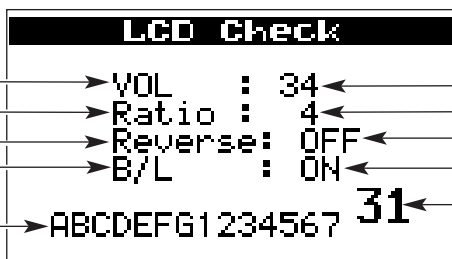
● adjustment
(▶▶ : +; ◀◀ : -)

● **REC**: Reverse

● **PLAY**: Back light ON/OFF

● Characters for after-image check

● **MARK**: All dots are displayed.



● コントラスト調整
(+ : アップ - : ダウン)

● コントラスト調整傾き
(▶▶ : + ◀◀ : -)

● **REC**: 反転

● **PLAY**: バックライトのON/OFF

● 残像確認用キャラクタ

● **MARK**: 全てのドットを表示

4) LCD Check

"**LCD**"を選択して**PLAY**キーを押すと下記画面を表示する。

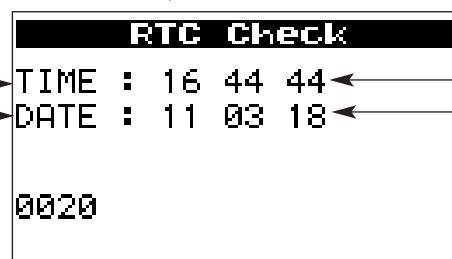
5) RTC Check

Select "**RTC**" and press **PLAY** key and the following are displayed:

Real-time clock indication.(Date and time indication only)

● Time

● Date (yy/mm/dd)
The year of 2000 is indicated as "00".



● 時刻.

● 日付 (年月日)
年は2000年を00と表示

5) RTC Check

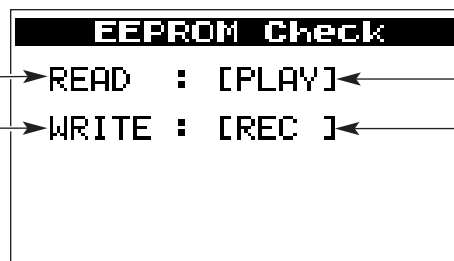
"**RTC**"を選択して**PLAY**キーを押すと下記画面を表示する。

リアルタイムクロック表示(日時の表示のみ)。

6) ROM Check

Select **"ROM"** and press **PLAY** key and the following are displayed:

- Read in from the ROM
"Reading..." is displayed at a press of the **PLAY** key.
- Writing all zeros to the ROM
The writing process starts at a press of the **PLAY** key in response to **"Are you sure?"**
To cancel the process, press the **MENU** key.



- ROMの読み込み実行。
PLAYキーで"Reading..."を表示。
- ROMのオールゼロ書き込み。
"Are you sure?"後に**PLAY**キーで書き込み。
MENUキーでキャンセル。

If errors occur during either the read or the write, the following are displayed:

- "Timeout Err" No response from the EEPROM
- "Error" Errors at data send/receive time
- "Verify Err" Errors in verification during the write process

6) ROM Check

"ROM"を選択して**PLAY**キーを押すと下記画面を表示する。

READ/WRITE共にエラーの場合には下記を表示する。

- "Timeout Err" EEPROMの応答なし
- "Error" データ送信/受信時のエラー
- "Verify Err" Write時のペリファイエラー

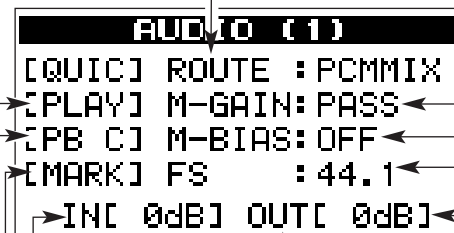
7) AUDIO Check

There are two audio check items: AUD 1 and AUD 2.
You can check audio by selecting either of **"AUD 1"** or **"AUD 2"** item.

AUD 1

Select **"AUD 1"** and press the **PLAY** key.

- **ROUTE:** Input routing setting.
Use the **QUICK** key to select PCMMIX, THRU or ADCMIX.
- **M-GAIN:** CODEC MIC pre-amp gain setting. Use the **PLAY** key to select PASS, 16dB, 17dB,, 31dB or 32dB.
- **M-BIAS:** CODEC MIC BIAS setting.
Use the **PB CONT** key to select OFF, 0.5, 0.6, 0.7, 0.8, 0.83 or 0.91.
- **FS:** Sampling frequency setting.
Use the **MARK** key to select 44.1kHz, 48kHz or 96kHz.
- **IN:** CODEC INPUT PGA setting.
Use the **◀▶** keys to select -6.0dB, -5.5dB, -5.0dB,, 11.5dB or 12.0dB.
- **OUT:** CODEC master volume setting. Use the **+ / -** keys to select -102dB, -54dB, -52dB,, -2dB, 0dB, 1dB, 2dB,, 11dB or 12dB.



- **ROUTE :** 入力経路設定、**QUICK**キーで選択、PCMMIX /THRU/ADCMIX
- **M-GAIN:** CODEC MIC Pre-Amp ゲイン設定、**PLAY**キーで選択、PASS/16dB/17dB/.../31dB/32dB
- **M-BIAS:** CODEC MIC BIAS設定 **PB CONT**キーで選択、OFF/0.5/0.6/0.7 /0.8/0.83/0.91
- **FS:** サンプリング周波数選択 **MARK**キーで選択。44.1kHz/48kHz/96kHz
- **IN:** CODEC INPUT PGA設定、**◀▶**キーで選択、-6.0dB/-5.5dB/-5.0dB/.../11.5dB/12.0dB
- **OUT:** CODEC Master Volume設定、**+ / -**キーで選択、-102dB/-54dB/-52dB/.../-2dB/0dB/1dB/2dB/.../11dB/12dB

7) AUDIO CHECK

AUD 1とAUD 2の2つあります。

"AUD 1"または**"AUD 2"**の項目を選択することにより、AUDIOのチェックができます。

AUD 1

"AUD 1"を選択して**PLAY**キーを押す。

AUD 2

Select "**AUD 2**" and press the **PLAY** key.

- **U-MUTE:** CODEC ADC output mute setting. Use the **QUICK** key to select OFF or ON.
- **CH-FREQ:** CODEC Charge Pump Freq setting. Use the **PLAY** key to select N=0, 1, 2, ..., 14 or 15.
- **HPGAIN:** CODEC HP/LINE OUT gain setting. Use the **PB CONT** key to select 0.3959, 0.4571/0.5111, 0.6047, 0.7099, 0.9399, 1.000 or 1.1430.
- **SPK:** Speaker mute setting. Use the **MARK** key to select MUTE or ON.
- **IN:** CODEC INPUT PGA setting. Use the **◀▶** keys to select -6.0dB, -5.5dB, -5.0dB, ..., 11.5dB or 12.0dB.
- **OUT:** CODEC master volume setting. Use the **+/-** keys to select -102dB, -54dB, -52dB, ..., -2dB, 0dB, 1dB, 2dB, ..., 11dB or 12dB.

```

AUD 2 (2)
[QUICK] I-MUTE: OFF
[PLAY] CH-FRQ: N= 5
[PB C] HPGAIN: 1.1430
[MARK] SPK : MUTE
[IN] 0dB [OUT] 0dB
  
```

AUD 2

"**AUD 2**"を選択して**PLAY**キーを押す。

- **I-MUTE:** CODEC ADC出力のミュート設定、**QUICK**キーで選択、OFF/ON
- **CH-FRQ:** CODEC Charge Pump Freq.設定、**PLAY**キーで選択、N=0/1/2/.../14/15
- **HPGAIN:** CODEC HP/LINE OUT ゲイン設定、**PB CONT**キーで選択、0.3959/0.4571/0.5111/0.6047/0.7099/0.9399/1.000/1.1430
- **SPK:** スピーカーミュート設定、**MARK**キーで選択、MUTE/ON
- **IN:** CODEC INPUT PGA設定、**◀▶**キーで選択、-6.0dB/-5.5dB/-5.0dB/.../11.5dB/12.0dB
- **OUT:** CODEC Master Volume設定、**+/-**キーで選択、-102dB/-54dB/-52dB/.../-2dB/0dB/1dB/2dB/.../11dB/12dB

8) BG

Select "**BG**" and press **PLAY** key:

Background samples

FWD(▶▶): Previous; **REW**(◀◀): Next

8) BG

"**BG**"を選択して**PLAY**キーを押す。

背景サンプル

FWD(▶▶): 後 **REW**(◀◀): 前

9) VERSION Check

Select "**VERSION**" and press **PLAY** key and the following are displayed:

9) VERSION Check

"**VERSION**"を選択して**PLAY**キーを押すと下記画面を表示する。

● Model Name	→	Model:DR-07MK2	←	● モデル名
● Version of the system firmware. The last 4 digits indicate a build number	→	Ver :0101.0011	←	● システムファームのバージョン。後半の4桁はビルド番号
● on which the system firmware was built.	→	Date :Mar 18 2011	←	● ファームビルド日付
● which the system firmware was built.	→	Time :16:00:10	←	● ファームビルド時刻

3. Updating of Firmware

ファームウェアのアップデート

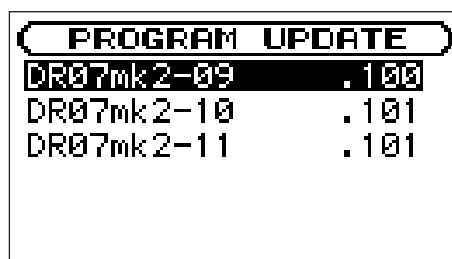
1. Preparations

- 1) Make the connection between this unit and the PC using a USB cable.
- 2) Place the update file in the UTILITY folder in the unit.
- 3) Perform the USB device “**remove**” action on the PC, and then switch off the power to the unit.

2. START-UP

While holding down the **MARK** and **REW** keys, switch the power on.

The LCD looks like this:



Update files are shown with extensions.

The USB connection can be made at this point.

When USB connected, the normal USB screen appears.
When USB connection is made, the normal USB screen appears. When the USB cable is disconnected, the unit turns off.

1. 準備

- 1) 本体とPCをUSBケーブルで接続する。
- 2) アップデートファイルを本体の「UTILITY」フォルダに置く。
- 3) PCでUSBデバイスの“**取り外し**”を行い、本体の電源を落とす。

2. 起動

MARK+REWキーを押しながら電源を投入する。

LCDに下記を表示する。

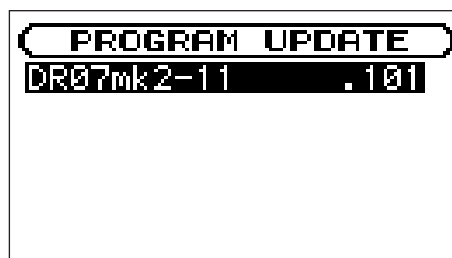
アップデートファイルを拡張子付きで表示する。

この時点でUSB接続することが可能です。

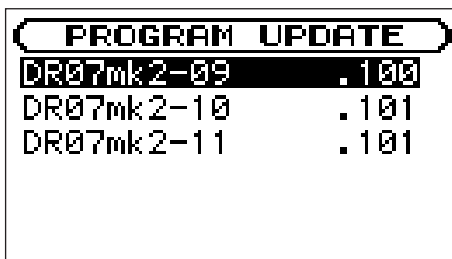
接続すると通常と同じUSB画面となり、USBケーブルを抜くと電源が切れます。

3. Displays explained

- 1) When only a single file is available:



- 2) When multiple files are available:



When there are 6 or more files, use the + key and - key to move the cursor over them.

3. 画面の説明

- 1) ファイルが一つの場合

- 2) ファイルが複数の場合

5つ以上の場合は+/-キーでカーソルが移動する。

3) When no update file is available:

Nothing can be done.

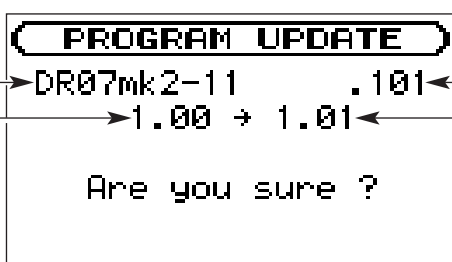
3) ファイルが無い場合

何も操作できません。

**4. File confirmation**Select a target file and press the **PLAY** key .**4. ファイルの確認**対象のファイルを選択し、**PLAY**キーを押す。

- Name of the file selected

- Current version at left and New version at right

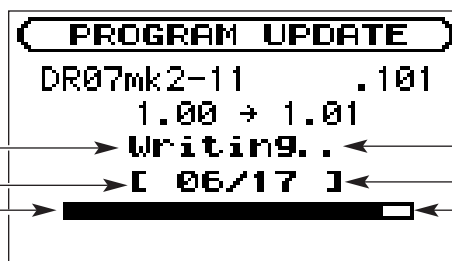


- 選択したファイル名

- 左: 現バージョン
右: 新バージョン

5. Getting update startedThe update process starts when pressing the **ENTER** key .**5. アップデート実行****ENTER**キーを押すとアップデートを実行する。

- Task progress.
- FLASH sector number
- Writing progress by sector



- 動作状況

- FLASHのセクタ番号

- セクタ単位の書き込み進捗

Pressing the **MENU** key brings you back to the file selection screen, as at step 2, without performing the update.アップデートを実行せず、2.のファイル選択画面へ戻るには**MENU**キーを押す。**6. Completion****6. 完了**Upon completion of the update process, "**Complete**" is displayed and the unit automatically switched off.アップデートが完了すると"**Complete**"と表示して自動的に電源が切れる。

7. Error messages

1) If an error occurs when selecting a file, the following messages appear:

Messages(メッセージ)	Meaning (内容)
Product	The product ID of the file does not match (the file may be for other products).
	ファイルのプロダクトIDが一致しない (別製品のファイルの可能性はある)。
Old Version	The file version is older than the current one.
	現バージョンよりもファイルのバージョンが古い。
Checksum	The checksum does not match.
	ファイルのチェックサムが一致しない。
Update File	Error in file reading.
	ファイル読み込みエラー。

7. エラー

1) ファイル選択時にエラーが発生した場合のメッセージ

2) If an error occurs in the data rewriting process, the following messages appear

2) 書き換え時にエラーが発生した場合のメッセージ

Messages(メッセージ)	Meaning (内容)
Flash Erase	Error in erasing.
	消去エラー
Flash Blank	Blank error as a result of data erasure.
	消去後のブランクエラー
Flash Write	Error in writing.
	書き込みエラー
Flash Verify	Error in verification after data has been written.
	書き込み後のベリファイエラー

4. Messages Explained

メッセージ一覧

The following is a list of the popup messages that might appear on the DR-07MK2 under certain conditions. Refer to this list if one of these popup messages appears and you want to check the meaning or determine a proper response.

以下にポップアップメッセージの一覧表を示します。

DR-07MK2では、状況に応じてポップアップメッセージが表示されますが、それぞれのメッセージの内容を知りたいとき、および対処方法を知りたいときにこの表をご覧ください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
File Name ERR	The DIVIDE function would cause the file name to exceed 200 characters. The DIVIDE function adds “_a” or “_b” to the end of the file name. Before choosing the DIVIDE function, connect the unit to a computer and edit the file name to less than 198 characters.
	DIVIDEによりファイル名の文字数が200文字を超えました。DIVIDEを行うとファイル名の末尾に“_a”または“_b”が追加されます。DIVIDEを行う前にパソコンと接続し、198文字以下のファイル名に変更してください。
Dup File Name	The DIVIDE function would cause the file name to be the same as that of an existing file. The DIVIDE function adds “_a” or “_b” to the end of the file name. Before choosing the DIVIDE function, connect the unit to a computer and edit the file name.
	DIVIDEにより作成されるファイルと同じファイル名のファイルが同じフォルダ内に既に存在します。DIVIDEを行うとファイル名の末尾に“_a”または“_b”が追加されます。DIVIDEを行う前にパソコンと接続し、ファイル名を変更してください。
File Not Found	The file added to the playlist cannot be found or a file could be damaged. Please check the file in question.
	プレイリストに登録されているファイルが見つからないか、ファイルが壊れている可能性があります。対象のファイルを確認してください。
Non-Supported	The audio file is not a supported format.
	ファイル形式がサポート対象外です。
Battery Empty	The battery is almost out of power. Replace the AA batteries.
	電池の残量がありません。電池を交換してください。
I/O Too Short	The IN and OUT points are too close together. Reset the IN and OUT points with at least 1 second between them.
	IN点とOUT点の間隔が短すぎます。1秒以上空けて設定してください。
File Not Found PLAYLIST	The file in the Playlist cannot be found. Please confirm that the file is still in the Music Folder.
	プレイリストに登録されているファイルが見つかりません。MUSICフォルダ内に対象のファイルがあるか確認してください。
No PLAYLIST	No files have been added to the Playlist. Add a file to the Playlist or change the play mode to something besides PLAYLIST.
	プレイリストにファイルが登録されていません。プレイリストにファイルを登録するか、プレイモードを「PLAYLIST」以外に設定してください。
PLAYLIST Full	The playlist is full. You cannot add more than 99 tracks to the Playlist.
	プレイリストが一杯です。プレイリストには、最大99ファイルまで登録可能です。
MBR Error Init CARD	The card is not formatted properly or the formatting is broken. Change the card or press the PLAY key when this message appears to format the card in FAT format . CAUTION Execution of FAT formatting erases all data currently on the card.
	カードが正常にフォーマットされていないか、カードが壊れている可能性があります。カードを交換するか、このメッセージが表示されている状態で PLAY キーを押すと、FATフォーマットが実行されます。
	注意 FATフォーマットが実行されるとカード内のデータは、すべて消去されます。

Messages(メッセージ)	Meaning and response(内容と対処方法)
Format Error Format CARD	The FAT formatting of the card is abnormal or broken. This message also appears if you FAT formatted the card using a computer connected by USB and if a new card is inserted in the unit. Always use the DR-07MK2 to conduct FAT formatting of cards to be used with it. Change the card or press the PLAY key when this message appears to format the card in FAT format. CAUTION Execution of FAT formatting erases all data currently on the card.
	カードが正常にフォーマットされていないか、カードが壊れている可能性があります。このメッセージは、USB接続したパソコンでFATフォーマットした場合や未フォーマットのカードを挿入した場合にも表示されます。フォーマットは、必ずDR-07MK2本体で行ってください。カードを交換するか、このメッセージが表示されている状態で PLAY キーを押すと、FATフォーマットが実行されます。 注意 FATフォーマットが実行されるとカード内のデータは、すべて消去されます。
File Not Found Make Sys File	The system file is missing. This unit requires a system file for operation. When this message appears, press PLAY key to automatically create a system file.
	本機を使用するために必要なシステムファイルがありません。このメッセージが表示されている状態で PLAY キーを押すと、システムファイルが作られます。
Invalid SysFile Make Sys File	The system file required to operate this unit is invalid. When this message appears, press PLAY key to automatically create a system file.
	本機を使用するために必要なシステムファイルが正常ではありません。このメッセージが表示されている状態で PLAY キーを押すと、新しいシステムファイルが作られます。
Invalid Card Change Card	Something might be wrong with the card. Change the card.
	カードが正常でない可能性があります。カードを交換してください。
Write Timeout	Writing to the card timed out. Backup files on the card to your computer, and format the card.
	カードへの書き込みが間に合いませんでした。 ファイルをパソコンへバックアップの上、フォーマットを実行してください。
Card Full	The card has no remaining capacity. Erase unnecessary files or move them to your computer to make open space.
	カードの残容量がありません。不要なファイルを削除するかパソコンへ移動してください。
Layer too Deep	Folders can be created down to two layers. You cannot create a new folder inside the current folder.
	フォルダは、2階層までです。このフォルダ内に新たなフォルダを作成することはできません。
Can't Divide	The position selected for divide is not suitable (too close to the beginning or end of a track).
	DIVIDE実行時に分割位置が適切ではありません。(曲の先頭、曲の最後)
Max File Size	The file is larger than the designated size or the recording time exceeded 24 hours.
	ファイルのサイズが指定のサイズを超えました。あるいは録音時間が24時間を超えました。
File Full	The total number of folders and files exceeds 5000. Erase unnecessary files or move them to your computer.
	フォルダとファイルの総数が制限値(5000個)を超えました。不要なフォルダやファイルを削除するかパソコンへ移動してください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
Card Error	The card could not be handled properly. Replace the card.
	カードを正常に認識できません。カードを交換してください。
Current File MP3	MP3 files cannot be divided.
	MP3ファイルの分割はできません。
File Protected	The file is read only and cannot be erased.
	リードオンリーファイルのため、削除できません。
No Card	No card is in the unit, so recording is not possible.
	カードが無いため、録音できません。
No PB File	There is no file that can be played back. The file might be damaged.
	再生可能なファイルがありません。ファイルが壊れている可能性があります。
No MUSIC File	There is no playback file, so DIVIDE and OVERDUB cannot be executed.
	再生ファイルが無いため、DIVIDE、OVERDUBは実行できません。
Cannot overdub! See REC setting	ou cannot overdub a WAV file with a sampling frequency of 96kHz in MP3 format. Change the recording format to WAV.
	96kHzのWAVファイルをMP3でオーバーダビングすることはできません。録音フォーマットをWAVにしてください。

System Error Messages (システムエラーメッセージ)

Messages(メッセージ)	Description(説明)	Cause(原因)
Not Continued	Playback not stopped, or card unmounted error.	The card or firmware may be defective.
	再生系の停止が未完了、あるいはカードのアンマウント時のエラー	カード不良もしくはF/Wの不具合の可能性有り。
File Error	File system error or recording/playback circuitry error.	The card or firmware may be defective.
	ファイルシステム上でエラー、あるいは録再生でのエラー	カード不良もしくはF/Wの不具合の可能性有り。
Can't Save Data	Write in the EEPROM or system file failed during shutdown or switching to USB.	Check that the card is inserted. The card may be defective. If the error occurs with the EEPROM, the PCB may be defective.
	シャットダウン時やUSB切り替え時にEEPROMあるいはシステムファイルへの書き込みが出来なかった。	カードの挿入を確認。 カード不良の可能性有り。 EEPROMの場合はPCB不良の可能性有り。
Player Error	Internal error in recording / playback.	The firmware may be defective.
	記録再生の内部的エラー	F/Wの不具合の可能性有り。
Device Error	Device Error 2: RTC initialization error.	The PCB may be defective.
	Device Error 2 : RTC初期化エラー	PCB不良の可能性有り。
Writing Failed	File creation error at the start of recording or file close error at the end of recording.	Confirm whether the error occurred during start or end of recording. The card may be defective.
	記録開始時のファイル作成エラー、あるいは記録終了時のファイルクローズエラー	録音開始時か記録終了時かの確認。 カード不良の可能性有り。
Sys Rom Err	Serial ROM read error.	The PCB may be defective.
	Serial ROMの読み込みエラー	PCB不良の可能性有り。
Remote Cmd	Error in communication with the the microcomputer for a remote control.	The firmware may be defective.
	リモート用マイコンとの通信でエラー。	F/Wの不具合の可能性有り。
Remote Rx	Error in communication with the the microcomputer for a remote control.	The microcomputer for a remote control or firmware may be defective.
	リモート用マイコンとの通信でエラー	リモート用マイコンもしくはF/Wの不具合の可能性有り。
System Err 50	Other fatal error.	The firmware may be defective.
	その他の致命的エラー	F/Wの不具合の可能性有り。
System Error 1	CPU access error.	The firmware may be defective.
	CPUのアクセスエラー	F/Wの不具合の可能性有り。
System Error 2	CPU address error.	The firmware may be defective.
	CPUのアドレスエラー	F/Wの不具合の可能性有り。
System Error 3	CPU instruction error.	The firmware may be defective.
	CPUのインストラクションエラー	F/Wの不具合の可能性有り。

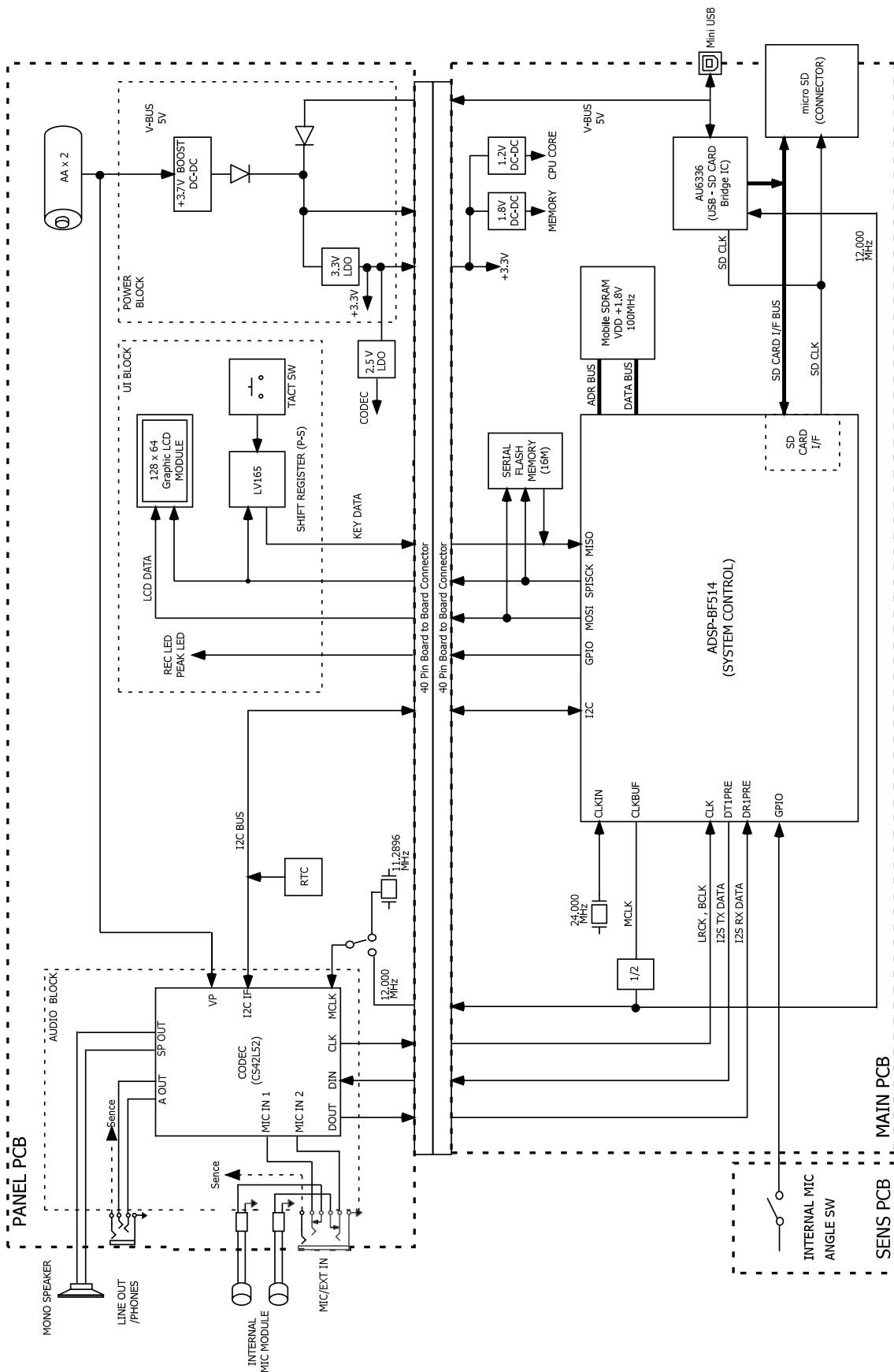
Messages(メッセージ)	Description(説明)	Cause(原因)
System Error 4	CPU zero division error.	The firmware may be defective.
	CPUのゼロ除算エラー	F/Wの不具合の可能性有り。
System Error 5	CPU Privilege Violation error.	The firmware may be defective.
	CPUのPrivilege Violationエラー	F/Wの不具合の可能性有り。
System Error 6	CPU Unimplemented line-a opcode error.	The firmware may be defective.
	CPUのUnimplemented line-a opcodeエラー	F/Wの不具合の可能性有り。
System Error 7	CPU Unimplemented line-f opcode error.	The firmware may be defective.
	CPUのUnimplemented line-f opcodeエラー	F/Wの不具合の可能性有り。
System Error 8	CPU format error.	The firmware may be defective.
	CPUのフォーマットエラー	F/Wの不具合の可能性有り。
System Error 9	CPU Uninitialized Interrupt error.	The firmware may be defective.
	CPUのUninitialized Interruptエラー	F/Wの不具合の可能性有り。

5. Block Diagram

ブロックダイアグラム

Exploded View-1

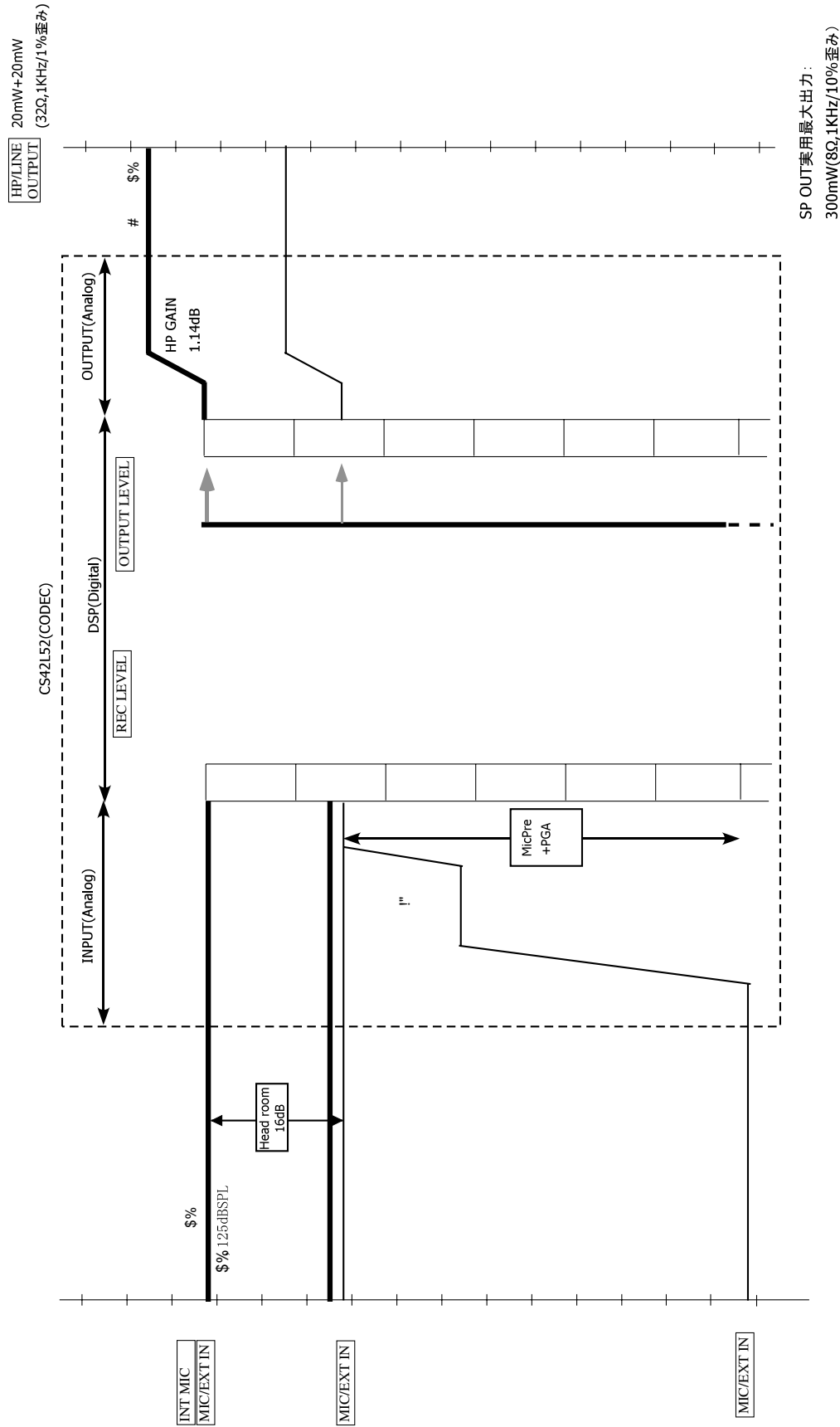
DR-07MKII Block Diagram



6. Level Diagram

レベルダイアグラム

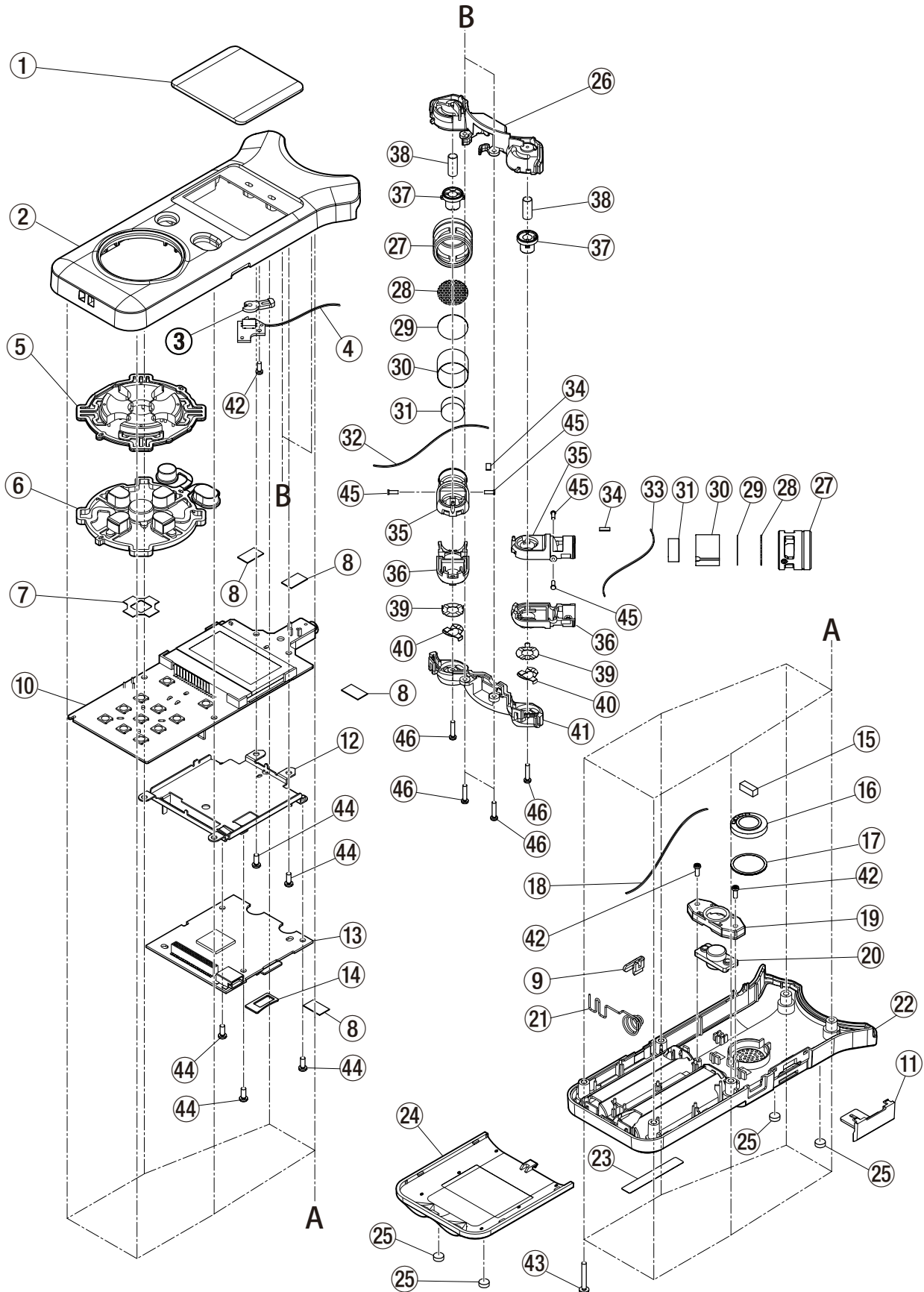
DR-05/DR-07MKII Level Diagram



7. Exploded Views and Parts List

分解図とパーツリスト

Exploded View-1



Exploded View-1

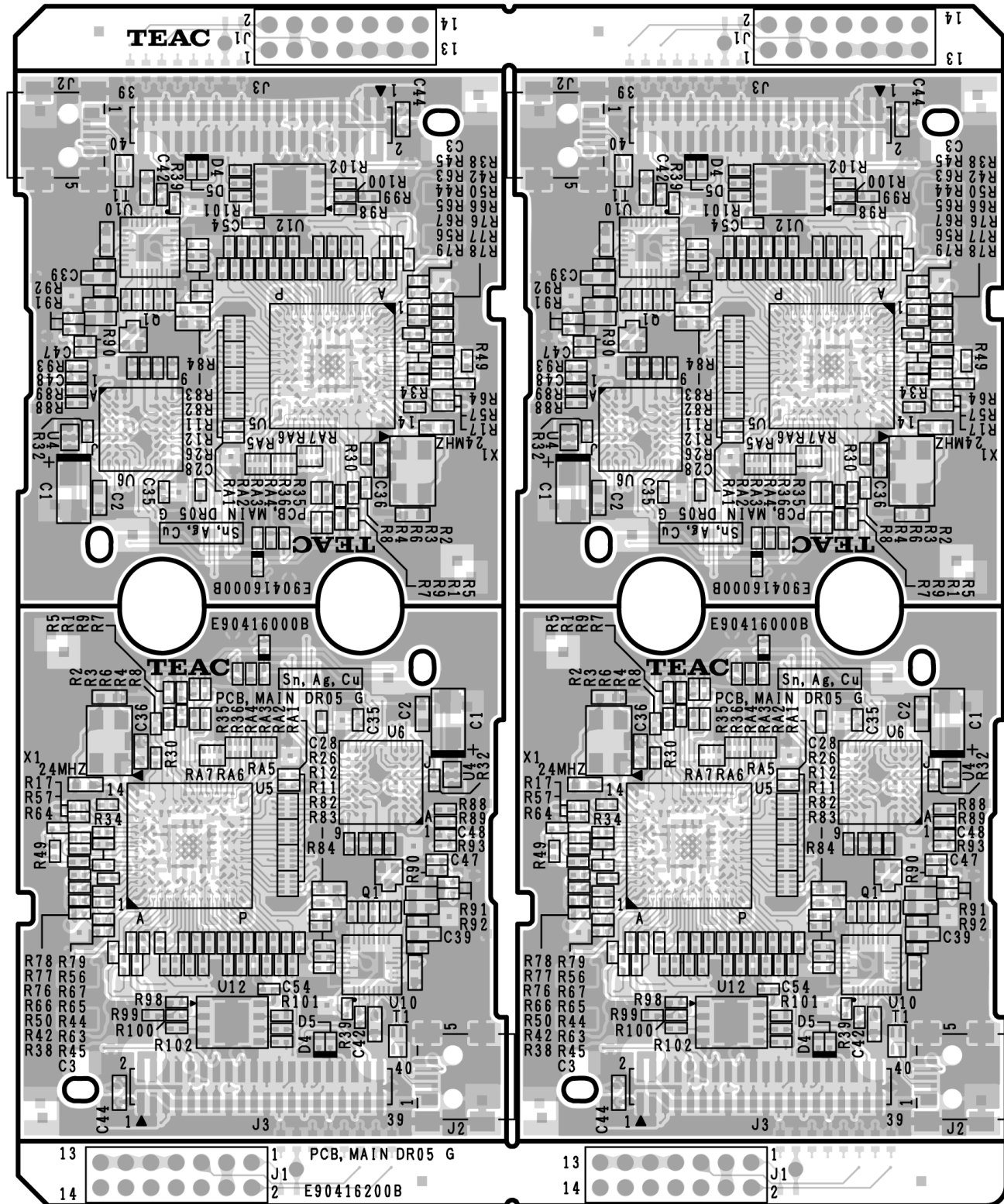
REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	M03270610A	WINDOW,07MK2 G	
1- 2	M03311300D	CASE, TOP 07MK2 G	
1- 3	M03311600B	LEVER,SENSOR 07MK2 G	
1- 4	E95425400A	PCB ASSY,SENS DR07MK2 G	Refer to page 27 (GATHER PCBA,PANEL 07MK2 G)
1- 5	M03269100C	BUTTON,MENU DR05 G	
1- 6	M03269200B	BUTTON,TRANS DR05 G	
1- 7	M03279700A	SHEET,PANEL DR05 G	
1- 8	M03142400A	SHEET,HM 6*10 G	
1- 9	M03269300A	KNOB,SLIDE DR05 G	
1-10	E95416110A	PCB ASSY,PANEL DR07MK2 G	Refer to page 26 (GATHER PCBA,MAIN 07MK2 G)
1-11	M03270300A	COVER, MICRO SD DR05 G	
1-12	M03269800B	CHASSIS,DR05 G	
1-13	E95416010A	PCB ASSY,MAIN DR07MK2 G	Refer to page 26 (GATHER PCBA,MAIN 07MK2 G)
1-14	M03322400A	SHEET,MSD DR05 G	
1-15	M03270200A	SHEET,CUSHION 8*3*T3 G	
1-16	E0166440	SPEAKER,HF-16008G-22 G	
1-17	M03270100A	SHEET,SPEAKER DR05 G	
1-18	E01749400A	WIRE,SPK P_ P8 DR05 G	
	E01749500A	WIRE,SPK N_ P7 DR05 G	
1-19	M03270000A	HOLDER,TRIPOD DR05 G	
1-20	M02954600A	ESCUTCHEON, TRIPOD DR100 G	
1-21	M03270400A	SPRING,BAT DR05 G	
1-22	M03311400D	CASE,BTM 07MK2 G	
1-23	M03313800A	NAMEPLATE,07MK2 G	
1-24	M03270700B	COVER,BAT DR05 G	
1-25	M03270800B	FOOT,PORON T1.5 G	
1-26	M03311700C	COVER,ARM UP 07MK2 G	
1-27	M03311900A	CASE,MIC 07MK2 G	
1-28	M03312000A	PLATE, TOP 07MK2 G	
1-29	M03312100A	SHEET, TOP 07MK2 G	
1-30	M03312200A	SHEET,MESH 07MK2 G	
1-31	E0176850	MICROPHONE,EM182-M1 G	
1-32	E01767600A	WIRE,MIC D_P1P6 DR07MK2 G	
	E01767700A	WIRE,MICL S_P2 DR07MK2 G	
	E01767800A	WIRE,MIC G_P3P5 DR07MK2 G	
1-33	E01767600A	WIRE,MIC D_P1P6 DR07MK2 G	
	E01767900A	WIRE,MICR S_P4 DR07MK2 G	
	E01767800A	WIRE,MIC G_P3P5 DR07MK2 G	
1-34	M03309700A	SHEET,HM 2*4.5 G	
1-35	M03312300B	HOLDER,MIC UP 07MK2 G	
1-36	M03312400B	HOLDER,MIC LOW 07MK2 G	
1-37	M03312500B	COLLAR,MIC 07MK2 G	
1-38	M03312600A	COLLAR,BUSH 3.4*4*L9.5 G	
1-39	M03108700A	PLATE,HINGE VR20 G	
1-40	M03326900A	LEAF SPR,MIC 07MK2 G	
1-41	M03311800C	COVER,ARM LOW 07MK2 G	
1-42	B00312500A	SCREW,MPPR 1.7*4.5 FZB G	
1-43	B00325800A	SCREW,BPB M2*5*9 FZB G	
1-44	B00303605A	SCREW,MPBR 2*5 FNI G	
1-45	B00326100A	SCREW,MPBR 1.4*4FCM G	
1-46	B00326200A	SCREW,MPPR 1.7*8FCM G	

8. PC Boards and Parts List

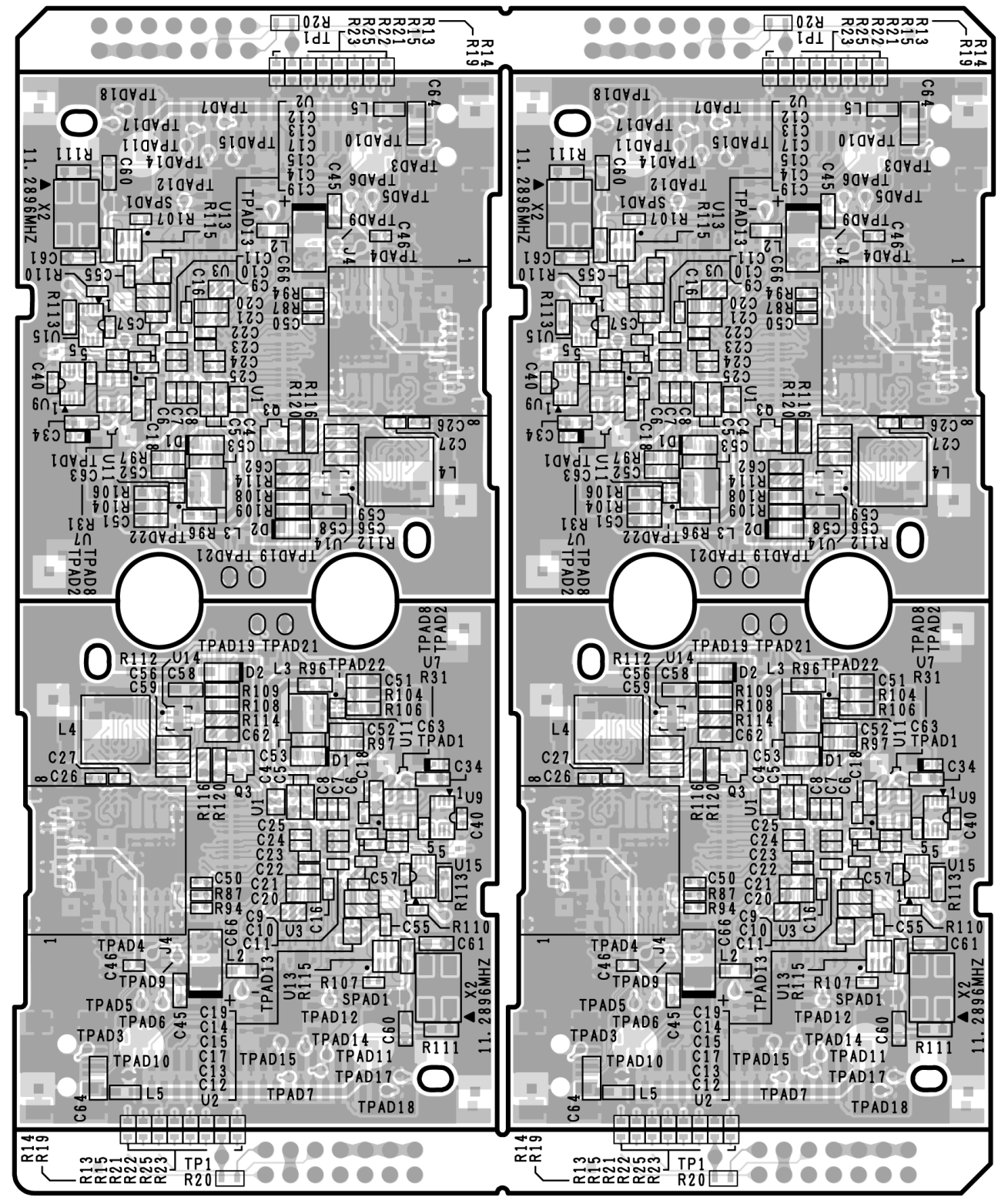
基板図とパーツリスト

GATHER PCB,MAIN DR05 G

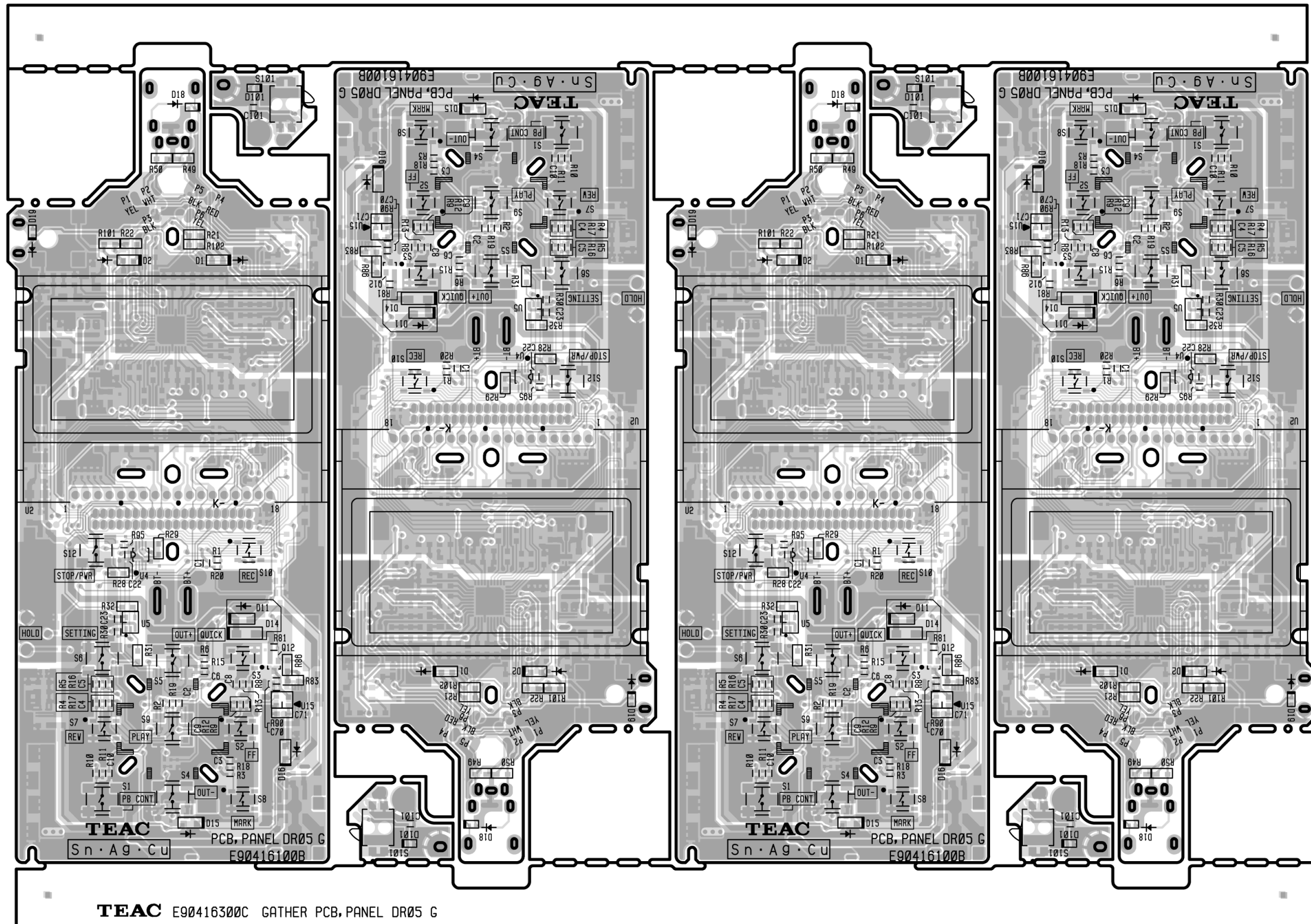
(Side A)



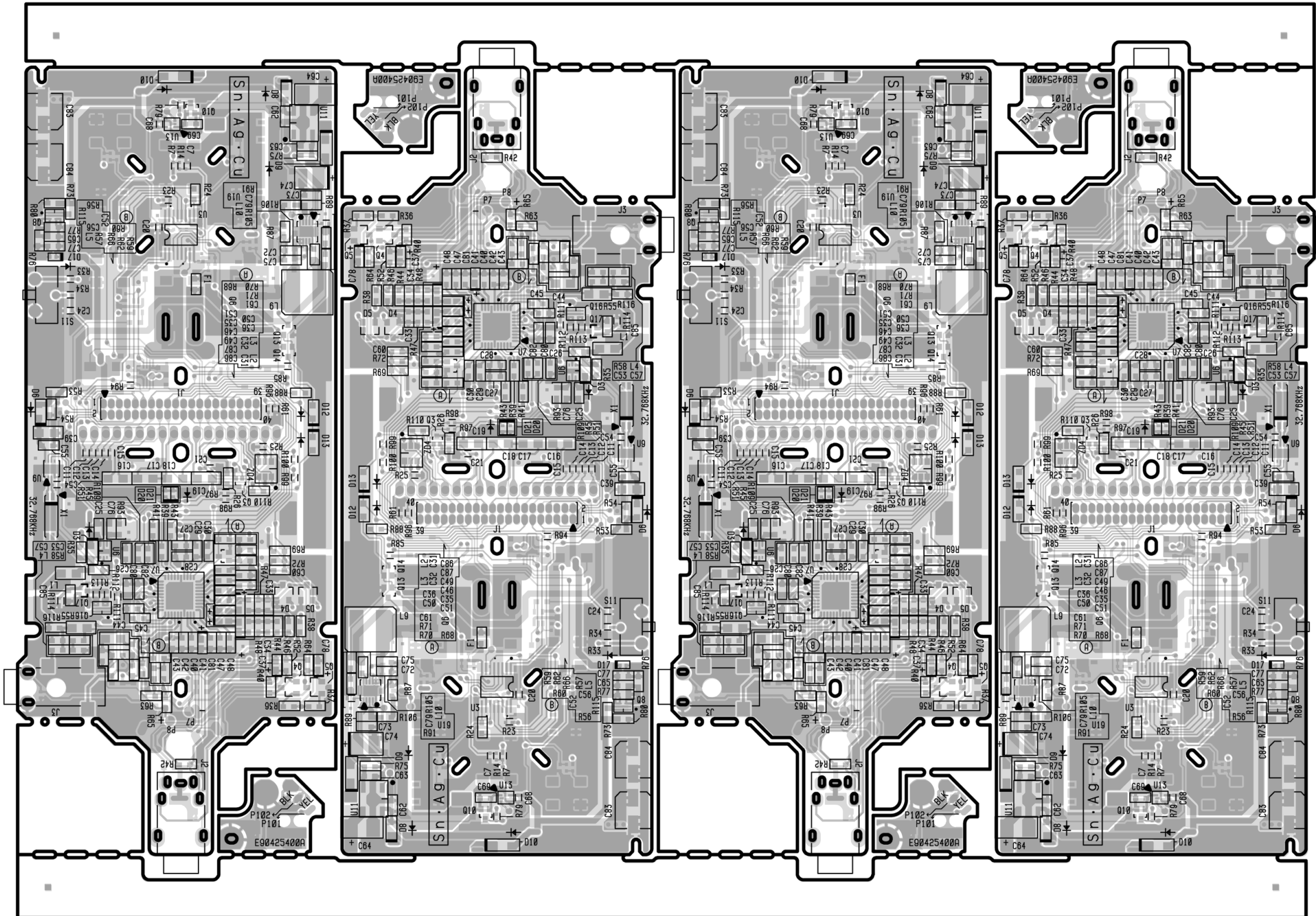
(Side B)



GATHER PCB,PANEL DR05 G (Side A) Rev:C



GATHER PCB,PANEL DR05 G (Side B) Rev:C



GATHER PCBA,MAIN 07MK2 G

REF.NO.	PARTS NO.	DESCRIPTION
	E95416210A (E90416000B)	GATHER PCBA,MAIN 07MK2 G PCB,MAIN DR05 G
	(E95416010A)	PCB ASSY,MAIN DR07MK2 G
D1	S0022094	DIODE,1SS355
D6	S0086044	ZENER DIO,CDZCT2R6.8B G
J2	E0143954	CONNECTOR,USB MINI-5B G
J3	E0174113	CONNECTOR,2200SB40GSM45 G
J4	E0170384	CONN,SCHA4B0100 G
L1	E0126164	BEAD COIL,BLM18PG471SN1D G
L2	E0126164	BEAD COIL,BLM18PG471SN1D G
L3	E0165254	COIL,LQH3NPN2R2MMO G
L4	E0069824	COIL,CDRH5D28-100NC G
L5	E0126164	BEAD COIL,BLM18PG471SN1D G
Q1	S0065074	TRANSISTOR,DTC124EUA TP G
Q3	S0065074	TRANSISTOR,DTC124EUA TP G
RA1	R0180534	RES ARRAY,1/32W 4* 56 J G
RA2	R0180534	RES ARRAY,1/32W 4* 56 J G
RA3	R0180534	RES ARRAY,1/32W 4* 56 J G
RA4	R0180534	RES ARRAY,1/32W 4* 56 J G
RA5	R0180554	RES ARRAY,1/32W 4*68 J G
RA6	R0180554	RES ARRAY,1/32W 4*68 J G
RA7	R0180554	RES ARRAY,1/32W 4*68 J G
T1	E0166304	FILTER,NT2012 985BH1007 G
U1	C0086034	CC3,NFM18PS105R0J3D G
U2	C0086034	CC3,NFM18PS105R0J3D G
U3	C0086034	CC3,NFM18PS105R0J3D G
U4	C0086034	CC3,NFM18PS105R0J3D G
U5	S0088574	IC,ADSP-BF-514KBCZ-4 G
U6	S0088994	IC,FMS4A16LCH-60EE G
U7	S0065024	IC,BD46285G G
U9	S0089084	IC,SN74LVC1G74DCUR G
U10	S0079744	IC,AU6336-MOF G
U11	S0088594	IC,TPS62231DRY G
U12	S0090083	IC,MX25L1606EZNI12G G
U12	S00901510A	IC,ROM ASSY MAIN 07MK2 G
U12	D01138110A	SOFTWARE SPEC,07MK2 G
U13	S0065014	IC,SN74LVC2GU04DCKR G
U14	S0090094	IC,XC9237D08CER-G HF
U15	S0085594	IC,SN74LVC2G157DCUR G
X1	E0175134	RESONATOR,24.0MHZ 6035 G
X2	E0141174	RESONATOR,11.2896MHZ G

GATHER PCBA,PANEL 07MK2 G

REF.NO.	PARTS NO.	DESCRIPTION
D	E95416310A (E90416100B) (E90425400A)	GATHER PCBA,PANEL 07MK2 G PCB,PANEL DR05 G PCB,SENS DR07MK2 G
	(E95416110A)	PCB ASSY,PANEL DR07MK2 G
	M01502000A	LABEL, TYPE 12*6(BLANK) G
BT+	M03271600A	SPRING,PLUS DR05 G
BT-	M03271500A	SPRING,MINUS DR05 G
D1	S0083594	LED,SML-E12U8W G
D10	S0071644	DIODE,RB161M-20 G
D11	S0075354	DIODE,RB551V-30 TE17 G
D12	S0067314	DIODE,RB751V-40/TE17 G
D13	S0022094	DIODE,1SS355
D14	S0071644	DIODE,RB161M-20 G
D15	S0022094	DIODE,1SS355
D16	S0075354	DIODE,RB551V-30 TE17 G
D17	S0086044	ZENER DIO,CDZCT2R6.8B G
D18	S0086044	ZENER DIO,CDZCT2R6.8B G
D19	S0086044	ZENER DIO,CDZCT2R6.8B G
D2	S0083594	LED,SML-E12U8W G
D4	S0081404	DIODE,RB706D-40 G
D5	S0081404	DIODE,RB706D-40 G
D6	S0067314	DIODE,RB751V-40/TE17 G
D8	S0022094	DIODE,1SS355
D9	S0071644	DIODE,RB161M-20 G
F1	E0165754	@FUSE,ERBSE2R00U HF
J1	E0174120	CONNECTOR,2199SB40G6122 G
J2	E0143793	JACK,LGY3009-0200F G
J3	E0166204	JACK,LGY2109-1001F G
L1	E0148584	COIL,10UH M LQM21F-70 G
L10	E0126164	BEAD COIL,BLM18PG471SN1D G
L2	E0158384	BEAD COIL,MMZ1608B601C G
L3	E0158384	BEAD COIL,MMZ1608B601C G
L4	E0158384	BEAD COIL,MMZ1608B601C G
L5	E0158384	BEAD COIL,MMZ1608B601C G
L9	E0124004	COIL,CDRH5D28-220 22UH G
Q10	S0065074	TRANSISTOR,DTC124EUA TP G
Q12	S0041574	TRANSISTOR,DTA124EUA G
Q13	S0065074	TRANSISTOR,DTC124EUA TP G
Q14	S0065074	TRANSISTOR,DTC124EUA TP G
Q16	S0090284	FET,RW1A025ZPT2R G
Q17	S0085924	FET,RUM002N02 T2L G
Q3	S0082684	TRANSISTOR,DTC143ZETL G
Q4	S0066984	TRANSISTOR,2SA1037AK TP G
Q5	S0066984	TRANSISTOR,2SA1037AK TP G
Q6	S0042944	TRANSISTOR,DTC143TUA T106
Q8	S0085694	FET,RW1A020ZP T2R G
S1	E00683600B	SW,TSW-6A-2-16-T50
S10	E0176074	SW,SKRWAHE030 G
S11	E0144730	SW,SSSS213100 G
S12	E00683600B	SW,TSW-6A-2-16-T50
S2	E0176074	SW,SKRWAHE030 G
S3	E0176074	SW,SKRWAHE030 G
S4	E00683600B	SW,TSW-6A-2-16-T50

GATHER PCBA,PANEL 07MK2 G

REF.NO.	PARTS NO.	DESCRIPTION
S5	E00683600B	SW,TSW-6A-2-16-T50
S6	E00683600B	SW,TSW-6A-2-16-T50
S7	E0176074	SW,SKRWAHE030 G
S8	E0176074	SW,SKRWAHE030 G
S9	E00683600B	SW,TSW-6A-2-16-T50
U11	S0075293	IC,R1173H331D-T1-F G
U13	S0080024	IC,BD4944FVE-TR G
U15	S0079934	IC,BU4918F-TR G
U19	S0080104	IC,TPS61020DRCR G
U2	E01743300A	LCD,SMMC12864-DQ-00-SPC G
U3	S0065384	IC,SN74LV165APWR G
U4	S0088614	IC,SN74LVC1G29DCUR G
U5	S0053294	IC,SN74LVC1G125DCKR
U6	S0085654	IC,S-1132B25-I6T2G G
U7	S0089123	IC,CS42L52-CNZR G
U9	S0075164	IC,S-35390A-I8T1G G
X1	E0143374	XTAL,SSP-T7-F 32.768K 7P G
ZD4	S0074914	ZENER DIO,RSA6.1U5 T108 G
	(E95425400A) PCB ASSY,SENS DR07MK2 G	
	M03325400A	SHEET,HM 6*6 G
P101	E01768200A	WIRE,SENS_P101_Y 07MK2 G
P102	E01768300A	WIRE,SENS_P102_B 07MK2 G
S101	E0166274	SW,MPU12580MLB1 G

REF.NO.	PARTS NO.	DESCRIPTION
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9. Included Accessories

付属品

Included Accessories

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	D01145001A	OWNERS MNL,DR07MK2 J G [J]	
	D01145020A	OWNERS MNL,DR07MK2 E G [Except J]	
	D01145080A	OWNERS MNL,DR07MK2 G G [E]	
	D01145081A	OWNERS MNL,DR07MK2 F G [E]	
	D01145082A	OWNERS MNL,DR07MK2 I G [E]	
	D01145083A	OWNERS MNL,DR07MK2 S G [E]	
	T0018100	MICROSD,SP002GST000UMPA G	
	E0174680	USB CABLE,CA3096080A37 G	
	E0174070	BAT,LR6(GD)CH G	

NOTES

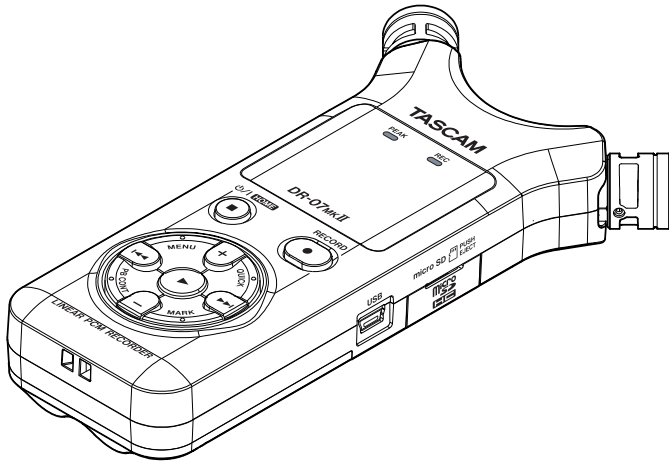
- PC boards shown are viewed from parts side.
- Parts marked with * require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in this manual.
- △ Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.

- Parts of [] mark can be used only with the version designated.
 [J] : JAPAN [US/C] : U.S.A./CANADA [K] : KOREA [E] : EUROPE
 [UK] : U.K. [JEX] : JAPAN & ASIA [A] : AUSTRALIA [T] : TAIWAN
 [CH] : CHINA [ETC] : U.S.A./CANADA/South America

注意

- プリント基板図は部品面を示しています。
- *印の部品は納期が若干かかります。あらかじめご了承ください。
- 分解図に部番のない部品および品番のない部品は供給できません。
- 標準の抵抗、コンデンサーは省略してあります。回路図を参照してください。
- △印は安全重要部品です。交換する時は必ず指定の部品を使用してください。

- 仕向先
 [J] : JAPAN [US/C] : U.S.A./CANADA [K] : KOREA [E] : EUROPE
 [UK] : U.K. [JEX] : JAPAN & ASIA [A] : AUSTRALIA [T] : TAIWAN
 [CH] : CHINA [ETC] : U.S.A./CANADA/South America



TASCAM[®]
TEAC PROFESSIONAL

SERVICE MANUAL

DR-07MKII

Linear PCM Recorder

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1. Specifications

仕様

Ratings

Recording media

microSD card (64 MB - 2 GB)
microSDHC card (4 GB - 32 GB)

Recording/playback format

WAV: 44.1/48/96 kHz, 16/24-bit
MP3: 44.1/48 kHz, 32/64/96/128/192/256/
320 kbps

Number of channels

2 channels (stereo)

Input/output ratings

Analog audio input/output ratings

MIC/EXT IN jacks (supporting plug-in power)

Connector: 1/8" (3.5 mm) stereo mini
Input impedance: 25 k Ω
Nominal input level: -20 dBV
Maximum input level: -4 dBV

/LINE OUT

Connector: 1/8" (3.5 mm) stereo mini
Output impedance: 12 Ω
Nominal output level: -14 dBV (10 k Ω load)
Maximum output level:
+2 dBV (10 k Ω load)
Maximum output: 20 mW + 20 mW (32 Ω load)

Built-in speaker 0.3 W (monaural)

Control input/output ratings

USB jack

Connector: Mini-B type
Format: USB 2.0 HIGH SPEED mass storage class

Audio performance

Frequency response

20 - 20 kHz +1/-3 dB (44.1 kHz, EXT IN to LINE
OUT) (JEITA)
20 - 22 kHz +1/-3 dB (48 kHz, EXT IN to LINE OUT)
(JEITA)
20 - 40 kHz +1/-3 dB (96 kHz, EXT IN to LINE
OUT) (JEITA)

Total harmonic distortion

0.05% or lower (EXT IN to LINE OUT,
Fs 44.1/48/96kHz) (JEITA)

S/N ratio

92dB or higher (EXT IN to LINE OUT,
Fs 44.1/48/96kHz) (JEITA)

Note) JEITA: Conforming to JEITA CP-2150

定格

記録メディア

microSDカード (64MB~2GB)
microSDHCカード (4GB~32GB)

録音再生フォーマット

WAV: 44.1/48/96 kHz, 16/24ビット
MP3: 44.1/48 kHz, 32/64/96/128/
192/256/320 kbps

チャンネル数

2チャンネル (ステレオ)

入出力定格

アナログオーディオ入出力定格

MIC/EXT IN 端子 (プラグインパワー対応)

コネクター: 1/8" (3.5mm) ステレオミニジャック
入力インピーダンス: 25k Ω
基準入力レベル: -20dBV
最大入力レベル: -4dBV

/LINE OUT 端子

コネクター: 1/8" (3.5mm) ステレオミニジャック
出力インピーダンス: 12 Ω
基準出力レベル: -14dBV (10k Ω 負荷時)
最大出力レベル: +2dBV (10k Ω 負荷時)
最大出力: 20mW+20mW (32 Ω 負荷時)

内蔵スピーカー

0.3W (モノラル)

コントロール入出力定格

USB 端子

コネクター: Mini-B タイプ
フォーマット: USB2.0 HIGH SPEED マスストレージ
クラス

オーディオ性能

周波数特性

20-20kHz +1/-3dB (EXT IN to LINEOUT,
Fs44.1kHz, JEITA)
20-22kHz +1/-3dB (EXT IN to LINEOUT,
Fs48kHz, JEITA)
20-40kHz +1/-3dB (EXT IN to LINEOUT,
Fs96kHz, JEITA)

歪率

0.05%以下 (EXT IN to LINE OUT,
Fs44.1k/48k/96 kHz, JEITA)

S/N 比

92dB以上 (EXT IN to LINE OUT,
Fs44.1k/48k/96 kHz, JEITA)

注) JEITA: JEITA CP-2150準拠

Computer compatibility

Windows Pentium 300 MHz or faster
128 MB or more memory
USB port (USB 2.0 recommended)

Macintosh Power PC, iMac, G3, G4 266 MHz or faster
64 MB or more memory
USB port (USB 2.0 recommended)

Recommended USB host controller

Intel chipset

Supported OS

Windows XP, Windows Vista,
Windows 7
Macintosh Mac OS X 10.2 or later

Other specifications

Power Two AA batteries (Alkaline or Ni-MH)
USB bus power supplied from a computer
AC adaptor (TASCAM PS-P515U, sold separately)

Power consumption

1.7 W (maximum)

Battery operation time (continuous operation)

● Alkaline type battery (EVOLTA)

Recording / playback	Format	Operation time	Note
Recording	WAV, 96kHz, 24bit	About 10,5 hours	Built-in microphone
Recording	WAV, 44.1kHz, 16bit	About 17,5 hours	Built-in microphone
Recording	MP3, 44.1kHz, 128Kbps	About 16 hours	Built-in microphone
Recording	MP3, 48kHz, 320Kbps	About 11 hours	Built-in microphone
Playback	WAV, 96kHz, 24bit	About 17 hours	Headphone
Playback	WAV, 96kHz, 24bit	About 17 hours	Built-in speaker
Playback	WAV, 44.1kHz, 16bit	About 19,5 hours	Headphone
Playback	WAV, 44.1kHz, 16bit	About 19,5 hours	Built-in speaker
Playback	MP3, 44.1kHz, 128Kbps	About 19,5 hours	Headphone
Playback	MP3, 44.1kHz, 128Kbps	About 18,5 hours	Built-in speaker

接続するパソコンの動作条件

Windowsマシン Pentium 300MHz以上
128MB 以上のMemory
USBポート (推奨 : USB2.0)

Macintoshマシン Power PC、iMac、G3、G4
266MHz以上
64MB以上のMemory
USBポート (推奨 : USB2.0)

推奨USBホストコントローラー

Intel製チップセット

サポートOS

Windows : Windows XP、Windows Vista、
Windows 7
Macintosh : Mac OS X 10.2以上

一般

電源 単3形電池2本 (アルカリ乾電池またはニッケル水素電池)
パソコンからのUSBバスパワー
専用ACアダプター
(TASCAM PS-P515U、別売)

消費電力 1.7W(最大時)

電池持続時間 (連続使用時)

● アルカリ乾電池 (EVOLTA) 使用時

録音/再生	フォーマット	持続時間	備考
録音時	WAV, 96kHz, 24ビット	約10.5時間	内蔵ステレオマイク入力時
録音時	WAV, 44.1kHz, 16ビット	約17.5時間	内蔵ステレオマイク入力時
録音時	MP3, 44.1kHz, 128kbps	約16時間	内蔵ステレオマイク入力時
録音時	MP3, 48kHz, 320kbps	約11時間	内蔵ステレオマイク入力時
再生時	WAV, 96kHz, 24ビット	約17時間	ヘッドホン使用時
再生時	WAV, 96kHz, 24ビット	約17時間	内蔵素スピーカー使用時
再生時	WAV, 44.1kHz, 16ビット	約19.5時間	ヘッドホン使用時
再生時	WAV, 44.1kHz, 16ビット	約19.5時間	内蔵素スピーカー使用時
再生時	MP3, 44.1kHz, 128kbps	約19.5時間	ヘッドホン使用時
再生時	MP3, 44.1kHz, 128kbps	約18.5時間	内蔵素スピーカー使用時

Recording / playback	Format	Operation time	Note
Playback	MP3,48kHz, 320Kbps	About 19,5 houes	Headphone
Playback	MP3,48kHz, 320Kbps	About 18,5 houes	Built-in speaker

● Ni-MH type battery (eneloop)

Recording / playback	Format	Operation time	Note
Recording	WAV,96kHz, 24bit	About 10 houes	Built-in microphone
Recording	WAV,44.1kHz, 16bit	About 15,5 houes	Built-in microphone
Recording	MP3,44.1kHz, 128Kbps	About 13 houes	Built-in microphone
Recording	MP3,48kHz, 320Kbps	About 11 houes	Built-in microphone
Playback	WAV,96kHz, 24bit	About 15 houes	Headphone
Playback	WAV,96kHz, 24bit	About 14 houes	Built-in speaker
Playback	WAV,44.1kHz, 16bit	About 16,5 houes	Headphone
Playback	WAV,44.1kHz, 16bit	About 16,5 houes	Built-in speaker
Playback	MP3,44.1kHz, 128Kbps	About 16 houes	Headphone
Playback	MP3,44.1kHz, 128Kbps	About 15 houes	Built-in speaker
Playback	MP3,48kHz, 320Kbps	About 16 houes	Headphone
Playback	MP3,48kHz, 320Kbps	About 15 houes	Built-in speaker

Dimensions (W x H x D)

68 x 158 x 26 mm
(25/8" x 63/16" x 1")
(when the microphone pair is close)
90 x 158 x 26 mm
(31/2" x 63/16" x 1")
(when the microphone pair is open)

Weight 127g (47/16 oz)
(not including batteries)

Operating temperature range
0 - 40°C (32°F - 104°F)

録音／再生	フォーマット	持続時間	備考
再生時	MP3,48kHz, 320kbps	約19.5時間	ヘッドホン使用時
再生時	MP3,48kHz, 320kbps	約18.5時間	内蔵素スピーカー使用時

録音時：JEITA録音時、再生時：JEITA音楽再生時

● ニッケル水素電池 (eneloop) 使用時

録音／再生	フォーマット	持続時間	備考
録音時	WAV,96kHz, 24ビット	約10.時間	内蔵ステレオマイク入力時
録音時	WAV,44.1kHz, 16ビット	約15.5時間	内蔵ステレオマイク入力時
録音時	MP3,44.1kHz, 128kbps	約13時間	内蔵ステレオマイク入力時
録音時	MP3,48kHz, 320kbps	約11時間	内蔵ステレオマイク入力時
再生時	WAV,96kHz, 24ビット	約15時間	ヘッドホン使用時
再生時	WAV,96kHz, 24ビット	約14時間	内蔵素スピーカー使用時
再生時	WAV,44.1kHz, 16ビット	約16.5時間	ヘッドホン使用時
再生時	WAV,44.1kHz, 16ビット	約16.5時間	内蔵素スピーカー使用時
再生時	MP3,44.1kHz, 128kbps	約16時間	ヘッドホン使用時
再生時	MP3,44.1kHz, 128kbps	約15時間	内蔵素スピーカー使用時
再生時	MP3,48kHz, 320kbps	約16時間	ヘッドホン使用時
再生時	MP3,48kHz, 320kbps	約15時間	内蔵素スピーカー使用時

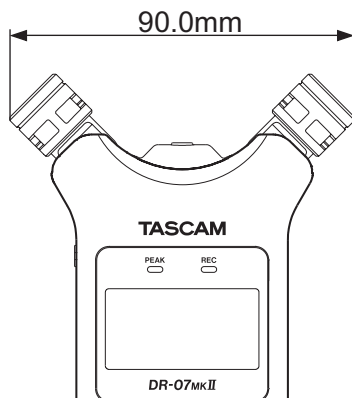
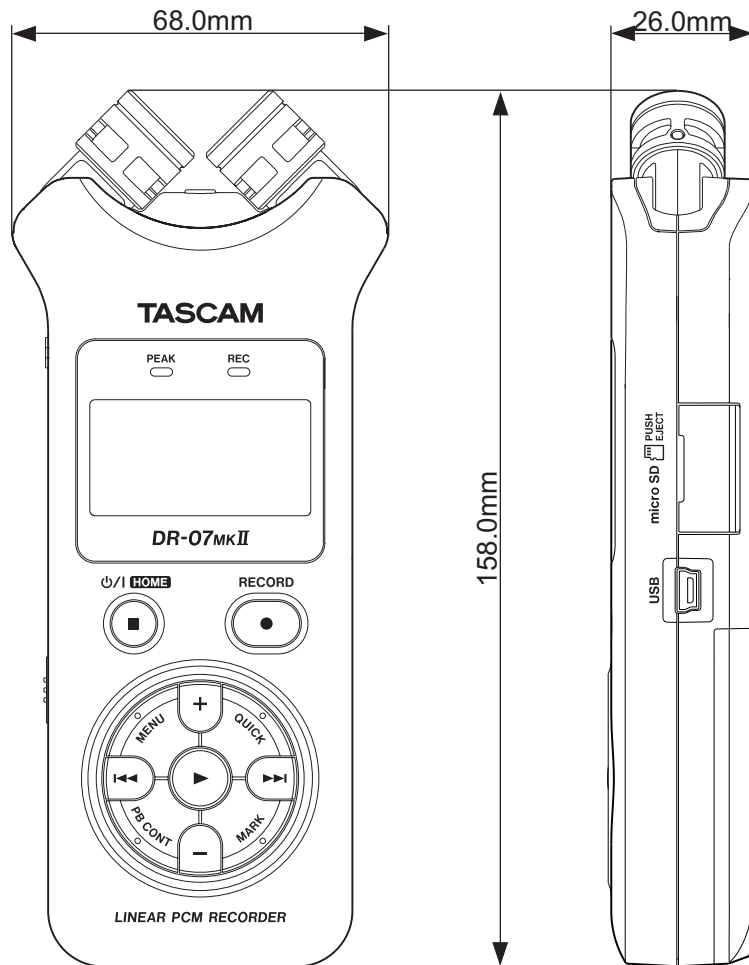
録音時：JEITA録音時、再生時：JEITA音楽再生時

外形寸法 68 x 158 x 26mm
(幅x高さx奥行き、マイク閉状態)
90 x 158 x 26mm
(幅x高さx奥行き、マイク開状態)

質量 127g (電池を含まず)

動作温度 0~40°C

Dimensional drawings(寸法図)



[Dimension of the microphone opened]
[マイク開状態の寸法]

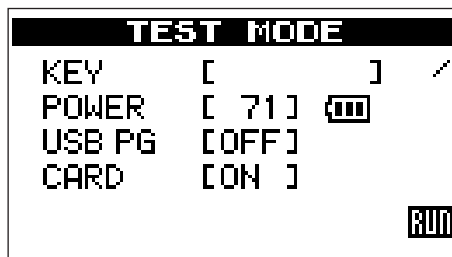
2. Test Mode

テストモード

1. How to enter test mode

While holding down the **QUICK+REW** keys, switch the power on.

The LCD shows the following message.



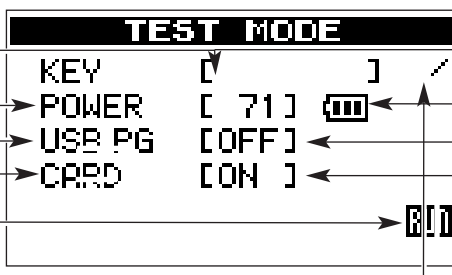
1. テストモードの起動方法

QUICK+REWキーを押しながら電源を投入する。

LCDに下記を表示する。

2. Displays explained

- Shows the name of a key pressed
- Power supply voltage (255 steps)
“ [] ” shown when powered on battery; “ AC ” shown when connected to an AC outlet.
- USB connection
- Card detection
- Operation indicator
- Event acceptance indicator. This indicator reacts when keys are operated for example



- 押されたキーを表示。
- 電源供給電圧 (255段階)
バッテリー時: [] AC接続時: AC
- USB接続
- カード検出
- 動作インジケータ
- イベント受付インジケータ。キーなど操作すると反応。

2. 画面の説明

3. Checking LEDs

REC LED: turns on when the **REC** key is pressed.

PEAK LED: turns on when the **MARK** key is pressed.

They turn off when the keys are held pressed for a certain time.

3. LED

REC LED: **REC**キーで点灯する。

PEAK LED: **MARK**キーで点灯する。

全てキーを長押しすると点滅する。

4. Menu

Pressing the **MENU** key reveals the following menu.

Options are selectable using the **◀◀**, **▶▶**, **+** and **-** key.

PLAY: mode selection

MENU: back to the TOP screen

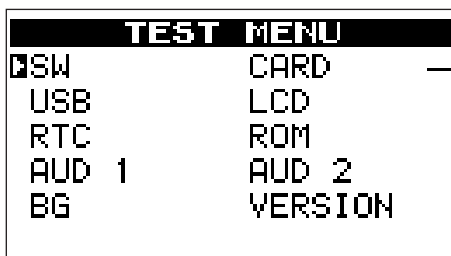
4. MENU

MENUキーを押すと下記メニューを表示する。

◀◀, **▶▶**, **+**, **-** キー操作で項目の移動をする。

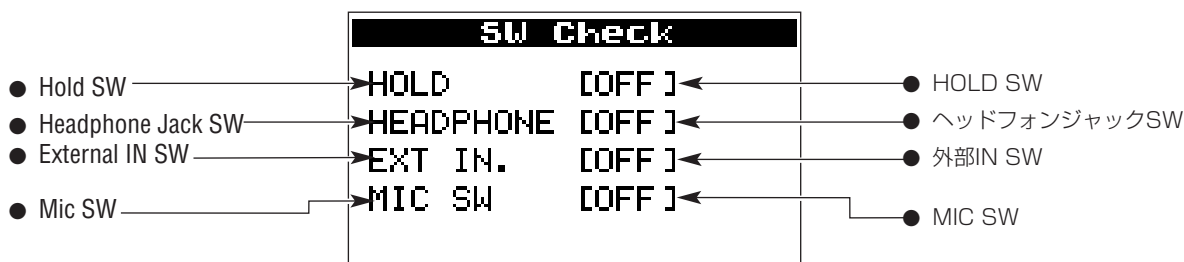
PLAY: 項目の選択。

MENU: TOP画面へ。



1) SW

Selecting "SW" and pressing the **PLAY** key gets you to the following menu:

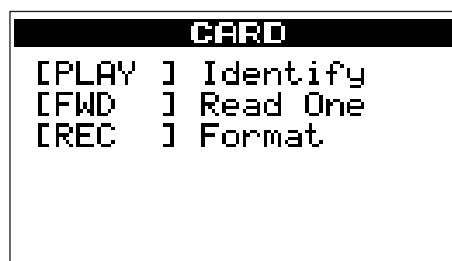


1)SW

"SW"を選択して**PLAY**キーを押すと下記メニューを表示する。

2) CARD

Selecting "CARD" and pressing the **PLAY** key gets you to the following menu:

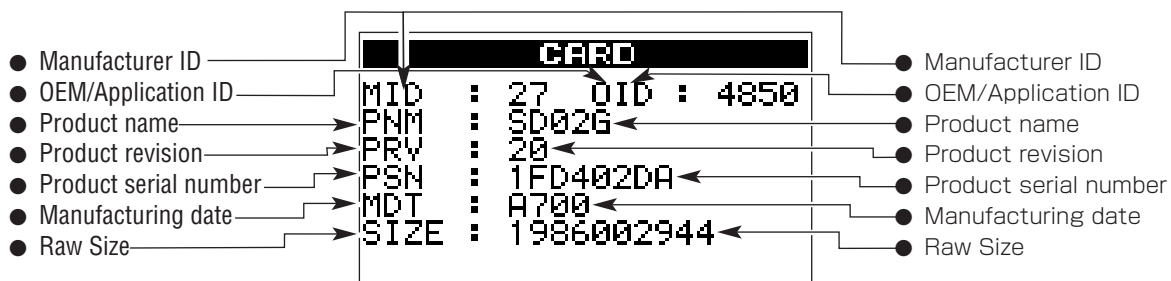


2)CARD

"CARD"を選択して**PLAY**キーを押すと下記メニューを表示する。

Identify: Read in data

Pressing the **PLAY** key indicates the following information:

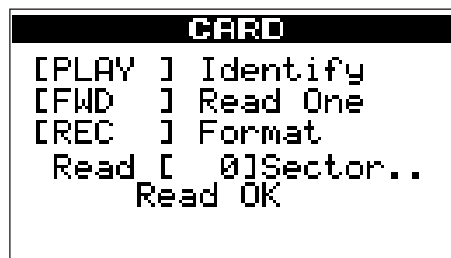


Identify : カードから情報の読み込み

PLAYキーを押すと下記の情報を表示する。

Read One: Read in data from the card per sector

At each press of the **▶▶** key, data is read in from the card per sector.

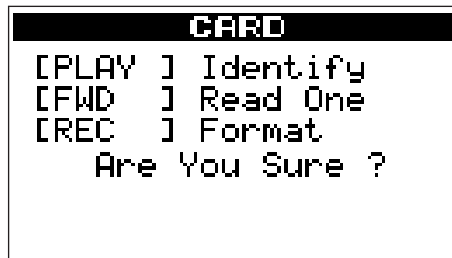


Read One : カードから1セクタ読み込み

▶▶キーを押すと、押すたびにカードから1セクター毎のデータの読み込みを行なう。

Format: Card formatting

At a press of the **REC** key, the following screen appears:



If **PLAY** key is pressed at this screen, the card starts being formatted. Upon completion of the formatting process, "**Complete**" is displayed.

Pressing **MENU** key brings you back to the top screen.

Format : カードフォーマット

RECキーを押すと下記画面を表示する。

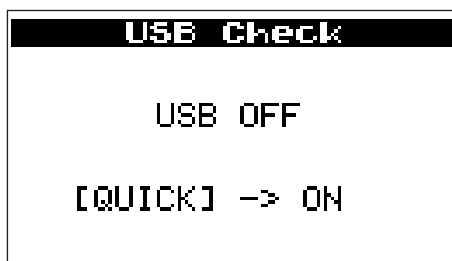
ここで**PLAY**キーを押すとFormatを実行し、実行後、"**Complete**"を表示して終了する。

MENUキーでTop画面へ戻る。

3) USB Check

Select "**USB**" and press the **QUICK** key.

Each time the **QUICK** key is pressed, the indication alternates between ON and OFF.

**3) USB Check**

"**USB**"を選択して**QUICK**キーを押す。

QUICKキーを押すたびにON/OFFを繰り返す。

4) LCD Check

Select "**LCD**" and press **PLAY** key and the following are displayed:

● Contrast adjustment
(+ : up; - : down)

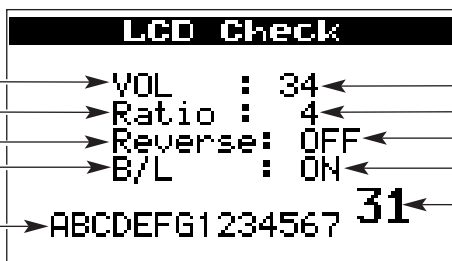
● adjustment
(▶▶ : +; ◀◀ : -)

● **REC**: Reverse

● **PLAY**: Back light ON/OFF

● Characters for after-image check

● **MARK**: All dots are displayed.



● コントラスト調整
(+ : アップ - : ダウン)

● コントラスト調整傾き
(▶▶ : + ◀◀ : -)

● **REC**: 反転

● **PLAY**: バックライトのON/OFF

● 残像確認用キャラクタ

● **MARK**: 全てのドットを表示

4) LCD Check

"**LCD**"を選択して**PLAY**キーを押すと下記画面を表示する。

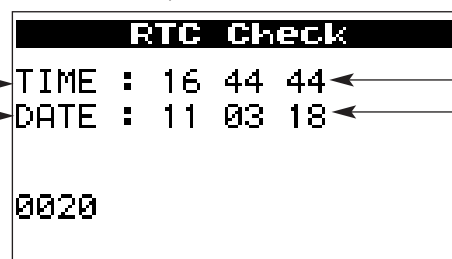
5) RTC Check

Select "**RTC**" and press **PLAY** key and the following are displayed:

Real-time clock indication.(Date and time indication only)

● Time

● Date (yy/mm/dd)
The year of 2000 is indicated as "00".



● 時刻.

● 日付 (年月日)
年は2000年を00と表示

5) RTC Check

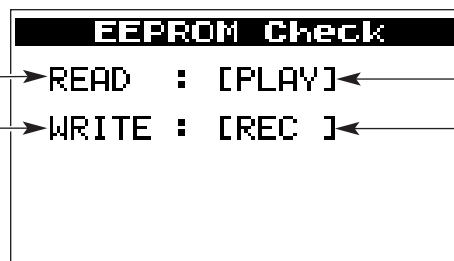
"**RTC**"を選択して**PLAY**キーを押すと下記画面を表示する。

リアルタイムクロック表示(日時の表示のみ)。

6) ROM Check

Select "ROM" and press **PLAY** key and the following are displayed:

- Read in from the ROM
"Reading..." is displayed at a press of the **PLAY** key.
- Writing all zeros to the ROM
The writing process starts at a press of the **PLAY** key in response to "Are you sure?"
To cancel the process, press the **MENU** key.



- ROMの読み込み実行。
PLAYキーで"Reading..."を表示。
- ROMのオールゼロ書き込み。
"Are you sure?"後に**PLAY**キーで書き込み。
MENUキーでキャンセル。

If errors occur during either the read or the write, the following are displayed:

- "Timeout Err" No response from the EEPROM
- "Error" Errors at data send/receive time
- "Verify Err" Errors in verification during the write process

6) ROM Check

"ROM"を選択して**PLAY**キーを押すと下記画面を表示する。

READ/WRITE共にエラーの場合には下記を表示する。

- "Timeout Err" EEPROMの応答なし
- "Error" データ送信/受信時のエラー
- "Verify Err" Write時のペリファイエラー

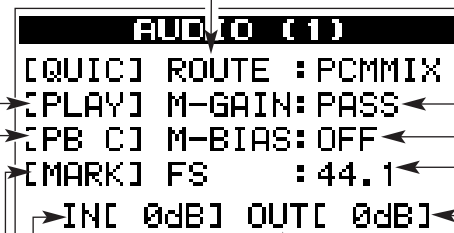
7) AUDIO Check

There are two audio check items: AUD 1 and AUD 2.
You can check audio by selecting either of "AUD 1" or "AUD 2" item.

AUD 1

Select "AUD 1" and press the **PLAY** key.

- **ROUTE:** Input routing setting.
Use the **QUICK** key to select PCMMIX, THRU or ADCMIX.
- **M-GAIN:** CODEC MIC pre-amp gain setting. Use the **PLAY** key to select PASS, 16dB, 17dB,, 31dB or 32dB.
- **M-BIAS:** CODEC MIC BIAS setting.
Use the **PB CONT** key to select OFF, 0.5, 0.6, 0.7, 0.8, 0.83 or 0.91.
- **FS:** Sampling frequency setting.
Use the **MARK** key to select 44.1kHz, 48kHz or 96kHz.
- **IN:** CODEC INPUT PGA setting.
Use the **◀▶** keys to select -6.0dB, -5.5dB, -5.0dB,, 11.5dB or 12.0dB.
- **OUT:** CODEC master volume setting. Use the **+/-** keys to select -102dB, -54dB, -52dB,, -2dB, 0dB, 1dB, 2dB,, 11dB or 12dB.



- **ROUTE :** 入力経路設定、**QUICK**キーで選択、PCMMIX /THRU/ADCMIX
- **M-GAIN:** CODEC MIC Pre-Amp ゲイン設定、**PLAY**キーで選択、PASS/16dB/17dB/.../31dB/32dB
- **M-BIAS:** CODEC MIC BIAS設定 **PB CONT**キーで選択、OFF/0.5/0.6/0.7 /0.8/0.83/0.91
- **FS:** サンプリング周波数選択 **MARK**キーで選択。44.1kHz/48kHz/96kHz
- **IN:** CODEC INPUT PGA設定、**◀▶**キーで選択、-6.0dB/-5.5dB/-5.0dB/.../11.5dB/12.0dB
- **OUT:** CODEC Master Volume設定、**+/-**キーで選択、-102dB/-54dB/-52dB/.../-2dB/0dB/1dB/2dB/.../11dB/12dB

7) AUDIO CHECK

AUD 1とAUD 2の2つあります。

"AUD 1"または"AUD 2"の項目を選択することにより、AUDIOのチェックができます。

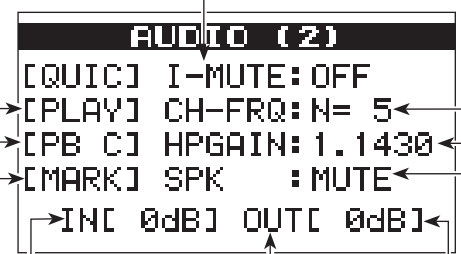
AUD 1

"AUD 1"を選択して**PLAY**キーを押す。

AUD 2

Select "AUD 2" and press the **PLAY** key.

- **U-MUTE:** CODEC ADC output mute setting. Use the **QUICK** key to select OFF or ON.
- **CH-FREQ:** CODEC Charge Pump Freq setting. Use the **PLAY** key to select N=0, 1, 2, ..., 14 or 15.
- **HPGAIN:** CODEC HP/LINE OUT gain setting. Use the **PB CONT** key to select 0.3959, 0.4571/0.5111, 0.6047, 0.7099, 0.9399, 1.000 or 1.1430.
- **SPK:** Speaker mute setting. Use the **MARK** key to select MUTE or ON.
- **IN:** CODEC INPUT PGA setting. Use the **◀▶** keys to select -6.0dB, -5.5dB, -5.0dB, ..., 11.5dB or 12.0dB.
- **OUT:** CODEC master volume setting. Use the **+/-** keys to select -102dB, -54dB, -52dB, ..., -2dB, 0dB, 1dB, 2dB, ..., 11dB or 12dB.



- **I-MUTE:** CODEC ADC 出力のミュート設定、**QUICK** キーで選択、OFF/ON
- **CH-FREQ:** CODEC Charge Pump Freq. 設定、**PLAY** キーで選択、N=0/1/2/.../14/15
- **HPGAIN:** CODEC HP/LINE OUT ゲイン設定、**PB CONT** キーで選択、0.3959/0.4571/0.5111/0.6047/0.7099/0.9399/1.000/1.1430
- **SPK:** スピーカーミュート設定、**MARK** キーで選択、MUTE/ON
- **IN:** CODEC INPUT PGA 設定、**◀▶** キーで選択、-6.0dB/-5.5dB/-5.0dB/.../11.5dB/12.0dB
- **OUT:** CODEC Master Volume 設定、**+/-** キーで選択、-102dB/-54dB/-52dB/.../-2dB/0dB/1dB/2dB/.../11dB/12dB

8) **BG**

Select "**BG**" and press **PLAY** key:

Background samples

FWD(▶▶): Previous; **REW**(◀◀): Next

9) **VERSION** Check

Select "**VERSION**" and press **PLAY** key and the following are displayed:

8) **BG**

"**BG**" を選択して **PLAY** キーを押す。

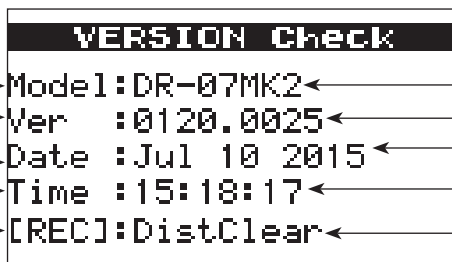
背景サンプル

FWD(▶▶): 後 **REW**(◀◀): 前

9) **VERSION** Check

"**VERSION**" を選択して **PLAY** キーを押すと下記画面を表示する。

- **Model Name**
- **Version of the system firmware.** The last 4 digits indicate a build number
- **on which the system firmware was built.**
- **which the system firmware was built.**
- **[REC]:** Language selection pop-up setting initialization.



- **モデル名**
- **システムファームのバージョン** 後半の4桁はビルド番号
- **ファームビルド日付**
- **ファームビルド時刻**
- **[REC]:** 言語選択ポップアップ設定初期化

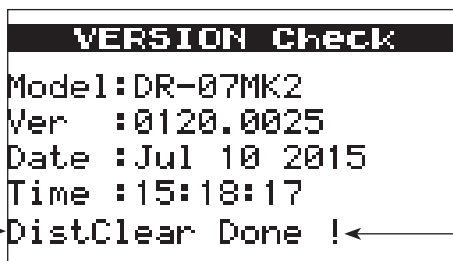
Press the **REC** button to clear the language selection pop-up setting flag. And the following screen appears.

(The language selection pop-up will be displayed at customer only the first time.)

REC キーを押して、言語選択ポップアップ設定済みフラグをクリアします。

(言語選択ポップアップは、客先での初回起動時のみ、表示されます。)

Language selection pop-up initialization Execution message.



言語選択ポップアップ初期化実行メッセージ

3. Updating of Firmware

ファームウェアのアップデート

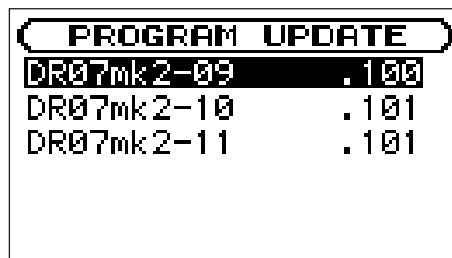
1. Preparations

- 1) Make the connection between this unit and the PC using a USB cable.
- 2) Place the update file in the UTILITY folder in the unit.
- 3) Perform the USB device “**remove**” action on the PC, and then switch off the power to the unit.

2. START-UP

While holding down the **MARK** and **REW** keys, switch the power on.

The LCD looks like this:



Update files are shown with extensions.

The USB connection can be made at this point.

When USB connected, the normal USB screen appears. When USB connection is made, the normal USB screen appears. When the USB cable is disconnected, the unit turns off.

1. 準備

- 1) 本体とPCをUSBケーブルで接続する。
- 2) アップデートファイルを本体の「UTILITY」フォルダに置く。
- 3) PCでUSBデバイスの“**取り外し**”を行い、本体の電源を落とす。

2. 起動

MARK+REWキーを押しながら電源を投入する。

LCDに下記を表示する。

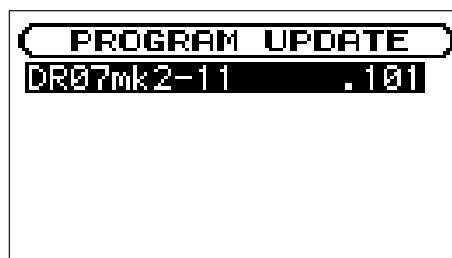
アップデートファイルを拡張子付きで表示する。

この時点でUSB接続することが可能です。

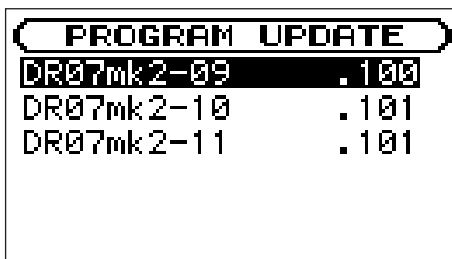
接続すると通常と同じUSB画面となり、USBケーブルを抜くと電源が切れます。

3. Displays explained

- 1) When only a single file is available:



- 2) When multiple files are available:



When there are 6 or more files, use the + key and - key to move the cursor over them.

3. 画面の説明

- 1) ファイルが一つの場合

- 2) ファイルが複数の場合

5つ以上の場合は+/-キーでカーソルが移動する。

3) When no update file is available:

Nothing can be done.

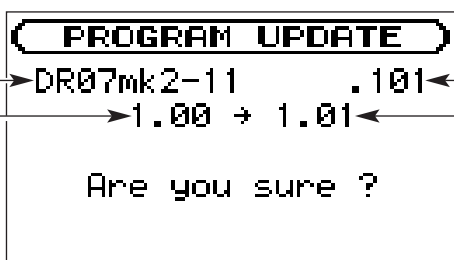
3) ファイルが無い場合

何も操作できません。

**4. File confirmation**Select a target file and press the **PLAY** key .**4. ファイルの確認**対象のファイルを選択し、**PLAY**キーを押す。

- Name of the file selected

- Current version at left and New version at right

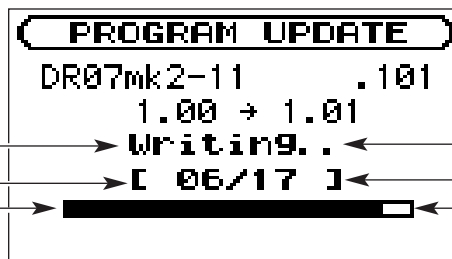


- 選択したファイル名

- 左: 現バージョン
右: 新バージョン

5. Getting update startedThe update process starts when pressing the **ENTER** key .**5. アップデート実行****ENTER**キーを押すとアップデートを実行する。

- Task progress.
- FLASH sector number
- Writing progress by sector



- 動作状況

- FLASHのセクタ番号

- セクタ単位の書き込み進捗

Pressing the **MENU** key brings you back to the file selection screen, as at step 2, without performing the update.アップデートを実行せず、2.のファイル選択画面へ戻るには**MENU**キーを押す。**6. Completion****6. 完了**Upon completion of the update process, "**Complete**" is displayed and the unit automatically switched off.アップデートが完了すると"**Complete**"と表示して自動的に電源が切れる。

7. Error messages

1) If an error occurs when selecting a file, the following messages appear:

Messages(メッセージ)	Meaning (内容)
Product	The product ID of the file does not match (the file may be for other products).
	ファイルのプロダクトIDが一致しない (別製品のファイルの可能性はある)。
Old Version	The file version is older than the current one.
	現バージョンよりもファイルのバージョンが古い。
Checksum	The checksum does not match.
	ファイルのチェックサムが一致しない。
Update File	Error in file reading.
	ファイル読み込みエラー。

7. エラー

1) ファイル選択時にエラーが発生した場合のメッセージ

2) If an error occurs in the data rewriting process, the following messages appear

2) 書き換え時にエラーが発生した場合のメッセージ

Messages(メッセージ)	Meaning (内容)
Flash Erase	Error in erasing.
	消去エラー
Flash Blank	Blank error as a result of data erasure.
	消去後のブランクエラー
Flash Write	Error in writing.
	書き込みエラー
Flash Verify	Error in verification after data has been written.
	書き込み後のベリファイエラー

4. Messages Explained

メッセージ一覧

The following is a list of the popup messages that might appear on the DR-07MK2 under certain conditions. Refer to this list if one of these popup messages appears and you want to check the meaning or determine a proper response.

以下にポップアップメッセージの一覧表を示します。

DR-07MK2では、状況に応じてポップアップメッセージが表示されますが、それぞれのメッセージの内容を知りたいとき、および対処方法を知りたいときにこの表をご覧ください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
File Name ERR	The DIVIDE function would cause the file name to exceed 200 characters. The DIVIDE function adds “_a” or “_b” to the end of the file name. Before choosing the DIVIDE function, connect the unit to a computer and edit the file name to less than 198 characters.
	DIVIDEによりファイル名の文字数が200文字を超えました。DIVIDEを行うとファイル名の末尾に“_a”または“_b”が追加されます。DIVIDEを行う前にパソコンと接続し、198文字以下のファイル名に変更してください。
Dup File Name	The DIVIDE function would cause the file name to be the same as that of an existing file. The DIVIDE function adds “_a” or “_b” to the end of the file name. Before choosing the DIVIDE function, connect the unit to a computer and edit the file name.
	DIVIDEにより作成されるファイルと同じファイル名のファイルが同じフォルダ内に既に存在します。DIVIDEを行うとファイル名の末尾に“_a”または“_b”が追加されます。DIVIDEを行う前にパソコンと接続し、ファイル名を変更してください。
File Not Found	The file added to the playlist cannot be found or a file could be damaged. Please check the file in question.
	プレイリストに登録されているファイルが見つからないか、ファイルが壊れている可能性があります。対象のファイルを確認してください。
Non-Supported	The audio file is not a supported format.
	ファイル形式がサポート対象外です。
Battery Empty	The battery is almost out of power. Replace the AA batteries.
	電池の残量がありません。電池を交換してください。
I/O Too Short	The IN and OUT points are too close together. Reset the IN and OUT points with at least 1 second between them.
	IN点とOUT点の間隔が短すぎます。1秒以上空けて設定してください。
File Not Found PLAYLIST	The file in the Playlist cannot be found. Please confirm that the file is still in the Music Folder.
	プレイリストに登録されているファイルが見つかりません。MUSICフォルダ内に対象のファイルがあるか確認してください。
No PLAYLIST	No files have been added to the Playlist. Add a file to the Playlist or change the play mode to something besides PLAYLIST.
	プレイリストにファイルが登録されていません。プレイリストにファイルを登録するか、プレイモードを「PLAYLIST」以外に設定してください。
PLAYLIST Full	The playlist is full. You cannot add more than 99 tracks to the Playlist.
	プレイリストが一杯です。プレイリストには、最大99ファイルまで登録可能です。
MBR Error Init CARD	The card is not formatted properly or the formatting is broken. Change the card or press the PLAY key when this message appears to format the card in FAT format . CAUTION Execution of FAT formatting erases all data currently on the card.
	カードが正常にフォーマットされていないか、カードが壊れている可能性があります。カードを交換するか、このメッセージが表示されている状態で PLAY キーを押すと、FATフォーマットが実行されます。 注意 FATフォーマットが実行されるとカード内のデータは、すべて消去されます。

Messages(メッセージ)	Meaning and response(内容と対処方法)
Format Error Format CARD	The FAT formatting of the card is abnormal or broken. This message also appears if you FAT formatted the card using a computer connected by USB and if a new card is inserted in the unit. Always use the DR-07MK2 to conduct FAT formatting of cards to be used with it. Change the card or press the PLAY key when this message appears to format the card in FAT format. CAUTION Execution of FAT formatting erases all data currently on the card.
	カードが正常にフォーマットされていないか、カードが壊れている可能性があります。このメッセージは、USB接続したパソコンでFATフォーマットした場合や未フォーマットのカードを挿入した場合にも表示されます。フォーマットは、必ずDR-07MK2本体で行ってください。カードを交換するか、このメッセージが表示されている状態で PLAY キーを押すと、FATフォーマットが実行されます。 注意 FATフォーマットが実行されるとカード内のデータは、すべて消去されます。
File Not Found Make Sys File	The system file is missing. This unit requires a system file for operation. When this message appears, press PLAY key to automatically create a system file.
	本機を使用するために必要なシステムファイルがありません。このメッセージが表示されている状態で PLAY キーを押すと、システムファイルが作られます。
Invalid SysFile Make Sys File	The system file required to operate this unit is invalid. When this message appears, press PLAY key to automatically create a system file.
	本機を使用するために必要なシステムファイルが正常ではありません。このメッセージが表示されている状態で PLAY キーを押すと、新しいシステムファイルが作られます。
Invalid Card Change Card	Something might be wrong with the card. Change the card.
	カードが正常でない可能性があります。カードを交換してください。
Write Timeout	Writing to the card timed out. Backup files on the card to your computer, and format the card.
	カードへの書き込みが間に合いませんでした。 ファイルをパソコンへバックアップの上、フォーマットを実行してください。
Card Full	The card has no remaining capacity. Erase unnecessary files or move them to your computer to make open space.
	カードの残容量がありません。不要なファイルを削除するかパソコンへ移動してください。
Layer too Deep	Folders can be created down to two layers. You cannot create a new folder inside the current folder.
	フォルダは、2階層までです。このフォルダ内に新たなフォルダを作成することはできません。
Can't Divide	The position selected for divide is not suitable (too close to the beginning or end of a track).
	DIVIDE実行時に分割位置が適切ではありません。(曲の先頭、曲の最後)
Max File Size	The file is larger than the designated size or the recording time exceeded 24 hours.
	ファイルのサイズが指定のサイズを超えました。あるいは録音時間が24時間を超えました。
File Full	The total number of folders and files exceeds 5000. Erase unnecessary files or move them to your computer.
	フォルダとファイルの総数が制限値(5000個)を超えました。不要なフォルダやファイルを削除するかパソコンへ移動してください。

Messages(メッセージ)	Meaning and response(内容と対処方法)
Card Error	The card could not be handled properly. Replace the card.
	カードを正常に認識できません。カードを交換してください。
Current File MP3	MP3 files cannot be divided.
	MP3ファイルの分割はできません。
File Protected	The file is read only and cannot be erased.
	リードオンリーファイルのため、削除できません。
No Card	No card is in the unit, so recording is not possible.
	カードが無いため、録音できません。
No PB File	There is no file that can be played back. The file might be damaged.
	再生可能なファイルがありません。ファイルが壊れている可能性があります。
No MUSIC File	There is no playback file, so DIVIDE and OVERDUB cannot be executed.
	再生ファイルが無いため、DIVIDE、OVERDUBは実行できません。
Cannot overdub! See REC setting	ou cannot overdub a WAV file with a sampling frequency of 96kHz in MP3 format. Change the recording format to WAV.
	96kHzのWAVファイルをMP3でオーバーダビングすることはできません。録音フォーマットをWAVにしてください。

System Error Messages (システムエラーメッセージ)

Messages(メッセージ)	Description(説明)	Cause(原因)
Not Continued	Playback not stopped, or card unmounted error.	The card or firmware may be defective.
	再生系の停止が未完了、あるいはカードのアンマウント時のエラー	カード不良もしくはF/Wの不具合の可能性有り。
File Error	File system error or recording/playback circuitry error.	The card or firmware may be defective.
	ファイルシステム上でエラー、あるいは録再生でのエラー	カード不良もしくはF/Wの不具合の可能性有り。
Can't Save Data	Write in the EEPROM or system file failed during shutdown or switching to USB.	Check that the card is inserted. The card may be defective. If the error occurs with the EEPROM, the PCB may be defective.
	シャットダウン時やUSB切り替え時にEEPROMあるいはシステムファイルへの書き込みが出来なかった。	カードの挿入を確認。 カード不良の可能性有り。 EEPROMの場合はPCB不良の可能性有り。
Player Error	Internal error in recording / playback.	The firmware may be defective.
	記録再生の内部的エラー	F/Wの不具合の可能性有り。
Device Error	Device Error 2: RTC initialization error.	The PCB may be defective.
	Device Error 2 : RTC初期化エラー	PCB不良の可能性有り。
Writing Failed	File creation error at the start of recording or file close error at the end of recording.	Confirm whether the error occurred during start or end of recording. The card may be defective.
	記録開始時のファイル作成エラー、あるいは記録終了時のファイルクローズエラー	録音開始時か記録終了時かの確認。 カード不良の可能性有り。
Sys Rom Err	Serial ROM read error.	The PCB may be defective.
	Serial ROMの読み込みエラー	PCB不良の可能性有り。
Remote Cmd	Error in communication with the the microcomputer for a remote control.	The firmware may be defective.
	リモート用マイコンとの通信でエラー。	F/Wの不具合の可能性有り。
Remote Rx	Error in communication with the the microcomputer for a remote control.	The microcomputer for a remote control or firmware may be defective.
	リモート用マイコンとの通信でエラー	リモート用マイコンもしくはF/Wの不具合の可能性有り。
System Err 50	Other fatal error.	The firmware may be defective.
	その他の致命的エラー	F/Wの不具合の可能性有り。
System Error 1	CPU access error.	The firmware may be defective.
	CPUのアクセスエラー	F/Wの不具合の可能性有り。
System Error 2	CPU address error.	The firmware may be defective.
	CPUのアドレスエラー	F/Wの不具合の可能性有り。
System Error 3	CPU instruction error.	The firmware may be defective.
	CPUのインストラクションエラー	F/Wの不具合の可能性有り。

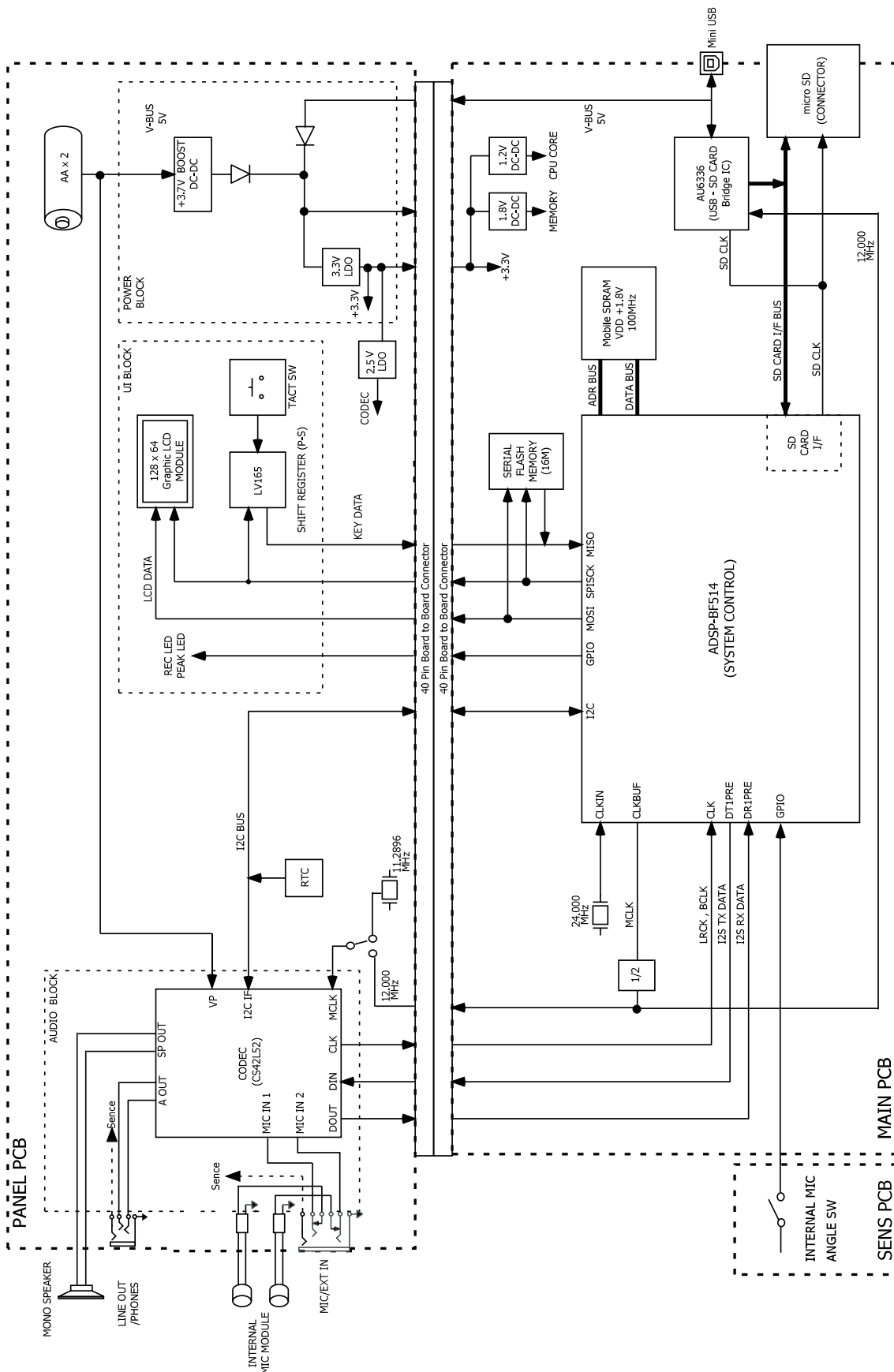
Messages(メッセージ)	Description(説明)	Cause(原因)
System Error 4	CPU zero division error.	The firmware may be defective.
	CPUのゼロ除算エラー	F/Wの不具合の可能性有り。
System Error 5	CPU Privilege Violation error.	The firmware may be defective.
	CPUのPrivilege Violationエラー	F/Wの不具合の可能性有り。
System Error 6	CPU Unimplemented line-a opcode error.	The firmware may be defective.
	CPUのUnimplemented line-a opcodeエラー	F/Wの不具合の可能性有り。
System Error 7	CPU Unimplemented line-f opcode error.	The firmware may be defective.
	CPUのUnimplemented line-f opcodeエラー	F/Wの不具合の可能性有り。
System Error 8	CPU format error.	The firmware may be defective.
	CPUのフォーマットエラー	F/Wの不具合の可能性有り。
System Error 9	CPU Uninitialized Interrupt error.	The firmware may be defective.
	CPUのUninitialized Interruptエラー	F/Wの不具合の可能性有り。

5. Block Diagram

ブロックダイアグラム

Exploded View-1

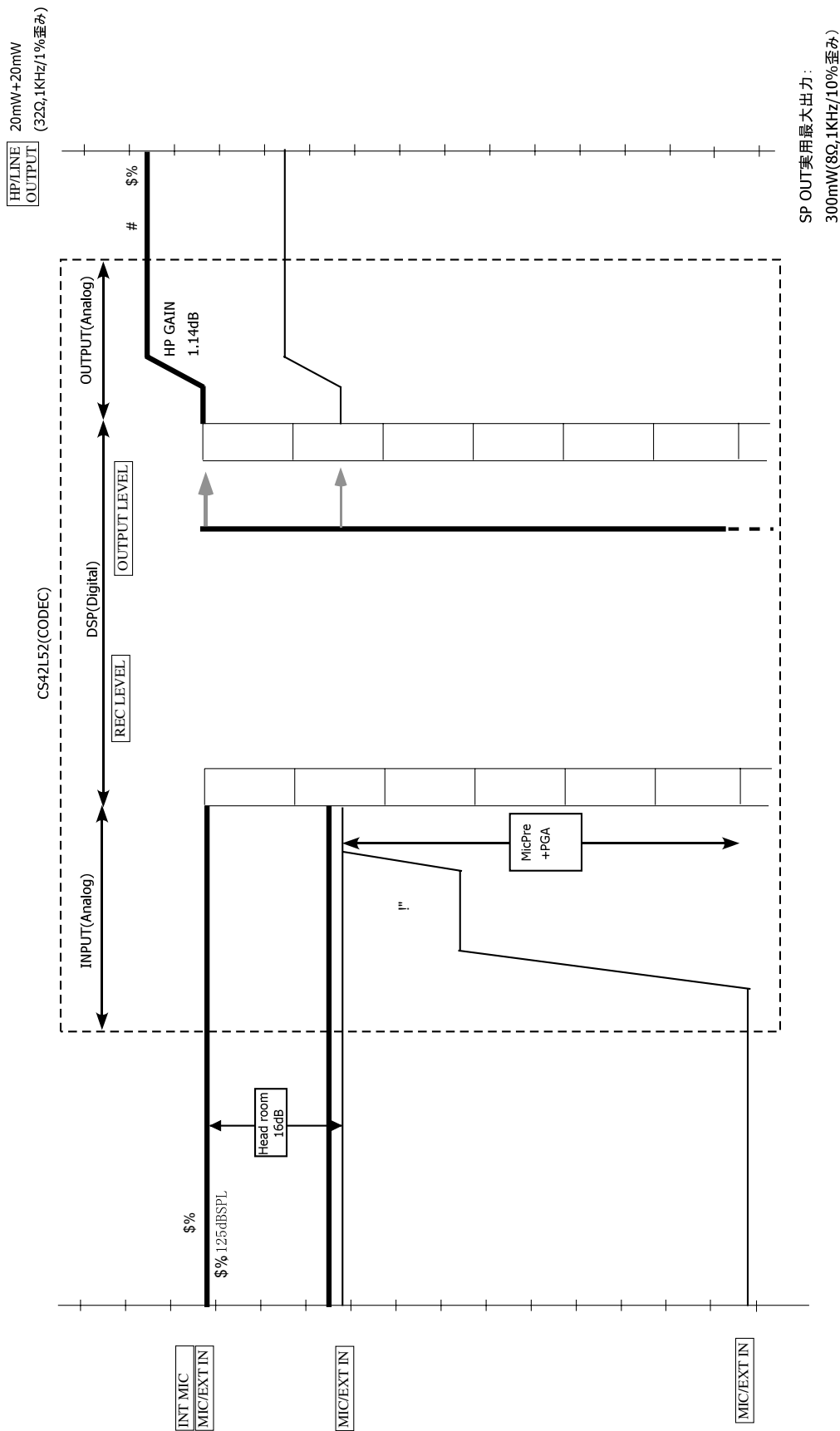
DR-07MKII Block Diagram



6. Level Diagram

レベルダイアグラム

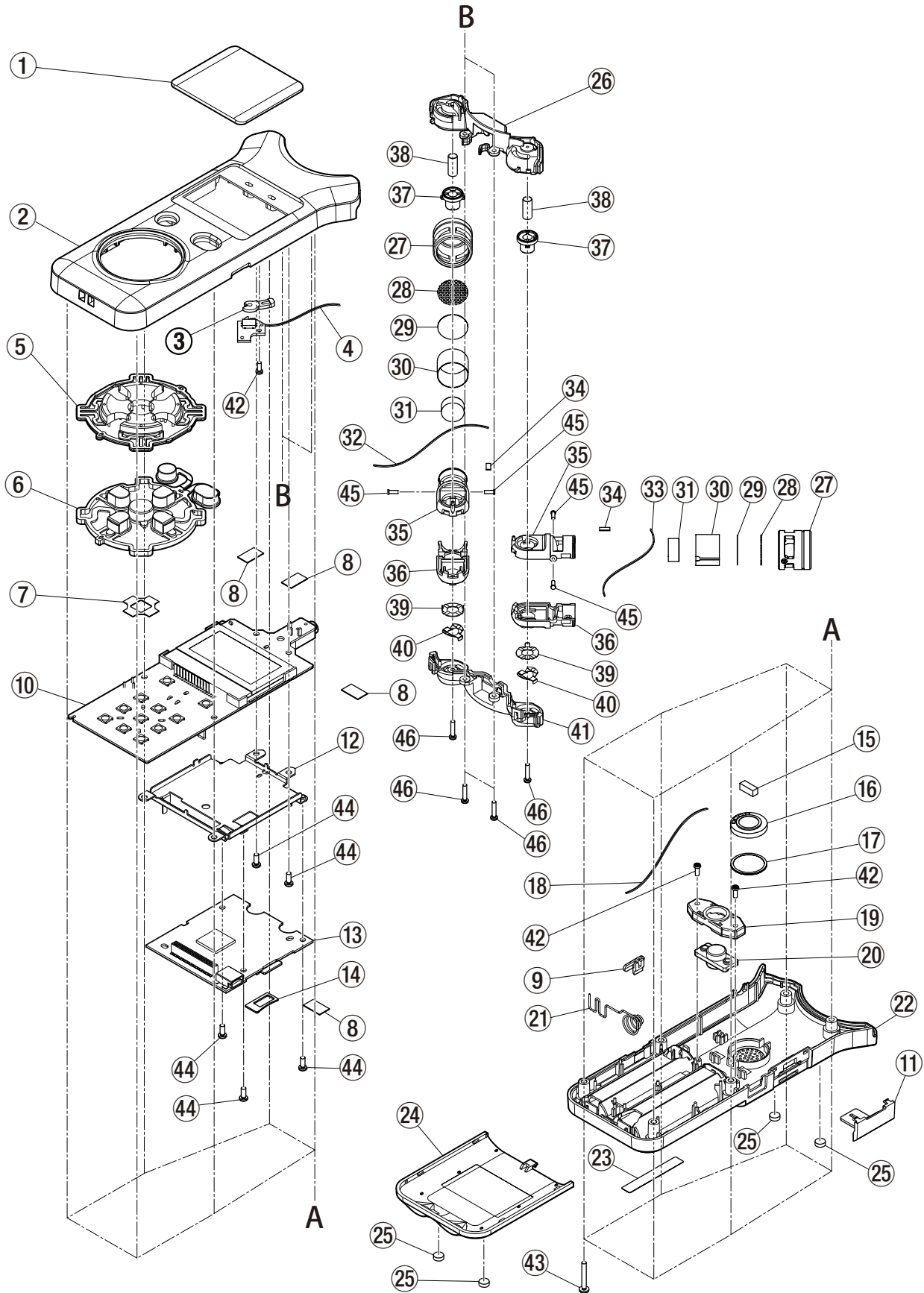
DR-05/DR-07MKII Level Diagram



7. Exploded Views and Parts List

分解図とパーツリスト

Exploded View-1



Exploded View-1

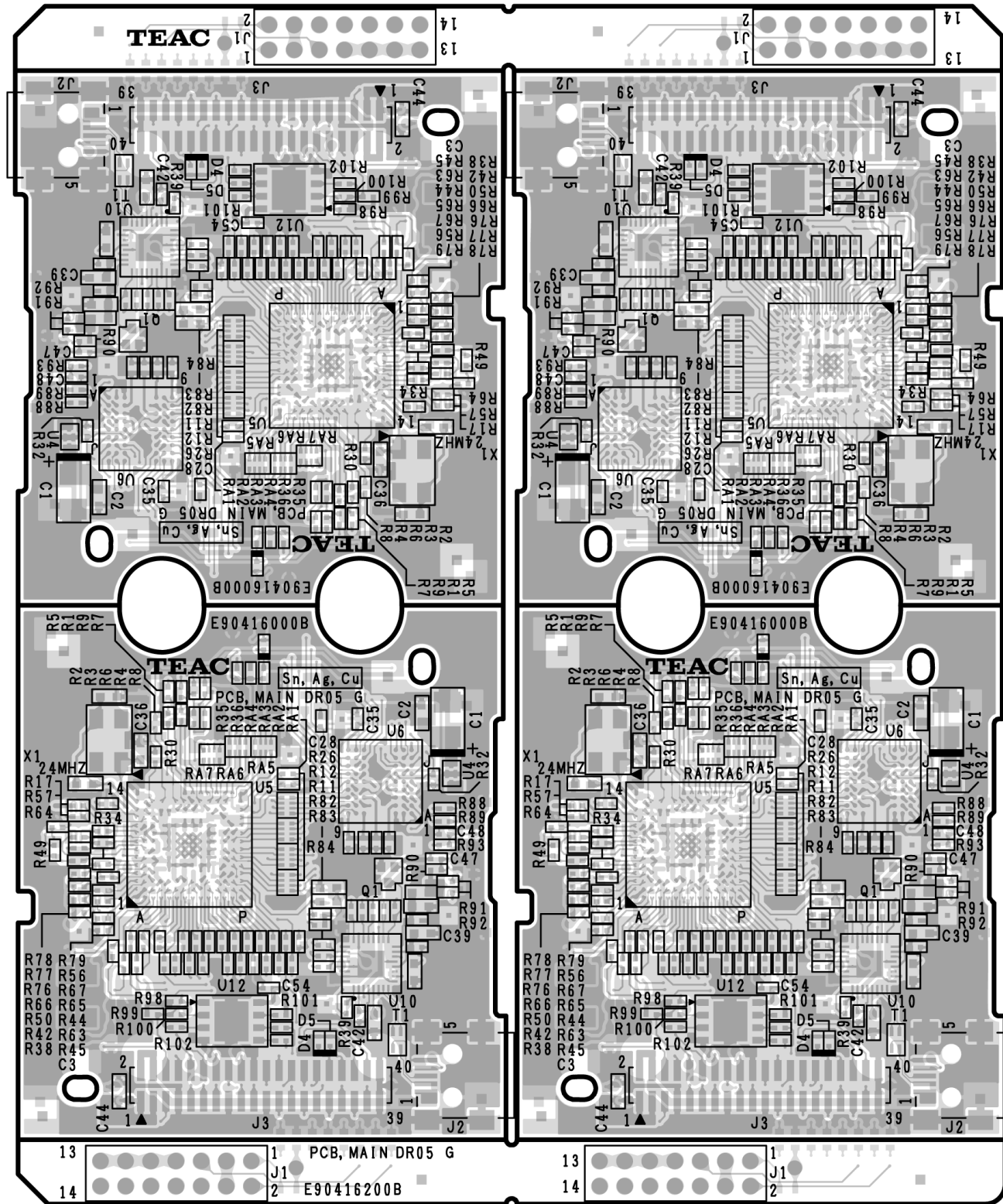
REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	M03270610A	WINDOW,07MK2 G	
1- 2	M03311300D	CASE, TOP 07MK2 G	
1- 3	M03311600B	LEVER, SENSOR 07MK2 G	
1- 4	E95425400A	PCB ASSY, SENS DR07MK2 G	Refer to page 27 (GATHER PCBA, PANEL 07MK2 G)
1- 5	M03269100C	BUTTON, MENU DR05 G	
1- 6	M03269200B	BUTTON, TRANS DR05 G	
1- 7	M03279700A	SHEET, PANEL DR05 G	
1- 8	M03142400A	SHEET, HM 6*10 G	
1- 9	M03269300A	KNOB, SLIDE DR05 G	
1-10	E95416110A	PCB ASSY, PANEL DR07MK2 G	Refer to page 26 (GATHER PCBA, MAIN 07MK2 G)
1-11	M03270300A	COVER, MICRO SD DR05 G	
1-12	M03269800B	CHASSIS, DR05 G	
1-13	E95416010A	PCB ASSY, MAIN DR07MK2 G	Refer to page 26 (GATHER PCBA, MAIN 07MK2 G)
1-14	M03322400A	SHEET, MSD DR05 G	
1-15	M03270200A	SHEET, CUSHION 8*3*T3 G	
1-16	E0166440	SPEAKER, HF-16008G-22 G	
1-17	M03270100A	SHEET, SPEAKER DR05 G	
1-18	E01749400A	WIRE, SPK P_ P8 DR05 G	
	E01749500A	WIRE, SPK N_ P7 DR05 G	
1-19	M03270000A	HOLDER, TRIPOD DR05 G	
1-20	M02954600A	ESCUTCHEON, TRIPOD DR100 G	
1-21	M03270400A	SPRING, BAT DR05 G	
1-22	M03311400D	CASE, BTM 07MK2 G	
1-23	M03313800A	NAMEPLATE, 07MK2 G	
1-24	M03270700B	COVER, BAT DR05 G	
1-25	M03270800B	FOOT, PORON T1.5 G	
1-26	M03311700C	COVER, ARM UP 07MK2 G	
1-27	M03311900A	CASE, MIC 07MK2 G	
1-28	M03312000A	PLATE, TOP 07MK2 G	
1-29	M03312100A	SHEET, TOP 07MK2 G	
1-30	M03312200A	SHEET, MESH 07MK2 G	
1-31	E0176850	MICROPHONE, EM182-M1 G	
1-32	E01767600A	WIRE, MIC D_P1P6 DR07MK2 G	
	E01767700A	WIRE, MIC S_P2 DR07MK2 G	
	E01767800A	WIRE, MIC G_P3P5 DR07MK2 G	
1-33	E01767600A	WIRE, MIC D_P1P6 DR07MK2 G	
	E01767900A	WIRE, MICR S_P4 DR07MK2 G	
	E01767800A	WIRE, MIC G_P3P5 DR07MK2 G	
1-34	M03309700A	SHEET, HM 2*4.5 G	
1-35	M03312300B	HOLDER, MIC UP 07MK2 G	
1-36	M03312400B	HOLDER, MIC LOW 07MK2 G	
1-37	M03312500B	COLLAR, MIC 07MK2 G	
1-38	M03312600A	COLLAR, BUSH 3.4*4*L9.5 G	
1-39	M03108700A	PLATE, HINGE VR20 G	
1-40	M03326900A	LEAF SPR, MIC 07MK2 G	
1-41	M03311800C	COVER, ARM LOW 07MK2 G	
1-42	B00312500A	SCREW, MPPR 1.7*4.5 FZB G	
1-43	B00325800A	SCREW, BPB M2*5*9 FZB G	
1-44	B00303605A	SCREW, MPBR 2*5 FNI G	
1-45	B00326100A	SCREW, MPBR 1.4*4FCM G	
1-46	B00326200A	SCREW, MPPR 1.7*8FCM G	

8. PC Boards and Parts List

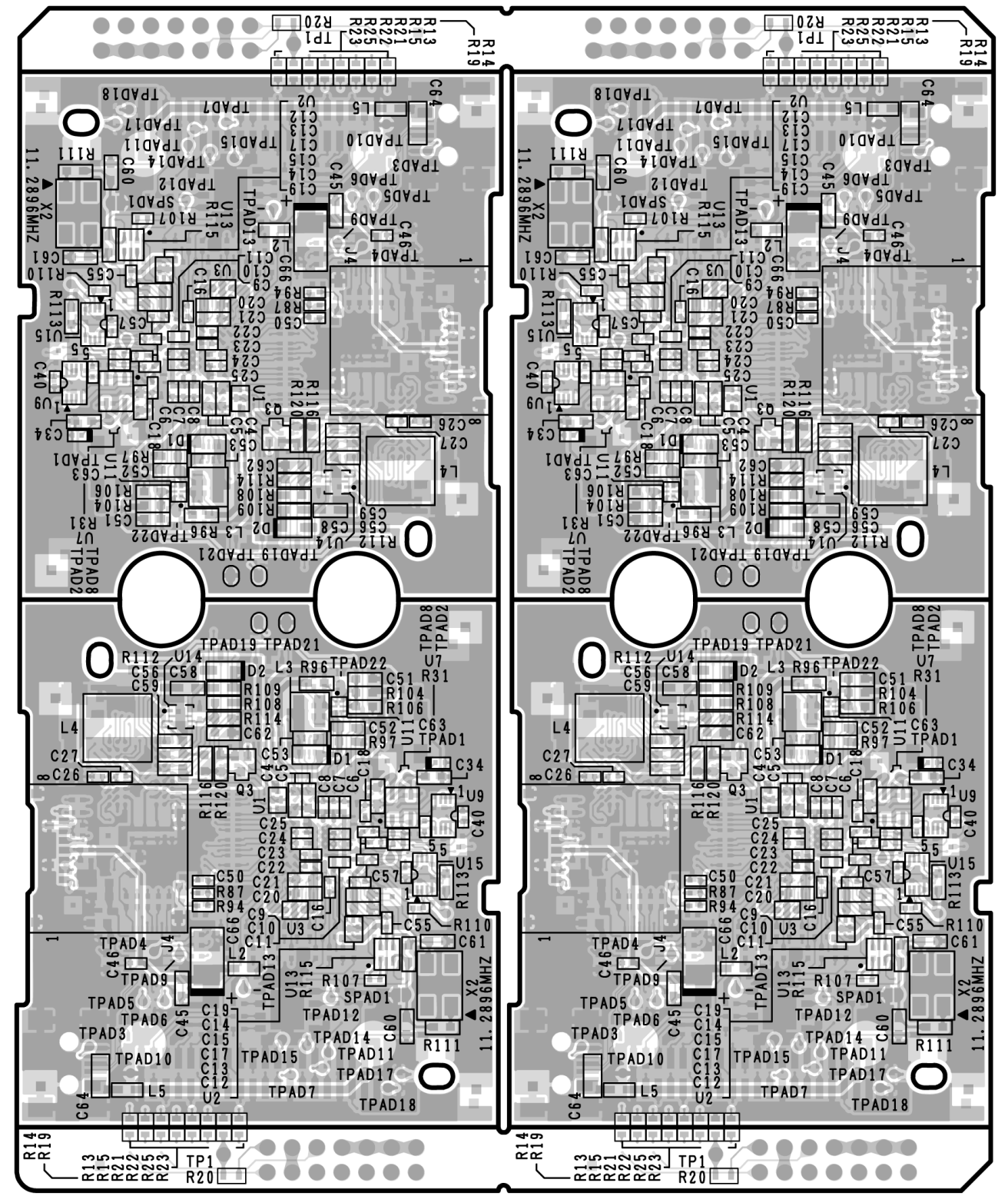
基板図とパーツリスト

GATHER PCB,MAIN DR05 G

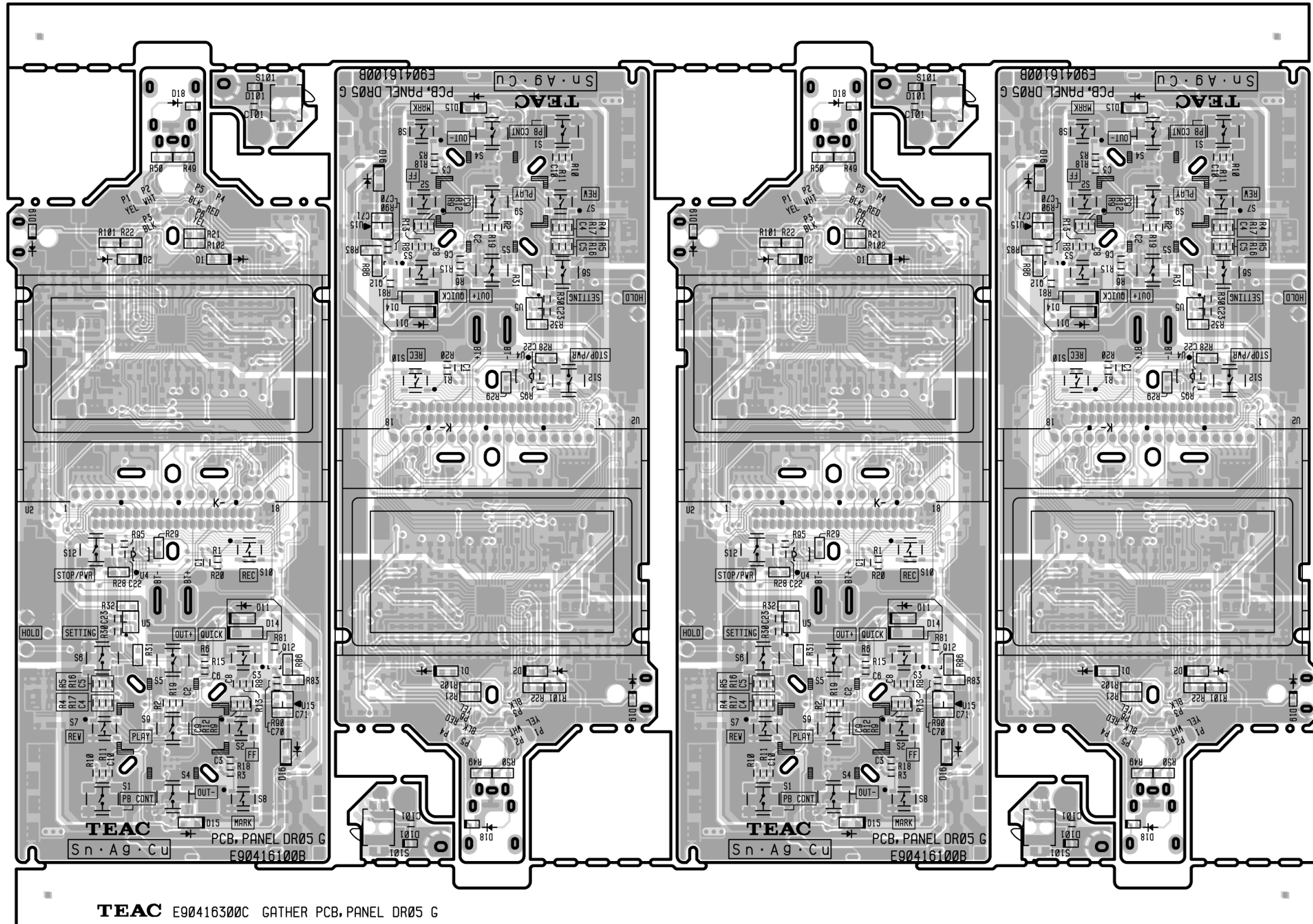
(Side A)



(Side B)

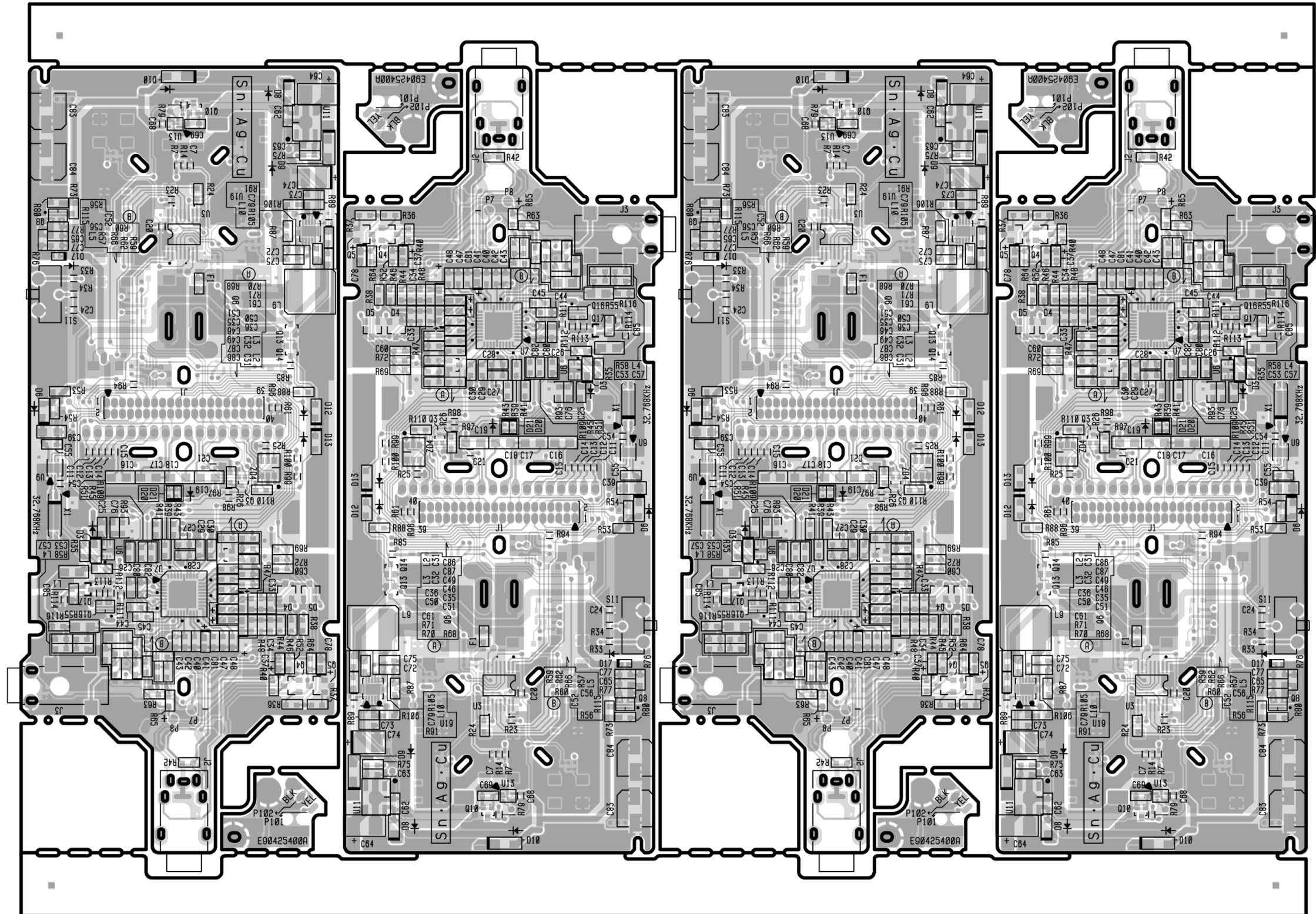


GATHER PCB,PANEL DR05 G (Side A) Rev:C



TEAC E90416300C GATHER PCB, PANEL DR05 G

GATHER PCB,PANEL DR05 G (Side B) Rev:C



GATHER PCBA,MAIN 07MK2 G

REF.NO.	PARTS NO.	DESCRIPTION
	E95416210A (E90416000B)	GATHER PCBA,MAIN 07MK2 G PCB,MAIN DR05 G
	(E95416010A)	PCB ASSY,MAIN DR07MK2 G
D1	S0022094	DIODE,1SS355
D6	S0086044	ZENER DIO,CDZCT2R6.8B G
J2	E0143954	CONNECTOR,USB MINI-5B G
J3	E0174113	CONNECTOR,2200SB40GSM45 G
J4	E0170384	CONN,SCHA4B0100 G
L1	E0126164	BEAD COIL,BLM18PG471SN1D G
L2	E0126164	BEAD COIL,BLM18PG471SN1D G
L3	E0165254	COIL,LQH3NPN2R2MMO G
L4	E0069824	COIL,CDRH5D28-100NC G
L5	E0126164	BEAD COIL,BLM18PG471SN1D G
Q1	S0065074	TRANSISTOR,DTC124EUA TP G
Q3	S0065074	TRANSISTOR,DTC124EUA TP G
RA1	R0180534	RES ARRAY,1/32W 4* 56 J G
RA2	R0180534	RES ARRAY,1/32W 4* 56 J G
RA3	R0180534	RES ARRAY,1/32W 4* 56 J G
RA4	R0180534	RES ARRAY,1/32W 4* 56 J G
RA5	R0180554	RES ARRAY,1/32W 4*68 J G
RA6	R0180554	RES ARRAY,1/32W 4*68 J G
RA7	R0180554	RES ARRAY,1/32W 4*68 J G
T1	E0166304	FILTER,NT2012 985BH1007 G
U1	C0086034	CC3,NFM18PS105R0J3D G
U2	C0086034	CC3,NFM18PS105R0J3D G
U3	C0086034	CC3,NFM18PS105R0J3D G
U4	C0086034	CC3,NFM18PS105R0J3D G
U5	S0088574	IC,ADSP-BF-514KBCZ-4 G
U6	S0088994	IC,FMS4A16LCH-60EE G
U7	S0065024	IC,BD46285G G
U9	S0089084	IC,SN74LVC1G74DCUR G
U10	S0079744	IC,AU6336-MOF G
U11	S0088594	IC,TPS62231DRY G
U12	S0090083	IC,MX25L1606EZNI12G G
U12	S00901510A	IC,ROM ASSY MAIN 07MK2 G
U12	D01138110A	SOFTWARE SPEC,07MK2 G
U13	S0065014	IC,SN74LVC2GU04DCKR G
U14	S0090094	IC,XC9237D08CER-G HF
U15	S0085594	IC,SN74LVC2G157DCUR G
X1	E0175134	RESONATOR,24.0MHZ 6035 G
X2	E0141174	RESONATOR,11.2896MHZ G

GATHER PCBA,PANEL 07MK2 G

REF.NO.	PARTS NO.	DESCRIPTION
D	E95416310A (E90416100B) (E90425400A)	GATHER PCBA,PANEL 07MK2 G PCB,PANEL DR05 G PCB,SENS DR07MK2 G
	(E95416110A)	PCB ASSY,PANEL DR07MK2 G
	M01502000A	LABEL, TYPE 12*6(BLANK) G
BT+	M03271600A	SPRING,PLUS DR05 G
BT-	M03271500A	SPRING,MINUS DR05 G
D1	S0083594	LED,SML-E12U8W G
D10	S0071644	DIODE,RB161M-20 G
D11	S0075354	DIODE,RB551V-30 TE17 G
D12	S0067314	DIODE,RB751V-40/TE17 G
D13	S0022094	DIODE,1SS355
D14	S0071644	DIODE,RB161M-20 G
D15	S0022094	DIODE,1SS355
D16	S0075354	DIODE,RB551V-30 TE17 G
D17	S0086044	ZENER DIO,CDZCT2R6.8B G
D18	S0086044	ZENER DIO,CDZCT2R6.8B G
D19	S0086044	ZENER DIO,CDZCT2R6.8B G
D2	S0083594	LED,SML-E12U8W G
D4	S0081404	DIODE,RB706D-40 G
D5	S0081404	DIODE,RB706D-40 G
D6	S0067314	DIODE,RB751V-40/TE17 G
D8	S0022094	DIODE,1SS355
D9	S0071644	DIODE,RB161M-20 G
F1	E0165754	@FUSE,ERBSE2R00U HF
J1	E0174120	CONNECTOR,2199SB40G6122 G
J2	E0143793	JACK,LGY3009-0200F G
J3	E0166204	JACK,LGY2109-1001F G
L1	E0148584	COIL,10UH M LQM21F-70 G
L10	E0126164	BEAD COIL,BLM18PG471SN1D G
L2	E0158384	BEAD COIL,MMZ1608B601C G
L3	E0158384	BEAD COIL,MMZ1608B601C G
L4	E0158384	BEAD COIL,MMZ1608B601C G
L5	E0158384	BEAD COIL,MMZ1608B601C G
L9	E0124004	COIL,CDRH5D28-220 22UH G
Q10	S0065074	TRANSISTOR,DTC124EUA TP G
Q12	S0041574	TRANSISTOR,DTA124EUA G
Q13	S0065074	TRANSISTOR,DTC124EUA TP G
Q14	S0065074	TRANSISTOR,DTC124EUA TP G
Q16	S0090284	FET,RW1A025ZPT2R G
Q17	S0085924	FET,RUM002N02 T2L G
Q3	S0082684	TRANSISTOR,DTC143ZETL G
Q4	S0066984	TRANSISTOR,2SA1037AK TP G
Q5	S0066984	TRANSISTOR,2SA1037AK TP G
Q6	S0042944	TRANSISTOR,DTC143TUA T106
Q8	S0085694	FET,RW1A020ZP T2R G
S1	E00683600B	SW,TSW-6A-2-16-T50
S10	E0176074	SW,SKRWAHE030 G
S11	E0144730	SW,SSSS213100 G
S12	E00683600B	SW,TSW-6A-2-16-T50
S2	E0176074	SW,SKRWAHE030 G
S3	E0176074	SW,SKRWAHE030 G
S4	E00683600B	SW,TSW-6A-2-16-T50

GATHER PCBA,PANEL 07MK2 G

REF.NO.	PARTS NO.	DESCRIPTION
S5	E00683600B	SW,TSW-6A-2-16-T50
S6	E00683600B	SW,TSW-6A-2-16-T50
S7	E0176074	SW,SKRWAHE030 G
S8	E0176074	SW,SKRWAHE030 G
S9	E00683600B	SW,TSW-6A-2-16-T50
U11	S0075293	IC,R1173H331D-T1-F G
U13	S0080024	IC,BD4944FVE-TR G
U15	S0079934	IC,BU4918F-TR G
U19	S0080104	IC,TPS61020DRCR G
U2	E01743300A	LCD,SMMC12864-DQ-00-SPC G
U3	S0065384	IC,SN74LV165APWR G
U4	S0088614	IC,SN74LVC1G29DCUR G
U5	S0053294	IC,SN74LVC1G125DCKR
U6	S0085654	IC,S-1132B25-I6T2G G
U7	S0089123	IC,CS42L52-CNZR G
U9	S0075164	IC,S-35390A-I8T1G G
X1	E0143374	XTAL,SSP-T7-F 32.768K 7P G
ZD4	S0074914	ZENER DIO,RSA6.1U5 T108 G
	(E95425400A) PCB ASSY,SENS DR07MK2 G	
	M03325400A	SHEET,HM 6*6 G
P101	E01768200A	WIRE,SENS_P101_Y 07MK2 G
P102	E01768300A	WIRE,SENS_P102_B 07MK2 G
S101	E0166274	SW,MPU12580MLB1 G

REF.NO.	PARTS NO.	DESCRIPTION
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9. Included Accessories

付属品

Included Accessories

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	D01145001A	OWNERS MNL,DR07MK2 J G [J]	
	D01145020A	OWNERS MNL,DR07MK2 E G [Except J]	
	D01145080A	OWNERS MNL,DR07MK2 G G [E]	
	D01145081A	OWNERS MNL,DR07MK2 F G [E]	
	D01145082A	OWNERS MNL,DR07MK2 I G [E]	
	D01145083A	OWNERS MNL,DR07MK2 S G [E]	
	T0018100	MICROSD,SP002GST000UMPA G	
	E0174680	USB CABLE,CA3096080A37 G	
	E0174070	BAT,LR6(GD)CH G	

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with * require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in this manual.
- △ Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.

- Parts of [] mark can be used only with the version designated.
 [J] : JAPAN [US/C] : U.S.A./CANADA [K] : KOREA [E] : EUROPE
 [UK] : U.K. [JEX] : JAPAN & ASIA [A] : AUSTRALIA [T] : TAIWAN
 [CH] : CHINA [ETC] : U.S.A./CANADA/South America

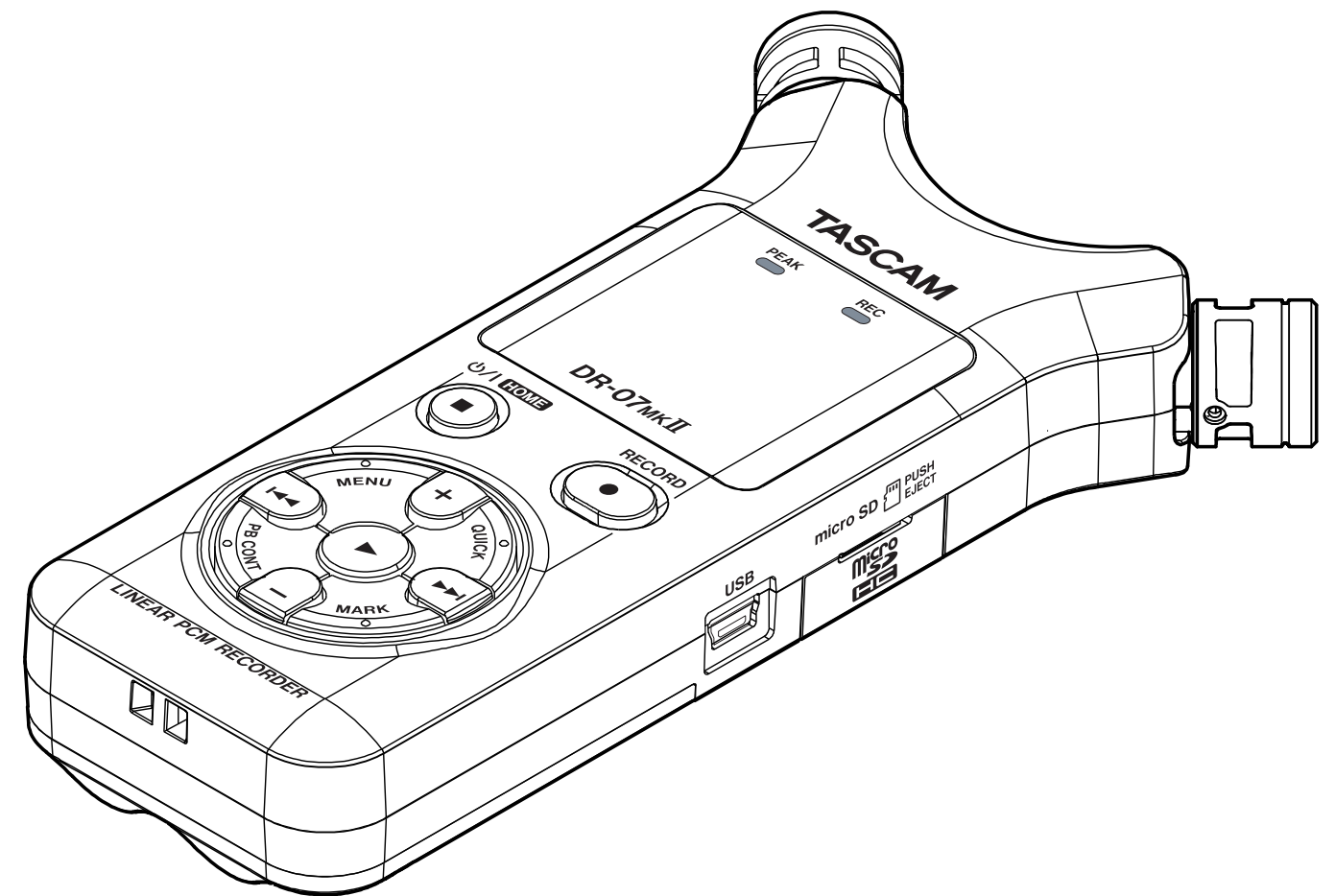
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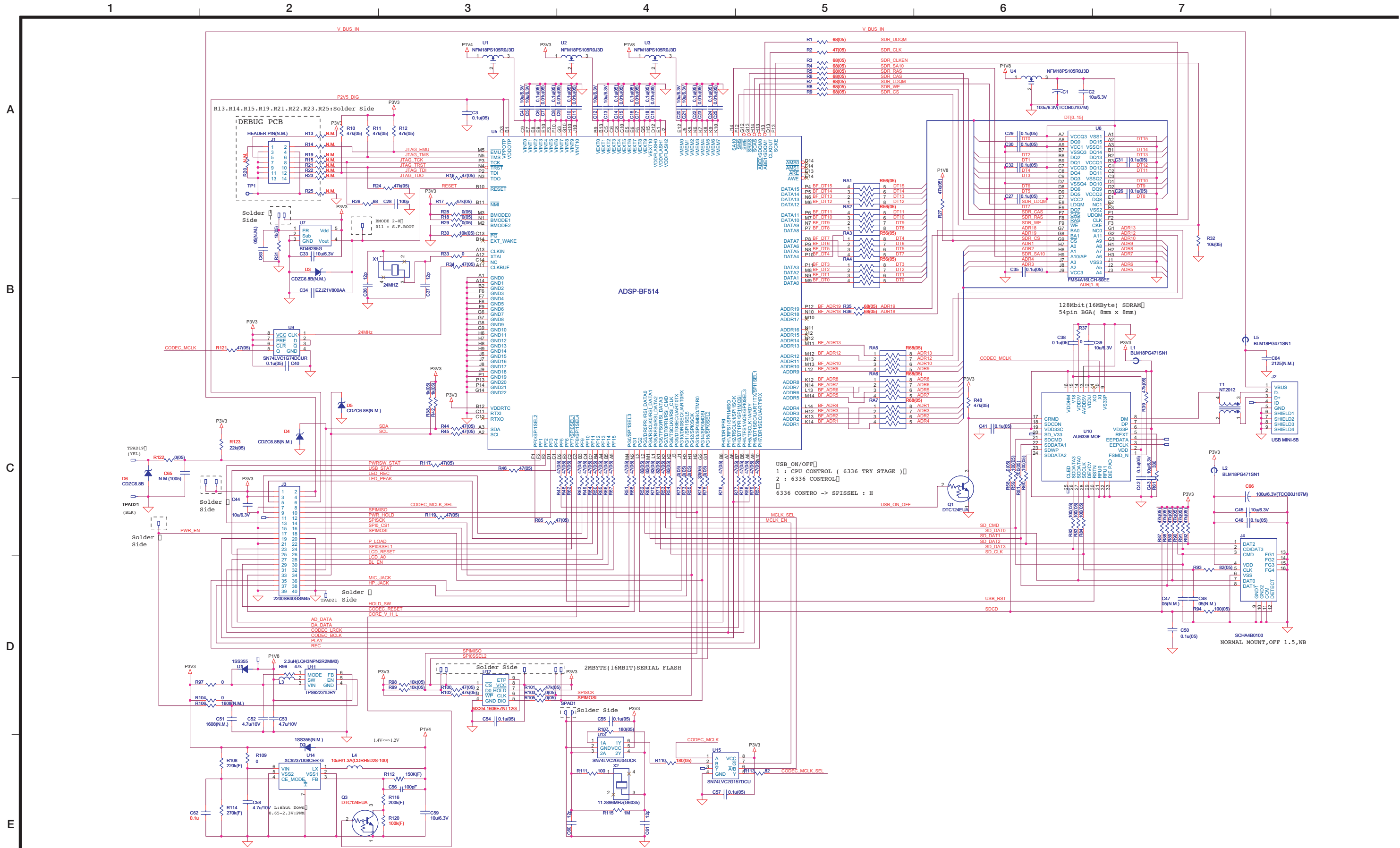
- プリント基板図は部品面を示しています。
- *印の部品は納期が若干かかります。
あらかじめご了承ください。
- 分解図に部番のない部品および品番のない部品は供給できません。
- 標準の抵抗、コンデンサーは省略してあります。
回路図を参照してください。
- △印は安全重要部品です。
交換する時は必ず指定の部品を使用してください。

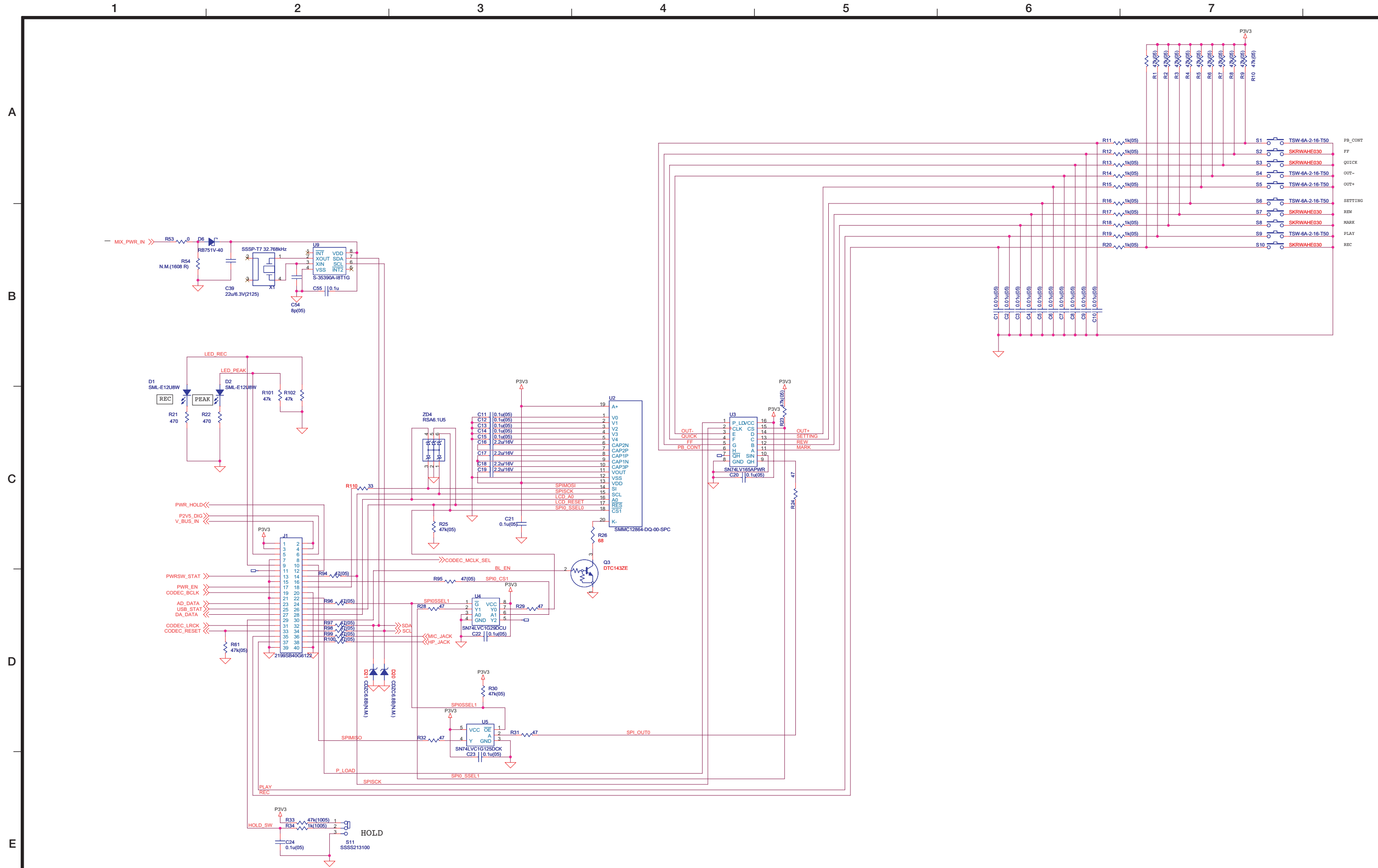
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 [CH] : CHINA [ETC] : U.S.A./CANADA/South America

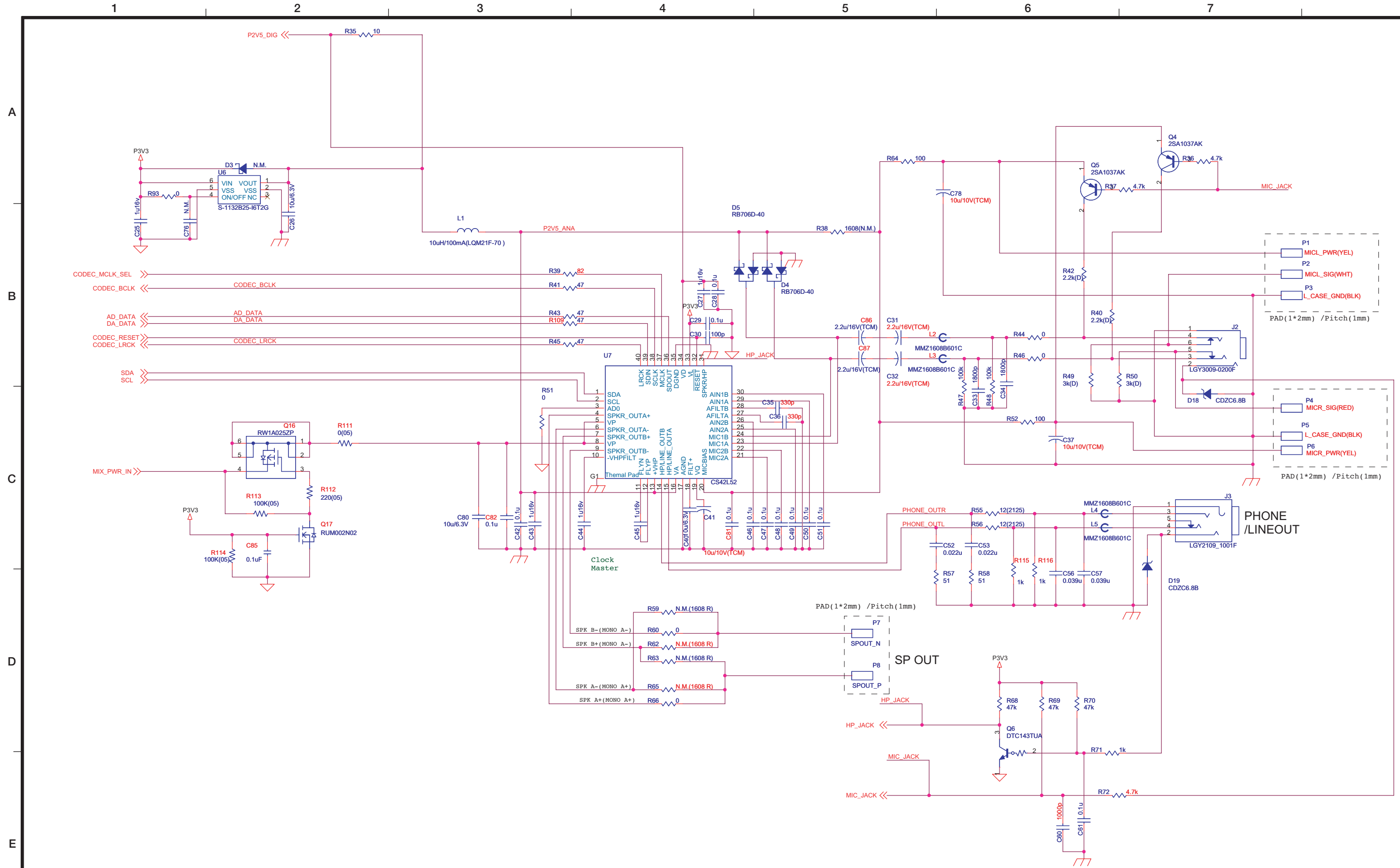
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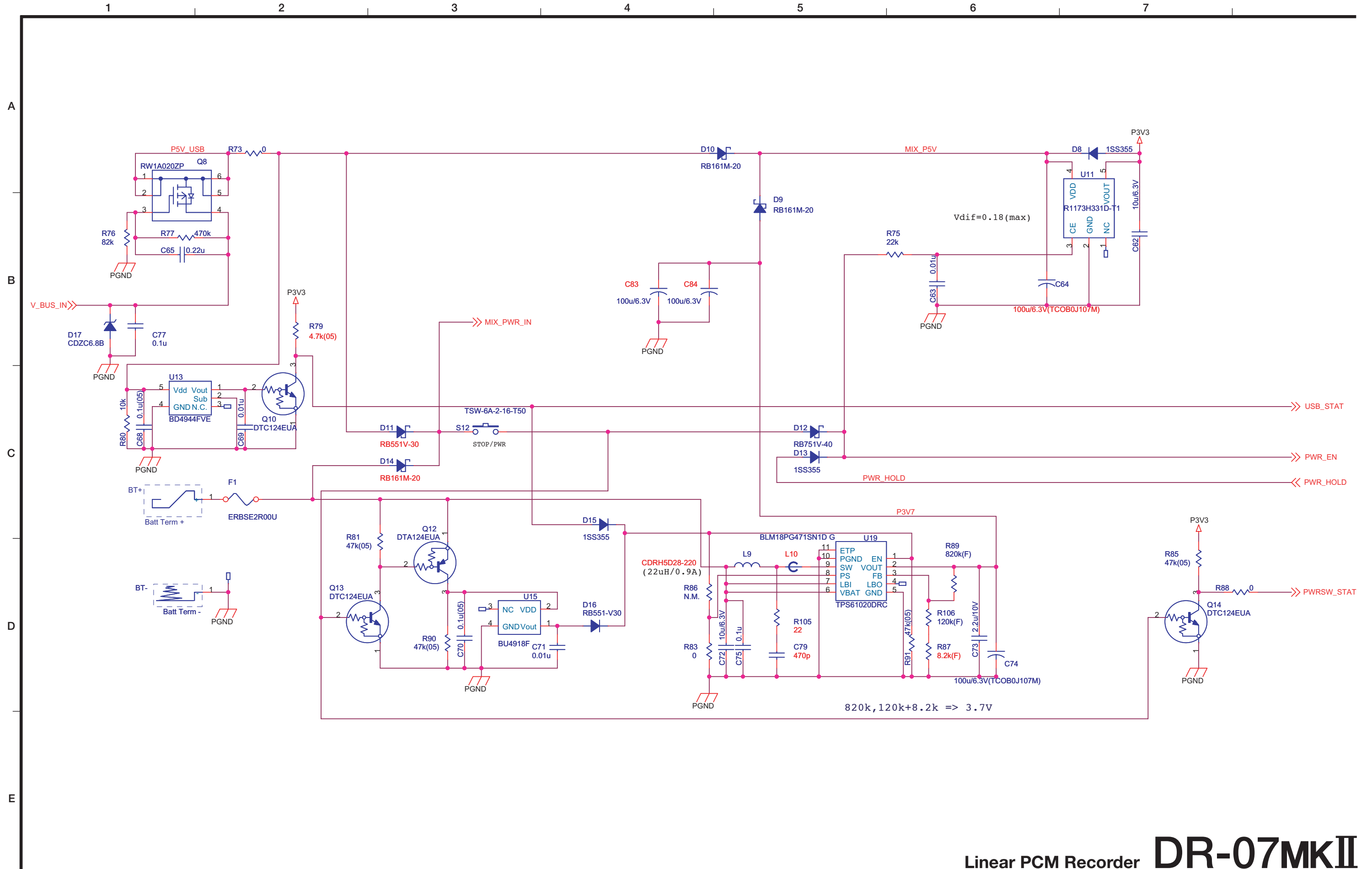
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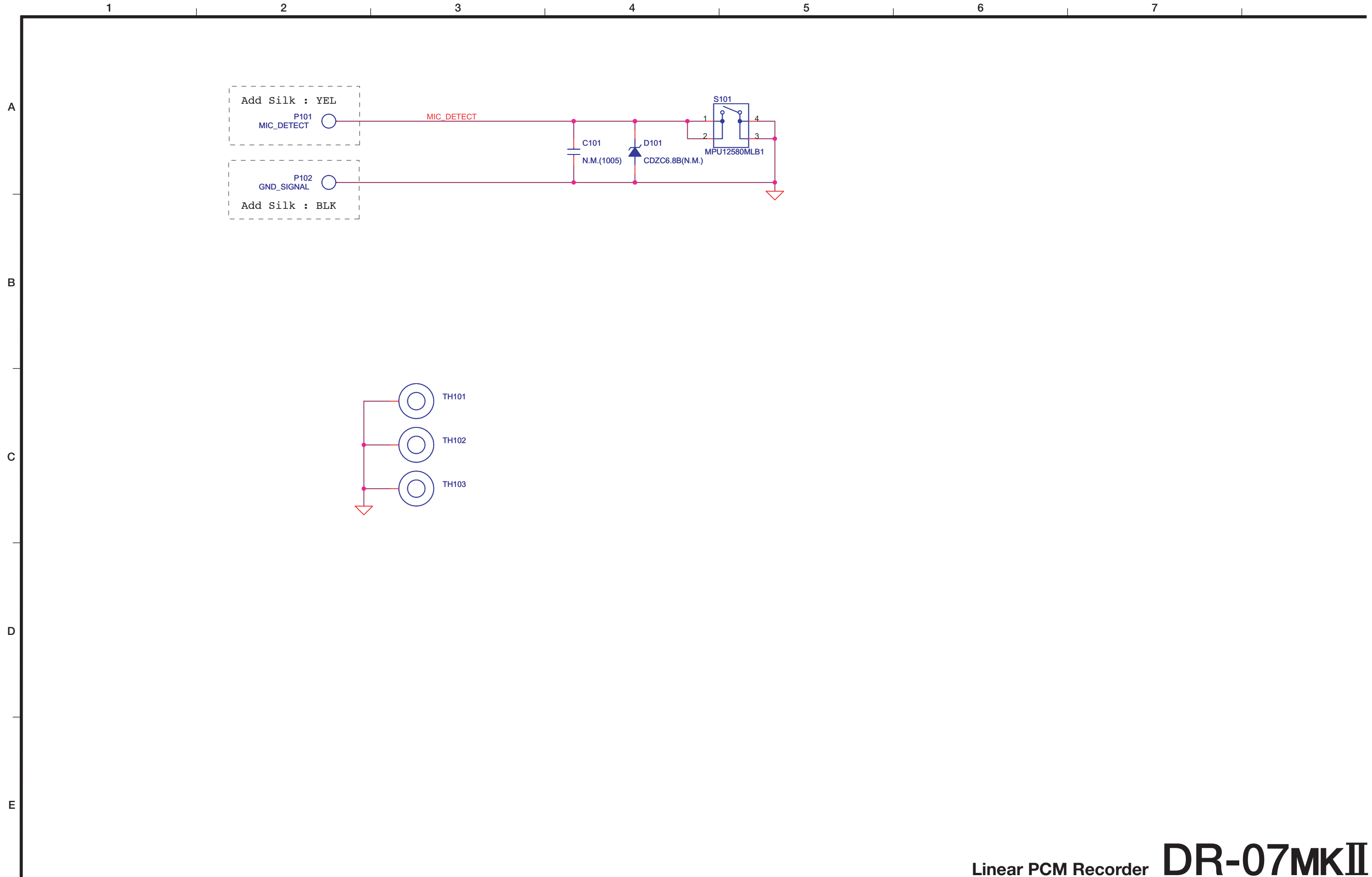












Low-power, Stereo CODEC w/ Headphone & Speaker Amps

Stereo CODEC

- ◆ High Performance Stereo ADC & DAC
 - 99 dB (ADC), 98 dB (DAC) Dyn. Range (A-wtd)
 - -88 dB THD+N
- ◆ Flexible Stereo Analog Input Architecture
 - 4:1 Analog Input MUX
 - Analog Input Mixing
 - Analog Passthrough with Volume Control
 - Analog Programmable Gain Amplifier (PGA)
- ◆ Programmable Automatic Level Control (ALC)
 - Noise Gate for Noise Suppression
 - Programmable Threshold & Attack/Release Rates
- ◆ Dual MIC Inputs
 - Differential or Single-ended
 - +16 dB to +32 dB w/ 1dB step MIC Pre-Amplifiers
 - Programmable, Low-noise MIC Bias Levels
- ◆ Digital Signal Processing Engine
 - Bass & Treble Tone Control, De-emphasis
 - Master Vol. and Independent PCM SDIN + ADC SDOOUT Mix Volume Control
 - Soft-ramp & Zero-Cross Transitions
 - Programmable Peak-detect and Limiter
 - Beep Generator w/Full Tone Control

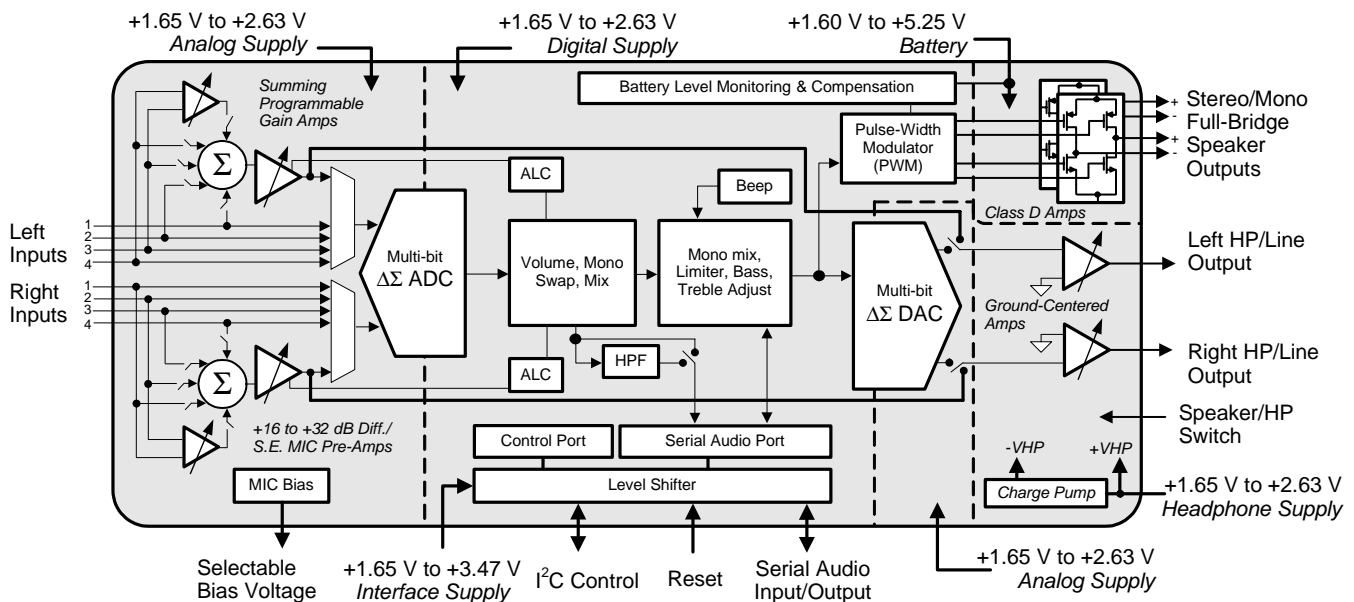
Class D Stereo/Mono Speaker Amplifier

- ◆ No External Filter Required
- ◆ High-power Stereo Output at 10% THD+N
 - 2 x 1.00 W into 8 Ω @ 5.0 V
 - 2 x 550 mW into 8 Ω @ 3.7 V
 - 2 x 230 mW into 8 Ω @ 2.5 V
- ◆ High-power Mono Output at 10% THD+N
 - 1 x 1.90 W into 4 Ω @ 5.0 V
 - 1 x 1.00 W into 4 Ω @ 3.7 V
 - 1 x 350 mW into 4 Ω @ 2.5 V
- ◆ Direct Battery-powered Operation
 - Battery Level Monitoring & Compensation
- ◆ 81% Efficiency at 800 mW
- ◆ Phase-aligned PWM Output Reduces Idle Channel Current
- ◆ Spread Spectrum Modulation
- ◆ Low Quiescent Current

Stereo Headphone Amplifier

- ◆ Ground-centered Outputs
 - No DC-Blocking Capacitors Required
 - Integrated Negative Voltage Regulator
- ◆ High-power Output at -75 dB THD+N
 - 2 x 23 mW Into 16 Ω @ 1.8 V
 - 2 x 44 mW Into 16 Ω @ 2.5 V

(Features continued on [page 2](#))



System Features

- ◆ 12, 24, and 27 MHz Master Clock Support in Addition to Typical Audio Clock Rates
- ◆ High-performance 24-bit Converters
 - Multi-bit Delta-Sigma Architecture
 - Very Low 64Fs Oversampling Clock Reduces Power Consumption
- ◆ Low-power Operation
 - Stereo Analog Passthrough: 10 mW @ 1.8 V
 - Stereo Playback: 14 mW @ 1.8 V
 - Stereo Rec. and Playback: 23 mW @ 1.8 V
- ◆ Variable Power Supplies
 - 1.8 V to 2.5 V Digital & Analog
 - 1.6 V to 5 V Class D Amplifier
 - 1.8 V to 2.5 V Headphone Amplifier
 - 1.8 V to 3.3 V Interface Logic
- ◆ Power-down Management
 - ADC, DAC, CODEC, MIC Pre-Amplifier, PGA, Headphone Amplifier, Speaker Amplifier
- ◆ Analog & Digital Routing/Mixes:
 - Line/Headphone Out = Analog In (ADC Bypassed)
 - Line/Headphone/Speaker Out = ADC + Digital In
 - Digital Out = ADC + Digital In
 - Internal Digital Loopback
 - Mono Mixes
- ◆ Flexible Clocking Options
 - Master or Slave Operation
 - High-impedance Digital Output Option (for easy MUXing between CODEC & other data sources)
 - Quarter-speed Mode - (i.e. allows 8 kHz Fs while maintaining a flat noise floor up to 16 kHz)
 - 4 kHz to 96 kHz Sample Rates
- ◆ I²C[®] Control Port Operation
- ◆ Headphone/Speaker Detection Input
- ◆ Pop and Click Suppression

Applications

- ◆ Digital Voice Recorders, Digital Cameras, & Camcorders
- ◆ PDA's
- ◆ Personal Media Players
- ◆ Portable Game Consoles

General Description

The CS42L52 is a highly integrated, low-power stereo CODEC with headphone and Class D speaker amplifiers. The CS42L52 offers many features suitable for low-power, portable system applications.

The **ADC input path** allows independent channel control of a number of features. Input summing amplifiers mix and select line-level and/or microphone-level inputs for each channel. The microphone input path includes a selectable programmable-gain pre-amplifier stage and a low-noise MIC bias voltage supply. A PGA is available for line or microphone inputs and provides analog gain with soft-ramp and zero-cross transitions. The ADC also features a digital volume control with soft ramp transitions. A programmable ALC and Noise Gate monitor the input signals and adjust the volume levels appropriately. To conserve power, the ADC may be bypassed while still allowing full analog volume control.

The **DAC output path** includes a digital signal processing engine with various fixed-function controls. Tone Control provides bass and treble adjustment of four selectable corner frequencies. The Digital Mixer provides independent volume control for both the ADC output and PCM input signal paths, as well as a master volume control. Digital Volume controls may be configured to change on soft-ramp transitions while the analog controls can be configured to occur on every zero crossing. The DAC also includes de-emphasis, limiting functions and a BEEP generator, delivering tones selectable across a range of two full octaves.

The **stereo headphone amplifier** is powered from a separate positive supply and the integrated **charge pump** provides a negative supply. This allows a ground-centered, analog output with a wide signal swing and eliminates external DC-blocking capacitors.

The **Class D stereo speaker amplifier** does not require an external filter and provides the high-efficiency amplification required by power-sensitive portable applications. The speaker amplifier may be powered directly from a battery while the internal DC supply monitoring and compensation provides a constant gain level as the battery's voltage decays.

In addition to its many features, the CS42L52 operates from a low-voltage analog and digital core making it ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS42L52 is available in a 40-pin QFN package in both Commercial (-40 to +85 °C) and Automotive (-40 to +105 °C) grades. The CS42L52 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "[Ordering Information](#)" on [page 81](#) for complete ordering information.

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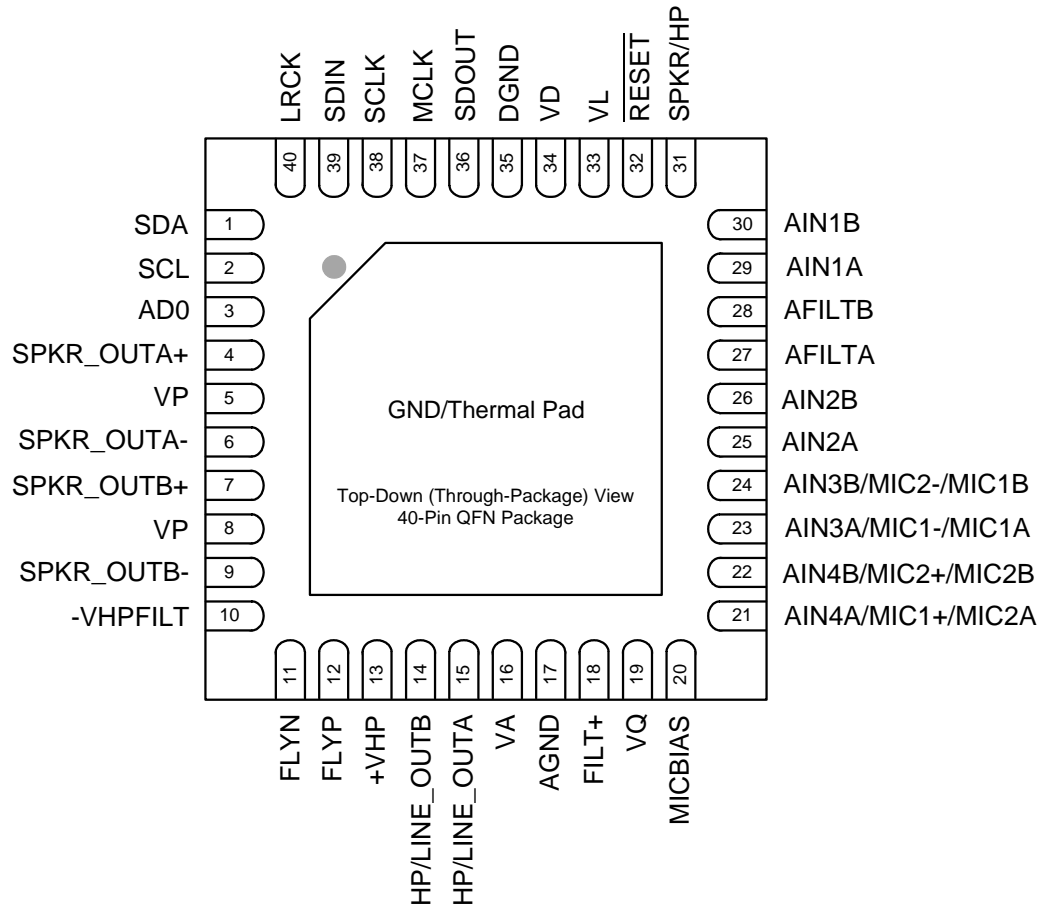
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1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDA	1	Serial Control Data (<i>Input/Output</i>) - SDA is a data I/O in I ² C Mode.
SCL	2	Serial Control Port Clock (<i>Input</i>) - Serial clock for the serial control port.
AD0	3	Address Bit 0 (<i>Input</i>) - Chip address bit 0.
SPKR_OUTA+	4	PWM Speaker Output (<i>Output</i>) - Full-bridge amplified PWM speaker outputs.
SPKR_OUTA-	6	
SPKR_OUTB+	7	
SPKR_OUTB-	9	
VP	5	Power for PWM Drivers (<i>Input</i>) - Power supply for the PWM output driver stages.
-VHPFILT	8	
-VHPFILT	10	Inverting Charge Pump Filter Connection (<i>Output</i>) - Power supply from the inverting charge pump that provides the negative rail for the headphone/line amplifiers.
FLYN	11	Charge Pump Cap Negative Node (<i>Output</i>) - Negative node for the inverting charge pump's flying capacitor.
FLYP	12	Charge Pump Cap Positive Node (<i>Output</i>) - Positive node for the inverting charge pump's flying capacitor.
+VHP	13	Positive Analog Power for Headphone (<i>Input</i>) - Positive voltage rail and power for the internal headphone amplifiers and inverting charge pump.
HP/LINE_OUTB, A	14,15	Headphone/Line Audio Output (<i>Output</i>) - Stereo headphone or line level analog outputs.
VA	16	Analog Power (<i>Input</i>) - Positive power for the internal analog section.

AGND	17	Analog Ground (<i>Input</i>) - Ground reference for the internal analog section.
FILT+	18	Positive Voltage Reference (<i>Output</i>) - Positive reference voltage for the internal sampling circuits.
VQ	19	Quiescent Voltage (<i>Output</i>) - Filter connection for the internal quiescent voltage.
MICBIAS	20	Microphone Bias (<i>Output</i>) - Low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AIN4A,B AIN3A,B	21,22 23,24	Line-Level Analog Inputs (<i>Input</i>) - Single-ended stereo line-level analog inputs.
MIC1+,- MIC2+,-	21,23 22,24	Differential Microphone Inputs (<i>Input</i>) - Differential stereo microphone inputs.
MIC2A,B MIC1A,B	21,22 23,24	Single-Ended Microphone Inputs (<i>Input</i>) - Single-ended stereo microphone inputs.
AIN2A,B AIN1A,B	25,26 29,30	Line-Level Analog Inputs (<i>Input</i>) - Single-ended stereo line-level analog inputs.
AFILTA,B	27,28	Anti-alias Filter Connection (<i>Output</i>) - Anti-alias filter connection for the ADC inputs.
SPKR/HP	31	Speaker/Headphone Switch (<i>Input</i>) - Powers down the left and/or right channel of the speaker and/or headphone outputs.
RESET	32	Reset (<i>Input</i>) - The device enters a low power mode when this pin is driven low.
VL	33	Digital Interface Power (<i>Input</i>) - Determines the required signal level for the serial audio interface and host control port.
VD	34	Digital Power (<i>Input</i>) - Positive power for the internal digital section.
DGND	35	Digital Ground (<i>Input</i>) - Ground reference for the internal digital section.
SDOUT	36	Serial Audio Data Output (<i>Output</i>) - Output for two's complement serial audio data.
MCLK	37	Master Clock (<i>Input</i>) - Clock source for the delta-sigma modulators.
SCLK	38	Serial Clock (<i>Input/Output</i>) - Serial clock for the serial audio interface.
SDIN	39	Serial Audio Data Input (<i>Input</i>) - Input for two's complement serial audio data.
LRCK	40	Left Right Clock (<i>Input/Output</i>) - Determines which channel, Left or Right, is currently active on the serial audio data line.
GND/Thermal Pad	-	Ground reference for PWM power FETs and charge pump; thermal relief pad for optimized heat dissipation.

1.1 I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name	I/O	Internal Connections	Driver	Receiver
VL	RESET	Input	-	-	1.65 V - 3.47 V, with Hysteresis
	SCL	Input	-	-	1.65 V - 3.47 V, with Hysteresis
	SDA	Input/ Output	-	1.65 V - 3.47 V, CMOS/Open Drain	1.65 V - 3.47 V, with Hysteresis
	MCLK	Input	-	-	1.65 V - 3.47 V
	LRCK	Input/ Output	Weak Pullup (~1 MΩ)	1.65 V - 3.47 V, CMOS	1.65 V - 3.47 V
	SCLK	Input/ Output	Weak Pullup (~1 MΩ)	1.65 V - 3.47 V, CMOS	1.65 V - 3.47 V
	SDOUT	Output	Weak Pullup (~1 MΩ)	1.65 V - 3.47 V, CMOS	
	SDIN	Input	-	-	1.65 V - 3.47 V
VA	SPKR/HP	Input	-	-	1.65 V - 2.63 V
VP	SPKR_OUTA+	Output	-	1.6 V - 5.25 V Power MOSFET	-
	SPKR_OUTA-	Output	-	1.6 V - 5.25 V Power MOSFET	-
	SPKR_OUTB+	Output	-	1.6 V - 5.25 V Power MOSFET	-
	SPKR_OUTB-	Output	-	1.6 V - 5.25 V Power MOSFET	-

2. TYPICAL CONNECTION DIAGRAM

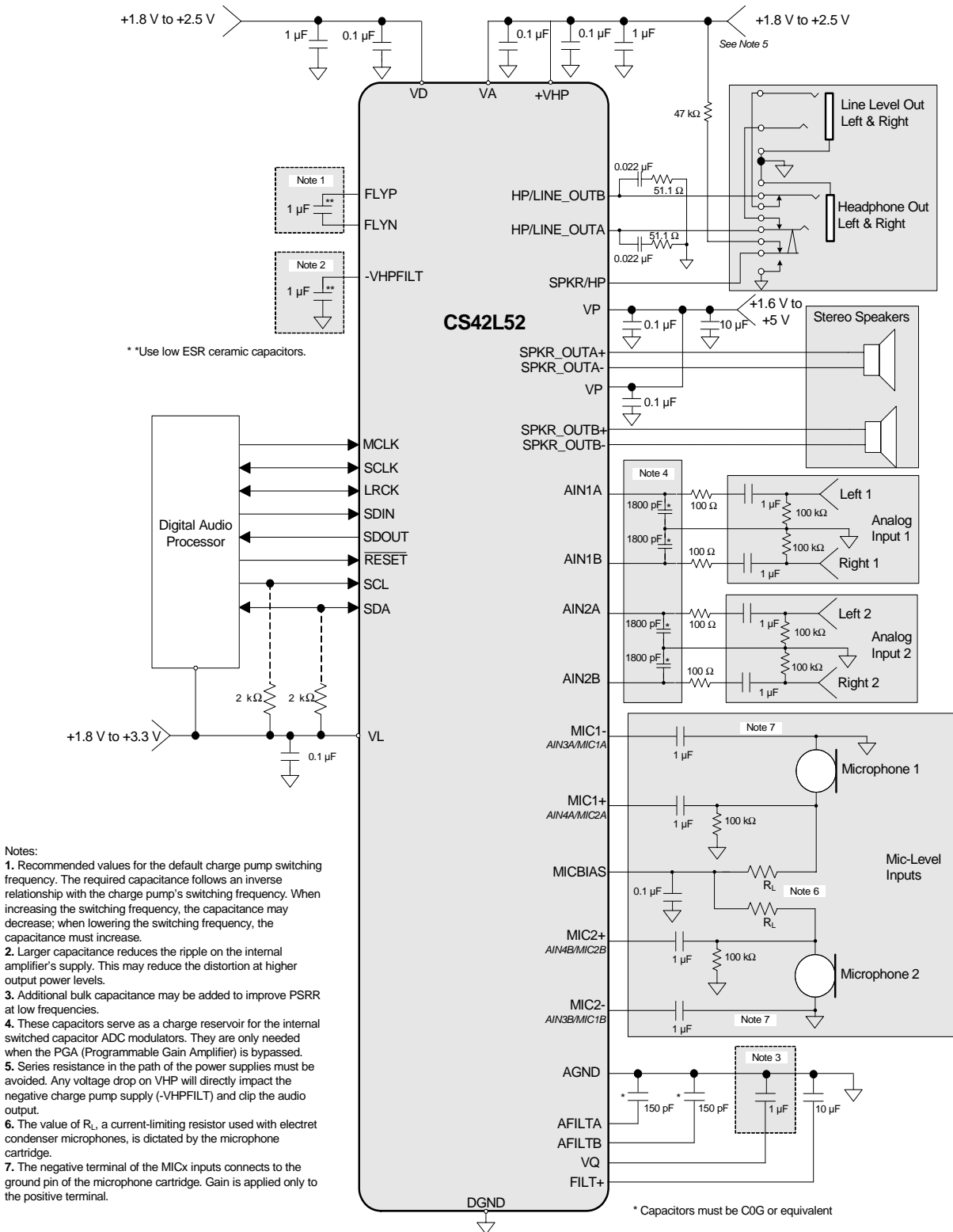


Figure 1. Typical Connection Diagram

3. CHARACTERISTIC AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND=DGND=0 V, All voltages with respect to ground.

Parameters	Symbol	Min	Max	Units	
DC Power Supply					
Analog	VA	1.65	2.63	V	
Headphone Amplifier	+VHP	1.65	2.63	V	
Speaker Amplifier	VP	1.60	5.25	V	
Digital	VD	1.65	2.63	V	
Serial/Control Port Interface	VL	1.65	3.47	V	
Ambient Temperature	T _A	Commercial - CNZ	-40	+85	°C
		Automotive - DNZ	-40	+105	°C

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V; All voltages with respect to ground.

Parameters	Symbol	Min	Max	Units	
DC Power Supply	Analog	VA, VHP	-0.3	3.0	V
	Speaker	VP	-0.3	6.0	V
	Digital	VD	-0.3	3.0	V
	Serial/Control Port Interface	VL	-0.3	4.0	V
Input Current	(Note 1)	I _{in}	-	±10	mA
External Voltage Applied to Analog Input	(Note 2)	V _{IN}	AGND-0.3	VA+0.3	V
External Voltage Applied to Analog Output		V _{IN}	-VHP - 0.3	+VHP + 0.3	V
External Voltage Applied to Digital Input	(Note 2)	V _{IND}	-0.3	VL+ 0.3	V
Ambient Operating Temperature (power applied)		T _A	-50	+115	°C
Storage Temperature		T _{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
2. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL - CNZ)

Test Conditions (unless otherwise specified): Input sine wave (relative to digital full scale): 1 kHz through passive input filter; All Supplies = VA; T_A = +25°C; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; "Required Initialization Settings" on page 37 written on power up.

Parameters		VA = 2.5V			VA = 1.8V			Unit	
		Min	Typ	Max	Min	Typ	Max		
Analog In to ADC (PGA bypassed)									
Dynamic Range	A-weighted	93	99	-	90	96	-	dB	
	unweighted	90	96	-	87	93	-	dB	
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-80	-	-84	-78	dB	
	-20 dBFS	-	-76	-	-	-73	-	dB	
	-60 dBFS	-	-36	-30	-	-33	-27	dB	
Analog In to PGA to ADC									
Dynamic Range	PGA Setting: 0 dB	A-weighted	92	96	-	89	95	-	dB
		unweighted	89	93	-	86	92	-	dB
PGA Setting: +12 dB	A-weighted	85	91	-	82	88	-	dB	
	unweighted	82	88	-	79	85	-	dB	
Total Harmonic Distortion + Noise	PGA Setting: 0 dB	-1 dBFS	-	-88	-82	-	-86	-80	dB
		-60 dBFS	-	-33	-27	-	-32	-26	dB
	PGA Setting: +12 dB	-1 dBFS	-	-85	-79	-	-83	-77	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC									
Dynamic Range	PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
		unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise	PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC									
Dynamic Range	PGA Setting: 0 dB	A-weighted	-	76	-	-	74	-	dB
		unweighted	-	73	-	-	71	-	dB
Total Harmonic Distortion + Noise	PGA Setting: 0 dB	-2 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics									
DC Accuracy									
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB	
Gain Drift		-	±100	-	-	±100	-	ppm/°C	
Offset Error		SDOUT Code with HPF On		-	352	-	-	352	LSB
Input									
Interchannel Isolation		-	90	-	-	90	-	dB	
HP Amp to Analog Input Isolation (Note 3)	R _L = 10 kΩ	-	100	-	-	100	-	dB	
	R _L = 16 Ω	-	70	-	-	70	-	dB	
Speaker Amp to Analog Input Isolation		-	60	-	-	60	-	dB	
Full-scale Input Voltage	ADC	0.73•VA	0.769•VA	0.83•VA	0.73•VA	0.769•VA	0.83•VA	V _{pp}	
	PGA (0 dB)	0.73•VA	0.770•VA	0.83•VA	0.73•VA	0.770•VA	0.83•VA	V _{pp}	
	PGA (+12 dB)		0.194•VA			0.194•VA		V _{pp}	
	MIC (+16 dB)		0.115•VA			0.115•VA		V _{pp}	
	MIC (+32 dB)		0.019•VA			0.019•VA		V _{pp}	
Input Impedance (Note 4)	ADC	-	20	-	-	20	-	kΩ	
	PGA	-	39	-	-	39	-	kΩ	
	MIC	-	50	-	-	50	-	kΩ	

3. Measured with DAC delivering full-scale output into specified load.

4. Measured between analog input and AGND.

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE - DNZ) Test Conditions (unless otherwise specified): Input sine wave (relative to full-scale): 1 kHz through passive input filter; All Supplies = VA; $T_A = -40$ to $+85^\circ\text{C}$; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; “Required Initialization Settings” on page 37 written on power up.

Parameters	VA = 2.37 - 2.63 V			VA = 1.65 - 1.89 V			Unit	
	Min	Typ	Max	Min	Typ	Max		
Analog In to ADC								
Dynamic Range	A-weighted	91	99	-	88	96	-	dB
	unweighted	88	96	-	85	93	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-78	-	-84	-76	dB
	-20 dBFS	-	-76	-	-	-73	-	dB
	-60 dBFS	-	-36	-28	-	-33	-25	dB
Analog In to PGA to ADC								
Dynamic Range PGA Setting: 0 dB	A-weighted	90	96	-	87	95	-	dB
	unweighted	87	93	-	84	92	-	dB
PGA Setting: +12 dB	A-weighted	83	91	-	80	88	-	dB
	unweighted	80	88	-	77	85	-	dB
Total Harmonic Distortion + Noise PGA Setting: 0 dB	-1 dBFS	-	-88	-80	-	-86	-78	dB
	-60 dBFS	-	-33	-25	-	-32	-24	dB
	PGA Setting: +12 dB	-1 dBFS	-	-85	-77	-	-83	-75
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC								
Dynamic Range PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
	unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC								
Dynamic Range PGA Setting: 0 dB	A-weighted	-	76	-	-	74	-	dB
	unweighted	-	73	-	-	71	-	dB
Total Harmonic Distortion + Noise PGA Setting: 0 dB	-2 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	± 100	-	-	± 100	-	ppm/ $^\circ\text{C}$
Offset Error	SDOUT Code with HPF On	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation		-	90	-	-	90	-	dB
HP Amp to Analog Input Isolation (Note 3)	$R_L = 10\text{ k}\Omega$	-	100	-	-	100	-	dB
	$R_L = 16\ \Omega$	-	70	-	-	70	-	dB
Speaker Amp to Analog Input Isolation		-	60	-	-	60	-	dB
Full-scale Input Voltage	ADC	$0.73 \cdot V_A$	$0.769 \cdot V_A$	$0.83 \cdot V_A$	$0.73 \cdot V_A$	$0.769 \cdot V_A$	$0.83 \cdot V_A$	V _{pp}
	PGA (0 dB)	$0.73 \cdot V_A$	$0.770 \cdot V_A$	$0.83 \cdot V_A$	$0.73 \cdot V_A$	$0.770 \cdot V_A$	$0.83 \cdot V_A$	V _{pp}
	PGA (+12 dB)	-	$0.194 \cdot V_A$	-	-	$0.194 \cdot V_A$	-	V _{pp}
	MIC (+16 dB)	-	$0.115 \cdot V_A$	-	-	$0.115 \cdot V_A$	-	V _{pp}
	MIC (+32 dB)	-	$0.019 \cdot V_A$	-	-	$0.019 \cdot V_A$	-	V _{pp}
Input Impedance (Note 4)	ADC	18	-	-	18	-	-	k Ω
	PGA	40	-	-	40	-	-	k Ω
	MIC	50	-	-	50	-	-	k Ω

ADC DIGITAL FILTER CHARACTERISTICS

Parameters (Note 5)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4948	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Group Delay		-	7.6/Fs	-	s
High-Pass Filter Characteristics (48 kHz Fs)					
Frequency Response	-3.0 dB	-	3.6	-	Hz
	-0.13 dB	-	24.2	-	Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	$10^5/Fs$	0	s

- Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 26 to 29 on page 78) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs. HPF parameters are for Fs = 48 kHz.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL - CNZ)

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; All Supplies = VA; T_A = +25°C; Sample Frequency = 48 kHz; Measurement bandwidth is 20 Hz to 20 kHz; Test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 2); Test load R_L = 16 Ω, C_L = 10 pF (see Figure 2) for the headphone output; HP_GAIN[2:0] = 011; “Required Initialization Settings” on page 37 written on power up.

Parameters (Note 6)		VA = 2.5 V			VA = 1.8 V			Unit
		Min	Typ	Max	Min	Typ	Max	
R_L = 10 kΩ								
Dynamic Range								
18- to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18- to 24-Bit	0 dB	-	-86	-80	-	-88	-82	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-29	-	-32	-26	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18- to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18- to 24-Bit	0 dB	-	-75	-69	-	-75	-69	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-29	-	-32	-26	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 7)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)	-	0.6047	-	-	0.6047	-	
Full-scale Output Voltage (2•G•MI•VA) (Note 7)		Refer to Table “Line Output Voltage Level Characteristics” on page 20						V _{pp}
Full-scale Output Power (Note 7)		Refer to Table “Headphone Output Power Characteristics” on page 19						
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Speaker Amp to HP Amp Isolation		-	80	-	-	80	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC Load Resistance (R _L)	(Note 8)	16	-	-	16	-	-	Ω
Load Capacitance (C _L)	(Note 8)	-	-	150	-	-	150	pF

- One-half LSB of triangular PDF dither is added to data.
- Full-scale output voltage and power is determined by the gain setting, G, in register “Headphone Analog Gain” on page 51. High gain settings at certain VA and VHP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output, as shown in Figures 22 - 25 on page 75.

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; All Supplies = VA; T_A = -40 to +85°C; Sample Frequency = 48 kHz and 96 kHz; Measurement bandwidth is 20 Hz to 20 kHz; Test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 2); Test load R_L = 16 Ω, C_L = 10 pF (see Figure 2) for the headphone output; HPGAIN[2:0] = 011. "Required Initialization Settings" on page 37 written on power up.

Parameters (Note 6)		VA = 2.37 - 2.63 V			VA = 1.65 - 1.89 V			Unit
		Min	Typ	Max	Min	Typ	Max	
R_L = 10 kΩ								
Dynamic Range								
18- to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18- to 24-Bit	0 dB	-	-86	-78	-	-88	-80	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-27	-	-32	-24	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18- to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18- to 24-Bit	0 dB	-	-75	-67	-	-75	-67	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-27	-	-32	-24	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 7)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)	-	0.6047	-	-	0.6047	-	
Full-scale Output Voltage (2•G•MI•VA)	(Note 7)	Refer to the table in "Line Output Voltage Level Characteristics" on page 20						V _{pp}
Full-scale Output Power	(Note 7)	Refer to the table in "Headphone Output Power Characteristics" on page 19						
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Speaker Amp to HP Amp Isolation		-	80	-	-	80	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC Load Resistance (R _L)	(Note 8)	16	-	-	16	-	-	Ω
Load Capacitance (C _L)	(Note 8)	-	-	150	-	-	150	pF

8. See Figure 2. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.

ANALOG PASSTHROUGH CHARACTERISTICS

Test Conditions (unless otherwise specified): Input sine wave (relative to full-scale): 1 kHz through passive input filter; PGA and HP/Line Gain = 0 dB; All Supplies = VA; T_A = +25°C; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; ["Required Initialization Settings" on page 37](#) written on power up.

Parameters		VA = 2.5 V			VA = 1.8 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog In to HP/Line Amp (ADC is powered down)								
R_L = 10 kΩ								
Dynamic Range	A-weighted	-	-96	-	-	-94	-	dB
	unweighted	-	-93	-	-	-91	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-70	-	-	-70	-	dB
	-20 dBFS	-	-73	-	-	-71	-	dB
	-60 dBFS	-	-33	-	-	-31	-	dB
Full-scale Input Voltage		-	0.91•VA	-	-	0.91•VA	-	V _{pp}
Full-scale Output Voltage		-	0.84•VA	-	-	0.84•VA	-	V _{pp}
Passband Ripple		-	0/-0.3	-	-	0/-0.3	-	dB
R_L = 16 Ω								
Dynamic Range	A-weighted	-	-96	-	-	-94	-	dB
	unweighted	-	-93	-	-	-91	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-70	-	-	-70	-	dB
	-20 dBFS	-	-73	-	-	-71	-	dB
	-60 dBFS	-	-33	-	-	-31	-	dB
Full-scale Input Voltage		-	0.91•VA	-	-	0.91•VA	-	V _{pp}
Full-scale Output Voltage		-	0.84•VA	-	-	0.84•VA	-	V _{pp}
Output Power		-	32	-	-	17	-	mW
Passband Ripple		-	0/-0.3	-	-	0/-0.3	-	dB

PWM OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full scale 997 Hz signal; MCLK = 12.2880 MHz; Measurement Bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load R_L = 8 Ω for stereo full-bridge, R_L = 4 Ω for mono parallel full-bridge; VD = VL = VA = VHP = 1.8V; PWM Modulation Index of 0.85; PWM Switch Rate = 384 kHz; ["Required Initialization Settings" on page 37](#) written on power up. (Note 9)

Parameters (Note 10)	Symbol	Conditions	Min	Typ	Max	Units
VP = 5.0 V						
Power Output per Channel	P _O					
Stereo Full-Bridge		THD+N < 10%	-	1.00	-	W _{rms}
		THD+N < 1%	-	0.80	-	W _{rms}
Mono Parallel Full-Bridge		THD+N < 10%	-	1.90	-	W _{rms}
		THD+N < 1%	-	1.50	-	W _{rms}
Total Harmonic Distortion + Noise	THD+N					
Stereo Full-Bridge		P _O = 0 dBFS = 0.8W	-	0.52	-	%
Mono Parallel Full-Bridge		P _O = -3 dBFS = 0.75 W	-	0.10	-	%
		P _O = 0 dBFS = 1.5 W	-	0.50	-	%
Dynamic Range	DR					
Stereo Full-Bridge		P _O = -60 dBFS, A-Weighted	-	91	-	dB
		P _O = -60 dBFS, Unweighted	-	88	-	dB
Mono Parallel Full-Bridge		P _O = -60 dBFS, A-Weighted	-	91	-	dB
		P _O = -60 dBFS, Unweighted	-	88	-	dB

Parameters (Note 10)	Symbol	Conditions	Min	Typ	Max	Units
VP = 3.7 V						
Power Output per Channel	PO					
Stereo Full-Bridge		THD+N < 10%	-	0.55	-	W _{rms}
		THD+N < 1%	-	0.45	-	W _{rms}
Mono Parallel Full-Bridge		THD+N < 10%	-	1.00	-	W _{rms}
		THD+N < 1%	-	0.84	-	W _{rms}
Total Harmonic Distortion + Noise	THD+N					
Stereo Full-Bridge		PO = 0 dBFS = 0.43 W	-	0.54	-	%
Mono Parallel Full-Bridge		PO = -3 dBFS = 0.41 W	-	0.09	-	%
		PO = 0 dBFS = 0.81 W	-	0.45	-	%
Dynamic Range	DR					
Stereo Full-Bridge		PO = -60 dBFS, A-Weighted	-	91	-	dB
		PO = -60 dBFS, Unweighted	-	88	-	dB
Mono Parallel Full-Bridge		PO = -60 dBFS, A-Weighted	-	95	-	dB
		PO = -60 dBFS, Unweighted	-	92	-	dB
VP = 2.5 V						
Power Output per Channel	PO					
Stereo Full-Bridge		THD+N < 10%	-	0.23	-	W _{rms}
		THD+N < 1%	-	0.19	-	W _{rms}
Mono Parallel Full-Bridge		THD+N < 10%	-	0.44	-	W _{rms}
		THD+N < 1%	-	0.35	-	W _{rms}
Total Harmonic Distortion + Noise	THD+N					
Stereo Full-Bridge		PO = 0 dBFS = 0.18 W	-	0.50	-	%
Mono Parallel Full-Bridge		PO = -3 dBFS = 0.17 W	-	0.08	-	%
		PO = 0 dBFS = 0.35 W	-	0.43	-	%
Dynamic Range	DR					
Stereo Full-Bridge		PO = -60 dBFS, A-Weighted	-	91	-	dB
		PO = -60 dBFS, Unweighted	-	88	-	dB
Mono Parallel Full-Bridge		PO = -60 dBFS, A-Weighted	-	94	-	dB
		PO = -60 dBFS, Unweighted	-	91	-	dB
MOSFET On Resistance	R _{DSON}	VP = 5.0V, Id = 0.5 A	-	600	-	mΩ
MOSFET On Resistance	R _{DSON}	VP = 3.7V, Id = 0.5 A	-	640	-	mΩ
MOSFET On Resistance	R _{DSON}	VP = 2.5V, Id = 0.5 A	-	760	-	mΩ
Efficiency	η	VP = 5.0 V, PO = 2 x 0.8 W, RL = 8 Ω	-	81	-	%
Output Operating Peak Current	I _{PC}		-	-	1.5	A
VP Input Current During Reset	I _{VP}	RESET, pin 32, is held low	-	0.8	5.0	μA

9. The PWM driver should be used in captive speaker systems only.
10. Optimal PWM performance is achieved when MCLK > 12 MHz.

HEADPHONE OUTPUT POWER CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Test load $R_L = 16 \Omega$, $C_L = 10 \text{ pF}$ (see [Figure 2](#)); “Required Initialization Settings” on [page 37](#) written on power up.

Parameters			VA = 2.5V			VA = 1.8V			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Power Into $R_L = 16 \Omega$									
HP_GAIN[2:0]	Analog Gain (G)	VHP							
000	0.3959	1.8 V	-	14	-	-	7	-	mW_{rms}
		2.5 V	-	14	-	-	7	-	mW_{rms}
001	0.4571	1.8 V	-	19	-	-	10	-	mW_{rms}
		2.5 V	-	19	-	-	10	-	mW_{rms}
010	0.5111	1.8 V	-	23	-	-	12	-	mW_{rms}
		2.5 V	-	23	-	-	12	-	mW_{rms}
011 (default)	0.6047	1.8 V	(Note 11)			-	17	-	mW_{rms}
		2.5 V	-	32	-	-	17	-	mW_{rms}
100	0.7099	1.8 V	(Note 11)			-	23	-	mW_{rms}
		2.5 V	-	44	-	-	23	-	mW_{rms}
101	0.8399	1.8 V	(Note 7, 11) See Figures 22 and 23 on page 74			(Note 7), Figure 22 on page 74		-	mW_{rms}
		2.5 V				-	32	-	mW_{rms}
110	1.0000	1.8 V	(Note 7, 11) See Figures 22 and 23 on page 74					-	mW_{rms}
		2.5 V						-	mW_{rms}
111	1.1430	1.8 V	(Note 7, 11) See Figures 22 and 23 on page 74					-	mW_{rms}
		2.5 V						-	mW_{rms}

11. VHP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the DAC may not achieve the full THD+N performance at full-scale output voltage and power.

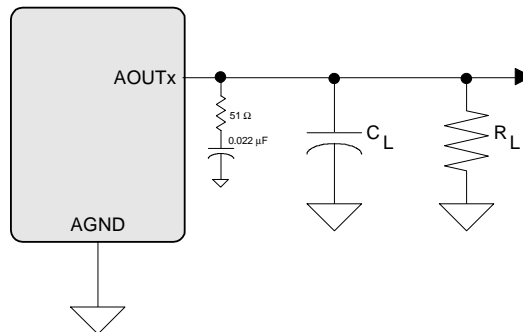


Figure 2. Headphone Output Test Load

LINE OUTPUT VOLTAGE LEVEL CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$ (see [Figure 2](#)); “Required Initialization Settings” on [page 37](#) written on power up.

Parameters			VA = 2.5V			VA = 1.8V			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Voltage Into $R_L = 10\text{ k}\Omega$									
HP_GAIN[2:0]	Analog Gain (G)	VHP							
000	0.3959	1.8 V	-	1.34	-	-	0.97	-	V_{pp}
		2.5 V	-	1.34	-	-	0.97	-	V_{pp}
001	0.4571	1.8 V	-	1.55	-	-	1.12	-	V_{pp}
		2.5 V	-	1.55	-	-	1.12	-	V_{pp}
010	0.5111	1.8 V	-	1.73	-	-	1.25	-	V_{pp}
		2.5 V	-	1.73	-	-	1.25	-	V_{pp}
011 (default)	0.6047	1.8 V	-	2.05	-	1.41	1.48	1.55	V_{pp}
		2.5 V	1.95	2.05	2.15	-	1.48	-	V_{pp}
100	0.7099	1.8 V	-	2.41	-	-	1.73	-	V_{pp}
		2.5 V	-	2.41	-	-	1.73	-	V_{pp}
101	0.8399	1.8 V	-	2.85	-	-	2.05	-	V_{pp}
		2.5 V	-	2.85	-	-	2.05	-	V_{pp}
110	1.0000	1.8 V	-	3.39	-	-	2.44	-	V_{pp}
		2.5 V	-	3.39	-	-	2.44	-	V_{pp}
111	1.1430	1.8 V	(See (Note 11))			-	2.79	-	V_{pp}
		2.5 V	-	3.88	-	-	2.79	-	V_{pp}

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameters (Note 12)	Min	Typ	Max	Unit	
Frequency Response 10 Hz to 20 kHz	-0.01	-	+0.08	dB	
Passband	to -0.05 dB corner	0	-	0.4780	Fs
	to -3 dB corner	0	-	0.4996	Fs
StopBand	0.5465	-	-	Fs	
StopBand Attenuation (Note 13)	50	-	-	dB	
Group Delay	-	9/Fs	-	s	
De-emphasis Error	Fs = 32 kHz	-	-	+1.5/+0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.25	dB
	Fs = 48 kHz	-	-	-0.2/-0.4	dB

12. Response is clock dependent and will scale with Fs. Note that the response plots ([Figures 30 and 33 on page 78](#)) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

13. Measurement Bandwidth is from Stopband to 3 Fs.

SWITCHING SPECIFICATIONS - SERIAL PORT

Inputs: Logic 0 = DGND, Logic 1 = VL, SDOUT $C_{LOAD} = 15$ pF.

Parameters	Symbol	Min	Max	Units	
RESET pin Low Pulse Width (Note 14)		1	-	ms	
MCLK Frequency (Note 15)		(See "Serial Port Clocking" on page 34)		MHz	
MCLK Duty Cycle		45	55	%	
Slave Mode					
Input Sample Rate (LRCK)	F_s	(See "Serial Port Clocking" on page 34)		kHz	
LRCK Duty Cycle		45	55	%	
SCLK Frequency	$1/t_P$	-	$64 \cdot F_s$	Hz	
SCLK Duty Cycle		45	55	%	
LRCK Setup Time Before SCLK Rising Edge	$t_{s(LK-SK)}$	40	-	ns	
LRCK Edge to SDOUT MSB Output Delay	$t_{d(MSB)}$	-	52	ns	
SDOUT Setup Time Before SCLK Rising Edge	$t_{s(SDO-SK)}$	20	-	ns	
SDOUT Hold Time After SCLK Rising Edge	$t_{h(SK-SDO)}$	30	-	ns	
SDIN Setup Time Before SCLK Rising Edge	$t_{s(SD-SK)}$	20	-	ns	
SDIN Hold Time After SCLK Rising Edge	t_h	20	-	ns	
Master Mode					
Output Sample Rate (LRCK) All Speed Modes	F_s	(See "Serial Port Clocking" on page 34)		Hz	
LRCK Duty Cycle		45	55	%	
SCLK Frequency	SCLK=MCLK mode	$1/t_P$	-	12.0000	MHz
	MCLK=12.0000 MHz	$1/t_P$	-	$68 \cdot F_s$	Hz
	all other modes	$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle		45	55	%	
LRCK Edge to SDOUT MSB Output Delay	$t_{d(MSB)}$	-	52	ns	
SDOUT Setup Time Before SCLK Rising Edge	$t_{s(SDO-SK)}$	20	-	ns	
SDOUT Hold Time After SCLK Rising Edge	$t_{h(SK-SDO)}$	30	-	ns	
SDIN Setup Time Before SCLK Rising Edge	$t_{s(SD-SK)}$	20	-	ns	
SDIN Hold Time After SCLK Rising Edge	t_h	20	-	ns	

14. After powering up the CS42L52, RESET should be held low after the power supplies and clocks are settled.

15. See "Example System Clock Frequencies" on page 76 for typical MCLK frequencies.

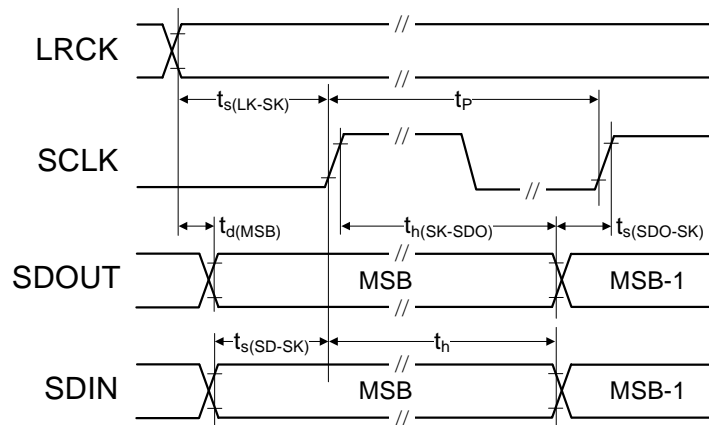


Figure 3. Serial Audio Interface Timing

SWITCHING SPECIFICATIONS - I²C CONTROL PORT

Inputs: Logic 0 = DGND, Logic 1 = VL, SDA C_L = 30 pF.

Parameters	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
RESET Rising Edge to Start	t_{irs}	550	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	μ s
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	μ s
Clock Low time	t_{low}	4.7	-	μ s
Clock High Time	t_{high}	4.0	-	μ s
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	μ s
SDA Hold Time from SCL Falling (Note 16)	t_{hdd}	0	-	μ s
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	μ s
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	μ s
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

16. Data must be held for sufficient time to bridge the transition time, t_{fc} , of SCL.

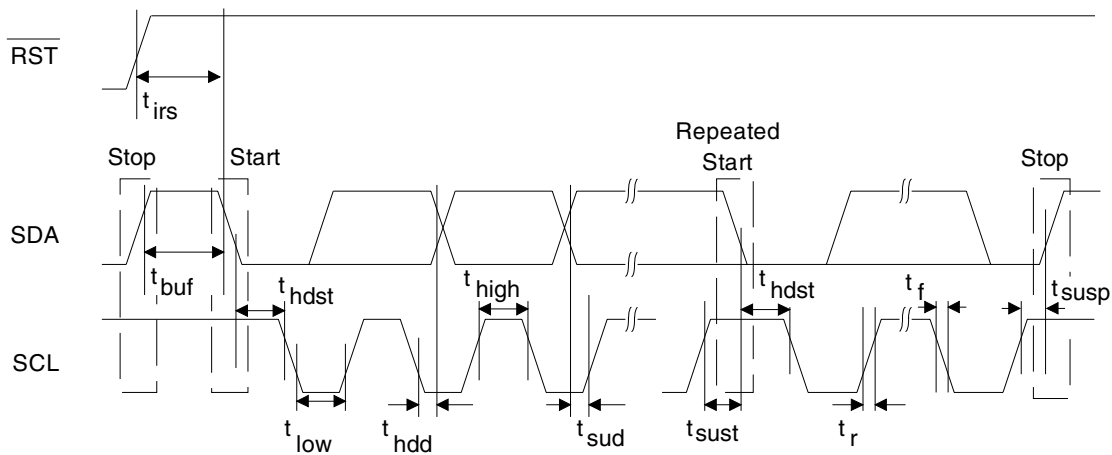


Figure 4. Control Port Timing - I²C

DC ELECTRICAL CHARACTERISTICS

AGND = 0 V; All voltages with respect to ground.

Parameters	Min	Typ	Max	Units	
VQ Characteristics					
Nominal Voltage	-	0.5•VA	-	V	
Output Impedance	-	23	-	kΩ	
DC Current Source/Sink	-	-	1	μA	
MIC BIAS Characteristics					
Nominal Voltage	BIASLVL[2:0] = 000	-	0.5•VA	-	V
	BIASLVL[2:0] = 001	-	0.6•VA	-	V
	BIASLVL[2:0] = 010	-	0.7•VA	-	V
	BIASLVL[2:0] = 011	-	0.8•VA	-	V
	BIASLVL[2:0] = 100	-	0.83•VA	-	V
	BIASLVL[2:0] = 101	-	0.91•VA	-	V
DC Output Current	-	-	1	mA	
Power Supply Rejection Ratio (PSRR)	1 kHz	-	50	-	dB
Power Supply Rejection Ratio Characteristics					
PSRR @1 kHz (Note 17)	PGA to ADC	-	44	-	dB
	ADC	-	60	-	dB
	DAC (HP & Line Amps)	-	60	-	dB
PSRR @60 Hz (Note 17)	PGA to ADC (Note 18)	-	22	-	dB
	ADC	-	42	-	dB
	DAC (HP & Line Amps)	-	60	-	dB
PSRR @217 Hz	Full-Bridge PWM Outputs	-	56	-	dB

17. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

18. The PGA is biased with VQ, created from a resistor divider from the VA supply. Increasing the capacitance on VQ will also increase the PSRR at low frequencies. A 10 μF capacitor on VQ improves the PSRR to 42 dB.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 19)	Symbol	Min	Max	Units	
Input Leakage Current	I_{in}	-	±10	μA	
Input Capacitance		-	10	pF	
1.8 V - 3.3 V Logic					
High-Level Output Voltage ($I_{OH} = -100 \mu A$)	V_{OH}	$V_L - 0.2$	-	V	
Low-Level Output Voltage ($I_{OL} = 100 \mu A$)	V_{OL}	-	0.2	V	
High-Level Input Voltage	V_{IH}	$V_L = 1.65 V$	0.85• V_L	-	V
		$V_L = 1.8 V$	0.76• V_L	-	V
		$V_L = 2.0 V$	0.68• V_L	-	V
		$V_L > 2.0 V$	0.65• V_L	-	V
Low-Level Input Voltage	V_{IL}	-	0.30• V_L	V	

19. See "I/O Pin Characteristics" on page 9 for serial and control port power rails.

POWER CONSUMPTION See (Note 20).

	Operation	Power Ctl. Registers										V	Typical Current (mA)					Total Power (mW _{rms})					
		02h		03h			04h						i _{VHP}	i _{VA}	i _{VD}	i _{VL} VL=3.3V (Note 23)	i _{VP} VP=3.7V						
		PDN_PGAB	PDN_PGAA	PDN_ADCB	PDN_ADCA	PDN	PDN_MICB	PDN_MICA	PDN_MICBIAS	PDN_HP[B][1:0]	PDN_HPA[1:0]								PDN_SPKB[1:0]	PDN_SPKA[1:0]			
1	Off (Note 21)	x	x	x	x	x	x	x	x	x	x	x	x	x	1.8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	
															2.5	0.00	0.00	0.00	0.00	0.00	0.00	0.00	
2	Standby (Note 22)	x	x	x	x	1	x	x	x	x	x	x	x	x	1.8	0.00	0.00	0.01	0.00	0.00	0.00	0.02	
															2.5	0.00	0.00	0.02	0.00	0.00	0.00	0.05	
3	Mono Record	ADC	1	1	1	0	0	1	1	1	11	11	11	11	1.8	0.00	1.67	2.32	0.03	0.00	0.00	7.24	
																2.5	0.00	1.87	3.72	0.03	0.00	0.00	14.05
			1	0	1	0	0	1	1	1	11	11	11	11	1.8	0.00	2.1	2.31	0.03	0.00	0.00	7.99	
																2.5	0.00	2.3	3.72	0.03	0.00	0.00	15.13
			1	0	1	0	0	1	0	0	11	11	11	11	1.8	0.00	3.48	2.32	0.03	0.00	0.00	10.49	
													2.5	0.00	3.71	3.72	0.03	0.00	0.00	18.65			
			1	0	1	0	0	1	0	1	11	11	11	11	1.8	0.00	3.15	2.32	0.03	0.00	0.00	9.90	
														2.5	0.00	3.37	3.73	0.03	0.00	0.00	17.83		
4	Stereo Record	ADC	1	1	0	0	0	1	1	1	11	11	11	11	1.8	0.00	2.31	2.37	0.03	0.00	0.00	8.48	
																2.5	0.00	2.53	3.82	0.03	0.00	0.00	15.95
			0	0	0	0	0	1	1	1	11	11	11	11	1.8	0.00	3.18	2.37	0.03	0.00	0.00	10.04	
														2.5	0.00	3.42	3.81	0.03	0.00	0.00	18.15		
			0	0	0	0	0	0	0	1	11	11	11	11	1.8	0.00	5.32	2.37	0.03	0.00	0.00	13.90	
														2.5	0.00	5.57	3.81	0.03	0.00	0.00	23.53		
5	Mono Playback to Headphone	ADC	1	1	1	1	0	1	1	1	10	11	11	11	1.8	1.59	1.99	2.72	0.01	0.00	0.00	11.36	
																2.5	2.07	2.62	4.27	0.01	0.00	0.00	22.43
6	Mono Playback to Speaker	ADC	1	1	1	1	0	1	1	1	11	11	10	10	1.8	0.00	0.20	4.42	0.01	1.00	1.00	12.05	
																2.5	0.00	0.22	6.77	0.01	1.00	1.00	21.21
7	Stereo Playback to Headphone	ADC	1	1	1	1	0	1	1	1	10	10	11	11	1.8	2.77	2.00	2.91	0.01	0.00	0.00	13.84	
																2.5	3.27	2.63	4.28	0.01	0.00	0.00	25.48
8	Stereo Playback to Speaker	ADC	1	1	1	1	0	1	1	1	11	11	10	10	1.8	0.00	0.20	4.38	0.01	1.00	1.00	11.98	
																2.5	0.00	0.22	6.80	0.01	1.00	1.00	21.28
9	Stereo Passthrough to Headphone	ADC	1	1	1	1	0	1	1	1	10	10	11	11	1.8	2.79	1.91	1.06	0.01	0.00	0.00	10.39	
																2.5	3.18	2.14	1.81	0.01	0.00	0.00	17.85
10	Mono Record & Playback PGA in (no MIC) to Mono HP	ADC	1	0	1	0	0	1	1	1	11	10	11	11	1.8	1.77	3.95	4.28	0.03	0.00	0.00	18.05	
																2.5	2.13	4.77	6.63	0.03	0.00	0.00	33.90
11	Phone Monitor MIC (w/bias) in to Mono Out	ADC	1	0	1	0	0	1	0	0	11	10	11	11	1.8	1.76	5.33	4.28	0.03	0.00	0.00	20.52	
																2.5	2.15	6.19	6.69	0.03	0.00	0.00	37.65
12	Stereo Record & Playback PGA in (no MIC) to St. HP Out	ADC	0	0	0	0	0	1	1	1	10	10	11	11	1.8	2.76	5.05	4.64	0.03	0.00	0.00	22.46	
																2.5	3.21	5.90	7.17	0.03	0.00	0.00	40.78
13	Stereo Rec. & Full Playback PGA (no MIC) to St. HP & SPK	ADC	0	0	0	0	0	1	1	1	10	10	10	10	1.8	3.49	5.24	7.20	0.03	1.00	1.00	32.47	
																2.5	3.95	6.10	10.46	0.03	1.00	1.00	55.07

20. Unless otherwise noted, test conditions are as follows: All zeros input, slave mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation. "Required Initialization Settings" on page 37 written on power up.

21. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.

22. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.

23. VL current will slightly increase in master mode.

4. APPLICATIONS

4.1 Overview

4.1.1 *Basic Architecture*

The CS42L52 is a highly integrated, low-power, 24-bit audio CODEC comprised of a stereo analog-to-digital converter (ADC), a stereo digital-to-analog converter (DAC), a digital PWM modulator and two full-bridge power back-ends. The ADC and DAC are designed using multi-bit delta-sigma techniques - the DAC operates at an oversampling ratio of 128Fs and the ADC operates at 64Fs, where Fs is equal to the system sample rate.

The different clock rates maximize power savings while maintaining high performance. The PWM modulator operates at a fixed frequency of 384 kHz. The power FETs are configured for either stereo full-bridge or mono parallel full-bridge output. The CODEC operates in one of four sample rate speed modes: Quarter, Half, Single, and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

4.1.2 *Line & MIC Inputs*

The analog input portion of the CODEC allows selection from and configuration of multiple combinations of stereo and microphone (MIC) sources. Eight line inputs with an option for two balanced MIC inputs, a MIC bias output, and a Programmable Gain Amplifier (PGA) comprise the analog front-end.

4.1.3 *Line & Headphone Outputs*

The analog output portion of the CODEC includes a headphone amplifier capable of driving headphone and line-level loads. An on-chip charge pump creates a negative headphone supply allowing a full-scale output swing centered around ground. This eliminates the need for large DC-Blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages.

4.1.4 *Speaker Driver Outputs*

The Class D power amplifiers drive 8 ohm (stereo) and 4 ohm (mono) speakers directly, without the need for an external filter. The power MOSFETS are powered directly from a battery eliminating the efficiency loss associated with an external regulator. Battery level monitoring and compensation maintains a steady output as battery levels fall. **NOTE:** The CS42L52 should only be used in captive speaker systems where the outputs are permanently tied to the speaker terminals.

4.1.5 *Fixed Function DSP Engine*

The fixed-function digital signal processing engine processes both the PCM serial input data and ADC output data, allowing a mix between the two. Independent volume control, left/right channel swaps, mono mixes, tone control, and limiting functions also comprise the DSP engine.

4.1.6 *Beep Generator*

The beep generator delivers tones at select frequencies across approximately two octave major scales. With independent volume control, beeps may be configured to occur continuously, periodically, or at single time intervals.

4.1.7 *Power Management*

Three control registers provide independent power-down control of the ADC, DAC, PGA, MIC pre-amp, MIC bias, Headphone, and Speaker outputs, allowing operation in select applications with minimal power consumption.

4.2 Analog Inputs

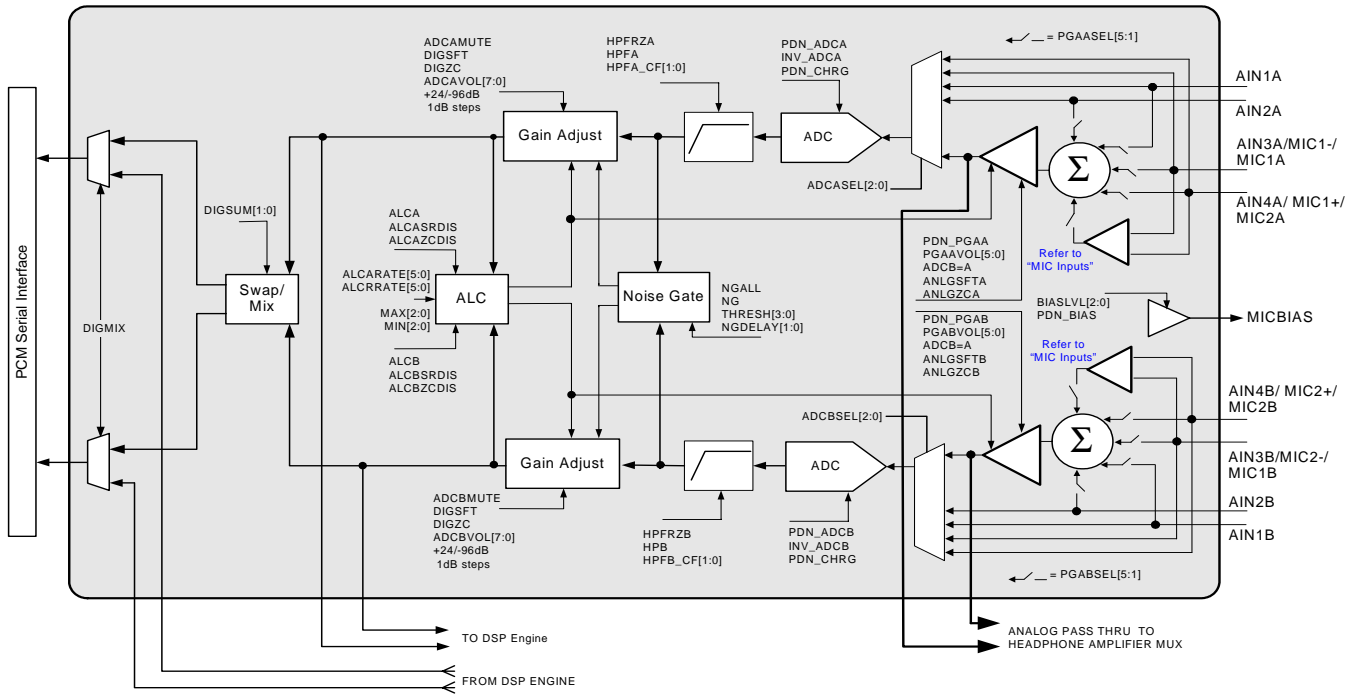


Figure 5. Analog Input Signal Flow

Referenced Control	Register Location
Analog Front End	
PDN_PGAx	“Power Down PGAx” on page 42
PGAxVOL[5:0]	“PGAx Volume” on page 56
ADCB=A	“Analog Front-End Volume Setting B=A” on page 50
ANLGSFTx	“Ch. x Analog Soft Ramp” on page 49
ANLGZCx	“Ch. x Analog Zero Cross” on page 49
ADCxSEL[2:0]	“ADC Input Select” on page 48
PGAxSEL5,4,3,2,1	“PGA Input Mapping” on page 49
BIASLVL[2:0]	“MIC Bias Level” on page 48
PDN_BIAS	“Power Down MIC Bias” on page 43
PDN_ADCx	“Power Down ADCx” on page 43
PDN_CHRG	“Power Down ADC Charge Pump” on page 42
INV_ADCx	“Invert ADC Signal Polarity” on page 51
HPFRZx	“ADCx High-Pass Filter Freeze” on page 49
HPFx	“ADCx High-Pass Filter” on page 49
HPFx_CF[1:0]	“HPF x Corner Frequency” on page 50
ADCxOVFL	“ADCx Overflow (Read Only)” on page 71
Digital Volume	
ADCxMUTE	“ADC Mute” on page 51
ADCxVOL	“ADCx Volume” on page 57
ALCx	“ALCx Enable” on page 67
ALCxSRDIS	“ALCx Soft Ramp Disable” on page 55
ALCxZCDIS	“ALCx Zero Cross Disable” on page 56
ALCARATE[5:0]	“ALC Attack Rate” on page 67
ALCRRATE[5:0]	“ALC Release Rate” on page 68
MAX[2:0]	“ALC Maximum Threshold” on page 68
MIN[2:0]	“ALC Minimum Threshold” on page 69
NGALL	“Noise Gate All Channels” on page 69
NG	“Noise Gate Enable” on page 69
THRESH[3:0]	“Noise Gate Threshold and Boost” on page 70
NGDELAY[1:0]	“Noise Gate Delay Timing” on page 70
Miscellaneous	
DIGSUM[1:0]	“Digital Sum” on page 50
DIGMUX	“Digital MUX” on page 50

4.2.1 MIC Inputs

The input pins 21, 22, 23, and 24 accept stereo line-level or microphone signals. For microphone inputs, either single-ended or differential configuration is allowed, providing programmable pre-amplification of low-level signals. In the single-ended configuration, an internal MUX chooses one of two stereo sets (selection is made independently on channels A and B). In the differential configuration, an internal voltage follower cascaded with the pre-amplifier maintains high input impedance and provides noise rejection above the MICxGAIN setting. The pre-amps are biased to VQ in both configurations.

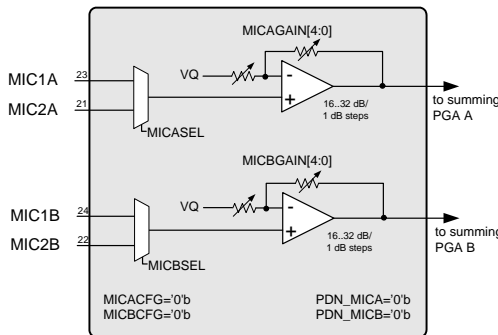
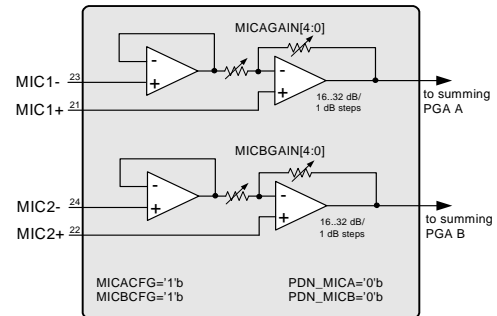


Figure 6. Single-Ended MIC Configuration



Note: Output to PGA = (MIC⁺ - MIC⁻)*gain + MIC⁻

Figure 7. Differential MIC Configuration

Referenced Control	Register Location
MICxCFG	"MICx Configuration" on page 55
PDN_MICx	"Power Down MICx" on page 43
MICxGAIN	"MICx Gain" on page 55

4.2.2 Automatic Level Control (ALC)

When enabled, the ALC monitors the analog input signal after the digital attenuator, detects when peak levels exceed the maximum (MAX) threshold settings, and responds by applying attenuation as necessary to maintain the resulting level below the MAX threshold. To apply this attenuation, the ALC first lowers the PGA gain settings and then increases the digital attenuation levels. All attenuation is applied at a programmable attack rate.

When input signal levels fall below the minimum (MIN) threshold, the ALC responds by removing any attenuation that it has previously applied until all ALC-applied attenuation has been removed or until the MAX threshold is again crossed. To remove this attenuation, the ALC first decreases the digital attenuation levels and then increases the PGA gain. All attenuation is removed at a programmable release rate.

It should be noted that the ALC is applied independently to channels A and B with one exception: the input signals on both channels A and B must be below the MIN threshold in order for the ALC attenuation to be released on channel B.

Attack and release rates are affected by the ADC soft-ramp/zero-cross settings and sample rate, Fs. ALC soft-ramp and zero-cross dependency may be independently enabled/disabled.

Recommended settings: Best level control may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers.

Notes:

1. When ALC x is enabled and the PGAxVOL[5:0] is set above 12 dB, the ADCxVOL[7:0] should not be set below 0 dB.
2. The maximum realized gain must be set in the PGAxVOL register. The ALC will only apply the gain set in the PGAxVOL.
3. The ALC maintains the output signal between the MIN and MAX thresholds. As the input signal level

changes, the level-controlled output may not always be the same but will always fall within the thresholds.

Referenced Control Register Location	
PGAxVOL[5:0]	"PGAx Vol. & ALCx Transition Ctl.: ALC, PGA A (Address 12h) & ALC, PGA B (Address 13h)" on page 55
MAX[2:0], MIN[2:0]	"ALC Threshold (Address 2Ch)" on page 68

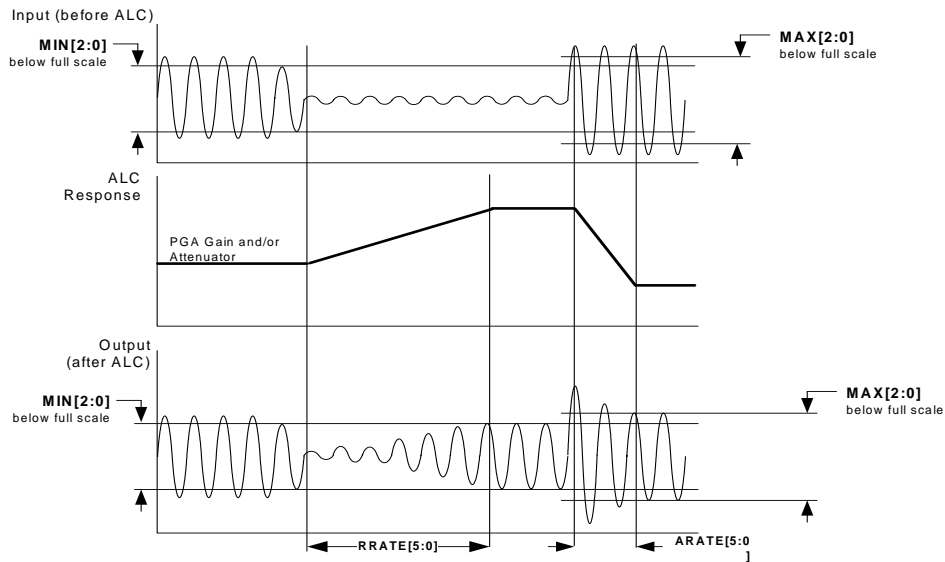


Figure 8. ALC

4.2.3 Noise Gate

The noise gate may be used to mute signal levels that fall below a programmable threshold. This prevents the ALC from applying gain to noise. A programmable delay may be used to set the minimum time before the noise gate attacks the signal.

Note: Maximum noise gate attenuation levels will depend on the gain applied in either the PGA or MIC pre-amplifier. For example: If both +32 dB pre-amplification and +12 dB programmable gain is applied, the maximum attenuation that the noise gate achieves will be 52 dB (-96 + 32 + 12) below full-scale.

Referenced Control	Register Location
Noise Gate Controls.....	"Noise Gate Control (Address 2Dh)" on page 69

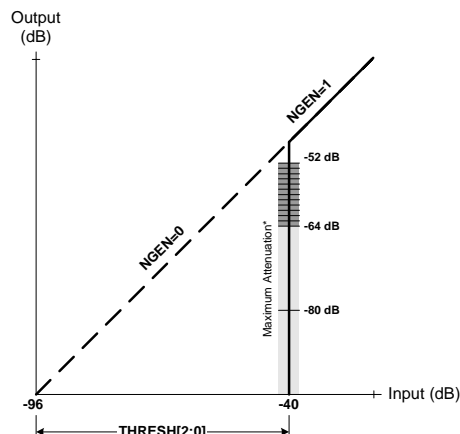


Figure 9. Noise Gate Attenuation

4.3 Analog Outputs

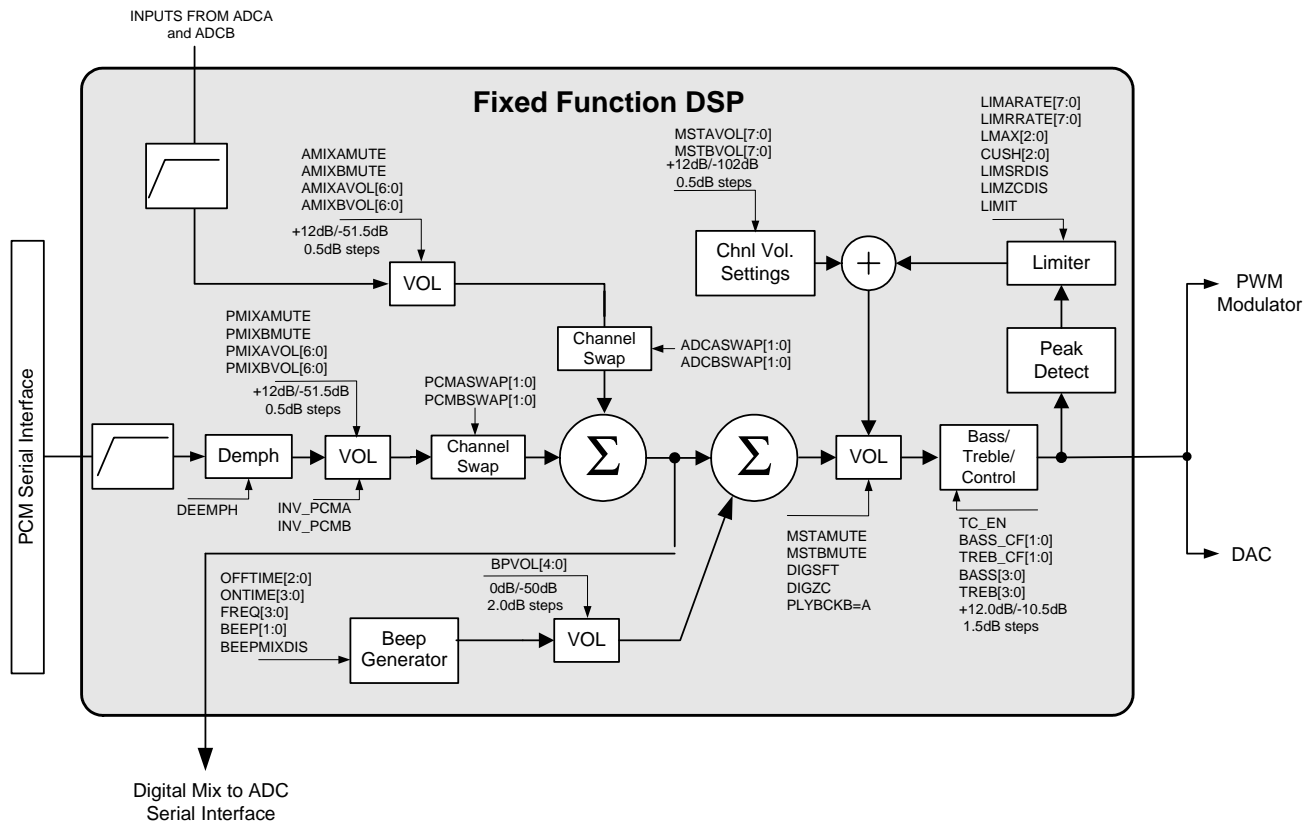
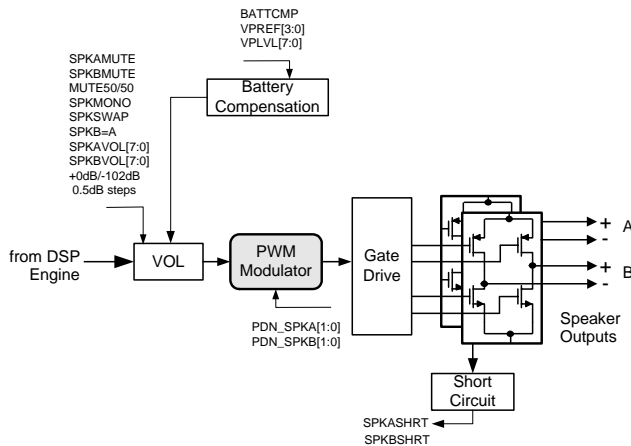
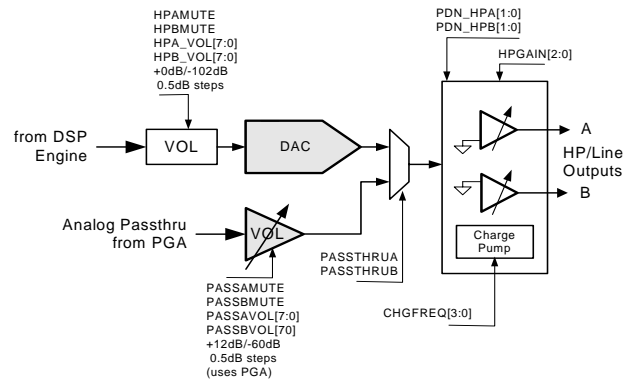


Figure 10. DSP Engine Signal Flow

Referenced Control	Register Location
DSP	
DEEMPH	"HP/Speaker De-emphasis" on page 53
PMIXxMUTE	"PCM Mixer Channel x Mute" on page 58
PMIXxVOL[6:0]	"PCM Mixer Channel x Volume" on page 58
INV_PCMx	"Invert PCM Signal Polarity" on page 52
PCMXSWAP[1:0]	"PCM Mix Channel Swap" on page 64
AMIXxMUTE	"ADC Mixer Channel x Mute" on page 58
AMIXxVOL[6:0]	"ADC Mixer Channel x Volume" on page 58
ADCxSWAP[1:0]	"ADC Mix Channel Swap" on page 64
MSTxVOL[7:0]	"Master Volume Control" on page 63
MSTxMUTE	"Master Playback Mute" on page 52
DIGSFT	"Digital Soft Ramp" on page 53
DIGZC	"Digital Zero Cross" on page 53
PLYBCKB=A	"Playback Volume Setting B=A" on page 51
TC_EN	"Tone Control Enable" on page 62
BASS_CF[1:0]	"Bass Corner Frequency" on page 62
TREB_CF[1:0]	"Treble Corner Frequency" on page 62
BASS[3:0]	"Bass Gain" on page 63
TREB[3:0]	"Treble Gain" on page 62
LIMIT	"Peak Detect and Limiter" on page 66
LIMSRDIS	"Limiter Soft Ramp Disable" on page 65
LIMZCDIS	"Limiter Zero Cross Disable" on page 66
LMAX[2:0]	"Limiter Maximum Threshold" on page 65
CUSH[2:0]	"Limiter Cushion Threshold" on page 65
LIMARATE[7:0]	"Limiter Attack Rate" on page 67
LIMRRATE[7:0]	"Limiter Release Rate" on page 66


Figure 11. PWM Output Stage

Figure 12. Analog Output Stage

Referenced Control	Register Location
PWM Control	
SPKxMUTE	"Speaker Mute" on page 54
MUTE50/50	"Speaker Mute 50/50 Control" on page 54
SPKMONO	"Speaker MONO Control" on page 54
SPKxVOL[7:0]	"Speaker Volume Control" on page 64
SPKSWAP	"Speaker Channel Swap" on page 54
SPKB=A	"Speaker Volume Setting B=A" on page 54
BATTCMP	"Battery Compensation" on page 71
VPREF[3:0]	"VP Reference" on page 72
VPLVL[7:0]	"VP Voltage Level (Read Only)" on page 72
PDN_SPKx[1:0]	"Speaker Power Control" on page 44
SPKxSHRT	"Speaker Current Load Status (Read Only)" on page 72

Referenced Control	Register Location
Analog Output	
HPxMUTE	"Headphone Mute" on page 54
HPxVOL[7:0]	"Headphone Volume Control" on page 63
PDN_HPxA[1:0]	"Headphone Power Control" on page 44
HPGAIN[2:0]	"Headphone Analog Gain" on page 51
PASSTHRUx	"Passthrough Analog" on page 52
PASSxMUTE	"Passthrough Mute" on page 52
PASSxVOL[7:0]	"Passthrough x Volume" on page 57
CHGFREQ	"Charge Pump Frequency" on page 73

4.3.1 Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple, and single (one-shot) beeps. Sixteen on and eight off times are available.

Note: The Beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be required to set the beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, MSTxVOL[7:0], will affect the beep volume, DAC volume may alternatively be controlled using the PMIXxVOL[6:0] bits.

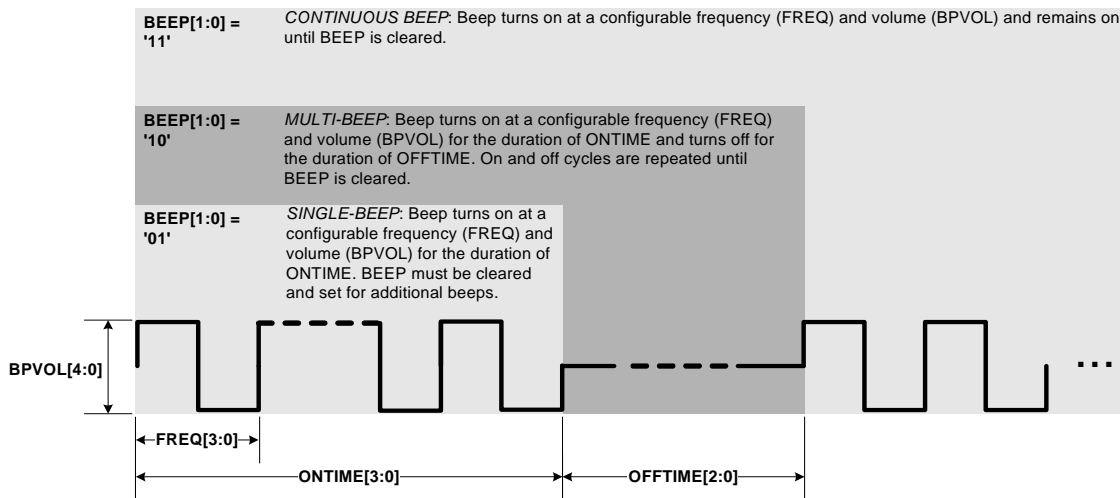


Figure 13. Beep Configuration Options

Referenced Control	Register Location
MSTxVOL[7:0].....	"Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h)" on page 63
PMIXxVOL[6:0].....	"PCMx Mixer Volume: PCMA (Address 1Ah) & PCMB (Address 1Bh)" on page 58
OFFTIME[2:0].....	"Beep Off Time" on page 60
ONTIME[3:0].....	"Beep On Time" on page 60
FREQ[3:0].....	"Beep Frequency" on page 59
BEEP[1:0].....	"Beep Configuration" on page 61
BEEP MIX DIS.....	"Beep Mix Disable" on page 61
BPVOL[4:0].....	"Beep Volume" on page 61

4.3.2 Limiter

When enabled, the limiter monitors the digital input signal before the DAC and PWM modulators, detects when levels exceed the maximum threshold settings, and lowers the master volume at a programmable attack rate below the maximum threshold. When the input signal level falls below the maximum threshold, the AOUT volume returns to its original level set in the Master Volume Control register at a programmable release rate. Attack and release rates are affected by the DAC soft-ramp/zero-cross settings and sample rate, Fs. Limiter soft-ramp and zero-cross dependency may be independently enabled/disabled.

Notes:

1. *Recommended settings:* Best limiting performance may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. The MIN bits allow the user to set a threshold slightly below the maximum threshold for hysteresis control - this cushions the sound as the limiter attacks and releases.
2. The Limiter maintains the output signal between the MIN and MAX thresholds. As the digital input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds.

Referenced Control	Register Location
Limiter Controls.....	"Limiter Control 2, Release Rate (Address 28h)" on page 66, "Limiter Attack Rate (Address 29h)" on page 67
Master Volume Control.....	"Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h)" on page 63

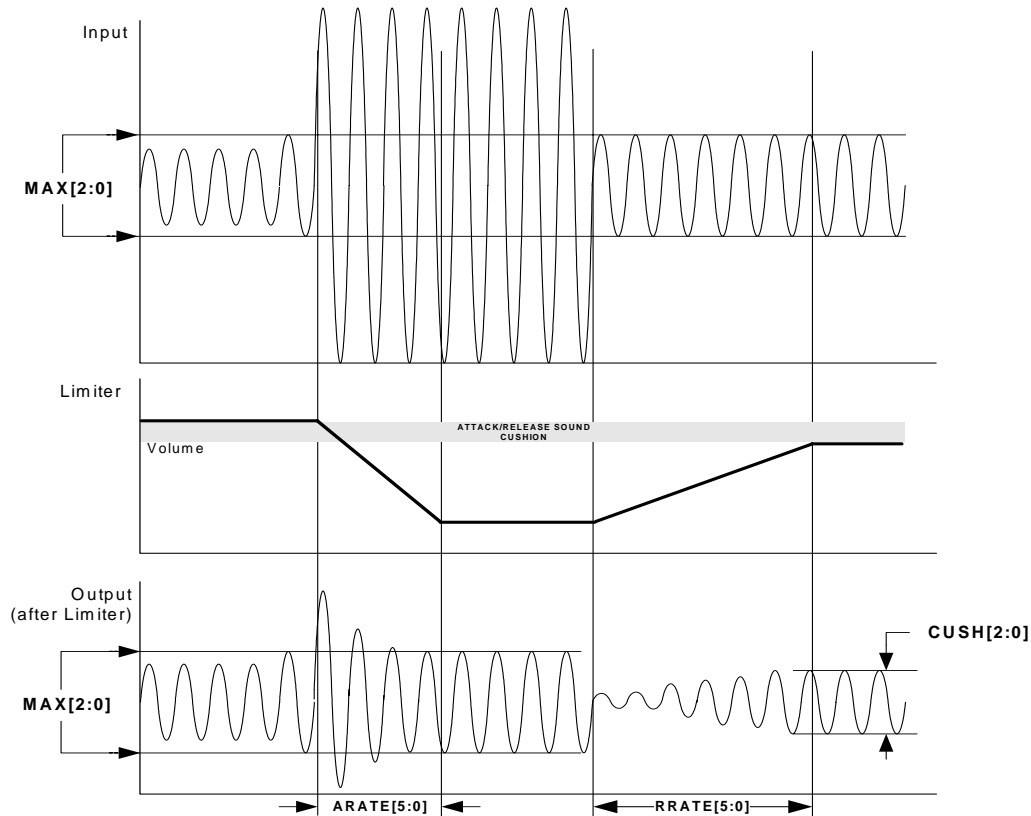


Figure 14. Peak Detect & Limiter

4.4 Analog In to Analog Out Passthrough

The CS42L52 accommodates analog routing of the analog input signal directly to the headphone amplifiers. This feature is useful in applications that utilize an FM tuner where audio recovered over-the-air must be transmitted to the headphone amplifier without digital conversion in the ADC and DAC. This analog passthrough path reduces power consumption and is immune to modulator switching noise that could interfere with some tuners.

4.4.1 Overriding the ADC Power Down

To accommodate automatic activation of the speaker amplifier when the SPK/HP_SW switch pin changes, the CS42L52 provides the option to automatically power up the ADC whenever the analog signal must route to the digital PWM modulator, regardless of the PDN_ADC bit. Refer to the table below for details on how this ADC power-down override functions in accordance with the state of the speaker channels. The shaded cells represent normal ADC operation when passthrough is disabled.

PDN_ADC	PASSTHRU	PDN_OVRD	Speaker Channel	ADC Status
0	x	x	x	Powered UP
	0	x	x	Powered DOWN
1	1	0	x	Powered DOWN
		1	OFF	Powered DOWN
			ON	Powered UP

When PASSTHRU and PDN_OVRD are enabled, turning the speaker channel ON (by writing '1'b to SPKx_PDN[1:0] or by automatic activation of the headphone detect switch, SPK/HP_SW) will automatically disable the ADCx_PDN in order to convert the analog input to a digital signal for the PWM modulator. This allows automatic analog input routing to the speaker amplifiers.

Referenced Control	Register Location
PDN_ADCx	"Power Down ADCx" on page 43
PASSTHRU	"Passthrough Analog" on page 52
PDN_OVRD	"Power Down ADC Override" on page 43
SPKx_PDN[1:0]	"Speaker Power Control" on page 44

4.4.2 Overriding the PGA Power Down

To accommodate automatic activation of the headphone amplifier when the SPK/HP_SW switch pin changes, the CS42L52 will automatically power up the PGA whenever passthrough is enabled, regardless of the PDN_PGA setting. Refer to the table below for details on how this PGA power-down override functions in accordance with the state of the headphone channels. The shaded cells represent normal PGA operation when passthrough is disabled.

PDN_PGA	PASSTHRU	HP Channel	PGA Status
0	x	x	Powered UP
1	0	x	Powered DOWN
	1	OFF	Powered DOWN
		ON	Powered UP

When passthrough is enabled, turning the headphone channel ON (by writing '11'b to HPx_PDN[1:0] or by automatic activation of the headphone detect switch, SPK/HP_SW) will automatically disable the PGAx_PDN in order to transmit the analog signal to the headphone.

Referenced Control	Register Location
PDN_PGAx	"Power Down PGAx" on page 42
PASSTHRU	"Passthrough Analog" on page 52
HPx_PDN[1:0]	"Headphone Power Control" on page 44

4.5 PWM Outputs

4.5.1 Mono Speaker Output Configuration

The CS42L52 accommodates a stereo as well as a mono speaker output configuration. In mono mode the output drivers of each channel are connected in parallel to deliver maximum power to a 4 ohm speaker. Refer to the table below for pin mapping in mono configuration.

Pin	Speaker Output			
	SPKMONO=0		SPKMONO=1	
	SPKSWAP=0	SPKSWAP=1	SPKSWAP=0	SPKSWAP=1
4	SPKOUTA+	SPKOUTB+	SPKOUTA+	SPKOUTB+
6	SPKOUTA-	SPKOUTB-	SPKOUTA+	SPKOUTB+
7	SPKOUTB+	SPKOUTA+	SPKOUTA-	SPKOUTB-
9	SPKOUTB-	SPKOUTA-	SPKOUTA-	SPKOUTB-

Referenced Control	Register Location
SPKMONO	"Speaker MONO Control" on page 54
SPKSWAP	"Speaker Channel Swap" on page 54

4.5.2 VP Battery Compensation

The CS42L52 provides the option to maintain a desired power output level, independent of the VP supply. When enabled, this feature works by monitoring the voltage on the VP supply and *reducing the attenuation* on the speaker outputs when VP voltage levels fall.

Note: The internal ADC that monitors the VP supply operates from the VA supply. Calculations are based on typical VA levels of 1.8 V and 2.5 V using the VPREF bits.

4.5.2.1 Maintaining a Desired Output Level

Using SPKxVOL, the speaker output level must first be attenuated by the decibel equivalent of the expected VP supply range (MAX relative to MIN). The CS42L52 then gradually *reduces* the attenuation as the VP supply drops from its maximum level, maintaining a nearly constant power output.

Compensation Example 1 (VP Battery supply ranges from 4.5 V to 3.0 V)

1. Set speaker attenuation (SPKxVOL) to -3.5 dB. *The VP supply changes ~-3.5 dB.*
2. Set the reference VP supply (VPREF) to 4.5 V.
3. Enable battery compensation (BATTCMP).

The CS42L52 automatically adjusts the output level as the battery discharges.

Compensation Example 2 (VP Battery supply ranges from 5.0 V to 1.6 V)

1. Set speaker attenuation (SPKxVOL) to -10 dB. *The VP supply changes ~-9.9 dB.*
2. Set the reference VP supply (VPREF) to 5.0 V.
3. Enable battery compensation (BATTCMP).

The CS42L52 automatically adjusts the output level as the battery discharges. Refer to Figure 15 on page 34. In this example, the VP supply changes over a wide range, illustrating the accuracy of the CS42L52's battery compensation.

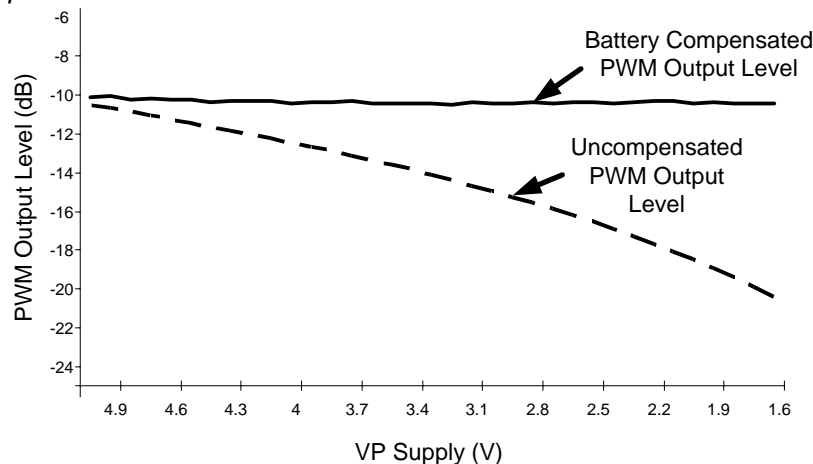


Figure 15. Battery Compensation

Referenced Control	Register Location
VPREF	"VP Reference" on page 72
SPKxVOL	"Speaker Volume Control" on page 64

4.6 Serial Port Clocking

The CODEC serial audio interface port operates either as a slave or master, determined by the M/\bar{S} bit. It accepts externally generated clocks in Slave Mode and will generate synchronous clocks derived from an input master clock (MCLK) in Master Mode. Refer to the tables below for the required setting in register 05h and 06h associated with a given MCLK and sample rate.

Referenced Control	Register Location
M/\bar{S}	"Master/Slave Mode" on page 46
Register 05h	"Clocking Control (Address 05h)" on page 44
Register 06h	"Interface Control 1 (Address 06h)" on page 46

MCLK (MHz)	Sample Rate, Fs (kHz)	SPEED[1:0] (AUTO='0'b)	32kGROUP	VIDEOCLK	RATIO[1:0]	MCLKDIV2
12.2880	8.0000	11	1	0	00	0
	12.0000	11	0	0	00	0
	16.0000	10	1	0	00	0
	24.0000	10	0	0	00	0
	32.0000	01	1	0	00	0
	48.0000	01	0	0	00	0
11.2896	96.0000	00	0	0	00	0
	11.0250	11	0	0	00	0
	22.0500	10	0	0	00	0
	44.1000	01	0	0	00	0
18.4320 (Slave Mode ONLY)	88.2000	00	0	0	00	0
	8.0000	11	1	0	00	0
	12.0000	11	0	0	00	0
	16.0000	10	1	0	00	0
	24.0000	10	0	0	00	0
	32.0000	01	1	0	00	0
16.9344 (Slave Mode ONLY)	48.0000	01	0	0	00	0
	96.0000	00	0	0	00	0
	8.0182	11	0	0	10	0
	11.0250	11	0	0	00	0
12.0000	22.0500	10	0	0	00	0
	44.1000	01	0	0	00	0
	88.2000	00	0	0	00	0
	8.0000	11	1	0	01	0
	11.0294	11	0	0	11	0
	12.0000	11	0	0	01	0
	16.0000	10	1	0	01	0
	22.0588	10	0	0	11	0
	24.0000	10	0	0	01	0
24.0000	32.0000	01	1	0	01	0
	44.1176	01	0	0	11	0
	48.0000	01	0	0	01	0
	88.2353	00	0	0	11	0
	96.0000	00	0	0	01	0
	8.0000	11	1	0	01	1
	11.0294	11	0	0	11	1
	12.0000	11	0	0	01	1
	16.0000	10	1	0	01	1
27.0000	22.0588	10	0	0	11	1
	24.0000	10	0	0	01	1
	32.0000	01	1	0	01	1
	44.1176	01	0	0	11	1
	48.0000	01	0	0	01	1
	88.2353	00	0	0	11	1
	96.0000	00	0	0	01	1
	8.0000	11	1	1	01	0
12.0000	12.0000	11	0	1	01	0
	24.0000	10	0	1	01	0
	32.0000	01	1	1	01	0
	44.1176	01	0	1	11	0
	48.0000	01	0	1	01	0
	11.0294	11	0	1	11	0
	22.0588	10	0	1	11	0
	16.0000	10	1	1	01	0

Table 1. MCLK, LRCK Quick Decode

4.7 Digital Interface Formats

The serial port operates in standard I²S, Left-justified, Right-justified (DAC only), or DSP Mode digital interface formats with varying bit depths from 16 to 24. Data is clocked out of the ADC or into the DAC on the rising edge of SCLK.

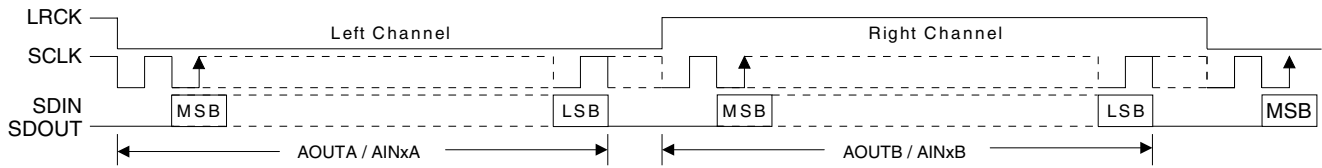


Figure 16. I²S Format

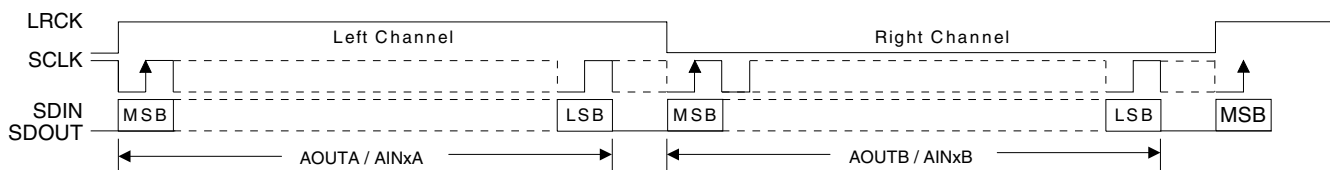


Figure 17. Left-Justified Format

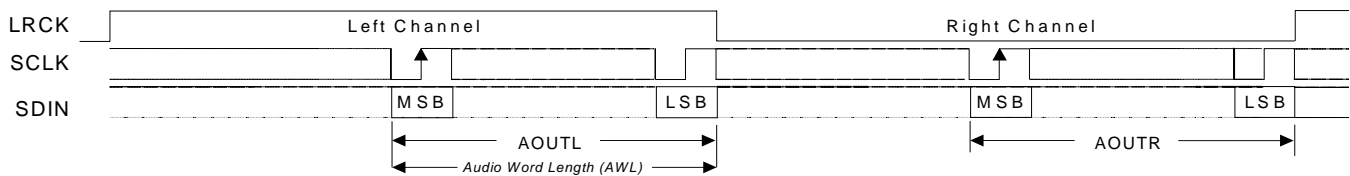


Figure 18. Right-Justified Format (DAC only)

4.7.1 DSP Mode

In DSP Mode, the LRCK acts as a frame sync for 2 data-packed words (left and right channel) input on SDIN and output on SDOUT. The MSB is input/output on the first SCLK rising edge after the frame sync rising edge. The right channel immediately follows the left channel.

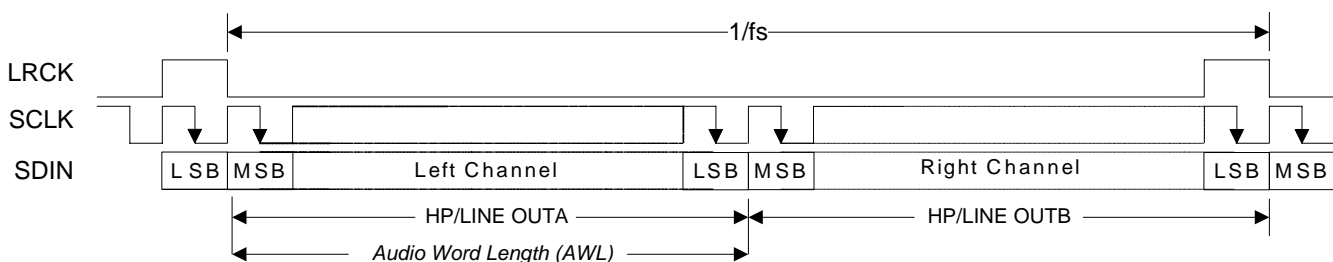


Figure 19. DSP Mode Format

4.8 Initialization

The CODEC enters a Power-down state upon initial power-up. The interpolation and decimation filters, delta-sigma and PWM modulators, and control port registers are reset. The internal voltage reference, and switched-capacitor low-pass filters are powered down.

The device will remain in the Power-down state until the $\overline{\text{RESET}}$ pin is brought high. The control port is accessible once $\overline{\text{RESET}}$ is high and the desired register settings can be loaded per the interface descriptions in the [“Register Description” on page 42](#).

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+, will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

4.9 Recommended Power-up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable.
2. Bring $\overline{\text{RESET}}$ high.
3. The default state of the PDN bit is ‘1’b. Load the desired register settings while keeping the PDN bit set to ‘1’b.
4. Load the required initialization settings listed in [Section 4.11](#).
5. Start MCLK to the appropriate frequency, as discussed in [Section 4.6](#).
6. Set the PDN bit to ‘0’b.
7. Apply LRCK, SCLK, and SDIN for normal operation to begin.
8. Bring $\overline{\text{RESET}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.10 Recommended Power-down Sequence

To minimize audible pops when turning off or placing the CODEC in standby:

1. Mute the DAC’s and ADC’s.
2. Set the PDN bit in the power control register to ‘1’b. The CODEC will not power down until it reaches a fully muted state. Do not remove MCLK until after the part has fully muted. Note that it may be necessary to disable the soft-ramp and/or zero-cross volume transitions to achieve faster muting/power down.
3. Bring $\overline{\text{RESET}}$ low.

4.11 Required Initialization Settings

The current and thresholds required for various sections in the CODEC must be adjusted by implementing the initialization settings shown below after power-up sequence step 3. All performance and power consumption measurements were taken with the following settings:

1. Write 0x99 to register 0x00.
2. Write 0xBA to register 0x3E.
3. Write 0x80 to register 0x47.
4. Write ‘1’b to bit 7 in register 0x32.
5. Write ‘0’b to bit 7 in register 0x32.
6. Write 0x00 to register 0x00.

4.12 Control Port Operation

The control port is used to access the registers, allowing the CODEC to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates using an I²C interface with the CODEC acting as a slave device.

4.12.1 I²C Control

SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. The signal timings for a read and write cycle are shown in [Figure 20](#) and [Figure 21](#). A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is defined as a rising transition of SDA while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42L52 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write).

The upper 7 bits of the address field are fixed at 1001010. To communicate with the CS42L52, the chip address field, which is the first byte sent to the CS42L52, should match 1001010. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP), which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42L52 after each input byte is read and is input to the CS42L52 from the microcontroller after each transmitted byte.

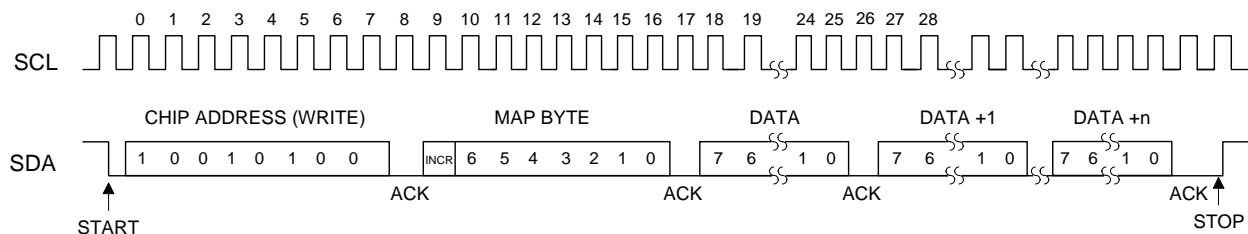


Figure 20. Control Port Timing, I²C Write

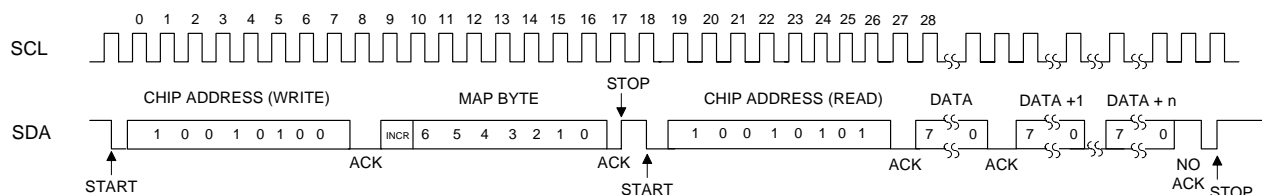


Figure 21. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in [Figure 21](#), the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.
Send 10010100 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto-increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10010101 (chip address & read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.12.2 Memory Address Pointer (MAP)

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudo code above for implementation details.

4.12.2.1 Map Increment (INCR)

The device has MAP auto-increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads. If INCR is set to 1, MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

5. REGISTER QUICK REFERENCE

(Default values are shown below the bit names)

I ² C Address: 1001010[R/W] - 10010100 = 0x94(Write); 10010101 = 0x95(Read)									
Adr.	Function	7	6	5	4	3	2	1	0
01h p 42	ID	CHIPID4 1	CHIPID3 1	CHIPID2 1	CHIPID1 0	CHIPID0 0	REVID2 x	REVID1 x	REVID0 x
02h p 42	Power Ctl 1	PDN_CHRG 0	Reserved 0	Reserved 0	PDN_PGAB 0	PDN_PGAA 0	PDN_ADCB 0	PDN_ADCA 0	PDN 1
03h p 43	Power Ctl 2	Reserved 0	Reserved 0	Reserved 0	OVRDB 0	OVRDA 0	PDN_MICB 1	PDN_MICA 1	PDN_BIAS 1
04h p 44	Power Ctl 3	PDN_HPB1 0	PDN_HPBO 0	PDN_HPA1 0	PDN_HPA0 0	PDN_SPKB1 0	PDN_SPKB0 1	PDN_SPKA1 0	PDN_SPKA0 1
05h p 44	Clocking Ctl	AUTO 1	SPEED1 0	SPEED0 1	32kGROUP 0	VIDEOCLK 0	RATIO1 0	RATIO0 0	MCLKDIV2 0
06h p 46	Interface Ctl 1	M/S 0	INV_SCLK 0	ADCDF1 0	DSP 0	DACDF1 0	DACDF0 0	AWL1 0	AWL0 0
07h p 47	Interface Ctl 2	Reserved 0	SCLK=MCLK 0	DIGLOOP 0	3ST_SP 0	INV_SWCH 0	BIASLVL2 0	BIASLVL1 0	BIASLVL0 0
08h p 48	Input A Select	ADCASEL2 1	ADCASEL1 0	ADCASEL0 0	PGAASEL5 0	PGAASEL4 0	PGAASEL3 0	PGAASEL2 0	PGAASEL1 1
09h p 48	Input B Select	ADCBSEL2 1	ADCBSEL1 0	ADCBSEL0 0	PGABSEL5 0	PGABSEL4 0	PGABSEL3 0	PGABSEL2 0	PGABSEL1 1
0Ah p 49	Analog, HPF Ctl	HPFB 1	HPFRZB 0	HPFA 1	HPFRZA 0	ANLGSFTB 0	ANLGZCB 1	ANLGSFTA 0	ANLGZCA 1
0Bh p 50	ADC HPF Corner Freq.	Reserved 0	Reserved 0	Reserved 0	Reserved 0	HPFB_CF1 0	HPFB_CF0 0	HPFA_CF1 0	HPFA_CF0 0
0Ch p 50	Misc. ADC Ctl	ADCB=A 0	DIGMIX 0	DIGSUM1 0	DIGSUM0 0	INV_ADCB 0	INV_ADCA 0	ADCBMUTE 0	ADCAMUTE 0
0Dh p 51	Playback Ctl 1	HPGAIN2 0	HPGAIN1 1	HPGAIN0 1	PLYBCKB=A 0	INV_PCMB 0	INV_PCMA 0	MSTBMUTE 0	MSTAMUTE 0
0Eh p 52	Misc. Ctl	PASSTHRUB 0	PASSTHUA 0	PASSBMUTE 0	PASSAMUTE 0	FREEZE 0	DEEMPH 0	DIGSFT 1	DIGZC 0
0Fh p 54	Playback Ctl 2	HPBMUTE 0	HPAMUTE 0	SPKBMUTE 0	SPKAMUTE 0	SPKB=A 0	SPKSWAP 0	SPKMONO 0	MUTE50/50 0
10h p 55	MICA Amp Ctl	Reserved 0	MICASEL 0	MICACFG 0	MICAGAIN4 0	MICAGAIN3 0	MICAGAIN2 0	MICAGAIN1 0	MICAGAIN0 0
11h p 55	MICB Amp Ctl	Reserved 0	MICBSEL 0	MICBCFG 0	MICBGAIN4 0	MICBGAIN3 0	MICBGAIN2 0	MICBGAIN1 0	MICBGAIN0 0
12h p 55	PGAA Vol, Misc	ALCASRDIS 0	ALCAZCDIS 0	PGAAVOL5 0	PGAAVOL4 0	PGAAVOL3 0	PGAAVOL2 0	PGAAVOL1 0	PGAAVOL0 0
13h p 55	PGAB Vol, Misc	ALCBSRDIS 0	ALCBZCDIS 0	PGABVOL5 0	PGABVOL4 0	PGABVOL3 0	PGABVOL2 0	PGABVOL1 0	PGABVOL0 0
14h p 57	Passthru A Vol	PASSAVOL7 0	PASSAVOL6 0	PASSAVOL5 0	PASSAVOL4 0	PASSAVOL3 0	PASSAVOL2 0	PASSAVOL1 0	PASSAVOL0 0
15h p 57	Passthru B Vol	PASSBVOL7 0	PASSBVOL6 0	PASSBVOL5 0	PASSBVOL4 0	PASSBVOL3 0	PASSBVOL2 0	PASSBVOL1 0	PASSBVOL0 0
16h p 57	ADCA Vol	ADCAVOL7 0	ADCAVOL6 0	ADCAVOL5 0	ADCAVOL4 0	ADCAVOL3 0	ADCAVOL2 0	ADCAVOL1 0	ADCAVOL0 0
17h p 57	ADCB Vol	ADCBVOL7 0	ADCBVOL6 0	ADCBVOL5 0	ADCBVOL4 0	ADCBVOL3 0	ADCBVOL2 0	ADCBVOL1 0	ADCBVOL0 0
18h p 58	ADCMIXA Vol	AMIXAMUTE 1	AMIXAVOL6 0	AMIXAVOL5 0	AMIXAVOL4 0	AMIXAVOL3 0	AMIXAVOL2 0	AMIXAVOL1 0	AMIXAVOL0 0
19h p 58	ADCMIXB Vol	AMIXBMUTE 1	AMIXBVOL6 0	AMIXBVOL5 0	AMIXBVOL4 0	AMIXBVOL3 0	AMIXBVOL2 0	AMIXBVOL1 0	AMIXBVOL0 0
1Ah p 58	PCMMIXA Vol	PMIXAMUTE 0	PMIXAVOL6 0	PMIXAVOL5 0	PMIXAVOL4 0	PMIXAVOL3 0	PMIXAVOL2 0	PMIXAVOL1 0	PMIXAVOL0 0

IPC Address: 1001010[R/W] - 10010100 = 0x94(Write); 10010101 = 0x95(Read)									
Adr.	Function	7	6	5	4	3	2	1	0
1Bh p 58	PCMMIXB Vol	PMIXBMUTE 0	PMIXBVOL6 0	PMIXBVOL5 0	PMIXBVOL4 0	PMIXBVOL3 0	PMIXBVOL2 0	PMIXBVOL1 0	PMIXBVOL0 0
1Ch p 59	BEEP Freq, On Time	FREQ3 0	FREQ2 0	FREQ1 0	FREQ0 0	ONTIME3 0	ONTIME2 0	ONTIME1 0	ONTIME0 0
1Dh p 60	BEEP Vol, Off Time	OFFTIME2 0	OFFTIME1 0	OFFTIME0 0	BPVOL4 0	BPVOL3 0	BPVOL2 0	BPVOL1 0	BPVOL0 0
1Eh p 61	BEEP, Tone Cfg.	BEEP1 0	BEEP0 0	BEEPPIXDIS 0	TREB_CF1 0	TREB_CF0 0	BASS_CF1 0	BASS_CF0 0	TC_EN 0
1Fh p 62	Tone Ctl	TREB3 1	TREB2 0	TREB1 0	TREB0 0	BASS3 1	BASS2 0	BASS1 0	BASS0 0
20h p 63	Master A Vol	MSTAVOL7 0	MSTAVOL6 0	MSTAVOL5 0	MSTAVOL4 0	MSTAVOL3 0	MSTAVOL2 0	MSTAVOL1 0	MSTAVOL0 0
21h p 63	Master B Vol	MSTBVOL7 0	MSTBVOL6 0	MSTBVOL5 0	MSTBVOL4 0	MSTBVOL3 0	MSTBVOL2 0	MSTBVOL1 0	MSTBVOL0 0
22h p 63	Headphone A Volume	HPAVOL7 0	HPAVOL6 0	HPAVOL5 0	HPAVOL4 0	HPAVOL3 0	HPAVOL2 0	HPAVOL1 0	HPAVOL0 0
23h p 63	Headphone B Volume	HPBVOL7 0	HPBVOL6 0	HPBVOL5 0	HPBVOL4 0	HPBVOL3 0	HPBVOL2 0	HPBVOL1 0	HPBVOL0 0
24h p 64	Speaker A Volume	SPKAVOL7 0	SPKAVOL6 0	SPKAVOL5 0	SPKAVOL4 0	SPKAVOL3 0	SPKAVOL2 0	SPKAVOL1 0	SPKAVOL0 0
25h p 64	Speaker B Volume	SPKBVOL7 0	SPKBVOL6 0	SPKBVOL5 0	SPKBVOL4 0	SPKBVOL3 0	SPKBVOL2 0	SPKBVOL1 0	SPKBVOL0 0
26h p 64	Channel Mixer & Swap	PCMASWP1 0	PCMASWP0 0	PCMBSWP1 0	PCMBSWP0 0	ADCASWP1 0	ADCASWP0 0	ADCBSWP1 0	ADCBSWP0 0
27h p 65	Limit Ctl 1, Thresholds	LMAX2 0	LMAX1 0	LMAX0 0	CUSH2 0	CUSH1 0	CUSH0 0	LIMSRDIS 0	LIMZCDIS 0
28h p 66	Limit Ctl 2, Release Rate	LIMIT 0	LIMIT_ALL 1	LIMRRATE5 1	LIMRRATE4 1	LIMRRATE3 1	LIMRRATE2 1	LIMRRATE1 1	LIMRRATE0 1
29h p 67	Limiter Attack Rate	Reserved 1	Reserved 1	LIMARATE5 0	LIMARATE4 0	LIMARATE3 0	LIMARATE2 0	LIMARATE1 0	LIMARATE0 0
2Ah p 67	ALC Ctl 1, Attack Rate	ALCB 0	ALCA 0	ALCARATE5 0	AALCRATE4 0	ALCARATE3 0	ALCARATE2 0	ALCARATE1 0	ALCARATE0 0
2Bh p 68	ALC Release Rate	Reserved 0	Reserved 0	ALCRRATE5 1	ALCRRATE4 1	ALCRRATE3 1	ALCRRATE2 1	ALCRRATE1 1	ALCRRATE0 1
2Ch p 68	ALC Thresh- olds	ALCMAX2 0	ALCMAX1 0	ALCMAX0 0	ALCMIN2 0	ALCMIN1 0	ALCMIN0 0	Reserved 0	Reserved 0
2Dh p 69	Noise Gate Ctl	NGALL 0	NG 0	NGBOOST 0	THRESH2 0	THRESH1 0	THRESH0 0	NGDELAY1 0	NGDELAY0 0
2Eh p 70	Overflow & Clock Status	Reserved 0	SPCLKERR 0	DSPBOVFL 0	DSPAOVFL 0	PCMAOVFL 0	PCMBOVFL 0	ADCAOVFL 0	ADCBVFL 0
2Fh p 71	Battery Com- pensation	BATTCMP 0	VPMONITOR 0	Reserved 0	Reserved 0	VPREF3 0	VPREF2 0	VPREF1 0	VPREF0 0
30h p 72	VP Battery Level	VPLVL7 0	VPLVL6 0	VPLVL5 0	VPLVL4 0	VPLVL3 0	VPLVL2 0	VPLVL1 0	VPLVL0 0
31h p 72	Speaker Status	Reserved 0	Reserved 0	SPKASHRT 0	SPKBSHRT 0	SPKR/HP 0	Reserved 0	Reserved 0	Reserved 0
32h	Reserved	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 1	Reserved 0	Reserved 1	Reserved 1
33h	Reserved	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
34h p 73	Charge Pump Frequency	CHGFREQ3 0	CHGFREQ2 1	CHGFREQ1 0	CHGFREQ0 1	Reserved 1	Reserved 1	Reserved 1	Reserved 1

6. REGISTER DESCRIPTION

All registers are read/write except for the chip I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description. Unless otherwise specified, all “Reserved” bits must maintain their default value.

6.1 Chip I.D. and Revision Register (Address 01h) (Read Only)

7	6	5	4	3	2	1	0
CHIPID4	CHIPID3	CHIPID2	CHIPID1	CHIPID0	REVID2	REVID1	REVID0

6.1.1 Chip I.D. (Read Only)

I.D. code for the CS42L52.

CHIPID[4:0]	Device
11100	CS42L52

6.1.2 Chip Revision (Read Only)

CS42L52 revision level.

REVID[2:0]	Revision Level
000	A0
001	A1
010	B0
011	B1

6.2 Power Control 1 (Address 02h)

7	6	5	4	3	2	1	0
PDN_CHRG	Reserved	Reserved	PDN_PGAB	PDN_PGAA	PDN_ADCB	PDN_ADCA	PDN

6.2.1 Power Down ADC Charge Pump

Configures the power state of the ADC charge pump.

PDN_CHRG	ADC Charge Pump Status
0	Powered Up
1	Powered Down

6.2.2 Power Down PGAx

Configures the power state of PGA channel x.

PDN_PGAx	PGA Status
0	Powered Up (ONLY when the ADC or the analog passthru is used)
1	Powered Down
Application	“Analog In to Analog Out Passthrough” on page 32

Notes:

1. The CS42L52 employs a clever scheme for controlling the power to the PGA when PASSTHRU (“Passthrough Analog” on page 52) is enabled. Refer to the referenced application for more information.
2. This bit should be used in conjunction with ADCxSEL and PGAxSEL bits to determine the analog

input path. The PGAxSEL bits may be used to isolate the input signal(s) from the PGA outputs. When the PGA is powered down, no input should be selected. Refer to [“ADC Input Select” on page 48](#) and [“PGA Input Mapping” on page 49](#) for the required settings.

6.2.3 Power Down ADCx

Configures the power state of ADC channel x.

PDN_ADCx	ADC Status
0	Powered Up
1	Powered Down
Application	“Analog In to Analog Out Passthrough” on page 32

Notes:

1. The CS42L52 employs a clever scheme for controlling the power to the ADC when PASSTHRU ([“Passthrough Analog” on page 52](#)) and PDN_OVRD ([“Power Down ADC Override” on page 43](#)) are enabled. Refer to the referenced application.

6.2.4 Power Down

Configures the power state of the entire CODEC.

PDN	CODEC Status
0	Powered Up
1	Powered Down

6.3 Power Control 2 (Address 03h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	OVRDB	OVRDA	PDN_MICB	PDN_MICA	PDN_BIAS

6.3.1 Power Down ADC Override

Configures an override of the power down control for ADCx.

OVRDx	PDN_ADC Override
0	Disable
1	Enable
Application	“Analog In to Analog Out Passthrough” on page 32

6.3.2 Power Down MICx

Configures the power state of the microphone pre-amplifier for channel x.

PDN_MICx	MIC Pre-Amp Status
0	Powered Up
1	Powered Down
Application	“MIC Inputs” on page 27

6.3.3 Power Down MIC Bias

Configures the power state of the microphone bias circuit.

PDN_BIAS	MIC Bias Status
0	Powered Up
1	Powered Down

6.4 Power Control 3 (Address 04h)

7	6	5	4	3	2	1	0
PDN_HP B1	PDN_HP B0	PDN_HP A1	PDN_HP A0	PDN_SPK B1	PDN_SPK B0	PDN_SPK A1	PDN_SPK A0

6.4.1 Headphone Power Control

Configures how the SPKR/HP pin, 31, controls the power for the headphone amplifier.

PDN_HP x[1:0]	Headphone Status
00	Headphone channel is ON when the SPKR/HP pin, 31, is LO. Headphone channel is OFF when the SPKR/HP pin, 31, is HI.
01	Headphone channel is ON when the SPKR/HP pin, 31, is HI. Headphone channel is OFF when the SPKR/HP pin, 31, is LO.
10	Headphone channel is always ON.
11	Headphone channel is always OFF.

6.4.2 Speaker Power Control

Configures how the SPKR/HP pin, 31, controls the power for the speaker amplifier.

PDN_SPK x[1:0]	Speaker Status
00	Speaker channel is ON when the SPKR/HP pin, 31, is LO. Speaker channel is OFF when the SPKR/HP pin, 31, is HI.
01	Speaker channel is ON when the SPKR/HP pin, 31, is HI. Speaker channel is OFF when the SPKR/HP pin, 31, is LO.
10	Speaker channel is always ON.
11	Speaker channel is always OFF.

6.5 Clocking Control (Address 05h)

7	6	5	4	3	2	1	0
AUTO	SPEED1	SPEED0	32k_GROUP	VIDEOCLK	RATIO1	RATIO0	MCLKDIV2

6.5.1 Auto-Detect

Configures the auto-detect circuitry for detecting the speed mode of the CODEC when operating as a slave.

AUTO	Auto-detection of Speed Mode
0	Disabled
1	Enabled
Application:	"Serial Port Clocking" on page 34

Notes:

1. The SPEED[1:0] bits are ignored and speed is determined by the MCLK/LRCK ratio.
2. When AUTO is disabled and the CODEC operates in master mode, the MCLKDIV2 bit is ignored.
3. Certain sample and MCLK frequencies require setting the SPEED[1:0] bits, the 32k_GROUP bit ("[32kHz Sample Rate Group](#)" on page 45) and/or the VIDEOCLK bit ("[27 MHz Video Clock](#)" on page 45) and RATIO[1:0] bits ("[Internal MCLK/LRCK Ratio](#)" on page 45). Low sample rates may also affect dynamic range performance in the typical audio band. Refer to the referenced application for more information.

6.5.2 Speed Mode

Configures the speed mode of the CODEC in slave mode and sets the appropriate MCLK divide ratio for LRCK and SCLK in master mode.

SPEED[1:0]	Slave Mode	Master Mode	
	Serial Port Speed	MCLK/LRCK Ratio	SCLK/LRCK Ratio
00	Double-Speed Mode (DSM - 50 kHz - 100 kHz Fs)	512	64
01	Single-Speed Mode (SSM - 4 kHz - 50 kHz Fs)	256	64
10	Half-Speed Mode (HSM - 12.5kHz - 25 kHz Fs)	128	64
11	Quarter-Speed Mode (QSM - 4 kHz - 12.5 kHz Fs)	128	64
Application:	"Serial Port Clocking" on page 34		

Notes:

1. Slave/Master Mode is determined by the M/ \bar{S} bit in "Master/Slave Mode" on page 46.
2. Certain sample and MCLK frequencies require setting the SPEED[1:0] bits, the 32k_GROUP bit ("32kHz Sample Rate Group" on page 45) and/or the VIDEOCLK bit ("27 MHz Video Clock" on page 45) and RATIO[1:0] bits ("Internal MCLK/LRCK Ratio" on page 45). Low sample rates may also affect dynamic range performance in the typical audio band. Refer to the referenced application for more information.
3. These bits are ignored when the AUTO bit ("Auto-Detect" on page 44) is enabled.

6.5.3 32kHz Sample Rate Group

Specifies whether or not the input/output sample rate is 8 kHz, 16 kHz or 32 kHz.

32kGROUP	8 kHz, 16 kHz or 32 kHz sample rate?
0	No
1	Yes
Application:	"Serial Port Clocking" on page 34

6.5.4 27 MHz Video Clock

Specifies whether or not the external MCLK frequency is 27 MHz

VIDEOCLK	27 MHz MCLK?
0	No
1	Yes
Application:	"Serial Port Clocking" on page 34

6.5.5 Internal MCLK/LRCK Ratio

Configures the internal MCLK/LRCK ratio.

RATIO[1:0]	Internal MCLK Cycles per LRCK	SCLK/LRCK Ratio in Master Mode
00	128	64
01	125	62
10	132	66
11	136	68
Application:	"Serial Port Clocking" on page 34	

6.5.6 MCLK Divide By 2

Divides the input MCLK by 2 prior to all internal circuitry.

MCLKDIV2	MCLK signal into CODEC
0	No divide
1	Divided by 2
Application:	“Serial Port Clocking” on page 34

Note: In slave mode, this bit is ignored when the AUTO bit ([“Auto-Detect” on page 44](#)) is disabled.

6.6 Interface Control 1 (Address 06h)

7	6	5	4	3	2	1	0
M/S	INV_SCLK	ADCDIF	DSP	DACDIF1	DACDIF0	AWL1	AWL0

6.6.1 Master/Slave Mode

Configures the serial port I/O clocking.

M/S	Serial Port Clocks
0	Slave (input ONLY)
1	Master (output ONLY)

6.6.2 SCLK Polarity

Configures the polarity of the SCLK signal.

INV_SCLK	SCLK Polarity
0	Not Inverted
1	Inverted

6.6.3 ADC Interface Format

Configures the digital interface format for data on SDOOUT.

ADCDIF	ADC Interface Format
0	Left Justified
1	I ² S
Application:	“Digital Interface Formats” on page 36

6.6.4 DSP Mode

Configures a data-packed interface format for both the ADC and DAC.

DSP	DSP Mode
0	Disabled
1	Enabled
Application:	“DSP Mode” on page 36

Notes:

1. Select the audio word length using the AWL[1:0] bits ([“Audio Word Length” on page 47](#)).
2. The interface format for both the ADC and the DAC must be set to “Left-Justified” when DSP Mode is enabled.

6.6.5 DAC Interface Format

Configures the digital interface format for data on SDIN.

DACDIF[1:0]	DAC Interface Format
00	Left Justified, up to 24-bit data
01	I ² S, up to 24-bit data
10	Right Justified
11	Reserved
Application:	"Digital Interface Formats" on page 36

Note: Select the audio word length for Right Justified using the AWL[1:0] bits (["Audio Word Length" on page 47](#)).

6.6.6 Audio Word Length

Configures the audio sample word length used for the data into SDIN and out of SDOOUT.

AWL[1:0]	Audio Word Length	
	DSP Mode	Right Justified (DAC ONLY)
00	32-bit data	24-bit data
01	24-bit data	20-bit data
10	20-bit data	18-bit data
11	16-bit data	16-bit data
Application:	"DSP Mode" on page 36	

Note: When the internal MCLK/LRCK ratio is set to 125 in master mode, the 32-bit data width option for DSP Mode is not valid unless SCLK=MCLK.

6.7 Interface Control 2 (Address 07h)

7	6	5	4	3	2	1	0
Reserved	SCLK=MCLK	DIGLOOP	3ST_SP	INV_SWCH	BIASLVL2	BIASLVL1	BIASLVL0

6.7.1 SCLK equals MCLK

Configures the SCLK signal source for master mode.

SCLK=MCLK	Output SCLK
0	Re-timed signal, synchronously derived from MCLK
1	Non-retimed, MCLK signal

Note: This bit is only valid for MCLK = 12.0000 MHz.

6.7.2 SDOOUT to SDIN Digital Loopback

Configures an internal loops the signal on the SDOOUT pin to SDIN.

DIGLOOP	Internal Loopback
0	Disabled; SDOOUT internally disconnected from SDIN
1	Enabled; SDOOUT internally connected to SDIN

6.7.3 Tri-State Serial Port Interface

Determines the state of the serial port drivers.

3ST_SP	Serial Port Status	
	Slave Mode	Master Mode
0	Serial Port clocks are inputs and SDOUT is output	Serial Port clocks and SDOUT are outputs
1	Serial Port clocks are inputs and SDOUT is HI-Z	Serial Port clocks and SDOUT are HI-Z

Notes:

1. Slave/Master Mode is determined by the M/S bit in “Master/Slave Mode” on page 46.
2. When the serial port is tri-stated in master mode, the ADC and DAC serial ports are clocked internally.

6.7.4 Speaker/Headphone Switch Invert

Determines the control signal polarity of the SPK/HP_SW pin.

INV_SWCH	SPK/HP_SW pin 6 Control
0	Not inverted
1	Inverted

6.7.5 MIC Bias Level

Sets the output voltage level on the MICBIAS output pin.

BIASLVL[2:0]	Output Bias Level
000	0.5 x VA
001	0.6 x VA
010	0.7 x VA
011	0.8 x VA
100	0.83 x VA
101	0.91 x VA
110	Reserved
111	Reserved

6.8 Input x Select: ADCA and PGAA (Address 08h), ADCB and PGAB (Address 09h)

7	6	5	4	3	2	1	0
ADCASEL2	ADCASEL1	ADCASEL0	PGAASEL5	PGAASEL4	PGAASEL3	PGAASEL2	PGAASEL1

6.8.1 ADC Input Select

Selects the specified analog input signal into ADCx.

ADCxSEL[2:0]	Selected Input to ADCx
000	AIN1x
001	AIN2x
010	AIN3x
011	AIN4x
100	PGAx - Use PGAxSEL bits (“PGA Input Mapping” on page 49) to select input channels
101	Reserved
110	Reserved
111	Reserved
Application:	“Analog Inputs” on page 26

6.8.2 PGA Input Mapping

Selects one or sums/mixes the analog input signal into the PGA. Each bit of the PGAx_SEL[5:1] word corresponds to individual channels (i.e. PGAx_SEL1 selects AIN1x, PGAx_SEL2 selects AIN2x, etc.).

PGAxSEL[5:1]	Selected Input to PGAx (Examples)
00000	No inputs selected
00001	AIN1x
00010	AIN2x
00100	AIN3x
01000	AIN4x
10000	MICx; for single-ended MIC inputs, use MICxSEL ("MIC x Select" on page 55) to select MIC 1 or MIC 2; for differential MIC inputs, enable MICxCFG ("MICx Configuration" on page 55)
10001	MICx + AIN1x
10011	MICx + AIN1x + AIN2x
Application:	"Analog Inputs" on page 26

Note: Table does not show all possible combinations.

6.9 Analog & HPF Control (Address 0Ah)

7	6	5	4	3	2	1	0
HPFB	HPFRZB	HPFA	HPFRZA	ANLGSFTB	ANLGZCB	ANLGSFTA	ANLGZCA

6.9.1 ADCx High-Pass Filter

Configures the internal high-pass filter after ADCx.

HPFx	High Pass Filter Status
0	Disabled
1	Enabled

6.9.2 ADCx High-Pass Filter Freeze

Configures the high pass filter's digital DC subtraction and/or calibration after ADCx.

HPFRZx	High Pass Filter Digital Subtraction
0	Continuous DC Subtraction
1	Frozen DC Subtraction

6.9.3 Ch. x Analog Soft Ramp

Configures an incremental volume ramp from the current level to the new level at the specified rate.

ANLGSFTx	Volume Changes	Affected Analog Volume Controls
0	Do not occur with a soft ramp	MICxGAIN[4:0] ("MICx Gain" on page 55), PGAxVOL[5:0] ("PGAx Volume" on page 56), and PASSxVOL[7:0] ("Passthrough x Volume" on page 57)
1	Occur with a soft ramp	
Ramp Rate:	1/2 dB every 16 LRCK cycles	

6.9.4 Ch. x Analog Zero Cross

Configures when the signal level changes occur for the analog volume controls.

ANLGZCx	Volume Changes	Affected Analog Volume Controls
0	Do not occur on a zero crossing	MICxGAIN[4:0] ("MICx Gain" on page 55), PGAxVOL[5:0] ("PGAx Volume" on page 56), and PASSxVOL[7:0] ("Passthrough x Volume" on page 57)
1	Occur on a zero crossing	

Note: If the signal does not encounter a zero crossing, the requested volume change will occur after a timeout period of 1024 sample periods (approximately 10.7 ms at 48 kHz sample rate).

6.10 ADC HPF Corner Frequency (Address 0Bh)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	HPFB_CF1	HPFB_CF0	HPFA_CF1	HPFA_CF0

6.10.1 HPF x Corner Frequency

Sets the corner frequency (-3 dB point) for the internal High-Pass Filter (HPF).

HPFx_CF[1:0]	HPF Corner Frequency Setting ($F_s=48$ kHz)
00	Normal setting as specified in "ADC Digital Filter Characteristics" on page 14
01	119 Hz
10	236 Hz
11	464 Hz

6.11 Misc. ADC Control (Address 0Ch)

7	6	5	4	3	2	1	0
ADCB=A	DIGMUX	DIGSUM1	DIGSUM0	INV_ADCB	INV_ADCA	ADCBMUTE	ADCAMUTE

6.11.1 Analog Front-End Volume Setting B=A

Configures independent or ganged volume control and muting of the analog front end.

ADCB=A	Single Volume Control	Affected Volume Controls
0	Disabled	ADCxVOL[7:0] ("ADCx Volume" on page 57), ADCxMUTE ("ADC Mute" on page 51), ALC and Limiter Attack/Release (page 66 to page 68)
1	Enabled	MICxGAIN[4:0] ("MICx Gain" on page 55), PGAxVOL[5:0] ("PGAx Volume" on page 56), PASSxVOL[7:0] ("Passthrough x Volume" on page 57)

6.11.2 Digital MUX

Selects the signal source for the ADC serial port

DIGMUX	SDOUT Signal Source
0	ADC
1	DSP

6.11.3 Digital Sum

Configures a mix/swap of ADCA and ADCB.

DIGSUM[1:0]	Serial Output Signal	
	Left Channel	Right Channel
00	ADCA	ADCB
01	$(ADCA + ADCB)/2$	$(ADCA + ADCB)/2$
10	$(ADCA - ADCB)/2$	$(ADCA - ADCB)/2$
11	ADCB	ADCA

6.11.4 Invert ADC Signal Polarity

Configures the polarity of the ADC signal.

INV_ADCx	ADC Signal Polarity
0	Not Inverted
1	Inverted

6.11.5 ADC Mute

Configures a digital mute on ADC channel x.

ADCxMUTE	ADC Mute
0	Disabled
1	Enabled

Note: When the ADCxMUTE bit is enabled, the PGA will automatically apply 6 dB of attenuation.

6.12 Playback Control 1 (Address 0Dh)

7	6	5	4	3	2	1	0
HPGAIN2	HPGAIN1	HPGAIN0	PLYBCKB=A	INV_PCMB	INV_PCMA	MSTBMUTE	MSTAMUTE

6.12.1 Headphone Analog Gain

Selects the gain multiplier for the headphone/line outputs.

HPGAIN[2:0]	Headphone/Line Gain Setting (G)
000	0.3959
001	0.4571
010	0.5111
011	0.6047
100	0.7099
101	0.8399
110	1.000
111	1.1430

Note: Refer to [“Line Output Voltage Level Characteristics”](#) on page 20 and [“Headphone Output Power Characteristics”](#) on page 19.

6.12.2 Playback Volume Setting B=A

Configures independent or ganged volume control of all playback channels.

PLYBCKB=A	Single Volume Control	Affected Volume Controls
0	Disabled	HPxMUTE (“Playback Control 2 (Address 0Fh)” on page 54), AMIXxVOL[7:0] (“ADC Mixer Channel x Volume” on page 58), PMIXxVOL[7:0] (“PCM Mixer Channel x Volume” on page 58), MSTxVOL[7:0] (“Master Volume Control” on page 63), HPxVOL[7:0] (“Headphone Volume Control” on page 63)
1	Enabled	

6.12.3 Invert PCM Signal Polarity

Configures the polarity of the digital input signal.

INV_PCMx	PCM Signal Polarity
0	Not Inverted
1	Inverted

6.12.4 Master Playback Mute

Configures a digital mute on the master volume control for channel x.

MSTxMUTE	Master Mute
0	Not Inverted
1	Inverted

Note: The muting function is affected by the DIGSFT (“Digital Soft Ramp” on page 53) and DIGZC (“Digital Zero Cross” on page 53) bits.

6.13 Miscellaneous Controls (Address 0Eh)

7	6	5	4	3	2	1	0
PASSTRUB	PASSTRUA	PASSBMUTE	PASSAMUTE	FREEZE	DEEMPH	DIGSFT	DIGZC

6.13.1 Passthrough Analog

Configures an analog passthrough from the PGA inputs to the headphone/line outputs.

PASSTRUx	Analog In Routed to HP/Line Output
0	Disabled
1	Enabled

Notes:

1. The Passthrough volume control is realized using a combination of the PGA volume control settings (“PGAx Volume” on page 56) and the headphone amplifier volume control settings (hidden). When passthrough is enabled and the PGA to ADC path is selected, the signal seen by the ADC will change depending on the passthrough volume setting.

6.13.2 Passthrough Mute

Configures an analog mute on the channel x analog in to analog out passthrough.

PASSxMUTE	Passthrough Mute
0	Disabled
1	Enabled

6.13.3 Freeze Registers

Configures a hold on all register settings.

FREEZE	Control Port Status
0	Register changes take effect immediately
1	Modifications may be made to all control port registers without the changes taking effect until after the FREEZE is disabled.

6.13.4 HP/Speaker De-emphasis

Configures a 15 μ s/50 μ s digital de-emphasis filter response on the headphone/line and speaker outputs.

DEEMPHASIS	Control Port Status
0	Disabled
1	Enabled

6.13.5 Digital Soft Ramp

Configures an incremental volume ramp from the current level to the new level at the specified rate.

DIGSFT	Volume Changes	Affected Digital Volume Controls
0	Do not occur with a soft ramp	MSTxMUTE (“ Master Playback Mute ” on page 52), HPxMUTE, SPKxMUTE (“ Playback Control 2 (Address 0Fh) ” on page 54), ADCxVOL[7:0] (“ ADCx Volume ” on page 57), AMIXxMUTE, AMIXxVOL[7:0] (“ ADC Mixer Channel x Volume ” on page 58), PMIXxMUTE, PMIXxVOL[7:0] (“ PCM Mixer Channel x Volume ” on page 58), MSTxVOL[7:0] (“ Master Volume Control ” on page 63), HPxVOL[7:0] (“ Headphone Volume Control ” on page 63), SPKxVOL[7:0] (“ Speaker Volume Control ” on page 64), ALC and Limiter Attack/Release (page 66 to page 68) Beep Volume (“ Beep Volume ” on page 61)
1	Occur with a soft ramp	
Ramp Rate:	1/8 dB every LRCK cycle	

Notes:

1. When the DIGSFT bit is enabled, the Master Volume (MSTxVOL[7:0]) transitions are guaranteed to occur with a soft ramp only when bits 7 and 6 in register 29h are set to ‘00’b.

6.13.6 Digital Zero Cross

Configures when the signal level changes occur for the digital volume controls.

DIGZC	Volume Changes	Affected Digital Volume Controls
0	Do not occur on a zero crossing	MSTxMUTE (“ Master Playback Mute ” on page 52), AMIXxMUTE, AMIXxVOL[7:0] (“ ADC Mixer Channel x Volume ” on page 58), PMIXxMUTE, PMIXxVOL[7:0] (“ PCM Mixer Channel x Volume ” on page 58), MSTxVOL[7:0] (“ Master Volume Control ” on page 63), ALC and Limiter Attack/Release (page 66 to page 68) Beep Volume (“ Beep Volume ” on page 61)
1	Occur on a zero crossing	

Notes:

1. If the signal does not encounter a zero crossing, the requested volume change will occur after a timeout period between 1024 and 2048 sample periods (21.3 ms to 42.7 ms at 48 kHz sample rate).
2. The zero cross function is independently monitored and implemented for each channel.
3. The DIS_LIMSFT bit (“[Limiter Soft Ramp Disable](#)” on page 65) is ignored when zero cross is enabled.
4. When the DIGSFT bit is enabled, the Master Volume (MSTxVOL[7:0]) transitions are guaranteed to occur on a zero crossing only when bits 7 and 6 in register 29h are set to ‘00’b.

6.14 Playback Control 2 (Address 0Fh)

7	6	5	4	3	2	1	0
HPBMUTE	HPAMUTE	SPKBMUTE	SPKAMUTE	SPKB=A	SPKSWAP	SPKMONO	MUTE50/50

6.14.1 Headphone Mute

Configures a digital mute on headphone channel x.

HPxMUTE	Headphone Mute
0	Disabled
1	Enabled

6.14.2 Speaker Mute

Configures a digital mute on speaker channel x.

SPKxMUTE	Speaker Mute
0	Disabled
1	Enabled

6.14.3 Speaker Volume Setting B=A

Configures independent or ganged volume control of the speaker output.

SPKB=A	Single Volume Control	Affected Volume Controls
0	Disabled	SPKxMUTE (“Speaker Mute” on page 54),
1	Enabled	SPKxVOL[7:0] (“Speaker Volume Control” on page 64)

6.14.4 Speaker Channel Swap

Configures a channel swap on the speaker channels.

SPKSWAP	Speaker Output
0	Channel A
1	Channel B
Application:	“Mono Speaker Output Configuration” on page 33

6.14.5 Speaker MONO Control

Configures a parallel full-bridge output for the speaker channels.

SPKMONO	Parallel Full Bridge Output
0	Disabled
1	Enabled
Application:	“Mono Speaker Output Configuration” on page 33

6.14.6 Speaker Mute 50/50 Control

Configures how the speaker channels mute.

MUTE50/50	Speaker Mute 50/50
0	Disabled; The PWM amplifiers outputs modulated silence when SPKxMUTE is enabled.
1	Enabled; The PWM amplifiers switch at an exact 50%-duty-cycle signal (not modulated) when SPKxMUTE is enabled.

6.15 MICx Amp Control: MIC A (Address 10h) & MIC B (Address 11h)

7	6	5	4	3	2	1	0
Reserved	MICxSEL	MICxCFG	MICxGAIN4	MICxGAIN3	MICxGAIN2	MICxGAIN1	MICxGAIN0

6.15.1 MIC x Select

Selects one of two single-ended MIC inputs on channel x.

MICxSEL	MIC x Selection
0	MIC 1x
1	MIC 2x
Application:	"MIC Inputs" on page 27

6.15.2 MICx Configuration

Configures the input topology for MICx.

MICxCFG	MIC Input Topology
0	Single-Ended
1	Differential
Application:	"MIC Inputs" on page 27

6.15.3 MICx Gain

Sets the gain of the microphone pre-amplifier.

MICxGAIN[4:0]	Gain
1 1111	32 dB
...	...
1 0000	32 dB
0 1111	30.5 dB
0 1110	30 dB
...	...
0 0000	16 dB
Step Size:	1 dB (unless otherwise noted)
Application:	"MIC Inputs" on page 27

**6.16 PGAx Vol. & ALCx Transition Ctl.:
ALC, PGA A (Address 12h) & ALC, PGA B (Address 13h)**

7	6	5	4	3	2	1	0
ALCxSRDIS	ALCxZCDIS	PGAxVOL5	PGAxVOL4	PGAxVOL3	PGAxVOL2	PGAxVOL1	PGAxVOL0

6.16.1 ALCx Soft Ramp Disable

Configures an override of the analog soft ramp setting.

ALCxSRDIS	ALC Soft Ramp Disable
0	OFF; ALC Attack Rate is dictated by the ANLGSFT (" Ch. x Analog Soft Ramp " on page 49) setting
1	ON; ALC volume changes take effect in one step, regardless of the ANLGSFT setting.
Application:	"Automatic Level Control (ALC)" on page 27

6.16.2 ALCx Zero Cross Disable

Configures an override of the analog zero cross setting.

ALCxZCDIS	ALC Zero Cross Disable
0	OFF; ALC Attack Rate is dictated by the ANLGZC ("Ch. x Analog Zero Cross" on page 49) setting
1	ON; ALC volume changes take effect at any time, regardless of the ANLGZC setting.
Application:	"Automatic Level Control (ALC)" on page 27

6.16.3 PGAx Volume

Sets the volume/gain of the Programmable Gain Amplifier (PGA).

PGAxVOL[5:0]	Volume
01 1111	12 dB
...	...
01 1000	12 dB
...	...
00 0001	+0.5 dB
00 0000	0 dB
11 1111	-0.5 dB
...	...
10 1000	-6.0 dB
...	...
10 0000	-6.0 dB
Step Size:	0.5 dB

Note: The PGAxVOL bits are ignored when the PASSTHRUx bit (["Passthrough Analog" on page 52](#)) is enabled.

6.17 Passthrough x Volume: PASSAVOL (Address 14h) & PASSBVOL (Address 15h)

7	6	5	4	3	2	1	0
PASSxVOL7	PASSxVOL6	PASSxVOL5	PASSxVOL4	PASSxVOL3	PASSxVOL2	PASSxVOL1	PASSxVOL0

6.17.1 Passthrough x Volume

Sets the volume/gain of the signal routed from the PGA to the headphone/line output.

PASSxVOL[7:0]	Gain
0111 1111	12 dB
...	...
0001 1000	12 dB
...	...
0000 0001	+0.5 dB
0000 0000	0 dB
11111 1111	-0.5 dB
...	...
1000 1000	-60.0 dB
...	...
1000 0000	-60.0 dB
Step Size:	0.5 dB (approximate)
Application:	"Analog In to Analog Out Passthrough" on page 32

Notes:

1. This register is ignored when the PASSTHRUx bit ("[Passthrough Analog](#)" on page 52) is disabled.
2. The step size may deviate from 0.5 dB at settings below -40 dB. Code settings 0x95, 0xA1, 0xAD, and 0xB9 are not guaranteed to be monotonic.

6.18 ADCx Volume Control: ADCAVOL (Address 16h) & ADCBVOL (Address 17h)

7	6	5	4	3	2	1	0
ADCAVOL7	ADCAVOL6	ADCAVOL5	ADCAVOL4	ADCAVOL3	ADCAVOL2	ADCAVOL1	ADCAVOL0

6.18.1 ADCx Volume

Sets the volume of the ADC signal out the serial data output (SDOUT).

ADCxVOL[7:0]	Volume
0111 1111	24 dB
...	...
0001 1000	24 dB
...	...
0000 0000	0 dB
1111 1111	-1.0 dB
1111 1110	-2.0 dB
...	...
1010 0000	-96.0 dB
...	...
1000 0000	-96.0 dB
Step Size:	1.0 dB

6.19 ADCx Mixer Volume: ADCA (Address 18h) & ADCB (Address 19h)

7	6	5	4	3	2	1	0
AMIXxMUTE	AMIXxVOL6	AMIXxVOL5	AMIXxVOL4	AMIXxVOL3	AMIXxVOL2	AMIXxVOL1	AMIXxVOL0

6.19.1 ADC Mixer Channel x Mute

Configures a digital mute on the ADC mix in the DSP.

AMIXxMUTE	ADC Mixer Mute
0	Disabled
1	Enabled

6.19.2 ADC Mixer Channel x Volume

Sets the volume/gain of the ADC mix in the DSP.

AMIXxVOL[6:0]	Volume
001 1000	+12.0 dB
...	...
000 0001	+0.5 dB
000 0000	0 dB
111 1111	-0.5 dB
...	...
001 1001	-51.5 dB
Step Size:	0.5 dB

6.20 PCMx Mixer Volume: PCMA (Address 1Ah) & PCMB (Address 1Bh)

7	6	5	4	3	2	1	0
PMIXxMUTE	PMIXxVOL6	PMIXxVOL5	PMIXxVOL4	PMIXxVOL3	PMIXxVOL2	PMIXxVOL1	PMIXxVOL0

6.20.1 PCM Mixer Channel x Mute

Configures a digital mute on the PCM mix from the serial data input (SDIN) to the DSP.

PMIXxMUTE	PCM Mixer Mute
0	Disabled
1	Enabled

6.20.2 PCM Mixer Channel x Volume

Sets the volume/gain of the PCM mix from the serial data input (SDIN) to the DSP.

PMIXxVOL[6:0]	Volume
001 1000	+12.0 dB
...	...
000 0001	+0.5 dB
000 0000	0 dB
111 1111	-0.5 dB
...	...
001 1001	-51.5 dB
Step Size:	0.5 dB

6.21 Beep Frequency & On Time (Address 1Ch)

7	6	5	4	3	2	1	0
FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0

6.21.1 Beep Frequency

Sets the frequency of the beep signal.

FREQ[3:0]	Frequency ($F_s = 12, 24, 48$ or 96 kHz)	Pitch
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5
0101	774.19 Hz	G5
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7
Application:	"Beep Generator" on page 30	

Notes:

1. This setting must not change when BEEP is enabled.
2. Beep frequency will scale directly with sample rate, F_s , but is fixed at the nominal F_s within each speed mode.

6.21.2 Beep On Time

Sets the on duration of the beep signal.

ONTIME[3:0]	On Time ($F_s = 12, 24, 48$ or 96 kHz)
0000	~86 ms
0001	~430 ms
0010	~780 ms
0011	~1.20 s
0100	~1.50 s
0101	~1.80 s
0110	~2.20 s
0111	~2.50 s
1000	~2.80 s
1001	~3.20 s
1010	~3.50 s
1011	~3.80 s
1100	~4.20 s
1101	~4.50 s
1110	~4.80 s
1111	~5.20 s
Application:	"Beep Generator" on page 30

Notes:

1. This setting must not change when BEEP is enabled.
2. Beep on time will scale inversely with sample rate, F_s , but is fixed at the nominal F_s within each speed mode.

6.22 Beep Volume & Off Time (Address 1Dh)

7	6	5	4	3	2	1	0
OFFTIME2	OFFTIME1	OFFTIME0	BPVOL4	BPVOL3	BPVOL2	BPVOL1	BPVOL0

6.22.1 Beep Off Time

Sets the off duration of the beep signal.

OFFTIME[2:0]	Off Time ($F_s = 48$ or 96 kHz)
000	~1.23 s
001	~2.58 s
010	~3.90 s
011	~5.20 s
100	~6.60 s
101	~8.05 s
110	~9.35 s
111	~10.80 s
Application:	"Beep Generator" on page 30

Notes:

1. This setting must not change when BEEP is enabled.
2. Beep off time will scale inversely with sample rate, F_s , but is fixed at the nominal F_s within each speed mode.

6.22.2 Beep Volume

Sets the volume of the beep signal.

BEEPVOL[4:0]	Gain
00110	+6.0 dB
...	...
00000	-6 dB
11111	-8 dB
11110	-10 dB
...	...
00111	-56 dB
Step Size:	2 dB
Application:	"Beep Generator" on page 30

Note: This setting must not change when BEEP is enabled.

6.23 Beep & Tone Configuration (Address 1Eh)

7	6	5	4	3	2	1	0
BEEP1	BEEP0	BEEPMIXDIS	TREBCF1	TREBCF0	BASSCF1	BASSCF0	TCEN

6.23.1 Beep Configuration

Configures a beep mixed with the HP/Line and SPK output.

BEEP[1:0]	Beep Occurrence
00	Off
01	Single
10	Multiple
11	Continuous
Application:	"Beep Generator" on page 30

Notes:

1. When used in analog pass-through mode, the output alternates between the signal from the PGA and the beep signal. The beep signal does not mix with the analog signal from the PGA.
2. Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration.

6.23.2 Beep Mix Disable

Configures how the beep mixes with the serial data input.

BEEPMIXDIS	Beep Output to HP/Line and Speaker
0	Mix Enabled; The beep signal mixes with the digital signal from the serial data input.
1	Mix Disabled; The output alternates between the signal from the serial data input and the beep signal. The beep signal does not mix with the digital signal from the serial data input.
Application:	"Beep Generator" on page 30

Note: This setting must not change when BEEP is enabled.

6.23.3 Treble Corner Frequency

Sets the corner frequency (-3 dB point) for the treble shelving filter.

TREBCF[1:0]	Treble Corner Frequency Setting
00	5 kHz
01	7 kHz
10	10 kHz
11	15 kHz

6.23.4 Bass Corner Frequency

Sets the corner frequency (-3 dB point) for the bass shelving filter.

BASSCF[1:0]	Bass Corner Frequency Setting
00	50 Hz
01	100 Hz
10	200 Hz
11	250 Hz

6.23.5 Tone Control Enable

Configures the treble and bass activation.

TCEN	Bass and Treble Control
0	Disabled
1	Enabled
Application:	"Beep Generator" on page 30

6.24 Tone Control (Address 1Fh)

7	6	5	4	3	2	1	0
TREB3	TREB2	TREB1	TREB0	BASS3	BASS2	BASS1	BASS0

6.24.1 Treble Gain

Sets the gain of the treble shelving filter.

TREB[3:0]	Gain Setting
0000	+12.0 dB
...	...
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
...	...
1111	-10.5 dB
Step Size:	1.5 dB

6.24.2 Bass Gain

Sets the gain of the bass shelving filter.

TREB[3:0]	Gain Setting
0000	+12.0 dB
...	...
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
...	...
1111	-10.5 dB
Step Size:	1.5 dB

6.25 Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h)

7	6	5	4	3	2	1	0
MSTxVOL7	MSTxVOL6	MSTxVOL5	MSTxVOL4	MSTxVOL3	MSTxVOL2	MSTxVOL1	MSTxVOL0

6.25.1 Master Volume Control

Sets the volume of the signal out the DSP.

MSTxVOL[7:0]	Master Volume
0001 1000	+12.0 dB
...	...
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-102 dB
...	...
0001 1001	-102 dB
Step Size:	0.5 dB

6.26 Headphone Volume Control: HPA (Address 22h) & HPB (Address 23h)

7	6	5	4	3	2	1	0
HPxVOL7	HPxVOL6	HPxVOL5	HPxVOL4	HPxVOL3	HPxVOL2	HPxVOL1	HPxVOL0

6.26.1 Headphone Volume Control

Sets the volume of the signal out the DAC.

HPxVOL[7:0]	Headphone Volume
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0011 0100	-96.0 dB
...	...
0000 0001	Muted
Step Size:	0.5 dB

6.27 Speaker Volume Control: SPKA (Address 24h) & SPKB (Address 25h)

7	6	5	4	3	2	1	0
SPKxVOL7	SPKxVOL6	SPKxVOL5	SPKxVOL4	SPKxVOL3	SPKxVOL2	SPKxVOL1	SPKxVOL0

6.27.1 Speaker Volume Control

Sets the volume of the signal out the PWM modulator.

SPKxVOL[7:0]	Speaker Volume
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
...	...
0100 0000	-96.0 dB
...	...
0000 0001	Muted
Step Size:	0.5 dB

Note: The maximum step size error is ± 0.15 dB.

6.28 ADC & PCM Channel Mixer (Address 26h)

7	6	5	4	3	2	1	0
PCMASWP1	PCMASWP0	PCMBSWP1	PCMBSWP0	ADCASWP1	ADCASWP0	ADCBSWP1	ADCBSWP0

6.28.1 PCM Mix Channel Swap

Configures a mix/swap of the PCM Mix to the headphone/line or speaker outputs.

PCMxSWP[1:0]	PCM Mix to HP/LINEOUTA	PCM Mix to HP/LINEOUTB
00	Left	Right
01	(Left + Right)/2	(Left + Right)/2
10		
11	Right	Left

6.28.2 ADC Mix Channel Swap

Configures a mix/swap of the ADC Mix to the headphone/line or speaker outputs.

ADCxSWP[1:0]	ADC Mix to HP/LINEOUTA Channel	ADC Mix to HP/LINEOUTB Channel
00	Left	Right
01	(Left + Right)/2	(Left + Right)/2
10		
11	Right	Left

6.29 Limiter Control 1, Min/Max Thresholds (Address 27h)

7	6	5	4	3	2	1	0
LMAX2	LMAX1	LMAX0	CUSH2	CUSH1	CUSH0	LIMSRDIS	LIMZCDIS

6.29.1 Limiter Maximum Threshold

Sets the maximum level, below full scale, at which to limit and attenuate the output signal at the attack rate (LIMARATE - [“Limiter Release Rate” on page 66](#)).

LMAX[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB
Application:	“Limiter” on page 31

Note: Bass, Treble, and digital gain settings that boost the signal beyond the maximum threshold may trigger an attack.

6.29.2 Limiter Cushion Threshold

Sets the minimum level at which to disengage the Limiter’s attenuation at the release rate (LIMRRATE - [“Limiter Release Rate” on page 66](#)) until levels lie between the LMAX and CUSH thresholds.

CUSH[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB
Application:	“Limiter” on page 31

Note: This setting is usually set slightly below the LMAX threshold.

6.29.3 Limiter Soft Ramp Disable

Configures an override of the digital soft ramp setting.

LIMSRDIS	Limiter Soft Ramp Disable
0	OFF; Limiter Attack Rate is dictated by the DIGSFT (“Digital Soft Ramp” on page 53) setting
1	ON; Limiter volume changes take effect in one step, regardless of the DIGSFT setting.
Application:	“Limiter” on page 31

Note: This bit is ignored when the DIGZC ([“Digital Zero Cross” on page 53](#)) is enabled.

6.29.4 Limiter Zero Cross Disable

Configures an override of the digital zero-cross setting.

LIMZCDIS	Limiter Zero Cross Disable
0	OFF; Limiter Attack Rate is dictated by the DIGZC (“Digital Zero Cross” on page 53) setting
1	ON; Limiter volume changes take effect in one step, regardless of the DIGZC setting.
Application:	“Limiter” on page 31

6.30 Limiter Control 2, Release Rate (Address 28h)

7	6	5	4	3	2	1	0
LIMIT	LIMIT_ALL	LIMRRATE5	LIMRRATE4	LIMRRATE3	LIMRRATE2	LIMRRATE1	LIMRRATE0

6.30.1 Peak Detect and Limiter

Configures the peak-detect and limiter circuitry.

LIMIT	Limiter Status
0	Disabled
1	Enabled
Application:	“Limiter” on page 31

6.30.2 Peak Signal Limit All Channels

Sets how channels are attenuated when the limiter is enabled.

LIMIT_ALL	Limiter action:
0	Apply the necessary attenuation on a specific channel only when the signal amplitude on <i>that</i> specific channel rises above LMAX. Remove attenuation on a specific channel only when the signal amplitude on <i>that</i> specific channel falls below CUSH.
1	Apply the necessary attenuation on BOTH channels when the signal amplitude on any ONE channel rises above LMAX. Remove attenuation on BOTH channels only when the signal amplitude on BOTH channels fall below CUSH.
Application:	“Limiter” on page 31

6.30.3 Limiter Release Rate

Sets the rate at which the limiter releases the digital attenuation from levels below the CUSH[2:0] threshold ([“Limiter Cushion Threshold” on page 65](#)) and returns the analog output level to the MSTxVOL[7:0] ([“Master Volume Control” on page 63](#)) setting.

LIMRRATE[5:0]	Release Time
00 0000	Fastest Release
...	...
11 1111	Slowest Release
Application:	“Limiter” on page 31

Note: The limiter release rate is user-selectable but is also a function of the sampling frequency, Fs, and the DIGSFT ([“Digital Soft Ramp” on page 53](#)) and DIGZC ([“Digital Zero Cross” on page 53](#)) setting.

6.31 Limiter Attack Rate (Address 29h)

7	6	5	4	3	2	1	0
Reserved	Reserved	LIMARATE5	LIMARATE4	LIMARATE3	LIMARATE2	LIMARATE1	LIMARATE0

6.31.1 Limiter Attack Rate

Sets the rate at which the limiter applies digital attenuation from levels above the MAX[2:0] threshold (“Limiter Maximum Threshold” on page 65).

LIMARATE[5:0]	Attack Time
00 0000	Fastest Attack
...	...
11 1111	Slowest Attack
Application:	“Limiter” on page 31

Note: The limiter attack rate is user-selectable but is also a function of the sampling frequency, F_s , and the DIGSFT (“Digital Soft Ramp” on page 53) and DIGZC (“Digital Zero Cross” on page 53) setting unless the respective disable bit (“Limiter Soft Ramp Disable” on page 65 or “Limiter Zero Cross Disable” on page 66) is enabled.

6.32 ALC Enable & Attack Rate (Address 2Ah)

7	6	5	4	3	2	1	0
ALCB	ALCA	ALCARATE5	AALCRATE4	ALCARATE3	ALCARATE2	ALCARATE1	ALCARATE0

6.32.1 ALCx Enable

Configures the automatic level controller.

ALC	ALC Status
0	Disabled
1	Enabled
Application:	“Automatic Level Control (ALC)” on page 27

Note: The ALC is not available in passthrough mode.

6.32.2 ALC Attack Rate

Sets the rate at which the ALC applies analog and/or digital attenuation from levels above the AMAX[2:0] threshold (“ALC Maximum Threshold” on page 68).

LIMARATE[5:0]	Attack Time
00 0000	Fastest Attack
...	...
11 1111	Slowest Attack
Application:	“Automatic Level Control (ALC)” on page 27

Note: The ALC attack rate is user-selectable but is also a function of the sampling frequency, F_s , and the ANLGSFTx (“Ch. x Analog Soft Ramp” on page 49) and ANLGZCx (“Ch. x Analog Zero Cross” on page 49) setting unless the respective disable bit (“ALCx Soft Ramp Disable” on page 55 or “ALCx Zero Cross Disable” on page 56) is enabled.

6.33 ALC Release Rate (Address 2Bh)

7	6	5	4	3	2	1	0
Reserved	Reserved	ALCRRATE5	ALCRRATE4	ALCRRATE3	ALCRRATE2	ALCRRATE1	ALCRRATE0

6.33.1 ALC Release Rate

Sets the rate at which the ALC releases the analog and/or digital attenuation from levels below the MIN[2:0] threshold ([“ALC Minimum Threshold” on page 69](#)) and returns the signal level to the PGAX-VOL[5:0] ([“PGAx Volume” on page 56](#)) and ADCxVOL[7:0] ([“ADCx Volume” on page 57](#)) setting.

ALCRRATE[5:0]	Release Time
00 0000	Fastest Release
...	...
11 1111	Slowest Release
Application:	“Automatic Level Control (ALC)” on page 27

Notes:

1. The ALC release rate is user-selectable but is also a function of the sampling frequency, Fs, and the ANLGSFTx ([“Ch. x Analog Soft Ramp” on page 49](#)) and ANLGZCx ([“Ch. x Analog Zero Cross” on page 49](#)) setting.
2. The Release Rate setting must always be slower than the Attack Rate.

6.34 ALC Threshold (Address 2Ch)

7	6	5	4	3	2	1	0
ALCMAx2	ALCMAx1	ALCMAx0	ALCMIx2	ALCMIx1	ALCMIx0	Reserved	Reserved

6.34.1 ALC Maximum Threshold

Sets the maximum level, below full scale, at which to limit and attenuate the input signal at the attack rate (ALCARATE - [“ALC Attack Rate” on page 67](#)).

MAX[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB
Application:	“Automatic Level Control (ALC)” on page 27

6.34.2 ALC Minimum Threshold

Sets the minimum level at which to disengage the ALC's attenuation or amplify the input signal at the release rate (ALCRRATE - [“ALC Release Rate” on page 68](#)) until levels lie between the ALCMAX and ALCMIN thresholds.

ALCMIN[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB
Application:	“Automatic Level Control (ALC)” on page 27

Notes:

1. This setting is usually set slightly below the ALCMAX threshold.

6.35 Noise Gate Control (Address 2Dh)

7	6	5	4	3	2	1	0
NGALL	NG	NG_BOOST	THRESH2	THRESH1	THRESH0	NGDELAY1	NGDELAY0

6.35.1 Noise Gate All Channels

Sets which channels are attenuated when clipping on any single channel occurs.

NGALL	Noise Gate triggered by:
0	Individual channel; Any channel that falls below the threshold setting triggers the noise gate attenuation for both channels.
1	Both channels A & B; Both channels must fall below the threshold setting for the noise gate attenuation to take effect.
Application:	“Noise Gate” on page 28

6.35.2 Noise Gate Enable

Configures the noise gate.

NG	Noise Gate Status
0	Disabled
1	Enabled
Application:	“Noise Gate” on page 28

6.35.3 Noise Gate Threshold and Boost

THRESH sets the threshold level of the noise gate. Input signals below the threshold level will be attenuated to -96 dB. NG_BOOST configures a +30 dB boost to the threshold settings.

THRESH[2:0]	Minimum Setting (NG_BOOST = '0'b)	Minimum Setting (NG_BOOST = '1'b)
000	-64 dB	-34 dB
001	-67 dB	-37 dB
010	-70 dB	-40 dB
011	-73 dB	-43 dB
100	-76 dB	-46 dB
101	-82 dB	-52 dB
110	Reserved	-58 dB
111	Reserved	-64 dB
Application:	"Noise Gate" on page 28	

6.35.4 Noise Gate Delay Timing

Sets the delay time before the noise gate attacks.

NGDELAY[1:0]	Delay Setting
00	50 ms
01	100 ms
10	150 ms
11	200 ms
Application:	"Noise Gate" on page 28

Note: The Noise Gate attack rate is a function of the sampling frequency, F_s , and the ANLGSFTx ("Ch. x Analog Soft Ramp" on page 49) and ANLGZCx ("Ch. x Analog Zero Cross" on page 49) setting unless the respective disable bit ("ALCx Soft Ramp Disable" on page 55 or "ALCx Zero Cross Disable" on page 56) is enabled.

6.36 Status (Address 2Eh) (Read Only)

For all bits in this register, a "1" means the associated error condition has occurred at least once since the register was last read. A "0" means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0.

7	6	5	4	3	2	1	0
Reserved	SPCLKERR	DSPAOVFL	DSPBOVFL	PCMAOVFL	PCMBOVFL	ADCAOVFL	ADCBVFL

6.36.1 Serial Port Clock Error (Read Only)

Indicates the status of the MCLK to LRCK ratio.

SPCLKERR	Serial Port Clock Status:
0	MCLK/LRCK ratio is valid.
1	MCLK/LRCK ratio is not valid.
Application:	"Serial Port Clocking" on page 34

Note: On initial power up and application of clocks, this bit will report '1'b as the serial port re-synchronizes.

6.36.2 DSP Engine Overflow (Read Only)

Indicates the over-range status in the DSP data path.

DSPxOVFL	DSP Overflow Status:
0	No digital clipping has occurred in the data path after the DSP.
1	Digital clipping has occurred in the data path after the DSP.
Application:	"Analog Outputs" on page 29

6.36.3 PCMx Overflow (Read Only)

Indicates the over-range status in the PCM mix data path.

PCMxOVFL	PCM Overflow Status:
0	No digital clipping has occurred in the data path of the PCM mix ("PCM Mixer Channel x Volume" on page 58) of the DSP.
1	Digital clipping has occurred in the data path of the PCM mix of the DSP.
Application:	"Analog Outputs" on page 29

6.36.4 ADCx Overflow (Read Only)

Indicates the over-range status in the ADC signal path.

ADCxOVFL	ADC Overflow Status:
0	No clipping has occurred anywhere in the ADC signal path.
1	Clipping has occurred in the ADC signal path.
Application:	"Analog Inputs" on page 26

6.37 Battery Compensation (Address 2Fh)

7	6	5	4	3	2	1	0
BATTCMP	VPMONITOR	Reserved	Reserved	VPREF3	VPREF2	VPREF1	VPREF0

6.37.1 Battery Compensation

Configures automatic adjustment of the speaker volume when VP deviates from VPREF[3:0].

BATTCMP	Automatic Battery Compensation
0	Disabled
1	Enabled
Application:	"Maintaining a Desired Output Level" on page 34

6.37.2 VP Monitor

Configures the internal ADC that monitors the VP voltage level.

VPMONITOR	VP ADC Status
0	Disabled
1	Enabled

Notes:

1. The internal ADC that monitors the VP supply is enabled automatically when BATTCMP is enabled, regardless of the VPMONITOR setting. Conversely, when BATTCMP is disabled, the ADC may be enabled by enabling VPMONITOR; this provides a convenient battery monitor without enabling battery compensation.
2. When enabled, VPMONITOR remains enabled regardless of the PDN bit setting.

6.37.3 VP Reference

Sets the desired VP reference used for battery compensation.

VPREF[3:0]	Desired VP used to calculate the required attenuation on the speaker output: (for VA = 1.8 V)
0000	1.5 V
0001	2.0 V
0010	2.5 V
0011	3.0 V
0100	3.5 V
0101	4.0 V
0110	4.5 V
0111	5.0 V
(for VA = 2.5 V)	
1000	1.5 V
1001	2.0 V
1010	2.5 V
1011	3.0 V
1100	3.5 V
1101	4.0 V
1110	4.5 V
1111	5.0 V
Application:	"VP Battery Compensation" on page 33

6.38 VP Battery Level (Address 30h) (Read Only)

7	6	5	4	3	2	1	0
VPLVL7	VPLVL6	VPLVL5	VPLVL4	VPLVL3	VPLVL2	VPLVL1	VPLVL0

6.38.1 VP Voltage Level (Read Only)

Indicates the unsigned VP voltage level.

VPLVL[7:0]	VP Voltage
...	
0101 1110	3.0 V (for VA = 2.0 V); apply formula using actual VA voltage to calculate VP voltage.
...	
0111 0010	3.7 V (for VA = 2.0 V); apply formula using actual VA voltage to calculate VP voltage.
...	
Formula:	$VP\ Voltage = (Binary\ representation\ of\ VPLVL[7:0]) * VA / 63.3$

6.39 Speaker Status (Address 31h) (Read Only)

7	6	5	4	3	2	1	0
Reserved	Reserved	SPKASHRT	SPKBSHRT	SPKR/HP	Reserved	Reserved	Reserved

6.39.1 Speaker Current Load Status (Read Only)

Indicates whether or not any of the speaker outputs is shorted to ground.

SPKxSHRT	Speaker Output Load
0	No overload detected
1	Overload detected

6.39.2 SPKR/HP Pin Status (Read Only)

Indicates the status of the SPKR/HP pin.

SPKR/HP	Pin State
0	Pulled Low
1	Pulled High

6.40 Charge Pump Frequency (Address 34h)

7	6	5	4	3	2	1	0
CHGFREQ3	CHGFREQ2	CHGFREQ1	CHGFREQ0	Reserved	Reserved	Reserved	Reserved

6.40.1 Charge Pump Frequency

Sets the charge pump frequency on FLYN and FLYP.

CHGFREQ[3:0]	N
0000	0
...	
0101	5
...	
1111	15
Formula:	Frequency = (64xFs)/(N+2)

Note: The headphone output THD+N performance may be affected.

7. ANALOG PERFORMANCE PLOTS

7.1 Headphone THD+N versus Output Power Plots

Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; $F_s = 48$ kHz.

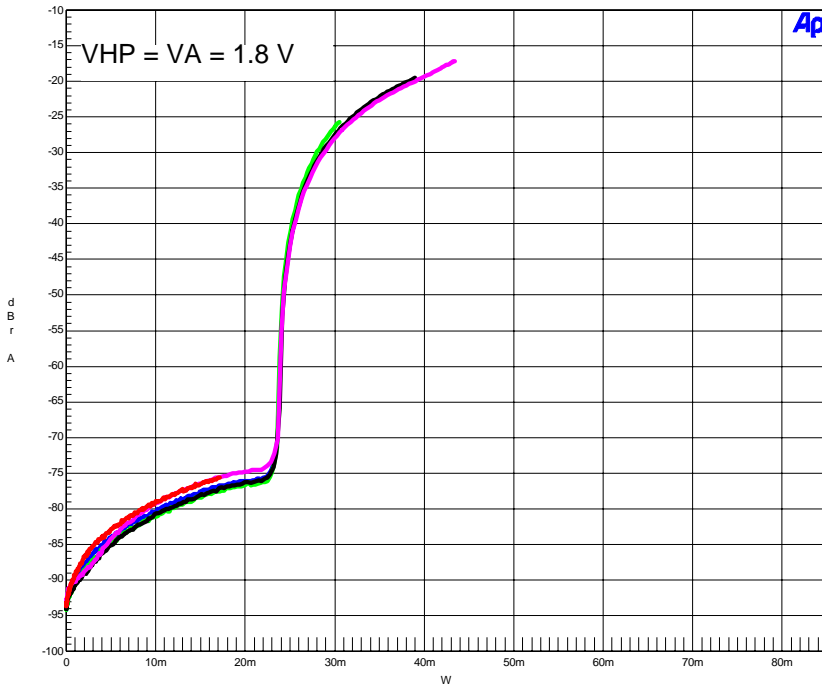
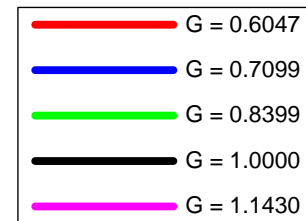


Figure 22. THD+N vs. Output Power per Channel at 1.8 V (16 Ω load)



Legend

NOTE: Graph shows the output power *per channel* (i.e. Output Power = 23 mW into single 16 Ω and 46 mW into stereo 16 Ω with THD+N = -75 dB).

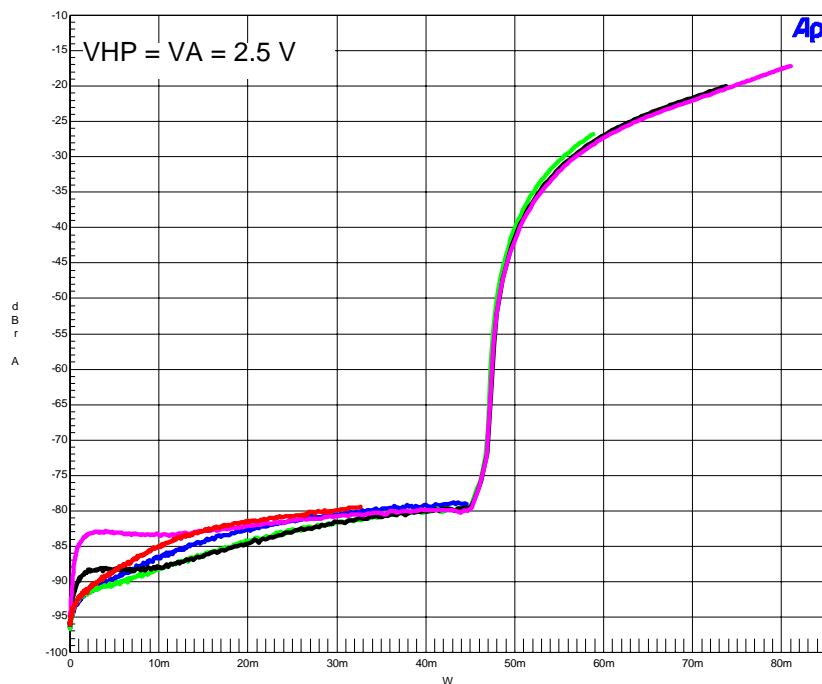
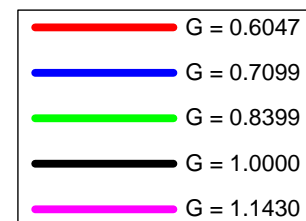


Figure 23. THD+N vs. Output Power per Channel at 2.5 V (16 Ω load)



Legend

NOTE: Graph shows the output power *per channel* (i.e. Output Power = 44 mW into single 16 Ω and 88 mW into stereo 16 Ω with THD+N = -75 dB).

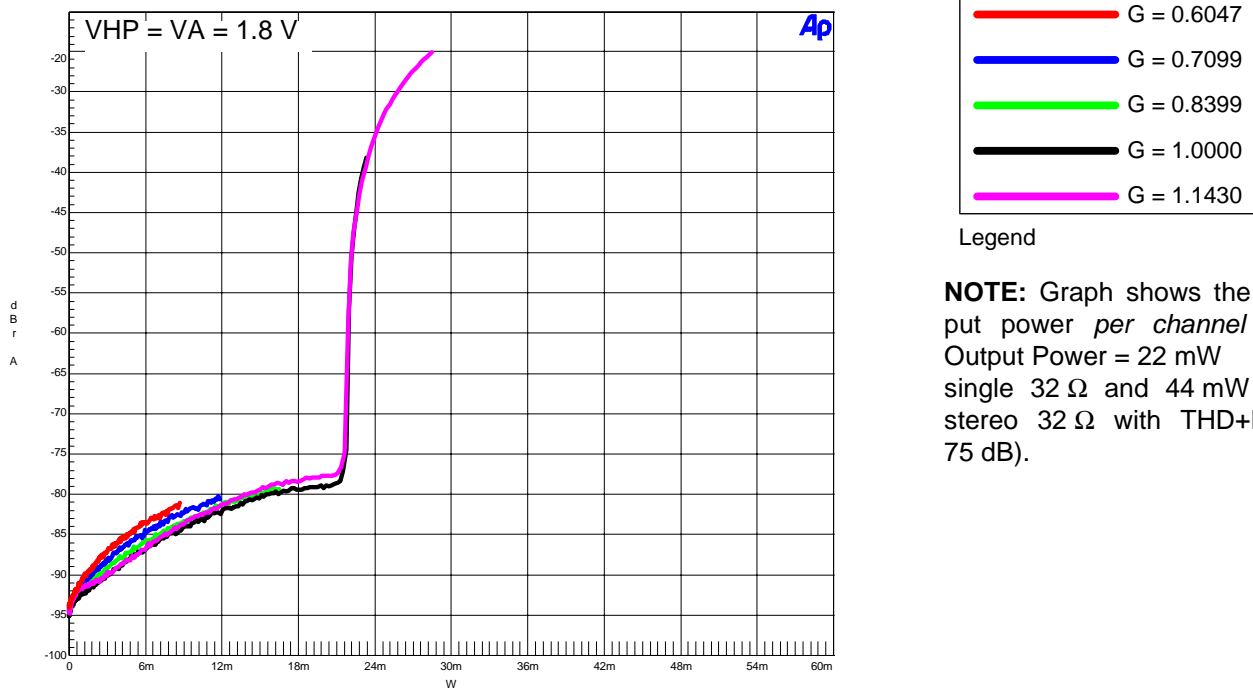


Figure 24. THD+N vs. Output Power per Channel at 1.8 V (32 Ω load)

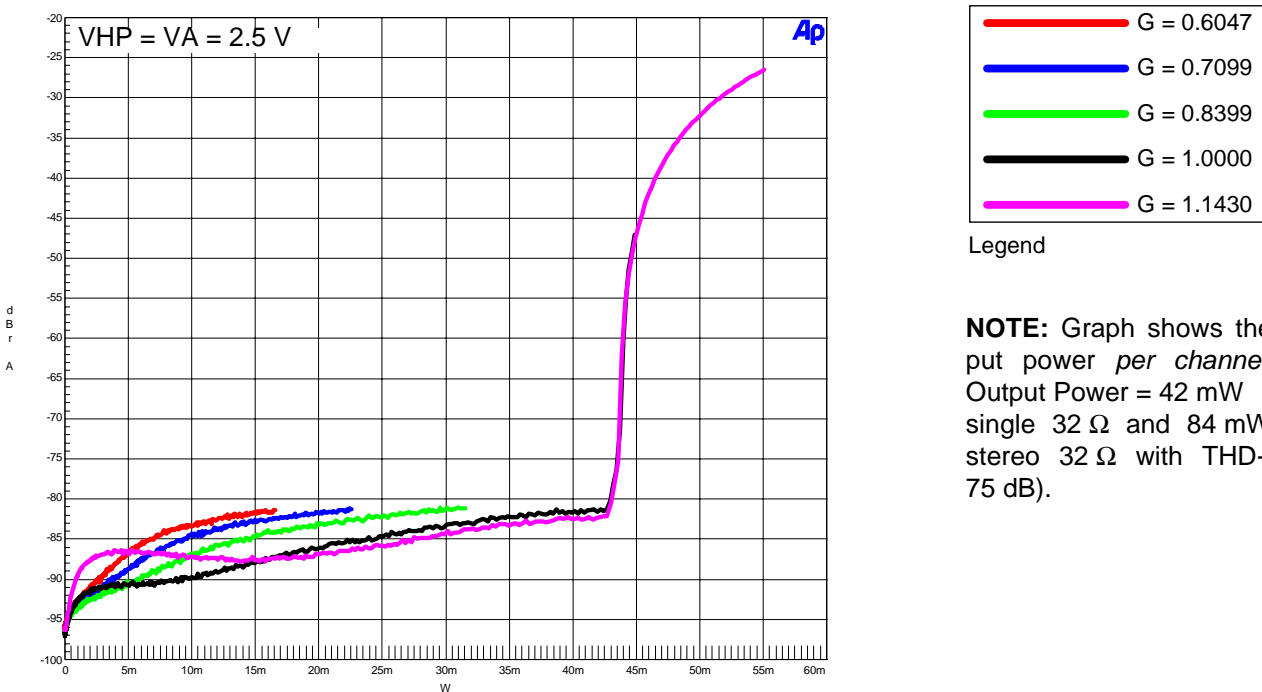


Figure 25. THD+N vs. Output Power per Channel at 2.5 V (32 Ω load)

8. EXAMPLE SYSTEM CLOCK FREQUENCIES *The "MCLKDIV2" bit must be enabled.

8.1 Auto Detect Enabled

Sample Rate LRCK (kHz)	MCLK (MHz)			
	1024x	1536x	2048x*	3072x*
8	8.1920	12.2880	16.3840	24.5760
11.025	11.2896	16.9344	22.5792	33.8688
12	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	512x	768x	1024x*	1536x*
16	8.1920	12.2880	16.3840	24.5760
22.05	11.2896	16.9344	22.5792	33.8688
24	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	256x	384x	512x*	768x*
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	128x	192x	256x*	384x*
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

8.2 Auto Detect Disabled

Sample Rate LRCK (kHz)	MCLK (MHz)					
	512x	768x	1024x	1536x	2048x	3072x
8	-	6.1440	8.1920	12.2880	16.3840	24.5760
11.025	-	8.4672	11.2896	16.9344	22.5792	33.8688
12	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)					
	256x	384x	512x	768x	1024x	1536x
16	-	6.1440	8.1920	12.2880	16.3840	24.5760
22.05	-	8.4672	11.2896	16.9344	22.5792	33.8688
24	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	256x	384x	512x	768x
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	128x	192x	256x	384x
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

9. PCB LAYOUT CONSIDERATIONS

9.1 Power Supply, Grounding

As with any high-resolution converter, the CS42L52 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. [Figure 1 on page 10](#) shows the recommended power arrangements, with VA and VHP connected to clean supplies VD, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VD may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS42L52 as possible. The low value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS42L52 to minimize inductance effects.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 μF , must be positioned to minimize the electrical path from FILT+ and AGND. The CDB42L52 evaluation board demonstrates the optimum layout and power supply arrangements.

9.2 QFN Thermal Pad

The CS42L52 is available in a compact QFN package. The underside of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. In split ground systems, it is recommended that this thermal pad be connected to AGND for best performance. The CS42L52 evaluation board demonstrates the optimum thermal pad and via configuration.

10.ADC & DAC DIGITAL FILTERS

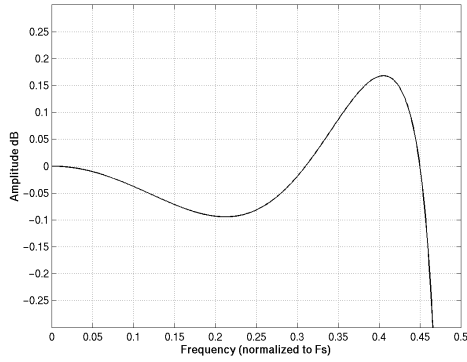


Figure 26. ADC Passband Ripple

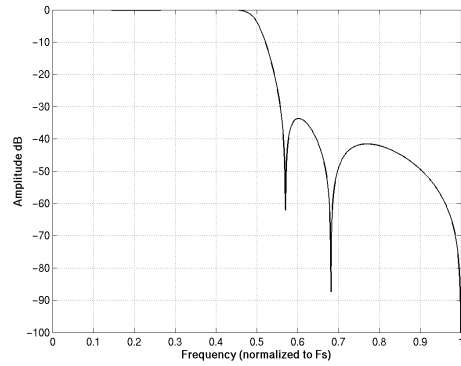


Figure 27. ADC Stopband Rejection

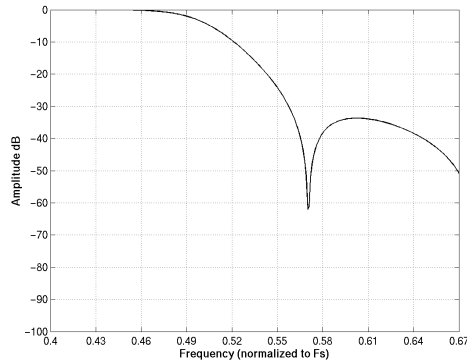


Figure 28. ADC Transition Band

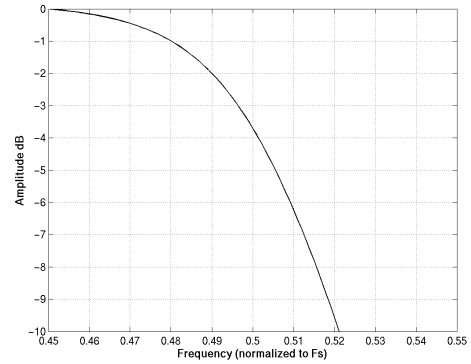


Figure 29. ADC Transition Band (Detail)

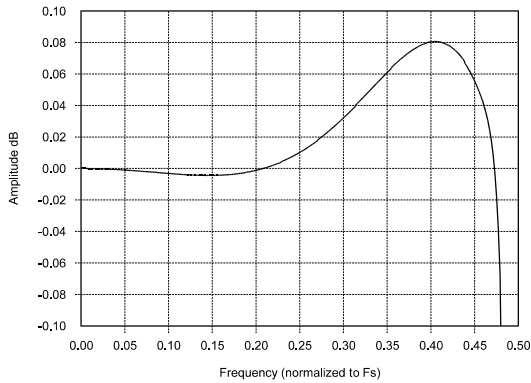


Figure 30. DAC Passband Ripple

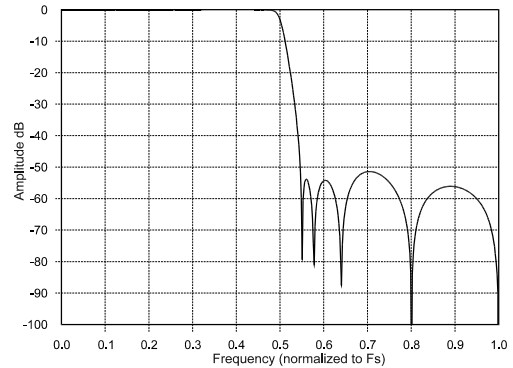


Figure 31. DAC Stopband

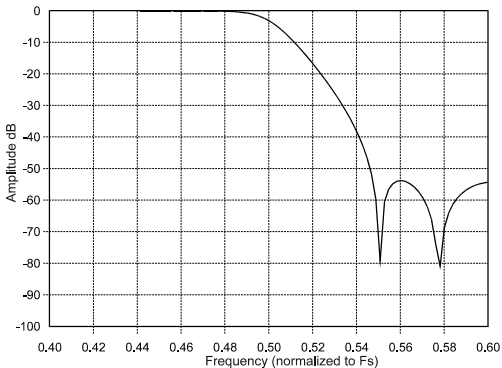


Figure 32. DAC Transition Band

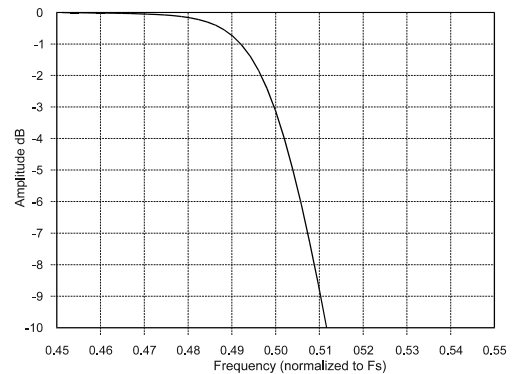


Figure 33. DAC Transition Band (Detail)

11. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

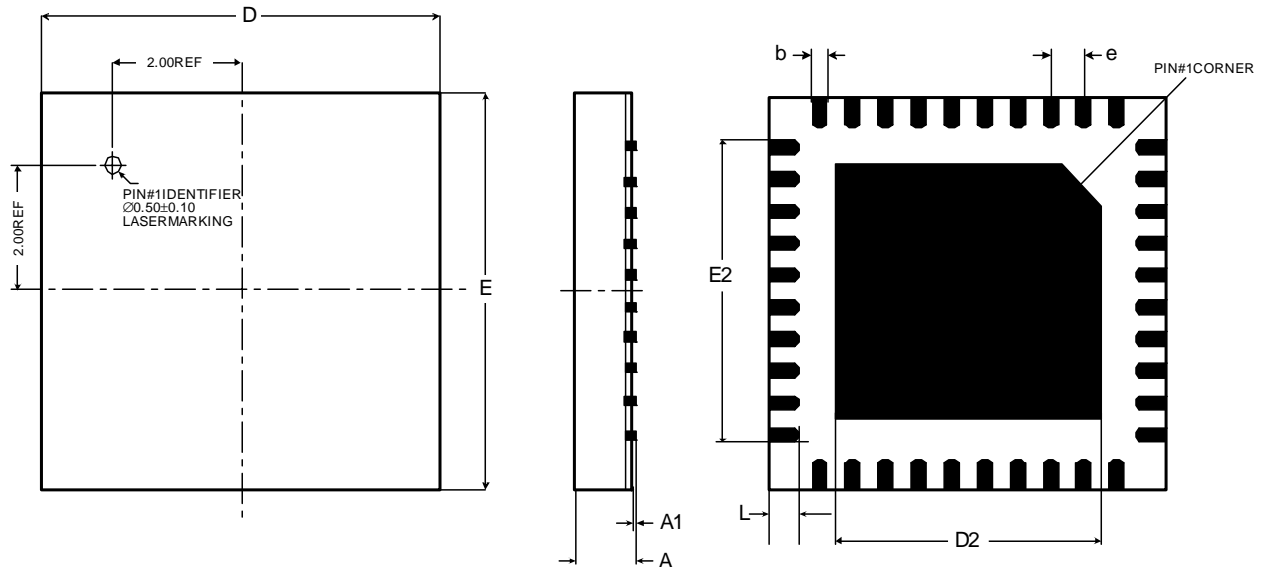
The gain difference between left and right channel pairs. Units in decibels.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

12.PACKAGE DIMENSIONS
40L QFN (6 X 6 mm BODY) PACKAGE DRAWING


DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0394	--	--	1.00	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0071	0.0091	0.0110	0.18	0.23	0.28	1,2
D	0.2362 BSC			6.00 BSC			1
D2	0.1594	0.1614	0.1634	4.05	4.10	4.15	1
E	0.2362 BSC			6.00 BSC			1
E2	0.1594	0.1614	0.1634	4.05	4.10	4.15	1
e	0.0197 BSC			0.50 BSC			1
L	0.0118	0.0157	0.0197	0.30	0.40	0.50	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

1. Dimensioning and tolerance per ASME Y 14.5M-1995.
2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board	θ_{JA}	-	44	-	°C/Watt
	4 Layer Board		-	19	-	

13.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42L52	Low-Power Stereo CODEC w/HP and Speaker Amps for Portable Apps	40L-QFN	Yes	Commercial	-40 to +85° C	Rail	CS42L52-CNZ
						Tape & Reel	CS42L52-CNZR
				Automotive	-40 to +105° C	Rail	CS42L52-DNZ
						Tape & Reel	CS42L52-DNZR
CDB42L52	CS42L52 Evaluation Board	-	No	-	-	-	CDB42L52
CRD42L52	CS42L52 Reference Design	-	No	-	-	-	CRD42L52

14.REFERENCES

1. Philips Semiconductor, *The I²C-Bus Specification: Version 2.1*, January 2000.
<http://www.semiconductors.philips.com>.

15.REVISION HISTORY

Revision	Changes
F1	<p>Removed the Thermal Error Detection and Thermal Foldback Feature</p> <p>Added "Internal Connections" to table in "I/O Pin Characteristics" on page 9.</p> <p>Added and updated absolute maximum parameters in "Absolute Maximum Ratings" on page 11</p> <p>Lowered the VP Current Consumption in "Power Consumption" on page 24.</p> <p>Updated the expected ALC behavior when signals cross the MIN threshold in "Automatic Level Control (ALC)" on page 27.</p> <p>Added the Thermal Error Disable control port initialization setting in "Required Initialization Settings" on page 37.</p> <p>Updated note 2 in "Power Down PGAx" on page 42.</p> <p>Added note in "ADC Mute" on page 51.</p> <p>Added note in "Digital Soft Ramp" on page 53.</p> <p>Added notes in "Digital Zero Cross" on page 53.</p> <p>Updated the ADCB=A, PLYBCKB=A and SPKRB=A descriptions in "Analog Front-End Volume Setting B=A" on page 50, "Playback Volume Setting B=A" on page 51, and "Speaker Volume Setting B=A" on page 54.</p> <p>Corrected the MICxGAIN decode settings in "MICx Gain" on page 55.</p> <p>Corrected BEEP volume settings to reflect level relative to DAC's full scale in "Beep Volume" on page 61.</p> <p>Added note 2 in "VP Monitor" on page 71.</p>

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.

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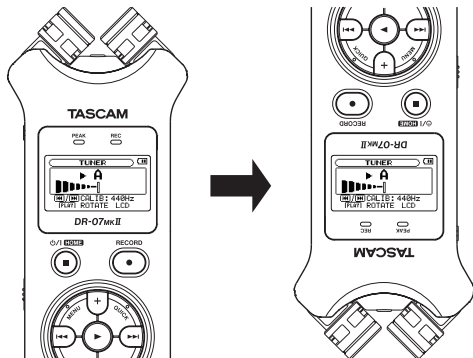
I²C is a registered trademark of Philips Semiconductor.

取扱説明書の追加

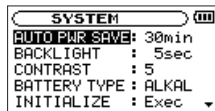
90ページ：楽器をチューニングする
(チューナー)の機能追加

チューナーが使いやすくなりました。

“TUNER”画面表示中にPLAYボタンを押すと画面の上下が反転します。内蔵マイクをチューナー使用者に向けたときに表示がわかりやすくなりました。



取扱説明書の訂正

96ページ：電源のオートオフ設定の
記述内容の訂正

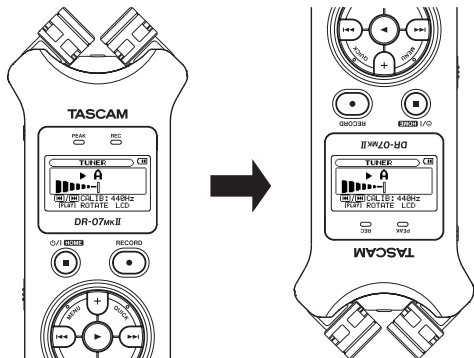
- 電源のオートオフ設定の項目名の訂正
(誤) “AUTO OFF”
(正) “AUTO PWR SAVE”
- 選択肢の初期値の変更
(誤) “OFF” (初期値、自動オフしない)、“3min”、“5min”、“10min”、“30min”
(正) “OFF”、“3min”、“5min”、“10min”、“30min” (初期値)

Owner's Manual Additional Information

Page 103: New function for "9-Tuning a Musical Instrument (Tuner)"

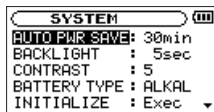
The tuner is now easier to use.

When the TUNER screen is open, you can press the **PLAY** button to reverse the screen orientation, making it easier to tune using the built-in mic.



Owner's Manual Correction

Page 109: Revisions in "Turning the unit power OFF automatically"



- Revision of the automatic power saving setting item name

Correct: AUTO PWR SAVE

Incorrect: AUTO OFF

- Change to the factory setting

Correct: Options: OFF, 3min, 5min, 10min, 30min (factory setting)

Incorrect: Options: OFF (factory setting—the unit does not automatically turn OFF), 3min, 5min, 10min, 30min

Updates

Always use the most recent firmware for this device. Please visit the TASCAM web site at <http://tascam.com/> to check for the latest firmware.

Maintenance items

V1.01 fixes

- If you pressed the **RECORD [●]** button when the Auto Record function was on and operating, the Auto Record function would not perform correctly in some cases. This has been fixed.
- If a folder created by a computer was present and you created an additional new folder and then tried to record to it, recording to the new folder would not occur in some cases. This has been fixed.
- Operation reliability has been improved.

Confirmation of firmware version

Confirm the firmware version of your DR-07MKII before conducting a firmware update.

- 1 **Turn the unit's power ON.**
- 2 **Press the MENU button to open the MENU screen, select INFORMATION and press the F4 (▶) key.**
- 3 **Use the +/- buttons to select the OTHERS menu item, and press the ▶ button to open the OTHERS submenu.**
- 4 **Use the +/- buttons to select the INFORMATION menu item, and press the ▶ button to open the INFORMATION screen FILE (1/3) page.**
- 5 **Use the +/- buttons to open the SYSTEM (3/3) page where you can check the System Ver. item that shows the firmware version.**

If the System Ver. shown here is the same or newer than the firmware version that you planned to update to, then there is no need to update it.

Firmware update procedures

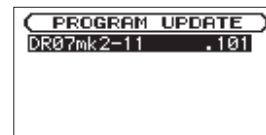
CAUTION

When updating the firmware, be sure that the batteries have sufficient charge or power the unit using a TASCAM PS-P515U AC adaptor (sold separately) or USB bus power from a computer.

The program has been set so that the update will not be conducted if battery power is insufficient.

- 1 **Download the most recent firmware from the TASCAM web site (<http://tascam.com/>). If the file that you have downloaded is compressed in ZIP format, for example, decompress it.**
- 2 **Turn the unit's power ON and use the included USB cable to connect it with a computer. This unit will be recognized as an external drive (external storage device) by the computer.**
- 3 **Copy the downloaded firmware (DR07mk2-11.101 for V1.01) to the UTILITY folder on the DR-07MKII.**
- 4 **After copying has completed, disconnect the unit from the computer following the correct procedures, and turn the unit power OFF.**
- 5 **While pressing and holding both the MARK and ◀◀ buttons, turn the unit power ON.**

The unit starts up in update mode, and the update file appears on the screen.



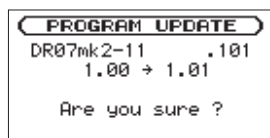
CAUTION

- If this screen does not appear, turn the power OFF. Then while pressing and holding both the **MARK** and ◀◀ buttons, turn the unit's power ON again. Continue to press and hold the **MARK** and ◀◀ buttons firmly until this screen appears.
- When firmware has been copied to this unit's *UTILITY* folder from a Mac, in addition to the firmware file itself, another file with "." added to the beginning of the firmware name is also shown. Use the file without the "." at the beginning of the name.

NOTE

- This screen shows a list of the firmware update files inside the *UTILITY* folder of the unit. Also, the screen shows the firmware copied at Step 3 above. No Update File appears if there is no update file in the *UTILITY* folder.
- The screen shown is an example. The actual display differs.

- 6 Use the +/- buttons to select the firmware and press the ► button to open the following screen.



The current version appears on the left and the updated version appears on the right.

NOTE

The screen shown is an example. The actual display differs.

- 7 Press the ► button to start the update.
- 8 When the update is complete, Update Complete appears at the bottom of the screen, and then the power turns OFF automatically. Turn the power ON again.
- 9 Follow the “Confirmation of firmware version” instructions above to check that the System Ver. is now the most recent version of the firmware.

This completes the procedure for updating this unit.

- 10 Connect to a computer with USB and delete the firmware update from the unit's *UTILITY* folder.

Updates

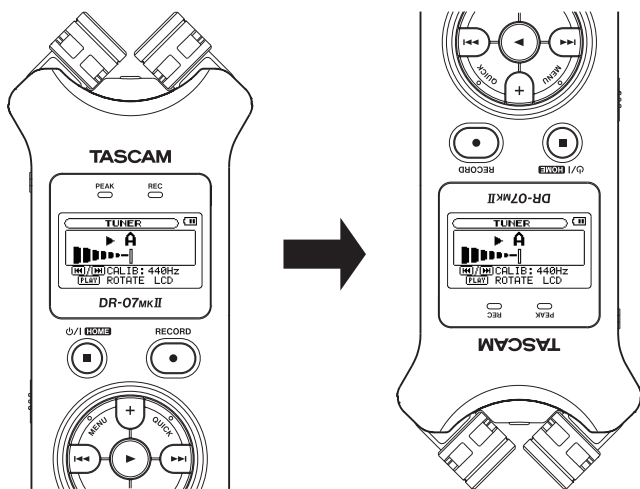
Always use the most recent firmware for this device.
Please visit the TASCAM web site at <http://tascam.com/> to check for the latest firmware.

New functions

V1.10 additions

The tuner is now easier to use.

When the TUNER screen is open, you can press the **PLAY** button to reverse the screen orientation, making it easier to tune using the built-in mic.



Maintenance items

V1.10 fixes

- If the power was turned OFF when the built-in mic right-left setting was set to R-L and then a stereo mini plug was inserted into the **MIC/EXT IN** jack before turning the power ON again, the right-left setting of the external input would be reversed. This has been fixed.
- The automatic power off setting item display has been changed to **AUTO PWR SAVE** and the default value has been changed to **30min**.

V1.01 fixes

- If you pressed the **RECORD [●]** button when the Auto Record function was on and operating, the Auto Record function would not perform correctly in some cases. This has been fixed.
- If a folder created by a computer was present and you created an additional new folder and then tried to record to it, recording to the new folder would not occur in some cases. This has been fixed.
- Operation reliability has been improved.

Confirmation of firmware version

Confirm the firmware version of your DR-07MKII before conducting a firmware update.

- 1 **Turn the unit's power ON.**
- 2 **Press the MENU button to open the MENU screen, select INFORMATION and press the F4 (▶) key.**
- 3 **Use the +/- buttons to select the OTHERS menu item, and press the ▶ button to open the OTHERS submenu.**
- 4 **Use the +/- buttons to select the INFORMATION menu item, and press the ▶ button to open the INFORMATION screen FILE (1/3) page.**
- 5 **Use the +/- buttons to open the SYSTEM (3/3) page where you can check the System Ver. item that shows the firmware version.**

If the System Ver. shown here is the same or newer than the firmware version that you planned to update to, then there is no need to update it.

Firmware update procedures

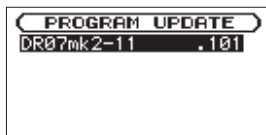
CAUTION

When updating the firmware, be sure that the batteries have sufficient charge or power the unit using a TASCAM PS-P515U AC adaptor (sold separately) or USB bus power from a computer.

The program has been set so that the update will not be conducted if battery power is insufficient.

- 1 **Download the most recent firmware from the TASCAM web site (<http://tascam.com/>). If the file that you have downloaded is compressed in ZIP format, for example, decompress it.**
- 2 **Turn the unit's power ON and use the included USB cable to connect it with a computer. This unit will be recognized as an external drive (external storage device) by the computer.**
- 3 **Copy the downloaded firmware (DR07mk2-11.101 for V1.01) to the *UTILITY* folder on the DR-07MKII.**
- 4 **After copying has completed, disconnect the unit from the computer following the correct procedures, and turn the unit power OFF.**
- 5 **While pressing and holding both the MARK and \blacktriangleleft buttons, turn the unit power ON.**

The unit starts up in update mode, and the update file appears on the screen.



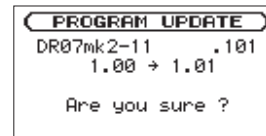
CAUTION

- If this screen does not appear, turn the power OFF. Then while pressing and holding both the **MARK** and \blacktriangleleft buttons, turn the unit's power ON again. Continue to press and hold the **MARK** and \blacktriangleleft buttons firmly until this screen appears.
- When firmware has been copied to this unit's *UTILITY* folder from a Mac, in addition to the firmware file itself, another file with "." added to the beginning of the firmware name is also shown. Use the file without the "." at the beginning of the name.

NOTE

- This screen shows a list of the firmware update files inside the *UTILITY* folder of the unit. Also, the screen shows the firmware copied at Step 3 above. No Update File appears if there is no update file in the *UTILITY* folder.
- The screen shown is an example. The actual display differs.

- 6 **Use the +/- buttons to select the firmware and press the \blacktriangleright button to open the following screen.**



The current version appears on the left and the updated version appears on the right.

NOTE

The screen shown is an example. The actual display differs.

- 7 **Press the \blacktriangleright button to start the update.**
 - 8 **When the update is complete, Update Complete appears at the bottom of the screen, and then the power turns OFF automatically. Turn the power ON again.**
 - 9 **Follow the "Confirmation of firmware version" instructions above to check that the System Ver. is now the most recent version of the firmware.**
- This completes the procedure for updating this unit.
- 10 **Connect to a computer with USB and delete the firmware update from the unit's *UTILITY* folder.**

Updates

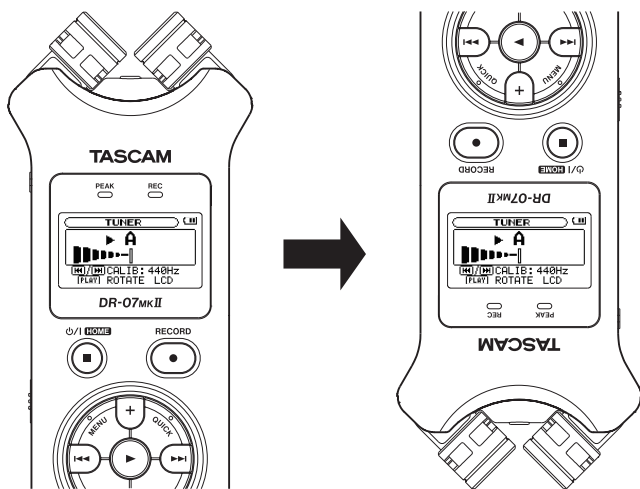
Always use the most recent firmware for this device.
Please visit the TASCAM web site at <http://tascam.com/> to check for the latest firmware.

New functions

V1.10 additions

The tuner is now easier to use.

When the TUNER screen is open, you can press the **PLAY** button to reverse the screen orientation, making it easier to tune using the built-in mic.



Maintenance items

V1.11 fixes

- Certain MP3 files could not be properly played back to their ends. This has been fixed.
- Operation reliability has been improved.

V1.10 fixes

- If the power was turned OFF when the built-in mic right-left setting was set to R-L and then a stereo mini plug was inserted into the **MIC/EXT IN** jack before turning the power ON again, the right-left setting of the external input would be reversed. This has been fixed.
- The automatic power off setting item display has been changed to **AUTO PWR SAVE** and the default value has been changed to **30min**.

V1.01 fixes

- If you pressed the **RECORD [●]** button when the Auto Record function was on and operating, the Auto Record function would not perform correctly in some cases. This has been fixed.
- If a folder created by a computer was present and you created an additional new folder and then tried to record to it, recording to the new folder would not occur in some cases. This has been fixed.
- Operation reliability has been improved.

Confirmation of firmware version

Confirm the firmware version of your DR-07MKII before conducting a firmware update.

- 1 **Turn the unit's power ON.**
- 2 **Press the MENU button to open the MENU screen, select INFORMATION and press the F4 (▶) key.**
- 3 **Use the +/- buttons to select the OTHERS menu item, and press the ▶ button to open the OTHERS submenu.**
- 4 **Use the +/- buttons to select the INFORMATION menu item, and press the ▶ button to open the INFORMATION screen FILE (1/3) page.**
- 5 **Use the +/- buttons to open the SYSTEM (3/3) page where you can check the System Ver. item that shows the firmware version.**

If the System Ver. shown here is the same or newer than the firmware version that you planned to update to, then there is no need to update it.

Firmware update procedures

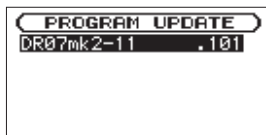
CAUTION

When updating the firmware, be sure that the batteries have sufficient charge or power the unit using a TASCAM PS-P515U AC adaptor (sold separately) or USB bus power from a computer.

The program has been set so that the update will not be conducted if battery power is insufficient.

- 1 **Download the most recent firmware from the TASCAM web site (<http://tascam.com/>). If the file that you have downloaded is compressed in ZIP format, for example, decompress it.**
- 2 **Turn the unit's power ON and use the included USB cable to connect it with a computer. This unit will be recognized as an external drive (external storage device) by the computer.**
- 3 **Copy the downloaded firmware (DR07mk2-11.101 for V1.01) to the *UTILITY* folder on the DR-07MKII.**
- 4 **After copying has completed, disconnect the unit from the computer following the correct procedures, and turn the unit power OFF.**
- 5 **While pressing and holding both the MARK and \blacktriangleleft buttons, turn the unit power ON.**

The unit starts up in update mode, and the update file appears on the screen.



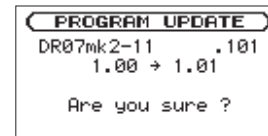
CAUTION

- If this screen does not appear, turn the power OFF. Then while pressing and holding both the **MARK** and \blacktriangleleft buttons, turn the unit's power ON again. Continue to press and hold the **MARK** and \blacktriangleleft buttons firmly until this screen appears.
- When firmware has been copied to this unit's *UTILITY* folder from a Mac, in addition to the firmware file itself, another file with "._" added to the beginning of the firmware name is also shown. Use the file without the "._" at the beginning of the name.

NOTE

- This screen shows a list of the firmware update files inside the *UTILITY* folder of the unit. Also, the screen shows the firmware copied at Step 3 above. No Update File appears if there is no update file in the *UTILITY* folder.
- The screen shown is an example. The actual display differs.

- 6 **Use the +/- buttons to select the firmware and press the \blacktriangleright button to open the following screen.**



The current version appears on the left and the updated version appears on the right.

NOTE

The screen shown is an example. The actual display differs.

- 7 **Press the \blacktriangleright button to start the update.**
 - 8 **When the update is complete, Update Complete appears at the bottom of the screen, and then the power turns OFF automatically. Turn the power ON again.**
 - 9 **Follow the "Confirmation of firmware version" instructions above to check that the System Ver. is now the most recent version of the firmware.**
- This completes the procedure for updating this unit.
- 10 **Connect to a computer with USB and delete the firmware update from the unit's *UTILITY* folder.**

Updates

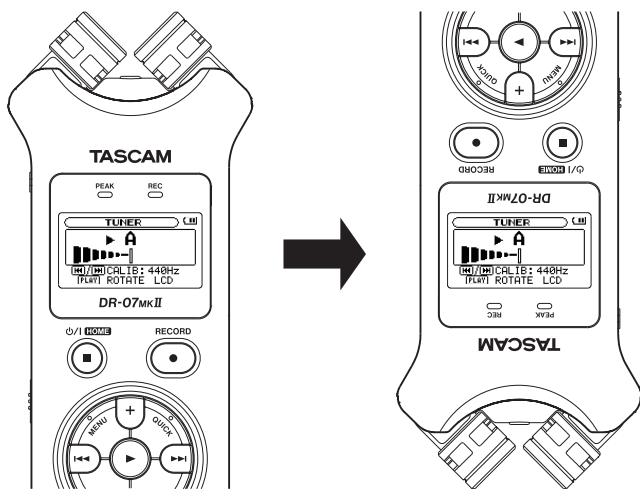
Always use the most recent firmware for this device. Please visit the TASCAM web site at <http://tascam.com/> to check for the latest firmware.

New functions

V1.10 additions

The tuner is now easier to use.

When the TUNER screen is open, you can press the **PLAY** button to reverse the screen orientation, making it easier to tune using the built-in mic.



Maintenance items

V1.12 fix

- When started in a cold environment, a loud noise would occur from the Ω /LINE OUT jack on rare occasions. This has been fixed.

V1.11 fixes

- Certain MP3 files could not be properly played back to their ends. This has been fixed.
- Operation reliability has been improved.

V1.10 fixes

- If the power was turned OFF when the built-in mic right-left setting was set to $R-L$ and then a stereo mini plug was inserted into the **MIC/EXT IN** jack before turning the power ON again, the right-left setting of the external input would be reversed. This has been fixed.

- The automatic power off setting item display has been changed to **AUTO PWR SAVE** and the default value has been changed to **30min**.

V1.01 fixes

- If you pressed the **RECORD [●]** button when the Auto Record function was on and operating, the Auto Record function would not perform correctly in some cases. This has been fixed.
- If a folder created by a computer was present and you created an additional new folder and then tried to record to it, recording to the new folder would not occur in some cases. This has been fixed.
- Operation reliability has been improved.

Confirmation of firmware version

Confirm the firmware version of your DR-07MKII before conducting a firmware update.

- Turn the unit's power ON.
- Press the **MENU** button to open the **MENU** screen, select **INFORMATION** and press the **F4 (▶)** key.
- Use the **+/-** buttons to select the **OTHERS** menu item, and press the **▶** button to open the **OTHERS** submenu.
- Use the **+/-** buttons to select the **INFORMATION** menu item, and press the **▶** button to open the **INFORMATION** screen **FILE (1/3)** page.
- Use the **+/-** buttons to open the **SYSTEM (3/3)** page where you can check the **System Ver.** item that shows the firmware version.

If the **System Ver.** shown here is the same or newer than the firmware version that you planned to update to, then there is no need to update it.

Firmware update procedures

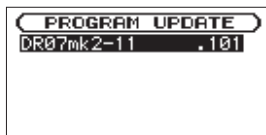
CAUTION

When updating the firmware, be sure that the batteries have sufficient charge or power the unit using a TASCAM PS-P515U AC adaptor (sold separately) or USB bus power from a computer.

The program has been set so that the update will not be conducted if battery power is insufficient.

- 1 **Download the most recent firmware from the TASCAM web site (<http://tascam.com/>). If the file that you have downloaded is compressed in ZIP format, for example, decompress it.**
- 2 **Turn the unit's power ON and use the included USB cable to connect it with a computer. This unit will be recognized as an external drive (external storage device) by the computer.**
- 3 **Copy the downloaded firmware (DR07mk2-11.101 for V1.01) to the *UTILITY* folder on the DR-07MKII.**
- 4 **After copying has completed, disconnect the unit from the computer following the correct procedures, and turn the unit power OFF.**
- 5 **While pressing and holding both the MARK and \blacktriangleleft buttons, turn the unit power ON.**

The unit starts up in update mode, and the update file appears on the screen.



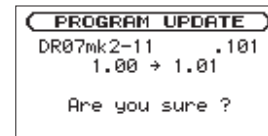
CAUTION

- If this screen does not appear, turn the power OFF. Then while pressing and holding both the **MARK** and \blacktriangleleft buttons, turn the unit's power ON again. Continue to press and hold the **MARK** and \blacktriangleleft buttons firmly until this screen appears.
- When firmware has been copied to this unit's *UTILITY* folder from a Mac, in addition to the firmware file itself, another file with "._" added to the beginning of the firmware name is also shown. Use the file without the "._" at the beginning of the name.

NOTE

- This screen shows a list of the firmware update files inside the *UTILITY* folder of the unit. Also, the screen shows the firmware copied at Step 3 above. No Update File appears if there is no update file in the *UTILITY* folder.
- The screen shown is an example. The actual display differs.

- 6 **Use the +/- buttons to select the firmware and press the \blacktriangleright button to open the following screen.**



The current version appears on the left and the updated version appears on the right.

NOTE

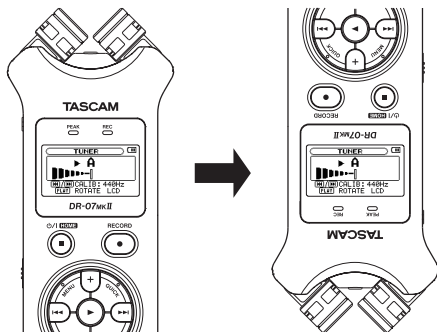
The screen shown is an example. The actual display differs.

- 7 **Press the \blacktriangleright button to start the update.**
 - 8 **When the update is complete, Update Complete appears at the bottom of the screen, and then the power turns OFF automatically. Turn the power ON again.**
 - 9 **Follow the "Confirmation of firmware version" instructions above to check that the System Ver. is now the most recent version of the firmware.**
- This completes the procedure for updating this unit.
- 10 **Connect to a computer with USB and delete the firmware update from the unit's *UTILITY* folder.**

Informazioni aggiuntive al manuale di istruzioni

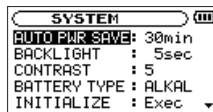
Pagina 103: Nuova funzione per "9– Accordare uno strumento musicale (Tuner)"

L'accordatore è ora più facile da usare. Quando è aperta la schermata TUNER, è possibile premere il pulsante **PLAY** per invertire l'orientamento dello schermo, rendendo più facile accordare tramite il microfono incorporato.



Correzioni nel manuale di istruzioni

Pagina 109: Revisioni riguardo allo "Autospegnimento dell'unità"



- Revisione del nome della voce di impostazione del risparmio energetico automatico

Corretto: AUTO PWR SAVE

Errato: AUTO OFF

- Modificare le impostazioni di fabbrica

Corretto: Opzioni: OFF, 3min, 5min, 10min, 30min (impostazione di fabbrica)

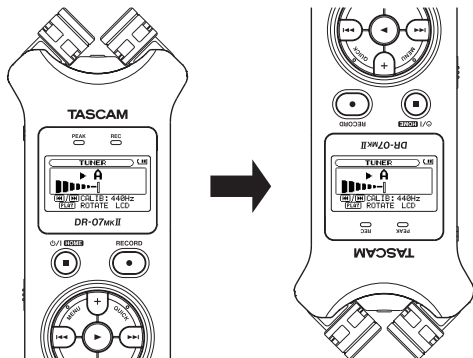
Errato: Opzioni: OFF (impostazione di fabbrica - l'unità non si spegne automaticamente), 3min, 5min, 10min, 30min

Información adicional al manual

Página 103: Nueva función para "9-Afinación de un instrumento musical (Afinador)"

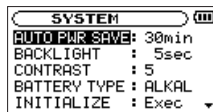
El uso del afinador es ahora mucho más fácil.

Cuando esté activa la pantalla TUNER, puede pulsar el botón **PLAY** para invertir la orientación de la pantalla, para facilitarle el uso del afinador interno.



Corrección del manual de instrucciones

Página 109: Revisión de "Apagado automático de la unidad"



- Revisión del nombre del elemento del ajuste de apagado automático

Correcto: AUTO PWR SAVE

Incorrecto: AUTO OFF

- Cambio en el ajuste de fábrica

Correcto: Opciones: OFF, 3min, 5min, 10min, 30min (valor de fábrica)

Incorrecto: Opciones: OFF (valor de fábrica—la unidad no se apaga de forma automática), 3min, 5min, 10min, 30min



TECHNICAL INFORMATION

TASCAM DR Series, OS Operation check

No. 1305

DATE 17th April. 2013

OS operation check result

■ Operation check had been done. The result is shown below.

OS operation check: Mac Mountain Lion/Windows8

April 15th, 2013

	Model name	Mac Mountain Lion	Windows8	Note
1	DP-03	ok	ok	
2	DR-05	ok	ok	
3	DR-07MK2	ok	ok	
4	DR-2d	ok	ok	
5	DR-100MK2	ok	ok	
6	DR-40	ok	ok	
7	DR-08	ok	ok	
8	DR-60D	ok	ok	
9	DR-680	ok	ok	
10	DR-V1HD	ok	ok	Playback sound isn't output because WindowsMediaPlayer doesn't support 24bit sound on movie playback. OK on QuickTime.
11	DP-24	ok	ok	
12	DP-32	ok	ok	
13	DP-004	ok	ok	
14	DP-008	ok	ok	
15	DP-006	ok	ok	
16	DP-008EX	ok	ok	



TECHNICAL INFORMATION

TASCAM DR-07MK2 V1.01 Firmware Update

No. 1110

DATE 20th Apr. 2011

The firmware V1.01 for DR-07mk2 has been released with some improvement and bug fixes from V1.00.

Improvements and Bug fixes:

1. If you pressed the RECORD button when the Auto Record function was on and operating, the Auto Record function would not perform correctly in some cases. –fixed-
2. If a folder created by a computer was present and you created an additional new folder and then tried to record to it, recording to the new folder would not occur in some cases. –fixed-
3. Operation reliability has been improved.

How to Firmware Update:

Refer to DR-07MKII Release Notes “Firmware update procedures” for details of it.
The firmware file for V1.01 is “DR07mk2-11.101” (1039KB)

Visit the [ROM Data Library](#) in the TASCAM Service HP website to download firmware.