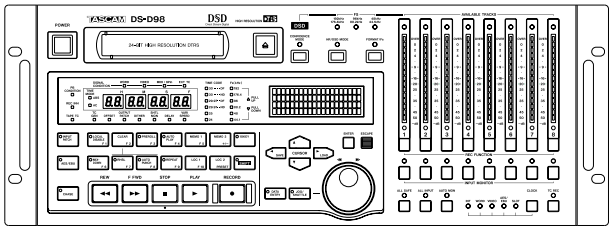


TASCAM
TEAC Professional Division

SERVICE MANUAL

DS-D98

Digital Multitrack Recorder

DSD
Direct Stream Digital

INSTRUCTIONS FOR SERVICE PERSONNEL

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

Effective : October, 2001 4B0367

S-0046

CONTENTS

1. SPECIFICATIONS ····3
2. TECHNICAL INFORMATION ····6
2-1. Activation of test mode ····6
2-2. Activation of VTR mode ····6
2-3. Displaying ROM version numbers ····6
2-4. Displaying SUB MPU version numbers ····6
2-5. Displaying the voltage of battery ····6
2-6. Displaying the hed drum utilized time ····6
2-7. Displaying the servo error history ····6
2-8. KEY PCB check mode ····7
2-9. How to use the built-in oscillator ····7
2-10. Removing the FRONT MPU ····7
2-11. Removing the SYS ROM ····7
2-12. EXTERNAL CONTROL I/O ····8
3. ASSEMBLING THE MECHANISM ASS'Y ····15
3-1. Flowchart of assembling ····15
3-2. Installation of the mechanical parts ····16
4. MECHANISM ADJUSTMENTS ····22
4-1. Preparation ····23
4-2. Test tape ····23
4-3. Adjusting the tension arm position ····24
4-4. Adjusting the torque ····24
4-5. Adjusting the tape travel ····25
4-6. Confirming the travel in F.FWD, REW and REV mode ····28
5. ELECTRICAL ADJUSTMENTS ····31
5-1. Check and adjustment points ····31
5-2. Test tape ····32
5-3. +5 V supply check ····32
5-4. P.G. (Phase generator) position adjustment ····32
5-5. Offset adjustment in the VCO free-running frequency automatic compensation circuit ····33
5-6. Playback equalizer adjustment ····34
5-7. RF level check ····35
5-8. Playback error rate check ····36
5-9. Recording current adjustment ····37
5-10. Recording/playback RF level check ····39
5-11. Recording/playback error rate check ····39
6. EXPLODED VIEWS AND PARTS LIST ····41
7. PC BOARDS AND PARTS LIST ····49
8. INCLUDED ACCESSORIES ····64

目 次

1. 仕様 ····3
2. テクニカルインフォメーション ····6
2-1. テストモードの起動 ····6
2-2. VTRモードの起動 ····6
2-3. ROMのバージョン表示 ····6
2-4. SUB MPUのバージョン表示 ····6
2-5. バッテリーの電圧表示 ····6
2-6. ドラム回転積算時間の表示 ····6
2-7. サーボエラー履歴の表示 ····6
2-8. KEY PCBチェックモード ····7
2-9. 内臓オシレーターの使用方法 ····7
2-10. FRONT MPUの外し方 ····7
2-11. SYS ROMの外し方 ····7
2-12. EXTERNAL CONTROL I/Oについて ····8
3. メカ ASS'Yの組立 ····15
3-1. 組立のフローチャート ····15
3-2. メカ部品の取付け ····16
4. 機構部調整 ····22
4-1. 準備 ····23
4-2. テストテープ ····23
4-3. テンションアーム位置調整 ····24
4-4. トルク調整 ····24
4-5. テープ走行調整 ····25
4-6. FF, REW, REV モードでの走行確認 ····28
5. 電気系調整 ····31
5-1. 測定箇所および調整箇所 ····31
5-2. テストテープ ····32
5-3. 電源+5Vの確認 ····32
5-4. PG（Phase Generator）位置調整 ····32
5-5. VCOフリーラン周波数自動補正回路のオフセット調整 ····33
5-6. 再生イコライザー調整 ····34
5-7. RFレベル確認 ····35
5-8. 再生エラーレート確認 ····36
5-9. 記録電流調整 ····37
5-10. 記録再生 RFレベル確認 ····39
5-11. 記録再生エラーレート確認 ····39
6. 分解図とパーツリスト ····41
7. 基板図とパーツリスト ····49
8. 付属品 ····64

1. SPECIFICATIONS
仕様

Tape recorder section

Format:	DTRS format
Recording method:	Rotary-head, helical-scan method
Tape type:	Hi8 MP tape / Hi8 ME
Head construction:	2 x record, 2 x playback
Tracking method:	ATF (Automatic Track Finding)
Erasure method:	Overwrite
Drum speed:	2,000 r.p.m.
Tape speed:	15.955 mm/sec.
Equivalent tape speed:	4.2 m/sec.
Maximum recording time:	108 min. (using P6-120 tape)
Time to play from stop:	Less than 2 seconds
Fast forward/rewind time:	80 seconds (using P6-120 tape)
Search speed:	Maximum of 100 x play speed
Shuttle speed:	Forward and reverse at 8.0, 4.0, 2.0, 1.0, 0.5 and 0.25 play speed (1.0 speed available only in forward shuttle mode)
Vari speed:	±6% (0.1% steps)
Positioning accuracy:	To 1 sample
Positioning lock time:	Within 8 seconds (when locating 2 DS-D98s synced together)
Number of recording tracks:	8
Sub-code:	ABS track, SMPTE/EBU timecode facility
Error correction:	Double- encoded Reed-Solomon code
Sampling frequency:	44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz
Recording resolution:	16/24 bits linear
Cross-fade time:	10 ms to 200 ms (10 ms increments)
Track delay:	–200 to +7,200 samples (–4 to +150 ms) in single-unit increments. Can be set in samples or ms.
Offset:	±2 hours (to frame accuracy)
Sync clock:	Internal, WORD or VIDEO
MIDI function:	MMC (MIDI Machine control) MTC (MIDI timecode) output TASCAM System Exclusive (track delay, etc.) Control Cahnge (mixdown)
Supported timecode formats:	SMPTE 30, 29.97 drop, 29.97 non-drop, EBU 25 and Film 24 fps with telecine pull-up and pull-down facilities

定格

録音フォーマット：	DTRSフォーマット
記録方式：	回転ヘッド式ヘリカルスキャン方式
使用テープ：	Hi8-ME および Hi8-MPテープ
ヘッド構成：	記録用×2　再生用×2
トラッキング方式：	ATF (Automatic Track Finding)
消去方法：	オーバーライト消去
ドラム回転数：	2,000 rpm.
テープ速度：	15.955 mm/sec
記録相対速度：	4.2 m/sec
記録時間：	108分（P6-120分テープ使用時）
再生立ち上がり時間：	2秒以内
早送り／巻き戻し時間：	約80秒（P6-120分テープ使用時）
サーチ速度：	最大100倍
シャトル速度：	正方向：×8,4,2,1,1/2,1/4 倍 逆方向：×8,4,2,1/2,1/4 倍
ピッチコントロール：	±6%（0.1%単位）
調整精度：	1 サンプル未満
調相時ロック時間：	8秒以内（DS-D98 2 台同期時）
記録チャンネル数：	最大8チャンネル
サブコード：	ABSタイム、SMPTE/EBUタイムコード記録可能
誤り訂正方式：	ダブルエンコーデッドリードソロモンコード
サンプリング周波数：	44.1kHz、48kHz、88.2kHz、96kHz、176.4kHz、192kHz
録音ビット：	16ビット、24ビット
基準レベル：	フルビット ー16、ー18、ー20dB 切替可能
エンファシス時定数：	50 μsec／15 μsec（再生時のみ自動選択）
クロスフェード時間：	10～200 msec（10msec 単位）
トラックディレイ：	ー200～+7200サンプル（1 サンプル単位）またはー4msec～+150msec（1msec 単位）
ABSタイムオフセット：	±2時間（フレーム単位）
シンククロック：	INT／WORD／VIDEO
MMCコントロール：	トラックディレイ、トラックコピー（システムエクスクルーシブメッセージ）
対応タイムコード：	SMPTE 30、29.97ドロップfps、29.97ノンドロップfps、EBU 25fps、フィルム 24fps

Audio characteristics (These figures are measured with the I/O Clock Range set to Narrow)

Frequency response:	10Hz to 20kHz ±0.5dB
	10Hz to 50kHz –3dB (±1dB)
Distortion*:	0.005% (1kHz, AES-17 filter)
SN ratio*:	> 102dB (1kHz, AES-17 filter and A-weighting)
Dynamic range:	> 102dB (1kHz, AES-17 filter and A-weighting)
Channel separation:	> 95dB (1kHz)

*: Use filter such as 3364A manufactured by NF.

Inputs and outputs

TDIF-1 (DIGITAL I/O):	25-pin D-sub
	TDIF-1 format
DIGITAL (AES/EBU):	25-pin D-sub
	PRO AES3-1992 Amendment 3-1999
REMOTE IN/SYNC IN:	15-pin D-sub
	Conforms to REMOTE IN/SYNC IN protocol
SYNC OUT:	15-pin D-sub
	Conforms to REMOTE IN/SYNC IN protocol
WORD SYNC IN/THRU:	BNC connector, 75 Ω at TTL level
	ON/OFF (THRU auto-terminated)
WORD SYNC OUT:	BNC connector, 75 Ω at TTL level
TIME CODE IN:	XLR-3 balanced
	Input impedance: 10 kΩ
	Input level: 0.5 Vp-p to 10.0 Vp-p
TIME CODE OUT:	XLR-3 balanced
	Output impedance: 100Ω
	Output level: 2.0 Vp-p
MIDI:	IN, OUT, THRU
VIDEO IN/THRU:	NTSC or PAL
	Negative Sync Composite video, Sync Composite Video or Frame Pulse (auto detect)
	1 Vp-p, ±0.2 V (Negative Sync Composite video or Sync Composite Video)
	TTL Level (Frame pulse)
	THRU autmatically terminated (75 Ω)
CONTROL I/O:	37-pin D-sub
RS-422:	9-pin D-sub
	Comforms to RS-422 specifications
METER UNIT:	15-pin D-sub

オーディオ特性（I/Oクロックレンジを“Narrow”に設定時）

録周波数特性：	10Hz～20kHz±0.5dB
	10Hz～50kHz−3 dB（±1dB）
歪率*：	0.005%（1kHz、AES-17 Filter）
SN比*：	102dB以上（1kHz、AES-17 Filter ＋A-Weighted）
ダイナミックレンジ：	102dB以上（1kHz、AES-17 Filter ＋A-Weighted）
チャンネルセパレーション：	95dB以上（1kHz）

* :3346A(NF 社）相当のフィルターを使用

入出力

TDIF-1（DIGITAL I/O）:	TDIF-1［不平衡、D－Sub 25ピン、メス］
DIGITAL (AES/EBU) :	PRO AES3-1992 Amendment 3-1999準拠［D-Sub 25ピン］
REMOTE IN/SYNC IN :	REMOTE IN/SYNC IN プロトコル［D-Sub 15ピン、メス］
SYNC OUT :	REMOTE IN/SYNC IN プロトコル［D-Sub 15ピン、メス］
WORD SYNC IN :	TTLレベル相当／75Ωターミネート［BNC］
WORD SYNC OUT :	TTLレベル相当［BNC］
WORD SYNC THRU :	接続時、WORD SYNC INのターミネートオフを自動認識
	自動オン／オフ方式［BNC］
TIME CODE IN :	0.5Vp-p ～ 10Vp-p／10kΩ ［平衡、XLR-3-31］
TIME CODE OUT :	2Vp-p／100Ω［平衡、XLR-3-32］
MIDI IN :	[DIN 5ピン]
MIDI OUT :	[DIN 5ピン]
MIDI THRU :	[DIN 5ピン]
VIDEO IN :	NTSC/PAL
	75Ωターミネート [BNC]
	ネガティブシンクコンポジットビデオ、シンクコンポジットビデオ、フレームパルス（自動検出）、1Vp-p ±0.2V（ネガティブシンクコンポジットビデオ、シンクコンポジットビデオ）、TTLレベル相当（フレームパルス）
VIDEO THRU :	接続時、VIDEO INのターミネートオフを自動認識
	自動オン／オフ方式「BNC]
CONTROL I/O :	[D-Sub 37ピン]
RS-422 :	[D-Sub 9ピン]
METER UNIT :	[D-Sub 15ピン、メス]

ANALOG INPUTS : XLR-3-31 type (x 2),
Nominal input level: +4 dBu
Referenve level: –16 dBFS* , –18 dBFS, –20 dBFS
Maximum input level: +20 dBu* , +22 dBu, +24 dBu (jumper-selectable)
* Factory setting
Input impedance: > 15 kΩ

ANALOG OUTPUTS : XLR-3-32 type (x 2),
Nominal output level: +4 dBu
Referenve level: –16 dBFS* , –18 dBFS, –20 dBFS
Maximum output level: +20 dBu* , +22 dBu, +24 dBu (jumper-selectable)
* Factory setting
Onput impedance: > 30 Ω

SDIF-3 OUT : BNC connector (x 2),
Output level: 5 V TTL
Output impedance: 10 Ω

SDIF-3 IN : BNC connector (x 2),
Input level: 5 V TTL
Input impedance: 75 Ω terminated
Input level H: Voh > 2.4V (minimum)
Input level L: Vol > 0.55V (maximum)

Physical specifications

Size (exc feet):	482 x 176 x 356 (mm)
w x h x d	19 x 6.9 x 14 (in)
Weight:	11 kg (24 lb)

Power specifications

Power requirements:	USA/Canada 120 VAC, 60 Hz
	U.K./Europe 230 VAC, 50 Hz
	Australia 240 VAC, 50 Hz
Power consumption:	30 W (IF-AN98HR installed: 46 W)
Applicable electromag-netic environment:	E4
Peak inrush current:	15.5 A (230 V, all options fitted)

ANALOG INPUTS : +4dBu/15kΩ 以上
［平衡、XLR-3-31タイプX2］
リファレンスレベル：−16dBFS、−18dBFS、−20dBFS
（ジャンパー切換、出荷時は−16dBFS）

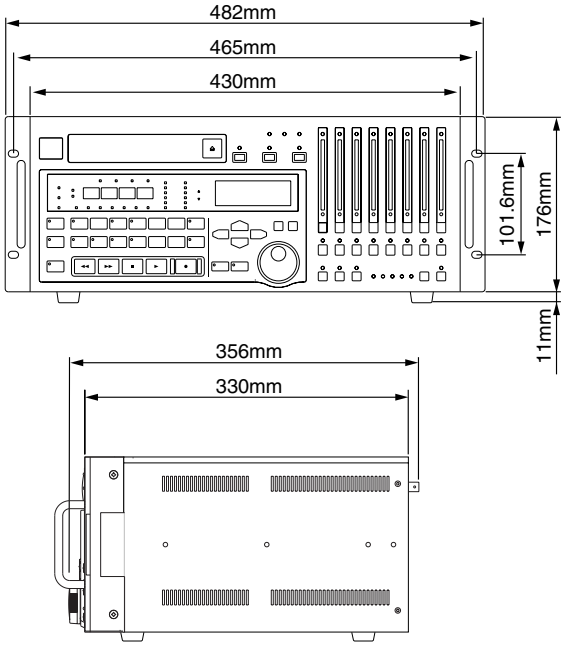
ANALOG OUTPUTS : +4dBu/30Ω 以上
［平衡、XLR-3-32タイプX2］
リファレンスレベル：−16dBFS、−18dBFS、−20dBFS
（ジャンパー切換、出荷時は−16dBFS）

SDIF-3 OUT : 5V TTL/10Ω［BNCX2］

SDIF-3 IN : 5V TTL/75Ω終端［BNCX2］
電圧 Hレベル： Voh>2.4V（最小）
電圧 Lレベル： Vol>0.55V（最大）

一般

電源：	100V AC 50-60Hz
消費電力：	30W（IF-AN98HR 装着時 46W）
質量：	11kg
外形寸法：	幅482×高さ176×奥行き356 mm（足を除く）



2. TECHNICAL INFORMATION
テクニカルインフォメーション

2-1. Activation of test mode

1. Hold down F.FWD + STOP + PLAY keys and press POWER key, and when "Select Mode" is displayed, let go of the three keys and, before 2 seconds is up, press STOP key. (TEST MODE should be displayed.)
2. The test mode is released when power is turned off.

2-2. Activation of VTR mode

1. Hold down F.FWD + STOP + PLAY keys and press POWER key, and when "Select Mode" is displayed, let go of the three keys and, before 2 seconds is up, press PLAY key. (VTR MODE should be displayed.)
2. The VTR mode is released when power is turned off.

2-3. Displaying ROM version numbers

1. Select the menu group F in the menu screen.
2. Move the cursor to the items shown below.
   Sys Ver : SYS ROM version
   Front Ver : FRONT MPU version
   Servo Ver : SERVO MPU version

2-4. Displaying SUB MPU version numbers

1. Enter the test mode.
2. Select the menu group N in the menu screen.
3. Move the cursor to "SubMpuVer" and press ENTER key.

2-5. Displaying the voltage of battery

1. Enter the test mode.
2. Select the menu group N in the menu screen.
3. Move the cursor to "Battery".

2-6. Displaying the hed drum utilized time

1. Select the menu group F in the menu screen.
2. Move the cursor to the items shown below.
   Dr Total : Total utilized time
   Dr Search : Fast-winded time

2-7. Displaying the servo error history

1. Enter the test mode.
2. Select the menu group M in the menu screen.
3. Move the cursor to "ServoErr" and press ENTER key.

Note)
Servo error data is stored in the SERVO PCB's EEPROM memory. As the power is unstable immediately after being turned ON, data written to the EEPROM at this time will be incorrect. To ensure accuracy, the DS-D98 prohibits data from being written to the EEPROM for 10 seconds after POWER ON. If an error occurs just 10 seconds, the error data is not stored in memory. As a result, the servo error history stored in the memory may differ from actual phenomena.

2-1. テストモードの起動

1. F FWDキー＋STOPキー＋PLAYキーを押しながら電源をONにし、“Select Mode”表示後 一旦手を離し、2秒以内にSTOPキーを押す。(TEST MODEと表示)
2. 電源をOFFにすると、テストモードが解除される。

2-2. VTRモードの起動

1. F FWDキー＋STOPキー＋PLAYキーを押しながら電源をONにし、“Select Mode”表示後 一旦手を離し、2秒以内にPLAYキーを押す。(VTR MODEと表示)
2. 電源をOFFにすると、VTRモードが解除される。

2-3. ROMのバージョン表示

1. メニュー画面で、メニューグループFを選択する。
2. カーソルを以下の項目に合わせる。
   Sys Ver : SYS ROMのバージョン
   Front Ver : FRONT MPUのバージョン
   Servo Ver : SERVO MPUのバージョン

2-4. SUB MPUのバージョン表示

1. テストモードにする。
2. メニュー画面で、グループNを選択する。
3. “SubMpuVer”にカーソルを合わせて、ENTERキーを押す。

2-5. バッテリーの電圧表示

1. テストモードにする。
2. メニュー画面で、グループNを選択する。
3. “Battery”にカーソルを合わせる。

2-6. ドラム回転積算時間の表示

1. メニュー画面で、メニューグループFを選択する。
2. カーソルを以下の項目に合わせる。
   Dr Total : トータル積算時間
   Dr Search : サーチ時 (PLAY, REC 以外) の積算時間

2-7. サーボエラー履歴の表示

1. テストモードにする。
2. メニュー画面で、メニューグループMを選択する。
3. “ServoErr”にカーソルを合わせて、ENTERキーを押す。

注)
サーボエラーはSERVO PCB内のEEPROMに記憶されていますが、POWER ON直後はまだ電源が十分安定しておらず、そのような状態でEEPROMにデータの書き込みを行うと誤ったデータを書き込んでしまいます。
そのため、DS-D98ではPOWER ON後10秒間はEEPROMへのデータの書き込みを禁止しています。したがって、POWER ON直後にサーボエラーが発生してから10秒経過する前にPOWER OFFした場合などでは、そのサーボエラーは経歴として記憶されませんので、実際の現象と記憶された情報とで差異が生じてしまう可能性があります。

2-8. KEY PCB check mode

1. While holding the PLAY, STOP, F FWD and REW key pressed, turn the power ON. In this case, all LED's light.
2. Press the STOP, F FWD, REW, PLAY or RECORD key. All LEDs go out.
3. When each key is pressed, the corresponding LED lights.

2-9. How to use the built-in oscillator

1. Enter the test mode.
2. Select the menu group 2 in the menu screen.
3. Move the cursor to "Sine Osc" and press ENTER key.
4. Use the ▲ and ▼ keys to select the output frequency (OFF, 440 Hz, 1 kHz, 10 kHz, 20 kHz, 20 Hz, wite noise). (The level is full scale.)

2-10. Removing the FRONT MPU

As shown in Fig. 2-1, hold the FRONT MPU (KEY PCB:U6) with the PLCC EXTRACTOR (P/N: 16910101) to remove it.

2-11. Removing the SYS ROM

Detach the socket cover to remove the SYS ROM (SYS PCB:U011). To remove the socket cover, slide it as shown in Fig. 2-2.

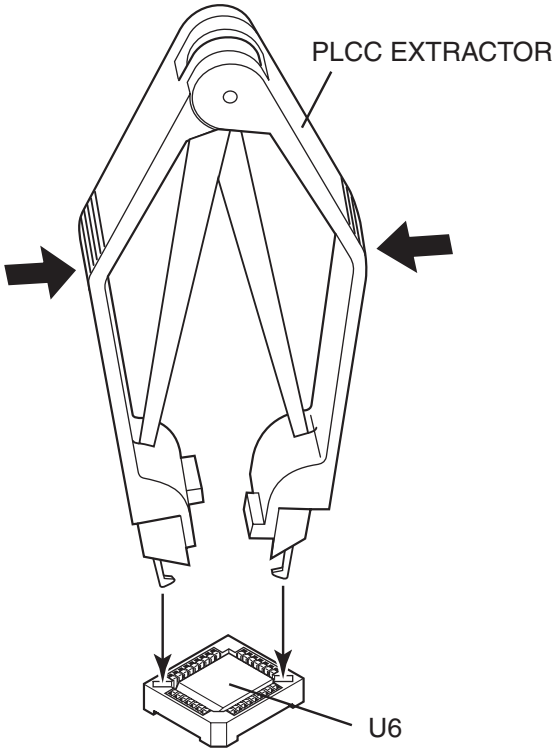


Fig. 2-1

2-8. KEY PCBチェックモード

1. PLAYキー＋STOPキー＋F FWDキー＋REWキーを押しながら電源をONにするとチェックモードに入る。このとき、LEDが全灯する。
2. STOP, F FWD, REW, PLAY, RECORDのいずれかのキーを押すと、LEDが全て消灯する。
3. その後、それぞれのキーを押すと、そのキーに対応するLEDが点灯する。

2-9. 内臓オシレーターの使用方法

1. テストモードにする。
2. メニュー画面で、メニューグループ2を選択する。
3. “Sine Osc”にカーソルを合わせてENTERキーを押す。
4. ▲キー/▼キーで、出力する周波数（OFF, 440Hz, 1kHz, 10kHz, 20kHz, 20Hz, White noise）を選択する。（レベルはフルスケール）

2-10. FRONT MPUの外し方

図2-1のように、PLCC EXTRACTOR（品番:16910101）でFRONT MPU（KEY PCB:U6)を挟んで取り外します。

2-11. SYS ROMの外し方

SYS ROM（SYS PCB:U011）はソケットカバーを取り外すことにより、外すことができます。
ソケットカバーは、図2-2のようにスライドさせることにより取り外します。

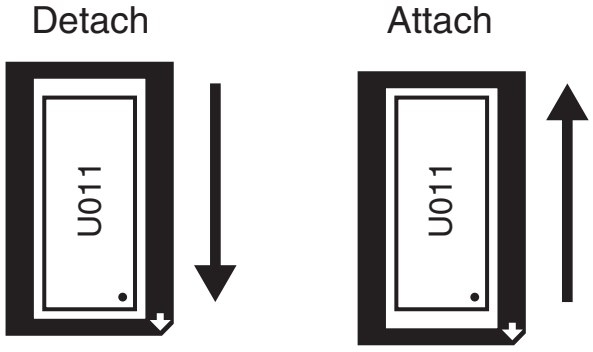


Fig. 2-2

2-12. EXTERNAL CONTROL I/O

A CONTROL I/O connector is provided to enable external control of the DS-D98. Transport control (+Chase) inputs and related tally (+Lock) outputs are readily available.
To enable further capability of REC FUNCTION and INPUT MONITOR inputs and its related tally outputs, the CONTROL I/O also consists of signals for serial communication data.

- The connector is a 37-pin D-sub and the output is an open collector. Each transistor supports a current of up to 50 mA.
  Input is at TTL level with 74LS240 of the LS-TTL used as a buffer (with Schmitt trigger).
- Power supplied from the DS-D98 is up to 50 mA at DC 5 V.
- The control system data output is 32-bit serial sync, of which 8 bits are output in parallel simultaneously.
  Input is 32-bit serial sync. The preceding 8 bits are merged with the parallel input.

The pin assignment, serial input/output signal format and recommended circuits for a controlling device are described here in after.

2-12. EXTERNAL CONTROL I/Oについて

CONTROL I/Oは外部からDS-D98をコントロールするために設けられた端子です。トランスポートコントロール（＋チェース）入力と、そのタリー（＋ロック）を出力します。また、REC FUNCTION、INPUT MONITORのキー入力と、そのタリーを出力することを可能とするために、シリアル通信用信号も用意されています。

- 端子は D-sub 37pin、出力はオープンコレクターで各トランジスターは 50mAまで電流を流すことができます。
  入力はTTLレベルで、バッファとしてLS-TTLの74LS240を使用（シュミットトリガ付き）しています。
- DS-D98から供給できる電源は DC5Vで 50mAまで可能です。
- コントロール系のデータの出力は、シリアル同期式 32ビット、そのうち 8ビットがパラレル出力され、入力はシリアル同期式 32ビット、先行 8ビットがパラレル入力とマージされます。

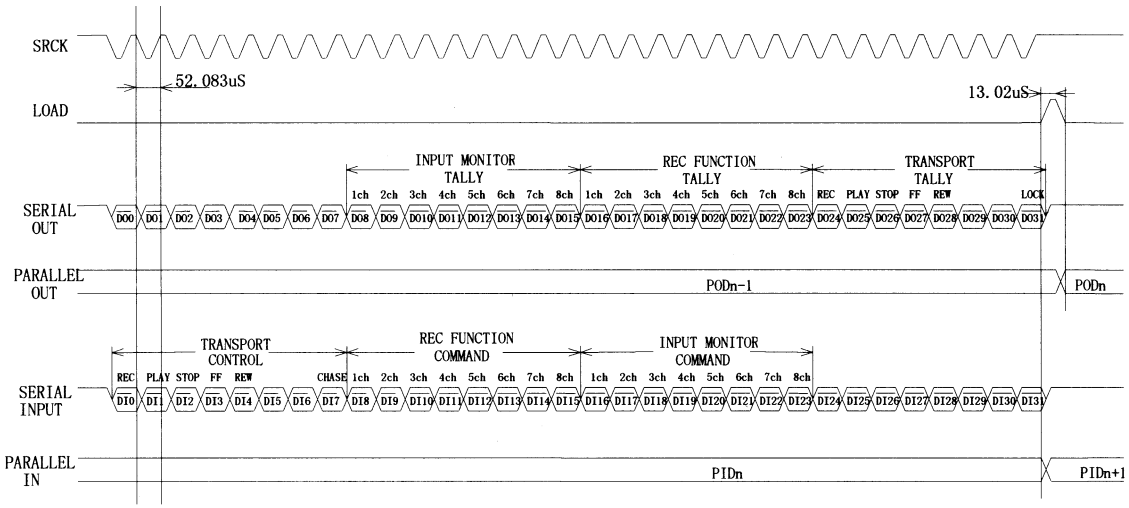
以下に、ピンアサイン、シリアル入出力信号フォ-マット、リモコンを作るときの推奨回路を記載します。

J11 Pin Assignment

Pin No.	Pin No.	Signal	Function	Input/output state
1		PLAY	PLAY command input	TTL
	20	GND	GND	GND
2		FF	FF command input	TTL
	21	SERIAL OUT	Serial data output	Open Collector
3		REW	REW command input	TTL
	22	NC	No connection　未使用端子	
4		AUX1	Auxiliary 1 input　予備1 入力	TTL
	23	SERIAL IN	Serial data input	TTL
5		STOP	Stop command input	TTL
	24	NC	No connection　未使用端子	
6		REC	REC command input	TTL
	25	NC	No connection　未使用端子	
7		AUX2	Auxiliary 2 input　予備2 入力	TTL
	26	NC	No connection　未使用端子	
8		CHASE	CHASE command input	TTL
	27	NC	No connection　未使用端子	
9		NC	No connection　未使用端子	
	28	NC	No connection　未使用端子	
10		GND	GND	GND
	29	NC	No connection　未使用端子	
11		PLAY TALLY	PLAY tally output	Open collector
	30	NC	No connection　未使用端子	
12		FF TALLY	FF tally output	Open collector
	31	NC	No connection　未使用端子	
13		REW TALLY	REW tally output	Open collector
	32	SRCK	Shift resister clock output	Open collector
14		STOP TALLY	STOP tally output	Open collector
	33	NC	No connection　未使用端子	
15		REC TALLY	REC tally output	Open collector
	34	LOAD	Load pulse output	Open collector
16		LOCK TALLY	LOCK tally output	Open collector
	35	NC	No connection　未使用端子	
17		AUX 1 TALLY	Auxiliary 1 output　予備1 出力	Open collector
	36	GND	GND	GND
18		AUX 2 TALLY	Auxiliary 2 ouput　予備2 出力	Open collector
	37	VCC +5V	Power supply DC +5V	DC5V
19		ACTIVE SENSE	Active sensse input ＊	TTL

＊: is to be connected to GND in the controlling device side to activate any tally output.
＊: はタリー出力を有効とするために、リモコン側でGNDに接続するものです。

CONTROL I/O Serial Input/output signal format



DS-D98 OUTPUT DATA（OPEN COLLECTOR）

DO0～DO7 : Undefined　未定義
DO8～DO15 : TALLY OF INPUT MONITOR（1ch, 2ch .... 8ch）
DO16～DO23 : TALLY OF REC FUNCTION（1ch, 2ch .... 8ch）
DO24 : REC TALLY
DO25 : PLAY TALLY
DO26 : STOP TALLY
DO27 : FF TALLY
DO28 : REW TALLY
DO29, DO30 : Undefined　未定義
DO31 : LOCK TALLY

DS-D98 INPUT DATA（TTL LEVEL）

DI0 : REC COMMAND
DI1 : PLAY COMMAND
DI2 : STOP COMMAND
DI3 : FF COMMAND
DI4 : REW COMMAND
DI5, DI6 : Undefined　未定義
DI7 : CHASE COMMAND
DI8～DI15 : REC FUNCTION COMMAND（1ch, 2ch .... 8ch）
DI16～DI23 : INPUT MONITOR COMMAND（1ch, 2ch .... 8ch）
DI24～DI31 : Undefined　未定義

Recommended circuit for a controlling device

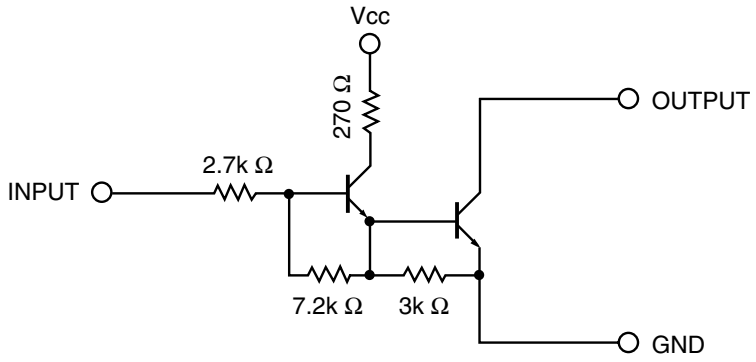
For detailed schematics of the circuit, refer to Figs. 2-3 and 2-4.

- The equivalent circuit (for one gate) of the transistor array TD62381F (P/N: S0036924) which is used for the CONTROL I/O parallel output is shown below.

リモコンの推奨回路について

具体的な回路については、図2-3, 2-4を参照してください。

- CONTROL I/Oのパラレル出力に使用されているトランジスターアレー TD62381F（品番: S0036924）の等価回路（1回路分）は以下の通りです。



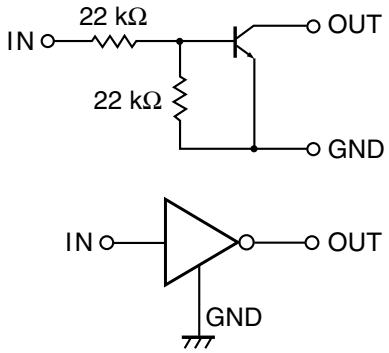
Contents 内 容		Condition 条 件	Min. 最小	Max. 最大
I_{OUT}	Current for one gate when 8 circuits operate 8回路動作時の1回路あたりの電流	Duty=10 %	0 mA	400 mA
		Duty=50 %	0 mA	330 mA
$V_{ce\ (sat)}$	Saturation voltage between collector and emitter コレクターエミッタ間飽和電圧	I_{OUT}=500 mA		0.9 V
		I_{OUT}=350 mA		0.7 V

Note) When using the power supply (DC 5 V) from the DS-D98, suppres all curent consumption to less than 50 mA.

注）DS-D98からの電源（DC 5V)を使用する場合は、全消費電流を50 mA以下に抑えてください。

● The equivalent circuit of the transistor DTC124EKA (P/N: 13428287) which is used for the CONTROL I/O serial output is shown below.

● CONTROL I/Oのシリアル出力に使用されているトランジスター DTC124EKA（品番: 13428287）の等価回路は以下の通りです。



	Typ. 標準	Max. 最大	Conditon 条件
V_O	0.1 V	0.3 V	I_O=10 mA, I_I=0.5 mA
I_I		0.36 mA	V_{II}=5 V
I_O		0.5 µA	V_{CC}=50 V, V_I=0 V

Note) When connecting more than one unit or when this unit incorporated in a system with high power comsumption, isolate the inputs/outputs from DS-D98 with a photo-coupler.

注）複数台の機器を接続する場合や消費電力の大きな機器に組み込む場合は、入出力をフォトカプラでアイソレーションしてください。

Recommended Circuit (For Basic Control)　推奨回路 1（BASIC CONTROL用）

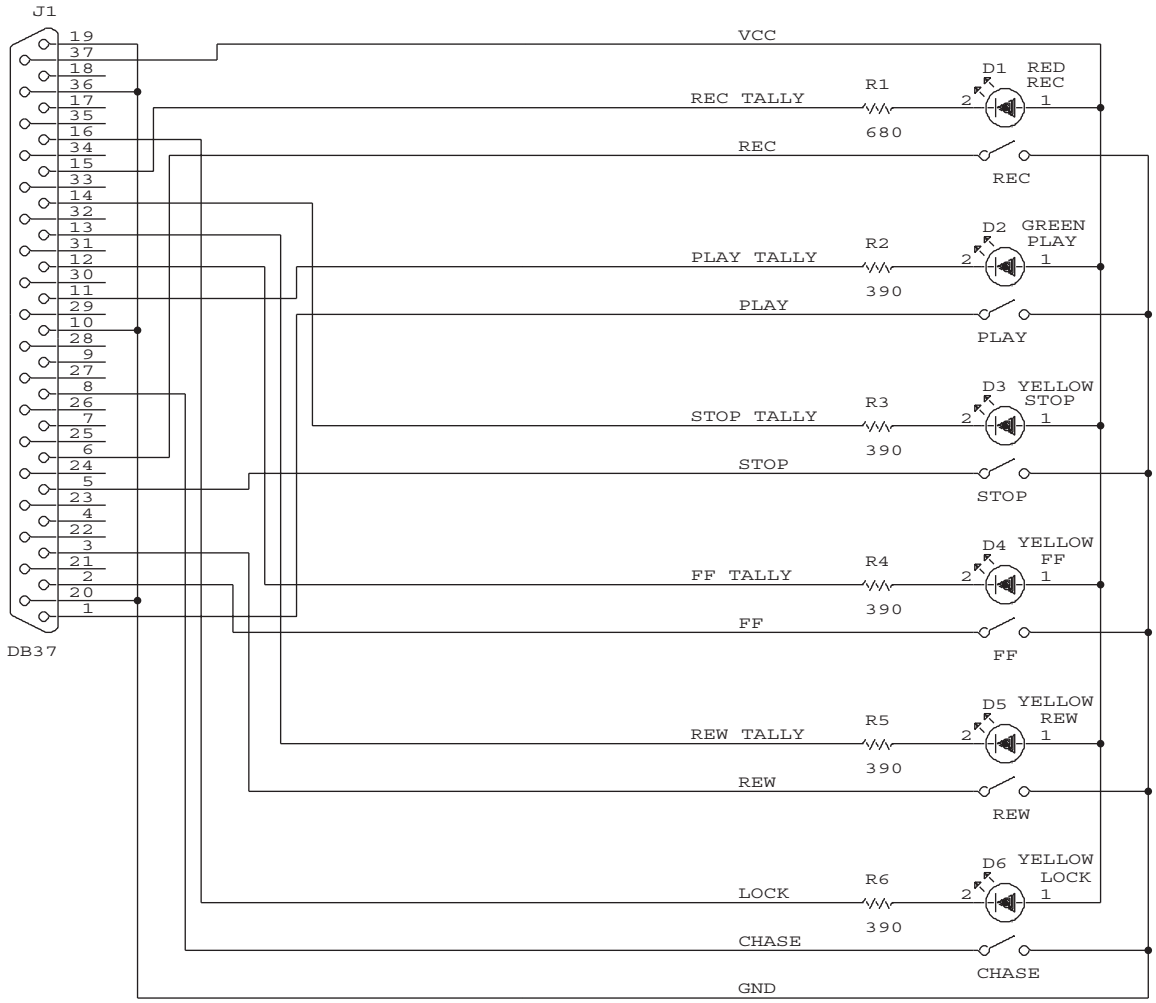


Fig. 2-3

Recommended Circuit (For Full Function)　推奨回路 2（FULL FUNCTION用）

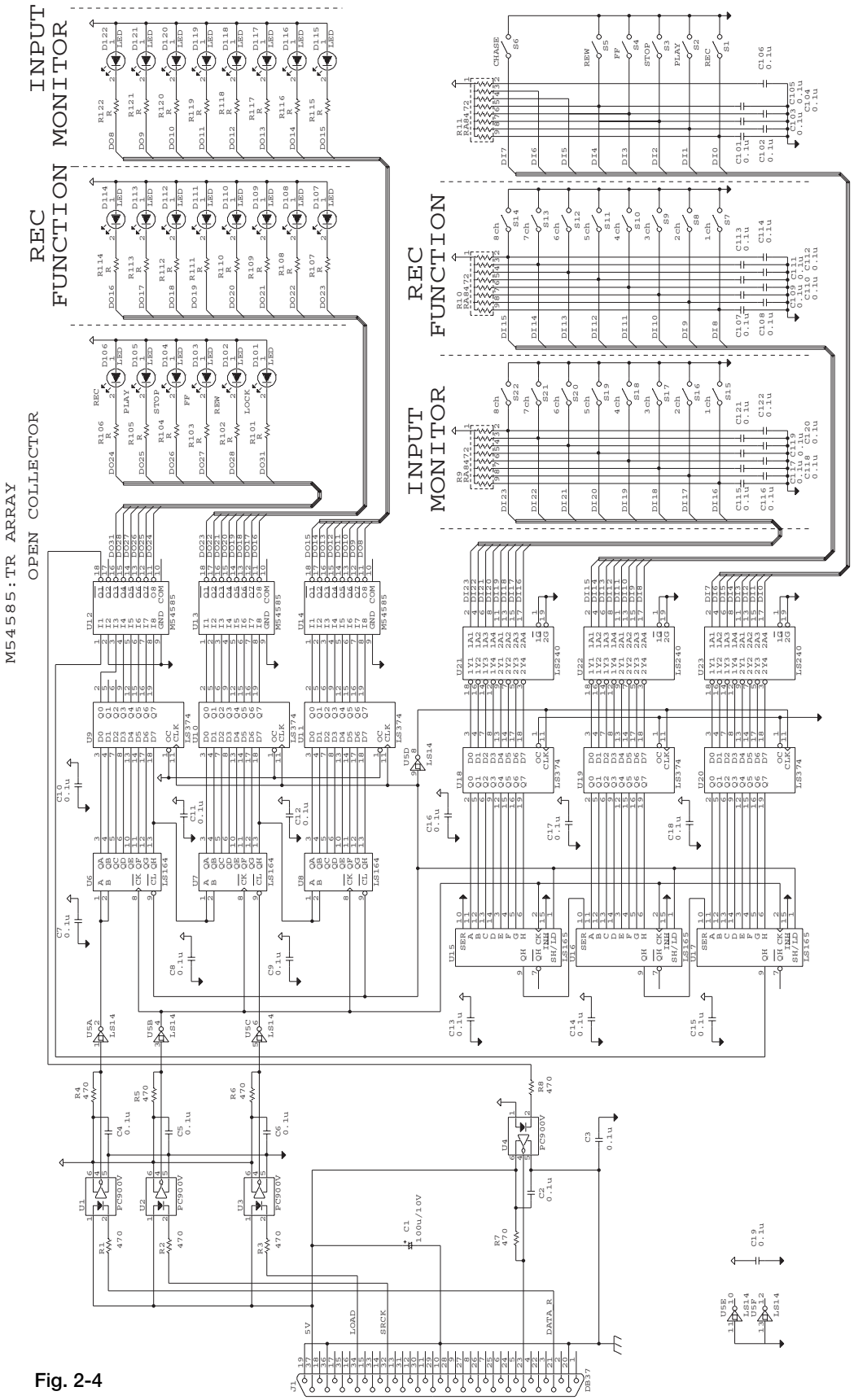


Fig. 2-4

3. ASSEMBLING THE MECHANISM ASS'Y

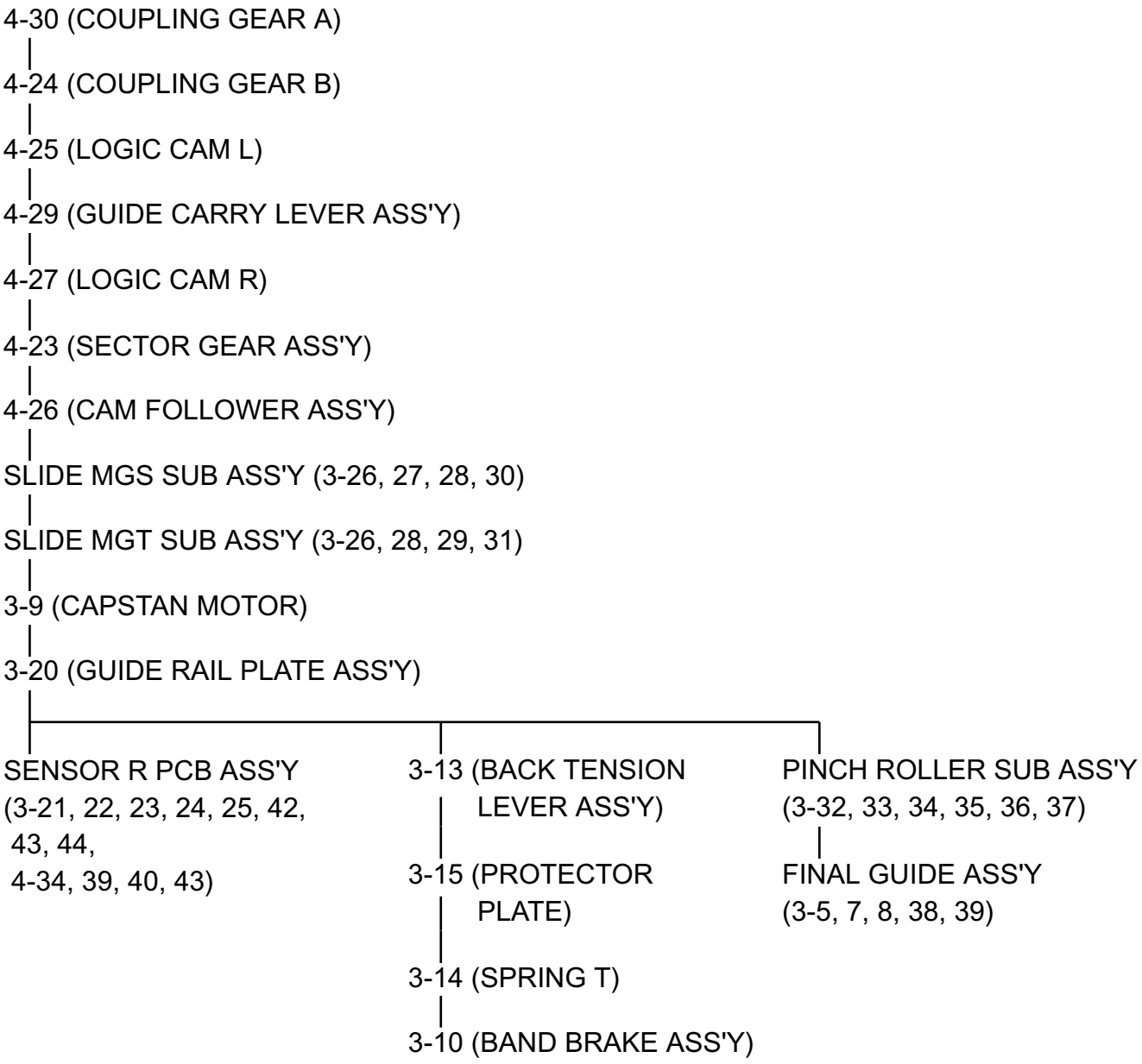
メカ ASS'Yの組立

3-1. Flowchart of assembling

For parts that require caution when reassembling the mechanism ass'y (especially critical gear meshes), a flowchart showing the order of installation is showed below. Disassembly should be performed in the reverse order of reassembly. As parts are indicated using reference numbers, refer to EXPLODED VIEWS -3 and -4 (☞ pages 45 & 47) for identification.

3-1. 組立のフローチャート

メカASS'Yの組立の際、取付け時に注意が必要な部品（特にギヤの噛み合わせ位置が重要）について、取付けの順番を示したフローチャートを以下に記します。
尚、分解は取付けの逆の順番で行って下さい。
また、部品は部番で示しますので、部番につきましては、EXPLODED VIEW-3, -4（☞ 45, 47ページ）を参照してください。



3-2. Installation of the mechanical parts

For parts that require caution when reassembling the mechanism ass'y(especially critical gear meshes), the following is showed.

[For order of installation, see flowchart (☞ page 15) and EXPLODED VIEWS -3 and -4 (☞ pages 45 & 47).]

1. Installing COUPLING GEAR B (4-24), and COUPLING GEAR A (4-30)

   As shown in Fig. 3-1, install 4-24 and 4-30 so that the two marks are visible.

2. Installing LOGIC CAM L (4-25) , and GUIDE CARRY LEVER ASS'Y (4-29)

   1) Install 4-25 so that hole ⓒ in 4-25 in Fig. 3-2 is aligned with hole ⓐ (Fig. 3-1) in the mechanism chassis. (Using a 1 mm dia. rod, pass it through the both holes to see if they are aligned with each other. Whenever checking holes for alignment hereafter, employ this method.)
   2) Similarly, install 4-29 so that hole ⓓ in 4-29 in Fig. 3-2 is aligned with hole ⓑ (Fig. 3-1) in the mechanism chassis.

3. Installing LOGIC CAM R (4-27)

   Install 4-27 so that hole ⓔ in 4-27 in Fig. 3-3 is aligned with the holes (hole ⓓ in 4-29 aligned in 2) of 2 with hole ⓑ in the mechanism chassis).
   At this time, recheck that the holes aligned in 1) of 2 (hole ⓒ in 4-25 and hole ⓐ in the mechanism chassis) are aligned with each other.

3-2. メカ部品の取付け

メカASSYの組立の際、取付け時に注意が必要な部品（特にギヤの噛み合わせ位置が重要）について述べます。

[取付けの順番については、フローチャート（☞ 15ページ）およびEXPLODED VIEW-3, -4（☞ 45, 47ページ）を参照してください。]

1. COUPLING GEAR B（4-24）、COUPLING GEAR A（4-30）の取付け

   4-24, 4-30は図3-1のように、マーク2個が表側になるように取り付ける。

2. LOGIC CAM L（4-25）、GUIDE CARRY LEVER ASS'Y（4-29）の取付け

   1）図3-2の4-25の穴 ⓒとメカシャーシの穴 ⓐ（図3-1）が一致するように、4-25を取り付ける。
   （1mm径の棒で両方の穴を貫通させるようにすると一致したかを確認することができます。以下、穴位置の一致を確認するときは、この方法で行ってください。）
   2）同様に、図3-2の4-29の穴 ⓓとメカシャーシの穴 ⓑ（図3-1）が一致するように、4-29を取り付ける。

3. LOGIC CAM R（4-27）の取付け

   図3-3の4-27の穴 ⓔと、2の2）で一致させた穴（4-29の穴 ⓓとメカシャーシの穴 ⓑ）が一致するように、4-27を取り付ける。
   このとき、2の1）で一致させた穴（4-25の穴 ⓒとメカシャーシの穴 ⓐ）が一致していることを再度確認する。

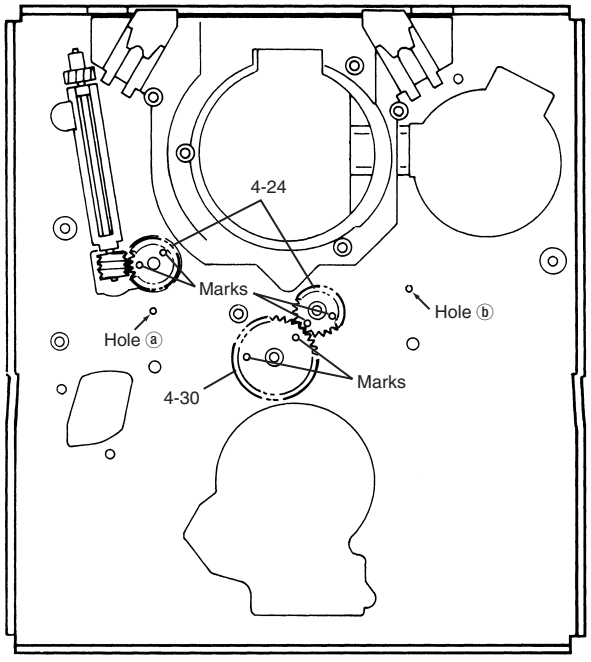


Fig. 3-1

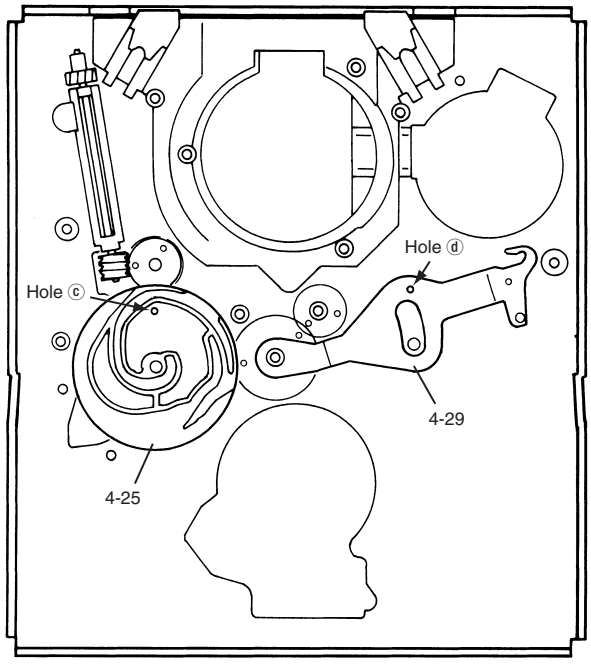


Fig. 3-2

4. Installing SECTOR GEAR ASS'Y (4-23)

Install 4-23 so that hole ⓕ in 4-23 in Fig. 3-3 is aligned with the holes (hole ⓒ in 4-25 aligned in 1) of 2 with hole ⓐ in the mechanism chassis).

5. Installing SLIDE MGS SUB ASS'Y (3-26, 27, 28, 30)

1) As shown in Fig. 3-4, install 3-30 so that mark ⓗ on 3-30 is aligned with mark ⓖ on 4-23.
2) Insert SLIDE MGS into the groove of catcher ⓞ by pushing it from the direction of arrow ⓚ.
(While retracting the lever of 3-30 in the direction of arrow ⓛ with one hand, then with the other hand, push SLIDE MGS towards the groove of catcher ⓞ and release the hands.)

6. Installing SLIDE MGT SUB ASS'Y (3-26, 28, 29, 31)

1) As shown in Fig. 3-4, install 3-31 so that mark ⓙ on 3-31 is aligned with mark ⓘ on 3-30.
2) Insert SLIDE MGT into the groove of catcher ⓟ by pushing it from the direction of arrow ⓜ.
(While retracting the lever of 3-31 in the direction of arrow ⓝ with one hand, then with the other hand, push SLIDE MGT towards the groove of catcher ⓟ and release the hands.)

4. SECTOR GEAR ASS'Y (4-23) の取付け

図3-3の4-23の穴 ⓕと、2の1) で一致させた穴（4-25の穴 ⓒとメカシャーシの穴 ⓐ）が一致するように4-23を取り付ける。

5. SLIDE MGS SUB ASS'Y (3-26, 27, 28, 30) の取付け

1) 図3-4のように、3-30のマーク ⓗと4-23のマーク ⓖが一致するように3-30を取り付ける。
2) SLIDE MGSを矢印 ⓚの方向からキャッチャー ⓞの溝に挿入する。(3-30のレバーを片方の指で矢印 ⓛの方向に戻しながら他方の指でSLIDE MGSをキャッチャー ⓞの溝に挿入し、指を離す。)

6. SLIDE MGT SUB ASS'Y (3-26, 28, 29, 31)の取付け

1) 図3-4のように、3-31のマーク ⓙと3-30のマーク ⓘが一致するように3-31を取り付ける。
2) SLIDE MGTを矢印 ⓜの方向からキャッチャー ⓟの溝に挿入する。(3-31のレバーを片方の指で矢印 ⓝの方向に戻しながら他方の指でSLIDE MGTをキャッチャー ⓟの溝に挿入し、指を離す。)

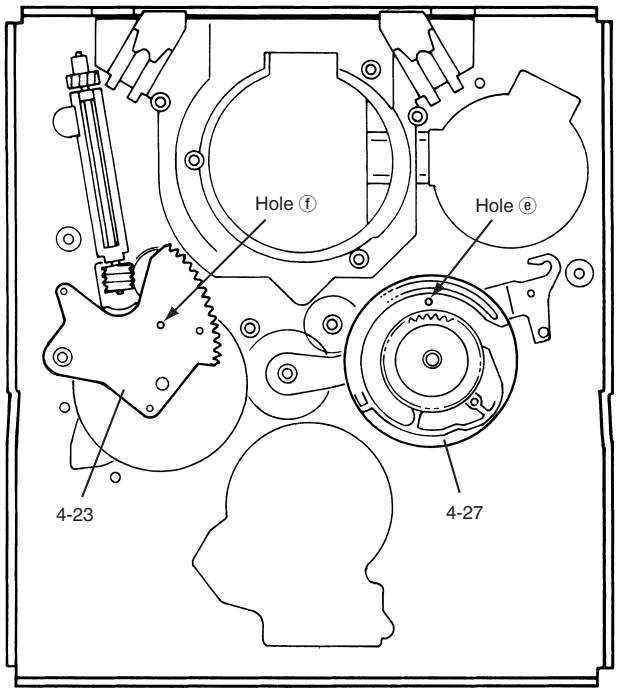


Fig. 3-3

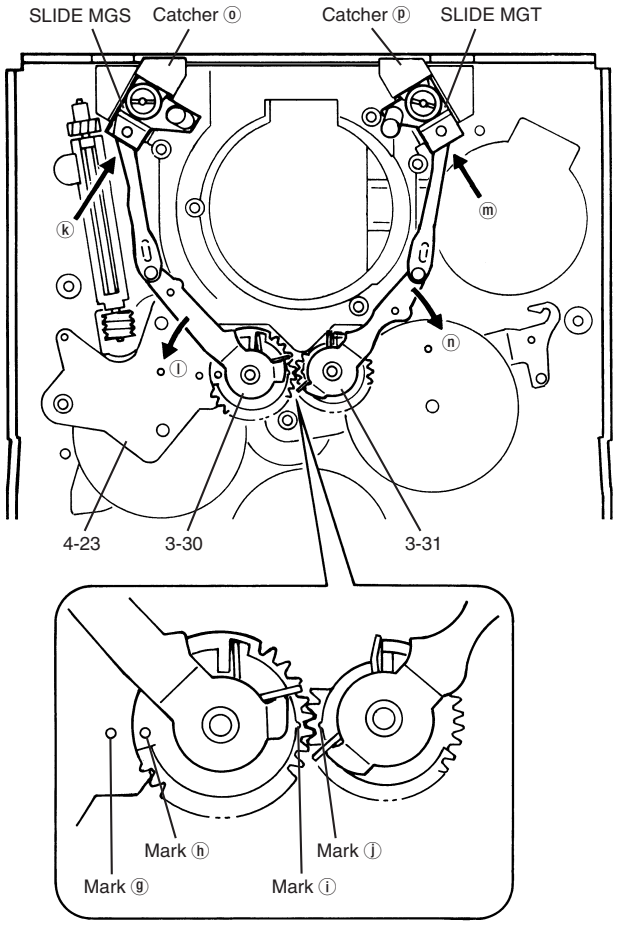


Fig. 3-4

7. Installing MODE SW ASS'Y (3-25)

See Fig. 3-5.

1) Align the U groove in the PCB on the back of the gear of 3-25 with the V groove in the gear by turning the gear.
Note)
For reasons of explanation the illustration shows a view from the gear, but in practice, you cannot see them clearly unless you see them from the PCB.
As a rule of thumb, align the mark on the gear with the U groove in the PCB behind the gear to facilitate the above positioning.
2) Fit 3-25 over the boss on the chassis.

7. MODE SW ASS'Y（3 - 25）の取付け

図3-5参照。

1）3-25のギヤの裏面にあるPCBのU溝にギヤのV溝がくるように、ギヤを回してセットする。
注）図では、説明のためギヤ面から見たイラストが書いてありますが、実際にはPCB面から見ないとよく確認することはできません。
尚、図のギヤのマークをギヤの裏面にあるPCBのU溝の位置に合わせるようにすると、上記位置合わせの目安になります。
2）3-25をシャーシの軸に挿入する。

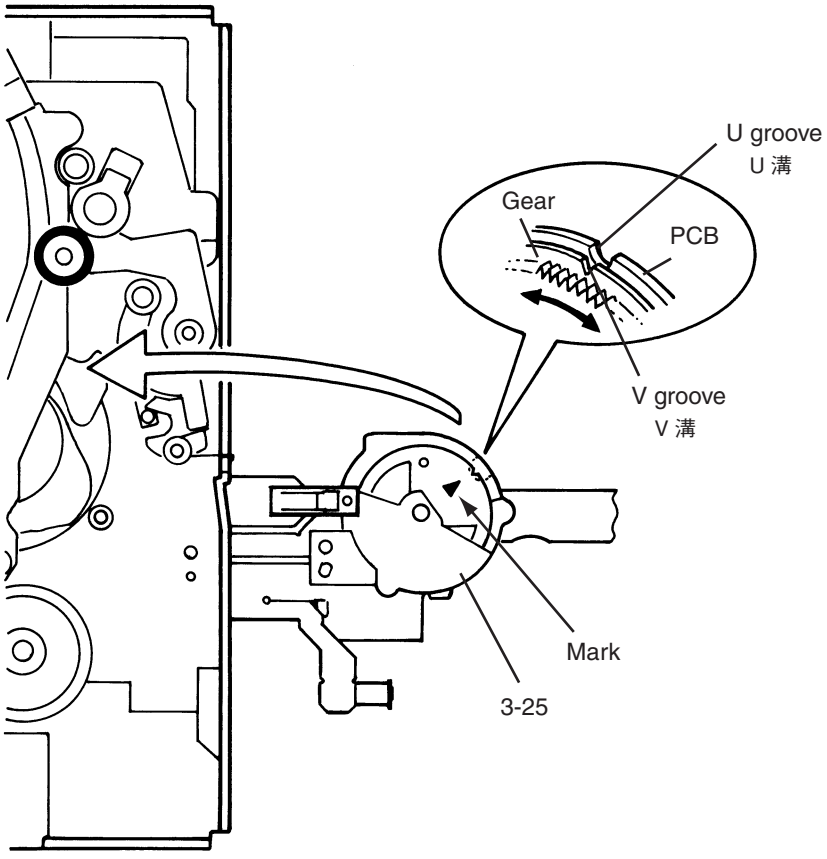


Fig. 3-5

8. Installing BAND BRAKE ASS'Y (3-10)

1) Before installing 3-10, fit COIL SPRING (3-11) to 3-10 as shown in Fig. 3-6.
2) After installing 3-10 as shown in Fig. 3-7, push portion A of 3-11 downward with a rod to disengage it, then hook it over the hook of REEL LOCK LEVER (4-21).

8. BAND BRAKE ASS'Y（3-10）の取付け

1）3-10を取り付ける前に、COIL SPRING（3-11）を図3-6のように3-10に取り付ける。
2）3-10を図3-7のように取り付けた後、3-11のA部を棒で下側に押して外し、その下にあるREEL LOCK LEVER（4-21）のフックに掛ける。

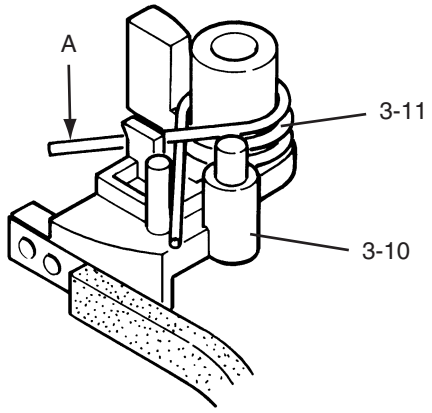


Fig. 3-6

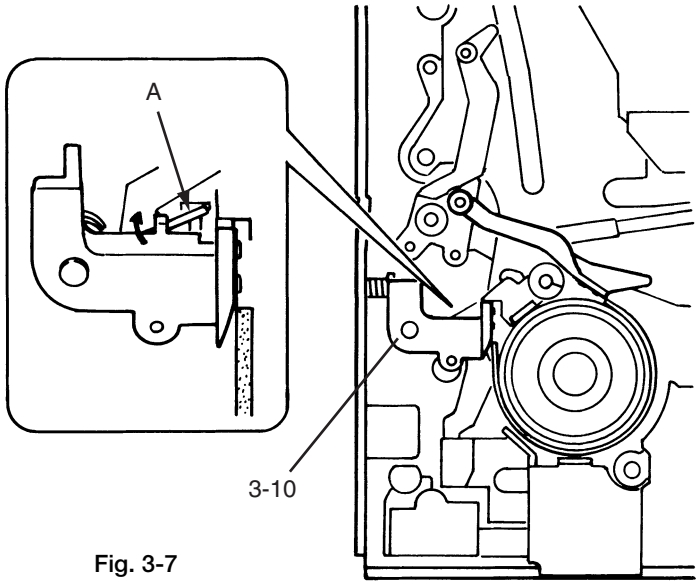


Fig. 3-7

9. Installing PINCH ROLLER SUB ASS'Y

See Fig. 3-8

Fit PINCH ROLLER SUB ASS'Y over the boss on the mechanism chassis, then hook spring edge A over hook B at the edge of the mechanism chassis.

9. PINCH ROLLER SUB ASS'Y の取付け

PINCH ROLLER SUB ASS'Yをメカシャーシの軸に取り付けた後、バネ端Aを図3-8のようにメカシャーシ側面のフックBに掛ける。

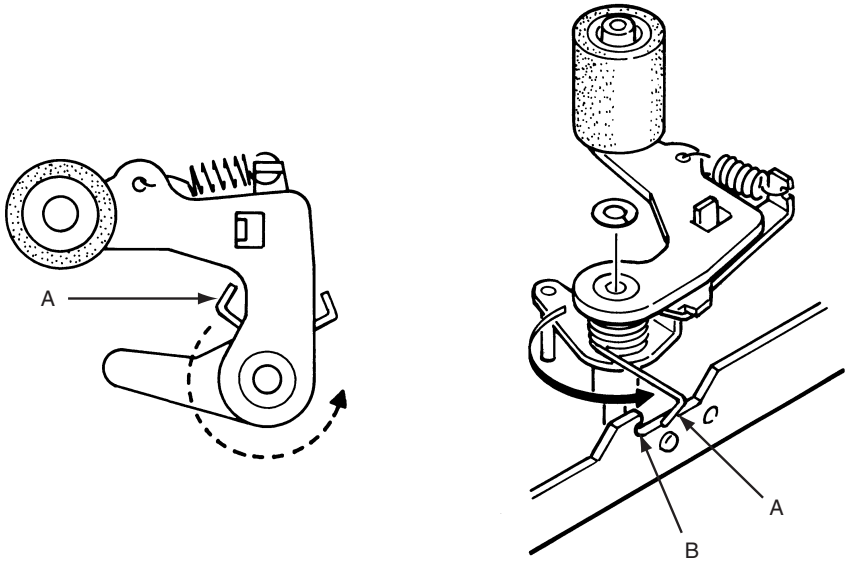


Fig. 3-8

10. Final checking of gear meshes

After installation of all mechanical parts is complete, check to see if gear meshes (items 1 to 7) are proper as follows:

1) Insert a 1 mm dia. rod into hole ' in Fig. 3-9, and check to see if it passes through up to the hole in the mechanism chassis.
2) Insert a 1 mm dia. rod into hole , in Fig. 3-9, and check to see if it passes through up to the hole in the mechanism chassis.
3) Check to see if the mark of 4-27 is aligned with the V groove in the MODE SW ASS'Y (3-25) gear as shown in Fig. 3-9.

10. ギヤの噛み合わせ位置最終確認

すべてのメカ部品を取り付けた後、ギヤの噛み合わせ（1～7項）が正しく行われたかを以下のように確認する。

1）図3-9の穴 ⓠに1mm径の棒を差し込んだとき、メカシャーシの穴まで貫通することを確認する。
2）図3-9の穴 ⓡに1mm径の棒を差し込んだとき、メカシャーシの穴まで貫通することを確認する。
3）図3-9のように、4-27のマークがMODE SW ASS'Y（3-25）のギアのV溝に合っていることを確認する。

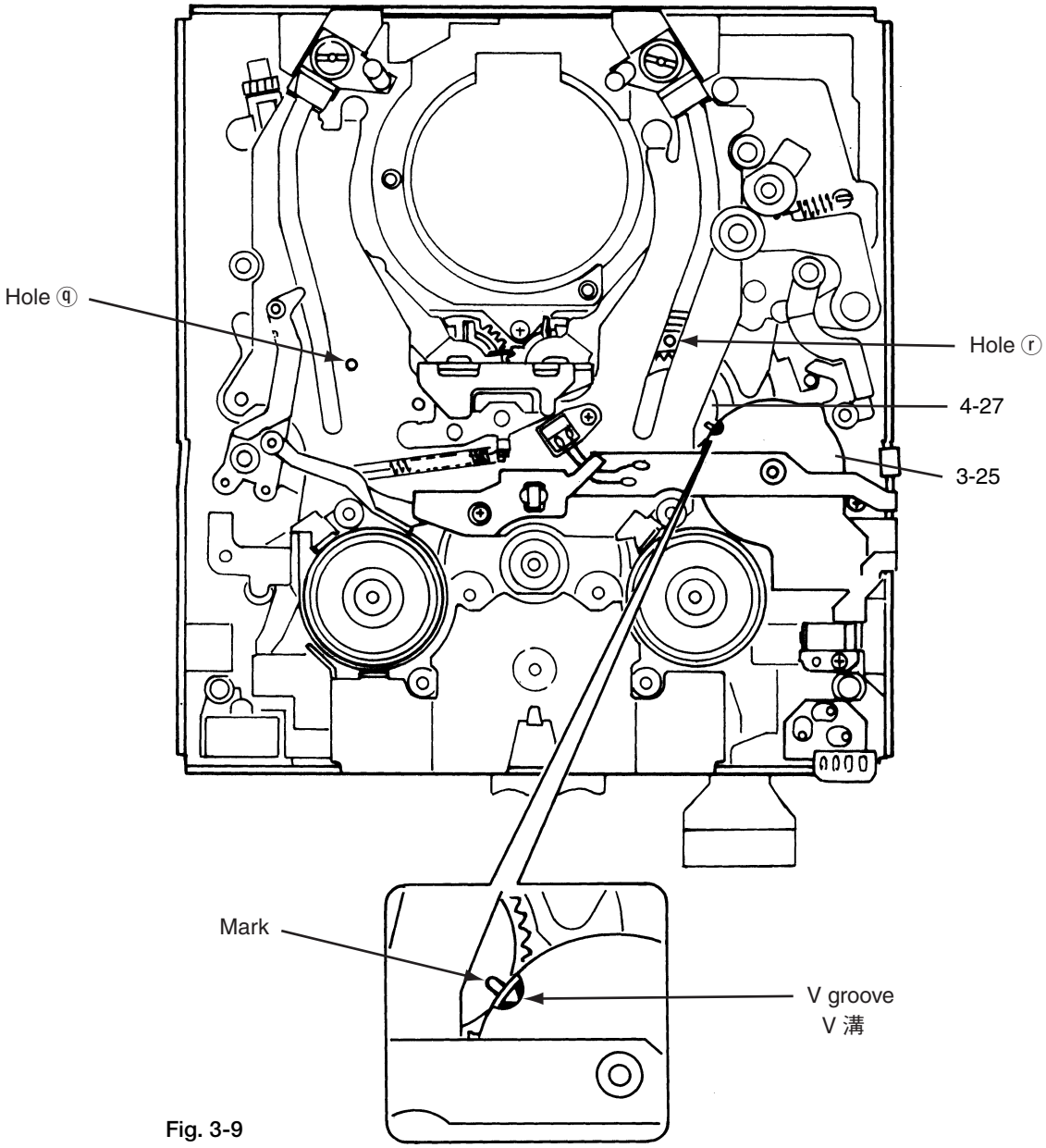


Fig. 3-9

11. Replacing BRUSH ASS'Y (4-33)

With the DS-D98, the drum is grounded through the sliding action of a slip ring and brush in place of through a single contact point which is the case with previous DTRSs. Therefore, when BRUSH ASS'Y (4-33) has been used for the specified hours, its performance can no longer be guaranteed, eventually leading to fracture of the brush. To prevent this, make sure to replace BRUSH ASS'Y when replacing DRUM ASS'Y.

The replacement timing is about 1000 hours which is the same as that of DRUM ASS'Y.

As the worn debris is accepted by COVER, BRUSH (4-45), also be sure to remove the debris when replacing BRUSH ASS'Y.

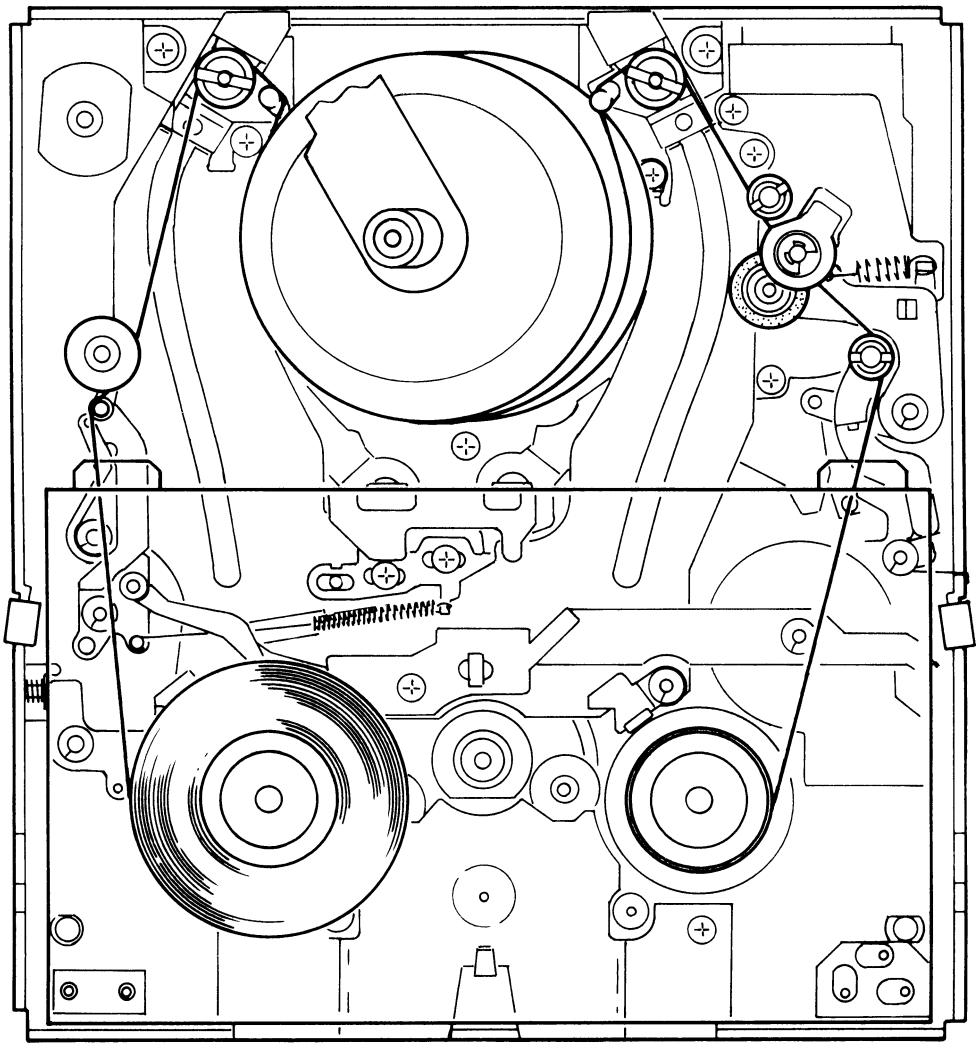
11. BRUSH ASS'Y（4-33）の交換について

DS-D98のドラムアースは、従来のDTRSのような接点式ではなく、スリップリングとブラシの摺動によっています。従って、BRUSH ASS'Y（4-33）の使用時間が限度を超えると磨耗により性能が保証できなくなり、最終的には切断してしまいます。そこで、ドラムASS'Y交換時には、必ずこのBRUSH ASS'Yの交換を行ってください。

交換周期は、ドラムASS'Y交換周期と同じ約1000時間です。

また、磨耗粉をCOVER, BRUSH（4-45）で受けるようになっていますので、BRUSH ASS'Y交換の際は磨耗粉の除去も行ってください。

4. MECHANISM ADJUSTMENTS
機構部調整



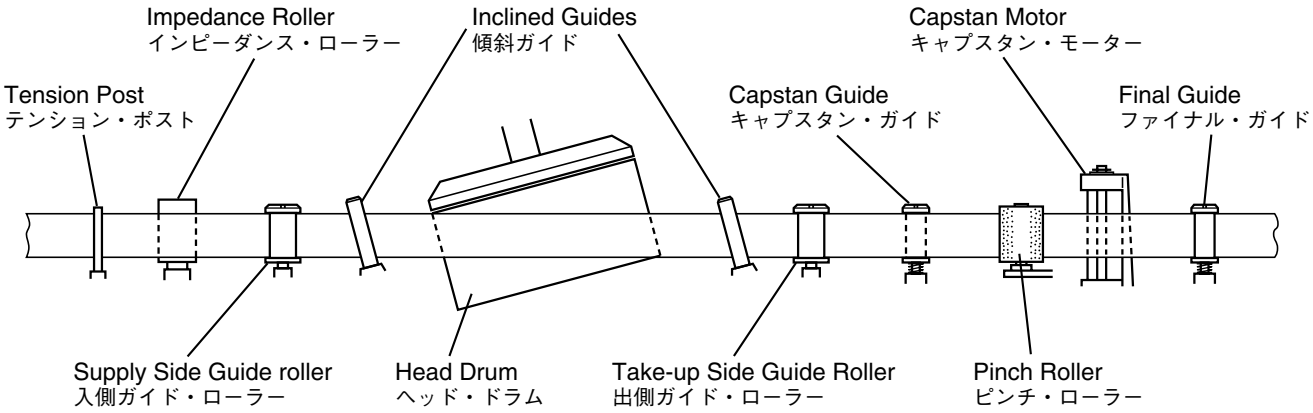


Fig. 4-1

4-1. Preparation

1. Cleaning the head drum (See Fig. 4-2)
   Press a cloth moistened with alcohol against the surface of the head drum, and clean the drum by turning it counter-clockwise with the fingers.
   Notes)
   - To turn the drum, insert a clip (or other appropriate piece) into the hole (ϕ1) in the drum shaft, and turn the clip, as shown in the figure.
   - When cleaning the head drum, be careful not to damage the head chip. It might be damaged if you apply a longitudinal force to it or turn it clockwise.
   - After cleaning the head drum, use a dry cloth to wipe off any residual alcohol (because when it vaporizes, condensation could occur). The tape would stick to the drum if its surface is wet, causing damage to the tape.

4-1. 準備

1. ヘッドドラムのクリーニング（図4-2参照）
   ヘッドドラムの表面にアルコールで浸した布をあて、ドラムを反時計方向に指で回してクリーニングする。
   注）
   - ドラムは、図のようにシャフトの穴（ϕ1）にクリップ等を差し込み、それを回すことにより回ります。
   - クリーニングするとき、ヘッドチップを破損しないように充分注意すること。ヘッドチップの上下方向に力を加えたり、ドラムを時計方向に回すと破損の可能性があります。
   - アルコールでクリーニングした場合は、アルコールが充分乾燥してからテープをローディングしてください。アルコールでクリーニングした後、乾いた布で乾拭きすることをお勧めします。（アルコールの気化時に結露が発生する可能性があるため）
     ドラム表面が濡れていると、ドラムにテープがはりつきテープダメージの原因となります。

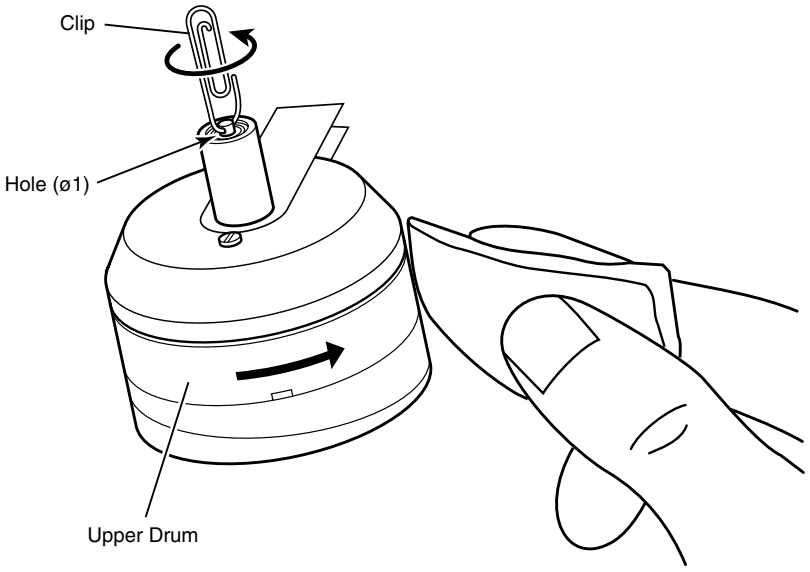


Fig. 4-2

2. Connecting the oscilloscope
   Connect CH1 of the oscilloscope to TP3 (RF A-HEAD) or TP4 (RF B-HEAD) on the RF PLAY PCB and CH2 to TP601 (SWP) on the SYS PCB. (See Fig. 5-1)

2. オシロスコープの接続
   オシロスコープのCH1をRF PLAY PCBのTP3（RF A-HEAD）またはTP4（RF B-HEAD）に、CH2をSYS PCBのTP601（SWP）に接続する。（図5-1参照）

4-2. Test tape

1. TEAC MTT-86131 : For adjusting the torque
2. TEAC MTT-88101(Fs=44.1 kHz):
   For adjusting the error rate and the RF level

4-2. テストテープ

1. TEAC MTT-86131 : トルク調整用
2. TEAC MTT-88101（Fs=44.1 kHz）:
   エラーレート、RFレベル調整用

4-3. Adjusting the tension arm position

1. Load a torque cassette MTT-86131, then set the DS-D98 to PLAY mode.
2. Using a Phillips screwdriver, turn adjust screw A (Fig. 4-3), then align the center of the semicircular portion of the tension arm to the guide rail edge.
   This should fall within range A to C (see Fig. 4-3).

4-4. Adjusting the torque

1. Load a torque cassette MTT-86131, then set the DS-D98 to PLAY mode.
2. Confirming the FWD back tension
   1) Read the torque value at the supply-reel (white) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard value: 10 to 12 g.cm
      Fluctuation range: 3 g.cm or less
   2) If the standard value is not satisfied, remove the torque cassette, loosen screws B (two) in Fig. 4-3 and adjust by moving the protector plate to the left and right. If moved to the left, the torque is reduced, whereas if moved to the right, it increases.
   3) Repeat 1 to 3 until the values fall within the standard.

4-3. テンションアーム位置調整

1. トルクカセットMTT-86131を装着し、PLAYモードにする。
2. プラスドライバーで調整ネジA（図4-3）を回し、テンションアームの半月部の中心をガイドレールエッジに合わせる。
   変動はA ～ Cの範囲であること。（図4-3参照）

4-4. トルク調整

1. トルクカセットMTT-86131を装着し、PLAYモードにする。
2. FWDバックテンションの確認
   1）サプライリール台（白）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。
      規格値: 10 ～ 12 g・cm
      変動幅: 3 g・cm以下
   2）もし規定値を満足しないときは、トルクカセットを外し、図4-3のネジB 2本を緩めプロテクタプレートを左右に動かして調整する。左に動かすとトルクが弱くなり、右に動かすと強くなります。
   3）1～3項を規格に入るまで繰り返す。

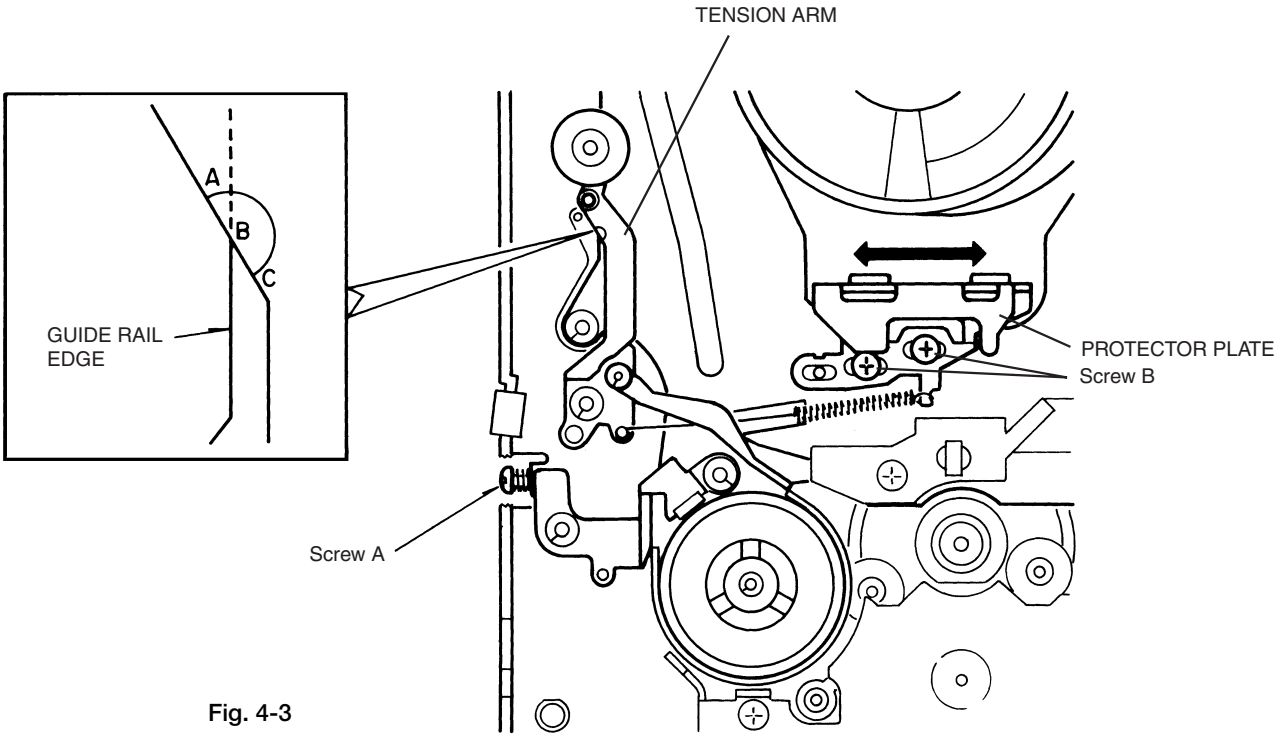


Fig. 4-3

3. Confirming the take-up torque of the take-up reel
   1) Read the torque value at the take-up reel (black) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard value: 8 to 15 g·cm
      Fluctuation value: 3 g·cm or less
   2) If the standard value is not satisfied, remove the torque cassette, replace the take-up reel table (black), and repeat 1 to 4 until the values fall within the standard.
      Note)
      When reinstalling, be sure not to forget to reinstall the cut washer.
4. Confirming the REV take-up torque
   1) Press the SHUTTLE switch, then turn the SHUTTLE knob to the left. Read the torque value at the supply-reel (white) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard range: 18 to 28 g·cm
      Fluctuation range: 3 g·cm or less
   2) If the standard value is not satisfied, remove the torque cassette, replace the supply-reel table (white), and repeat 1 to 5 until the values fall within the standard.
      Note)
      When reinstalling, be sure not to forget to reinstall the cut washer.
   3) Read the torque value at the take-up reel (black) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard range: 8 to 25 g·cm
      Fluctuation range: 3 g·cm or less

＊Cautions when replacing the reel table

When removing the supply-reel table or take-up reel table, the disk reflector (4-3 on page 47) beneath the reel table may also be disengaged as well.

In such a case, see that the polyethylene slider washer (4-55 on page 47) remains on the reel table shaft (mechanism chassis) without fail.

If the disk reflector is affixed over the reel table shaft with the polyethylene slider washer stuck on the backside of the disk reflector, the polyethylene slider washer may NOT fit over the reel table shaft but enter the mechanism chassis.

4-5. Adjusting the tape travel

When adjusting the height of each roller guide, be sure to slightly loosen the screws securing the guide beforehand.

After adjustment is complete, tighten the screws using a torque driver. Observe a tightening torque of 200 g·cm.

Torque driver: 0.2 to 1.5 kg; parts No. 5772827800

(Torque driver bit: M2 (+); parts No. 5772828000)

3. テイクアップリール巻取りトルクの確認
   1）テイクアップリール台（黒）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。
      規定値：8 〜15 g・cm
      変動幅：3 g・cm以下
   2）もし規定値を満足しないときは、トルクカセットを外し、テイクアップリール台（黒）を交換し、1〜4項を規格に入るまで繰り返す。
      注）取付け時、カットワッシャーの取付を忘れないこと。
4. REV巻取りトルクの確認
   1）SHUTTLEキーを押し、SHUTTLEノブを左に回す。そのときのサプライリール台（白）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。
      規定値: 18 〜 28 g・cm
      変動幅: 3 g・cm以下
   2）もし規定値を満足しないときは、トルクカセットを外し、サプライリール台（白）を交換し、1〜5項を規格に入るまで繰り返す。
      注）取付け時、カットワッシャーの取付を忘れないこと。
   3）テイクアップリール台（黒）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。
      規格値: 8 〜 25g・cm
      変動幅: 3 g・cm以下

＊リール台交換時の注意

サプライリール台またはテイクアップリール台を外すとき、リール台の下のディスクリフレクタ（47ページ 4-3）が一緒に外れることがあります。

その場合は、必ずポリスライダワッシャ(47ページ 4-55)がリール台軸（メカシャーシ）に残っていることを確認してください。

ディスクリフレクタの裏側にポリスライダワッシャがついたまま、リール台軸にディスクリフレクタを挿入すると、ポリスライダワッシャがリール台軸に挿入されずメカシャーシに混入してしまうおそれがあります。

4-5. テープ走行調整

各回転ガイドの高さを調整する場合は、必ず回転ガイドを止めているネジを少し緩めてから行ってください。

調整後は、そのネジをトルクドライバーにより締め付けること。締め付けトルクは、200g・cm厳守のこと。

トルクドライバー 0.2〜1.5kg : 品番 5772827800

（トルクドライバー用ビット M2（＋）: 品番 5772828000）

1. Load the test tape MTT-88101, then set the DS-D98 to PLAY mode.
2. While observing the A-HEAD waveform using the oscilloscope, fine-adjust the heights of the roller guides at the supply side and take-up side of the drum using a wrench, so that the leading and trailing edges of the RF waveform have virtually the same level as that of the peak portion on the center of the waveform. (See Fig. 4-4)

   Note)

   Be careful not to hold down the roller guide at the supply side too much by way of making the leading edge of the RF waveform flat. Otherwise, it may lead to rounding of the RF waveform during REV mode.
3. So that the tape travels on the lower edge of the capstan guide, adjust the height of the capstan guide.

   The adjustment method is as follows:

   1) Turn the adjustment screw counterclockwise to raise the lower flange.
   2) If tape is curled, turn the screw clockwise to lower the lower flange. Stop turning the screw when the tape curl dissolves.

   Notes)

   - It is acceptable in principle if the tape is confirmed to be free from curl at the lower edge of the guide.
   - Prior to adjustment, be sure to dissolve the screw-locking compound applied to the head of the guide using alcohol. After the adjustment is complete, reapply screw-locking compound.
4. Adjust the height of the final guide so that the tape is free from curl between the take-up side of the capstan and the final guide, and that the tape is NOT curled by the upper and lower edges of the final guide.

   Notes)

   - It is acceptable in principle if confirmation is made only.
   - Prior to adjustment, be sure to dissolve the screw-locking compound applied to the head of the guide using alcohol. After the adjustment is complete, reapply screw-locking compound.

1. テストテープ MTT-88101を装着し、PLAYモードにする。
2. オシロスコープでA-HEADの波形を観測しながらドラム入口、出口の回転ガイドの高さを二股レンチにより調整し、RF波形の入口、出口が中央の最大部分とほぼ同じ高さ（フラット）になるように（図4-4）、ドラム入口、出口の回転ガイドの高さを微調整する。

   注）RF波形の入口側をフラットにするために入口の回転ガイドを押さえすぎないこと。REV時のRF波形のつぶれの原因となります。

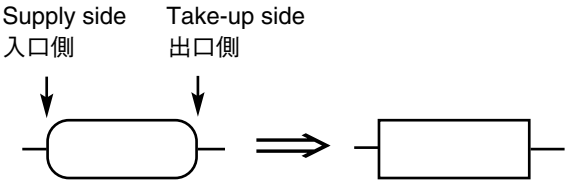


Fig. 4-4

3. キャプスタンガイドの下エッジをテープが走行するように、キャプスタンガイドの高さを調整する。

   調整方法は以下の通り。

   1）下フランジを一度上に上げるように調整ネジを左に回す。
   2）テープのカールが確認できたらネジを右に回して下フランジを下げてゆき、テープのカールがなくなった時点で調整を止める。

   注）調整する場合は、必ずガイド頭部のネジロックをアルコールで溶かしてから行ってください。
   調整後は、必ずネジロックをすること。
4. キャプスタン出口からファイナルガイドの間でテープのよじれがなく、またファイナルガイドの上下エッジでテープがカールしないように、ファイナルガイドの高さを調整する。

   注）
   - 原則は確認のみでOKです。
   - 調整する場合は、必ずガイド頭部のネジロックをアルコールで溶かしてから行ってください。
     調整後は、必ずネジロックをすること。

5. Linearity check
   1) Set the unit to the VTR mode (☞ page 6).
   2) When the unit is in the VTR mode, the level fluctuates spontaneously.
      At this time, check that the shape of the waveform remains consistent while the level is changes.
      If it doesn't, fine-adjust the guide rollers located at the entrance and exit of the drum.
      If the level stops varying, set the unit to the track-off mode so that the level continues to vary. (see below.)

   (How to Set the Track-Off Mode)
   ① Set the unit to the VTR mode.
   ② Select the menu group M in the menu screen, then press ENTER key.
   ③ Move the cursor to "Track Off" and press ENTER key. (The display shows "Track off Mode : off".)
   ④ Press the ▲ key to change the "off" to "manual +0.0".
   ⑤ Press the ▶ key. ("+0.0" will start blinking.)
   ⑥ Using the ▲ and ▼keys, change the display within the limits of from -0.5 to +0.5.

6. Final checking of each guide
   1) Confirm that the upper edge travel regulation is observed for the roller guide at the supply side of the drum.
   2) Confirm that the upper edge travel regulation is observed for the roller guide at the take-up side of the drum.
      Note)
      - Gently push the head of the roller guides at the supply side and the take-up side of the drum in the direction of the rear of the mechanism using a bamboo skewer, then confirm that the waveform in 2 will resume soon (within one second) when the bamboo skewer is released. If the waveform does NOT quickly resume, upper edge tape travel regulation is roughly made; fine-adjustment is necessary.
      - If dirt is adhered to the roller guides, the level will fluctuate while they turn.
        In such a case, moisten a cotton swab with alcohol, and clean the roller guides.
   3) Confirm the lower edge travel regulation for the capstan guide.
      Note) Play an ME tape and make adjustments as described in item 3 on page 26, then check again.
   4) Confirm the upper and lower edge travel regulation for the final guide (the tape should be free from curl).

5. 直線性の確認
   1）VTRモードにする。（☞ 6ページ）
   2）VTRモードにすると、レベルがかってに大きくなったり小さくなったりします。このときの波形が形を変えずにレベルだけが大小することを確認する。そうでない場合は、ドラム入口、出口の回転ガイドを微調整する。
      もし、レベルが大小を繰り返さないようならば、以下の方法でトラックオフさせるとレベルが変化するよになります。

   （トラックオフのさせ方）
   ① VTRモードにする。
   ② メニュー画面で、メニューグループMを選択し、ENTERキーを押す。
   ③ “Track Off” にカーソルを合わせて ENTERキーを押す。（Track off Mode : off 表示）
   ④ ▲キーを押す。（off → manual +0.0 表示）
   ⑤ ▶キーを押す。（+0.0 点滅）
   ⑥ ▲または▼キーにより、表示を－0.5 ～ ＋0.5の範囲で変化させる。

6. 各ガイドの最終チェック
   1）ドラム入口回転ガイドの上エッジ走行規制を確認する。
   2）ドラム出口回転ガイドの上エッジ走行規制を確認する。
   注）● 入口回転ガイドおよび出口回転ガイドの上部をメカ後部方向に竹串で軽く押し、竹串を離したとき、すぐ（1秒以内）に2項の波形に戻ることを確認する。波形がすぐに戻らない場合は、上エッジテープ走行規制が甘いので微調整する必要があります。
      ● 回転ガイドにゴミが付着しているとガイド回転時にレベル変動を生じます。この場合は、綿棒にアルコール塗布し、回転ガイドをクリーニングしてください。
   3）キャプスタン部ガイドの下エッジ走行規制を確認する。
      注）MEテープを走行させ、26ページの3項の調整を再度行って確認する。
   4）ファイナルガイドの上下エッジ走行規制（テープのカールが無いこと）を確認する。

4-6. Confirming the travel in F.FWD, REW and REV modes

1. In all modes, including F.FWD, REW and REV/SHUTTLE, confirm that the tape is free from damage at each guide.
   Note)
   - If, in F.FWD mode, the impedance roller generates a strange noise, replace it.
   - If the leading edge of the playback RF waveform is slow to rise up (the waveform gradually increases in level), or the tape curl is excessive during reverse mode, choose a polyethylene slider washer (beneath the impedance roller) from the following three washers and adjust the height of the impedance roller.
     - 0.13 mm(P/N M00221900A)
     - 0.20 mm(P/N M00222000A)
     - 0.25 mm(P/N M00222100A)
     - No washer

     Observe a screw tightening torque of 500 g•cm.
     Torque driver: 0.2 to 1.5 kg; parts No. 5772827800
     (Torque driver bit: M2 (+); parts No. 5772828000)
2. Load the test tape MTT-88101, then confirm the counter indication in F.FWD and REW modes from the beginning to the end of the tape. See that the counter indication is not a continuous bar indication "---". (Momentary bar indication is acceptable.)

   In the case of a continuous bar indication, refer to the following:

4-6. FF, REW, REVモードでの走行確認

1. FFモード、REWモード、REV/SHUTTLEモードなどすべてのモードで、各ガイドでのテープダメージが無いことを確認する。
   注）● FF時、インピーダンスローラーの回転異音がある場合は交換する。
   ● 再生RF波形の立ち上りが遅い（波形が徐々に大きくなる）場合や、リバース時にテープのカールが著しい場合は、インピーダンスローラーの下に敷いてあるポリスライダワッシャを次の4種類のうちから選択し、インピーダンスローラーの高さを調整する。
     ・0.13mm(品番M00221900A)
     ・0.20mm(品番M00222000A)
     ・0.25mm(品番M00222100A)
     ・ワッシャ無し

     ネジの締め付けトルクは、500g･cm 厳守のこと。
     トルクドライバー 0.2～1.5kg：品番5772827800
     （トルクドライバー用ビットM2（+）：品番5772828000）
2. テストテープ MTT-88101を装着して、FFおよび REWをテープの巻始めから巻終りまで通してカウンタ表示を確認する。カウンタ表示が連続してバー表示“---"にならないことを確認する。（一瞬のバー表示はOKです）連続してバー表示がでる場合は、以下を参照してください。

① Fig. 4-5 shows the normal RF waveform (for both A-HEAD and B-HEAD) in F.FWD or REW mode (reel speed:100 times).

② Fig. 4-6 shows the RF waveform in which the indication will result in a bar indication in 1 mode (the ABS time CANNOT be read due to a missing or distorted waveform).

In such a case, the following measures are required:

- If the waveform is as in Fig. 4-6 in F.FWD mode, replace the soft brake (3-18 on page 45) or coil spring (3-17 on page 45) at the supply reel side.
- If the waveform is as in Fig. 4-6 in REW mode, replace the soft brake (3-18 on page 45) or torsion spring (3-19 on page 45) at the take-up reel side.

③ Fig. 4-7 shows the normal RF waveform in REV mode (capstan feed).

④ Fig. 4-8 shows the RF waveform in which the indication will result in a bar indication in 3 mode (the ABS time CANNOT be read due to a missing or distorted waveform).

In such a case, the following causes are conceivable:

- The roller guide at the supply side of the drum is held down too much. The roller guide needs readjustment.
- The REV take-up torque at the supply reel pad is low. It should be replaced with a reel table with a REV take-up torque of approx. 30 g.cm.

① 図4-5は、FFまたはREWモード（リール送り, 100倍速）時のRF通常波形（A-HEAD, B-HEADとも）です。

② 図4-6は、①のモード時にバー表示（ABSタイムが読めない）になってしまう場合（波形抜けまたは波形つぶれ）のRF波形です。

この場合は、下記の処置が必要です。

- FF時に図4-6の波形になる場合は、サプライリール台側のSOFT BRAKE LEVER ASS'Y（45ページ 3-18）またはCOIL SPRING（45ページ 3-17）を交換してください。
- REW時に図4-6の波形になる場合は、テイクアップリール台側のSOFT BRAKE LEVER ASS'Y（45ページ 3-18）またはTORSION SPRING（45ページ 3-19）を交換してください。

③ 図4-7は、REVモード（キャプスタン送り）時のRF通常波形です。

④ 図4-8は、③ のモード時にバー表示（ABSタイムが読めない）になってしまう場合（波形抜けまたは波形つぶれ）のRF波形です。

この場合は、下記の原因が考えられます。

- ドラム入口の回転ガイドの押さえすぎ。回転ガイドの再調整が必要です。
- サプライリール台のREV巻取りトルクが弱い。REV巻取りトルクが、30g.cm前後のリール台と交換が必要です。

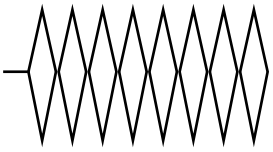


Fig. 4-5

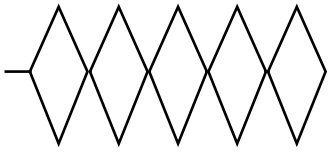


Fig. 4-7

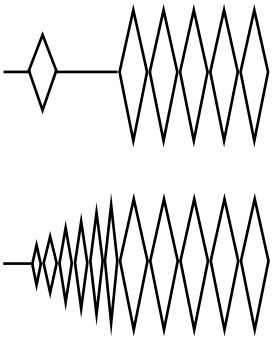


Fig. 4-6

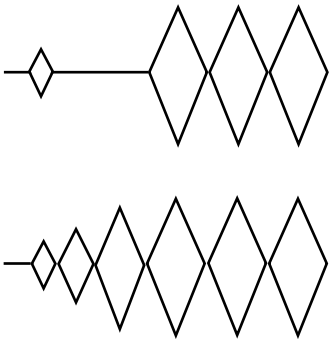


Fig. 4-8

＊Cautions when replacing the drum

When the drum is replaced, be sure to confirm and adjust the following items other than tape travel adjustments.
As for adjustment methods, refer to 5 (ELECTRICAL ADJUSTMENTS):

- Adjustment of the P.G. (phase generator) position
- Playback error rate (MP tape and ME tape)
- Adjustment of the recording current
- R/P error rate (MP tape and ME tape)

Be also sure to replace BRUSH ASS'Y when replacing the drum. (☞ page 21)

＊ドラム交換時の注意

ドラムを交換した場合は、テープ走行調整以外に下記項目の確認・調整を必ず行ってください。
調整方法については、5項（電気系調整）を参照してください。

・P.G.（PHASE GENERATOR）位置調整
・再生エラーレート（MPテープおよびMEテープ）
・記録電流調整
・録再エラーレート（MPテープおよびMEテープ）

また、ドラム交換時には、必ずBRUSH ASS'Yの交換も行ってください。（☞ 21ページ）

5. ELECTRICAL ADJUSTMENTS
電気系調整

5-1. Check and adjustment points

5-1. 測定箇所および調整箇所

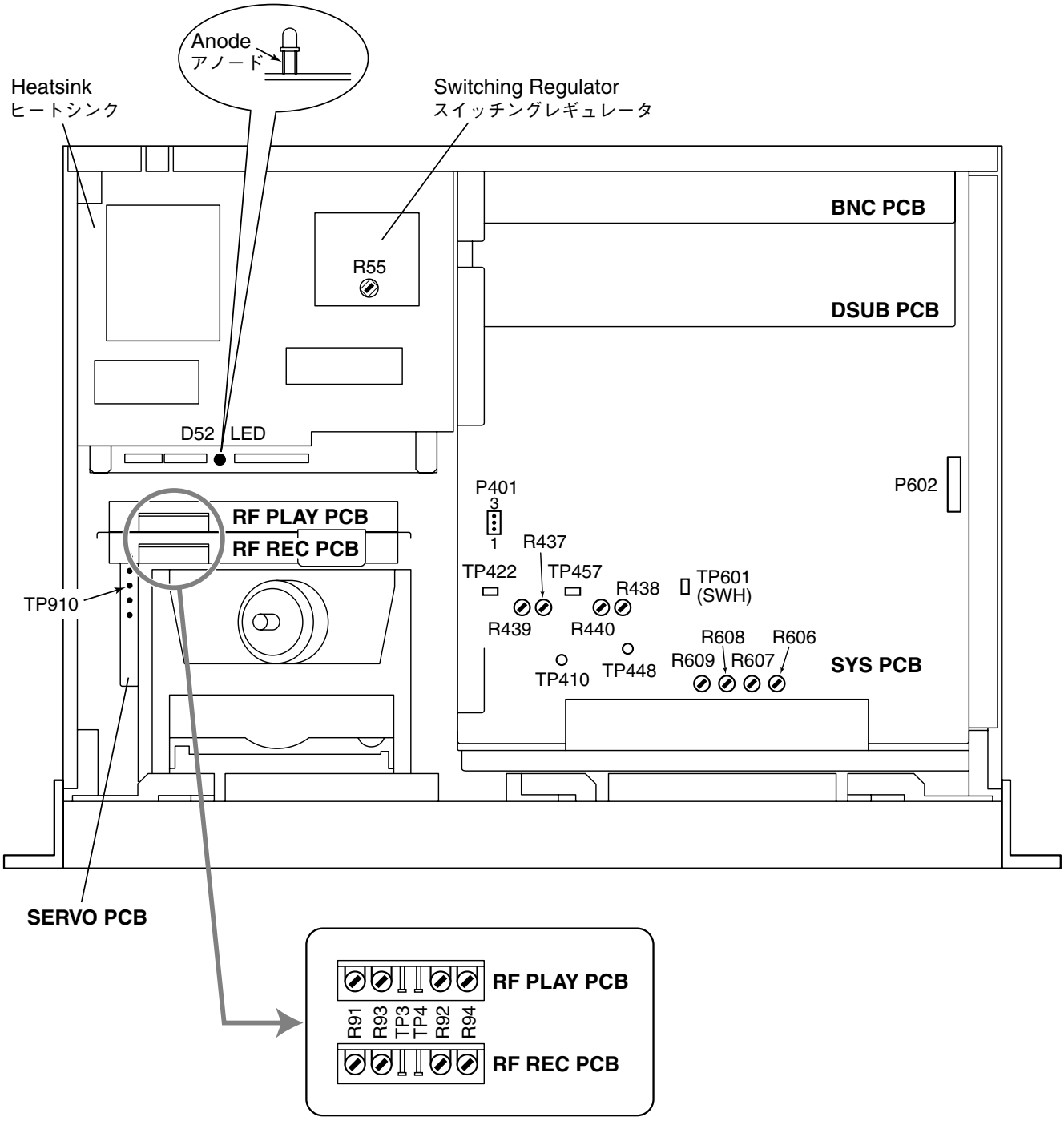


Fig. 5-1

5-2. Test tape

1. TEAC MTT-88101 (Fs=44.1 kHz):
   For adjusting the error rate and the RF level
2. TEAC MTT-88102 (Fs=48 kHz):
   For adjusting the error rate, the RF level,
   and the P.G. position
3. TEAC MTT-88201 : For recording (blank MP tape)
4. TEAC MTT-88202 : For recording (blank ME tape)

5-3. +5 V supply check

1. Connect a digital tester between the heat sink in the switching regulator and the anode of the LED for +5 V supply (D52).
2. Check that the DC voltage reading is +5.1 ± 0.1 V.
3. If voltage is not within these limits, adjust the semi-fixed resistor R55 until correct.

5-4. P.G. (Phase generator) position adjustment

1. Connect CH1 of the oscilloscope to TP410 (RF A-HEAD) on the SYS PCB and CH2 to TP910 (SWP) on the SERVO PCB.
2. Load the test tape MTT-88102.
3. Set the DS-D98 to test mode. (☞ page 6)
4. Select the menu group M in the menu screen.
5. Move the cursor to "PG.AdJuSt" and press ENTER key.
6. Enter the play mode and, using the ▲ and ▼ keys, adjust the lag between the fall of the switching pulse and the end of ATF portion of the RF wave for 250 µsec, as shown in Photo-1.
7. Press STOP, then switch power off to save the setting.
8. Switch on power again, then enter the play mode to check that the lag of 250 µsec is maintained.

5-2. テストテープ

1. TEAC MTT-88101（Fs=44.1 kHz）:
   エラーレート、RFレベル
2. TEAC MTT-88102（Fs=48 kHz）:
   エラーレート、RFレベル、記録位置調整用
3. TEAC MTT-88201 : 記録用MP生テープ（未記録）
4. TEAC MTT-88202 : 記録用ME生テープ（未記録）

5-3. 電源 +5Vの確認

1. スイッチングレギュレーター内のヒートシンクと＋5V用LED（D52）のアノード側間にデジタルテスターを接続する。
2. DC電圧が、＋5.1V±0.1Vであることを確認する。
3. 上記規格内に入っていない場合は、スイッチングレギュレーター内の半固定抵抗 R55で調整する。

5-4. PG（Phase Generator）位置調整

1. オシロスコープのCH1をSYS PCBのTP410（RF A-HEAD）に、CH2をSERVO PCBのTP910（SWP）に接続する。
2. テストテープ MTT-88102を装着する。
3. テストモードにする。（☞ 6ページ）
4. メニュー画面で、メニューグループMを選択する。
5. “PG AdJuSt”にカーソルを合わせ ENTERキーを押す。
6. PLAYモードにして、スイッチングパルスの立ち下がりからRF波形のATF部分の終わりまでが 250 μ secになるように、▲または▼キーを押して調整する。
   （写真-1参照）
7. STOP後、一度電源をOFFして値を記憶させる。
8. 再度電源をONにし、PLAYモードにして250 μ secが変化していないことを確認する。

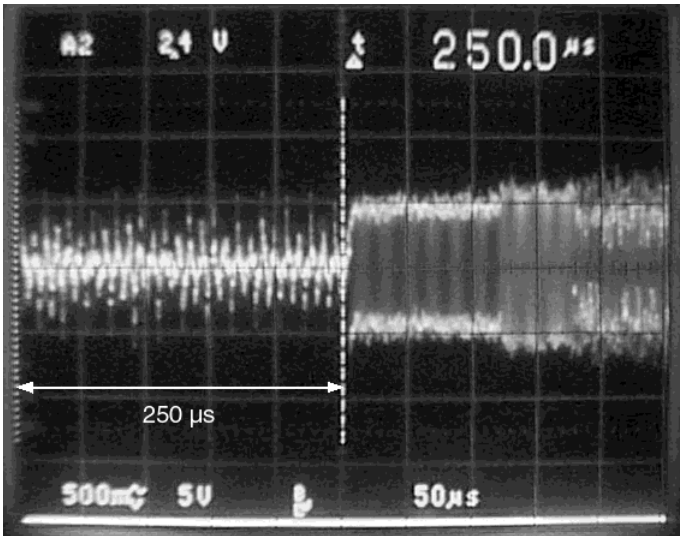


Photo-1

5-5. Offset adjustment in the VCO free-running frequency automatic compensation circuit

1. DTRS mode
   1) Play the MTT-88101 or MTT-88102 test tape.
   2) Short-circuit P401's 1 and 2 on the SYS PCB (A-HEAD placed in test condition).
   3) Connect an oscilloscope to TP422 on the SYS PCB, and adjust the scope range to 1V DC, 0.5 µsec.
   4) Adjust R439 (A-HEAD) on the SYS PCB for 2.5 V DC at TP422.
   5) In a similar way, short-circuit P401's 2 and 3 (B-HEAD placed in test condition), then adjust R440 (B-HEAD) for 2.5 V DC at TP457.
   6) After adjustment is complete, release P401.

   Note)
   In 4) and 5), even if a positive-going or negative-going slight glitch is observed as shown in Fig. 5-2, it should be acceptable. However, perform adjustment to alleviate glitches as much as possible.

5-5. VCOフリーラン周波数自動補正回路のオフセット調整

1. DTRSモード
   1）テストテープ MTT-88101または MTT-88102を再生する。
   2）SYS PCBのP401の1-2間をショートする。
   （A-HEAD テスト状態）
   3）SYS PCBのTP422にオシロスコープを接続し、オシロスコープのレンジをDC 1V, 0.5 µ secにセットする。
   4）TP422のDC電圧が 2.5VになるようにSYS PCBのR439（A-HEAD）を調整する。
   5）同様に、P401の2-3間をショートし（B-HEAD テスト状態)、TP457のDC電圧が 2.5VになるようにR440（B-HEAD）を調整する。
   6）調整後、P401を解放する。

   注）4), 5) 項でオシロスコープの波形が、図5-2のように上または下方向に若干のヒゲが観測されても可とするが、なるべくひげを小さくするように調整する。

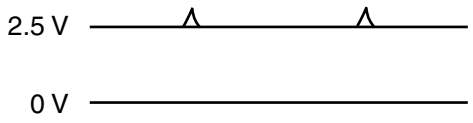


Fig. 5-2

2. HR mode
   1) Play a tape recorded in HR mode.
   2) Short-circuit P401's 1 and 2 on the SYS PCB (A-HEAD placed in test condition).
   3) Connect an oscilloscope to TP422 on the SYS PCB, and adjust the scope range to 1V DC, 0.5 µsec.
   4) Adjust R437 (A-HEAD) on the SYS PCB for 2.5 V DC at TP422.
   5) In a similar way, short-circuit P401's 2 and 3 (B-HEAD placed in test condition), then adjust R438 (B-HEAD) for 2.5 V DC at TP457.
   6) After adjustment is complete, release P401.

2. HRモード
   1）HRモードで記録したテープを再生する。
   2）SYS PCBのP401の1-2間をショートする。
   （A-HEAD テスト状態）
   3）SYS PCBのTP422にオシロスコープを接続し、オシロスコープのレンジをDC 1V, 0.5 µ secにセットする。
   4）TP422のDC電圧が 2.5VになるようにSYS PCBのR437（A-HEAD）を調整する。
   5）同様に、P401の2-3間をショートし（B-HEAD テスト状態)、TP457のDC電圧が 2.5VになるようにR438（B-HEAD）を調整する。
   6）調整後、P401を解放する。

5-6. Playback equalizer adjustment

5-6-1. Checks in Normal mode

1. ME tape
   1) Load Sony ME tape.
   2) Connect the oscilloscope to TP3 (RF A-HEAD) on the RF PLAY PCB , then set the oscilloscope range to 500 mV AC, 50 nsec.
   3) Set REC FUNCTION ON (All channels) and execute format recording in HR mode.
   4) Rewind and play the tape, and observe the eye pattern of A-HEAD.
   5) Adjust R91 on RF PLAY PCB so that the 3.1 MHz waveform is almost flat at top and bottom as shown in Photo-3.
      * Photo-2 shows the eye pattern when the oscilloscope is set to the 50 nsec/div. range.
      * Photo-3 shows the eye pattern when the oscilloscope is set to the 100 nsec/div. range.
   6) Similarly, connect the oscilloscope to TP4 (RF B-HEAD) on the RF PLAY PCB, then observe the eye pattern of B-HEAD.
      For adjustment, use R92 on the RF PLAY PCB.

2. MP tape
   1) Load Sony MP tape.
   2) In the same way as in 1 (adjusting the equalizer using an ME tape), adjust R93 (A-HEAD) and R94 (B-HEAD) on the RF PLAY PCB.

5-6-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-6-1. (The same check, but test points and adjustments not on RF PLAY PCB, but on RF REC PCB.)

5-6. 再生イコライザー調整

5-6-1. ノーマルモードでの確認

1. MEテープ
   1）SONY MEテープを装着する。
   2）RF PLAY PCBのTP3（RF A-HEAD）にオシロスコープを接続し、オシロスコープのレンジを AC 500mV, 50nsecにする。
   3）REC FUNCTION ON（全ch）にし、HRモードでFORMAT記録する。
   4）巻戻して再生したときの A-HEADのアイパターンを観測する。
   5）写真-3のように 3.1MHzの波形の凸凹がほぼフラットになるように RF PLAY PCBの R91を調整する。
      ＊写真-2は、オシロスコープレンジが 50nsec/divの状態です。
      ＊写真-3は、オシロスコープレンジが 100nsec/divの状態です。
   6）RF PLAY PCBの TP4（RF B-HEAD）にオシロスコープを接続し、同様にB-HEADのアイパターンを観測する。
      調整は、RF PLAY PCBの R92で行う。

2. MPテープ
   1）SONY MP テープを装着する。
   2）1項（MEテープ イコライザー調整）と同様の方法で RF PLAY PCBの R93（A-HEAD）, R94（B-HEAD）を調整する。

5-6-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-6-1項と同様の確認を行う。（但し、テストポイント、調整箇所はRF PLAY PCBではなくてRF REC PCBとなります。）

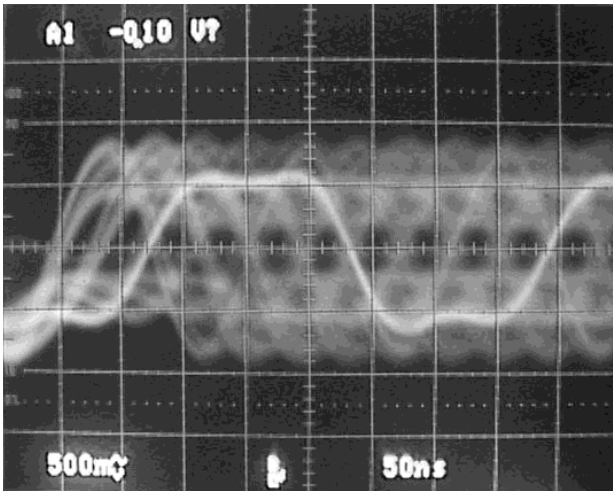


Photo-2. eye pattern (50 nsec/div)

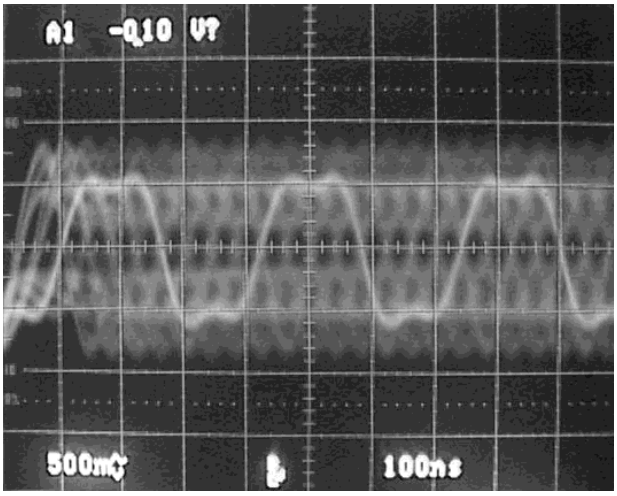


Photo-3. eye pattern (100 nsec/div)

5-7. RF level check

5-7-1. Checks in Normal mode

1. Connect the oscilloscope's CH1 to TP3 (RF A-HEAD) on the RF PLAY PCB and CH2 to TP601 (SWH) on the SYS PCB.
2. Set the oscilloscope's CH1 range to 500 mV AC, 2 msec.
3. Set the oscilloscope's CH2 range to 5 V DC, and (-) trigger.
4. Play the test tape MTT-88101.
5. Observe the waveform at TP3 (RF A-HEAD) , and see that the following standard is satisfied.

   Standard value (see Fig. 5-3):
   B, C (minimum) : 1000 mV or more
   B/A, C/A : 80 % or more

5-7. RFレベル確認

5-7-1. ノーマルモードでの確認

1. オシロスコープのCH1をRF PLAY PCBのTP3（RF A-HEAD）に、CH2をSYS PCBのTP601（SWH）に接続する。
2. オシロスコープの CH1のレンジをAC 500mV, 2msecにセットする。
3. オシロスコープの CH2のレンジをDC 5Vにセットし、（−）トリガーとする。
4. テストテープ MTT-88101を再生する。
5. TP3（RF A-HEAD）の波形を観測し、下記の規格値を満足すること。

   規格値（図5-3参照）
   B, C（最小部）: 1000mV以上
   B/A, C/A　　: 80%以上

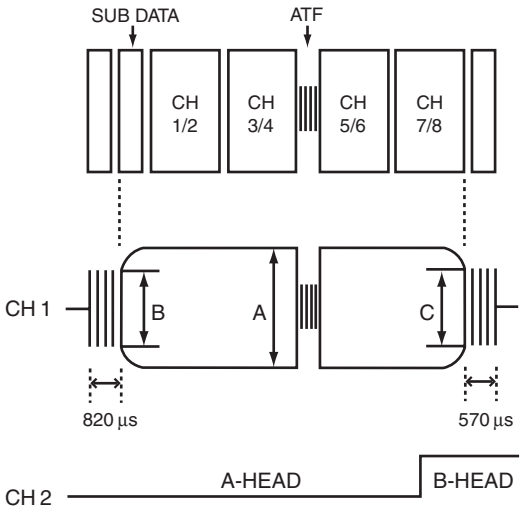


Fig. 5-3

6. Next, set the oscilloscope's CH2 to (+) triggering.
7. Connect the oscilloscope's CH1 to TP4 (RF B-HEAD) on the RF PLAY PCB, then observe the B-HEAD waveform, see that the standard is satisfied:

5-7-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-7-1.

6. 次にオシロスコープのCH2を（+）トリガーにセットする。
7. オシロスコープのCH1をRF PLAY PCBのTP4（RF B-HEAD）に接続して B-HEADの波形を観測し、A-HEADと同様に規格値を満足すること。

5-7-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-7-1項と同様の確認を行う。

5-8. Playback error rate check

5-8-1. Checks in Normal mode

1. ME tape
   1) As shown in Fig. 5-4, connect the ERC-88 error rate counter (P/N:5772926600) to P602 on the SYS PCB via the ERC-78HR adaptor (P/N:V00089100A).
      Note) To supply power to the ERC-88, use the PS-P2 AC adaptor.
   2) Play the MTT-88102 test tape, and check error rate (for both A- and B-HEADS).
      If error rate is out of the following specifications, readjust R91 (A-HEAD) or R92 (B-HEAD) on the RF PLAY PCB. (see paragraph 5-6)

      Standard value : less than 200 x 10^{-4}

5-8. 再生エラーレート確認

5-8-1. ノーマルモードでの確認

1. MEテープ
   1）図5-4のように、SYS PCBのP602にアダプターERC-78HR（品番:V00089100A）を介してエラーレートカウンターERC-88（品番:5772926600）を接続する。
   注）ERC-88には、ACアダプター PS-P2より電源を供給してください。
   2）テストテープ MTT-88102を再生してエラーレート（A-HEAD, B-HEAD共）を確認する。
   エラーレートが下記規格を満足していない場合は、RF PLAY PCBの R91（A-HEAD）または R92（B-HEAD）を再調整する。（5-6項参照）

   規格値 : 200×10^{-4}以下

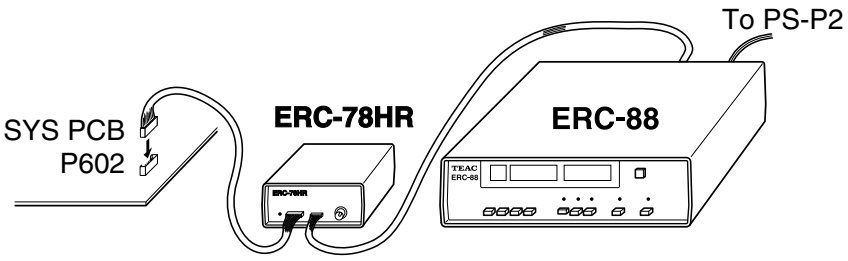


Fig. 5-4

2. MP tape
   Play the MTT-88101 test tape, and confirm the error rate (for both A- and B-HEADS) in the same way as with an ME tape.
   If error rate is out of the following specifications, readjust R93 (A-HEAD) or R94 (B-HEAD) on the RF PLAY PCB. (see paragraph 5-6)

   Standard value : less than 200 x 10^{-4}

2. MPテープ
   テストテ-プ MTT-88101を再生して、MEテープと同様にエラーレート（A-HEAD, B-HEAD共）を確認する。
   エラーレートが下記規格を満足していない場合は、RF PLAY PCBの R93（A-HEAD）または R94（B-HEAD）を再調整する。（5-6項参照）

   規格値 : 200×10^{-4}以下

5-8-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-8-1.

5-8-2. コンフィデンスモードでの確認

コンフフィデンスモードに切換えて、5-8-1項と同様の確認を行う。

5-9. Recording current adjustment

5-9-1. Checks in Normal mode

1. MP tape
   1) Load MP blank tape MTT-88201.
   2) As shown in the Fig. 5-5, connect the REC CURRENT KIT (P/N:V00024700A) between P10 on the MOTHER PCB and P102 on the RF REC PCB.
   3) Set the oscilloscope to 10 mV DC, 50 ns.
   4) Select the menu group 2 in the menu screen.
   5) Move the cursor to "Sine Osc" and press ENTER key.
   6) Press the ▲ key to display "Sine Oscillator 440".

5-9. 記録電流調整

5-9-1. ノーマルモードでの確認

1. MPテープ
   1）MP生テープ MTT-88201を装着する。
   2）図5-5の様に REC CURRENT KIT（品番V00024700A）をMOTHER PCBのP10とRF REC PCBの P102間に接続する。
   3）オシロスコープは、DC 10mV, 50nsに設定する。
   4）メニュー画面で、メニューグループ2を選択する。
   5）“Sine Osc”にカーソルを合わせ、ENTERキーを押す。
   6）▲キーを押して、“Sine Oscillator 440”表示にする。

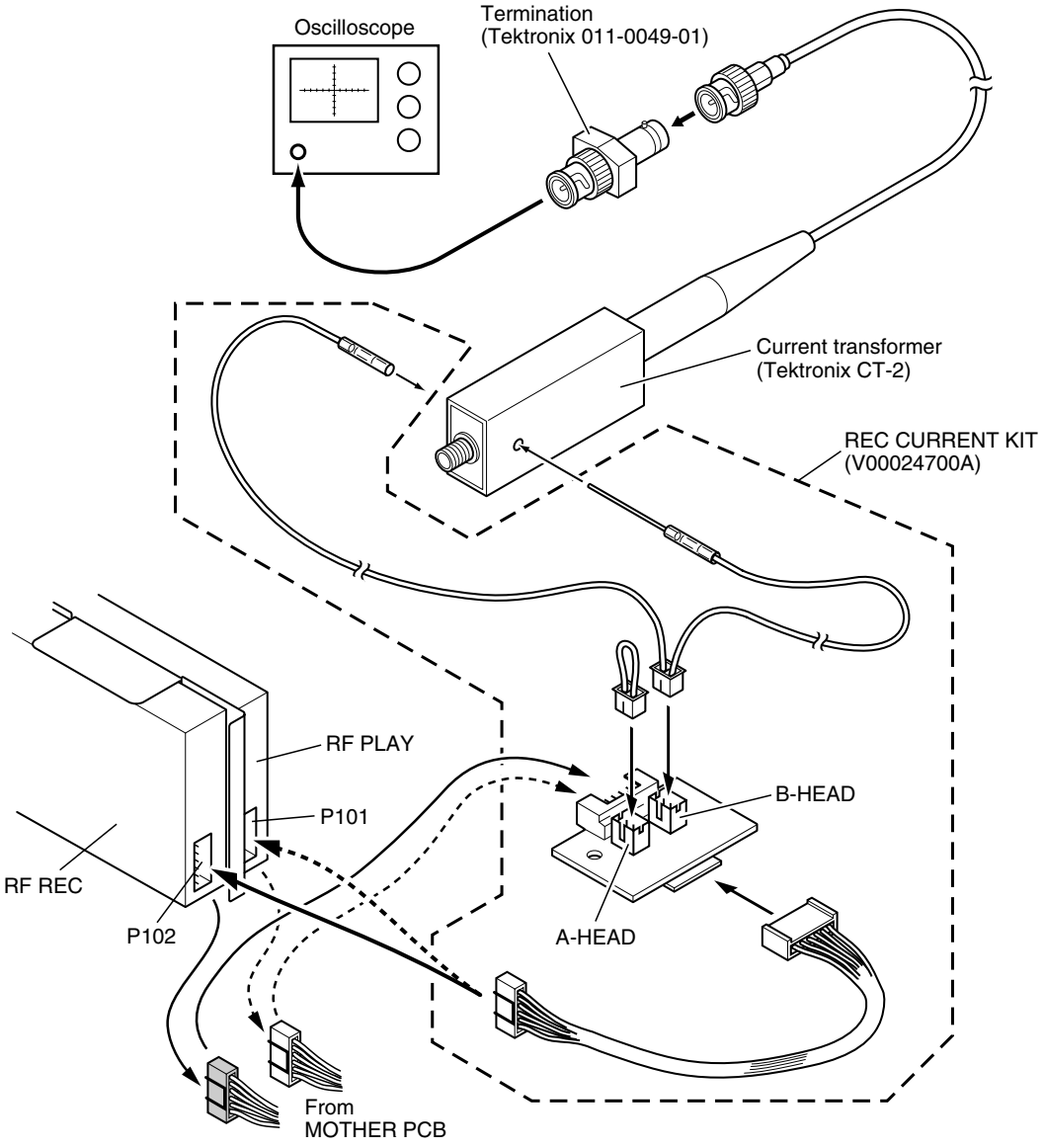


Fig. 5-5

7) Press the ESCAPE key.
8) Enter HR mode and set the REC FUNCTION keys of all channels to ON.
9) Start recording in tape format mode, and adjust R606 on the SYS PCB for 11.2 mAp-p (indication is in voltage) of A-HEAD current.
10) Similarly, adjust R607 for 11.2 mAp-p of B-HEAD current.

Note)
The state in which shorting pins A and B inserted as shown in Fig. 5-5 is one in which current flowing through the B-HEAD is to be measured. The state with shorting pins A and B reversed is one in which current flowing through the A-HEAD is to be measured. For a reference waveform using the oscilloscope, refer to Photo-4.

7）ESCAPEキーを押す。
8）HRモードにし、全CHのREC FUNCTIONキーをONにする。
9）FORMAT 記録状態で、A-HEADの電流値が 11.2 mAp-p（表示は電圧表示）になるようにSYS PCBのR606を調整する。
10）同様に、B-HEADの電流値が 11.2 mAp-pになるようにSYS PCBのR607を調整する。

注）図5-5の様に、ショートピンA, Bを差した状態がB-HEADの電流値測定の状態です。
ショートピンA, Bの差す位置を逆にした状態が、A-HEADの電流値測定の状態です。尚、オシロスコープの参考波形として、写真-4を参照してください。

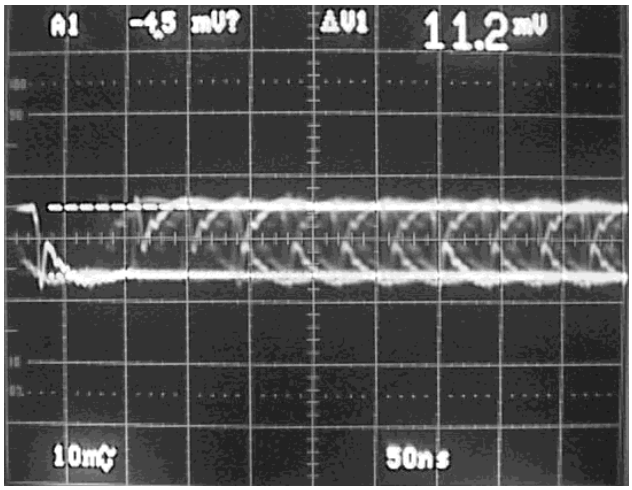


Photo-4

2. ME tape
Load ME blank tape MTT-88202 and check the current values at A-HEAD and B-HEAD in the same way as a MP tape. The current values should be 12.4 ± 0.6 mAp-p.

5-9-2. Checks in Confidence mode

1. Set the Confidence mode on, and connect the REC CURRENT KIT (P/N:V00024700A) between P9 on the MOTHER PCB and P101 on the RF REC PCB.
2. Perform the same check and adjustment as discussed in 5-9-1. Use R608 (A-HEAD) and R609 (B-HEAD) on SYS PCB for adjustment.

2. MEテープ
ME生テープ MTT-88202を装着し、MPテープと同様にA-HEAD, B-HEADの電流値を確認する。
電流値は 12.4±0.6 mAp-p であること。

5-9-2. コンフィデンスモードでの確認

1. コンフィデンスモードに切換え、REC CURRENT KIT（品番V00024700A）をMOTHER PCBのP9とRF PLAY PCBの P101間に接続する。
2. 5-9-1項と同様に確認、調整する。
調整は、SYS PCBのR608（A-HEAD）、R609（B-HEAD）で行う。

5-10. Recording/playback RF level check

5-10-1. Checks in Normal mode

1. After adjusting the recording current following section 5-9, rewind the tape section where format recording was executed in HR mode, and overwrite a signal on that section.
2. Rewind the tape section recorded in 1 above and play it.
3. In the same was as section 5-7, ensure that the RF level is 1200 mV minimum and that the waveform ratio is 80% minimum (with both ME and MP tapes).

5-10-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-10-1.

5-11. Recording/playback error rate check

5-11-1. Checks in Normal mode

Play back the recording you made as per instructions in paragraph 5-10, and check for less than 200 x 10^{-4} of error rate (with both ME and MP tapes).

5-11-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-11-1.

5-10. 記録再生RFレベル確認

5-10-1. ノーマルモードでの確認

1. 5-9項で記録電流調整後、HRモードで FORMAT記録した部分を巻き戻し、その部分にオーバーライト記録する。
2. 1項で記録した部分を巻き戻し、その部分を再生する。
3. 5-7項と同様に、RFレベルが 最小部で 1200mV以上、波形比 80%以上であることを確認する。
（ME, MPテープ共）

5-10-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-10-1項と同様の確認を行う。

5-11. 記録再生エラーレート確認

5-11-1. ノーマルモードでの確認

5-10項で記録した部分を再生する。
このときのエラーレートは、200×10^{-4}以下であること。
（ME, MPテープ共）

5-11-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-11-1項と同様の確認を行う。

PARTS LIST SECTION

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with ∗ require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in the manual.
- ⚠Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J]: JAPAN [US/C]: U.S.A./CANADA [E]: EUROPE [K]: KOREA
  [UK]: U.K. [A]: AUSTRALIA

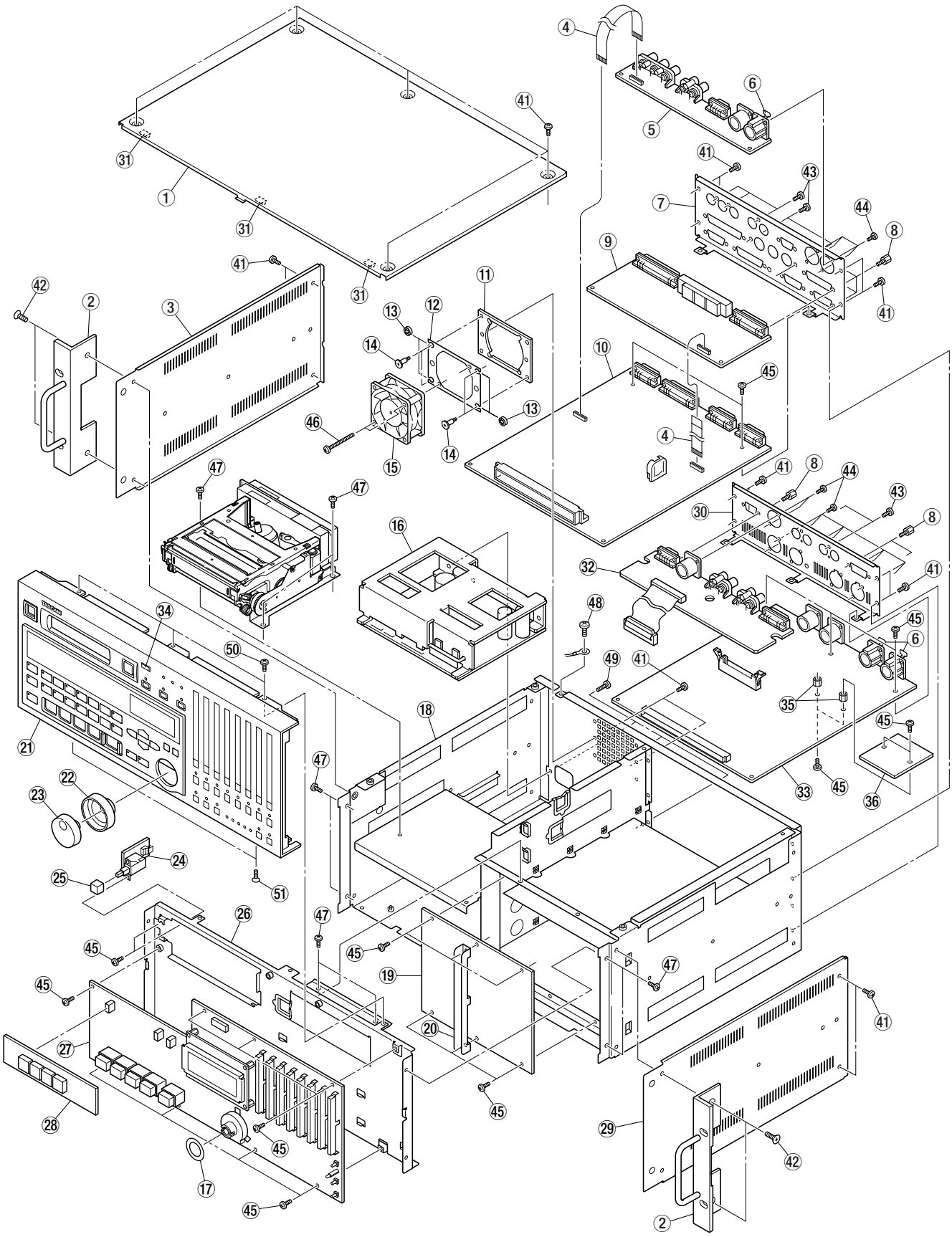
注 意

- プリント基板は部品面が示されています。
- ∗印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品及び品番のない部品は供給しません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠は安全重要部品です。
  交換する時は必ずティアック指定の部品を使用してください。
- 仕向先
  [J]: JAPAN [US/C]: U.S.A./CANADA [E]: EUROPE [K]: KOREA
  [UK]: U.K. [A]: AUSTRALIA

6. EXPLODED VIEWS AND PARTS LIST

分解図とパーツリスト

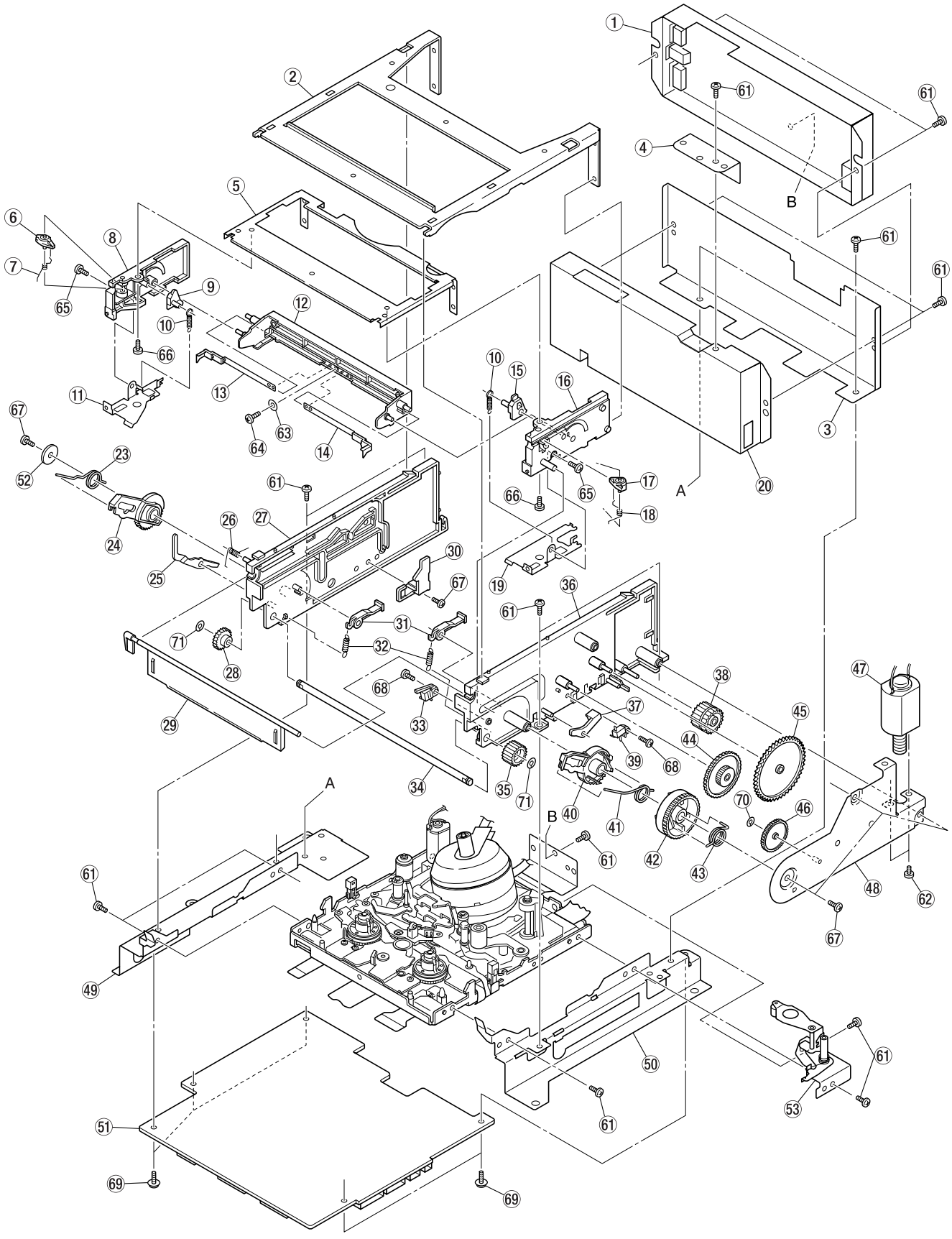
EXPLODED VIEW-1



EXPLODED VIEW-1

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	*M01074900A	COVER,TOP	
1- 2	*M01319500A	ANGLE ASSY	
1- 3	*M01075000A	COVER,SIDE L	
1- 4	*E00556300A	FLAT CABLE,DSUB16	
1- 5	*E95105500A	PCB ASSY,BNC	
1- 6	5334075900	CLAMP,CANNON CONNECTOR SOCKET	
1- 7	*M01075400A	REAR PANEL,SYS	
1- 8	5801536400	SCREW,DSUB LOCK M2.6X0.45	
1- 9	*E95105600A	PCB ASSY,DSUB	
1-10	*E95106300C	PCB ASSY,SYS	
1-11	*M01075700A	BRACKET,FAN A	
1-12	*M01075900A	BRACKET,FAN B	
1-13	*M00039100A	DAMPER	
1-14	*M00039000A	PIN,STEP	
1-15	*E0051380	DC FAN MOT,FBA06A12L	
1-16	*E00345500C	SW RGLTD PS [J,US/C]	
	*E00345540C	SW RGLTD PS [E,K,UK,A]	
1-17	*M01247100A	SPACER,SHUTTLE	
1-18	*M01075300B	CHASSIS ASSY	
1-19	*E95106410A	PCB ASSY,MOTHER	
1-20	*M00617200A	BRACKET	
1-21	*M01319000A	FRONT PANEL ASSY	
1-22	M01074700A	KNOB,SHUTTLE N64	
1-23	M01074600A	KNOB,JOG N64	
1-24	*E95103200B	PCB ASSY,SW	
1-25	M00001500A	BUTTON,C	
1-26	*M01075100B	CHASSIS,FRONT	
1-27	*E95103010B	PCB ASSY,KEY	
1-28	*E95103100B	PCB ASSY,COUNTER	
1-29	*M01075001A	COVER,SIDE R	
1-30	*M01319600A	REAR PANEL,DS-D98	
1-31	5801599400	GASKET	
1-32	*E95129500A	PCB ASSY,IF DSD	
1-33	*E95129400A	PCB ASSY,DSD	
1-34	*M01319200A	LENS ASSY	
1-35	*M01341500A	COLLAR,PCB	
1-36	*E95131600B	PCB ASSY,DSD SUB	
1-41	5780023006	SCREW,BIND M3X6 (BLK NI)	
1-42	5780224008	SCREW,FLAT M4X8 (BLK NI)	
1-43	5783543008	SCREW,BIND P-TITE M3X8 (BLK NI)	
1-44	*5780112605	SCREW,PAN M2.6X5 (NI)	
1-45	5780003006	SCREW,BIND M3X6	
1-46	5780003030	SCREW,BIND M3X30	
1-47	5780103006	SCREW,PAN M3X6	
1-48	5780004008	SCREW,BIND M4X8	
1-49	5780023010	SCREW,BIND M3X10 (BLK NI)	
1-50	*B00049700A	SCREW,BPAR3*6FZC	
1-51	5780203006	SCREW,FLAT M3X6	

EXPLODED VIEW-2

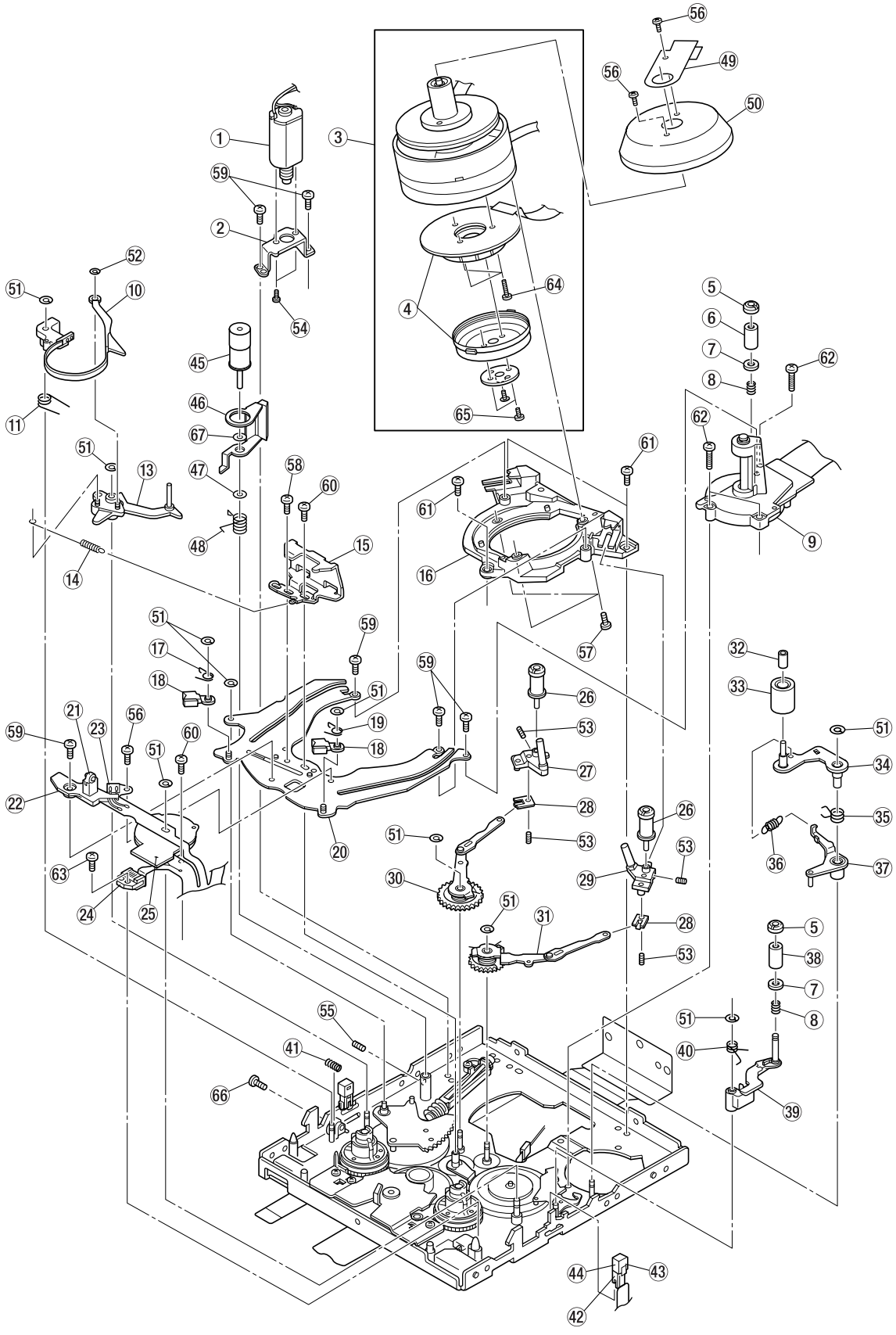


EXPLODED VIEW-2

REF.NO.	PARTS NO.	DESCRIPTION
2- 1	*E95106000B	PCB ASSY,RF PLAY
2- 2	5801527902	BRACKET,CAM PLATE
2- 3	*M01101300A	BRACKET,RF
2- 4	*M01101600A	SHIELD PLATE,FPC
2- 5	M00434400A	HOLDER,MAIN
2- 6	5801525500	LEVER L,CASSETTE PRESS
2- 7	5801525600	SPRING,COIL LLCP
2- 8	5801525300	BASE L,SLIDE
2- 9	5801525700	LEVER L,BRAKE
2-10	5801525800	SPRING T,BRAKE
2-11	5801525400	SUB HOLDER L
2-12	5801524601	OPENER,LID
2-13	5801524700	LEVER L ASSY,LOCK
2-14	5801525000	LEVER R ASSY,LOCK
2-15	5801526300	LEVER R,BRAKE
2-16	5801525900	BASE R,SLIDE
2-17	5801526100	LEVER R,CASSETTE PRESS
2-18	5801526200	SPRING,COIL LRCP
2-19	5801526000	SUB HOLDER R
2-20	*E95106100B	PCB ASSY,RF REC
2-21	Vacant	
2-22	Vacant	
2-23	5801526800	SPRING,COIL CPL
2-24	5801526700	GEAR L,TRANSFER
2-25	5801528000	LEVER,FRONT LID
2-26	5801529200	SPRING,COIL LID
2-27	*5801526503	PLATE L,CAM
2-28	5801528700	GEAR L,SYNCRONIZE
2-29	M00365790B	DOOR,LID FRONT 78
2-30	5801526601	CAM,LID OPENER
2-31	5801528900	LEVER,LOCK
2-32	5801529000	SPRING T,LOCK LEVER
2-33	5300060200	SW,PUSH SPPB21
2-34	5801528600	SHAFT,SYNCRONIZE
2-35	5801528800	GEAR R,SYNCRONIZE
2-36	5801526902	PLATE R,CAM
2-37	5801527000	LEVER,SWITCH
2-38	5801528200	GEAR A,REDUCTION
2-39	5300060100	SW,PUSH SPPB12
2-40	5801527100	GEAR R,TRANSFER
2-41	5801527200	SPRING,COIL CPR
2-42	5801527300	GEAR,RELEASE
2-43	5801527400	SPRING,COIL GR
2-44	5801528400	GEAR C,REDUCTION
2-45	5801528300	GEAR B,REDUCTION
2-46	5801528500	GEAR D,REDUCTION
2-47	5600165100	MOTOR SUB ASSY,CASSETTE
2-48	5801527601	BRACKET ASSY,C MOTOR
2-49	*M00434100A	BRACKET,L
2-50	*M00434200A	BRACKET,R

REF.NO.	PARTS NO.	DESCRIPTION
2-51	*E95106200B	PCB ASSY,SERVO
2-52	5801528100	PLATE,TRANSFER GEAR
2-53	M00435600A	CLEANER ASSY,HEAD
2-61	5780012004	SCREW,BIND M2X4 (NI)
2-62	5782522028	SCREW,PAN 1# M2X2.8 (NI)
2-63	5785022200	WASHER,2X6X0.4T
2-64	5782551640	SCREW,PAN BT 3# M1.6X4 (NI)
2-65	5782521630	SCREW,PAN 3# M1.6X3 (NI)
2-66	5782521625	SCREW,PAN 3# M1.6X2.5 (NI)
2-67	5782552040	SCREW,PAN BT 3# M2X4 (NI)
2-68	5782552080	SCREW,PAN BT 3# M2X8 (NI)
2-69	B0005020	SCREW,PPAB 2X5FNI
2-70	5785341200	WASHER,POLYS. 1.7X4X0.25T
2-71	5785343000	WASHER,POLYS. 3.2X5.5X0.25T

EXPLODED VIEW-3

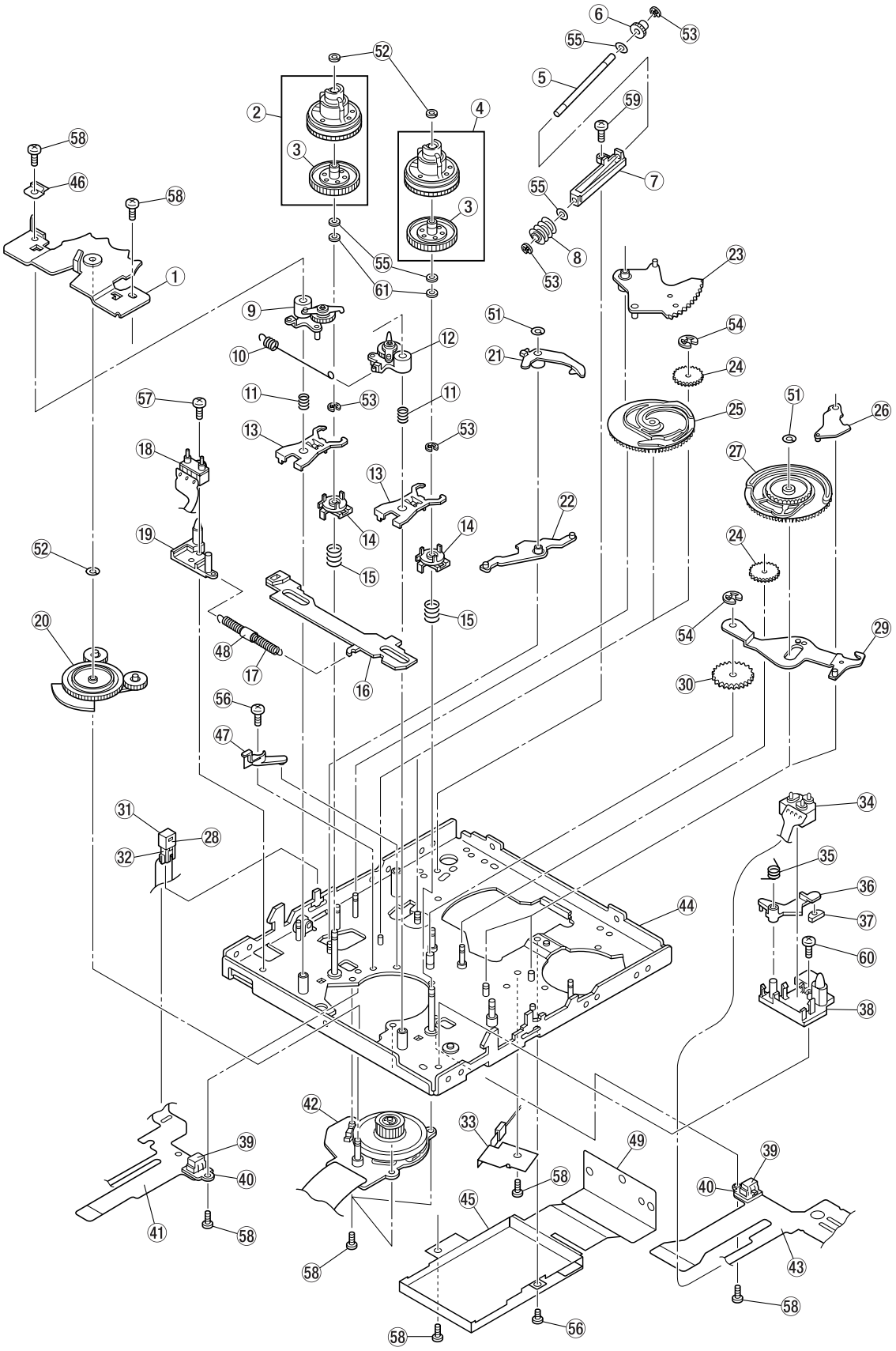


EXPLODED VIEW-3

REF.NO.	PARTS NO.	DESCRIPTION
3- 1	*M00438800A	LD MOTOR ASSY,DTRS
3- 2	M00434000A	HOLDER,LD MOTOR
3- 3	M01101110A	DRUM ASSY,98HR-10
3- 4	1473407500	MOTOR ASSY,DRAM
3- 5	1676742500	FLANGE,NUT
3- 6	1676744900	GUIDE,CAPSTAN
3- 7	1676742300	FRANGE,GUIDE
3- 8	1638547600	SPRING C
3- 9	1473407700	MOTOR,CAPSTAN
3-10	M00822300A	BRAKE ASSY,BAND
3-11	1638913401	SPRING,COIL 01
3-12	Vacant	
3-13	1796821300	LEVER ASSY,BACK TENSION
3-14	1638209100	SPRING T
3-15	1680464800	PLATE,PROTECTOR
3-16	1615405600	BASE ASSY,DRAM
3-17	1638913800	SPRING,COIL
3-18	1796826300	LEVER ASSY,SOFT BRAKE
3-19	M00256300A	TORSION SPRING,20G
3-20	1615405700	PLATE ASSY,GUIDE RAIL
3-21	13419521	PHOTO ELEMENT,GL450
3-22	1678872150	BRACKET,LED (BRACK)
3-23	13299679	SENSOR,DEW HDP-07-C2
3-24	14771017	SOLENOID,LUTCH 6V 240 OHM
3-25	1796822901	MODE SW ASSY (01)
3-26	1796826900	ROLLER ASSY,M GUIDE
3-27	1796822700	SLIDE MGS ASSY
3-28	1680461900	BRACKET MG
3-29	1796822800	SLIDE MGT ASSY
3-30	1796821100	LEVER ASSY,L THREAD
3-31	1796821200	LEVER ASSY,R THREAD
3-32	1678871800	SLEEVE,PINCH ROLLER
3-33	1796821900	ROLLER ASSY,PINCH
3-34	1796821700	LEVER ASSY,PINCH
3-35	1638913500	SPRING,COIL
3-36	1638209200	SPRING T
3-37	1796821800	LINK ASSY,PINCH
3-38	1676742400	GUIDE,FINAL
3-39	1796822200	LEVER ASSY,GUIDE
3-40	1638913600	SPRING,COIL
3-41	1638547500	SPRING,C
3-42	1678872700	HOLDER,TE SENSOR
3-43	13419660	PHOTO ELEMENT,RPM-20PB-T
3-44	1680472902	PLATE,SLIT 02
3-45	1796822600	ROLLER ASSY,IMPEADANCE
3-46	M00123400A	CLEANER ASSY,TAPE
3-47	M0090610	WASHER,1.63X3X0.13
3-48	M00122100A	TORSION SPRING,ARM T
3-49	M00433900A	SHIELD PLATE,FPC
3-50	M00433800A	SHIELD PLATE,S

REF.NO.	PARTS NO.	DESCRIPTION
3-51	16499908	WASHER,SLIT 1.57X4X0.3
3-52	16499907	WASHER,SLIT 1.2X3X0.3
3-53	B0001450	SPBOLT,NO.0 PAN1.2X2.5FNB
3-54	16502019	SCREW,PAN NO.0 3# 2X2
3-55	B0001540	SPBOLT,NO.0 TP3P1.4X2FNB
3-56	16499864	SCREW,PAN NO.0 M1.6X2
3-57	16499873	SCREW,PAN NO.0 M1.6X5.5
3-58	16499772	SCREW,PAN NO.0 3# 2X2
3-59	16499773	SCREW,PAN NO.0 3# 2X2.5
3-60	16499909	SCREW,PAN NO.0 3# 2X3.5
3-61	16499776	SCREW PAN NO.0 3# 2X5
3-62	16499910	SCREW PAN NO.0 3# 2X8
3-63	16502031	SCREW,TAP TITE ETP 1.4X3.5
3-64	16502044	SCREW,PAN NO.0 1.6X6.5
3-65	*16499870	SCREW PAN NO.0 M1.6X4
3-66	B0000430	SCREW,PAN NO.0 3 2X4.5
3-67	M0090660	WASHER,3.85X6X0.2

EXPLODED VIEW-4



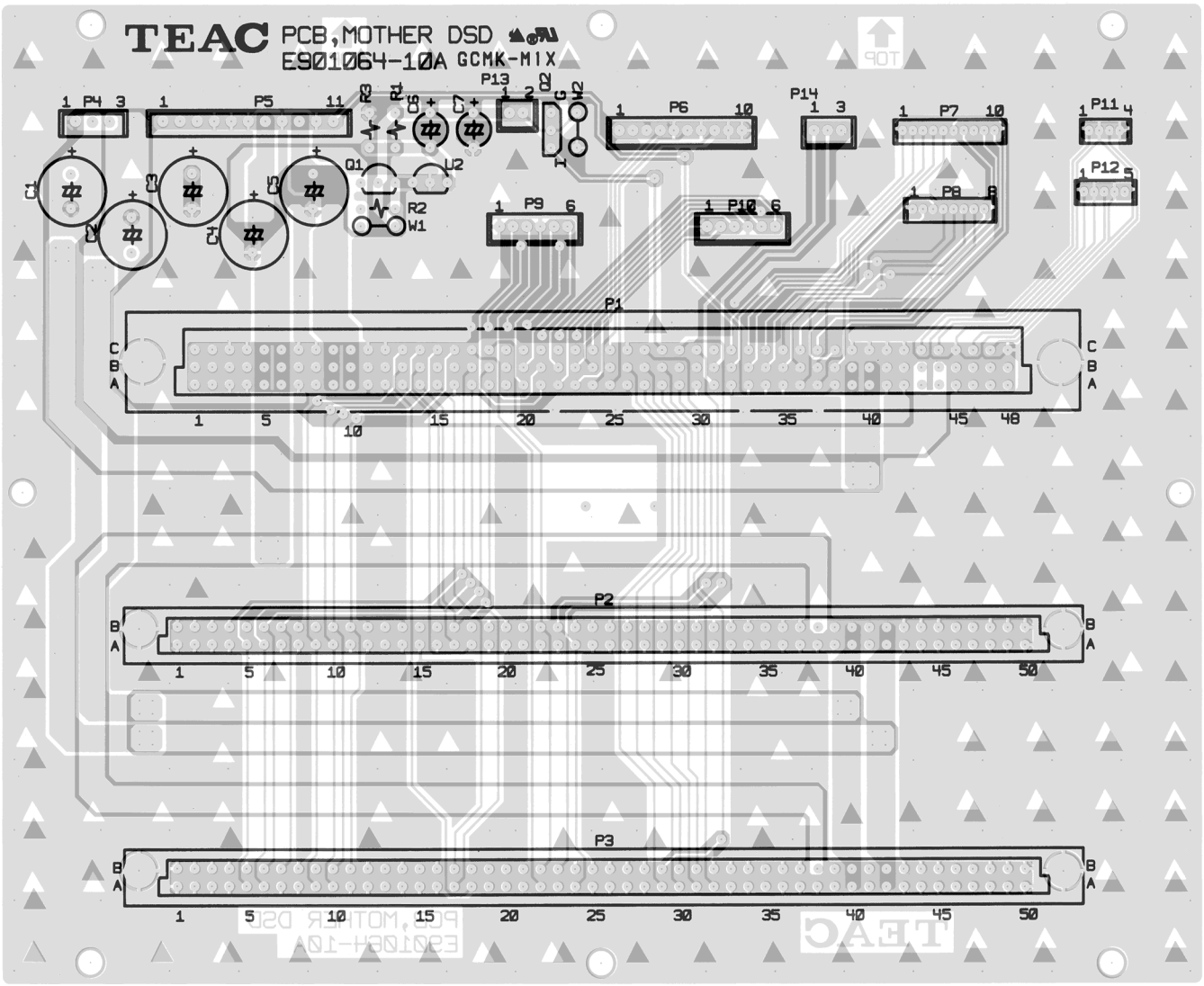
EXPLODED VIEW-4

REF.NO.	PARTS NO.	DESCRIPTION
4- 1	1680462100	BRACKET,T OPENER
4- 2	M00607100A	REEL TABLE ASSY,S
4- 3	1796826600	DISC ASSY,REFRECTOR
4- 4	M00607200B	REEL TABLE ASSY,T
4- 5	1676741400	SHAFT,LOADING GEAR
4- 6	1678870600	WORM WHEEL,LOADING
4- 7	1680460800	BRACKET,GEAR
4- 8	1678870700	WORM,LOADING
4- 9	M00877600A	BRAKE ASSY,S
4-10	1638209000	SPRING T
4-11	1638547400	SPRING C
4-12	M00877700A	BRAKE ASSY,T
4-13	1680460600	LEVER,CLUTCH
4-14	1796820200	CLUTCH ASSY
4-15	1638547300	SPRING C
4-16	1678870001	SLIDE,REEL OPERATING CAM
4-17	1638208900	SPRING T
4-18	13222478	SW,PUSH SPPW62 SPPW62
4-19	1678872500	HOLDER,SWL
4-20	1796826100	GEAR ASSY,CENTER
4-21	1678871700	LEVER,REEL LOCK
4-22	1796820701	LEVER ASSY,SLIDE (-01)
4-23	1796821003	GEAR ASSY,SECTOR (-03)
4-24	1678871000	GEAR B,COUPLING
4-25	1678870800	CAM L,LOGIC
4-26	1796822000	CAM FOLLOWER ASSY,PINCH
4-27	1678871100	CAM R,LOGIC
4-28	1680472902	PLATE,SLIT 02
4-29	1796822300	LEVER ASSY,GUIDE CARRY
4-30	1678870900	GEAR A,COUPLING
4-31	13419660	PHOTO ELEMENT,RPM-20PB-T
4-32	1678872700	HOLDER,TE SENSOR
4-33	M00914300A	BRUSH ASSY
4-34	13222479	SW,PUSH SW-101-2P
4-35	1638913100	SPRING,COIL
4-36	1678870402	LEVER,SLID KEEP (02)
4-37	14771018	SOLENOID,LUTCH
4-38	1678872601	HOLDER,SWR (01)
4-39	13419663	PHOTO ELEMENT,NJL5165KA
4-40	1678872400	HOLDER,REEL SENSOR
4-41	1336133600	PCB,SENSOR L
4-42	1473407800	MOTER,REEL
4-43	1336133700	PCB,SENSOR R
4-44	1796823001	MECHA CHASSIS ASSY (01)
4-45	*M01101700A	COVER,BRUSH
4-46	1630187000	STOPPER TB
4-47	1678889500	SUPPORT,TR BAND
4-48	13090294	TUBE,F 2 PHI
4-49	*M01101600A	SHIELD PLATE,FPC

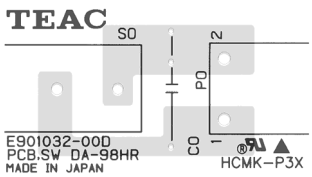
REF.NO.	PARTS NO.	DESCRIPTION
4-51	16499908	WASHER,SLIT 1.57X4X0.3
4-52	16499907	WASHER,SLIT 1.2X3X0.3
4-53	16351100	E-RING,1.2J
4-54	16351150	E-RING,2.5J
4-55	16496335	WASHER,1.7X3.2X0.25
4-56	16499864	SCREW,PAN NO.0 M1.6X2
4-57	16499873	SCREW,PAN NO.0 M1.6X5.5
4-58	16499773	SCREW,PAN NO.0 3# 2X2.5
4-59	16499909	SCREW,PAN NO.0 3# 2X3.5
4-60	16499776	SCREW PAN NO.0 3# 2X5
4-61	16496604	WASHER,1.7X3.2X0.13

7. PC BOARDS AND PARTS LIST
基板図とパーツリスト

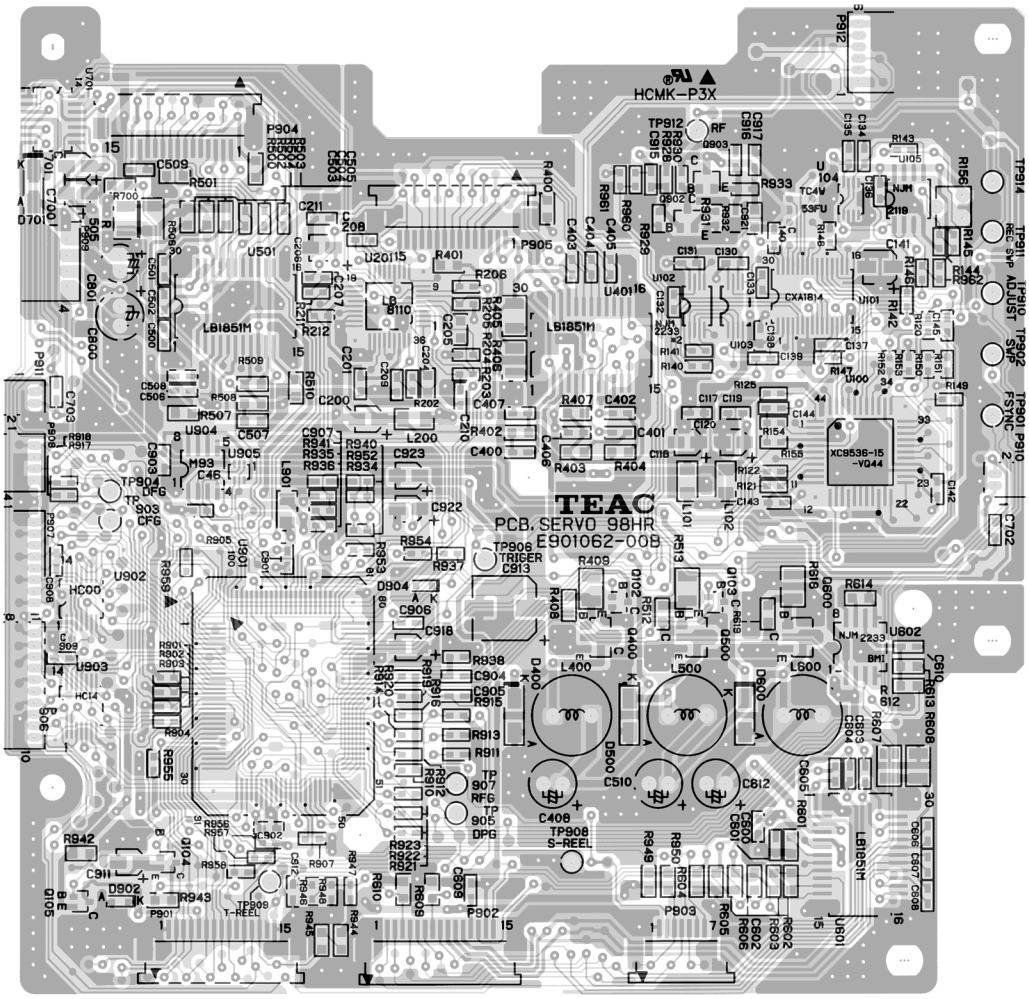
MOTHER PCB



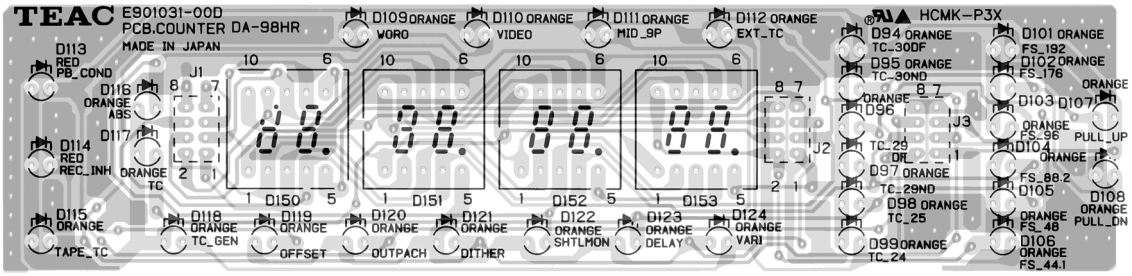
SW PCB



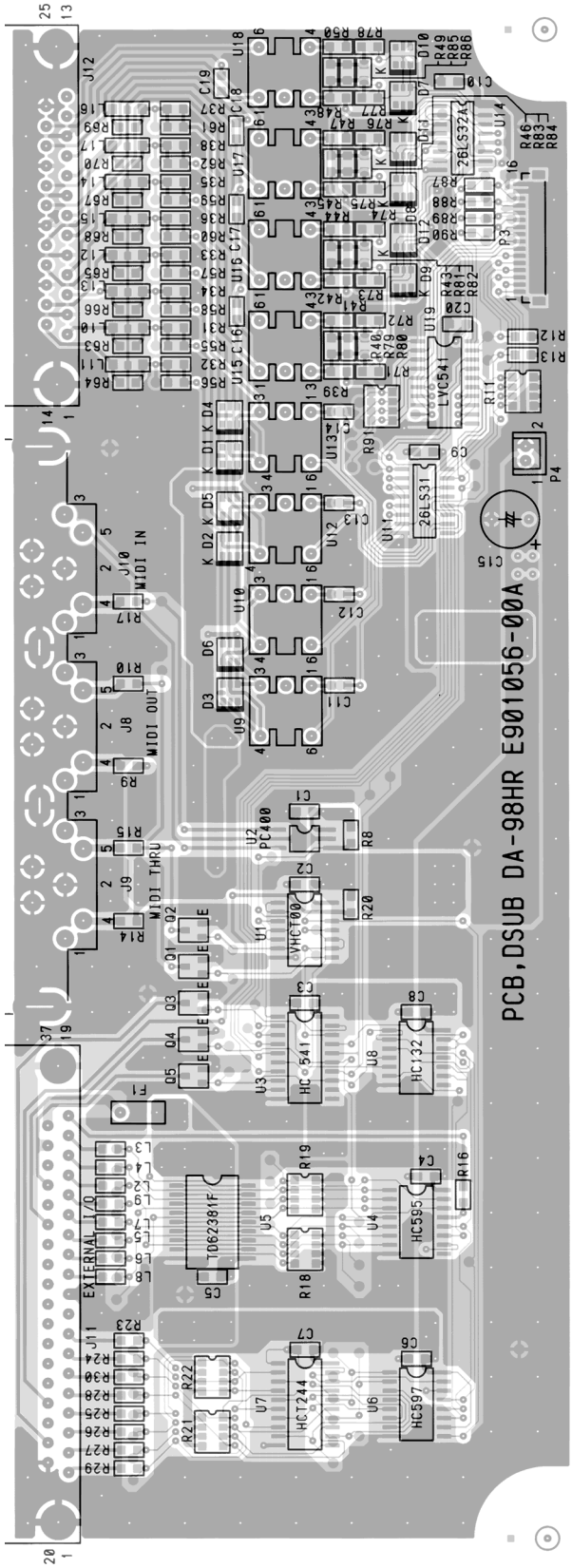
SERVO PCB



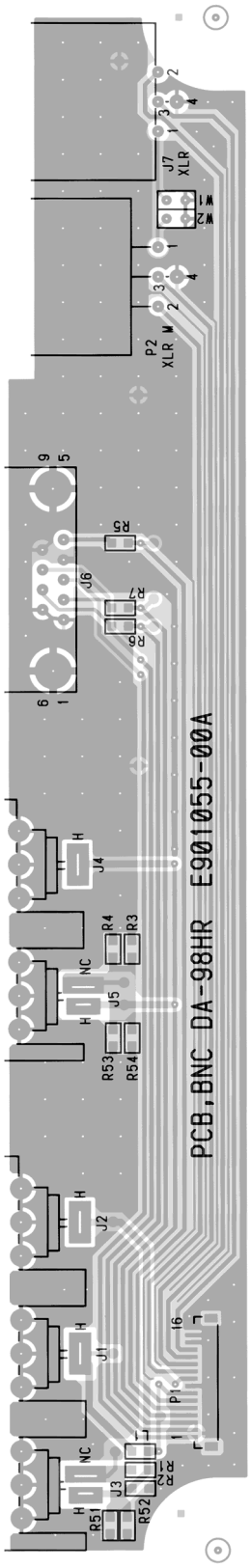
COUNTER PCB



DSUB PCB

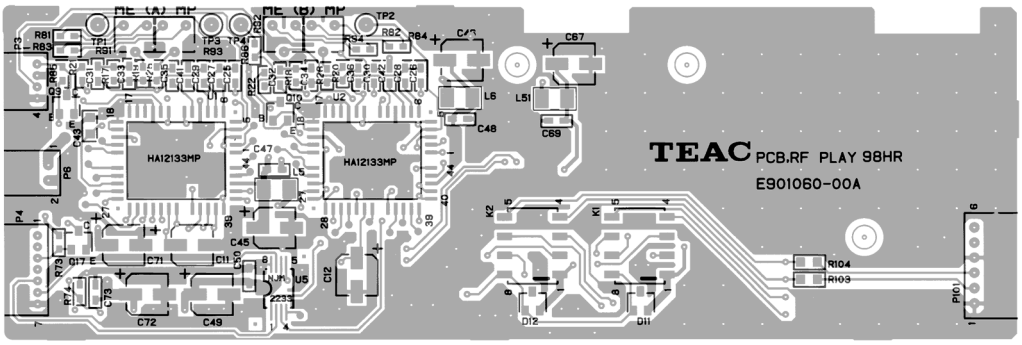


BNC PCB



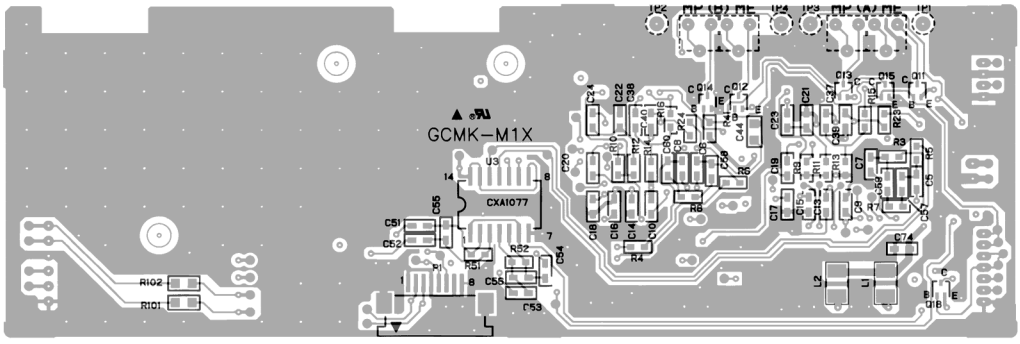
RF PLAY PCB

SIDE A



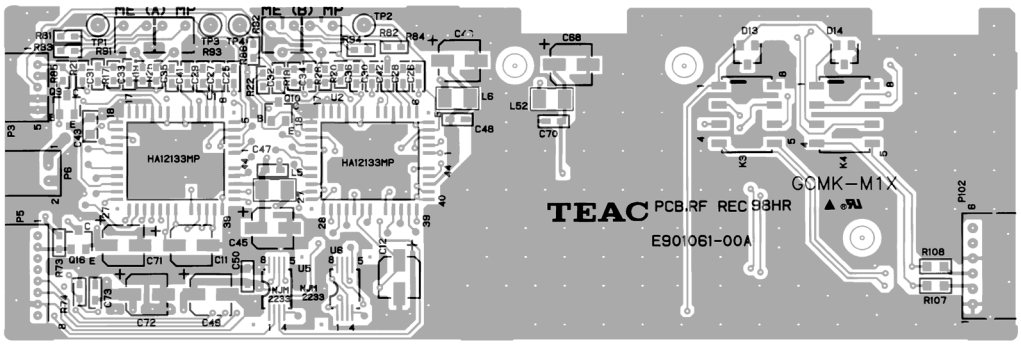
RF PLAY PCB

SIDE B



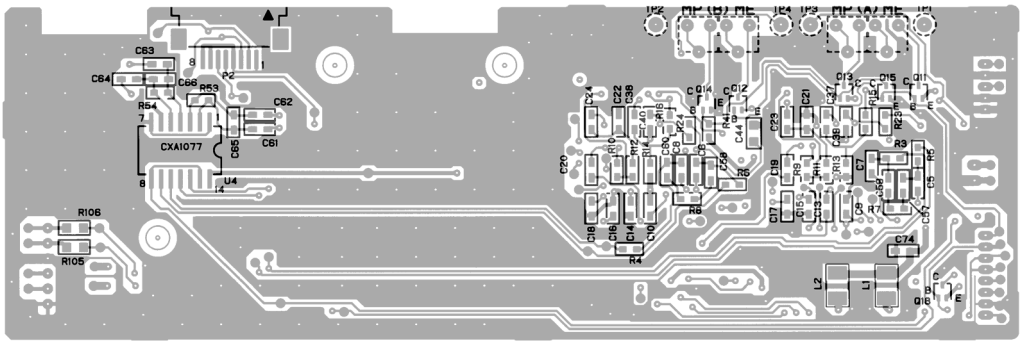
RF REC PCB

SIDE A



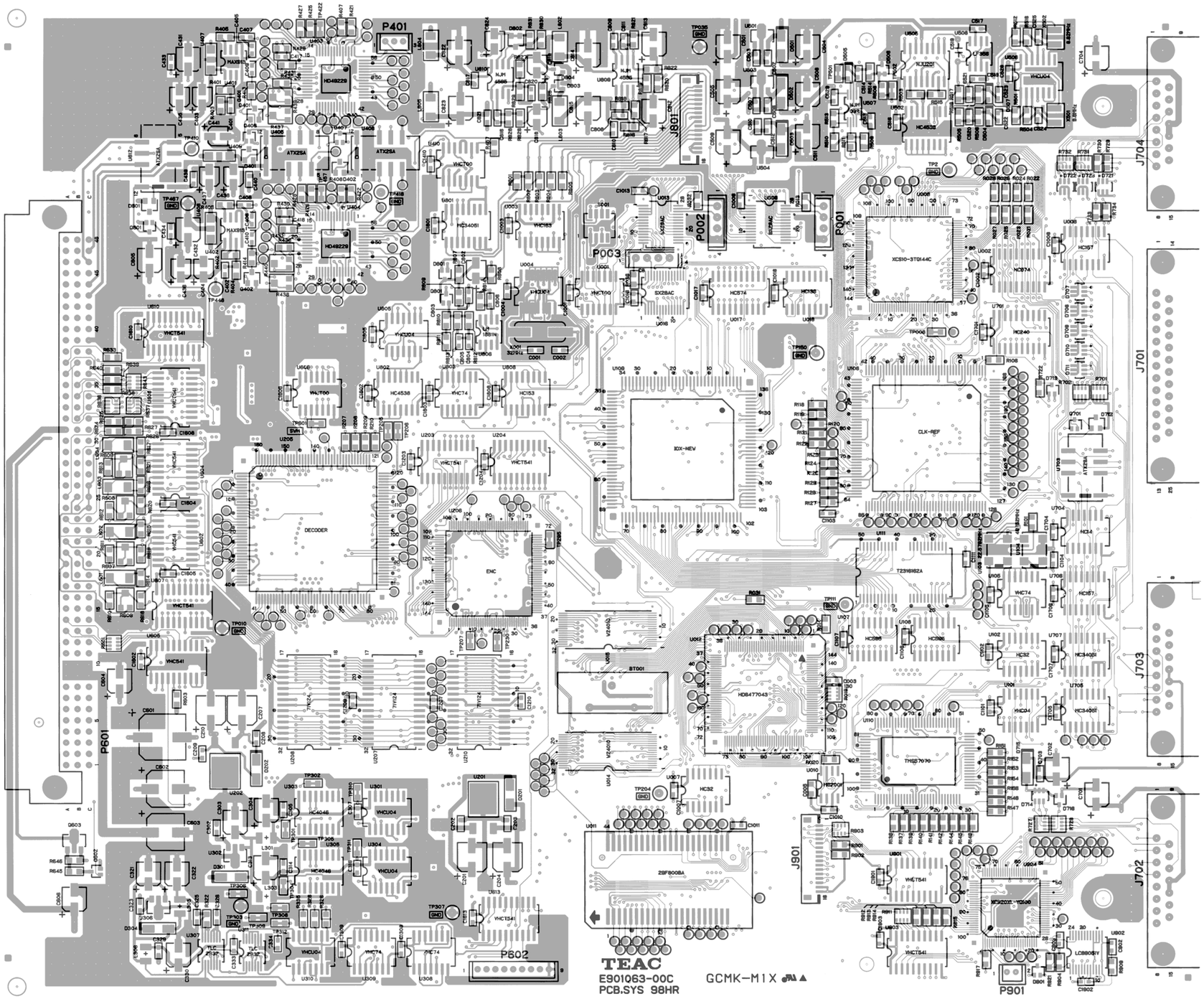
RF REC PCB

SIDE B



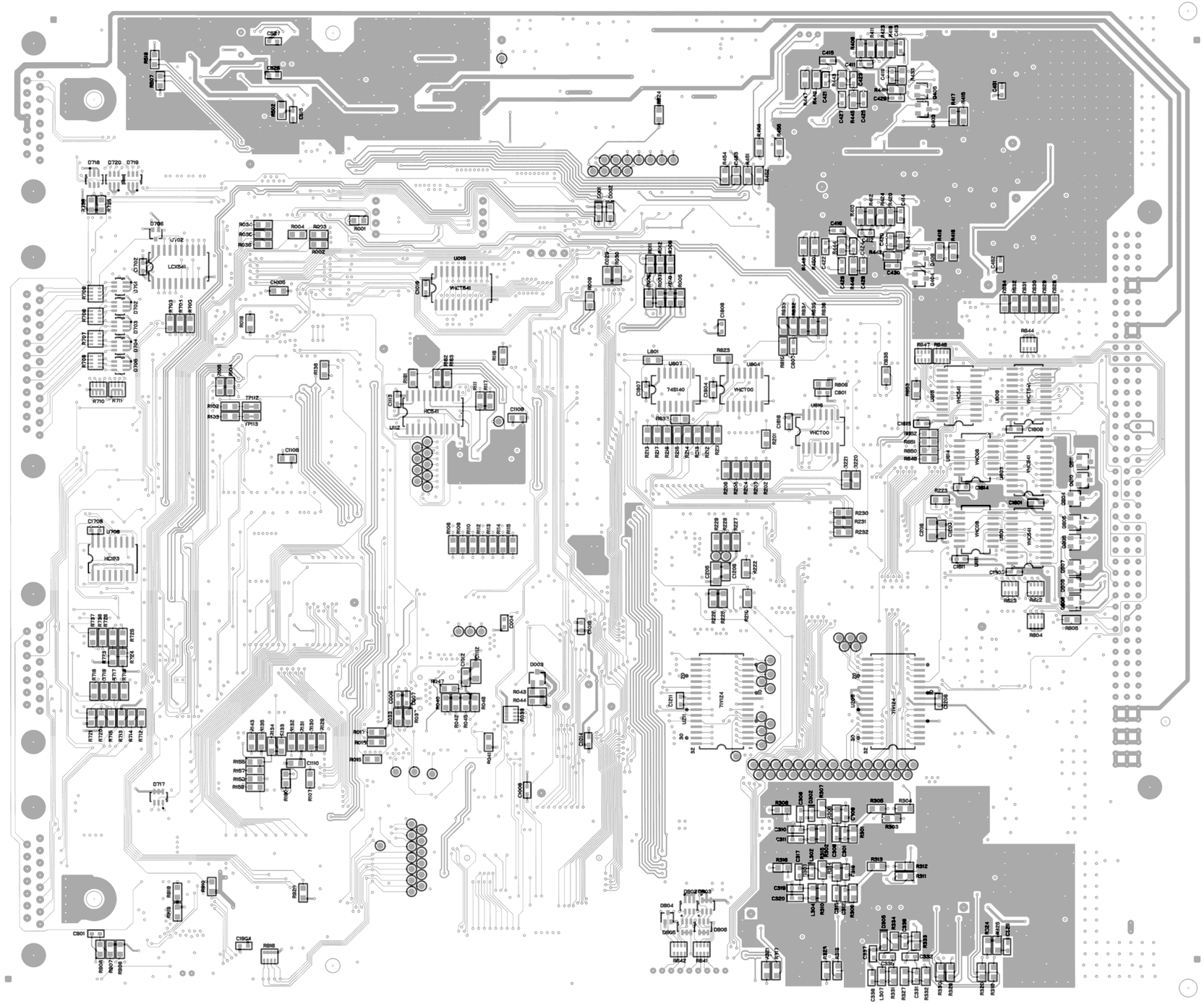
SYS PCB

SIDE A

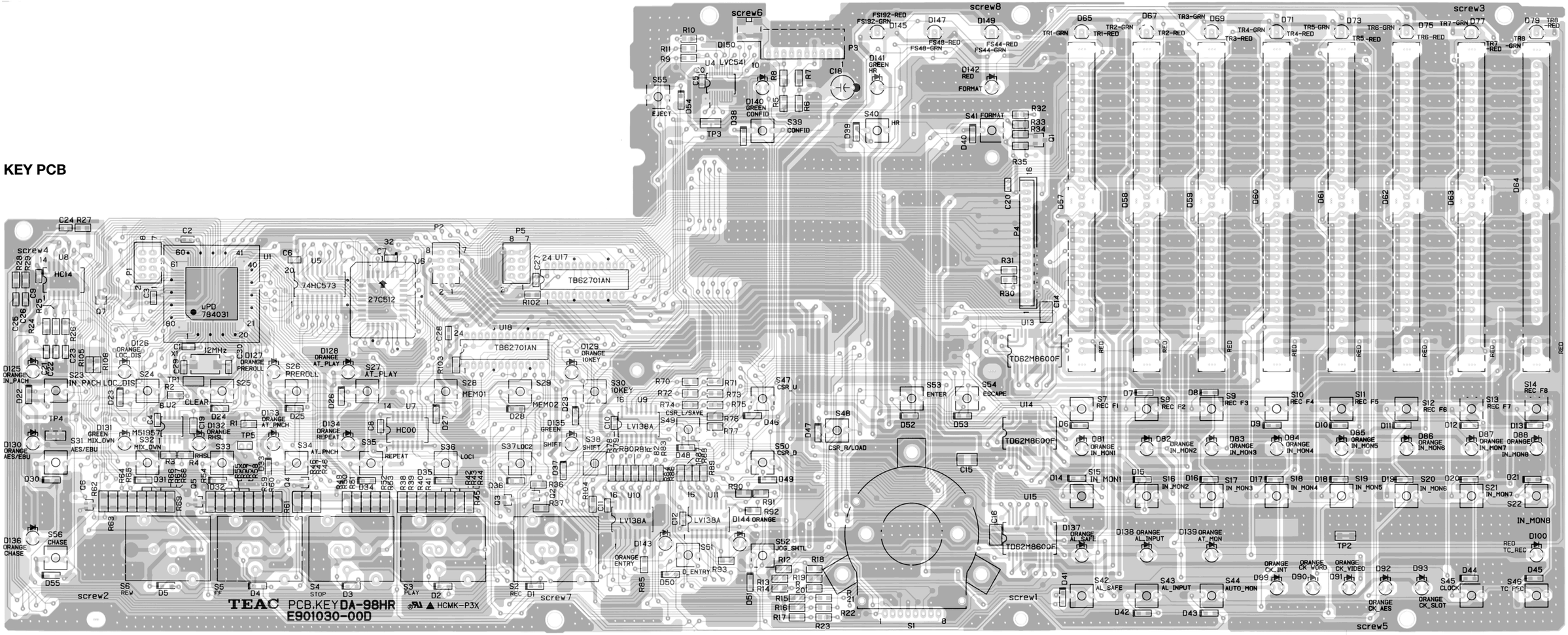


SYS PCB

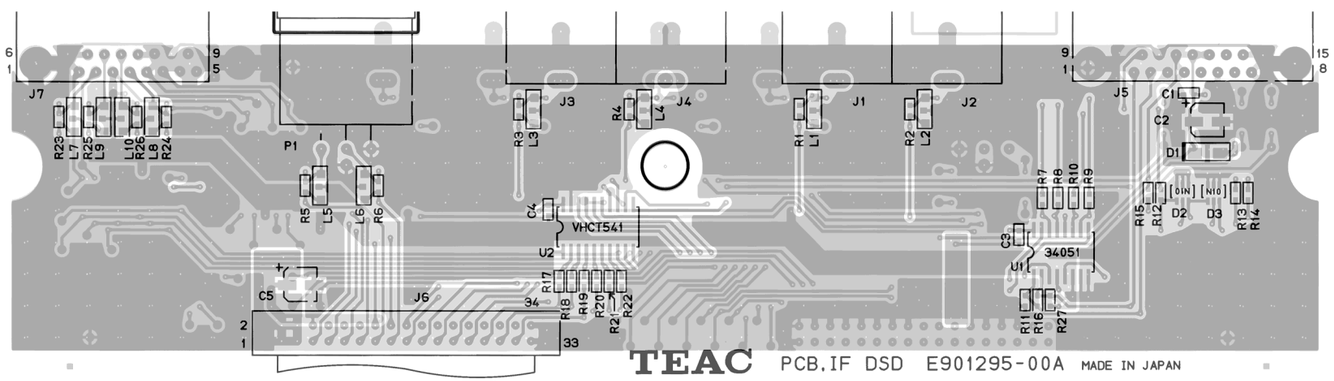
SIDE B



KEY PCB

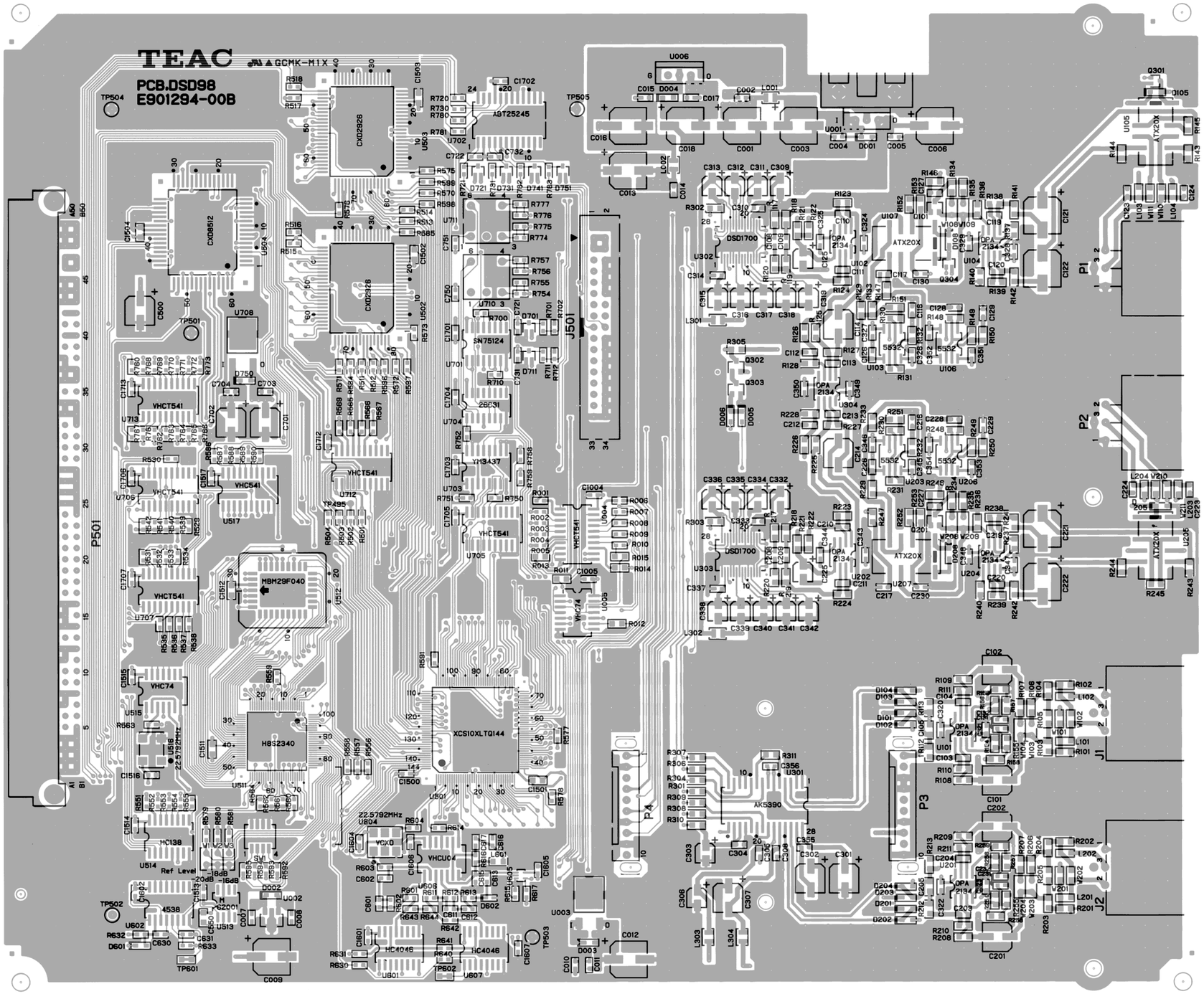


IF DSD PCB



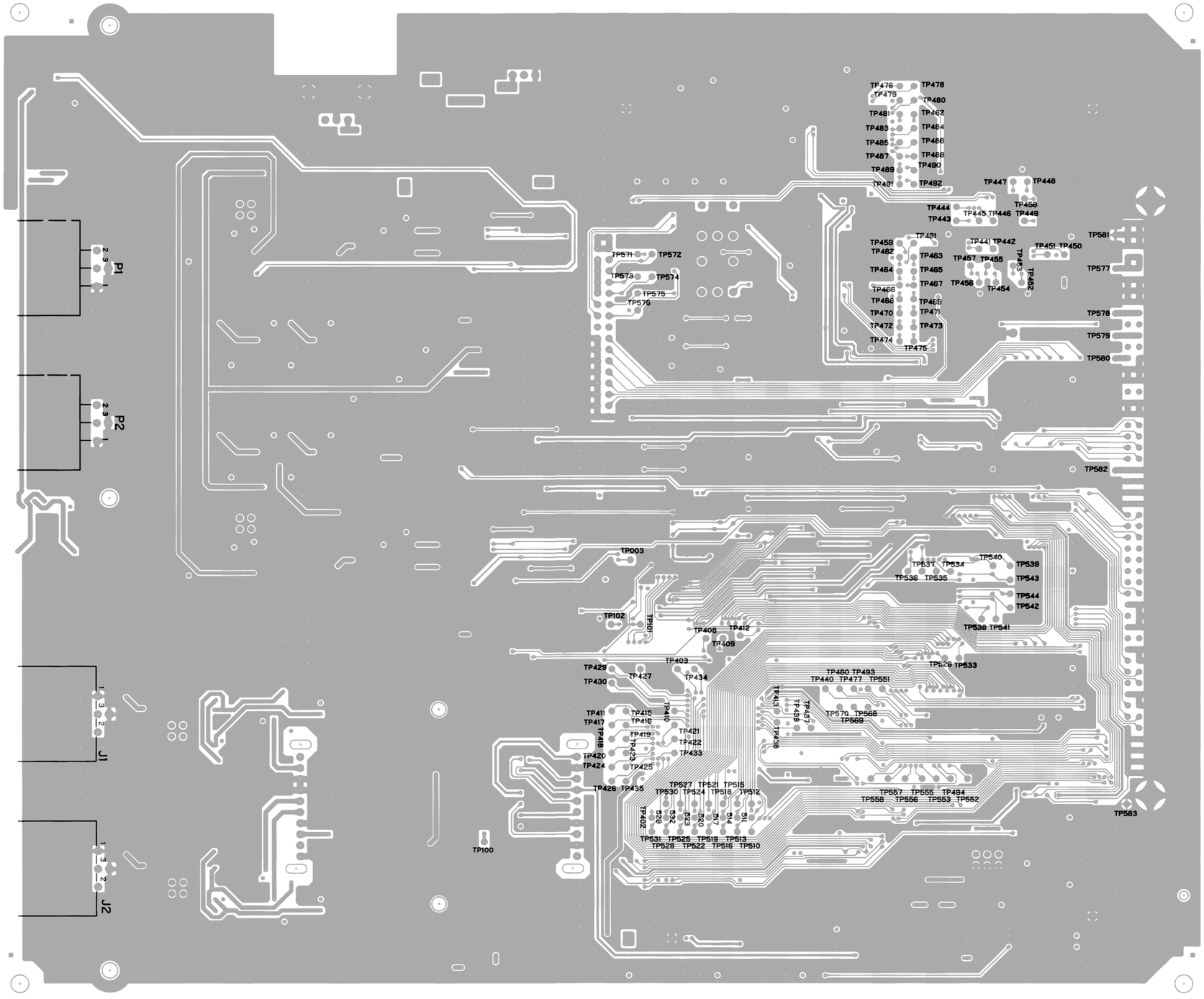
DSD PCB

SIDE A



DSD PCB

SIDE B



MOTHER PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106410A	PCB ASSY,MOTHER DS-D98
P1	E0033030	CONNECTOR,PCN10MA-144S
P2,P3	5334079500	CONNECTOR,SKT 100P
P4	5336303300	PLUG,CONN. B3B-EH(WHT)
P5	5336304100	PLUG,CONN. B11B-EH(WHT
P6	5336250000	PLUG,CONN. B10B-PH-K-S W
P7	13124432	CONNECTOR,ZH B 10B-ZR
P8	13124430	CONNECTOR,ZH B 8B-ZR
P9	5336251600	PLUG,CONN. B06B-PH-K-R R
P10	5336249600	PLUG,CONN. B06B-PH-K-S W
P11	13124426	CONNECTOR,ZH B 4B-ZR
P12	13124427	CONNECTOR,ZH B 5B-ZR
P13	5336249200	PLUG,CONN. B02B-PH-K-S W
P14	5336249300	PLUG,CONN. B03B-PH-K-S W
Q1	S0031562	TR,2SB1592
U2	5220446100	IC,M5237L

SW PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95103200B	PCB ASSY,SW
S0	E0038520	SW,PUSH SDDLB14000
C0	E0022570	SPK KILLER,0.0047UF250V
P0	E0042990	CONNECTOR,S2P3-VH

COUNTER PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95103100B	PCB ASSY,COUNTER
D94-99	5225018500	LED,SLR-34DU3F
D94A-99A	M00608701A	SPACER,LH-5 L=2
D101-112	5225018500	LED,SLR-34DU3F
D101A-108A	M00608701A	SPACER,LH-5 L=2
D109A-112A	M00608701A	SPACER,LH-5 L=2
D113-114	5225013500	LED,SLR-34VR3F (R)
D115-124	5225018500	LED,SLR-34DU3F
D113A-124A	M00608701A	SPACER,LH-5 L=2
D150-153	5225028400	LED INDICATOR,B-302DF
J1-3	5336372000	CONNECTOR,SKT 8P BTK 8S-2S

SERVO PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106200B	PCB ASSY,SERVO
D400-600	5224019200	DIODE,EC10QS04TE12L
D701	S0034934	DIODE,RB051L-40 TE25
D902,904	S0022094	DIODE,1SS355
L101,102	E0022854	COIL,COILCHIP 100UF
L200	E0022854	COIL,COILCHIP 100UF
L400,500	14728449	COIL,390UH 10%
L600	14728444	COIL,150UH 10%
L901	E0022854	COIL,COILCHIP 100UF
P901	13153693	CONNECTOR,52271-1590
P902	13153479	CONNECTOR,15P
P903	5336379500	CONNECTOR,7P 52271-0790
P904,905	13153693	CONNECTOR,52271-1590
P906	13124443	CONNECTOR,ZH S10B-ZR
P907	13124025	CONNECTOR,ZN S 8B-ZR
P908	13124021	CONNECTOR,ZN S 4B-ZR
P909	5336287400	PLUG,CONN. S4B-PH-K-S W
P910,911	13124435	CONNECTOR,ZH S 2B-ZR
P912	13124439	CONNECTOR,ZH S 6B-ZR
Q102,103	S0000674	TR,DTC123JUA
Q104,105	S0019894	TRR,DTA114EUA-T106
Q400-600	5230020200	TR,2SA1314B-TE12L,C
Q902,903	13427337	TR,2SC2412K
R156	R0016720	VAR RES,4.7KB RH0422C
U100	S00381800A	IC,ATF-CTRL
U101	S0038383	IC,CXA1814N
U102,103	S0020414	IC,NJM2233BV-TE1
U104	S0001204	IC,TC4W53FU-TE12L
U105	S0038394	IC NJM2119M,
U201	5220448800	IC,LB8110M
U401-601	5220448900	IC,LB1851M
U602	5220450800	IC,TL5001CPS-T
U701	5220449000	IC,LB1836M
U901	S00241900A	IC,UPD78146GF-025-3BA
U902	S0033274	IC,SN74LV00APW
U903	S0020454	IC,SN74LV14PW
U904	S0033414	IC,M93C46-MN6T
U905	S0034654	IC,TC7S08FU

DSUB PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95105600A	PCB ASSY,DSUB
D1-12	13411596	DIODE,IMN10
F1	E0039020	CKT PTCT,RXE010
J8-10	E0022450	CONNECTOR,DIN5 YKF51-5040
J11	E0032230	CONNECTOR,DSUB 37PIN
J12	E0032220	CONNECTOR,DSUB 25PIN
L2-9	5347027700	FERRITE BEADS,CHIP BK2125HS121
L10-17	5292810900	EMI FILTER,CHIP 100PFT
P3	E0032364	CONNECTOR,FMN 16BMT
P4	5336249200	PLUG,CONN. B02B-PH-K-S(WHT)
Q1-5	13428287	TR,DTC124EKAT-146
R11	11985206	RES ARRAY,CHIP 4X10K J
R18,19	11985206	RES ARRAY,CHIP 4X10K J
R21,22	11985206	RES ARRAY,CHIP 4X10K J
R91	11985206	RES ARRAY,CHIP 4X10K J
U1	S0024314	IC,TC74VHCT00F(EL)
U2	S0024184	PHOTO COUPLER,PC400
U3	S0000584	IC,HD74HC541FPEL
U4	5220121100	IC,HD74HC595FPEL
U5	S0036924	TR,TD62381F TP
U6	5220117000	IC,HD74HC597FP
U7	S0038234	IC,TC74HCT244AF
U8	5220111400	IC,HD74HC132FP
U9,10	E00595800A	TRANS,PULSE 400UH
U11	S0038974	IC,DS26C31TMX
U12,13	E00595800A	TRANS,PULSE 400UH
U14	S0038984	IC,DS26C32ATMX
U15-18	E00595800A	TRANS,PULSE 400UH
U19	S0020344	IC,TC74VHC541

BNC PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95105500A	PCB ASSY,BNC
J1-3	E0033070	JACK,P2286-A BNC3P(1SW)
J4-5	E0033060	JACK,P2360 BNC2P(1SW)
J6	E0032200	CONNECTOR,DSUB 9PIN
J7	5334076000	SOCKET,CANNON CONNECTOR
L1	5347027700	FERRITE BEADS,CHIP BK2125HS121
P1	E0032364	CONNECTOR,FMN 16BMT
P2	5334072800	PLUG,CANNON CONNECTOR

RF PLAY PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106000B	PCB ASSY,RF PLAY
	*M01101400A	SHIELD COVER,RF P
D11,12	S0023224	DIODE,DAN217 T146
K1,2	E0054744	RELAY,G6K-2F
L1,2	14728152	COIL,CHIP 47UF 10%
L5,6	14728152	COIL,CHIP 47UH 10%
L51	14728152	COIL,CHIP 47UH 10%
P1	13153472	CONNECTOR,8P
P3	13124021	CONNECTOR,ZN S 4B-ZR
P4	13124440	CONNECTOR,ZH S 7B-ZR
P6	5336287200	PLUG,CONN. S2B-PH-K-S(WHT)
P101	5336287600	PLUG,CONN. S6B-PH-K-S(WHT)
Q9,10	13427337	TR,2SC2412K
Q11-15	S0020404	TR,DTC124EEATL
Q17	13427256	TR,DTD123YK
Q18	S0024374	TR,DTA124EETL
R91-94	R0016700	VAR RES,2.2KB RH0422C
U1,2	5220449300	IC,HA12133MP
U3	13448164	IC,CXA1077M-T4
U5	S0020414	IC,NJM2233BV-TE1

RF REC PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106100B	PCB ASSY,RF REC
	*M01101500A	SHIELD COVER,RF R
D13,14	S0023224	DIODE,DAN217 T146
K3,4	E0054744	RELAY,G6K-2F
L1,2	11986516	COIL,CHIP 47UH 10%
L5,6	11986516	COIL,CHIP 47UH 10%
L52	11986516	COIL,CHIP 47UH 10%
P2	13153472	CONNECTOR,8P
P3	13124438	CONNECTOR,ZH S 5B-ZR
P5	13124025	CONNECTOR,ZN S 8B-ZR
P6	5336287200	PLUG,CONN. S2B-PH-K-S(WHT)
P102	5336291600	PLUG,CONN. S6B-PH-K-R(RED)
Q9,10	13427337	TR,2SC2412K
Q11-15	S0020404	TR,DTC124EEATL
Q16	13427250	TR,DTB123YK
Q18	S0024374	TR,DTA124EETL
R91-94	R0016700	VAR RES,2.2KB RH0422C
U1,2	5220449300	IC,HA12133MP
U4	13448164	IC,CXA1077M-T4
U5,6	S0020414	IC,NJM2233BV-TE1

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106300C	PCB ASSY,SYS
	*M00473600A	HEATSINK,IOX
	*M00473900A	SPACER,IOX
	*5780002606	SCREW,BIND M2.6X6
BT1	E0055380	BATTERY,CR2032
BT1A	E0055390	HOLDER,BCR20V4
D001,002	13411644	DIODE,CHIP 1SS355 TE-17
D003	S0035734	DIODE,1SS377(TE85L)
D201,202	S0021344	DIODE,RB160L-40
D301,304	S0021344	DIODE,RB160L-40
D302,303	S0035214	DIODE,HVC376B-TRF
D305	5228018100	C,VARI HVU17TR
D402	S0023224	DIODE,DAN217 T146
D501-503	S0021344	DIODE,RB160L-40
D504	5228018100	C,VARI HVU17TR
D505	S0020814	ZENER DIODE,UDZ 5.1B
D506	S0025274	DIODE,RB706F-40
D507	5228018100	C,VARI HVU17TR
D601	S0023224	DIODE,DAN217 T146
D602,603	13411596	DIODE,IMN10
D604	S0025274	DIODE,RB706F-40
D605,606	13411596	DIODE,IMN10
D701-705	13411596	DIODE,IMN10
D706	S0025274	DIODE,RB706F-40
D707-711	13411596	DIODE,IMN10
D712	S0023224	DIODE,DAN217 T146
D713	S0025274	DIODE,RB706F-40
D714	13411596	DIODE,IMN10
D715	S0021344	DIODE,RB160L-40
D716	S0025274	DIODE,RB706F-40
D717-723	13411596	DIODE,IMN10
D801	S0025274	DIODE,RB706F-40
D802	S0023224	DIODE,DAN217 T146
D803,804	S0025274	DIODE,RB706F-40
D901	S0025274	DIODE,RB706F-40
J701	E0032220	CONNECTOR,DSUB 25PIN
J702-704	E0032210	CONNECTOR,DSUB 15PIN
J801,J901	E0032364	CONNECTOR,FMN 16BMT
L301,303	14728209	COIL,CHIP 47UH
L302,304	5286051500	COIL,CHIP 2.7UH K LK2125
L305,306	14728209	COIL,CHIP 47UH
L307	5286051300	COIL,CHIP 2.2UH K LK2125
L601-604	E0055364	COIL,COILCHIP 1000UH 5%
L801	E0031304	BEAD COIL,BLM21A601S
L802-805	E0055364	COIL,COILCHIP 1000UH 5%
P001-003	5336303400	PLUG,CONN. B4B-EH(WHT)
P401	5336249300	PLUG,CONN. B03B-PH-K-S(WHT)
P601	E0033020	CONNECTOR,PCN10MA-144P
P602	5336249900	PLUG,CONN. B09B-PH-K-S(WHT)
P901	5336249200	PLUG,CONN. B02B-PH-K-S(WHT)

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
Q403-406	13428287	TR,DTC124EKAT-146
Q407	S0019224	TR,DTC143XUA T106
Q601	S0019224	TR,DTC143XUA T106
Q604-611	13428287	TR,DTC124EKAT-146
Q701	S0019224	TR,DTC143XUA T106
Q801	S0019204	TR,2SC4081 T106R
R019	R0067304	RES ARRAY,1/16W 4X10K J
R039	R0067224	RES ARRAY,1/16W 4X4.7K J
R437-440	R0066374	VAR RES,EVM3VSX50B54
R601	R0092704	RES ARRAY,1/16W 4X47 J
R604	R0067304	RES ARRAY,1/16W 4X10K J
R606-609	R0092754	VAR RES,1KB RH03ADC
R622,623	R0092704	RES ARRAY,1/16W 4X47 J
R636	R0067304	RES ARRAY,1/16W 4X10K J
R637	R0092704	RES ARRAY,1/16W 4X47 J
R641-643	R0092704	RES ARRAY,1/16W 4X47 J
R644	R0067304	RES ARRAY,1/16W 4X10K J
R647,648	R0092704	RES ARRAY,1/16W 4X47 J
R701 R702	R0092714	RES ARRAY,1/16W 4X2.2K J
R706-709	R0092704	RES ARRAY,1/16W 4X47 J
R710,711	R0067224	RES ARRAY,1/16W 4X4.7K J
R727	R0067304	RES ARRAY,1/16W 4X10K J
R728	R0092704	RES ARRAY,1/16W 4X47 J
R731,732	R0092704	RES ARRAY,1/16W 4X47 J
R903	R0092704	RES ARRAY,1/16W 4X47 J
R911	R0092704	RES ARRAY,1/16W 4X47 J
R916	R0067304	RES ARRAY,1/16W 4X10K J
S001	E0031074	SW,SLIDE SW CHS-04TA
U001	S0024314	IC,TC74VHCT00F(EL)
U002	13444685	IC,74HC 574F
U003	S0025594	IC,TC74VHC163FEL
U004	S0018944	IC,TC74VHCU04F(EL)
U005	S0035143	IC,XCS10-3TQ144C
U007	5220118000	IC,TC74HC32AF-TP2
U008	5220103800	IC,TC74HC157AF-TP2
U009	S00396800C	IC,SX28AC SC2
U010	S0024464	IC,M62001FP-600D
U011	S00396700B	IC,SYS V1.02 LH28F800SGN-70
U011	E0033093	SOCKET,44PIN SOP IC179
U012	S0035133	IC,HD6437043AE00F
U013	S00351700D	IC,SX28AC/SS TC
U014,015	S0037443	IC,BS62LV1024TC-70
U016	S00397100A	IC,SX28AC TCR
U017	13444685	IC,74HC 574F
U018	5220116400	IC,HD74HC138FP
U019	S0025614	IC,TC74VHCT541AFEL
U101	S0020334	IC,TC74VHC04
U102	5220118000	IC,TC74HC32AF-TP2
U103	E0013344	CRYSTAL OSC,22.5792MHZ
U104	E00546900A	CRYSTAL OSC,49.152MHZ

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
U105	S0020354	IC,TC74VHC74
U106	S00177600A	IC,CLK1
U107,108	5220104000	IC,TC74HC595AF-TP2
U109	S00190600A	IC,IOX
U110	S0024353	IC,DSP TMS57070FFT
U111	S0039753	IC,M11B16161A-45T
U112	S0020344	IC,TC74VHC541
U201,202	S0035714	IC,BA033FP
U203,204	S0025614	IC,TC74VHCT541AFEL
U205	S00335600A	IC,DTRS-HR DEC
U206	S00335500A	IC,DTRS-HR ENC
U207-211	S0042224	IC,63LV1024-15T
U301	S0018944	IC,TC74VHCU04F(EL)
U302,306	13447922	IC NJM78L05UA-TE1
U303,305	5220123500	IC,MC74HC4046AF-FR1
U304	S0018944	IC,TC74VHCU04F(EL)
U307,311	S0029674	IC,TLC2932IPWR
U308,309	S0020354	IC,TC74VHC74
U310	S0018944	IC,TC74VHCU04F(EL)
U401,402	S0035274	IC,MAX913CSA
U403,404	5220101800	IC,HD49229
U406	E0042034	RELAY,ATX206SA 2C,SMT
U407-409	5292811400	EMI FLTR,CHIP 10000PFT
U410	S0024314	IC,TC74VHCT00F(EL)
U501	13447922	IC,NJM78L05UA-TE1
U502,802	S0020064	IC,MC74HC4538AF LEFT
U503	S0024284	IC,NJM 78L09UA-TE1
U504	S0024294	IC,NJM 79L09UA-TE1
U505	S0024304	IC,NJU201AM-TE2
U506	S0018944	IC,TC74VHCU04F(EL)
U507	S0032804	IC,NJM082BV(TE1)
U508	S0004244	IC,LINEER,LF356MX
U601-605	S0020344	IC,TC74VHC541
U606	S0024314	IC,TC74VHCT00F(EL)
U607-610	S0025614	IC,TC74VHCT541AFEL
U611,614	S0019594	IC,TC74VHC08F(EL)
U612	E0042034	RELAY,ATX206SA 2C,SMT
U613	S0025614	IC,TC74VHCT541AFEL
U615	S0025614	IC,TC74VHCT541AFEL
U616	S0024314	IC,TC74VHCT00F(EL)
U701	5220116700	IC,HD74HC240FP TAPE
U702	S0037124	IC,TC74LCX541F(EL)
U703	E0042034	RELAY,ATX206SA 2C,SMT
U704	5220115800	IC,MC74HC14AF TAPE
U705	S0026540	IC,M5M34051FP
U706	5220103800	IC,TC74HC157AF-TP2
U707	S0026540	IC,M5M34051FP
U708	5220120700	IC,HD74HC153FPEL
U801	S0026540	IC,M5M34051FP

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
U803	S0020354	IC,TC74VHC74
U804	S0024314	IC,TC74VHCT00F(EL)
U805	S0018944	IC,TC74VHCU04F(EL)
U806	13448089	IC,LIN LM1881M
U807	5220102000	IC,SN74S140NS
U808	5220120700	IC,HD74HC153FPEL
U809,810	S0023994	IC,NJM4565M-T1
U901,903	S0025614	IC,TC74VHCT541AFEL
U902	S0036964	IC,LC89051V
U904	S0036913	IC,XCS20XL-4VQ100C
X001	E00547000A	RESONATOR,SD3 32MHZ
X501	E00331100B	RESONATOR,9.60MHZ SMT
X502	E00331000B	RESONATOR,8.82MHZ SMT

KEY PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95103010B	PCB ASSY,KEY
	E0054840	LCD,MC2004E-SYL-2
	M01077400A	COLLAR,LCD
	E00351400A	HARNESS ASSY,FRONT DA98
D1-55	S0022094	DIODE,1SS355
D57-64	M00572500A	LED ASSY,BAR METER 15DOT
D65,67	S0038240	LED,LT3ED87
D65A,67A	M00608702A	SPACER,LH-5 L=10
D69,71	S0038240	LED,LT3ED87
D69A,71A	M00608702A	SPACER,LH-5 L=10
D73,75	S0038240	LED,LT3ED87
D73A,75A	M00608702A	SPACER,LH-5 L=10
D77,79	S0038240	LED,LT3ED87
D77A,79A	M00608702A	SPACER,LH-5 L=10
D81-93	5225018500	LED,SLR-34DU3F
D81A-93A	5801550400	SPACER,LH-5 L=14.0
D100	5225013500	LED,SLR-34VR3F (R)
D100A	5801550400	SPACER,LH-5 L=14.0
D125-130	5225018500	LED,SLR-34DU3F
D131	5225013600	LED,SLR-34MG3F (GRN)
D132-134	5225018500	LED,SLR-34DU3F
D135	5225013600	LED,SLR-34MG3F (GRN)
D136-139	5225018500	LED,SLR-34DU3F
D140,141	5225013600	LED,SLR-34MG3F (GRN)
D142	5225013500	LED,SLR-34VR3F (R)
D125A-136A	M00608702A	SPACER,LH-5 L=10
D137A-142A	5801550400	SPACER,LH-5 L=14.0
D143,144	5225018500	LED,SLR-34DU3F
D143A,144A	M00608702A	SPACER,LH-5 L=10
D145,147	S0038240	LED,LT3ED87

KEY PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
D145A,147A	5801550400	SPACER,LH-5 L=14.0
D149	S0038240	LED,LT3ED87
D150	S0043884	LED,GM5BC01200AC
P1,2	5336370000	PLUG,CONN. 8P BTK-2S-H
P3	5336288000	PLUG,CONN. S10B-PH-K-S W
P4	5336242600	PLUG,CONN. B16B-PH-K-S
P5	5336370000	PLUG,CONN. 8P BTK-2S-H
Q1	S0001054	TR,2SD1757K
Q2-7	S0001664	TR,DTC114TU-106
S1	E0000460	ENCODER,SRGPHJ
S2	E0057520	SW,LC1B-L1R-1400-11
S3	5300059900	SW,PUSH(LED GRN) PLAY
S4	5300059800	SW,PUSH (LED WHT) STOP
S5,6	E00412700A	SW,LC1B-L1W-1400-12-FF
S7-56	E0021092	SW,SKHVBH
TP5	13122939	CONN.,2P IMSA-9210B-1-02-T
U1	S0024873	IC,UPD784031GC-8BT
U2	S0022434	IC,M51957AFP-600C
U4	S0028234	IC,HD74LVC541A TSSOP
U5	13445670	IC,HD74HC573F
U6	S00384100A	IC,FRONT V1.00 M27C512-12C1
U6A	E0003273	SOCKET,IC 160-0324-240*
U7	5220093300	IC,TC74HC00AF-TP2
U8	5220115800	IC,MC74HC14AF
U9-11	S0029394	IC,SN74LV138ANST-EL
U13-15	S0033394	IC,TD62M8600F-EL
U17,18	S0035690	IC,TB62701AN
X1	E0060344	OOSONATOR,29.4912MHZ

IF DSD PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95129500A	PCB ASSY,IF DSD
D1	13411667	DIODE,HRF22 CHIPTAPING
D2,3	13411596	DIODE,IMN10
J1-4	5334087600	CONNECTOR,SKT 2P(BNC) P2183
J5	E0032210	CONNECTOR,DSUB 15PIN
J6	E00667400A	FLAT CABLE,DSD98
J7	E0032200	CONNECTOR,DSUB 9PIN
L1-10	5292810900	EMI FLTR,CHIP 100PFT
P1	5334072800	PLUG,CANNON CONNECTOR
U1	S0026540	IC,M5M34051FP
U2	S0025614	IC,TC74VHCT541AFEL

DSD PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95129400A	PCB ASSY,DSD
U205	E0058404	RELAY,ATX203SA(12V)
U206	5220450400	IC,NJM5532M-T2
U207	E0058404	RELAY,ATX203SA(12V)
U302,303	S0043864	IC,DSD1700
U304	S0043963	IC,OPA2134UA
U501	S0043853	IC,XCS30XL-4TQ144C
U502,503	S0043833	IC,CXD2926AQ
U504	S0043843	IC,CXD8512Q
U511	S0037253	IC,HD6412340TE20
U512	S00443400A	IC,DSD V1.00 MBM29F040C-90PD
U512A	E0003273	SOCKET,IC160-0324-240*
U513	S0024464	IC,M62001FP-600D
U514	5220116400	IC,HD74HC138FP
U515	S0019600	IC,TC74VHC74F
U516	E0013344	CRYSTAL OSC,22.5792MHZ
U517	S0020344	IC,TC74VHC541
U601	5220123500	IC,MC74HC4046AF-FR1
U602	5220113500	IC,TC74HC4538AF-TP2
U604	E00581900A	RESONATOR,COC22AT22.57MHZ
U605	S0031074	IC,TC7S66FU(TE85L)
U606	S0018944	IC,TC74VHCU04F(EL)
U701	S0025574	IC,SN75124NS-ELL2000
U702	S0043893	IC,SN74ABT25245DW
U703	S0021514	IC,YM3437C-FE2
U704	S0038974	IC,DS26C31TMX
U705-707	S0025614	IC,TC74VHCT541AFEL
U708	S0035714	IC,BA033FP
U710,711	E00595800A	TRANS,PULSE 400UH
U712-713	S0025614	IC,TC74VHCT541AFEL

DSD SUB PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95131600A	PCB ASSY,DSD SUB
	M01341500A	COLLAR,PCB
	5780003006	SCREW,BIND M3X6
J1,2	E0068240	CONNECTOR,PB-1 10P
L1,2	E0068254	COIL,LQH43CN 10UH
U1	S0044900	IC,ADMOD79

8. INCLUDED ACCESSORIES
付属品

INCLUDED ACCESSORIES

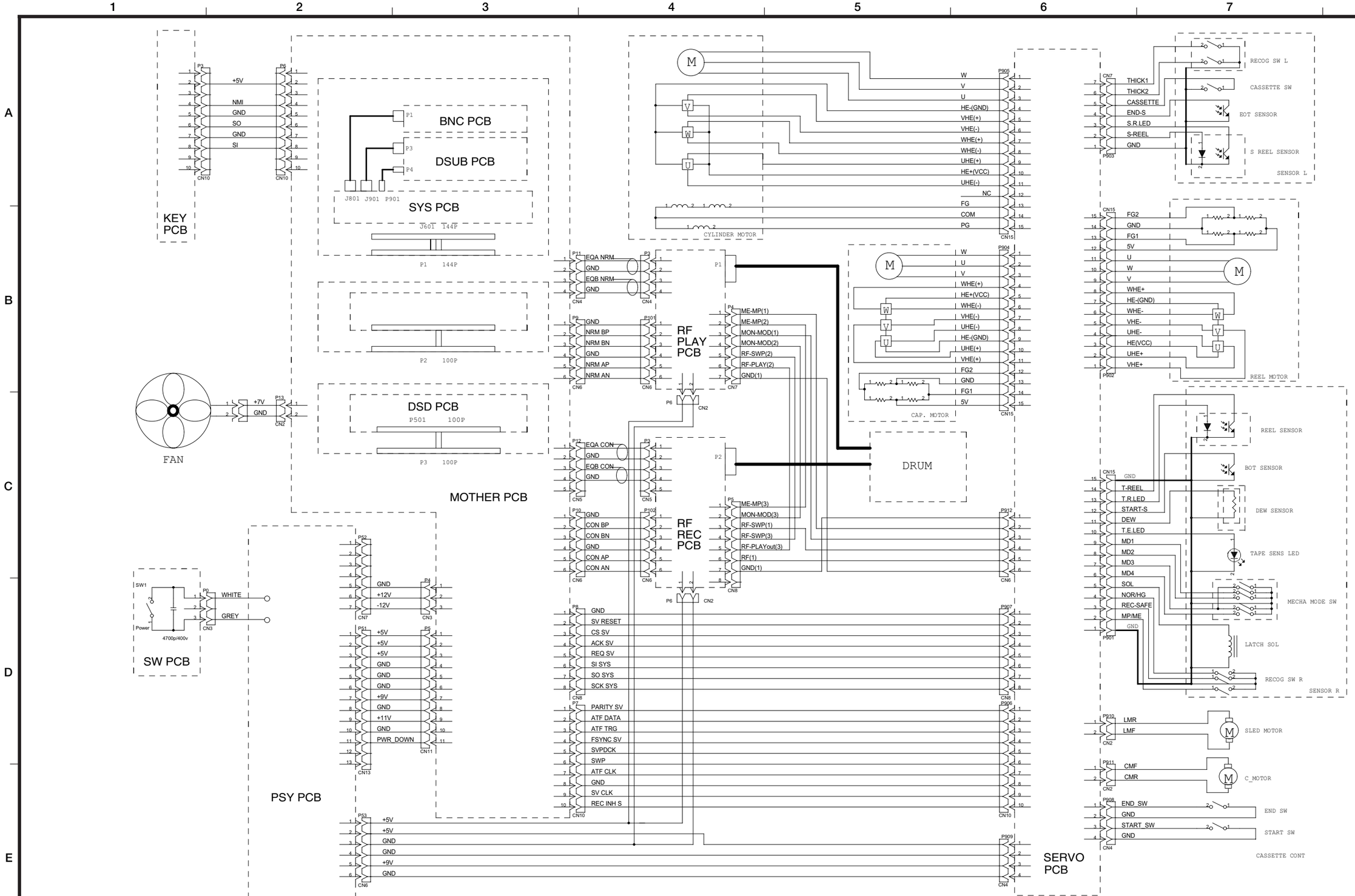
REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	*D00539500A	OWNER'S MANUAL,DA-98HR JAPANESE [J]	
	*D00635700A	OWNER'S MANUAL,DS-D98 JAPANESE [J]	
	*D00539600A	OWNER'S MANUAL,DA-98HR ENGLISH [EXCEPT J]	
	*D00635720A	OWNER'S MANUAL,DS-D98 ENGLISH [EXCEPT J]	
	*T00030500A	CLEANING TAPE,HC-8	
	5740004100	MOUNT SCREW KIT,DX-2D	
	5350014400	AC CORD ASSY [J]	
	5350018800	AC CORD SET,W/PLUG [US/C]	
	15922303	3-WIRED CORD SET [E,K]	
	5350018500	3-WIRED CORD SET (13A FUSE) [UK]	
	5350018600	3-WIRED CORD SET [A]	
	5347009000	ADAPTOR,KPR-18 [J]	

SCHEMATIC DIAGRAMS
回路図

CONTENTS 目次

WIRING (1/2) ..... Page 1/33
WIRING (2/2) ..... Page 2/33
MOTHER PCB ..... Page 3/33
SYS PCB ..... Pages 4-13/33
KEY PCB (1/2), SW PCB ..... Page 14/33
KEY PCB (2/2) ..... Page 15/33
COUNTER PCB ..... Page 16/33
BNC PCB ..... Page 17/33
DSUB PCB ..... Page 18/33
RF PLAY PCB ..... Page 19/33
RF REC PCB ..... Page 20/33
SERVO PCB ..... Pages 21-22/33
DSD PCB ..... Pages 23-30/33
DSD SUB PCB ..... Page 31/33
IF DSD PCB ..... Page 32/33
POWER SUPPLY SECTION ..... Page 33/33

SCHEMATIC DIAGRAM DS-D98 WIRING (1/2)



Digital Multitrack Recorder **DS-D98**

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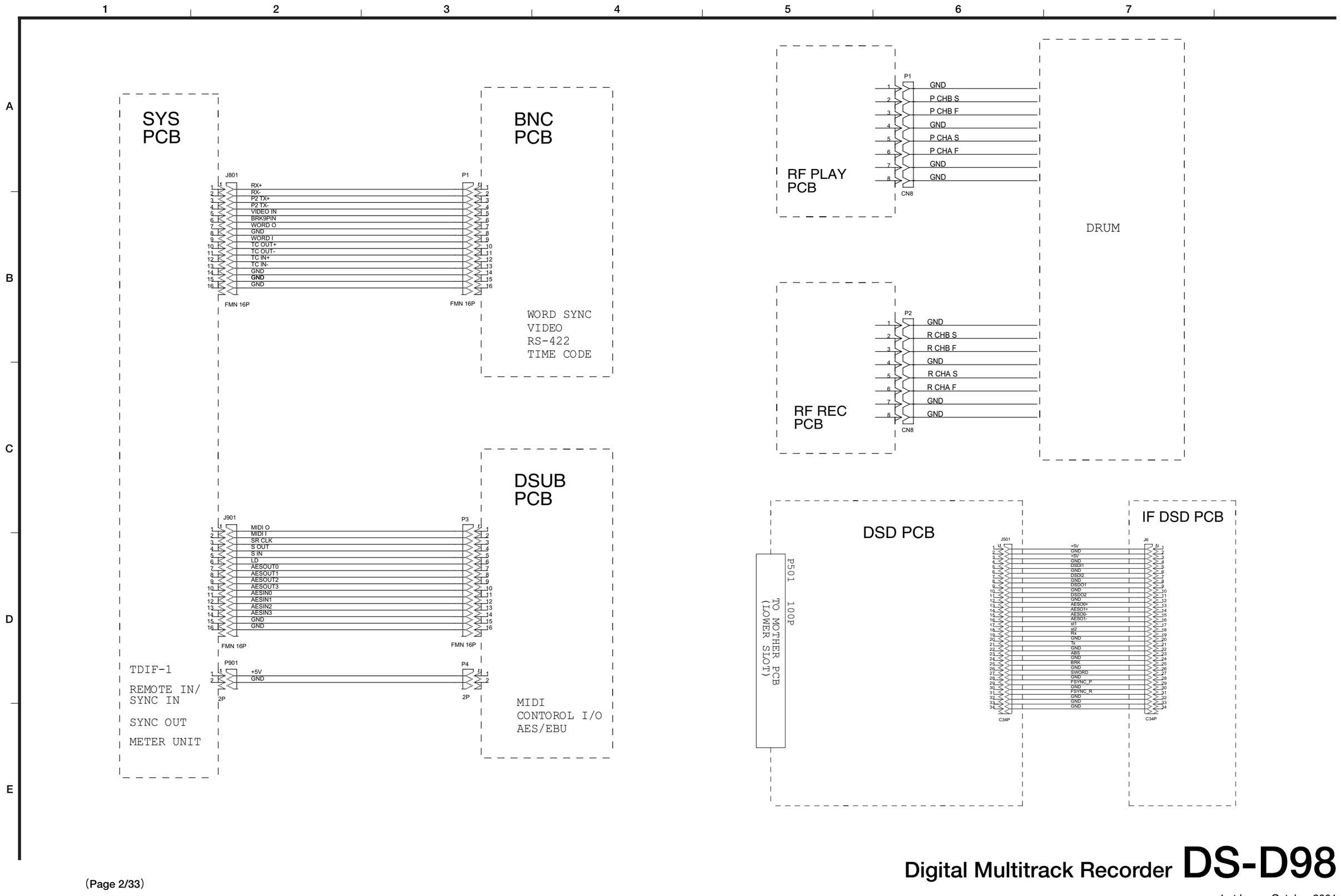

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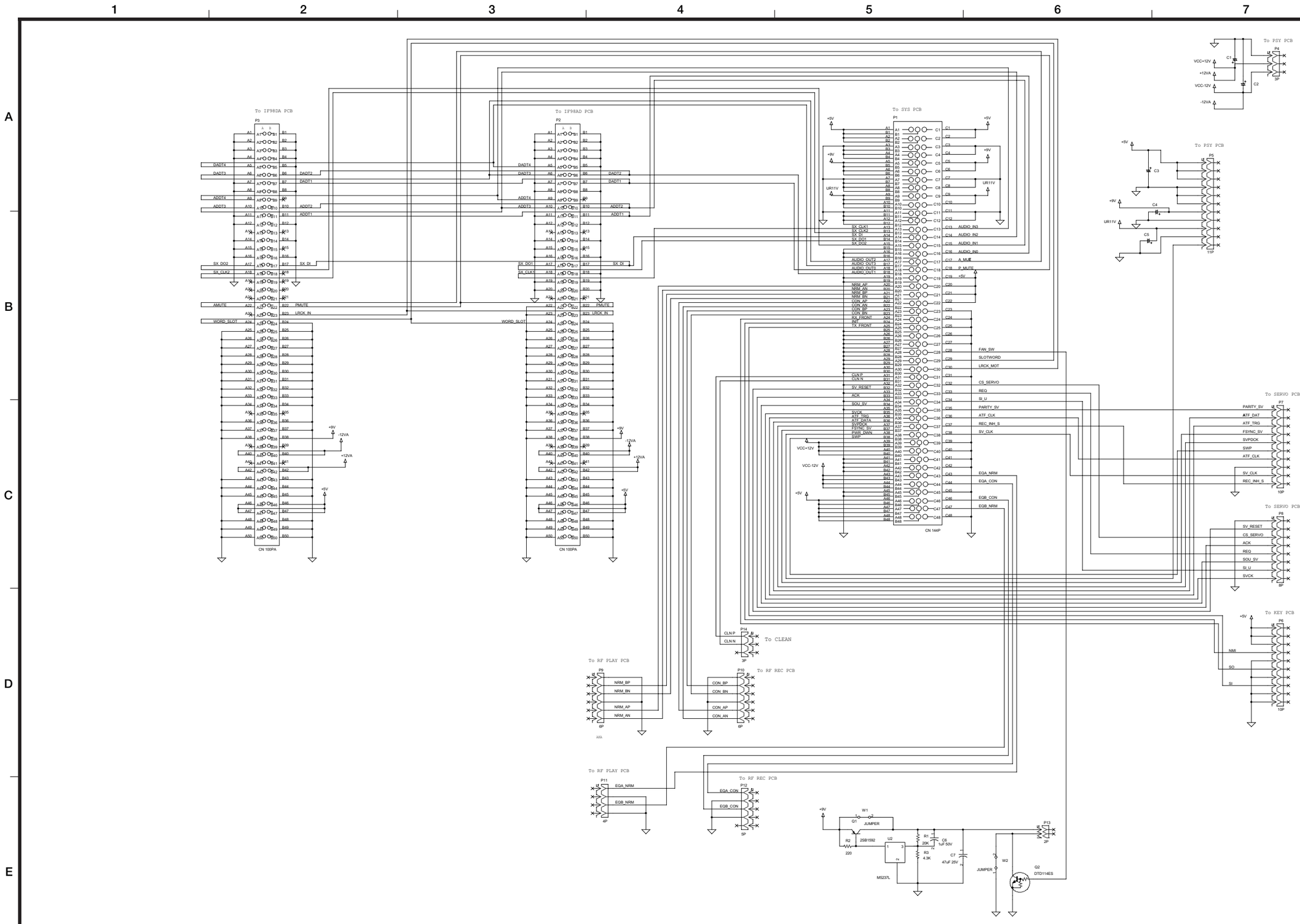
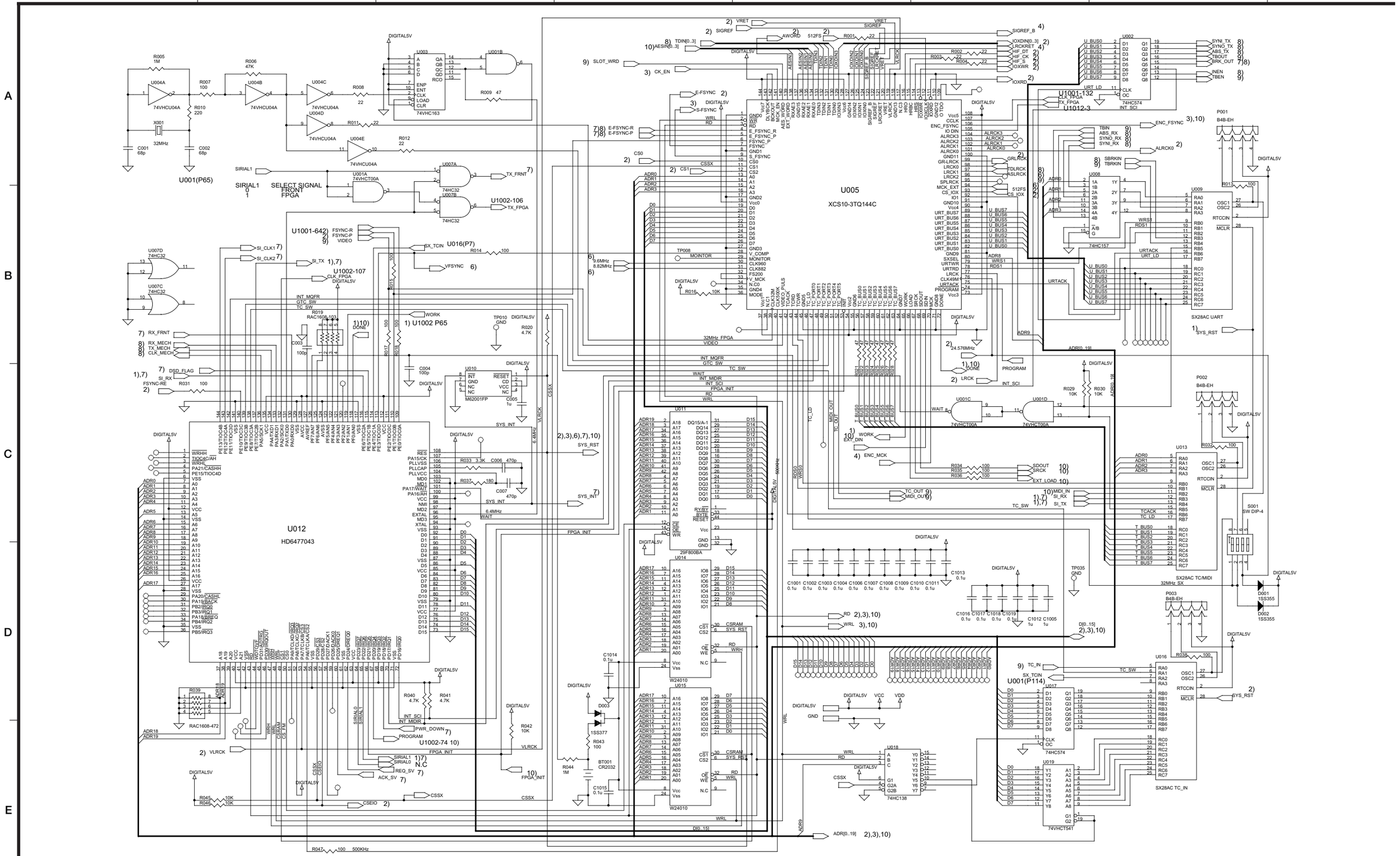


Digital Multitrack Recorder **DS-D98**

1 st Issue; October 2001

SCHEMATIC DIAGRAM DS-D98 SYS PCB (1/10)



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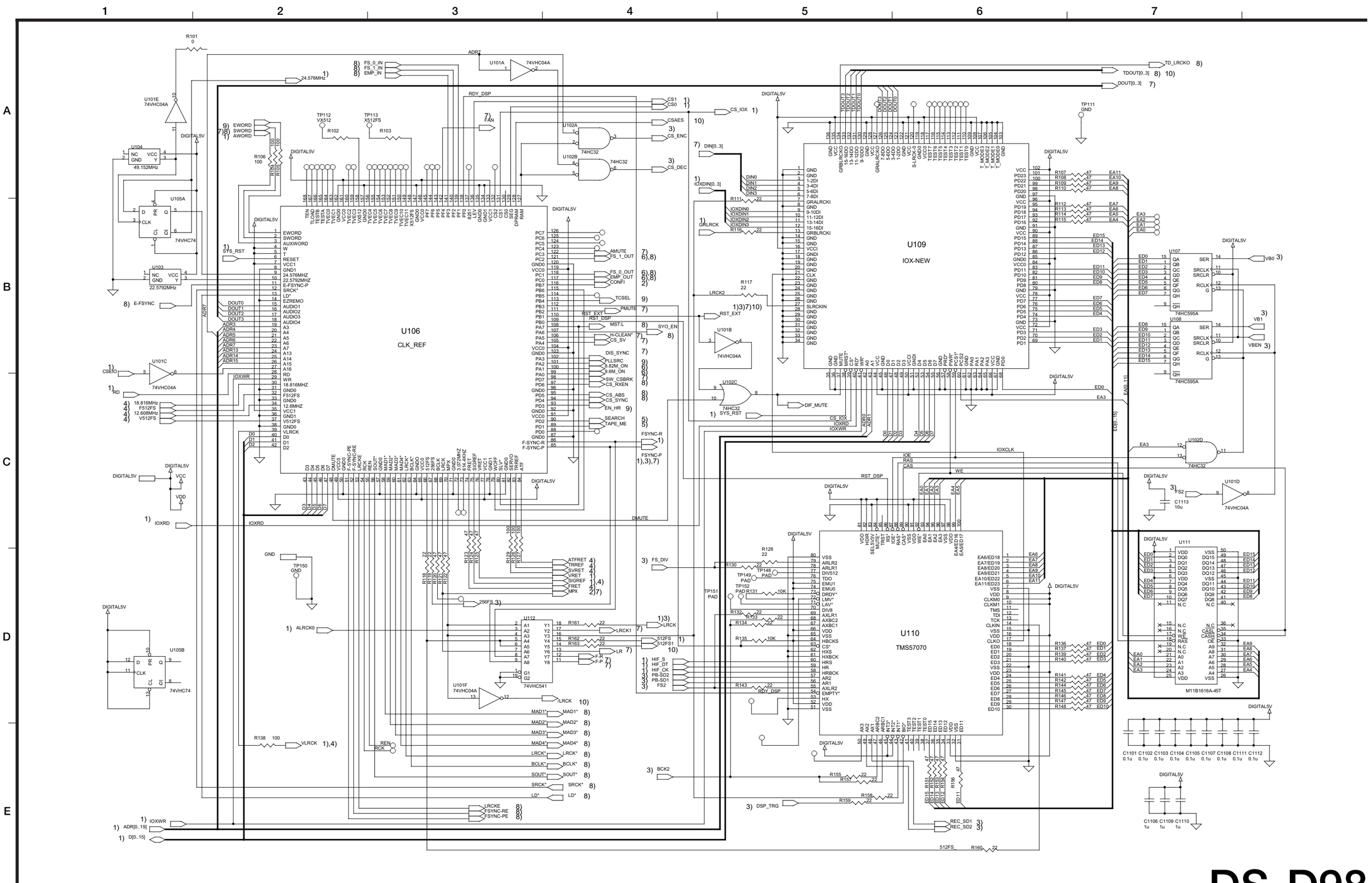

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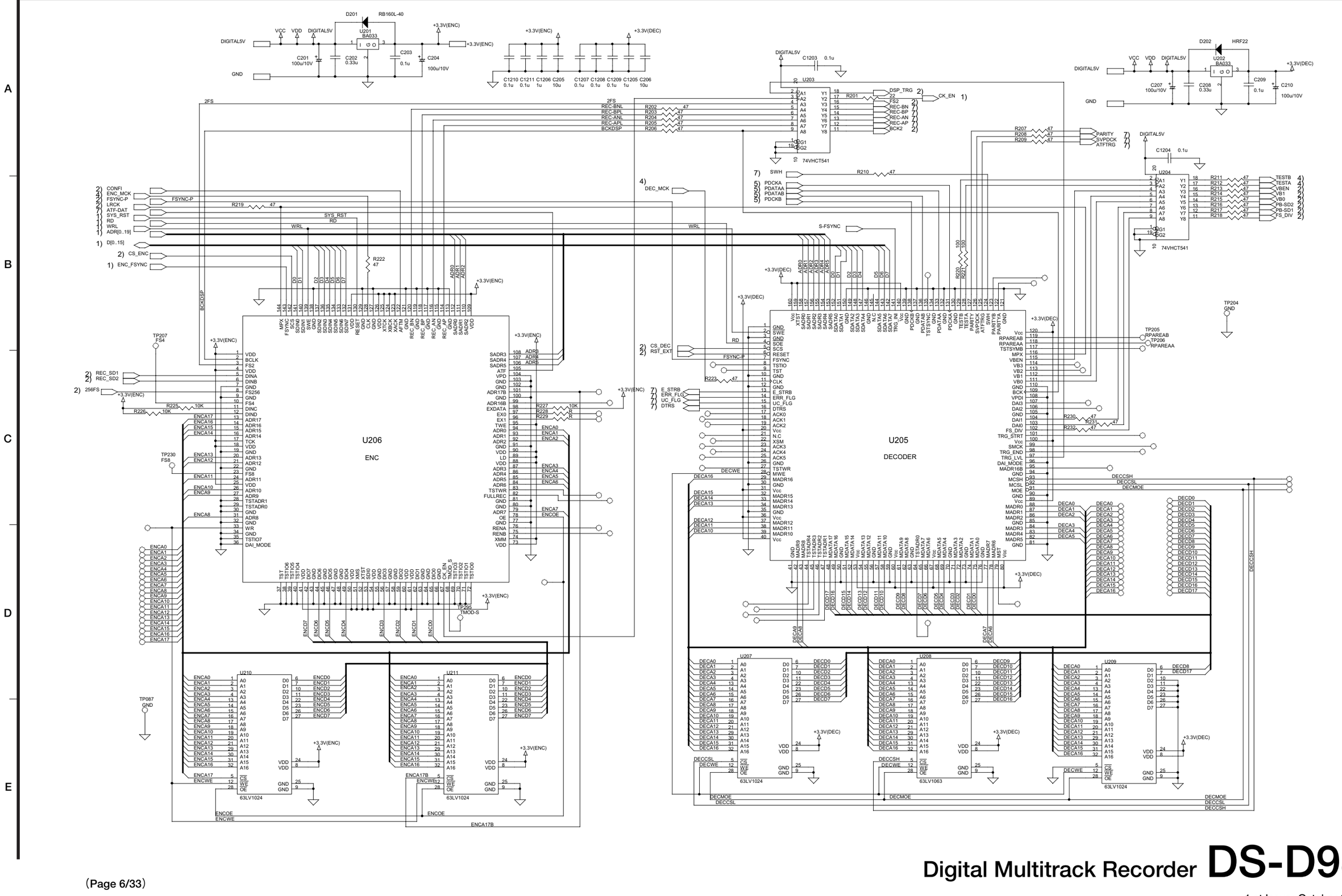

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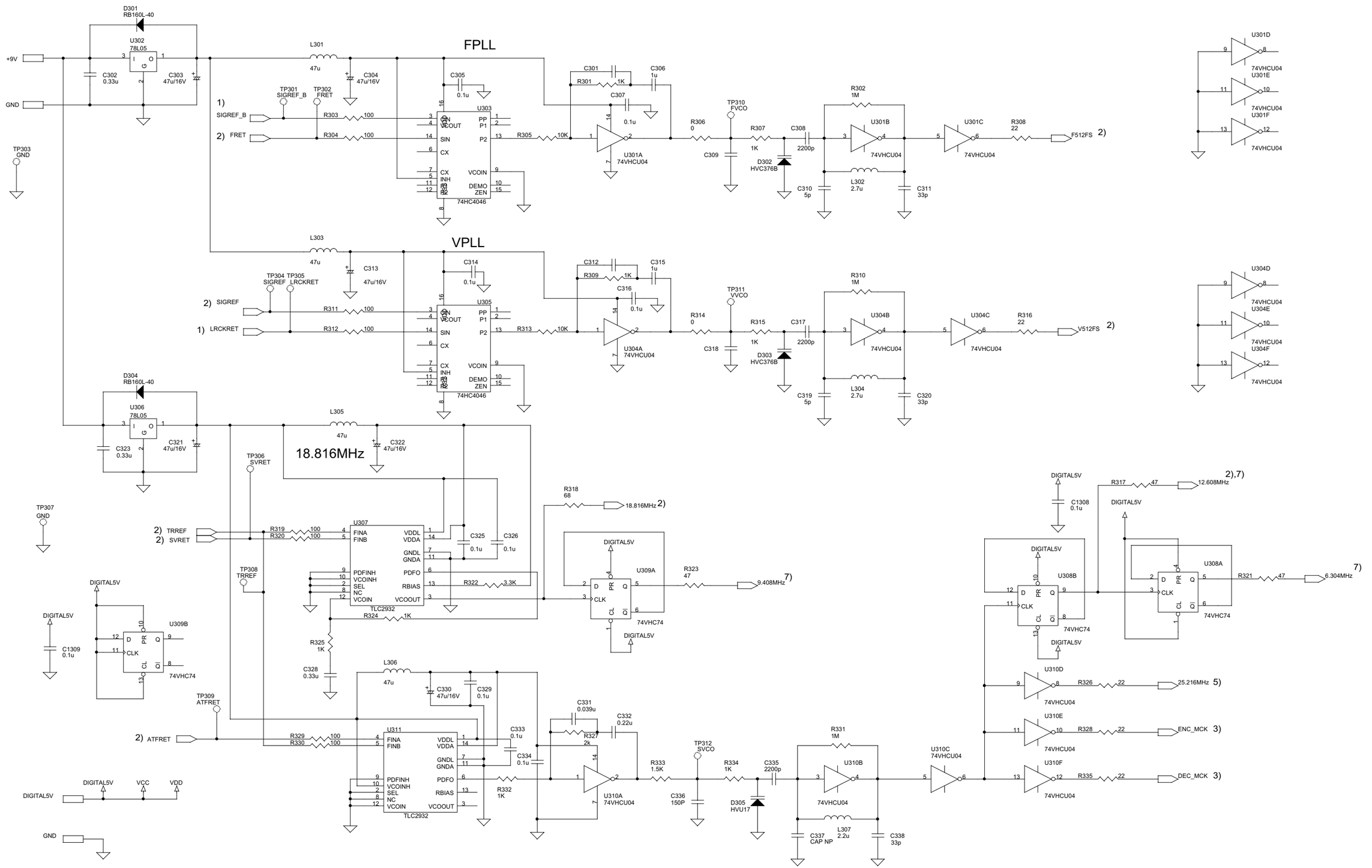

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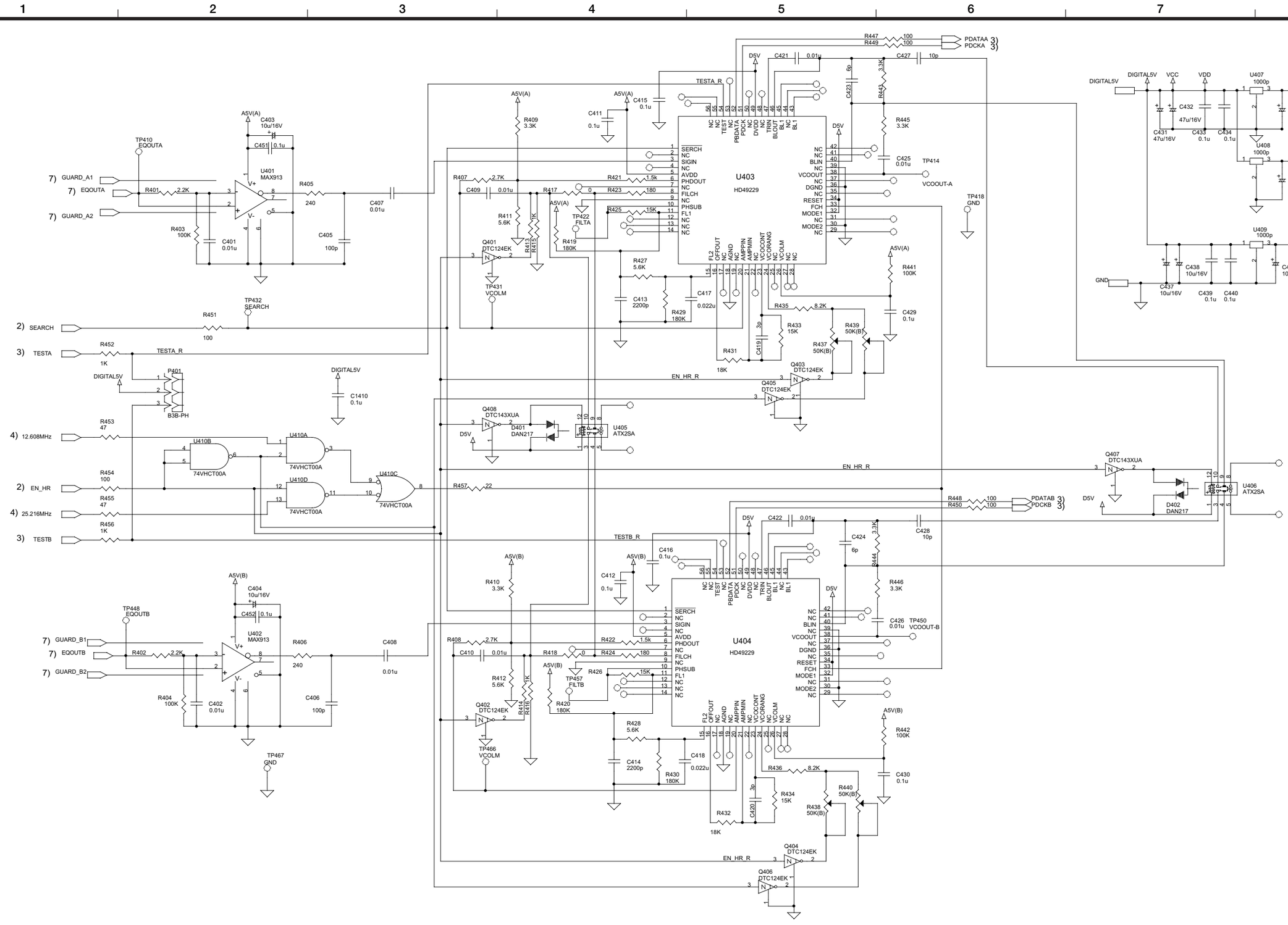

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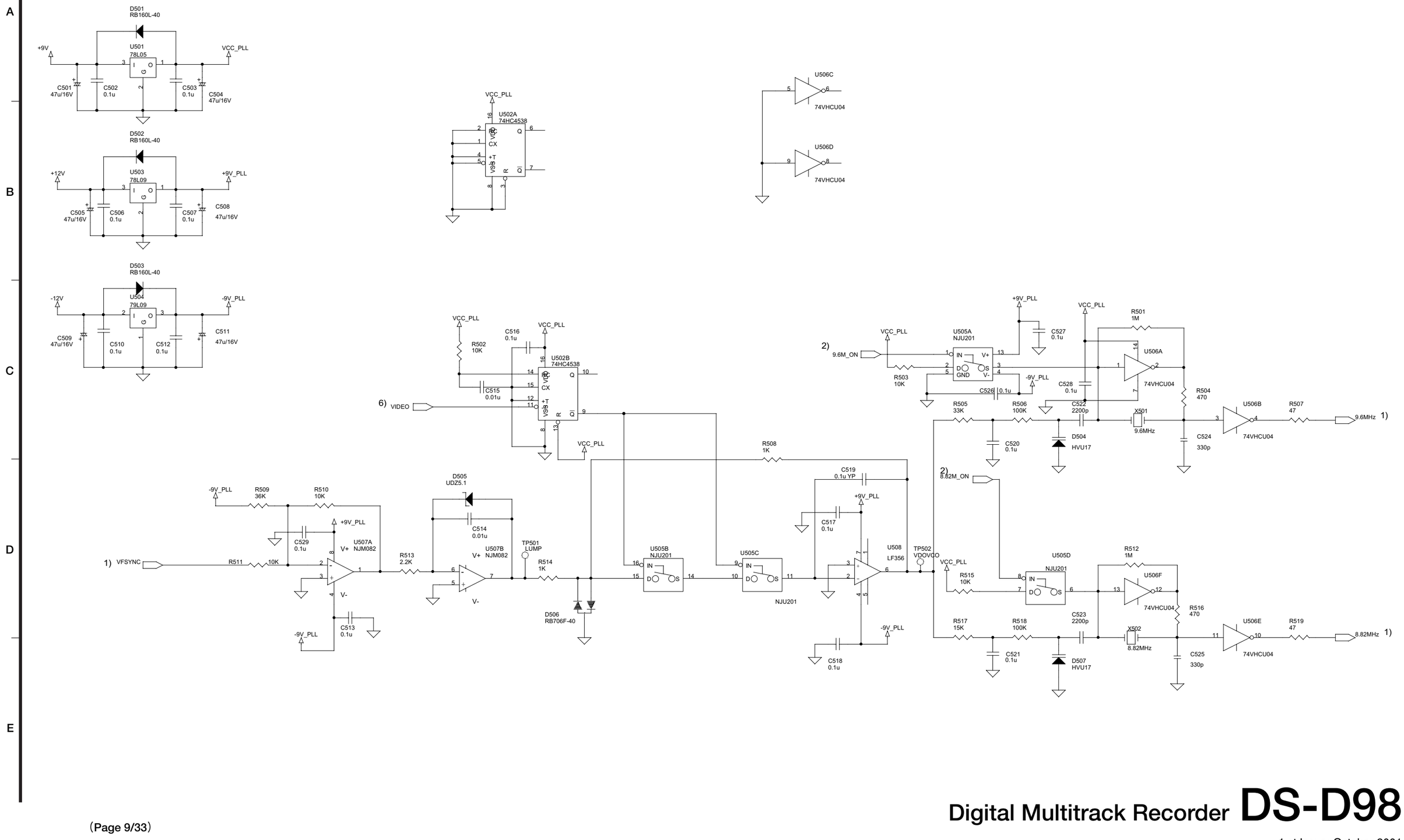

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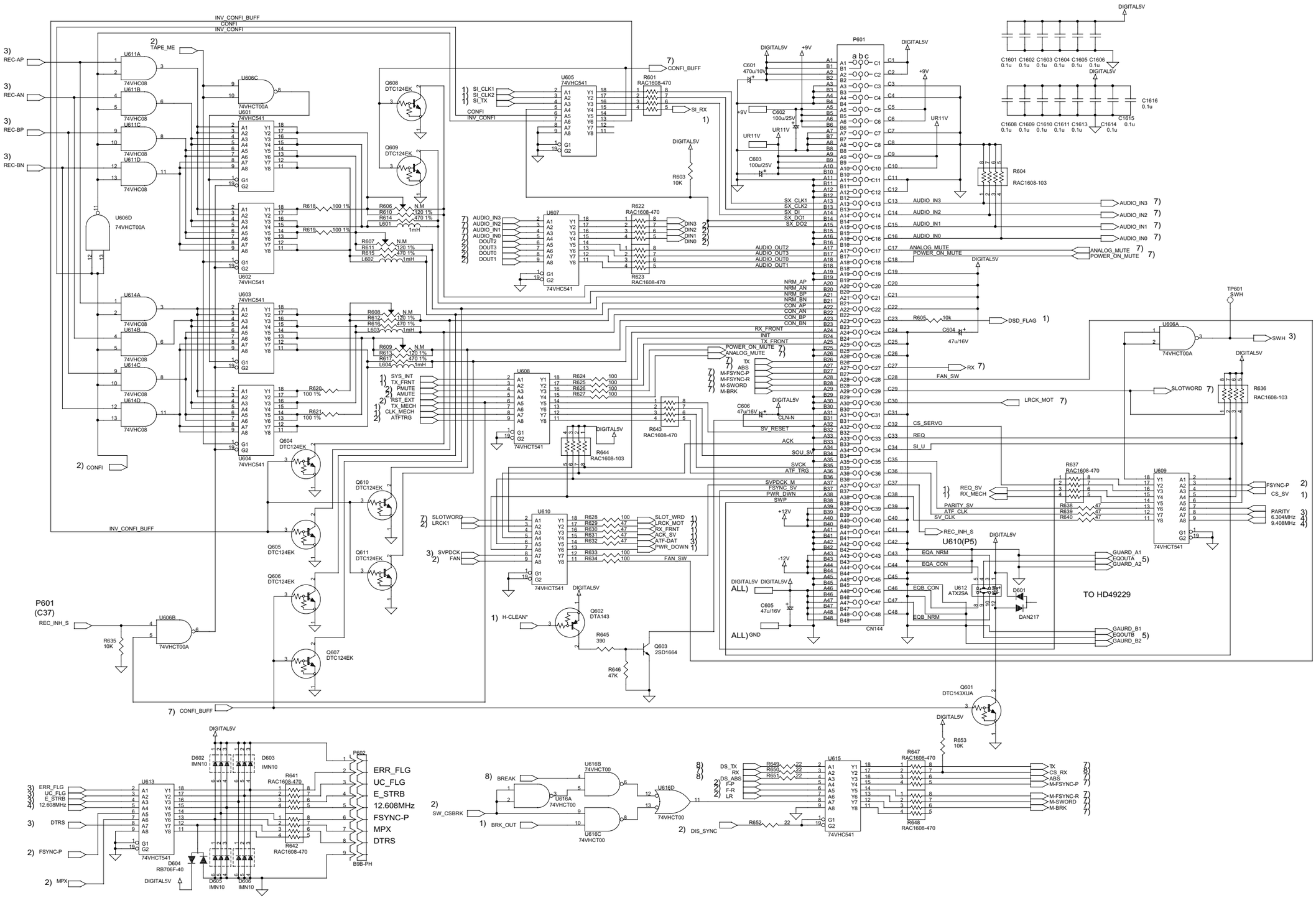


Digital Multitrack Recorder **DS-D98**

1 st Issue; October 2001

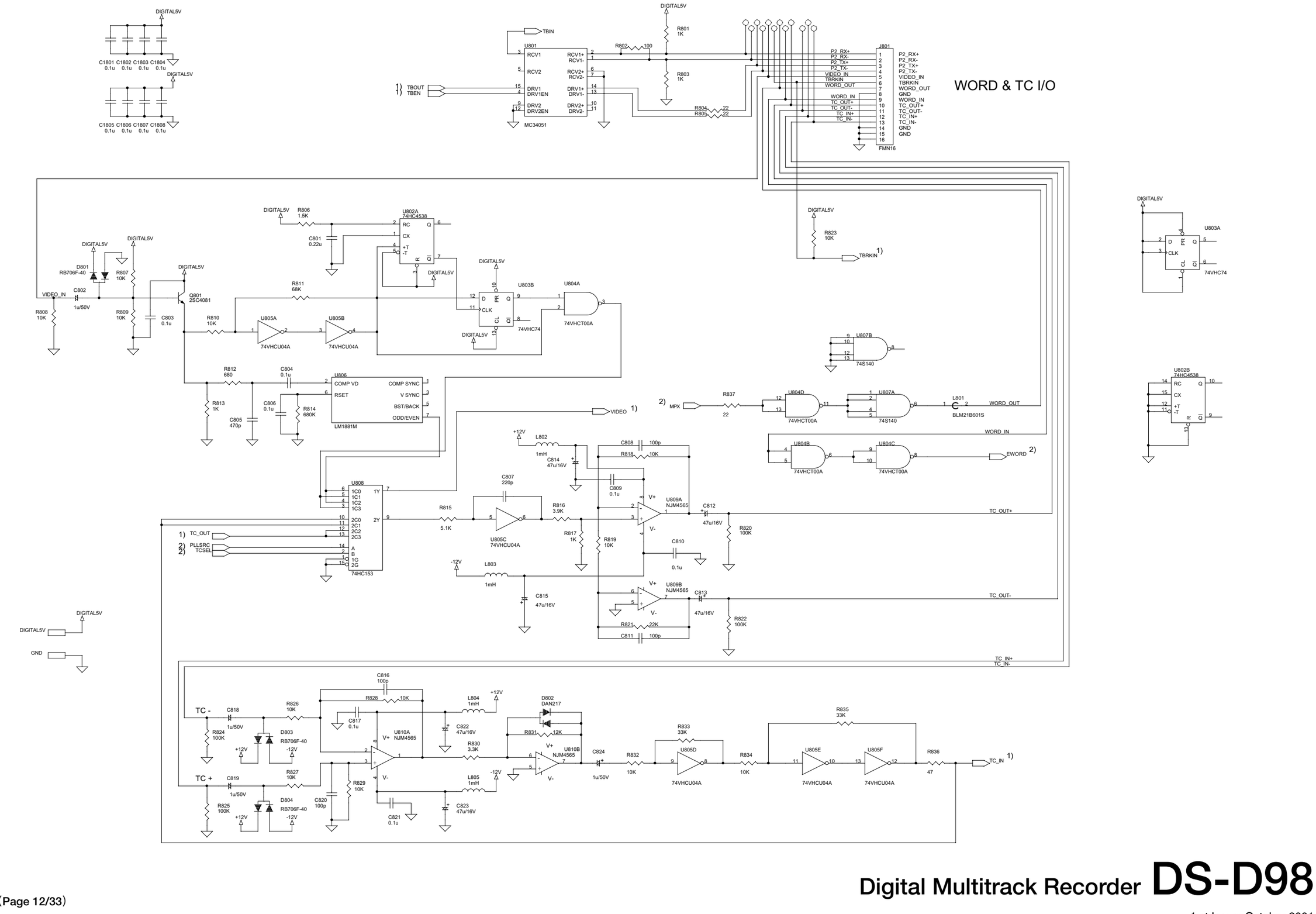
TDIF

SYNC IN

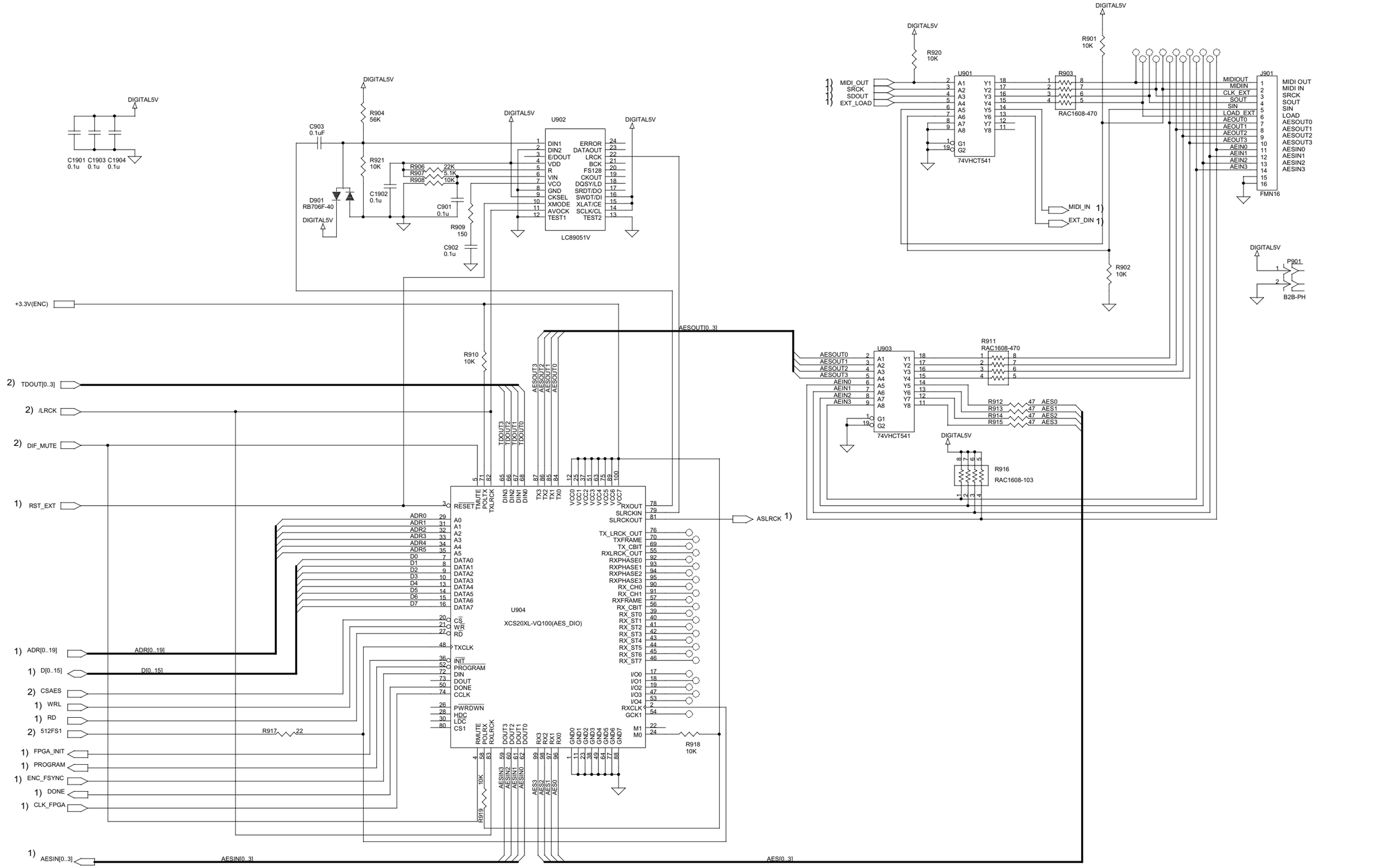
SYNC OUT

MU-8824

WORD & TC I/O


DIGITAL5V
C1801 C1802 C1803 C1804 0.1u
C1805 C1806 C1807 C1808 0.1u
TBIN
U801
MC34051
R801 1K
R802 100
R803 1K
R804 22
R805 22
1) TBOUT
1) TBEN
J801
FMN16
P2_RX+
P2_RX-
P2_TX+
P2_TX-
VIDEO_IN
TBRKIN
WORD_OUT
WORD_IN
TC_OUT+
TC_OUT-
TC_IN+
TC_IN-
GND
R823 10K
TBRKIN 1)
U803A
74VHC74
U802B 74HC4538
D801 RB706F-40
R807 10K
Q801 2SC4081
C802 1u/50V
R808 10K
R809 10K
C803 0.1u
R806 1.5K
C801 0.22u
U802A 74HC4538
R811 68K
R810 10K
U805A
U805B
74VHCU04A
U803B
U804A
74VHCT00A
R812 680
R813 1K
C804 0.1u
C805 470p
C806 0.1u
R814 680K
U806
LM1881M
COMP VD
RSET
COMP SYNC
V SYNC
BST/BACK
ODD/EVEN
VIDEO 1)
U807B
74S140
2) MPX
R837 22
U804D
U807A
L801 BLM21B601S
WORD_OUT
WORD_IN
U804B
U804C
EWORD 2)
+12V
L802 1mH
C814 47u/16V
C808 100p
R818 10K
C809 0.1u
C807 220p
U808
74HC153
1) TC_OUT
2) PLLSRC
2) TCSEL
R815 5.1K
U805C
R816 3.9K
R817 1K
R819 10K
U809A NJM4565
C812 47u/16V
R820 100K
TC_OUT+
C810 0.1u
-12V
L803 1mH
C815 47u/16V
U809B NJM4565
C813 47u/16V
R822 100K
TC_OUT-
R821 22K
C811 100p
TC_IN+
TC_IN-
DIGITAL5V
GND
C816 100p
R828 10K
TC -
TC +
C818 1u/50V
C819 1u/50V
R824 100K
R825 100K
R826 10K
R827 10K
D803 RB706F-40
D804 RB706F-40
C817 0.1u
C820 100p
C821 0.1u
U810A NJM4565
L804 1mH
L805 1mH
C822 47u/16V
C823 47u/16V
R829 10K
R830 3.3K
D802 DAN217
R831 12K
U810B NJM4565
C824 1u/50V
R832 10K
R833 33K
U805D
R834 10K
R835 33K
U805E
U805F
R836 47
TC_IN 1)

No.10



Digital Multitrack Recorder DS-D98

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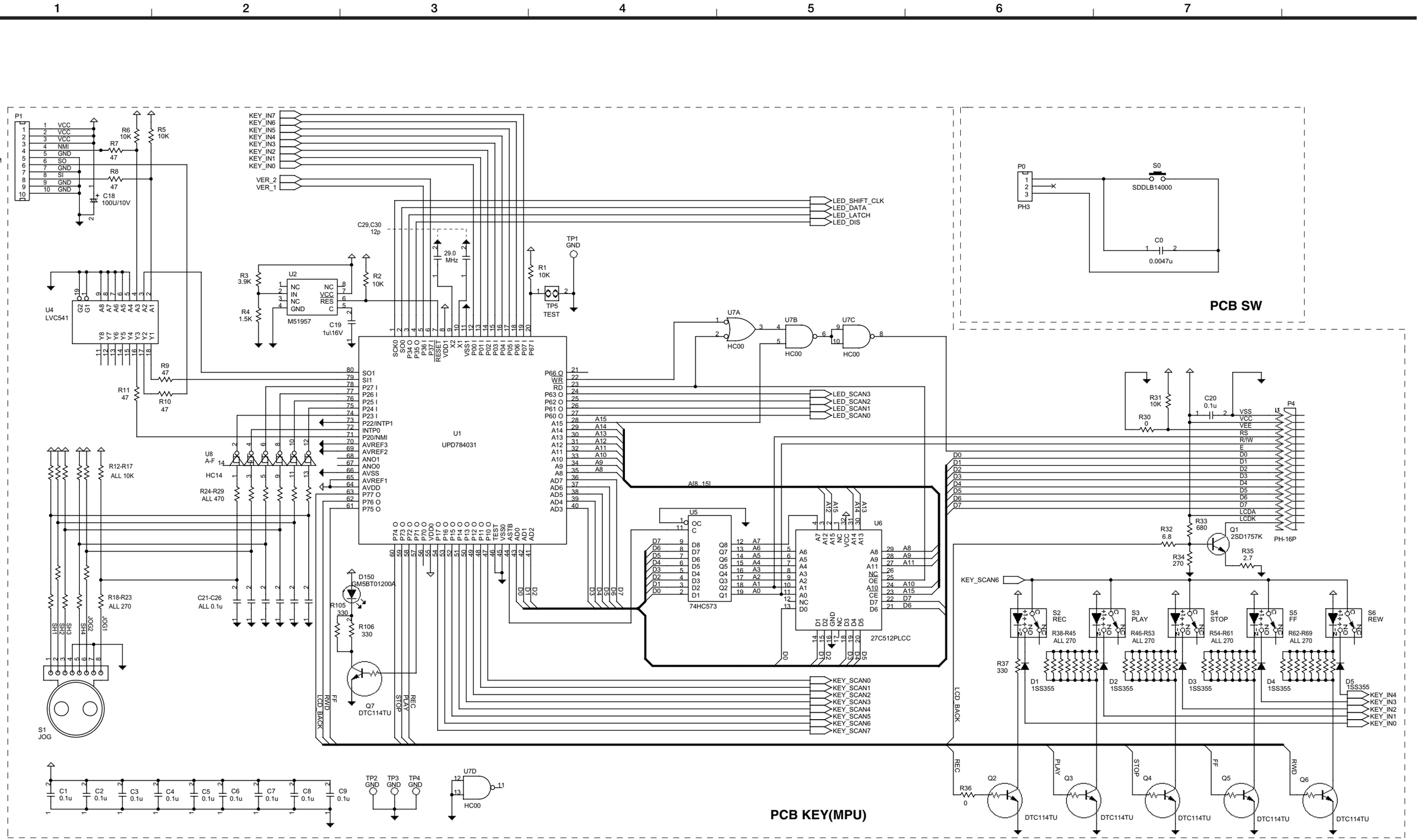
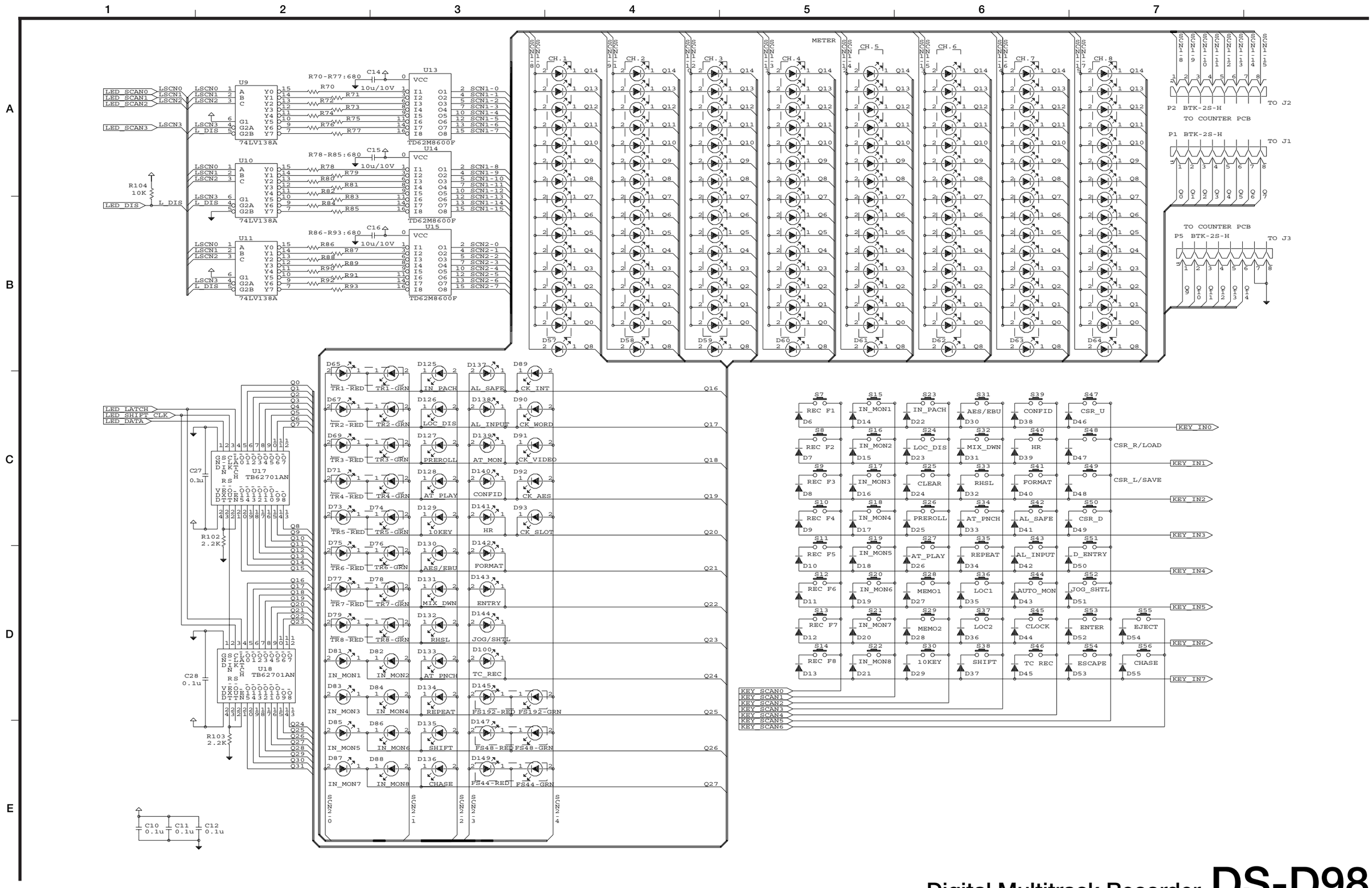


Digital Multitrack Recorder **DS-D98**

1 st Issue; October 2001



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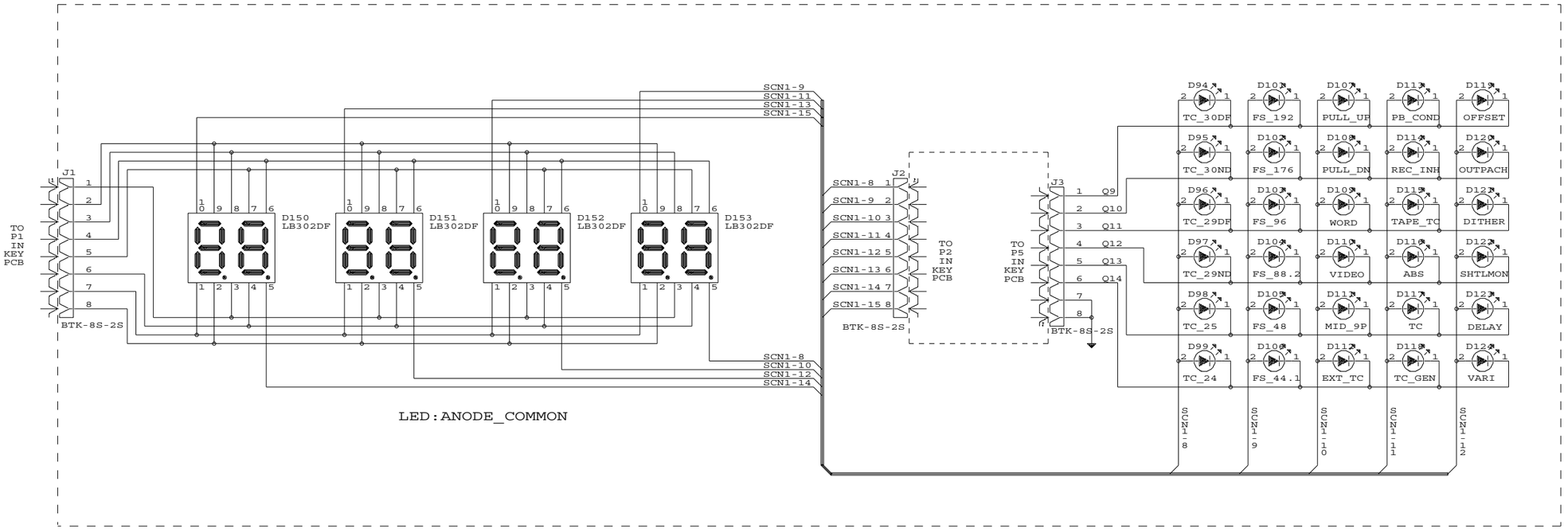
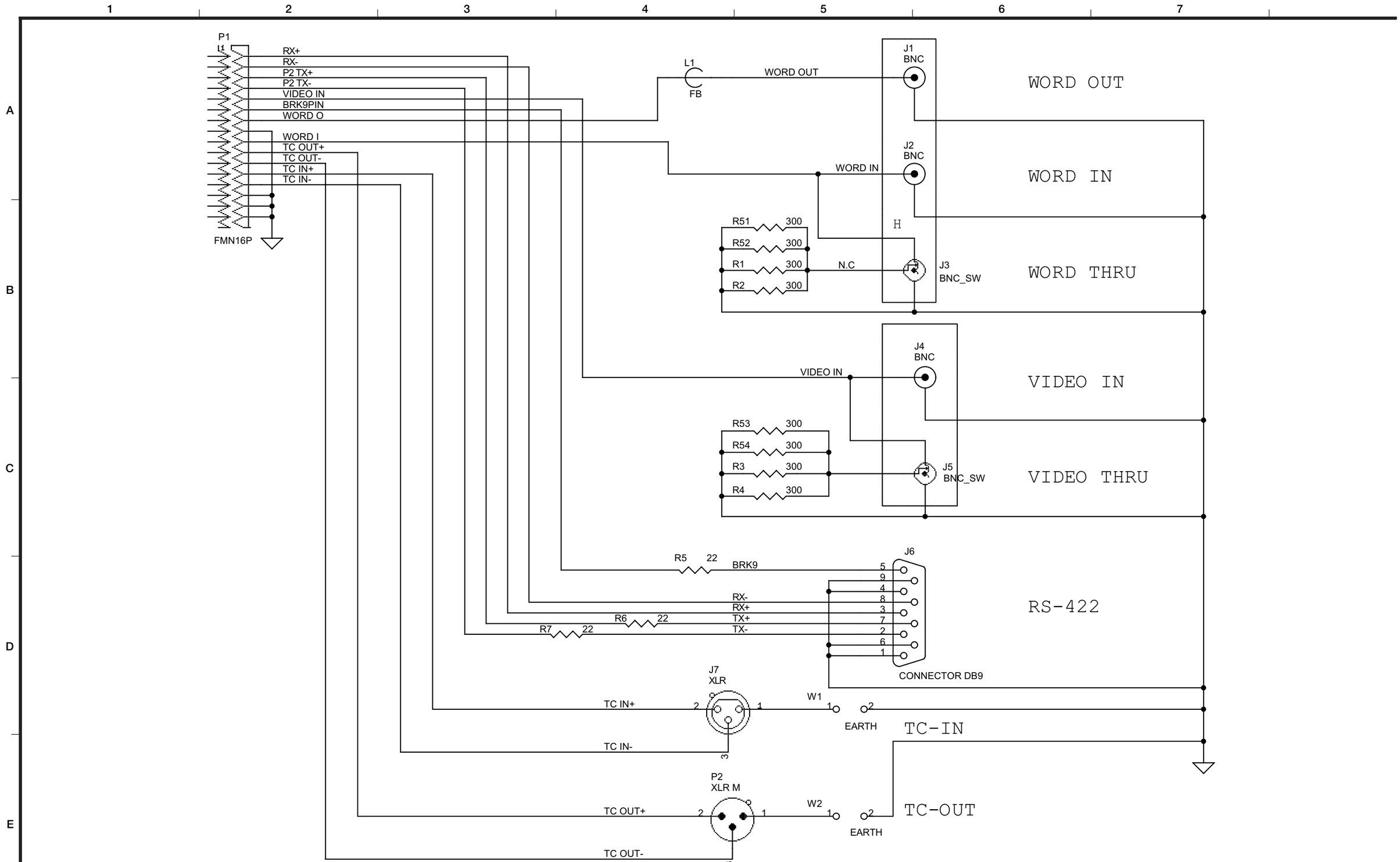
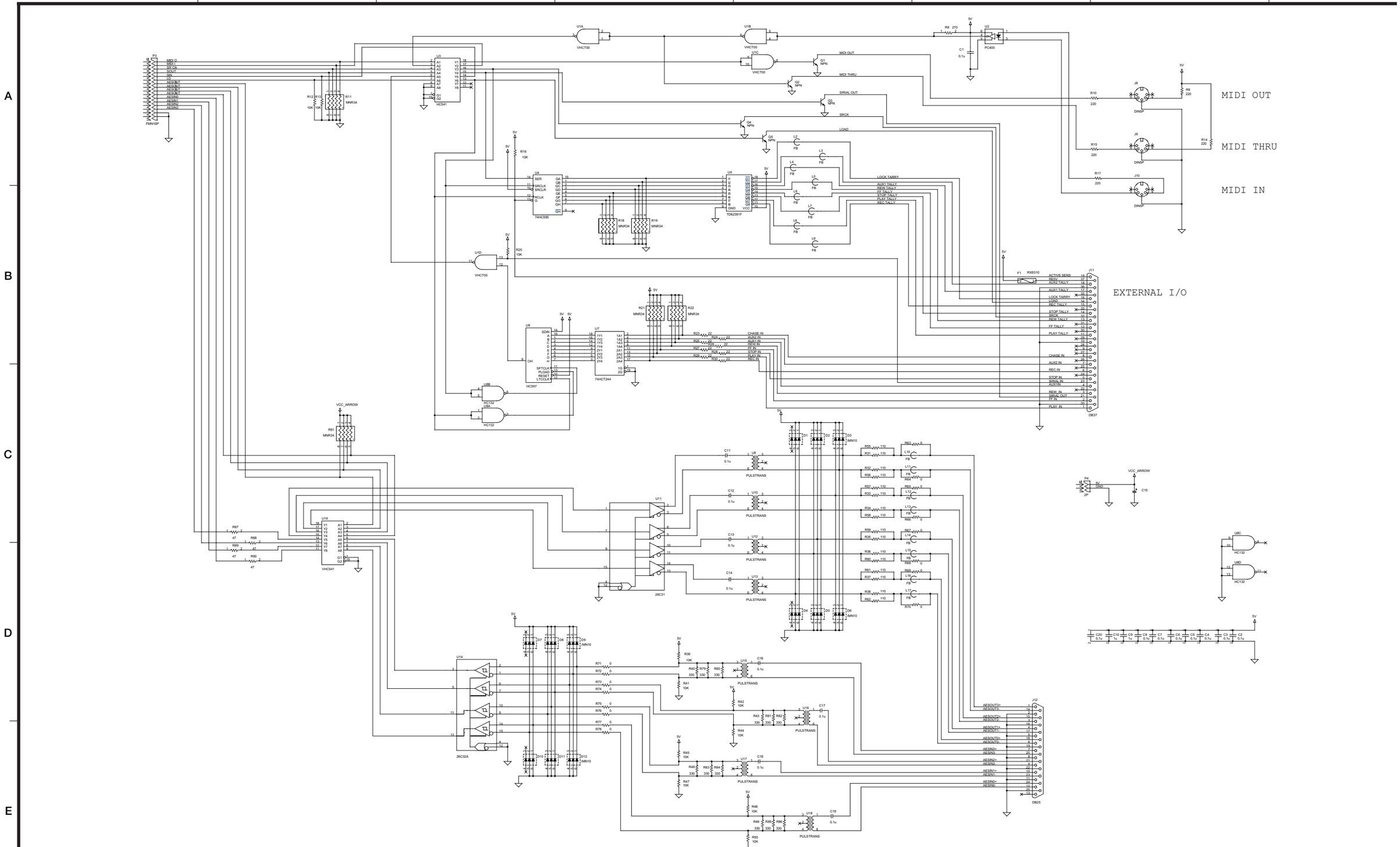

J1
TO P1 IN KEY PCB
BTK-8S-2S
D150 LB302DF
D151 LB302DF
D152 LB302DF
D153 LB302DF
SCN1-9
SCN1-11
SCN1-13
SCN1-15
SCN1-8
SCN1-10
SCN1-12
SCN1-14
LED:ANODE_COMMON
J2
TO P2 IN KEY PCB
J3
TO P5 IN KEY PCB
Q9
Q10
Q11
Q12
Q13
Q14
D94 TC_30DF
D10? FS_192
D10? PULL_UP
D11? PB_COND
D11? OFFSET
D95 TC_30ND
D10? FS_176
D10? PULL_DN
D11? REC_INH
D12? OUTPACH
D96 TC_29DF
D10? FS_96
D10? WORD
D11? TAPE_TC
D12? DITHER
D97 TC_29ND
D10? FS_88.2
D11? VIDEO
D11? ABS
D12? SHTLMON
D98 TC_25
D10? FS_48
D11? MID_9P
D11? TC
D12? DELAY
D99 TC_24
D10? FS_44.1
D11? EXT_TC
D11? TC_GEN
D12? VARI


1
2
3
4
5
6
7
A
B
C
D
E
P1
RX+
RX-
P2 TX+
P2 TX-
VIDEO IN
BRK9PIN
WORD O
WORD I
TC OUT+
TC OUT-
TC IN+
TC IN-
FMN16P
L1
FB
WORD OUT
J1
BNC
WORD OUT
WORD IN
J2
BNC
WORD IN
H
R51 300
R52 300
R1 300
R2 300
N.C
J3
BNC_SW
WORD THRU
J4
BNC
VIDEO IN
VIDEO IN
R53 300
R54 300
R3 300
R4 300
J5
BNC_SW
VIDEO THRU
J6
R5 22
BRK9
RX-
RX+
R6 22
TX+
R7 22
TX-
RS-422
CONNECTOR DB9
J7
XLR
TC IN+
TC IN-
W1
EARTH
TC-IN
P2
XLR M
TC OUT+
TC OUT-
W2
EARTH
TC-OUT



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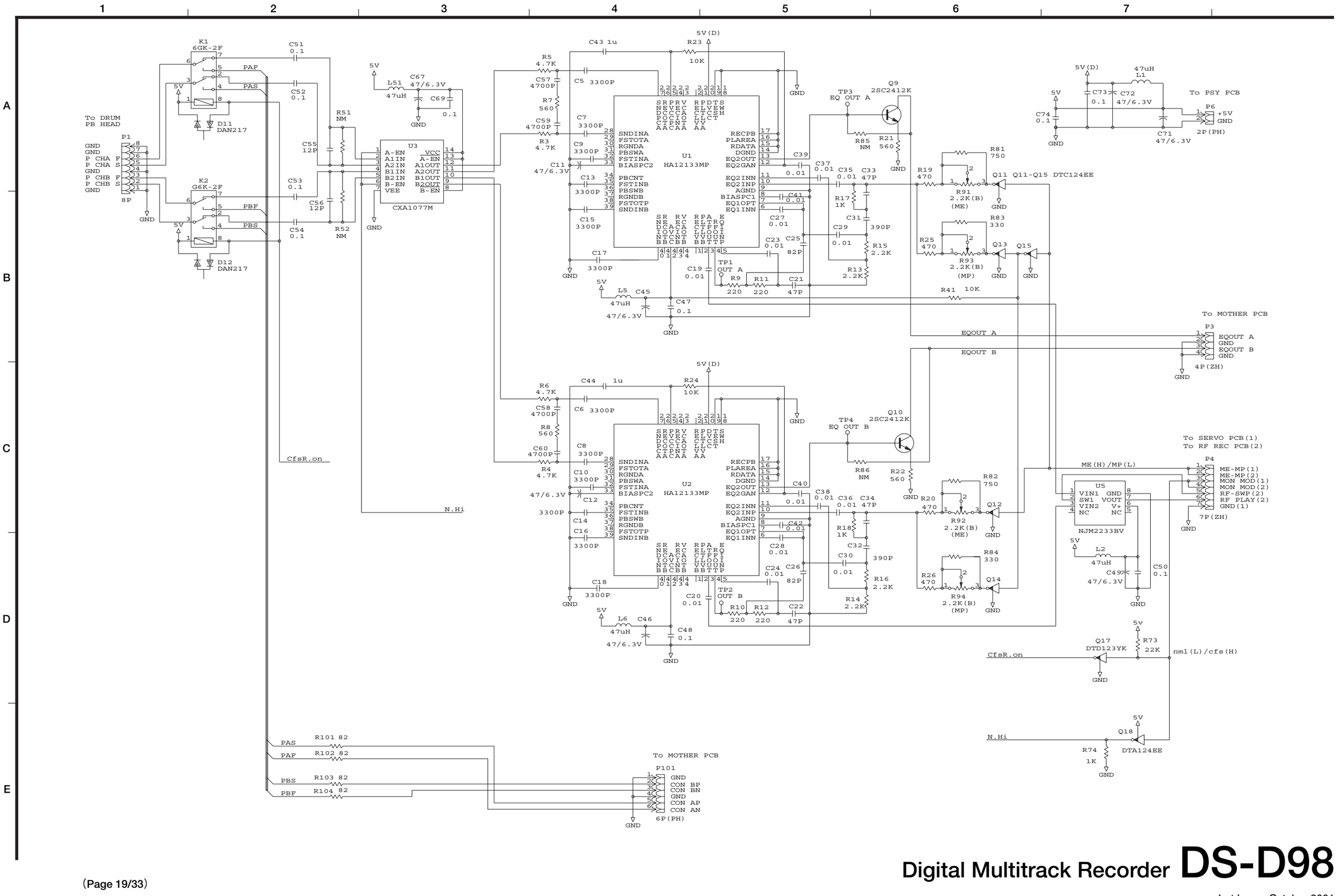

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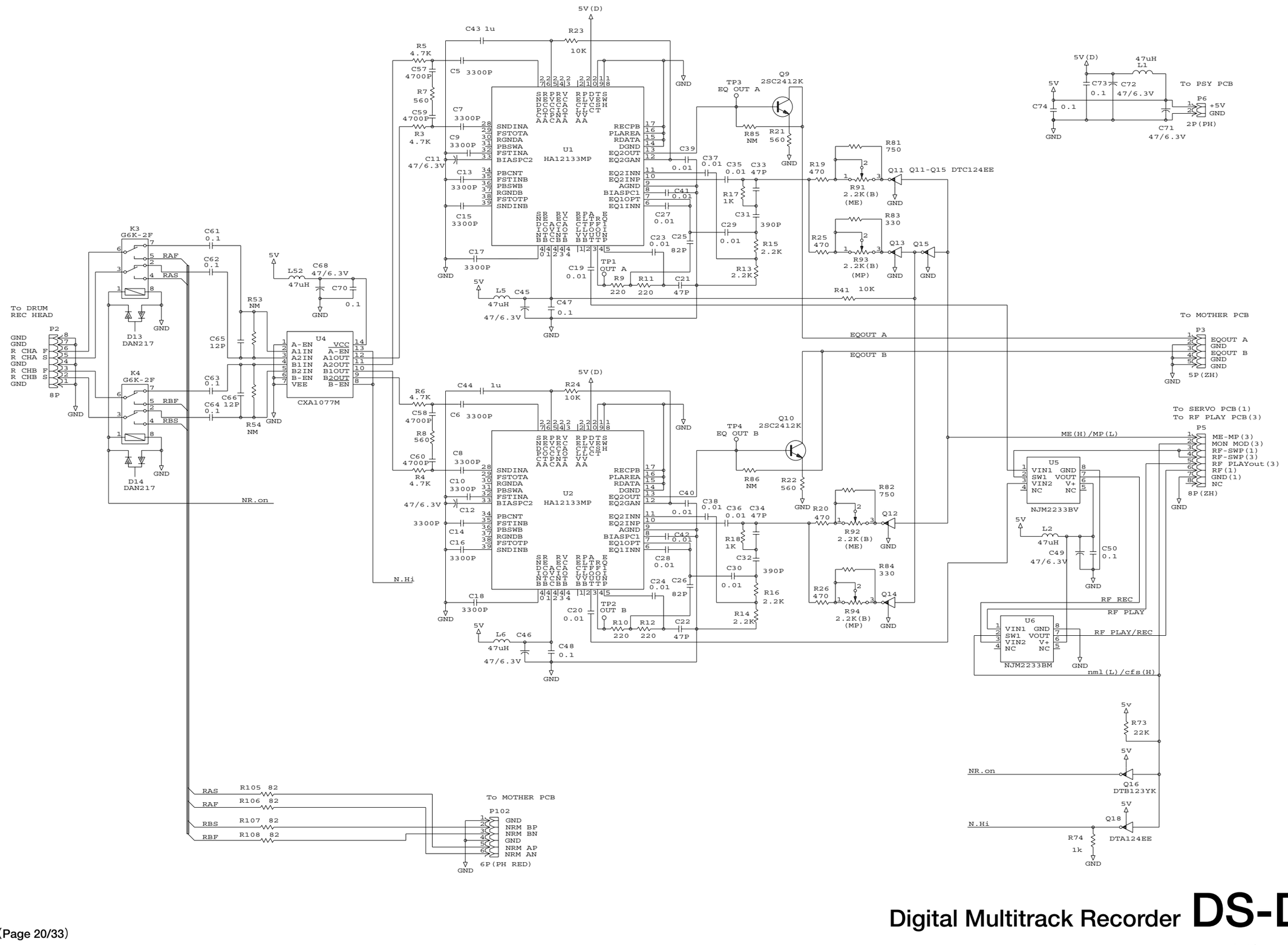
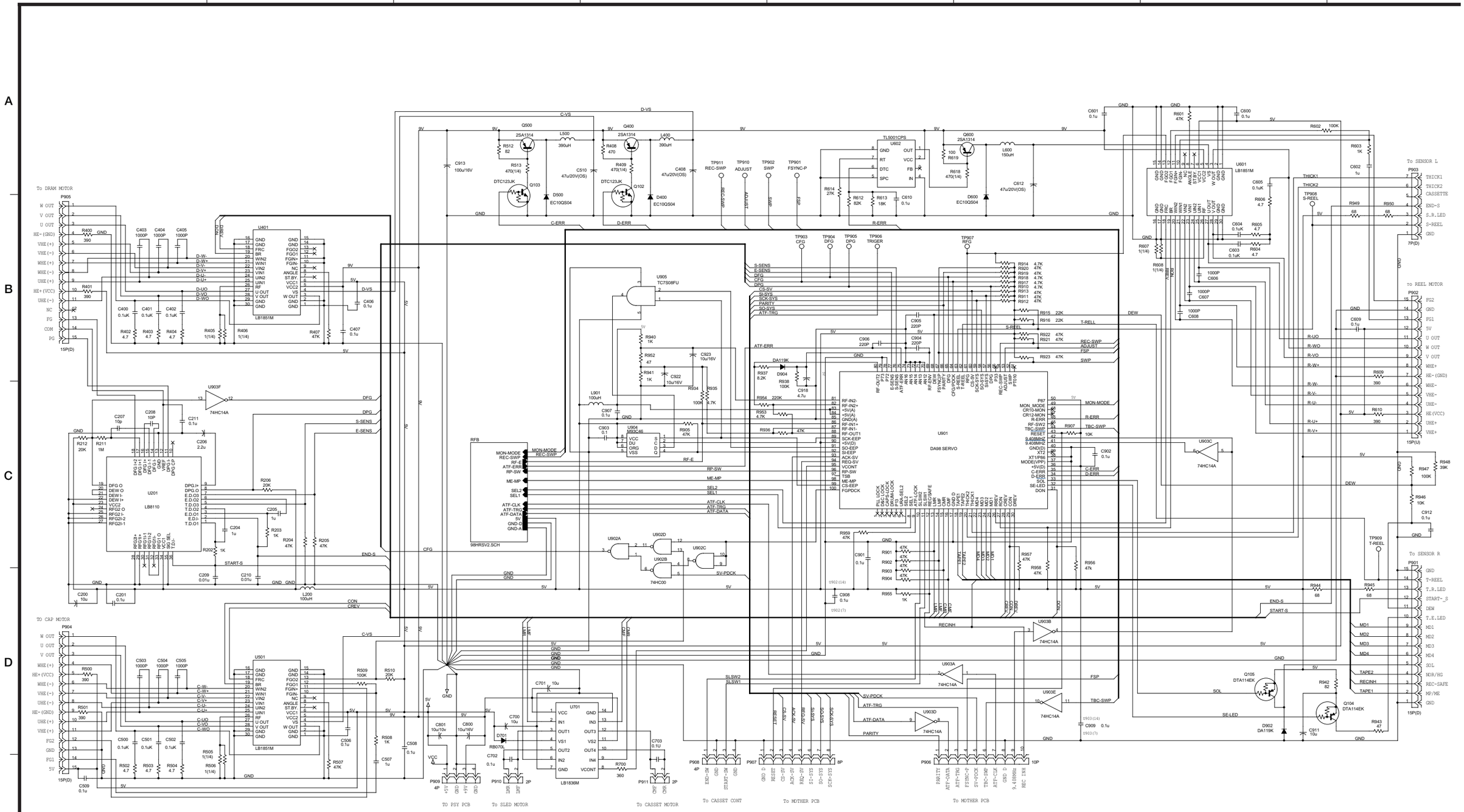
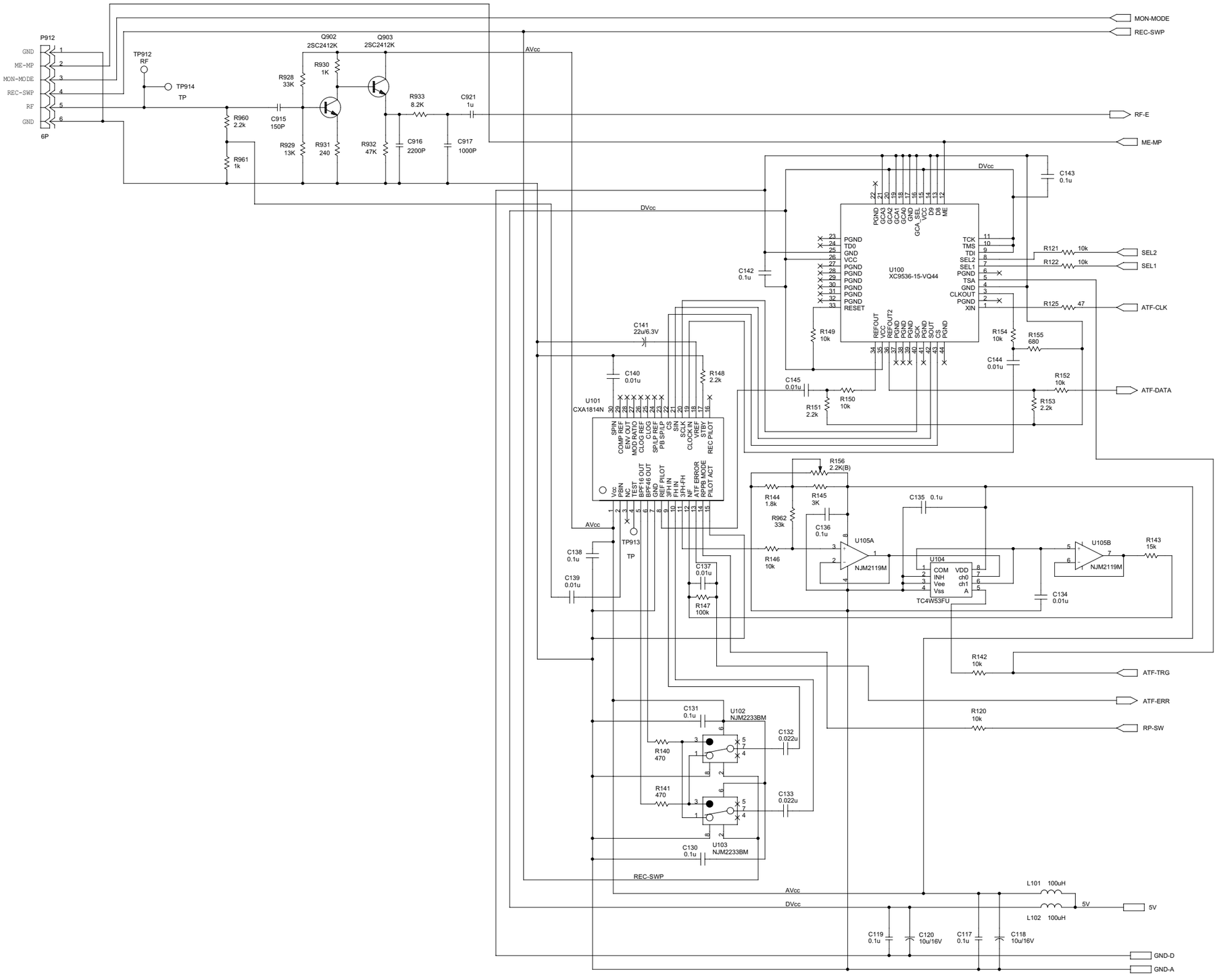
1 st Issue; October 2001

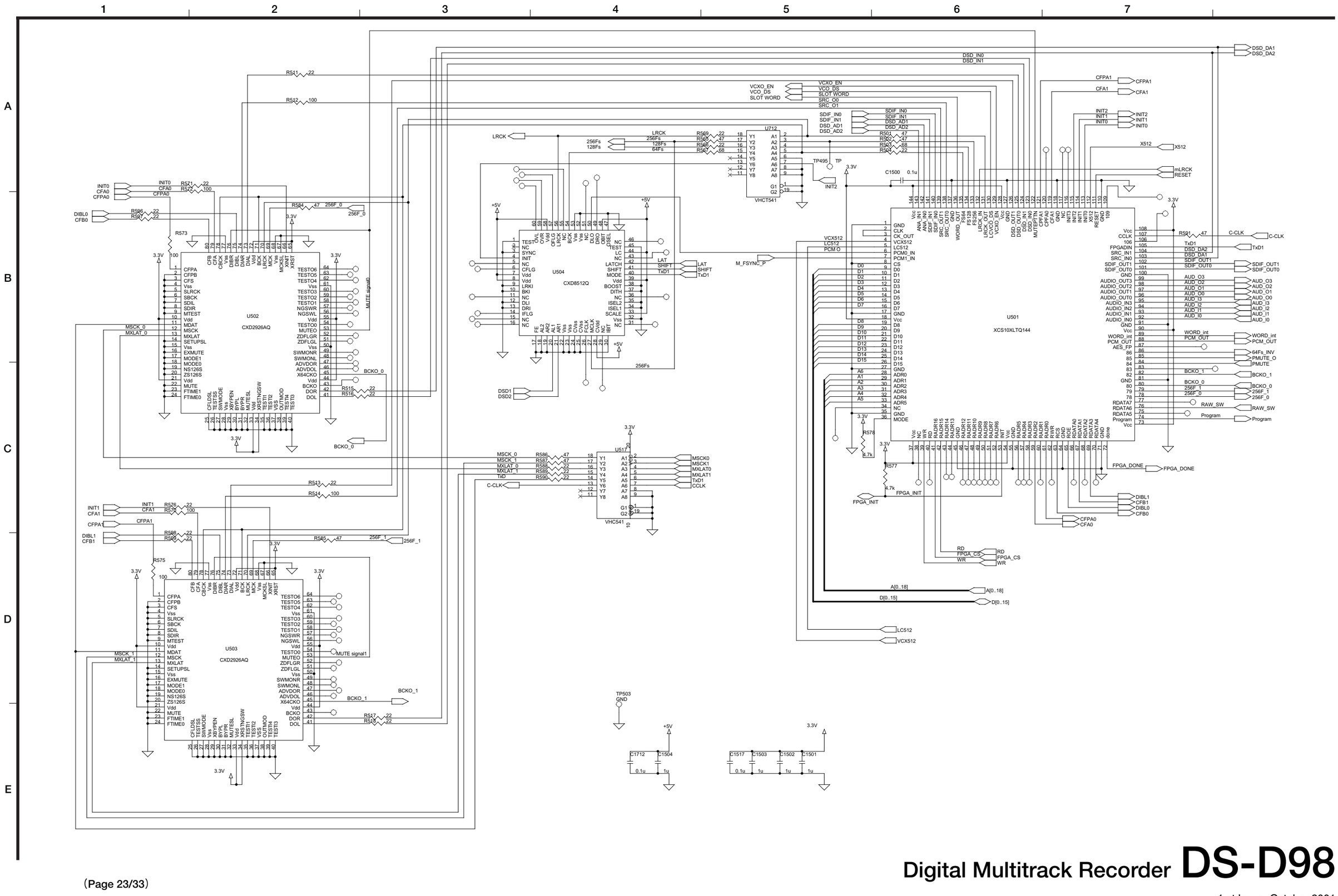

1
2
3
4
5
6
7
A
B
C
D
E
U1
HA12133MP
U2
HA12133MP
U4
CXA1077M
K3
G6K-2F
K4
G6K-2F
D13
DAN217
D14
DAN217
P2
8P
To DRUM
REC HEAD
GND
GND
R CHA F
R CHA S
GND
R CHB F
R CHB S
GND
RAF
RAS
RBF
RBS
NR.on
N.Hi
5V(D)
5V
GND
TP1
OUT A
TP2
OUT B
TP3
EQ OUT A
TP4
EQ OUT B
Q9
2SC2412K
Q10
2SC2412K
Q11 Q11-Q15 DTC124EE
Q12
Q13
Q14
Q15
Q16
DTB123YK
Q18
DTA124EE
EQOUT A
EQOUT B
To MOTHER PCB
P3
5P(ZH)
To PSY PCB
P6
2P(PH)
To SERVO PCB(1)
To RF PLAY PCB(3)
P5
ME-MP(3)
MON MOD(3)
RF-SWP(1)
RF-SWP(3)
RF PLAYout(3)
RF(1)
GND(1)
NC
8P(ZH)
ME(H)/MP(L)
U5
NJM2233BV
U6
NJM2233BM
RF REC
RF PLAY
RF PLAY/REC
nml(L)/cfs(H)
To MOTHER PCB
P102
6P(PH RED)
NRM BP
NRM BN
NRM AP
NRM AN
R5 4.7K
R6 4.7K
R3 4.7K
R4 4.7K
R7 560
R8 560
R23 10K
R24 10K
R85 NM
R86 NM
R21 560
R22 560
R81 750
R82 750
R83 330
R84 330
R91 2.2K(B) (ME)
R92 2.2K(B) (ME)
R93 2.2K(B) (MP)
R94 2.2K(B) (MP)
R19 470
R20 470
R25 470
R26 470
R17 1K
R18 1K
R15 2.2K
R16 2.2K
R13 2.2K
R14 2.2K
R9 220
R10 220
R11 220
R12 220
R41 10K
R53 NM
R54 NM
R73 22K
R74 1k
R105 82
R106 82
R107 82
R108 82
C5 3300P
C6 3300P
C7 3300P
C8 3300P
C9 3300P
C10 3300P
C12 3300P
C13 3300P
C14 3300P
C15 3300P
C16 3300P
C17 3300P
C18 3300P
C11 47/6.3V
C43 1u
C44 1u
C57 4700P
C58 4700P
C59 4700P
C60 4700P
C61 0.1
C62 0.1
C63 0.1
C64 12P 0.1
C65 12P
C66
C68 47/6.3V
C70 0.1
C45 47/6.3V
C46 47/6.3V
C47 0.1
C48 0.1
C19 0.01
C20 0.01
C21 47P
C22 47P
C23 0.01
C24 0.01
C25 82P
C26 82P
C27 0.01
C28 0.01
C29 0.01
C30 0.01
C31 390P
C32 390P
C33 47P
C34 47P
C35 0.01
C36 0.01
C37 0.01
C38 0.01
C39 0.01
C40 0.01
C41 0.01
C42 0.01
L52 47uH
L5 47uH
L6 47uH
L1 47uH
L2 47uH
C73 0.1
C72 47/6.3V
C71 47/6.3V
C74 0.1
C49 47/6.3V
C50 0.1



Digital Multitrack Recorder **DS-D98**

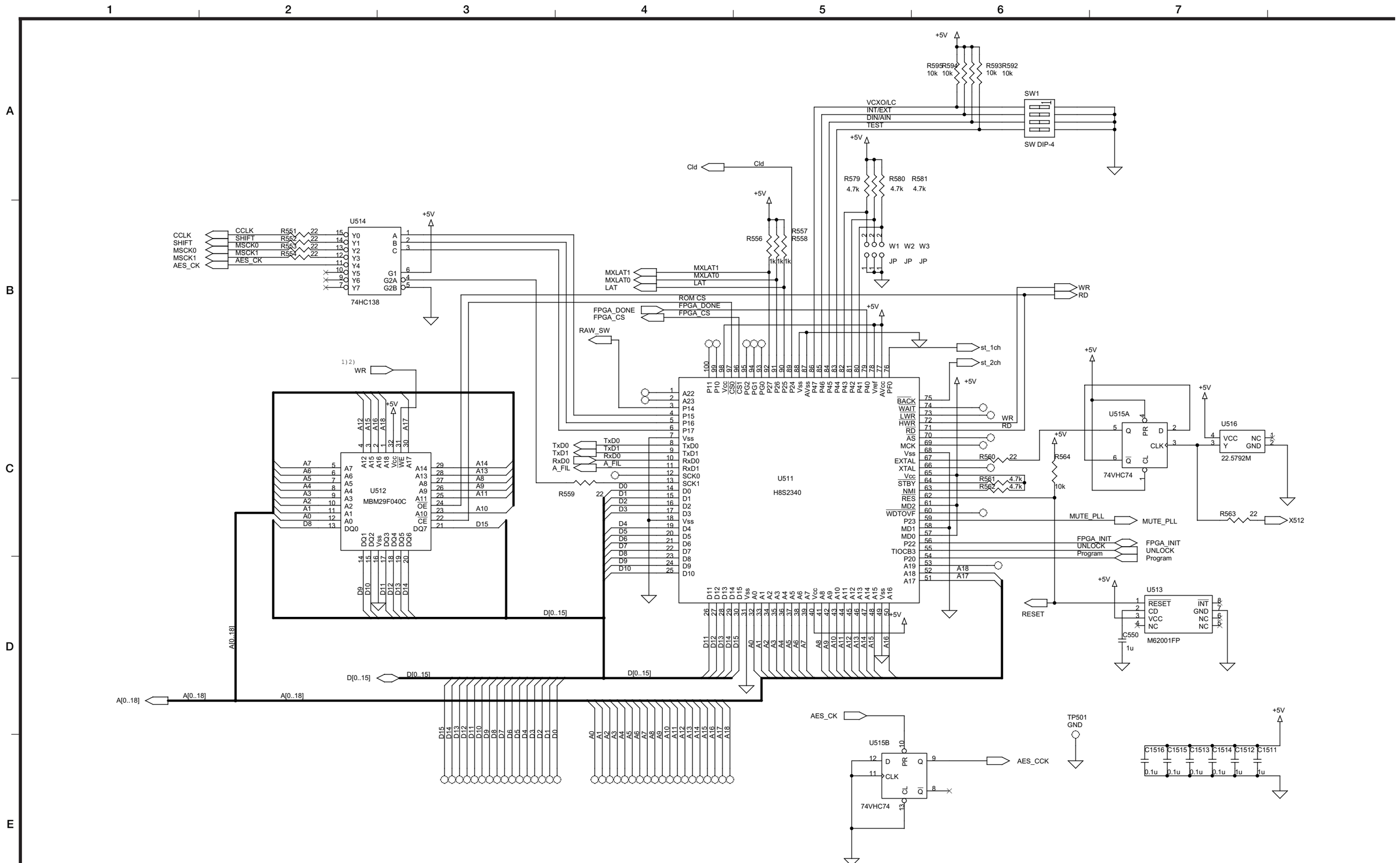
1 st Issue; October 2001


P912
GND
ME-MP
MON-MODE
REC-SWP
RF
GND
6P
TP912
RF
TP914
TP
Q902
2SC2412K
Q903
2SC2412K
R928
33K
R930
1K
R933
8.2K
C921
1u
R960
2.2k
C915
150P
R929
13K
R931
240
R932
47K
C916
2200P
C917
1000P
R961
1k
AVcc
DVcc
MON-MODE
REC-SWP
RF-E
ME-MP
U100
XC9536-15-VQ44
C142
0.1u
C143
0.1u
R149
10k
R121
10k
R122
10k
SEL2
SEL1
R125
47
ATF-CLK
R154
10k
R155
680
C144
0.01u
C145
0.01u
R151
2.2k
R150
10k
R152
10k
R153
2.2k
ATF-DATA
C141
22u/6.3V
C140
0.01u
R148
2.2k
U101
CXA1814N
R156
2.2K(B)
R144
1.8k
R145
3K
R962
33k
C136
0.1u
C135
0.1u
U105A
NJM2119M
U104
TC4W53FU
U105B
NJM2119M
R143
15k
C134
0.01u
R146
10k
TP913
TP
C138
0.1u
C139
0.01u
C137
0.01u
R147
100k
R142
10k
ATF-TRG
ATF-ERR
R120
10k
RP-SW
C131
0.1u
U102
NJM2233BM
C132
0.022u
R140
470
R141
470
C133
0.022u
C130
0.1u
U103
NJM2233BM
REC-SWP
L101
100uH
L102
100uH
5V
C119
0.1u
C120
10u/16V
C117
0.1u
C118
10u/16V
GND-D
GND-A



Digital Multitrack Recorder DS-D98

1 st Issue; October 2001



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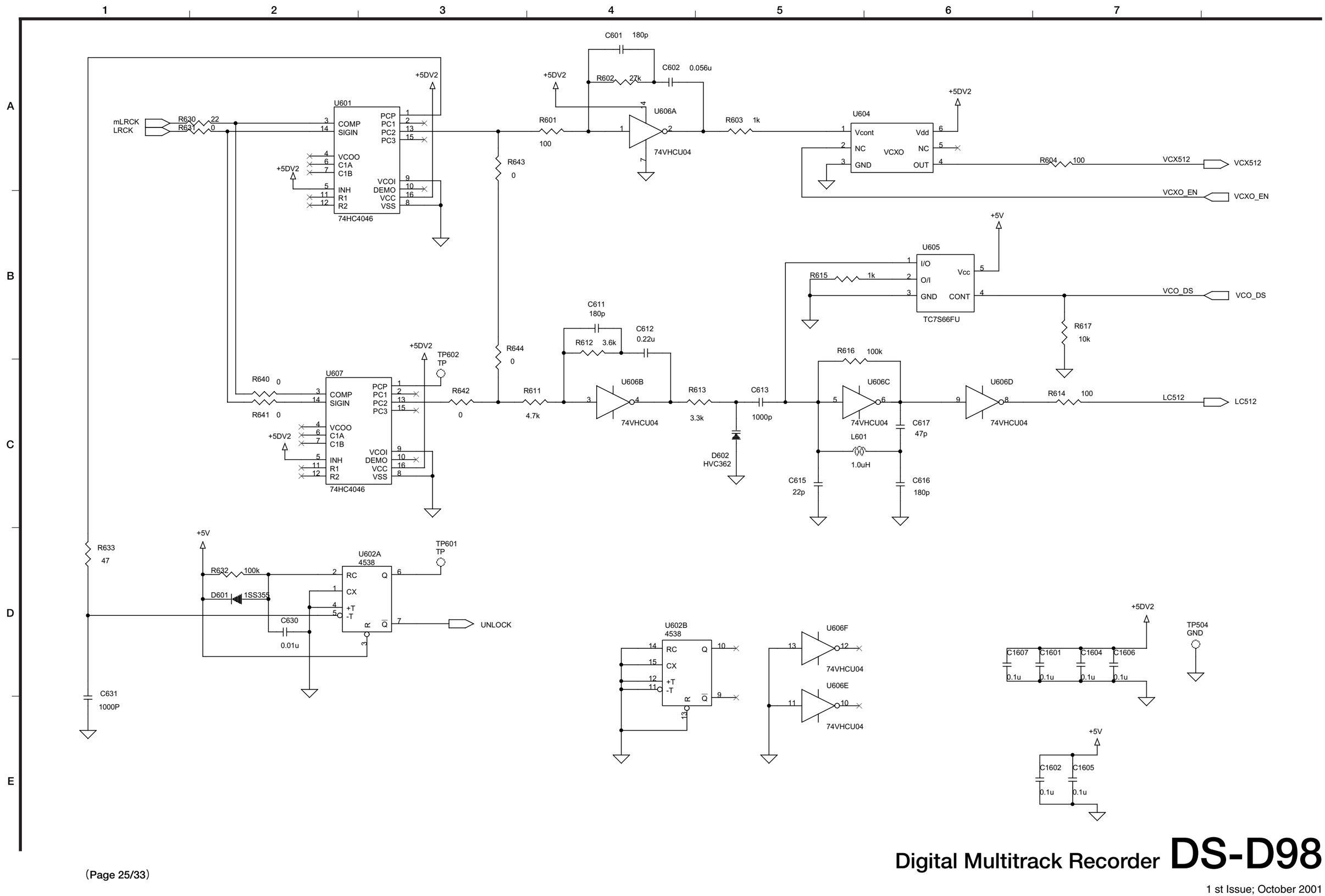
1 st Issue; October 2001



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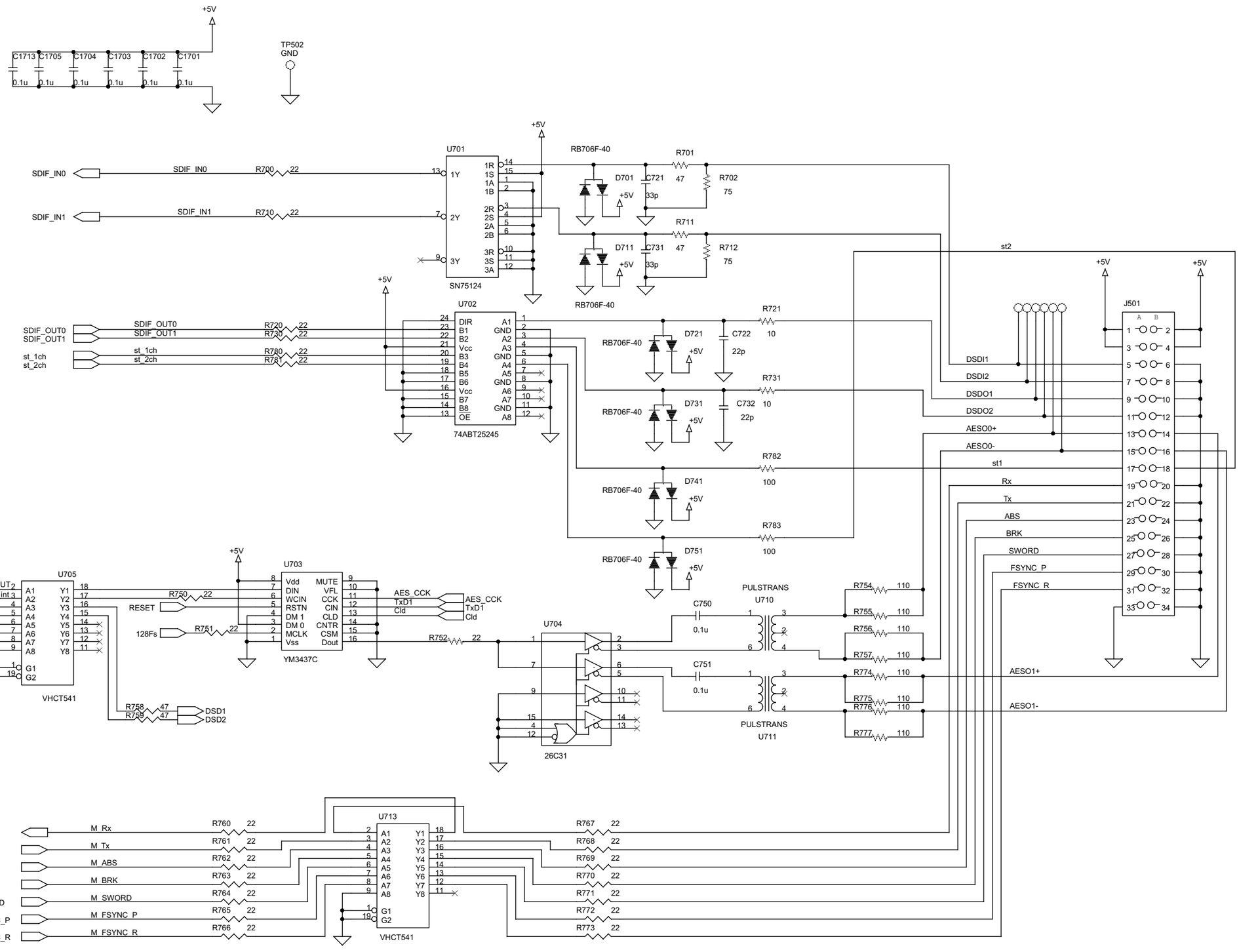
1 st Issue; October 2001



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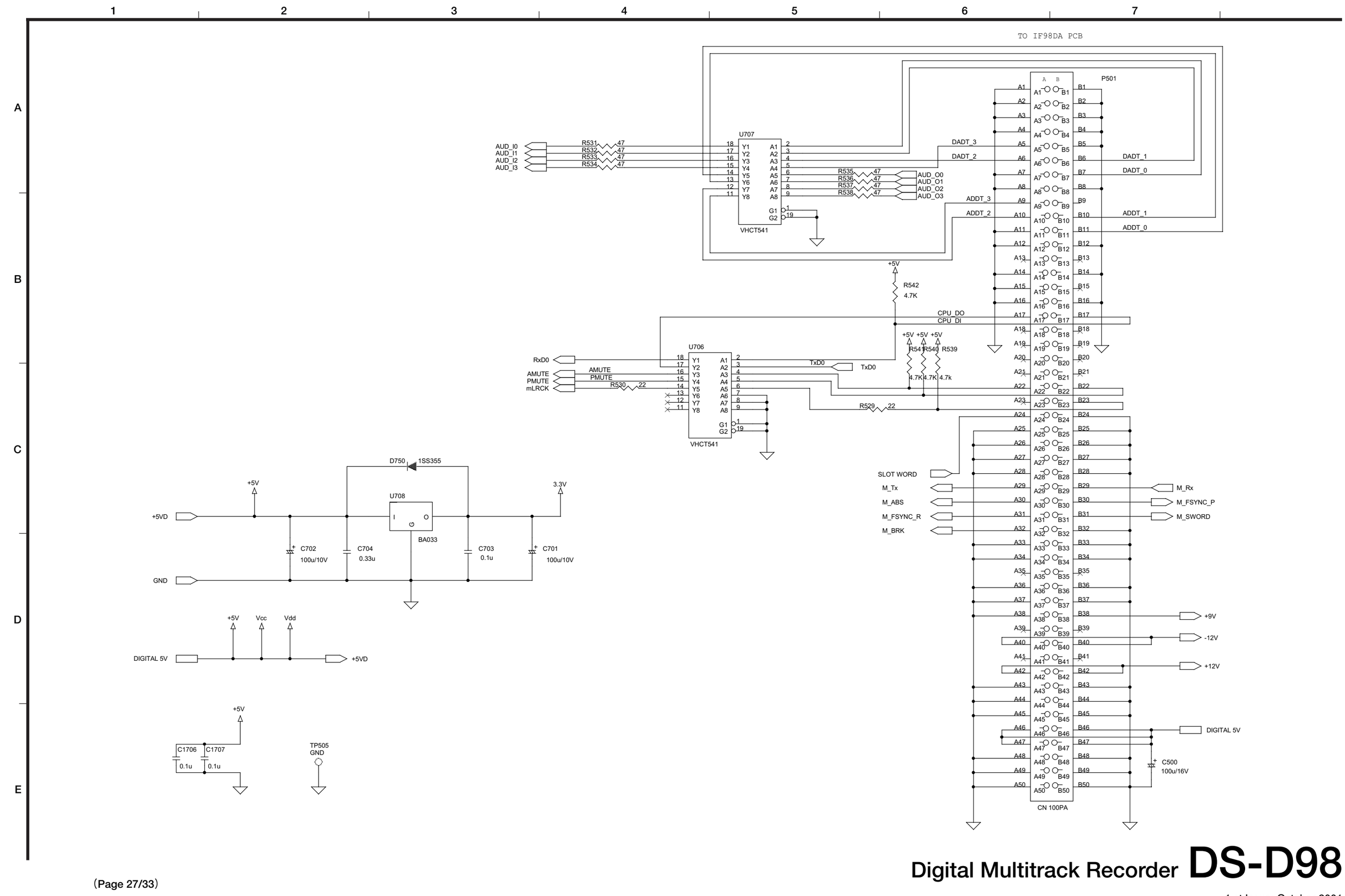
1 st Issue; October 2001



Digital Multitrack Recorder **DS-D98**

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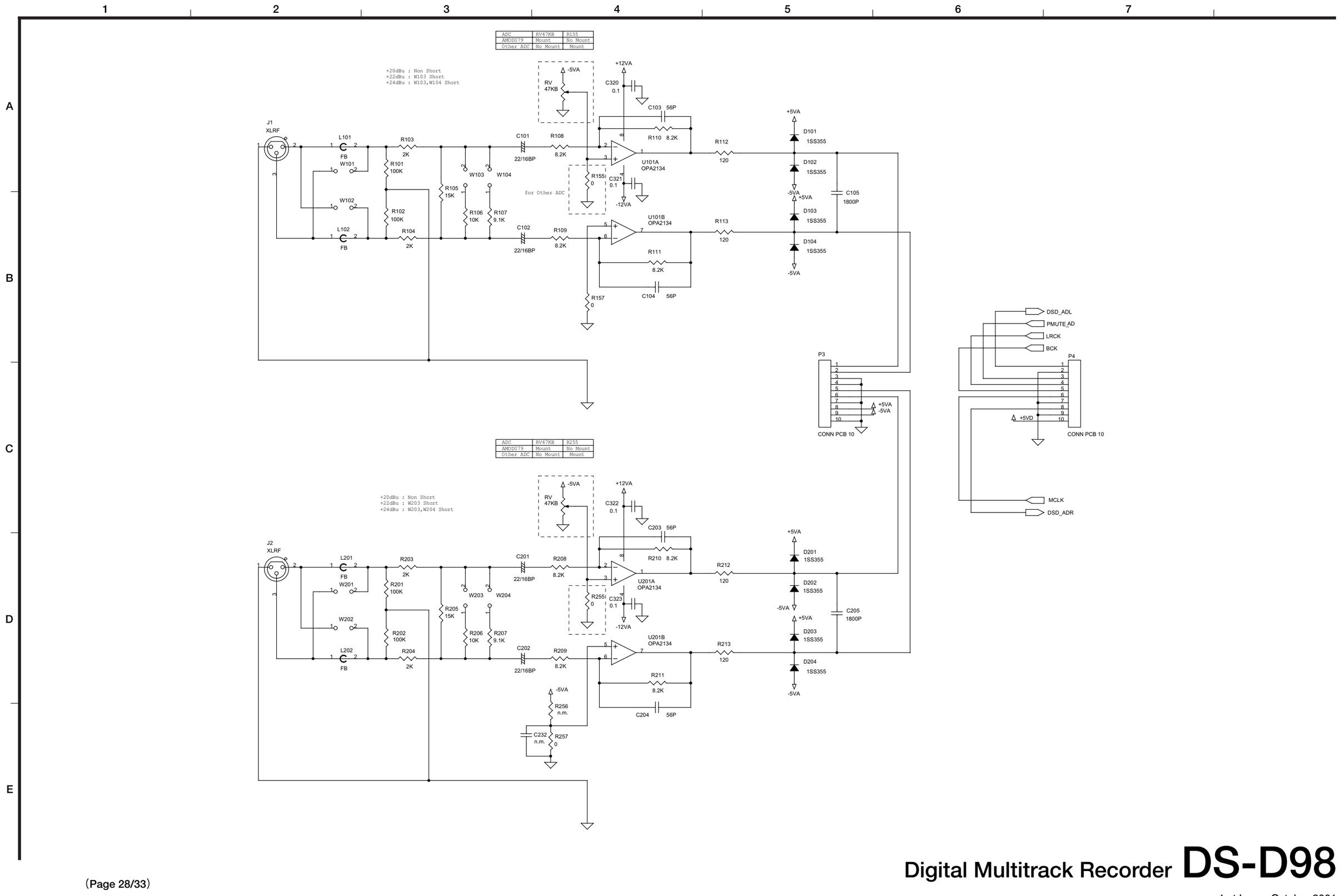

Digital Multitrack Recorder DS-D98
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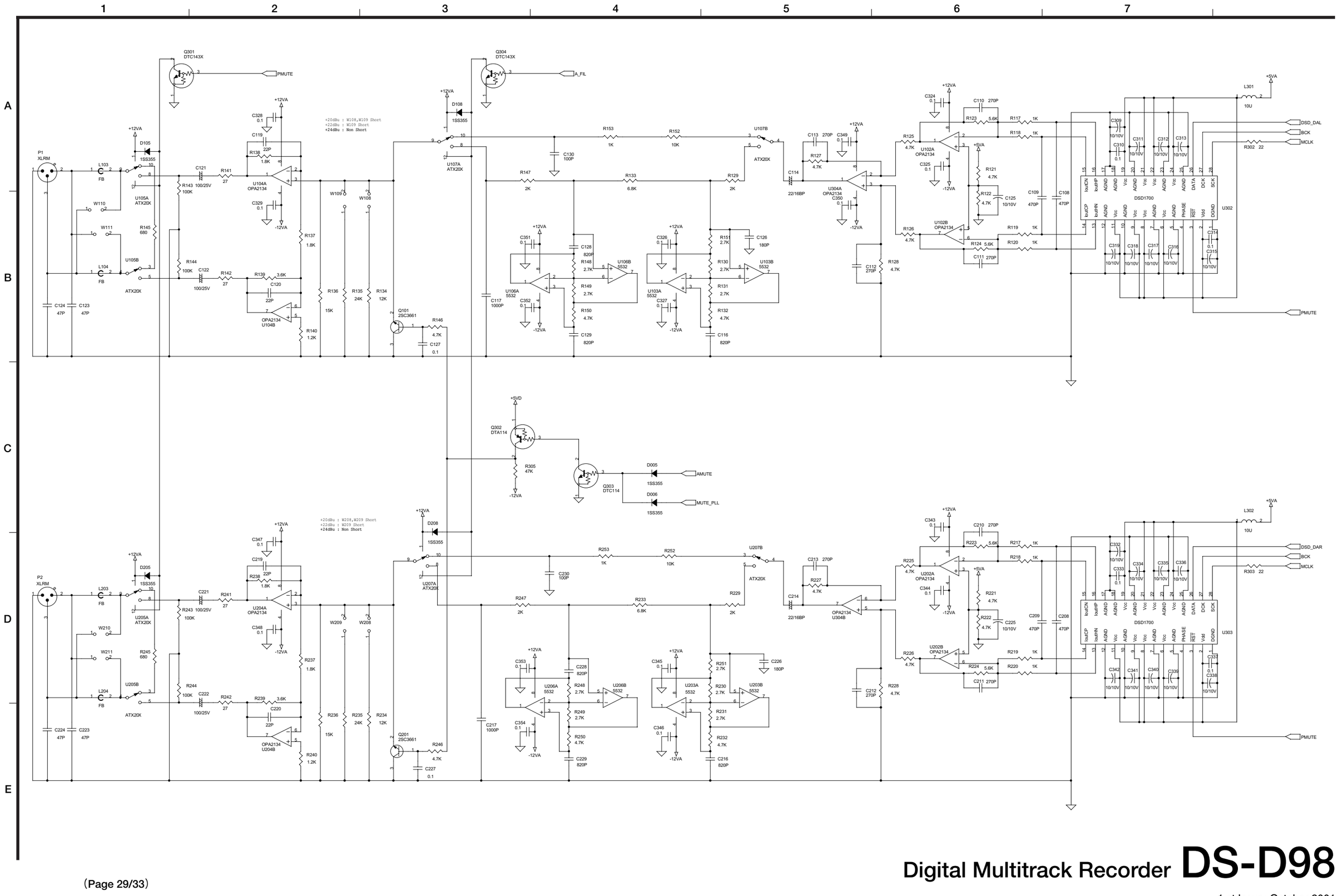
SCHEMATIC DIAGRAM DS-D98 DSD PCB (7/8)



Digital Multitrack Recorder **DS-D98**

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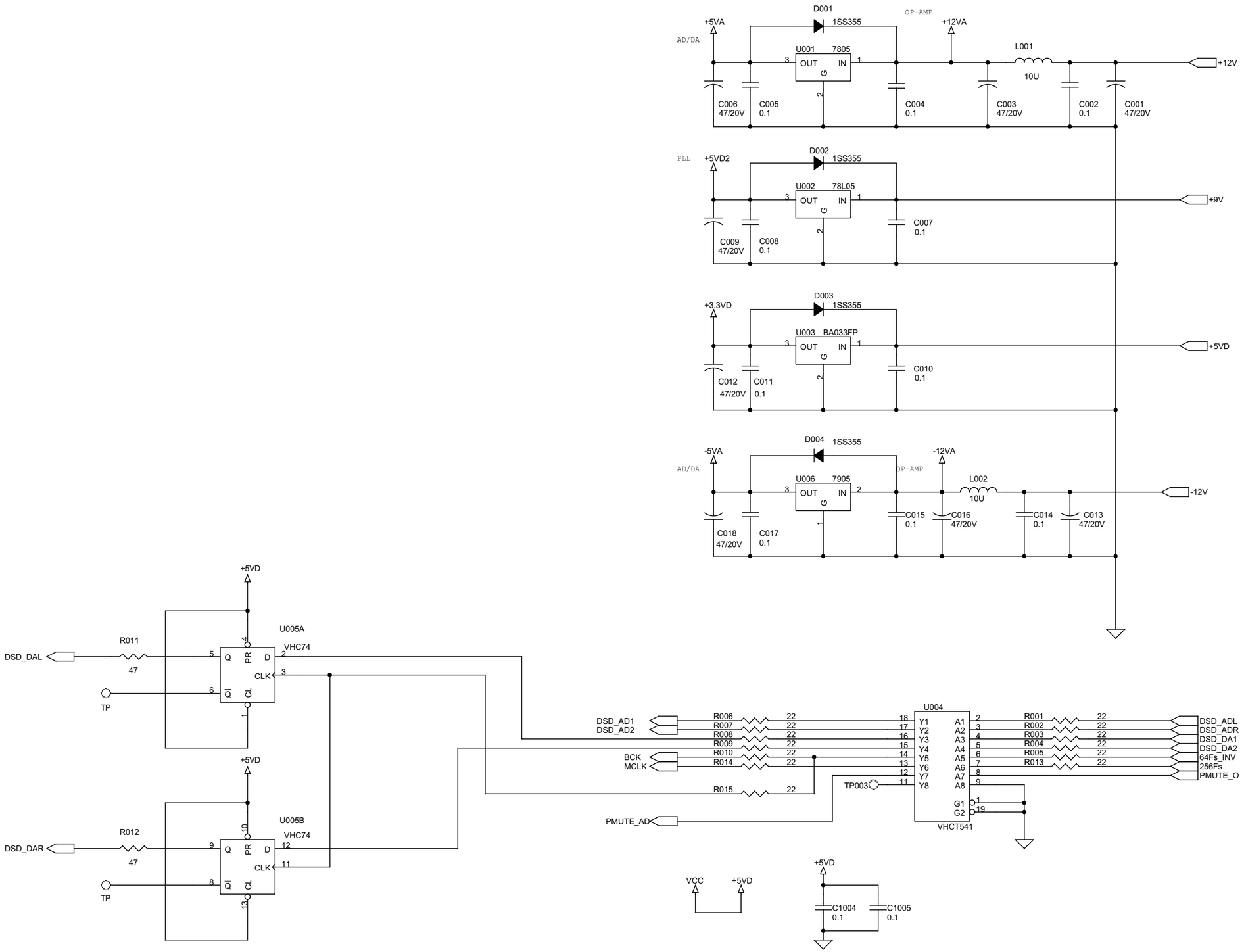
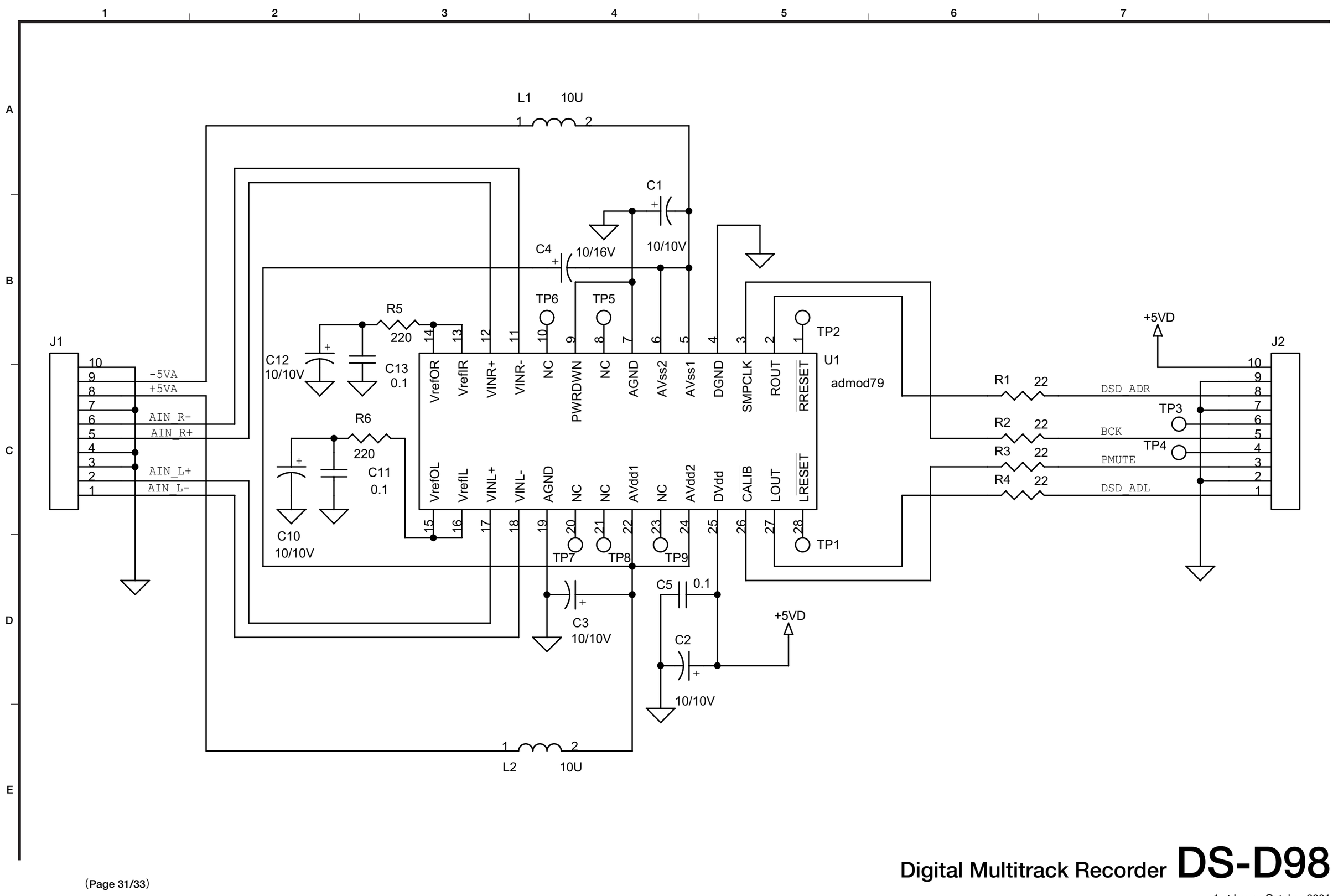
1 2 3 4 5 6 7

A B C D E



Digital Multitrack Recorder **DS-D98**

1 st Issue; October 2001



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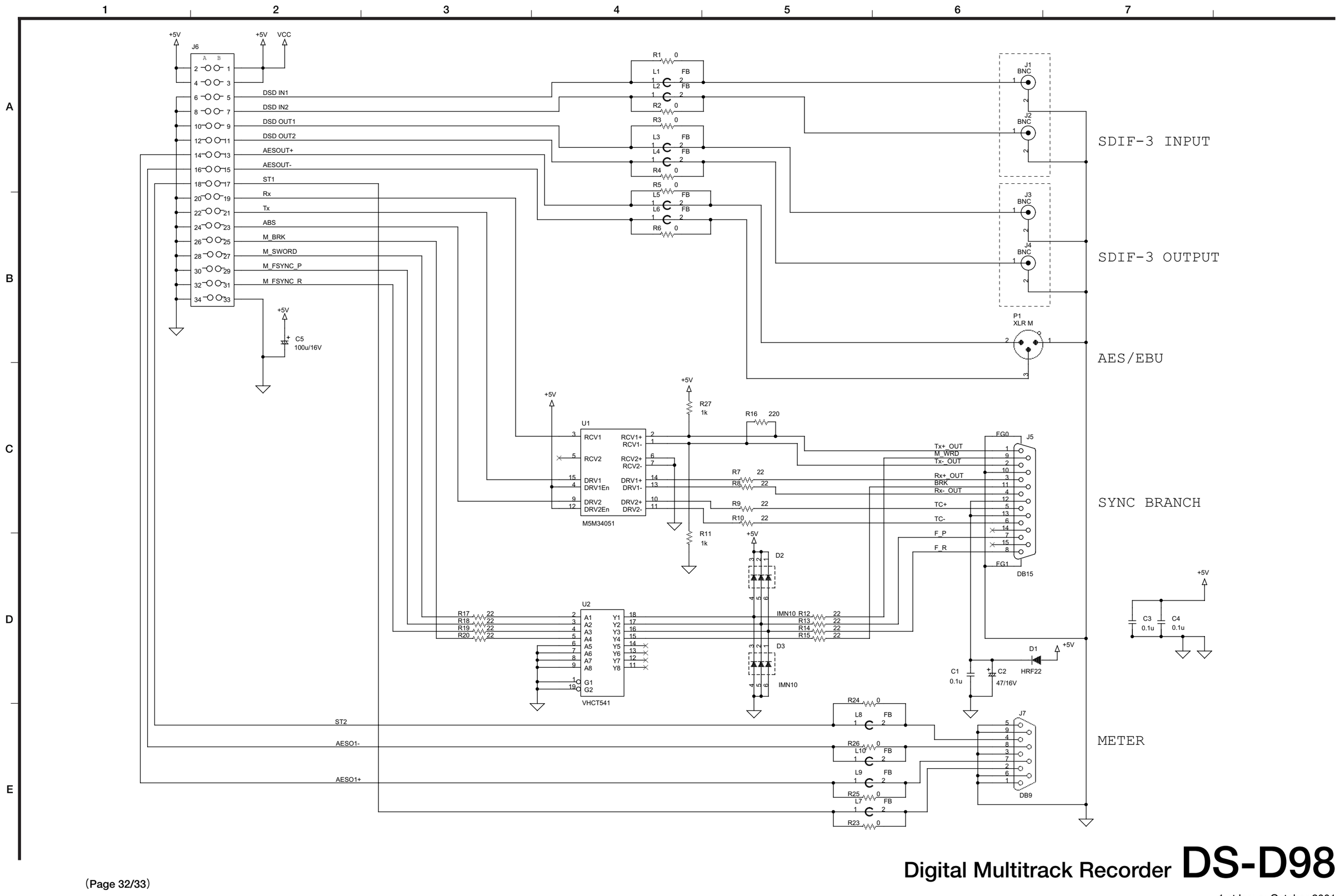
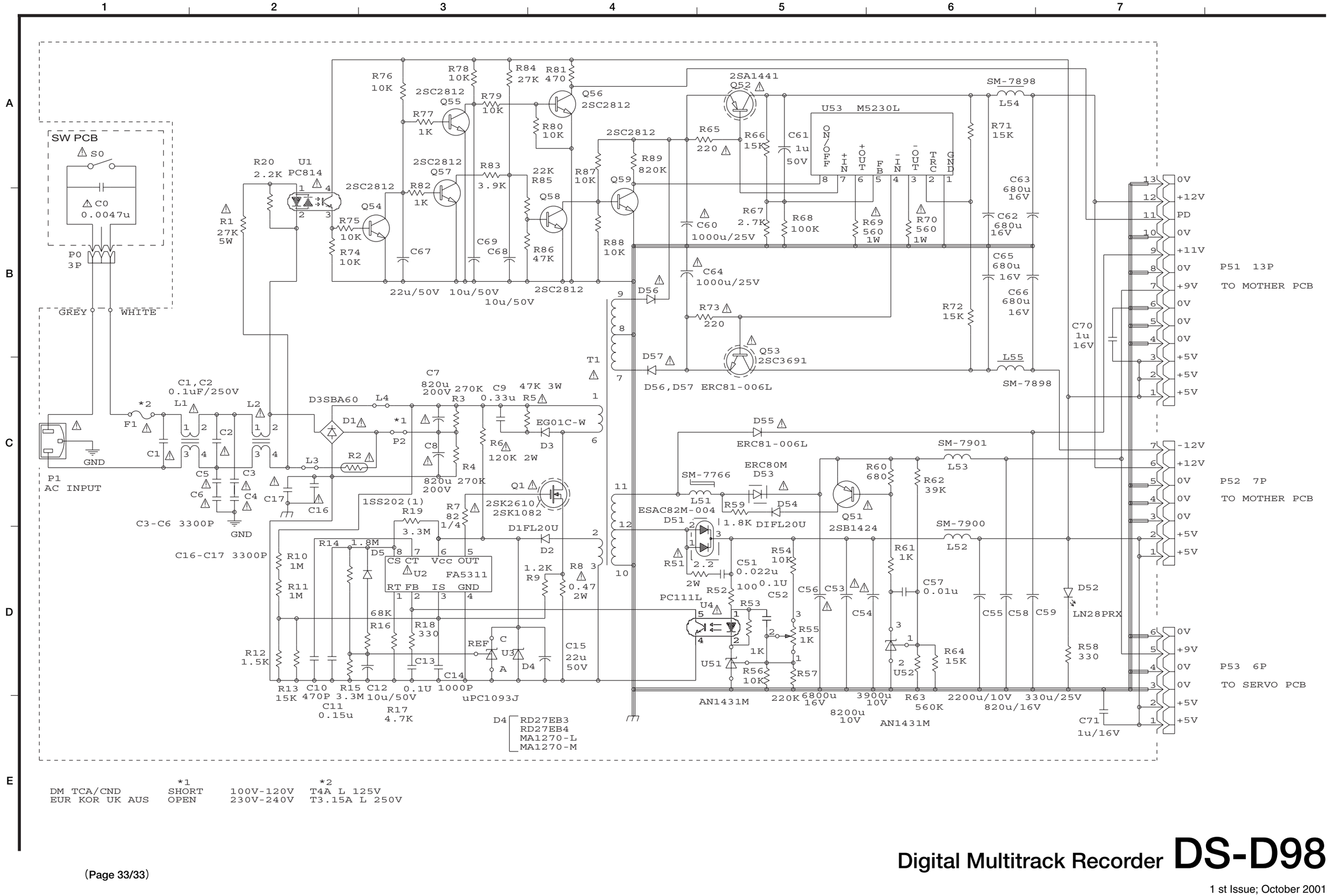
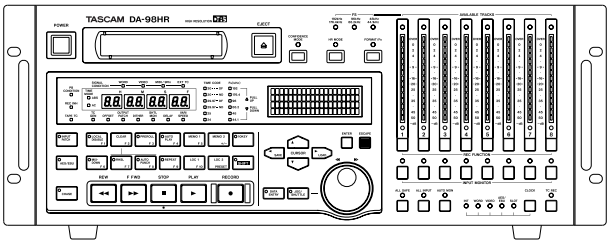

1
2
3
4
5
6
7
A
B
C
D
E
J6
DSD IN1
DSD IN2
DSD OUT1
DSD OUT2
AESOUT+
AESOUT-
ST1
Rx
Tx
ABS
M_BRK
M_SWORD
M_FSYNC_P
M_FSYNC_R
+5V
VCC
C5
100u/16V
R1
R2
R3
R4
R5
R6
L1
L2
L3
L4
L5
L6
FB
J1
J2
J3
J4
BNC
SDIF-3 INPUT
SDIF-3 OUTPUT
P1
XLR M
AES/EBU
U1
M5M34051
RCV1
RCV2
DRV1
DRV1En
DRV2
DRV2En
RCV1+
RCV1-
RCV2+
RCV2-
DRV1+
DRV1-
DRV2+
DRV2-
R27
1k
R16
220
R7
R8
R9
R10
22
R11
1k
U2
VHCT541
A1
A2
A3
A4
A5
A6
A7
A8
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
G1
G2
R17
R18
R19
R20
R12
R13
R14
R15
IMN10
D2
D3
IMN10
J5
DB15
Tx+ OUT
M_WRD
Tx- OUT
Rx+ OUT
BRK
Rx- OUT
TC+
TC-
F_P
F_R
FG0
FG1
SYNC BRANCH
C3
C4
0.1u
D1
HRF22
C1
0.1u
C2
47/16V
R24
R26
R25
R23
L8
L10
L9
L7
J7
DB9
ST2
AESO1-
AESO1+
METER

SCHEMATIC DIAGRAM DS-D98 POWER SUPPLY SECTION



	*1	*2
DM TCA/CND	SHORT	T4A L 125V
EUR KOR UK AUS	OPEN	T3.15A L 250V

Digital Multitrack Recorder DS-D98
1 st Issue; October 2001



TASCAM
TEAC Professional Division

SERVICE MANUAL

DA-98HR

Digital Multitrack Recorder

INSTRUCTIONS FOR SERVICE PERSONNEL

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

Effective : October, 2000 4A3489

S-0029

CONTENTS

1. SPECIFICATIONS ····· 3
2. TECHNICAL INFORMATION ····· 7
2-1. Activation of test mode ····· 7
2-2. Activation of VTR mode ····· 7
2-3. Displaying ROM version numbers ····· 7
2-4. Displaying SUB MPU version numbers ····· 7
2-5. Displaying the voltage of battery ····· 7
2-6. Displaying the hed drum utilized time ····· 7
2-7. Displaying the servo error history ····· 7
2-8. KEY PCB check mode ····· 8
2-9. How to use the built-in oscillator ····· 8
2-10. Removing the FRONT MPU ····· 8
2-11. Removing the SYS ROM ····· 8
2-12. Checking the optional IF-AN98HR (A/D board and D/A board) ····· 9
2-13. Changeover of Reference level ····· 9
2-14. EXTERNAL CONTROL I/O ····· 12
3. ASSEMBLING THE MECHANISM ASS'Y ····· 19
3-1. Flowchart of assembling ····· 19
3-2. Installation of the mechanical parts ····· 20
4. MECHANISM ADJUSTMENTS ····· 26
4-1. Preparation ····· 27
4-2. Test tape ····· 27
4-3. Adjusting the tension arm position ····· 28
4-4. Adjusting the torque ····· 28
4-5. Adjusting the tape travel ····· 29
4-6. Confirming the travel in F.FWD, REW and REV mode ····· 32
5. ELECTRICAL ADJUSTMENTS ····· 35
5-1. Check and adjustment points ····· 35
5-2. Test tape ····· 36
5-3. +5 V supply check ····· 36
5-4. P.G. (Phase generator) position adjustment ····· 36
5-5. Offset adjustment in the VCO free-running frequency automatic compensation circuit ····· 37
5-6. Playback equalizer adjustment ····· 38
5-7. RF level check ····· 39
5-8. Playback error rate check ····· 40
5-9. Recording current adjustment ····· 41
5-10. Recording/playback RF level check ····· 43
5-11. Recording/playback error rate check ····· 43
6. EXPLODED VIEWS AND PARTS LIST ····· 45
7. PC BOARDS AND PARTS LIST ····· 53
8. INCLUDED ACCESSORIES ····· 71

目 次

1. 仕様 ····· 3
2. テクニカルインフォメーション ····· 7
2-1. テストモードの起動 ····· 7
2-2. VTRモードの起動 ····· 7
2-3. ROMのバージョン表示 ····· 7
2-4. SUB MPUのバージョン表示 ····· 7
2-5. バッテリーの電圧表示 ····· 7
2-6. ドラム回転積算時間の表示 ····· 7
2-7. サーボエラー履歴の表示 ····· 7
2-8. KEY PCBチェックモード ····· 8
2-9. 内臓オシレーターの使用方法 ····· 8
2-10. FRONT MPUの外し方 ····· 8
2-11. SYS ROMの外し方 ····· 8
2-12. オプション IF-AN98HR（A/Dボード, D/Aボード）のチェックについて ····· 9
2-13. リファレンスレベルの変更について ····· 9
2-14. EXTERNAL CONTROL I/Oについて ····· 12
3. メカ ASS'Yの組立 ····· 19
3-1. 組立のフローチャート ····· 19
3-2. メカ部品の取付け ····· 20
4. 機構部調整 ····· 26
4-1. 準備 ····· 27
4-2. テストテープ ····· 27
4-3. テンションアーム位置調整 ····· 28
4-4. トルク調整 ····· 28
4-5. テープ走行調整 ····· 29
4-6. FF, REW, REV モードでの走行確認 ····· 32
5. 電気系調整 ····· 35
5-1. 測定箇所および調整箇所 ····· 35
5-2. テストテープ ····· 36
5-3. 電源＋5Vの確認 ····· 36
5-4. PG（Phase Generator）位置調整 ····· 36
5-5. VCOフリーラン周波数自動補正回路のオフセット調整 ····· 37
5-6. 再生イコライザー調整 ····· 38
5-7. RFレベル確認 ····· 39
5-8. 再生エラーレート確認 ····· 40
5-9. 記録電流調整 ····· 41
5-10. 記録再生 RFレベル確認 ····· 43
5-11. 記録再生エラーレート確認 ····· 43
6. 分解図とパーツリスト ····· 45
7. 基板図とパーツリスト ····· 53
8. 付属品 ····· 71

1. SPECIFICATIONS
仕様

Tape recorder section

Format:	DTRS format
Recording method:	Rotary-head, helical-scan method
Tape type:	Hi8 MP tape / Hi8 ME
Head construction:	2 x record, 2 x playback
Tracking method:	ATF (Automatic Track Finding)
Erasure method:	Overwrite
Drum speed:	2,000 r.p.m.
Tape speed:	15.955 mm/sec.
Equivalent tape speed:	4.2 m/sec.
Maximum recording time:	108 min. (using P6-120 tape)
Time to play from stop:	Less than 2 seconds
Fast forward/rewind time:	80 seconds (using P6-120 tape)
Search speed:	Maximum of 100 x play speed
Shuttle speed:	Forward and reverse at 8.0, 4.0, 2.0, 1.0, 0.5 and 0.25 play speed (1.0 speed available only in forward shuttle mode)
Vari speed:	±6% (0.1% steps)
Positioning accuracy:	To 1 sample
Positioning lock time:	Within 8 seconds (when locating 2 DA-98HRs synced together)
Number of recording tracks:	8
Sub-code:	ABS track, SMPTE/EBU timecode facility
Error correction:	Double- encoded Reed-Solomon code
Sampling frequency:	44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz
Recording resolution:	16/24 bits linear
Cross-fade time:	10 ms to 200 ms (10 ms increments)
Track delay:	–200 to +7,200 samples (–4 to +150 ms) in single-unit increments. Can be set in samples or ms.
Offset:	±2 hours (to frame accuracy)
Sync clock:	Internal, WORD or VIDEO
MIDI function:	MMC (MIDI Machine control) MTC (MIDI timecode) output TASCAM System Exclusive (track delay, etc.) Control Cahnge (mixdown)
Supported timecode formats:	SMPTE 30, 29.97 drop, 29.97 non-drop, EBU 25 and Film 24 fps with telecine pull-up and pull-down facilities

定格

録音フォーマット：	DTRSフォーマット
記録方式：	回転ヘッド式ヘリカルスキャン方式
使用テープ：	Hi8-ME および Hi8-MPテープ
ヘッド構成：	記録用×2　再生用×2
トラッキング方式：	ATF (Automatic Track Finding)
消去方法：	オーバーライト消去
ドラム回転数：	2,000 rpm.
テープ速度：	15.955 mm/sec
記録相対速度：	4.2 m/sec
記録時間：	108分（P6-120分テープ使用時）
再生立ち上がり時間：	2秒以内
早送り／巻き戻し時間：	約80秒（P6-120分テープ使用時）
サーチ速度：	最大100倍
シャトル速度：	正方向：×8,4,2,1,1/2,1/4 倍 逆方向：×8,4,2,1/2,1/4 倍
ピッチコントロール：	±6%（0.1%単位）
調整精度：	1 サンプル未満
調相時ロック時間：	8秒以内（DA-98HR 2 台同期時）
記録チャンネル数：	最大8チャンネル
サブコード：	ABSタイム、SMPTE/EBUタイムコード記録可能
誤り訂正方式：	ダブルエンコーデッドリードソロモンコード
サンプリング周波数：	44.1kHz、48kHz、88.2kHz、96kHz、176.4kHz、192kHz
録音ビット：	16ビット、24ビット
基準レベル：	フルビット ー16、ー18、ー20dB 切替可能
エンファシス時定数：	50 μsec／15 μsec（再生時のみ自動選択）
クロスフェード時間：	10～200 msec（10msec 単位）
トラックディレイ：	ー200～+7200サンプル（1 サンプル単位）またはー4msec～+150msec（1msec 単位）
ABSタイムオフセット：	±2時間（フレーム単位）
シンククロック：	INT／WORD／VIDEO
MMCコントロール：	トラックディレイ、トラックコピー（システムエクスクルーシブメッセージ）
対応タイムコード：	SMPTE 30、29.97ドロップfps、29.97ノンドロップfps、EBU 25fps、フィルム 24fps

Inputs and outputs

TDIF-1 (DIGITAL I/O):	25-pin D-sub TDIF-1 format
DIGITAL (AES/EBU):	25-pin D-sub PRO AES3-1992 Amendment 3-1999
REMOTE IN/SYNC IN:	15-pin D-sub Conforms to REMOTE IN/SYNC IN protocol
SYNC OUT:	15-pin D-sub Conforms to REMOTE IN/SYNC IN protocol
WORD SYNC IN/THRU:	BNC connector, 75 Ω at TTL level ON/OFF (THRU auto-terminated)
WORD SYNC OUT:	BNC connector, 75 Ω at TTL level
TIME CODE IN:	XLR-3 balanced Input impedance: 10 kΩ Input level: 0.5 Vp-p to 10.0 Vp-p
TIME CODE OUT:	XLR-3 balanced Output impedance: 100Ω Output level: 2.0 Vp-p
MIDI:	IN, OUT, THRU
VIDEO IN/THRU:	NTSC or PAL Negative Sync Composite video, Sync Composite Video or Frame Pulse (auto detect) 1 Vp-p, ±0.2 V (Negative Sync Composite video or Sync Composite Video) TTL Level (Frame pulse) THRU autmatically terminated (75 Ω)
CONTROL I/O:	37-pin D-sub
RS-422:	9-pin D-sub Comforms to RS-422 specifications
METER UNIT:	15-pin D-sub

Physical specifications

Size (exc feet): w x h x d	482 x 176 x 356 (mm) 19 x 6.9 x 14 (in)
Weight:	11 kg (24 lb)

Power specifications

Power requirements:	USA/Canada 120 VAC, 60 Hz U.K./Europe 230 VAC, 50 Hz Australia 240 VAC, 50 Hz
Power consumption:	30 W (IF-AN98HR installed: 46 W)
Applicable electromagnetic environment:	E4
Peak inrush current:	15.5 A (230 V, all options fitted)

入出力

TDIF-1（DIGITAL I/O）:	TDIF-1［不平衡、D－Sub 25ピン、メス］
DIGITAL (AES/EBU) :	PRO AES3-1992 Amendment 3-1999準拠［D-Sub 25ピン］
REMOTE IN/SYNC IN :	REMOTE IN/SYNC IN プロトコル［D-Sub 15ピン、メス］
SYNC OUT :	REMOTE IN/SYNC IN プロトコル［D-Sub 15ピン、メス］
WORD SYNC IN :	TTLレベル相当／75Ωターミネート［BNC］
WORD SYNC OUT :	TTLレベル相当［BNC］
WORD SYNC THRU :	接続時、WORD SYNC INのターミネートオフを自動認識 自動オン／オフ方式［BNC］
TIME CODE IN :	0.5Vp-p ～ 10Vp-p／10kΩ ［平衡、XLR-3-31］
TIME CODE OUT :	2Vp-p／100Ω［平衡、XLR-3-32］
MIDI IN :	[DIN 5ピン]
MIDI OUT :	[DIN 5ピン]
MIDI THRU :	[DIN 5ピン]
VIDEO IN :	NTSC/PAL 75Ωターミネート [BNC] ネガティブシンクコンポジットビデオ、シンクコンポジットビデオ、フレームパルス（自動検出）、1Vp-p ±0.2V（ネガティブシンクコンポジットビデオ、シンクコンポジットビデオ）、TTLレベル相当（フレームパルス）
VIDEO THRU :	接続時、VIDEO INのターミネートオフを自動認識 自動オン／オフ方式「BNC]
CONTROL I/O :	[D-Sub 37ピン]
RS-422 :	[D-Sub 9ピン]
METER UNIT :	[D-Sub 15ピン、メス]

一般

電源：	100V AC 50-60Hz
消費電力：	30W（IF-AN98HR 装着時 46W）
質量：	11kg
外形寸法：	幅482×高さ176×奥行き356 mm（足を除く）

IF-AN98HR (Option)

All specifications refer to both D/A and A/D unless otherwise specified and are measured using Audio Precision System TWO cascade:

DTRS-HR mode

Sampling frequency:	44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz (±6%)
Sampling resolution:	24 bits
Frequency response:	
Fs=44.1 kHz, 48 kHz	20 Hz — 20,000 Hz (±0.5 dB)
Fs=96 kHz	20 Hz — 40,000 Hz (±1 dB)
THD:	< 0.004% (1 kHz, Fs=48 kHz) *
S/N, dynamic range:	> 110 dB (1 kHz, Fs=48 kHz) *
Channel separation:	> 95 dB (1 kHz)
De-emphasis:	50/15 µs
Nominal output level:	+4 dBu
Output impedance:	< 100 kΩ
Maximum output level:	20 dBu, 22 dBu, 24 dBu (selectable)
Nominal input level:	+4 dBu
Input impedance:	> 10 kΩ
Maximum input level:	20 dBu, 22 dBu, 24 dBu (selectable)

DTRS mode

As for DTRS-HR mode, except:

S/N, dynamic range:	> 100 dB (1 kHz, Fs=48 kHz) *

＊: These values are obtained with the I/O clock set to the Narrow setting.

IF-AN98HR（オプション）

● 特に明記していない項目はA/D ボード、D/A ボード共通の仕様です。
● Audio Precision System TWO cascade にて測定しています。

DTRS-HR モード

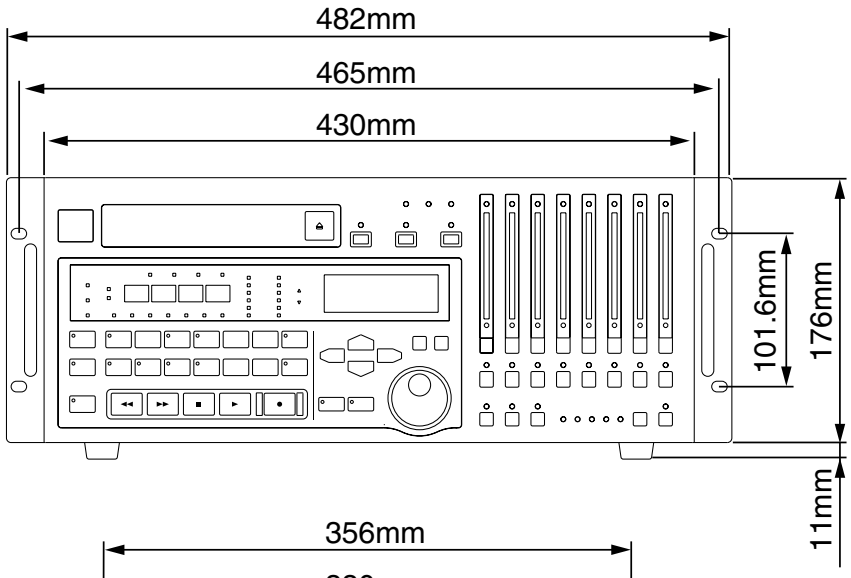
サンプリング周波数：	44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz (±6%)
サンプリング解像度：	24 ビット
録音再生周波数特性：	
Fs=44.1 kHz,48 kHz	20 Hz ～20,000 Hz (±0.5 dB)
Fs=96 kHz,88.2 kHz	20 Hz ～40,000 Hz (±1 dB)
THD＋N［22K LPF］：	0.004%以下 [1 kHz, Fs=48 kHz] * ［録音／再生時］
S/N 比、ダイナミックレンジ［22K LPF / A-Weight ］：	110 dB 以上 [1 kHz, Fs=48 kHz] * ［録音／再生時］
チャンネルセパレーション：	95 dB 以上[1 kHz]
デエンファシス：	50/15 µs
規定出力レベル：	+4 dBu
出力インピーダンス：	100 Ω以下
最大出力レベル：	20 dBu,22 dBu,24 dBu（選択可）
規定入力レベル：	+4 dBu
入力インピーダンス：	10 k Ω以上
最大入力レベル：	20 dBu,22 dBu,24 dBu（選択可）

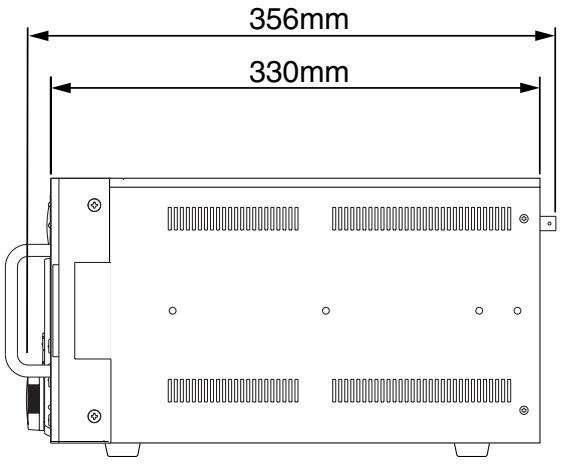
DTRS モード

［以下の項目を除いてDTRS-HR モード時と同じ］

S/N 比、ダイナミックレンジ［22K LPF / A-Weight］：	100 dB 以上 [1 kHz, Fs=48 kHz] * ［録音／再生時］

＊： I/O クロック＝Narrow 設定時の値


482mm
465mm
430mm
101.6mm
176mm
11mm


356mm
330mm

2. TECHNICAL INFORMATION

テクニカルインフォメーション

2-1. Activation of test mode

1. Hold down F.FWD + STOP + PLAY keys and press POWER key, and when "Select Mode" is displayed, let go of the three keys and, before 2 seconds is up, press STOP key. (TEST MODE should be displayed.)
2. The test mode is released when power is turned off.

2-2. Activation of VTR mode

1. Hold down F.FWD + STOP + PLAY keys and press POWER key, and when "Select Mode" is displayed, let go of the three keys and, before 2 seconds is up, press PLAY key. (VTR MODE should be displayed.)
2. The VTR mode is released when power is turned off.

2-3. Displaying ROM version numbers

1. Select the menu group F in the menu screen.
2. Move the cursor to the items shown below.
   Sys Ver : SYS ROM version
   Front Ver : FRONT MPU version
   Servo Ver : SERVO MPU version

2-4. Displaying SUB MPU version numbers

1. Enter the test mode.
2. Select the menu group N in the menu screen.
3. Move the cursor to "SubMpuVer" and press ENTER key.

2-5. Displaying the voltage of battery

1. Enter the test mode.
2. Select the menu group N in the menu screen.
3. Move the cursor to "Battery".

2-6. Displaying the hed drum utilized time

1. Select the menu group F in the menu screen.
2. Move the cursor to the items shown below.
   Dr Total : Total utilized time
   Dr Search : Fast-winded time

2-7. Displaying the servo error history

1. Enter the test mode.
2. Select the menu group M in the menu screen.
3. Move the cursor to "ServoErr" and press ENTER key.

Note)
Servo error data is stored in the SERVO PCB's EEPROM memory. As the power is unstable immediately after being turned ON, data written to the EEPROM at this time will be incorrect. To ensure accuracy, the DA-98HR prohibits data from being written to the EEPROM for 10 seconds after POWER ON. If an error occurs just 10 seconds, the error data is not stored in memory. As a result, the servo error history stored in the memory may differ from actual phenomena.

2-1. テストモードの起動

1. F FWDキー＋STOPキー＋PLAYキーを押しながら電源をONにし、“Select Mode”表示後 一旦手を離し、2秒以内にSTOPキーを押す。(TEST MODEと表示)
2. 電源をOFFにすると、テストモードが解除される。

2-2. VTRモードの起動

1. F FWDキー＋STOPキー＋PLAYキーを押しながら電源をONにし、“Select Mode”表示後 一旦手を離し、2秒以内にPLAYキーを押す。(VTR MODEと表示)
2. 電源をOFFにすると、VTRモードが解除される。

2-3. ROMのバージョン表示

1. メニュー画面で、メニューグループFを選択する。
2. カーソルを以下の項目に合わせる。
   Sys Ver : SYS ROMのバージョン
   Front Ver : FRONT MPUのバージョン
   Servo Ver : SERVO MPUのバージョン

2-4. SUB MPUのバージョン表示

1. テストモードにする。
2. メニュー画面で、グループNを選択する。
3. “SubMpuVer”にカーソルを合わせて、ENTERキーを押す。

2-5. バッテリーの電圧表示

1. テストモードにする。
2. メニュー画面で、グループNを選択する。
3. “Battery”にカーソルを合わせる。

2-6. ドラム回転積算時間の表示

1. メニュー画面で、メニューグループFを選択する。
2. カーソルを以下の項目に合わせる。
   Dr Total : トータル積算時間
   Dr Search : サーチ時 (PLAY, REC 以外) の積算時間

2-7. サーボエラー履歴の表示

1. テストモードにする。
2. メニュー画面で、メニューグループMを選択する。
3. “ServoErr”にカーソルを合わせて、ENTERキーを押す。

注)
サーボエラーはSERVO PCB内のEEPROMに記憶されていますが、POWER ON直後はまだ電源が十分安定しておらず、そのような状態でEEPROMにデータの書き込みを行うと誤ったデータを書き込んでしまいます。
そのため、DA-98HRではPOWER ON後10秒間はEEPROMへのデータの書き込みを禁止しています。したがって、POWER ON直後にサーボエラーが発生してから10秒経過する前にPOWER OFFした場合などでは、そのサーボエラーは経歴として記憶されませんので、実際の現象と記憶された情報とで差異が生じてしまう可能性があります。

2-8. KEY PCB check mode

1. While holding the PLAY, STOP, F FWD and REW key pressed, turn the power ON. In this case, all LED's light.
2. Press the STOP, F FWD, REW, PLAY or RECORD key. All LEDs go out.
3. When each key is pressed, the corresponding LED lights.

2-9. How to use the built-in oscillator

1. Enter the test mode.
2. Select the menu group 2 in the menu screen.
3. Move the cursor to "Sine Osc" and press ENTER key.
4. Use the ▲ and ▼ keys to select the output frequency (OFF, 440 Hz, 1 kHz, 10 kHz, 20 kHz, 20 Hz, wite noise). (The level is full scale.)

2-10. Removing the FRONT MPU

As shown in Fig. 2-1, hold the FRONT MPU (KEY PCB:U6) with the PLCC EXTRACTOR (P/N: 16910101) to remove it.

2-11. Removing the SYS ROM

Detach the socket cover to remove the SYS ROM (SYS PCB:U011). To remove the socket cover, slide it as shown in Fig. 2-2.

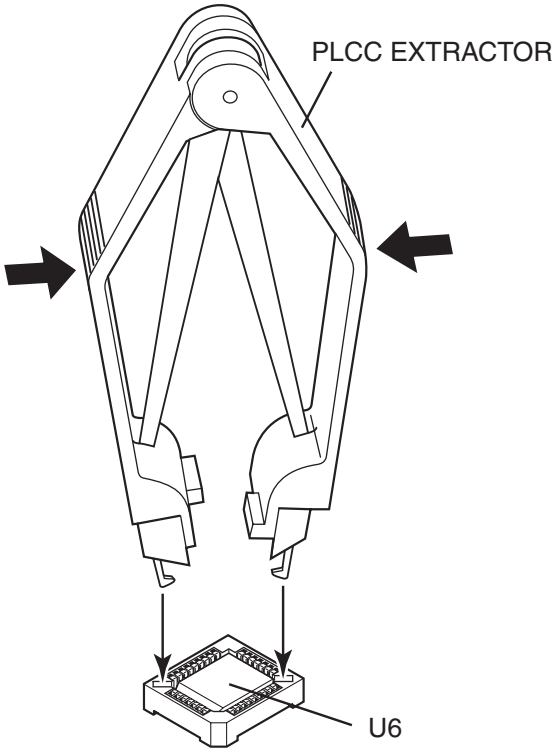


Fig. 2-1

2-8. KEY PCBチェックモード

1. PLAYキー＋STOPキー＋F FWDキー＋REWキーを押しながら電源をONにするとチェックモードに入る。このとき、LEDが全灯する。
2. STOP, F FWD, REW, PLAY, RECORDのいずれかのキーを押すと、LEDが全て消灯する。
3. その後、それぞれのキーを押すと、そのキーに対応するLEDが点灯する。

2-9. 内臓オシレーターの使用方法

1. テストモードにする。
2. メニュー画面で、メニューグループ2を選択する。
3. “Sine Osc”にカーソルを合わせてENTERキーを押す。
4. ▲キー/▼キーで、出力する周波数（OFF, 440Hz, 1kHz, 10kHz, 20kHz, 20Hz, White noise）を選択する。（レベルはフルスケール）

2-10. FRONT MPUの外し方

図2-1のように、PLCC EXTRACTOR（品番:16910101）でFRONT MPU（KEY PCB:U6)を挟んで取り外します。

2-11. SYS ROMの外し方

SYS ROM（SYS PCB:U011）はソケットカバーを取り外すことにより、外すことができます。
ソケットカバーは、図2-2のようにスライドさせることにより取り外します。

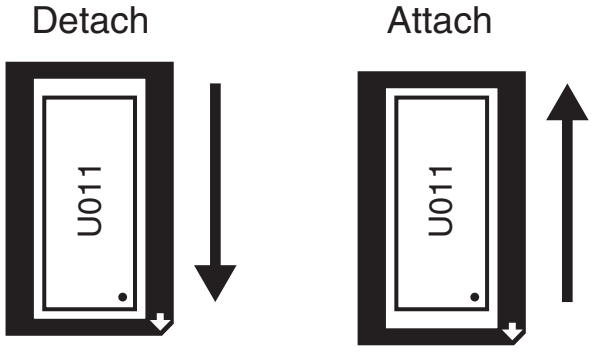


Fig. 2-2

2-12. Checking the optional IF-AN98HR (A/D board and D/A board)

To check the A/D board and D/A board, connect the EXTENSION PCB (P/N : 5200353800) to each board.
Note)
The EXTENSION PCB cannot be connected to the SYS PCB.

2-13. Changeover of Reference level

By replacing jumpers on the A/D and D/A boards, you can set the unit for one of the following reference levels.

Standard	Reference level	Nominal level	Maximum lelel
TASCAM	–16 dBFS	+4 dBu	+20 dBu
European	–18 dBFS	+4 dBu	+22 dBu
SMPTE	–20 dBFS	+4 dBu	+24 dBu

Depending on the required reference level, plug in jumpers as shown below. (See also figures 2-3 and 2-4.)

A/D board (ANALOG INPUT)

	–16 dBFS	–18 dBFS	–20 dBFS
W031 – 038	–	●	●
W041 – 048	–	–	●
W010	●	–	–
W020	–	●	–
W030	–	–	●

D/A board (ANALOG OUTPUT)

	–16 dBFS	–18 dBFS	–20 dBFS
W011 – 018	●	●	–
W021 – 028	●	–	–
W010	●	–	–
W020	–	●	–
W030	–	–	●

● : jumper plugged in (closed)
ー : jumper not plugged in (open)

2-12. オプション IF-AN98HR（A/Dボード, D/Aボード）のチェックについて

A/Dボード, D/Aボードのチェックの際は、EXTENSION PCB（品番:5200353800）を各PCBに接続してください。
注）EXTENSION PCBはSYS PCBには接続できません。

2-13. リファレンスレベルの変更について

A/Dボード, D/Aボード上のショートピンを差し換えることにより、以下の3種類の中からリファレンスレベルを選択することができます。

スタンダード	リファレンスレベル	基準レベル	最大レベル
TASCAM	－16 dBFS	+4 dBu	+20 dBu
ヨーロッパ	－18 dBFS	+4 dBu	+22 dBu
SMPTE	－20 dBFS	+4 dBu	+24 dBu

リファレンスレベルに応じて、ショートピンを下表のように設定します。（図2-3, 2-4 参照）

A/Dボード（ANALOG INPUT）

	－16 dBFS	－18 dBFS	－20 dBFS
W031～038	–	●	●
W041～048	–	–	●
W010	●	–	–
W020	–	●	–
W030	–	–	●

D/Aボード（ANALOG OUTPUT）

	－16 dBFS	－18 dBFS	－20 dBFS
W011～018	●	●	–
W021～028	●	–	–
W010	●	–	–
W020	–	●	–
W030	–	–	●

●：ショートピンを差す（クローズ）
ー：ショートピンを差さない（オープン）

A/D board

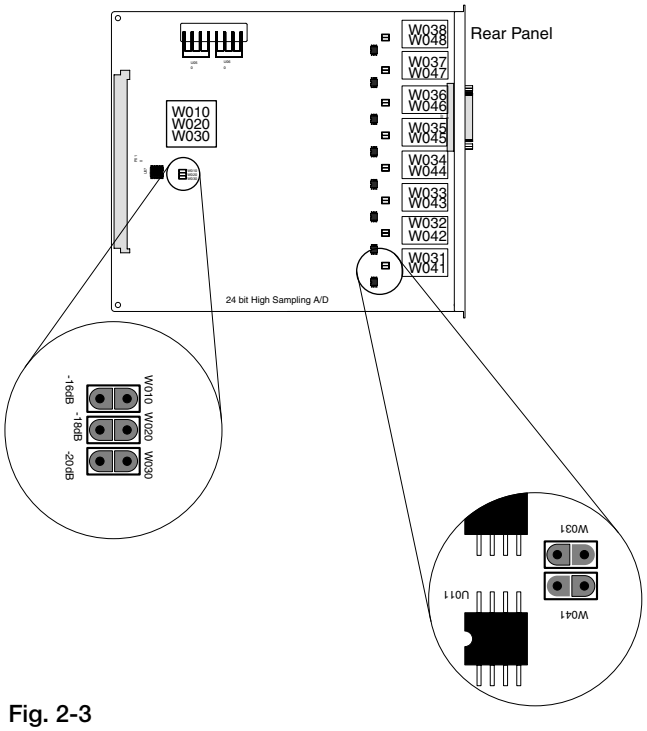
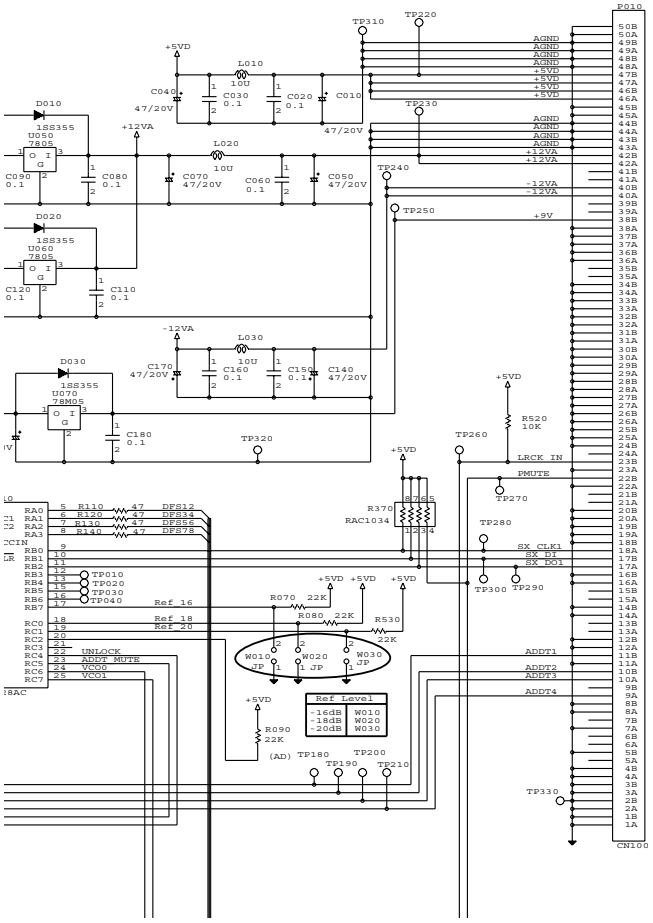
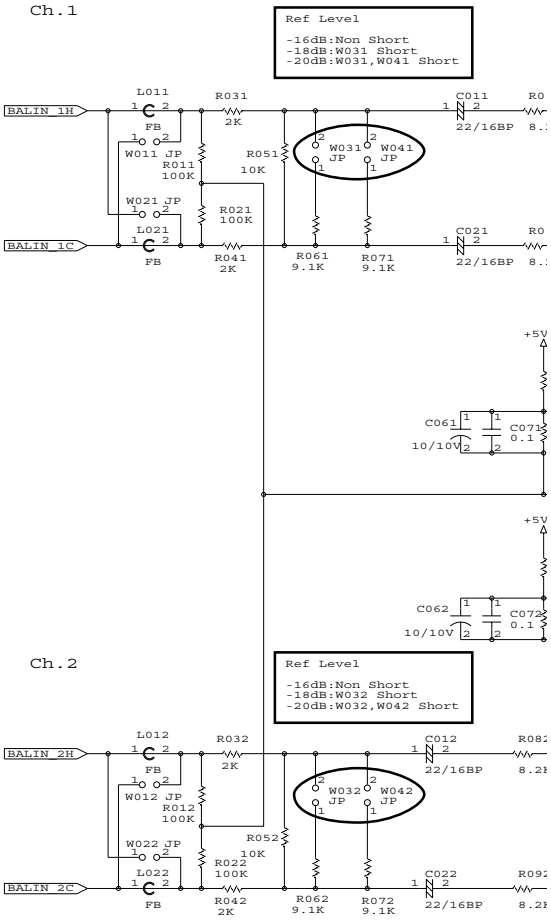


Fig. 2-3





D/A board

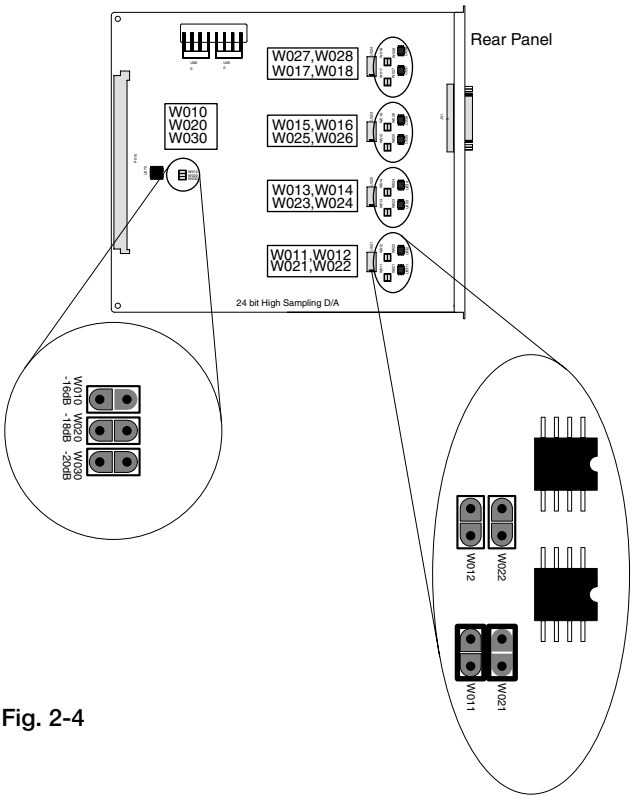
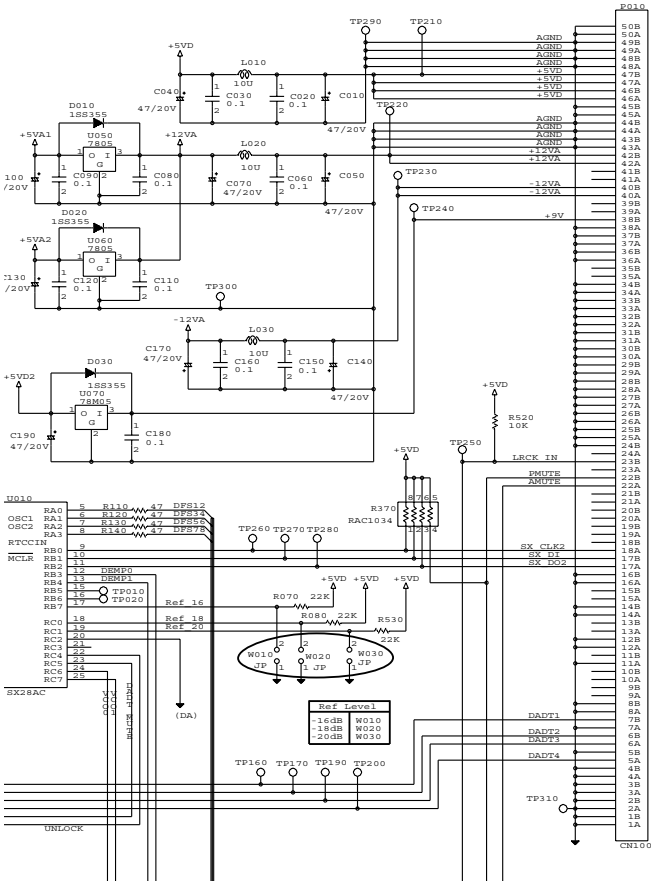
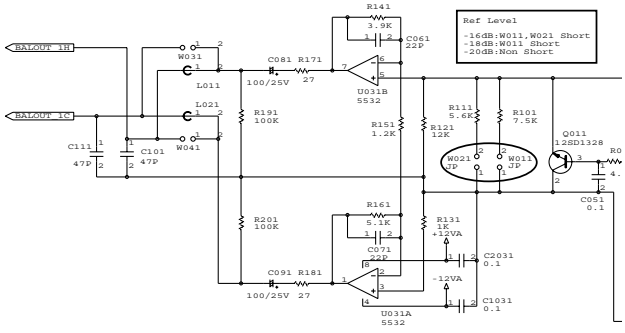


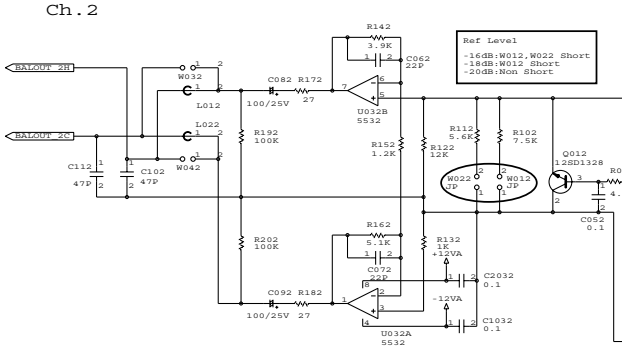
Fig. 2-4



Ch.1



Ch.2



2-14. EXTERNAL CONTROL I/O

A CONTROL I/O connector is provided to enable external control of the DA-98HR. Transport control (+Chase) inputs and related tally (+Lock) outputs are readily available.
To enable further capability of REC FUNCTION and INPUT MONITOR inputs and its related tally outputs, the CONTROL I/O also consists of signals for serial communication data.

- The connector is a 37-pin D-sub and the output is an open collector. Each transistor supports a current of up to 50 mA.
  Input is at TTL level with 74LS240 of the LS-TTL used as a buffer (with Schmitt trigger).
- Power supplied from the DA-98HR is up to 50 mA at DC 5 V.
- The control system data output is 32-bit serial sync, of which 8 bits are output in parallel simultaneously.
  Input is 32-bit serial sync. The preceding 8 bits are merged with the parallel input.

The pin assignment, serial input/output signal format and recommended circuits for a controlling device are described here in after.

2-14. EXTERNAL CONTROL I/Oについて

CONTROL I/Oは外部からDA-98HRをコントロールするために設けられた端子です。トランスポートコントロール（＋チェース）入力と、そのタリー（＋ロック）を出力します。また、REC FUNCTION、INPUT MONITORのキー入力と、そのタリーを出力することを可能とするために、シリアル通信用信号も用意されています。

- 端子は D-sub 37pin、出力はオープンコレクターで各トランジスターは 50mAまで電流を流すことができます。
  入力はTTLレベルで、バッファとしてLS-TTLの74LS240を使用（シュミットトリガ付き）しています。
- DA-98HRから供給できる電源は DC5Vで 50mAまで可能です。
- コントロール系のデータの出力は、シリアル同期式 32ビット、そのうち 8ビットがパラレル出力され、入力はシリアル同期式 32ビット、先行 8ビットがパラレル入力とマージされます。

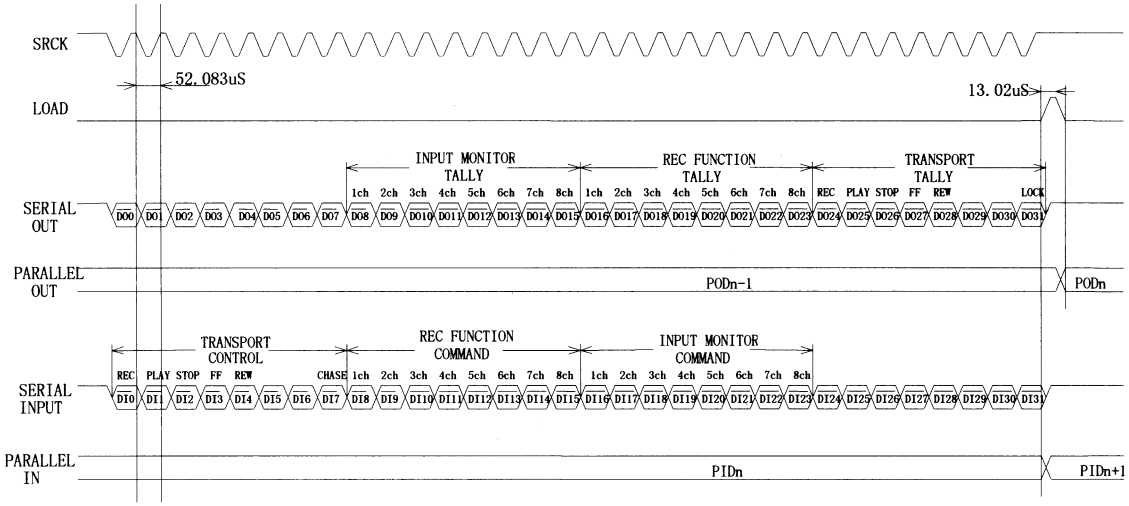
以下に、ピンアサイン、シリアル入出力信号フォ-マット、リモコンを作るときの推奨回路を記載します。

J11 Pin Assignment

Pin No.	Pin No.	Signal	Function	Input/output state
1		PLAY	PLAY command input	TTL
	20	GND	GND	GND
2		FF	FF command input	TTL
	21	SERIAL OUT	Serial data output	Open Collector
3		REW	REW command input	TTL
	22	NC	No connection　未使用端子	
4		AUX1	Auxiliary 1 input　予備1 入力	TTL
	23	SERIAL IN	Serial data input	TTL
5		STOP	Stop command input	TTL
	24	NC	No connection　未使用端子	
6		REC	REC command input	TTL
	25	NC	No connection　未使用端子	
7		AUX2	Auxiliary 2 input　予備2 入力	TTL
	26	NC	No connection　未使用端子	
8		CHASE	CHASE command input	TTL
	27	NC	No connection　未使用端子	
9		NC	No connection　未使用端子	
	28	NC	No connection　未使用端子	
10		GND	GND	GND
	29	NC	No connection　未使用端子	
11		PLAY TALLY	PLAY tally output	Open collector
	30	NC	No connection　未使用端子	
12		FF TALLY	FF tally output	Open collector
	31	NC	No connection　未使用端子	
13		REW TALLY	REW tally output	Open collector
	32	SRCK	Shift resister clock output	Open collector
14		STOP TALLY	STOP tally output	Open collector
	33	NC	No connection　未使用端子	
15		REC TALLY	REC tally output	Open collector
	34	LOAD	Load pulse output	Open collector
16		LOCK TALLY	LOCK tally output	Open collector
	35	NC	No connection　未使用端子	
17		AUX 1 TALLY	Auxiliary 1 output　予備1 出力	Open collector
	36	GND	GND	GND
18		AUX 2 TALLY	Auxiliary 2 ouput　予備2 出力	Open collector
	37	VCC +5V	Power supply DC +5V	DC5V
19		ACTIVE SENSE	Active sensse input ＊	TTL

＊: is to be connected to GND in the controlling device side to activate any tally output.
＊: はタリー出力を有効とするために、リモコン側でGNDに接続するものです。

CONTROL I/O Serial Input/output signal format



DA-98HR OUTPUT DATA（OPEN COLLECTOR）

DO0～DO7 : Undefined　未定義
DO8～DO15 : TALLY OF INPUT MONITOR（1ch, 2ch .... 8ch）
DO16～DO23 : TALLY OF REC FUNCTION（1ch, 2ch .... 8ch）
DO24 : REC TALLY
DO25 : PLAY TALLY
DO26 : STOP TALLY
DO27 : FF TALLY
DO28 : REW TALLY
DO29, DO30 : Undefined　未定義
DO31 : LOCK TALLY

DA-98HR INPUT DATA（TTL LEVEL）

DI0 : REC COMMAND
DI1 : PLAY COMMAND
DI2 : STOP COMMAND
DI3 : FF COMMAND
DI4 : REW COMMAND
DI5, DI6 : Undefined　未定義
DI7 : CHASE COMMAND
DI8～DI15 : REC FUNCTION COMMAND（1ch, 2ch .... 8ch）
DI16～DI23 : INPUT MONITOR COMMAND（1ch, 2ch .... 8ch）
DI24～DI31 : Undefined　未定義

Recommended circuit for a controlling device

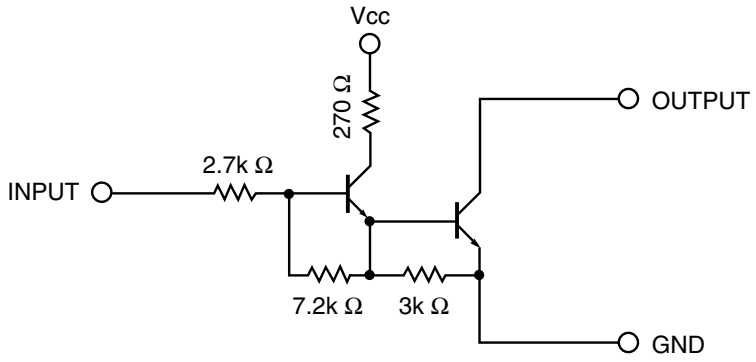
For detailed schematics of the circuit, refer to Figs. 2-5 and 2-6.

- The equivalent circuit (for one gate) of the transistor array TD62381F (P/N: S0036924) which is used for the CONTROL I/O parallel output is shown below.

リモコンの推奨回路について

具体的な回路については、図2-5, 2-6を参照してください。

- CONTROL I/Oのパラレル出力に使用されているトランジスターアレー TD62381F（品番: S0036924）の等価回路（1回路分）は以下の通りです。



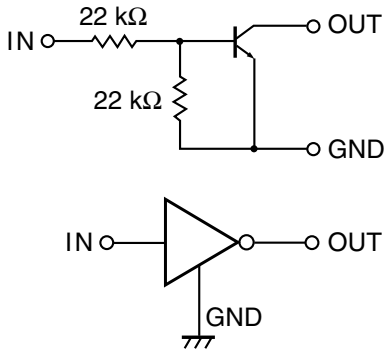
Contents 内 容		Condition 条 件	Min. 最小	Max. 最大
I_{OUT}	Current for one gate when 8 circuits operate 8回路動作時の1回路あたりの電流	Duty=10 %	0 mA	400 mA
		Duty=50 %	0 mA	330 mA
$V_{ce\ (sat)}$	Saturation voltage between collector and emitter コレクターエミッタ間飽和電圧	I_{OUT}=500 mA		0.9 V
		I_{OUT}=350 mA		0.7 V

Note) When using the power supply (DC 5 V) from the DA-98HR, suppres all curent consumption to less than 50 mA.

注) DA-98HRからの電源（DC 5V)を使用する場合は、全消費電流を50 mA以下に抑えてください。

● The equivalent circuit of the transistor DTC124EKA (P/N: 13428287) which is used for the CONTROL I/O serial output is shown below.

● CONTROL I/Oのシリアル出力に使用されているトランジスター DTC124EKA（品番: 13428287）の等価回路は以下の通りです。



	Typ. 標 準	Max. 最 大	Conditon 条 件
V_O	0.1 V	0.3 V	I_O=10 mA, I_I=0.5 mA
I_I		0.36 mA	V_{II}=5 V
I_O		0.5 μA	V_{CC}=50 V, V_I=0 V

Note) When connecting more than one unit or when this unit incorporated in a system with high power comsumption, isolate the inputs/outputs from DA-98HR with a photo-coupler.

注）複数台の機器を接続する場合や消費電力の大きな機器に組み込む場合は、入出力をフォトカプラでアイソレーションしてください。

Recommended Circuit (For Basic Control)　推奨回路 1（BASIC CONTROL用）

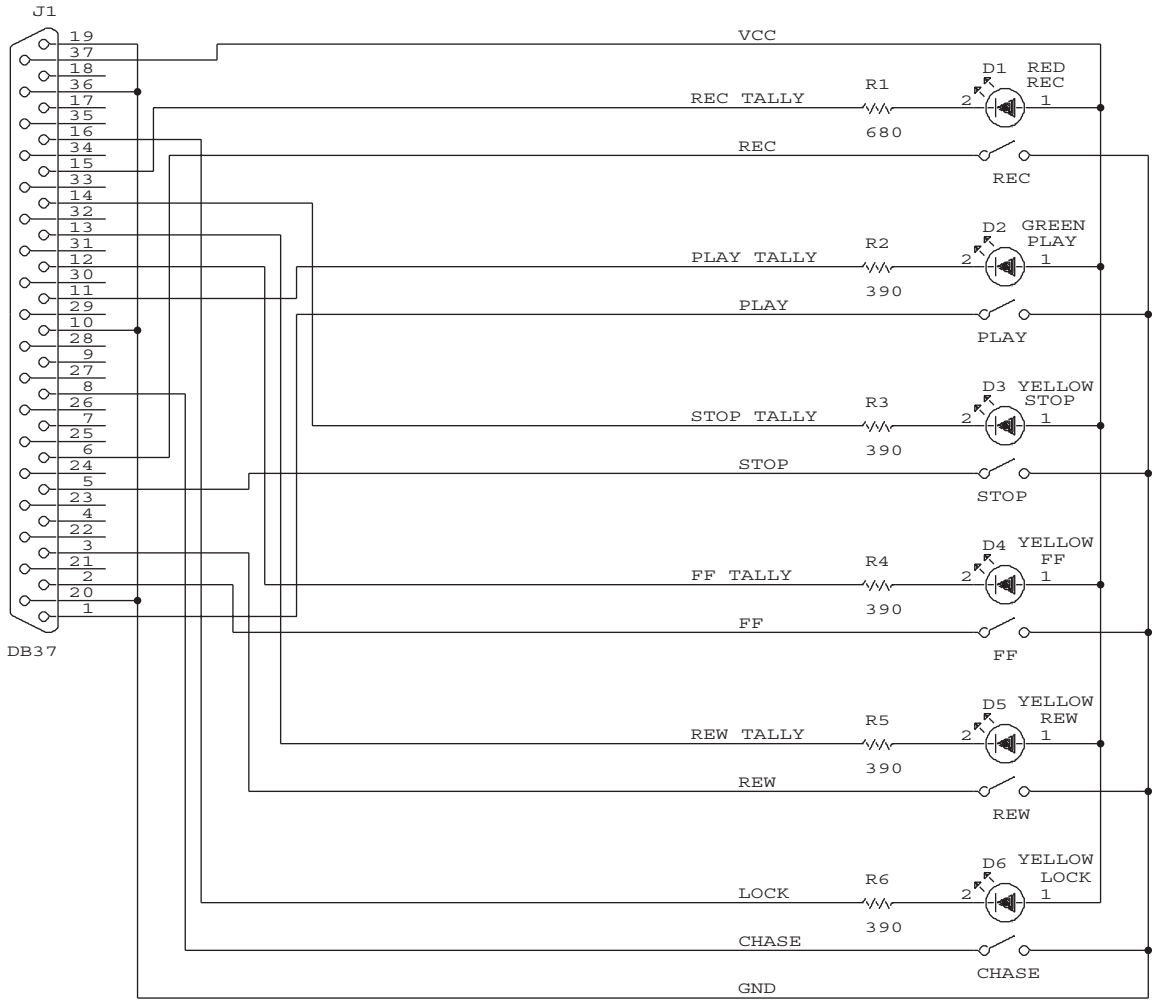


Fig. 2-5

Recommended Circuit (For Full Function)　推奨回路 2（FULL FUNCTION用）

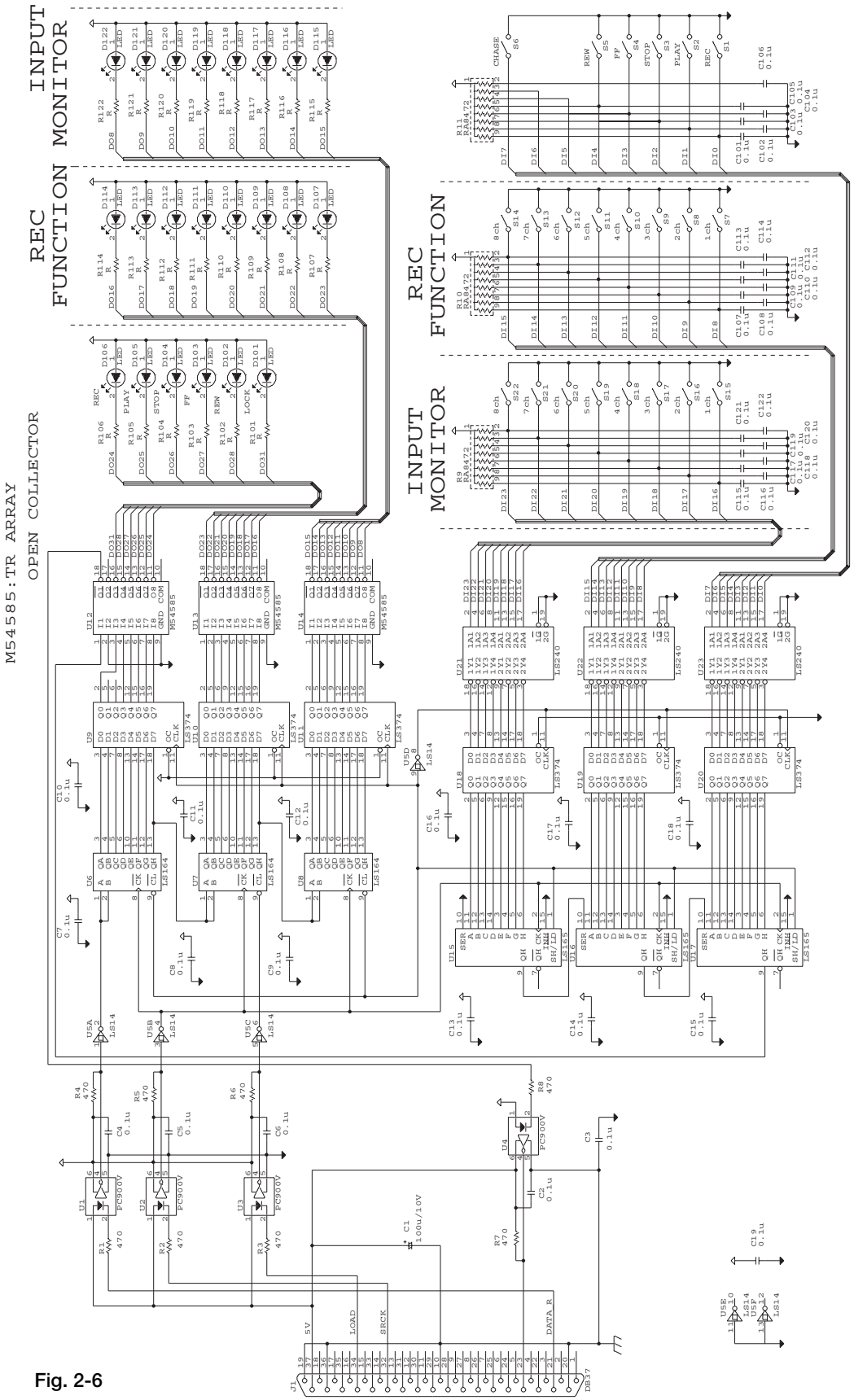


Fig. 2-6

3. ASSEMBLING THE MECHANISM ASS'Y

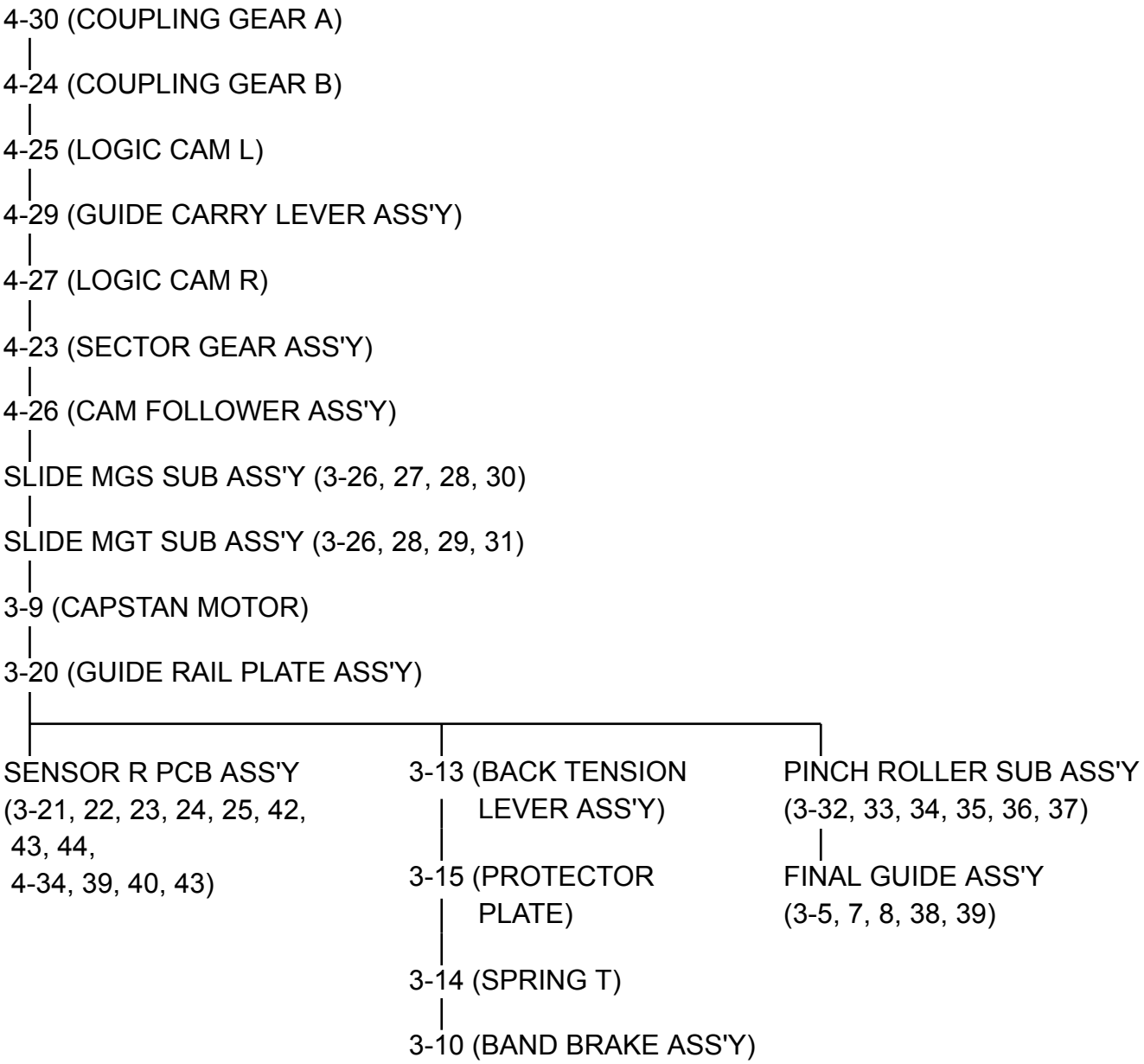
メカ ASS'Yの組立

3-1. Flowchart of assembling

For parts that require caution when reassembling the mechanism ass'y (especially critical gear meshes), a flowchart showing the order of installation is showed below. Disassembly should be performed in the reverse order of reassembly. As parts are indicated using reference numbers, refer to EXPLODED VIEWS -3 and -4 (☞ pages 49 & 51) for identification.

3-1. 組立のフローチャート

メカASS'Yの組立の際、取付け時に注意が必要な部品（特にギヤの噛み合わせ位置が重要）について、取付けの順番を示したフローチャートを以下に記します。
尚、分解は取付けの逆の順番で行って下さい。
また、部品は部番で示しますので、部番につきましては、EXPLODED VIEW-3, -4（☞ 49, 51ページ）を参照してください。



3-2. Installation of the mechanical parts

For parts that require caution when reassembling the mechanism ass'y(especially critical gear meshes), the following is showed.

[For order of installation, see flowchart (☞ page 19) and EXPLODED VIEWS -3 and -4 (☞ pages 49 & 51).]

1. Installing COUPLING GEAR B (4-24), and COUPLING GEAR A (4-30)

   As shown in Fig. 3-1, install 4-24 and 4-30 so that the two marks are visible.

2. Installing LOGIC CAM L (4-25) , and GUIDE CARRY LEVER ASS'Y (4-29)

   1) Install 4-25 so that hole ⓒ in 4-25 in Fig. 3-2 is aligned with hole ⓐ (Fig. 3-1) in the mechanism chassis. (Using a 1 mm dia. rod, pass it through the both holes to see if they are aligned with each other. Whenever checking holes for alignment hereafter, employ this method.)
   2) Similarly, install 4-29 so that hole ⓓ in 4-29 in Fig. 3-2 is aligned with hole ⓑ (Fig. 3-1) in the mechanism chassis.

3. Installing LOGIC CAM R (4-27)

   Install 4-27 so that hole ⓔ in 4-27 in Fig. 3-3 is aligned with the holes (hole ⓓ in 4-29 aligned in 2) of 2 with hole ⓑ in the mechanism chassis).
   At this time, recheck that the holes aligned in 1) of 2 (hole ⓒ in 4-25 and hole ⓐ in the mechanism chassis) are aligned with each other.

3-2. メカ部品の取付け

メカASSYの組立の際、取付け時に注意が必要な部品（特にギヤの噛み合わせ位置が重要）について述べます。

[取付けの順番については、フローチャート（☞ 19ページ）およびEXPLODED VIEW-3, -4（☞ 49, 51ページ）を参照してください。]

1. COUPLING GEAR B（4-24）、COUPLING GEAR A（4-30）の取付け

   4-24, 4-30は図3-1のように、マーク2個が表側になるように取り付ける。

2. LOGIC CAM L（4-25）、GUIDE CARRY LEVER ASS'Y（4-29）の取付け

   1）図3-2の4-25の穴 ⓒとメカシャーシの穴 ⓐ（図3-1）が一致するように、4-25を取り付ける。
   （1mm径の棒で両方の穴を貫通させるようにすると一致したかを確認することができます。以下、穴位置の一致を確認するときは、この方法で行ってください。）
   2）同様に、図3-2の4-29の穴 ⓓとメカシャーシの穴 ⓑ（図3-1）が一致するように、4-29を取り付ける。

3. LOGIC CAM R（4-27）の取付け

   図3-3の4-27の穴 ⓔと、2の2）で一致させた穴（4-29の穴 ⓓとメカシャーシの穴 ⓑ）が一致するように、4-27を取り付ける。
   このとき、2の1）で一致させた穴（4-25の穴 ⓒとメカシャーシの穴 ⓐ）が一致していることを再度確認する。

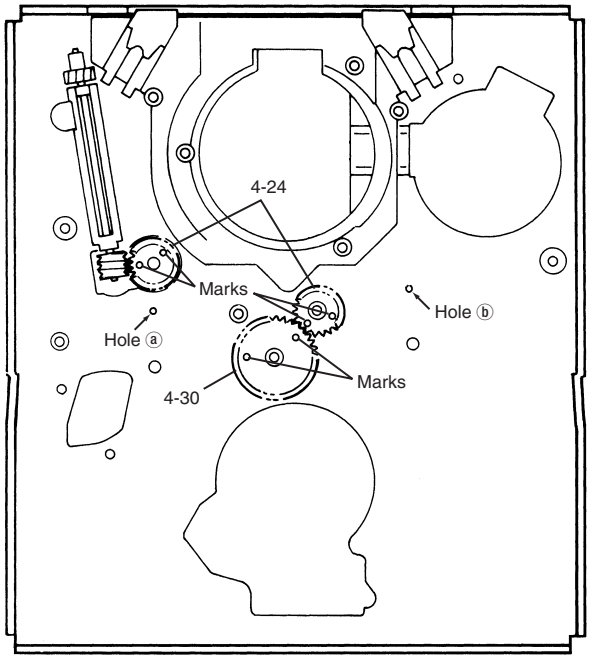


Fig. 3-1

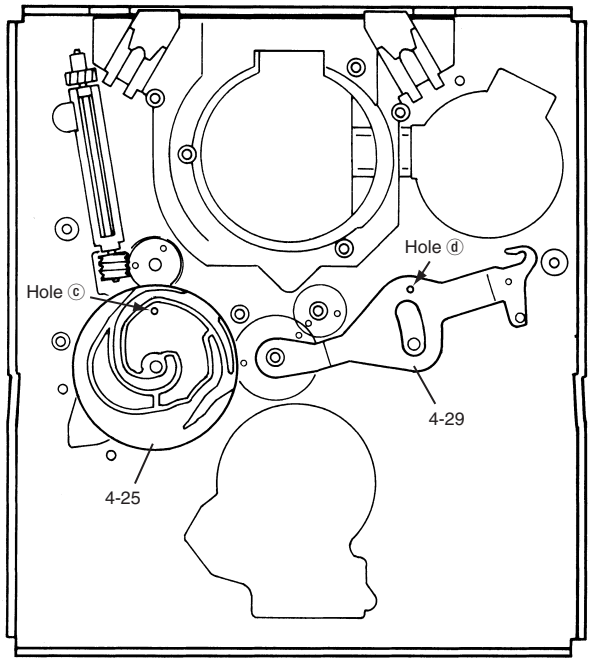


Fig. 3-2

4. Installing SECTOR GEAR ASS'Y (4-23)

Install 4-23 so that hole ⓕ in 4-23 in Fig. 3-3 is aligned with the holes (hole ⓒ in 4-25 aligned in 1) of 2 with hole ⓐ in the mechanism chassis).

5. Installing SLIDE MGS SUB ASS'Y (3-26, 27, 28, 30)

1) As shown in Fig. 3-4, install 3-30 so that mark ⓗ on 3-30 is aligned with mark ⓖ on 4-23.
2) Insert SLIDE MGS into the groove of catcher ⓞ by pushing it from the direction of arrow ⓚ.
(While retracting the lever of 3-30 in the direction of arrow ⓛ with one hand, then with the other hand, push SLIDE MGS towards the groove of catcher ⓞ and release the hands.)

6. Installing SLIDE MGT SUB ASS'Y (3-26, 28, 29, 31)

1) As shown in Fig. 3-4, install 3-31 so that mark ⓙ on 3-31 is aligned with mark ⓘ on 3-30.
2) Insert SLIDE MGT into the groove of catcher ⓟ by pushing it from the direction of arrow ⓜ.
(While retracting the lever of 3-31 in the direction of arrow ⓝ with one hand, then with the other hand, push SLIDE MGT towards the groove of catcher ⓟ and release the hands.)

4. SECTOR GEAR ASS'Y (4-23) の取付け

図3-3の4-23の穴 ⓕと、2の1) で一致させた穴（4-25の穴 ⓒとメカシャーシの穴 ⓐ）が一致するように4-23を取り付ける。

5. SLIDE MGS SUB ASS'Y (3-26, 27, 28, 30) の取付け

1) 図3-4のように、3-30のマーク ⓗと4-23のマーク ⓖが一致するように3-30を取り付ける。
2) SLIDE MGSを矢印 ⓚの方向からキャッチャー ⓞの溝に挿入する。(3-30のレバーを片方の指で矢印 ⓛの方向に戻しながら他方の指でSLIDE MGSをキャッチャー ⓞの溝に挿入し、指を離す。)

6. SLIDE MGT SUB ASS'Y (3-26, 28, 29, 31)の取付け

1) 図3-4のように、3-31のマーク ⓙと3-30のマーク ⓘが一致するように3-31を取り付ける。
2) SLIDE MGTを矢印 ⓜの方向からキャッチャー ⓟの溝に挿入する。(3-31のレバーを片方の指で矢印 ⓝの方向に戻しながら他方の指でSLIDE MGTをキャッチャー ⓟの溝に挿入し、指を離す。)

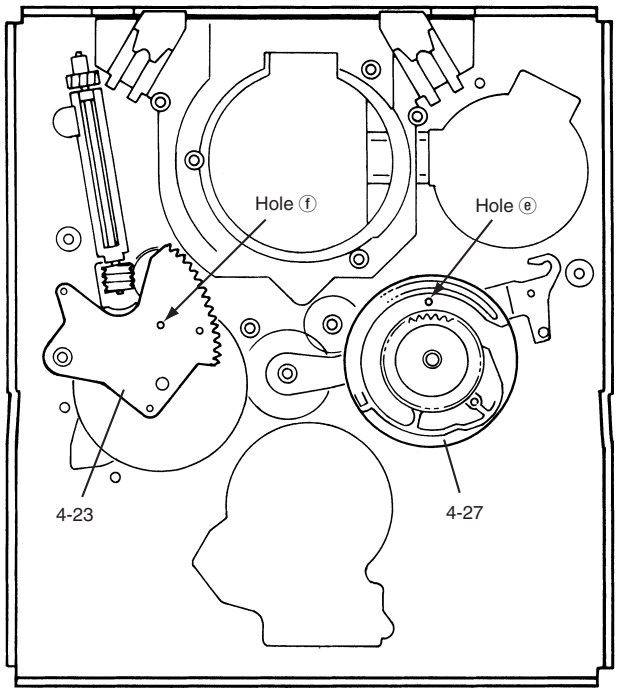


Fig. 3-3

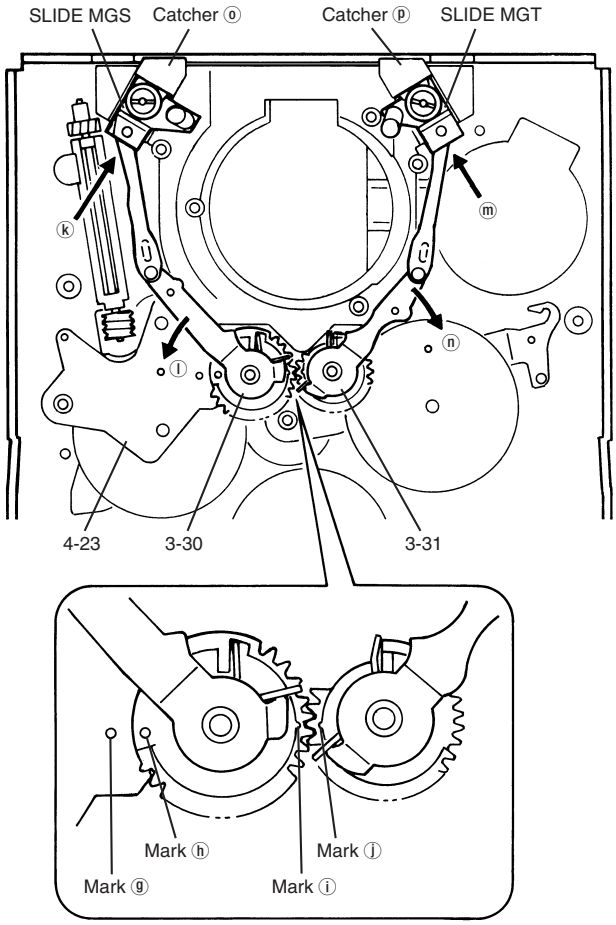


Fig. 3-4

7. Installing MODE SW ASS'Y (3-25)

See Fig. 3-5.

1) Align the U groove in the PCB on the back of the gear of 3-25 with the V groove in the gear by turning the gear.
Note)
For reasons of explanation the illustration shows a view from the gear, but in practice, you cannot see them clearly unless you see them from the PCB.
As a rule of thumb, align the mark on the gear with the U groove in the PCB behind the gear to facilitate the above positioning.
2) Fit 3-25 over the boss on the chassis.

7. MODE SW ASS'Y（3‐25）の取付け

図3-5参照。

1）3-25のギヤの裏面にあるPCBのU溝にギヤのV溝がくるように、ギヤを回してセットする。
注）図では、説明のためギヤ面から見たイラストが書いてありますが、実際にはPCB面から見ないとよく確認することはできません。
尚、図のギヤのマークをギヤの裏面にあるPCBのU溝の位置に合わせるようにすると、上記位置合わせの目安になります。
2）3-25をシャーシの軸に挿入する。

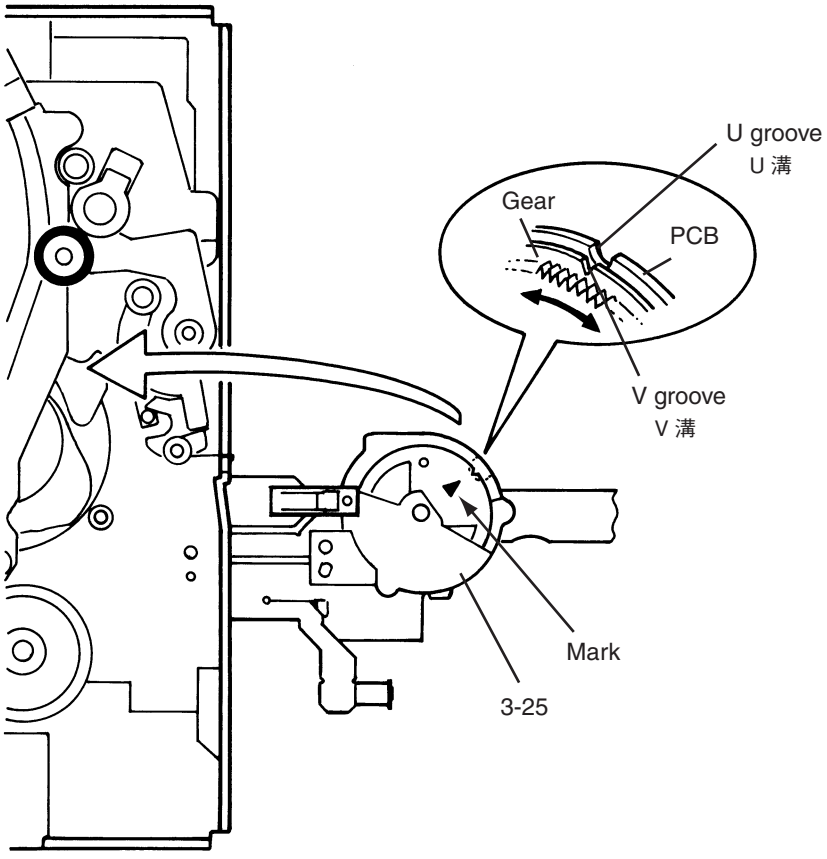


Fig. 3-5

8. Installing BAND BRAKE ASS'Y (3-10)

1) Before installing 3-10, fit COIL SPRING (3-11) to 3-10 as shown in Fig. 3-6.
2) After installing 3-10 as shown in Fig. 3-7, push portion A of 3-11 downward with a rod to disengage it, then hook it over the hook of REEL LOCK LEVER (4-21).

8. BAND BRAKE ASS'Y（3-10）の取付け

1）3-10を取り付ける前に、COIL SPRING（3-11）を図3-6のように3-10に取り付ける。
2）3-10を図3-7のように取り付けた後、3-11のA部を棒で下側に押して外し、その下にあるREEL LOCK LEVER（4-21）のフックに掛ける。

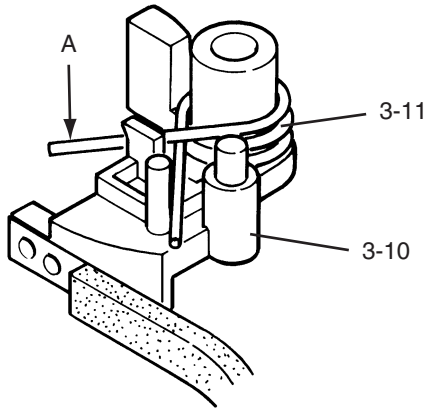


Fig. 3-6

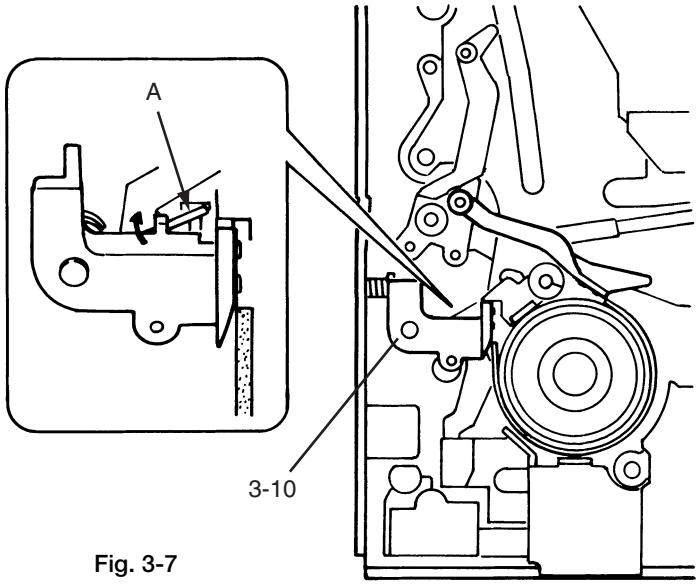


Fig. 3-7

9. Installing PINCH ROLLER SUB ASS'Y

See Fig. 3-8

Fit PINCH ROLLER SUB ASS'Y over the boss on the mechanism chassis, then hook spring edge A over hook B at the edge of the mechanism chassis.

9. PINCH ROLLER SUB ASS'Y の取付け

PINCH ROLLER SUB ASS'Yをメカシャーシの軸に取り付けた後、バネ端Aを図3-8のようにメカシャーシ側面のフックBに掛ける。

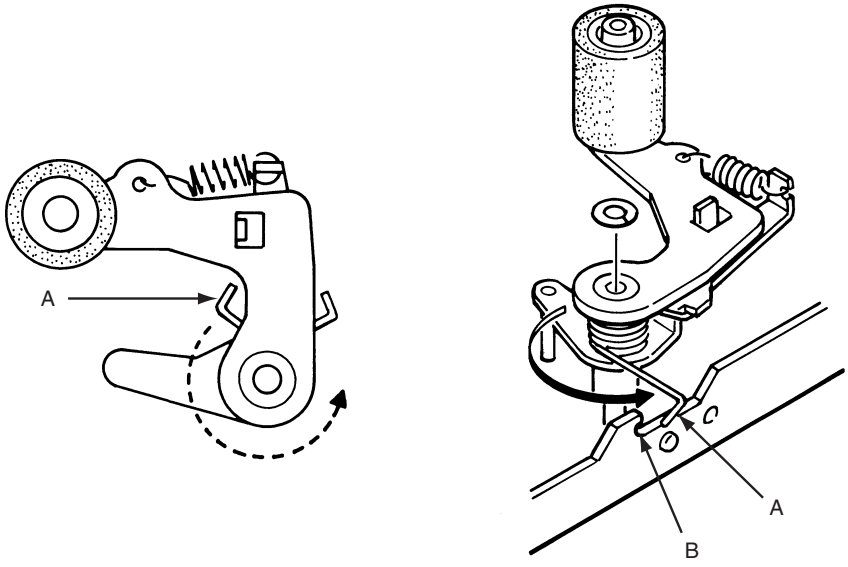


Fig. 3-8

10. Final checking of gear meshes

After installation of all mechanical parts is complete, check to see if gear meshes (items 1 to 7) are proper as follows:

1) Insert a 1 mm dia. rod into hole ' in Fig. 3-9, and check to see if it passes through up to the hole in the mechanism chassis.
2) Insert a 1 mm dia. rod into hole , in Fig. 3-9, and check to see if it passes through up to the hole in the mechanism chassis.
3) Check to see if the mark of 4-27 is aligned with the V groove in the MODE SW ASS'Y (3-25) gear as shown in Fig. 3-9.

10. ギヤの噛み合わせ位置最終確認

すべてのメカ部品を取り付けた後、ギヤの噛み合わせ（1～7項）が正しく行われたかを以下のように確認する。

1）図3-9の穴 ⓠに1mm径の棒を差し込んだとき、メカシャーシの穴まで貫通することを確認する。
2）図3-9の穴 ⓡに1mm径の棒を差し込んだとき、メカシャーシの穴まで貫通することを確認する。
3）図3-9のように、4-27のマークがMODE SW ASS'Y（3-25）のギアのV溝に合っていることを確認する。

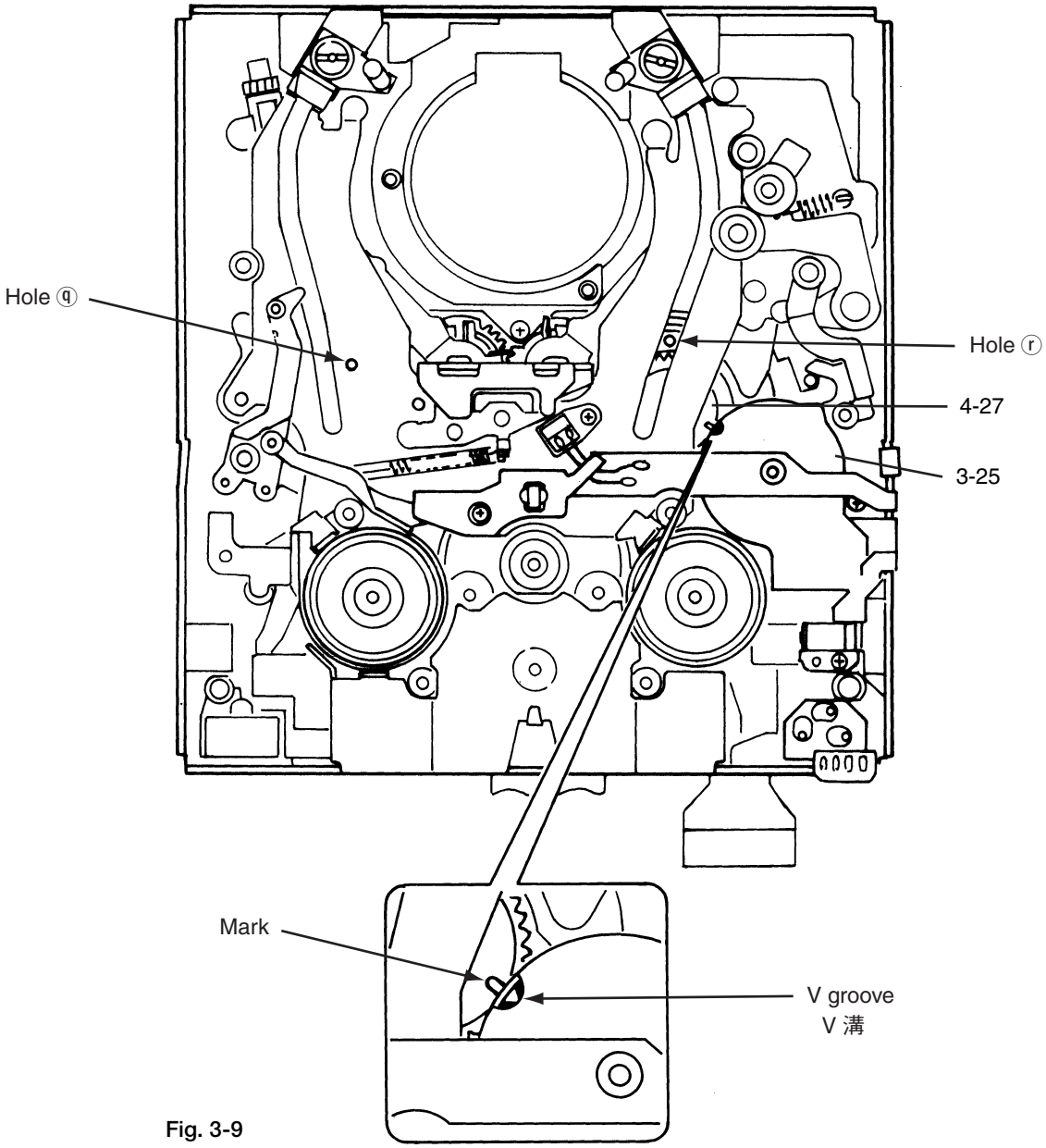


Fig. 3-9

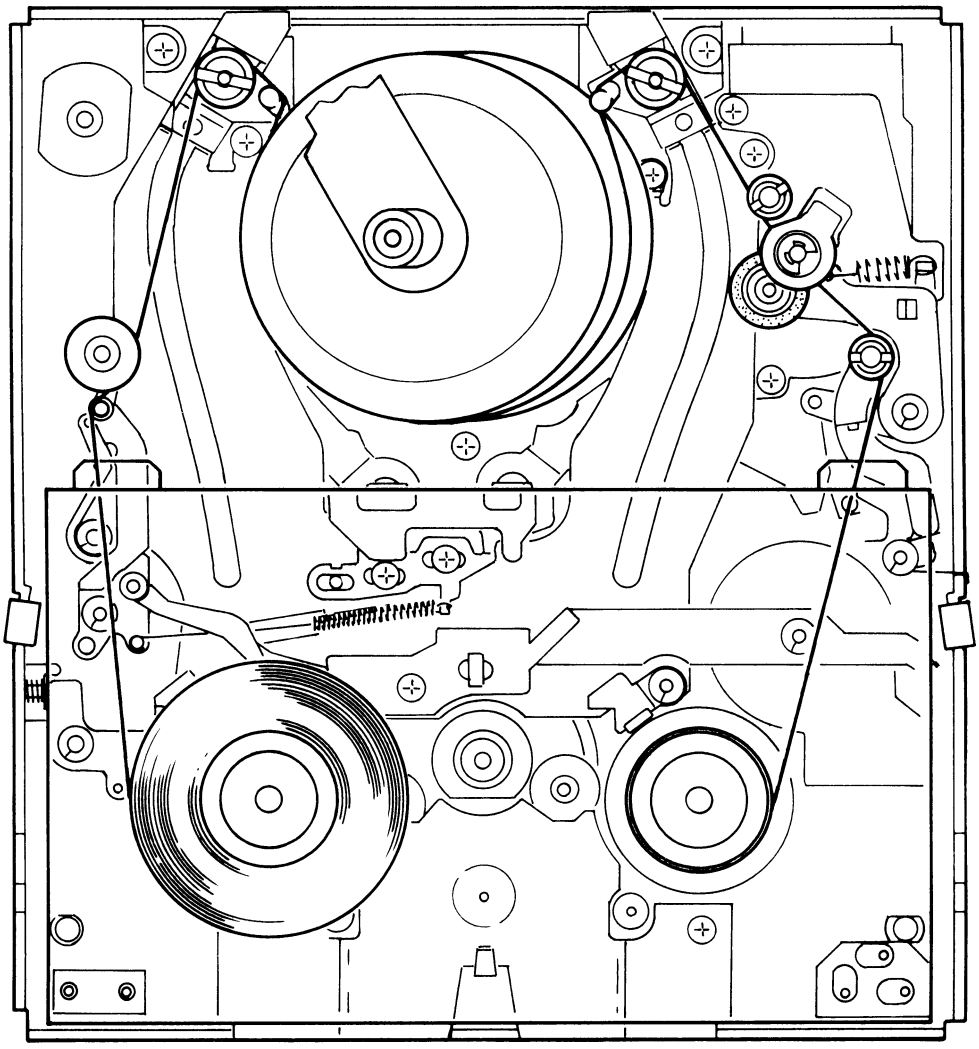
11. Replacing BRUSH ASS’Y (4-33)

With the DA-98HR, the drum is grounded through the sliding action of a slip ring and brush in place of through a single contact point which is the case with previous DTRSs. Therefore, when BRUSH ASS’Y (4-33) has been used for the specified hours, its performance can no longer be guaranteed, eventually leading to fracture of the brush. To prevent this, make sure to replace BRUSH ASS’Y when replacing DRUM ASS’Y.
The replacement timing is about 1000 hours which is the same as that of DRUM ASS’Y.
As the worn debris is accepted by COVER, BRUSH (4-45), also be sure to remove the debris when replacing BRUSH ASS’Y.

11. BRUSH ASS'Y（4-33）の交換について

DA-98HRのドラムアースは、従来のDTRSのような接点式ではなく、スリップリングとブラシの摺動によっています。従って、BRUSH ASS'Y（4-33）の使用時間が限度を超えると磨耗により性能が保証できなくなり、最終的には切断してしまいます。そこで、ドラムASS'Y交換時には、必ずこのBRUSH ASS'Yの交換を行ってください。
交換周期は、ドラムASS'Y交換周期と同じ約1000時間です。
また、磨耗粉をCOVER, BRUSH（4-45）で受けるようになっていますので、BRUSH ASS'Y交換の際は磨耗粉の除去も行ってください。

4. MECHANISM ADJUSTMENTS
機構部調整



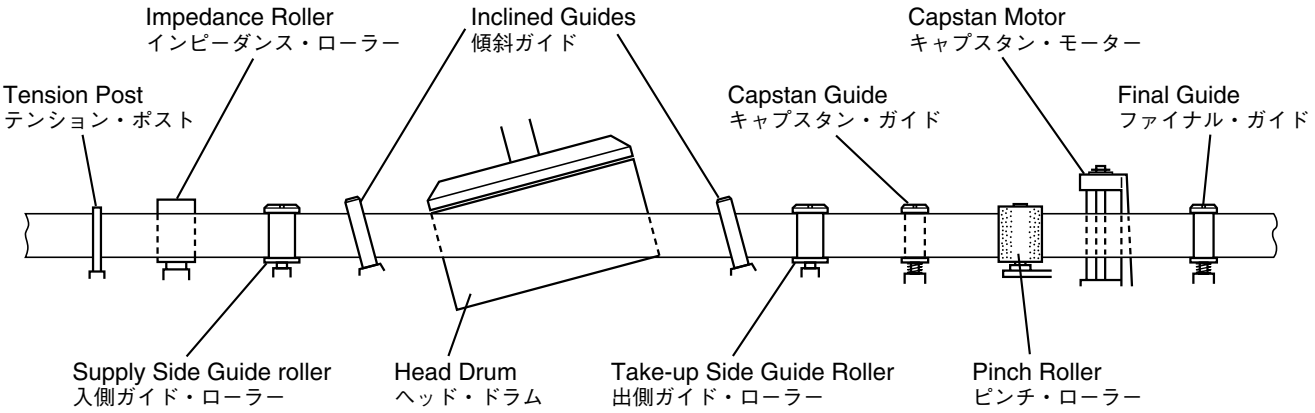


Fig. 4-1

4-1. Preparation

1. Cleaning the head drum (See Fig. 4-2)
   Press a cloth moistened with alcohol against the surface of the head drum, and clean the drum by turning it counter-clockwise with the fingers.
   Notes)
   - To turn the drum, insert a clip (or other appropriate piece) into the hole (ϕ1) in the drum shaft, and turn the clip, as shown in the figure.
   - When cleaning the head drum, be careful not to damage the head chip. It might be damaged if you apply a longitudinal force to it or turn it clockwise.
   - After cleaning the head drum, use a dry cloth to wipe off any residual alcohol (because when it vaporizes, condensation could occur). The tape would stick to the drum if its surface is wet, causing damage to the tape.

4-1. 準備

1. ヘッドドラムのクリーニング（図4-2参照）
   ヘッドドラムの表面にアルコールで浸した布をあて、ドラムを反時計方向に指で回してクリーニングする。
   注）
   - ドラムは、図のようにシャフトの穴（ϕ1）にクリップ等を差し込み、それを回すことにより回ります。
   - クリーニングするとき、ヘッドチップを破損しないように充分注意すること。ヘッドチップの上下方向に力を加えたり、ドラムを時計方向に回すと破損の可能性があります。
   - アルコールでクリーニングした場合は、アルコールが充分乾燥してからテープをローディングしてください。アルコールでクリーニングした後、乾いた布で乾拭きすることをお勧めします。（アルコールの気化時に結露が発生する可能性があるため）
     ドラム表面が濡れていると、ドラムにテープがはりつきテープダメージの原因となります。

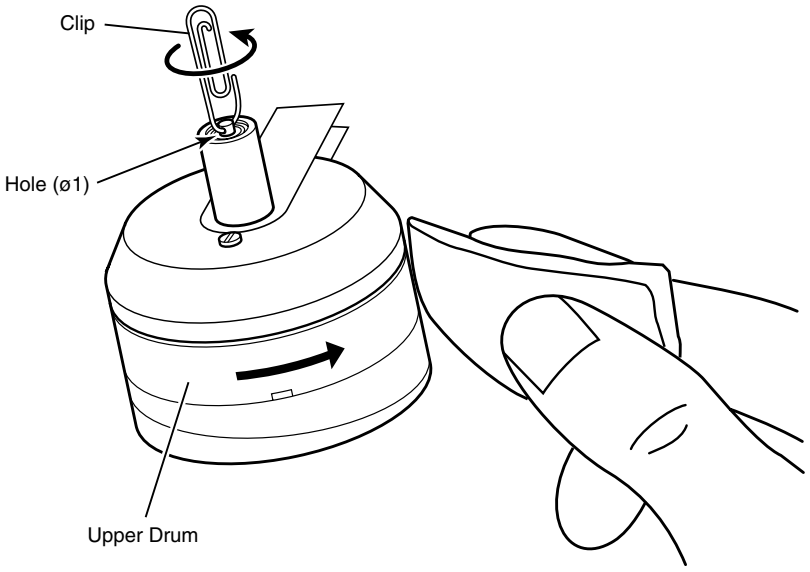


Fig. 4-2

2. Connecting the oscilloscope
   Connect CH1 of the oscilloscope to TP3 (RF A-HEAD) or TP4 (RF B-HEAD) on the RF PLAY PCB and CH2 to TP601 (SWP) on the SYS PCB. (See Fig. 5-1)

2. オシロスコープの接続
   オシロスコープのCH1をRF PLAY PCBのTP3（RF A-HEAD）またはTP4（RF B-HEAD）に、CH2をSYS PCBのTP601（SWP）に接続する。（図5-1参照）

4-2. Test tape

1. TEAC MTT-86131 : For adjusting the torque
2. TEAC MTT-88101(Fs=44.1 kHz):
   For adjusting the error rate and the RF level

4-2. テストテープ

1. TEAC MTT-86131 : トルク調整用
2. TEAC MTT-88101（Fs=44.1 kHz）:
   エラーレート、RFレベル調整用

4-3. Adjusting the tension arm position

1. Load a torque cassette MTT-86131, then set the DA-98HR to PLAY mode.
2. Using a Phillips screwdriver, turn adjust screw A (Fig. 4-3), then align the center of the semicircular portion of the tension arm to the guide rail edge.
   This should fall within range A to C (see Fig. 4-3).

4-4. Adjusting the torque

1. Load a torque cassette MTT-86131, then set the DA-98HR to PLAY mode.
2. Confirming the FWD back tension
   1) Read the torque value at the supply-reel (white) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard value: 10 to 12 g.cm
      Fluctuation range: 3 g.cm or less
   2) If the standard value is not satisfied, remove the torque cassette, loosen screws B (two) in Fig. 4-3 and adjust by moving the protector plate to the left and right. If moved to the left, the torque is reduced, whereas if moved to the right, it increases.
   3) Repeat 1 to 3 until the values fall within the standard.

4-3. テンションアーム位置調整

1. トルクカセットMTT-86131を装着し、PLAYモードにする。
2. プラスドライバーで調整ネジA（図4-3）を回し、テンションアームの半月部の中心をガイドレールエッジに合わせる。
   変動はA ～ Cの範囲であること。（図4-3参照）

4-4. トルク調整

1. トルクカセットMTT-86131を装着し、PLAYモードにする。
2. FWDバックテンションの確認
   1）サプライリール台（白）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。
      規格値: 10 ～ 12 g･cm
      変動幅: 3 g･cm以下
   2）もし規定値を満足しないときは、トルクカセットを外し、図4-3のネジB 2本を緩めプロテクタプレートを左右に動かして調整する。左に動かすとトルクが弱くなり、右に動かすと強くなります。
   3）1～3項を規格に入るまで繰り返す。

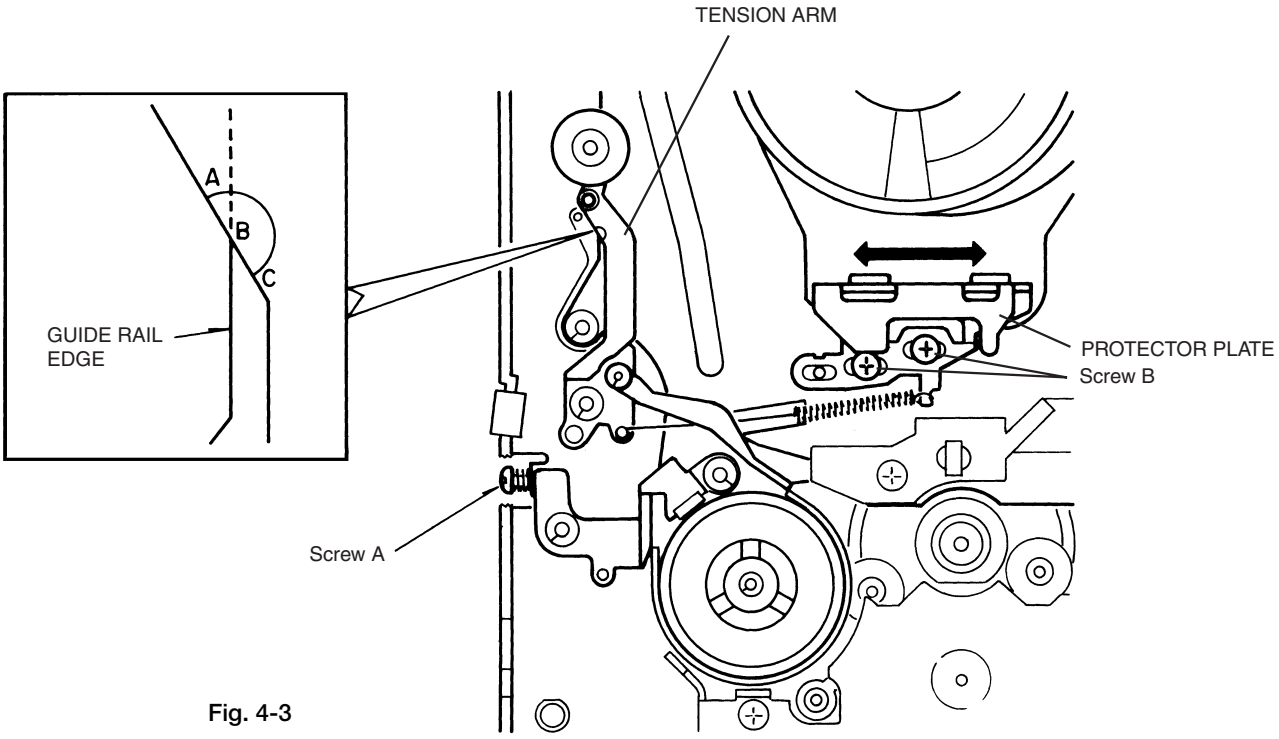


Fig. 4-3

3. Confirming the take-up torque of the take-up reel
   1) Read the torque value at the take-up reel (black) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard value: 8 to 15 g·cm
      Fluctuation value: 3 g·cm or less
   2) If the standard value is not satisfied, remove the torque cassette, replace the take-up reel table (black), and repeat 1 to 4 until the values fall within the standard.
      Note)
      When reinstalling, be sure not to forget to reinstall the cut washer.
4. Confirming the REV take-up torque
   1) Press the SHUTTLE switch, then turn the SHUTTLE knob to the left. Read the torque value at the supply-reel (white) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard range: 18 to 28 g·cm
      Fluctuation range: 3 g·cm or less
   2) If the standard value is not satisfied, remove the torque cassette, replace the supply-reel table (white), and repeat 1 to 5 until the values fall within the standard.
      Note)
      When reinstalling, be sure not to forget to reinstall the cut washer.
   3) Read the torque value at the take-up reel (black) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard range: 8 to 25 g·cm
      Fluctuation range: 3 g·cm or less

＊Cautions when replacing the reel table

When removing the supply-reel table or take-up reel table, the disk reflector (4-3 on page 51) beneath the reel table may also be disengaged as well.

In such a case, see that the polyethylene slider washer (4-55 on page 51) remains on the reel table shaft (mechanism chassis) without fail.

If the disk reflector is affixed over the reel table shaft with the polyethylene slider washer stuck on the backside of the disk reflector, the polyethylene slider washer may NOT fit over the reel table shaft but enter the mechanism chassis.

4-5. Adjusting the tape travel

When adjusting the height of each roller guide, be sure to slightly loosen the screws securing the guide beforehand.

After adjustment is complete, tighten the screws using a torque driver. Observe a tightening torque of 200 g·cm.

Torque driver: 0.2 to 1.5 kg; parts No. 5772827800

(Torque driver bit: M2 (+); parts No. 5772828000)

3. テイクアップリール巻取りトルクの確認
   1）テイクアップリール台（黒）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。

      規定値：8 〜15 g・cm
      変動幅：3 g・cm以下

   2）もし規定値を満足しないときは、トルクカセットを外し、テイクアップリール台（黒）を交換し、1〜4項を規格に入るまで繰り返す。
      注）取付け時、カットワッシャーの取付を忘れないこと。
4. REV巻取りトルクの確認
   1）SHUTTLEキーを押し、SHUTTLEノブを左に回す。そのときのサプライリール台（白）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。

      規定値: 18 〜 28 g・cm
      変動幅: 3 g・cm以下

   2）もし規定値を満足しないときは、トルクカセットを外し、サプライリール台（白）を交換し、1〜5項を規格に入るまで繰り返す。
      注）取付け時、カットワッシャーの取付を忘れないこと。
   3）テイクアップリール台（黒）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。

      規格値: 8 〜 25g・cm
      変動幅: 3 g・cm以下

＊リール台交換時の注意

サプライリール台またはテイクアップリール台を外すとき、リール台の下のディスクリフレクタ（51ページ 4-3）が一緒に外れることがあります。

その場合は、必ずポリスライダワッシャ(51ページ 4-55)がリール台軸（メカシャーシ）に残っていることを確認してください。

ディスクリフレクタの裏側にポリスライダワッシャがついたまま、リール台軸にディスクリフレクタを挿入すると、ポリスライダワッシャがリール台軸に挿入されずメカシャーシに混入してしまうおそれがあります。

4-5. テープ走行調整

各回転ガイドの高さを調整する場合は、必ず回転ガイドを止めているネジを少し緩めてから行ってください。

調整後は、そのネジをトルクドライバーにより締め付けること。締め付けトルクは、200g・cm厳守のこと。

トルクドライバー 0.2〜1.5kg : 品番 5772827800

（トルクドライバー用ビット M2（＋）: 品番 5772828000）

1. Load the test tape MTT-88101, then set the DA-98HR to PLAY mode.
2. While observing the A-HEAD waveform using the oscilloscope, fine-adjust the heights of the roller guides at the supply side and take-up side of the drum using a wrench, so that the leading and trailing edges of the RF waveform have virtually the same level as that of the peak portion on the center of the waveform. (See Fig. 4-4)

   Note)

   Be careful not to hold down the roller guide at the supply side too much by way of making the leading edge of the RF waveform flat. Otherwise, it may lead to rounding of the RF waveform during REV mode.
3. So that the tape travels on the lower edge of the capstan guide, adjust the height of the capstan guide.

   The adjustment method is as follows:

   1) Turn the adjustment screw counterclockwise to raise the lower flange.
   2) If tape is curled, turn the screw clockwise to lower the lower flange. Stop turning the screw when the tape curl dissolves.

   Notes)

   - It is acceptable in principle if the tape is confirmed to be free from curl at the lower edge of the guide.
   - Prior to adjustment, be sure to dissolve the screw-locking compound applied to the head of the guide using alcohol. After the adjustment is complete, reapply screw-locking compound.
4. Adjust the height of the final guide so that the tape is free from curl between the take-up side of the capstan and the final guide, and that the tape is NOT curled by the upper and lower edges of the final guide.

   Notes)

   - It is acceptable in principle if confirmation is made only.
   - Prior to adjustment, be sure to dissolve the screw-locking compound applied to the head of the guide using alcohol. After the adjustment is complete, reapply screw-locking compound.

1. テストテープ MTT-88101を装着し、PLAYモードにする。
2. オシロスコープでA-HEADの波形を観測しながらドラム入口、出口の回転ガイドの高さを二股レンチにより調整し、RF波形の入口、出口が中央の最大部分とほぼ同じ高さ（フラット）になるように（図4-4）、ドラム入口、出口の回転ガイドの高さを微調整する。

   注）RF波形の入口側をフラットにするために入口の回転ガイドを押さえすぎないこと。REV時のRF波形のつぶれの原因となります。

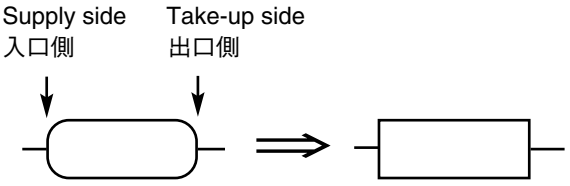


Fig. 4-4

3. キャプスタンガイドの下エッジをテープが走行するように、キャプスタンガイドの高さを調整する。

   調整方法は以下の通り。

   1）下フランジを一度上に上げるように調整ネジを左に回す。
   2）テープのカールが確認できたらネジを右に回して下フランジを下げてゆき、テープのカールがなくなった時点で調整を止める。

   注）調整する場合は、必ずガイド頭部のネジロックをアルコールで溶かしてから行ってください。
   調整後は、必ずネジロックをすること。
4. キャプスタン出口からファイナルガイドの間でテープのよじれがなく、またファイナルガイドの上下エッジでテープがカールしないように、ファイナルガイドの高さを調整する。

   注）
   - 原則は確認のみでOKです。
   - 調整する場合は、必ずガイド頭部のネジロックをアルコールで溶かしてから行ってください。
     調整後は、必ずネジロックをすること。

5. Linearity check
   1) Set the unit to the VTR mode (☞ page 7).
   2) When the unit is in the VTR mode, the level fluctuates spontaneously.
      At this time, check that the shape of the waveform remains consistent while the level is changes.
      If it doesn't, fine-adjust the guide rollers located at the entrance and exit of the drum.
      If the level stops varying, set the unit to the track-off mode so that the level continues to vary. (see below.)

   (How to Set the Track-Off Mode)
   ① Set the unit to the VTR mode.
   ② Select the menu group M in the menu screen, then press ENTER key.
   ③ Move the cursor to "Track Off" and press ENTER key. (The display shows "Track off Mode : off".)
   ④ Press the ▲ key to change the "off" to "manual +0.0".
   ⑤ Press the ▶ key. ("+0.0" will start blinking.)
   ⑥ Using the ▲ and ▼keys, change the display within the limits of from -0.5 to +0.5.

6. Final checking of each guide
   1) Confirm that the upper edge travel regulation is observed for the roller guide at the supply side of the drum.
   2) Confirm that the upper edge travel regulation is observed for the roller guide at the take-up side of the drum.
      Note)
      - Gently push the head of the roller guides at the supply side and the take-up side of the drum in the direction of the rear of the mechanism using a bamboo skewer, then confirm that the waveform in 2 will resume soon (within one second) when the bamboo skewer is released. If the waveform does NOT quickly resume, upper edge tape travel regulation is roughly made; fine-adjustment is necessary.
      - If dirt is adhered to the roller guides, the level will fluctuate while they turn.
        In such a case, moisten a cotton swab with alcohol, and clean the roller guides.
   3) Confirm the lower edge travel regulation for the capstan guide.
      Note) Play an ME tape and make adjustments as described in item 3 on page 30, then check again.
   4) Confirm the upper and lower edge travel regulation for the final guide (the tape should be free from curl).

5. 直線性の確認
   1）VTRモードにする。（☞ 7ページ）
   2）VTRモードにすると、レベルがかってに大きくなったり小さくなったりします。このときの波形が形を変えずにレベルだけが大小することを確認する。そうでない場合は、ドラム入口、出口の回転ガイドを微調整する。
      もし、レベルが大小を繰り返さないようならば、以下の方法でトラックオフさせるとレベルが変化するよになります。

   （トラックオフのさせ方）
   ① VTRモードにする。
   ② メニュー画面で、メニューグループMを選択し、ENTERキーを押す。
   ③ “Track Off”にカーソルを合わせて ENTERキーを押す。（Track off Mode : off 表示）
   ④ ▲キーを押す。（off → manual +0.0 表示）
   ⑤ ▶キーを押す。（+0.0 点滅）
   ⑥ ▲または▼キーにより、表示を－0.5 ～ ＋0.5の範囲で変化させる。

6. 各ガイドの最終チェック
   1）ドラム入口回転ガイドの上エッジ走行規制を確認する。
   2）ドラム出口回転ガイドの上エッジ走行規制を確認する。
   注）● 入口回転ガイドおよび出口回転ガイドの上部をメカ後部方向に竹串で軽く押し、竹串を離したとき、すぐ（1秒以内）に2項の波形に戻ることを確認する。波形がすぐに戻らない場合は、上エッジテープ走行規制が甘いので微調整する必要があります。
      ● 回転ガイドにゴミが付着しているとガイド回転時にレベル変動を生じます。この場合は、綿棒にアルコール塗布し、回転ガイドをクリーニングしてください。
   3）キャプスタン部ガイドの下エッジ走行規制を確認する。
      注）MEテープを走行させ、30ページの3項の調整を再度行って確認する。
   4）ファイナルガイドの上下エッジ走行規制（テープのカールが無いこと）を確認する。

4-6. Confirming the travel in F.FWD, REW and REV modes

1. In all modes, including F.FWD, REW and REV/SHUTTLE, confirm that the tape is free from damage at each guide.
   Note)
   - If, in F.FWD mode, the impedance roller generates a strange noise, replace it.
   - If the leading edge of the playback RF waveform is slow to rise up (the waveform gradually increases in level), or the tape curl is excessive during reverse mode, choose a polyethylene slider washer (beneath the impedance roller) from the following three washers and adjust the height of the impedance roller.
     - 0.13 mm(P/N M00221900A)
     - 0.20 mm(P/N M00222000A)
     - 0.25 mm(P/N M00222100A)
     - No washer

     Observe a screw tightening torque of 500 g·cm.
     Torque driver: 0.2 to 1.5 kg; parts No. 5772827800
     (Torque driver bit: M2 (+); parts No. 5772828000)
2. Load the test tape MTT-88101, then confirm the counter indication in F.FWD and REW modes from the beginning to the end of the tape. See that the counter indication is not a continuous bar indication "---". (Momentary bar indication is acceptable.)

   In the case of a continuous bar indication, refer to the following:

4-6. FF, REW, REVモードでの走行確認

1. FFモード、REWモード、REV/SHUTTLEモードなどすべてのモードで、各ガイドでのテープダメージが無いことを確認する。
   注）● FF時、インピーダンスローラーの回転異音がある場合は交換する。
   ● 再生RF波形の立ち上りが遅い（波形が徐々に大きくなる）場合や、リバース時にテープのカールが著しい場合は、インピーダンスローラーの下に敷いてあるポリスライダワッシャを次の4種類のうちから選択し、インピーダンスローラーの高さを調整する。

     ・0.13mm(品番M00221900A)
     ・0.20mm(品番M00222000A)
     ・0.25mm(品番M00222100A)
     ・ワッシャ無し

     ネジの締め付けトルクは、500g·cm 厳守のこと。
     トルクドライバー 0.2～1.5kg：品番5772827800
     （トルクドライバー用ビットM2（+）：品番5772828000）
2. テストテープ MTT-88101を装着して、FFおよび REWをテープの巻始めから巻終りまで通してカウンタ表示を確認する。カウンタ表示が連続してバー表示“---"にならないことを確認する。（一瞬のバー表示はOKです）連続してバー表示がでる場合は、以下を参照してください。

① Fig. 4-5 shows the normal RF waveform (for both A-HEAD and B-HEAD) in F.FWD or REW mode (reel speed:100 times).

② Fig. 4-6 shows the RF waveform in which the indication will result in a bar indication in 1 mode (the ABS time CANNOT be read due to a missing or distorted waveform).

In such a case, the following measures are required:

- If the waveform is as in Fig. 4-6 in F.FWD mode, replace the soft brake (3-18 on page 49) or coil spring (3-17 on page 49) at the supply reel side.
- If the waveform is as in Fig. 4-6 in REW mode, replace the soft brake (3-18 on page 49) or torsion spring (3-19 on page 49) at the take-up reel side.

③ Fig. 4-7 shows the normal RF waveform in REV mode (capstan feed).

④ Fig. 4-8 shows the RF waveform in which the indication will result in a bar indication in 3 mode (the ABS time CANNOT be read due to a missing or distorted waveform).

In such a case, the following causes are conceivable:

- The roller guide at the supply side of the drum is held down too much. The roller guide needs readjustment.
- The REV take-up torque at the supply reel pad is low. It should be replaced with a reel table with a REV take-up torque of approx. 30 g.cm.

① 図4-5は、FFまたはREWモード（リール送り, 100倍速）時のRF通常波形（A-HEAD, B-HEADとも）です。

② 図4-6は、①のモード時にバー表示（ABSタイムが読めない）になってしまう場合（波形抜けまたは波形つぶれ）のRF波形です。

この場合は、下記の処置が必要です。

- FF時に図4-6の波形になる場合は、サプライリール台側のSOFT BRAKE LEVER ASS'Y（49ページ 3-18）またはCOIL SPRING（49ページ 3-17）を交換してください。
- REW時に図4-6の波形になる場合は、テイクアップリール台側のSOFT BRAKE LEVER ASS'Y（49ページ 3-18）またはTORSION SPRING（49ページ 3-19）を交換してください。

③ 図4-7は、REVモード（キャプスタン送り）時のRF通常波形です。

④ 図4-8は、③ のモード時にバー表示（ABSタイムが読めない）になってしまう場合（波形抜けまたは波形つぶれ）のRF波形です。

この場合は、下記の原因が考えられます。

- ドラム入口の回転ガイドの押さえすぎ。回転ガイドの再調整が必要です。
- サプライリール台のREV巻取りトルクが弱い。REV巻取りトルクが、30g.cm前後のリール台と交換が必要です。

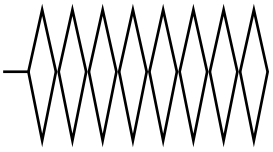


Fig. 4-5

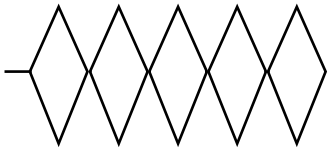
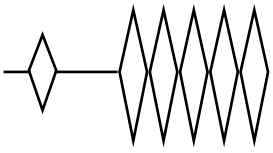


Fig. 4-7



or

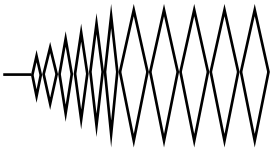
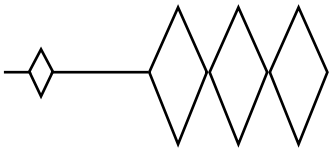


Fig. 4-6



or

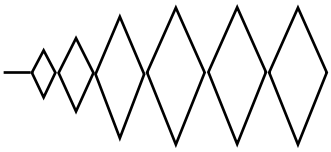


Fig. 4-8

＊ Cautions when replacing the drum

When the drum is replaced, be sure to confirm and adjust the following items other than tape travel adjustments.
As for adjustment methods, refer to 5 (ELECTRICAL ADJUSTMENTS):

- Adjustment of the P.G. (phase generator) position
- Playback error rate (MP tape and ME tape)
- Adjustment of the recording current
- R/P error rate (MP tape and ME tape)

Be also sure to replace BRUSH ASS'Y when replacing the drum. (☞ page 25)

＊ドラム交換時の注意

ドラムを交換した場合は、テープ走行調整以外に下記項目の確認・調整を必ず行ってください。
調整方法については、5項（電気系調整）を参照してください。

・P.G.（PHASE GENERATOR）位置調整
・再生エラーレート（MPテープおよびMEテープ）
・記録電流調整
・録再エラーレート（MPテープおよびMEテープ）

また、ドラム交換時には、必ずBRUSH ASS'Yの交換も行ってください。（☞ 25ページ）

5. ELECTRICAL ADJUSTMENTS

電気系調整

5-1. Check and adjustment points

5-1. 測定箇所および調整箇所

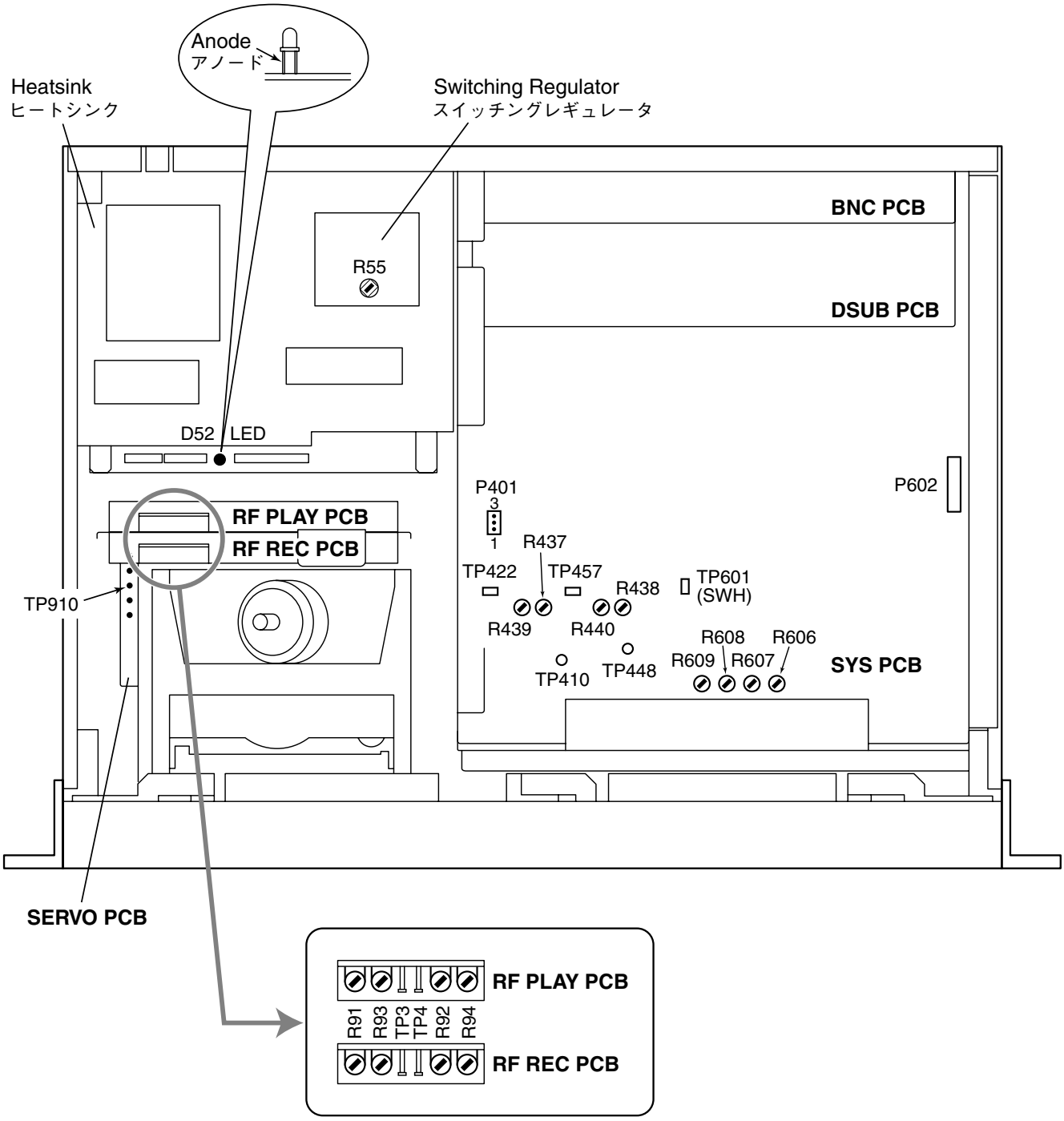


Fig. 5-1

5-2. Test tape

1. TEAC MTT-88101 (Fs=44.1 kHz):
   For adjusting the error rate and the RF level
2. TEAC MTT-88102 (Fs=48 kHz):
   For adjusting the error rate, the RF level,
   and the P.G. position
3. TEAC MTT-88201 : For recording (blank MP tape)
4. TEAC MTT-88202 : For recording (blank ME tape)

5-3. +5 V supply check

1. Connect a digital tester between the heat sink in the switching regulator and the anode of the LED for +5 V supply (D52).
2. Check that the DC voltage reading is +5.1 ± 0.1 V.
3. If voltage is not within these limits, adjust the semi-fixed resistor R55 until correct.

5-4. P.G. (Phase generator) position adjustment

1. Connect CH1 of the oscilloscope to TP410 (RF A-HEAD) on the SYS PCB and CH2 to TP910 (SWP) on the SERVO PCB.
2. Load the test tape MTT-88102.
3. Set the DA-98HR to test mode. (☞ page 7)
4. Select the menu group M in the menu screen.
5. Move the cursor to "PG.AdJuSt" and press ENTER key.
6. Enter the play mode and, using the ▲ and ▼ keys, adjust the lag between the fall of the switching pulse and the end of ATF portion of the RF wave for 250 µsec, as shown in Photo-1.
7. Press STOP, then switch power off to save the setting.
8. Switch on power again, then enter the play mode to check that the lag of 250 µsec is maintained.

5-2. テストテープ

1. TEAC MTT-88101（Fs=44.1 kHz）:
   エラーレート、RFレベル
2. TEAC MTT-88102（Fs=48 kHz）:
   エラーレート、RFレベル、記録位置調整用
3. TEAC MTT-88201 : 記録用MP生テープ（未記録）
4. TEAC MTT-88202 : 記録用ME生テープ（未記録）

5-3. 電源 +5Vの確認

1. スイッチングレギュレーター内のヒートシンクと＋5V用LED（D52）のアノード側間にデジタルテスターを接続する。
2. DC電圧が、＋5.1V±0.1Vであることを確認する。
3. 上記規格内に入っていない場合は、スイッチングレギュレーター内の半固定抵抗 R55で調整する。

5-4. PG（Phase Generator）位置調整

1. オシロスコープのCH1をSYS PCBのTP410（RF A-HEAD）に、CH2をSERVO PCBのTP910（SWP）に接続する。
2. テストテープ MTT-88102を装着する。
3. テストモードにする。（☞ 7ページ）
4. メニュー画面で、メニューグループMを選択する。
5. “PG AdJuSt”にカーソルを合わせ ENTERキーを押す。
6. PLAYモードにして、スイッチングパルスの立ち下がりからRF波形のATF部分の終わりまでが 250 μ secになるように、▲または▼キーを押して調整する。
   （写真-1参照）
7. STOP後、一度電源をOFFして値を記憶させる。
8. 再度電源をONにし、PLAYモードにして250 μ secが変化していないことを確認する。

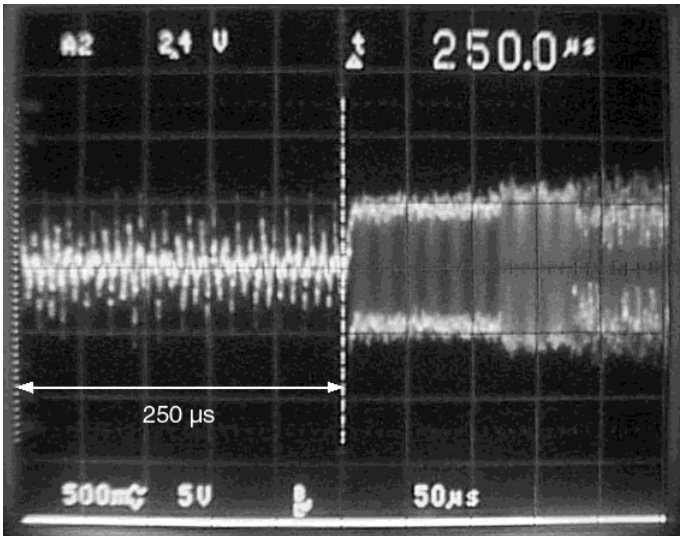


Photo-1

5-5. Offset adjustment in the VCO free-running frequency automatic compensation circuit

1. DTRS mode
   1) Play the MTT-88101 or MTT-88102 test tape.
   2) Short-circuit P401's 1 and 2 on the SYS PCB (A-HEAD placed in test condition).
   3) Connect an oscilloscope to TP422 on the SYS PCB, and adjust the scope range to 1V DC, 0.5 µsec.
   4) Adjust R439 (A-HEAD) on the SYS PCB for 2.5 V DC at TP422.
   5) In a similar way, short-circuit P401's 2 and 3 (B-HEAD placed in test condition), then adjust R440 (B-HEAD) for 2.5 V DC at TP457.
   6) After adjustment is complete, release P401.

   Note)
   In 4) and 5), even if a positive-going or negative-going slight glitch is observed as shown in Fig. 5-2, it should be acceptable. However, perform adjustment to alleviate glitches as much as possible.

5-5. VCOフリーラン周波数自動補正回路のオフセット調整

1. DTRSモード
   1）テストテープ MTT-88101または MTT-88102を再生する。
   2）SYS PCBのP401の1-2間をショートする。
   （A-HEAD テスト状態）
   3）SYS PCBのTP422にオシロスコープを接続し、オシロスコープのレンジをDC 1V, 0.5 μ secにセットする。
   4）TP422のDC電圧が 2.5VになるようにSYS PCBのR439（A-HEAD）を調整する。
   5）同様に、P401の2-3間をショートし（B-HEAD テスト状態)、TP457のDC電圧が 2.5VになるようにR440（B-HEAD）を調整する。
   6）調整後、P401を解放する。

   注）4), 5) 項でオシロスコープの波形が、図5-2のように上または下方向に若干のヒゲが観測されても可とするが、なるべくひげを小さくするように調整する。

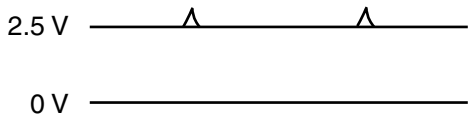


Fig. 5-2

2. HR mode
   1) Play a tape recorded in HR mode.
   2) Short-circuit P401's 1 and 2 on the SYS PCB (A-HEAD placed in test condition).
   3) Connect an oscilloscope to TP422 on the SYS PCB, and adjust the scope range to 1V DC, 0.5 µsec.
   4) Adjust R437 (A-HEAD) on the SYS PCB for 2.5 V DC at TP422.
   5) In a similar way, short-circuit P401's 2 and 3 (B-HEAD placed in test condition), then adjust R438 (B-HEAD) for 2.5 V DC at TP457.
   6) After adjustment is complete, release P401.

2. HRモード
   1）HRモードで記録したテープを再生する。
   2）SYS PCBのP401の1-2間をショートする。
   （A-HEAD テスト状態）
   3）SYS PCBのTP422にオシロスコープを接続し、オシロスコープのレンジをDC 1V, 0.5 μ secにセットする。
   4）TP422のDC電圧が 2.5VになるようにSYS PCBのR437（A-HEAD）を調整する。
   5）同様に、P401の2-3間をショートし（B-HEAD テスト状態)、TP457のDC電圧が 2.5VになるようにR438（B-HEAD）を調整する。
   6）調整後、P401を解放する。

5-6. Playback equalizer adjustment

5-6-1. Checks in Normal mode

1. ME tape
   1) Load Sony ME tape.
   2) Connect the oscilloscope to TP3 (RF A-HEAD) on the RF PLAY PCB , then set the oscilloscope range to 500 mV AC, 50 nsec.
   3) Set REC FUNCTION ON (All channels) and execute format recording in HR mode.
   4) Rewind and play the tape, and observe the eye pattern of A-HEAD.
   5) Adjust R91 on RF PLAY PCB so that the 3.1 MHz waveform is almost flat at top and bottom as shown in Photo-3.
      * Photo-2 shows the eye pattern when the oscilloscope is set to the 50 nsec/div. range.
      * Photo-3 shows the eye pattern when the oscilloscope is set to the 100 nsec/div. range.
   6) Similarly, connect the oscilloscope to TP4 (RF B-HEAD) on the RF PLAY PCB, then observe the eye pattern of B-HEAD.
      For adjustment, use R92 on the RF PLAY PCB.

2. MP tape
   1) Load Sony MP tape.
   2) In the same way as in 1 (adjusting the equalizer using an ME tape), adjust R93 (A-HEAD) and R94 (B-HEAD) on the RF PLAY PCB.

5-6-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-6-1. (The same check, but test points and adjustments not on RF PLAY PCB, but on RF REC PCB.)

5-6. 再生イコライザー調整

5-6-1. ノーマルモードでの確認

1. MEテープ
   1）SONY MEテープを装着する。
   2）RF PLAY PCBのTP3（RF A-HEAD）にオシロスコープを接続し、オシロスコープのレンジを AC 500mV, 50nsecにする。
   3）REC FUNCTION ON（全ch）にし、HRモードでFORMAT記録する。
   4）巻戻して再生したときの A-HEADのアイパターンを観測する。
   5）写真-3のように 3.1MHzの波形の凸凹がほぼフラットになるように RF PLAY PCBの R91を調整する。
      ＊写真-2は、オシロスコープレンジが 50nsec/divの状態です。
      ＊写真-3は、オシロスコープレンジが 100nsec/divの状態です。
   6）RF PLAY PCBの TP4（RF B-HEAD）にオシロスコープを接続し、同様にB-HEADのアイパターンを観測する。
      調整は、RF PLAY PCBの R92で行う。

2. MPテープ
   1）SONY MP テープを装着する。
   2）1項（MEテープ イコライザー調整）と同様の方法で RF PLAY PCBの R93（A-HEAD）, R94（B-HEAD）を調整する。

5-6-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-6-1項と同様の確認を行う。（但し、テストポイント、調整箇所はRF PLAY PCBではなくてRF REC PCBとなります。）

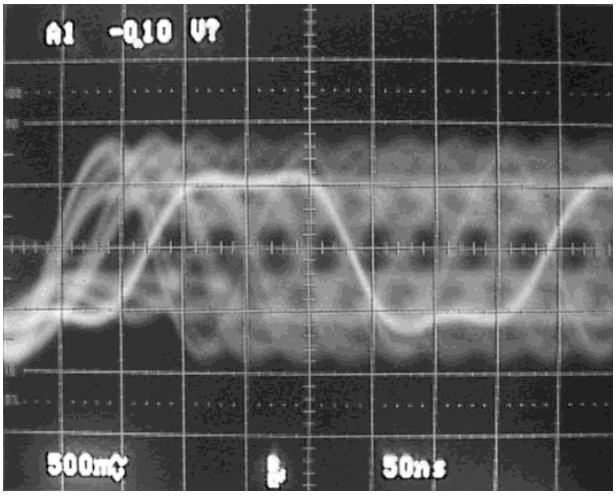


Photo-2. eye pattern (50 nsec/div)

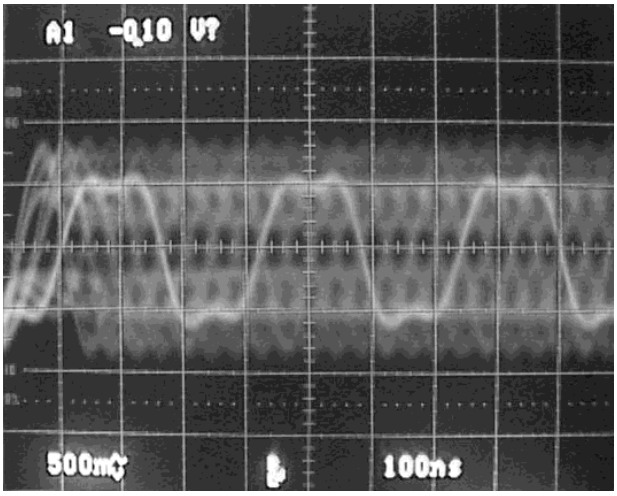


Photo-3. eye pattern (100 nsec/div)

5-7. RF level check

5-7-1. Checks in Normal mode

1. Connect the oscilloscope's CH1 to TP3 (RF A-HEAD) on the RF PLAY PCB and CH2 to TP601 (SWH) on the SYS PCB.
2. Set the oscilloscope's CH1 range to 500 mV AC, 2 msec.
3. Set the oscilloscope's CH2 range to 5 V DC, and (-) trigger.
4. Play the test tape MTT-88101.
5. Observe the waveform at TP3 (RF A-HEAD) , and see that the following standard is satisfied.

   Standard value (see Fig. 5-3):
   B, C (minimum) : 1000 mV or more
   B/A, C/A : 80 % or more

5-7. RFレベル確認

5-7-1. ノーマルモードでの確認

1. オシロスコープのCH1をRF PLAY PCBのTP3（RF A-HEAD）に、CH2をSYS PCBのTP601（SWH）に接続する。
2. オシロスコープの CH1のレンジをAC 500mV, 2msecにセットする。
3. オシロスコープの CH2のレンジをDC 5Vにセットし、（−）トリガーとする。
4. テストテープ MTT-88101を再生する。
5. TP3（RF A-HEAD）の波形を観測し、下記の規格値を満足すること。

   規格値（図5-3参照）
   B, C（最小部）: 1000mV以上
   B/A, C/A　　: 80%以上

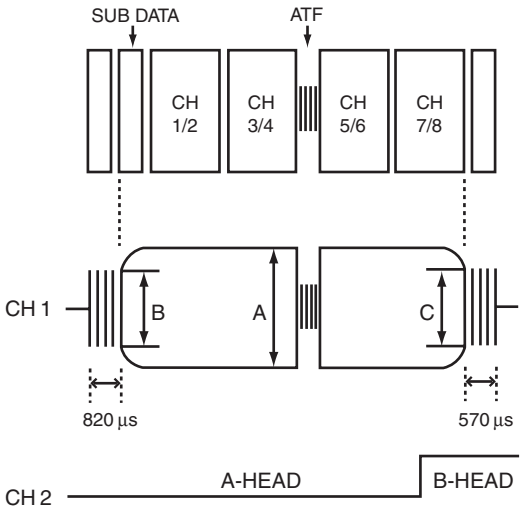


Fig. 5-3

6. Next, set the oscilloscope's CH2 to (+) triggering.
7. Connect the oscilloscope's CH1 to TP4 (RF B-HEAD) on the RF PLAY PCB, then observe the B-HEAD waveform, see that the standard is satisfied:

5-7-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-7-1.

6. 次にオシロスコープのCH2を（+）トリガーにセットする。
7. オシロスコープのCH1をRF PLAY PCBのTP4（RF B-HEAD）に接続して B-HEADの波形を観測し、A-HEADと同様に規格値を満足すること。

5-7-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-7-1項と同様の確認を行う。

5-8. Playback error rate check

5-8-1. Checks in Normal mode

1. ME tape
   1) As shown in Fig. 5-4, connect the ERC-88 error rate counter (P/N:5772926600) to P602 on the SYS PCB via the ERC-78HR adaptor (P/N:V00089100A).
      Note) To supply power to the ERC-88, use the PS-P2 AC adaptor.
   2) Play the MTT-88102 test tape, and check error rate (for both A- and B-HEADS).
      If error rate is out of the following specifications, readjust R91 (A-HEAD) or R92 (B-HEAD) on the RF PLAY PCB. (see paragraph 5-6)

      Standard value : less than 200 x 10^{-4}

5-8. 再生エラーレート確認

5-8-1. ノーマルモードでの確認

1. MEテープ
   1）図5-4のように、SYS PCBのP602にアダプターERC-78HR（品番:V00089100A）を介してエラーレートカウンターERC-88（品番:5772926600）を接続する。
      注）ERC-88には、ACアダプター PS-P2より電源を供給してください。
   2）テストテープ MTT-88102を再生してエラーレート（A-HEAD, B-HEAD共）を確認する。
      エラーレートが下記規格を満足していない場合は、RF PLAY PCBの R91（A-HEAD）または R92（B-HEAD）を再調整する。（5-6項参照）

      規格値 : 200×10^{-4}以下

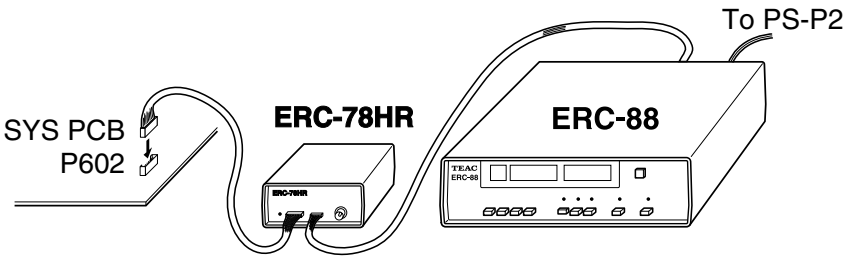


Fig. 5-4

2. MP tape
   Play the MTT-88101 test tape, and confirm the error rate (for both A- and B-HEADS) in the same way as with an ME tape.
   If error rate is out of the following specifications, readjust R93 (A-HEAD) or R94 (B-HEAD) on the RF PLAY PCB. (see paragraph 5-6)

   Standard value : less than 200 x 10^{-4}

2. MPテープ
   テストテ-プ MTT-88101を再生して、MEテープと同様にエラーレート（A-HEAD, B-HEAD共）を確認する。
   エラーレートが下記規格を満足していない場合は、RF PLAY PCBの R93（A-HEAD）または R94（B-HEAD）を再調整する。（5-6項参照）

   規格値 : 200×10^{-4}以下

5-8-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-8-1.

5-8-2. コンフィデンスモードでの確認

コンフフィデンスモードに切換えて、5-8-1項と同様の確認を行う。

5-9. Recording current adjustment

5-9-1. Checks in Normal mode

1. MP tape
   1) Load MP blank tape MTT-88201.
   2) As shown in the Fig. 5-5, connect the REC CURRENT KIT (P/N:V00024700A) between P10 on the MOTHER PCB and P102 on the RF REC PCB.
   3) Set the oscilloscope to 10 mV DC, 50 ns.
   4) Select the menu group 2 in the menu screen.
   5) Move the cursor to "Sine Osc" and press ENTER key.
   6) Press the ▲ key to display "Sine Oscillator 440".

5-9. 記録電流調整

5-9-1. ノーマルモードでの確認

1. MPテープ
   1）MP生テープ MTT-88201を装着する。
   2）図5-5の様に REC CURRENT KIT（品番V00024700A）をMOTHER PCBのP10とRF REC PCBの P102間に接続する。
   3）オシロスコープは、DC 10mV, 50nsに設定する。
   4）メニュー画面で、メニューグループ2を選択する。
   5）“Sine Osc”にカーソルを合わせ、ENTERキーを押す。
   6）▲キーを押して、“Sine Oscillator 440”表示にする。

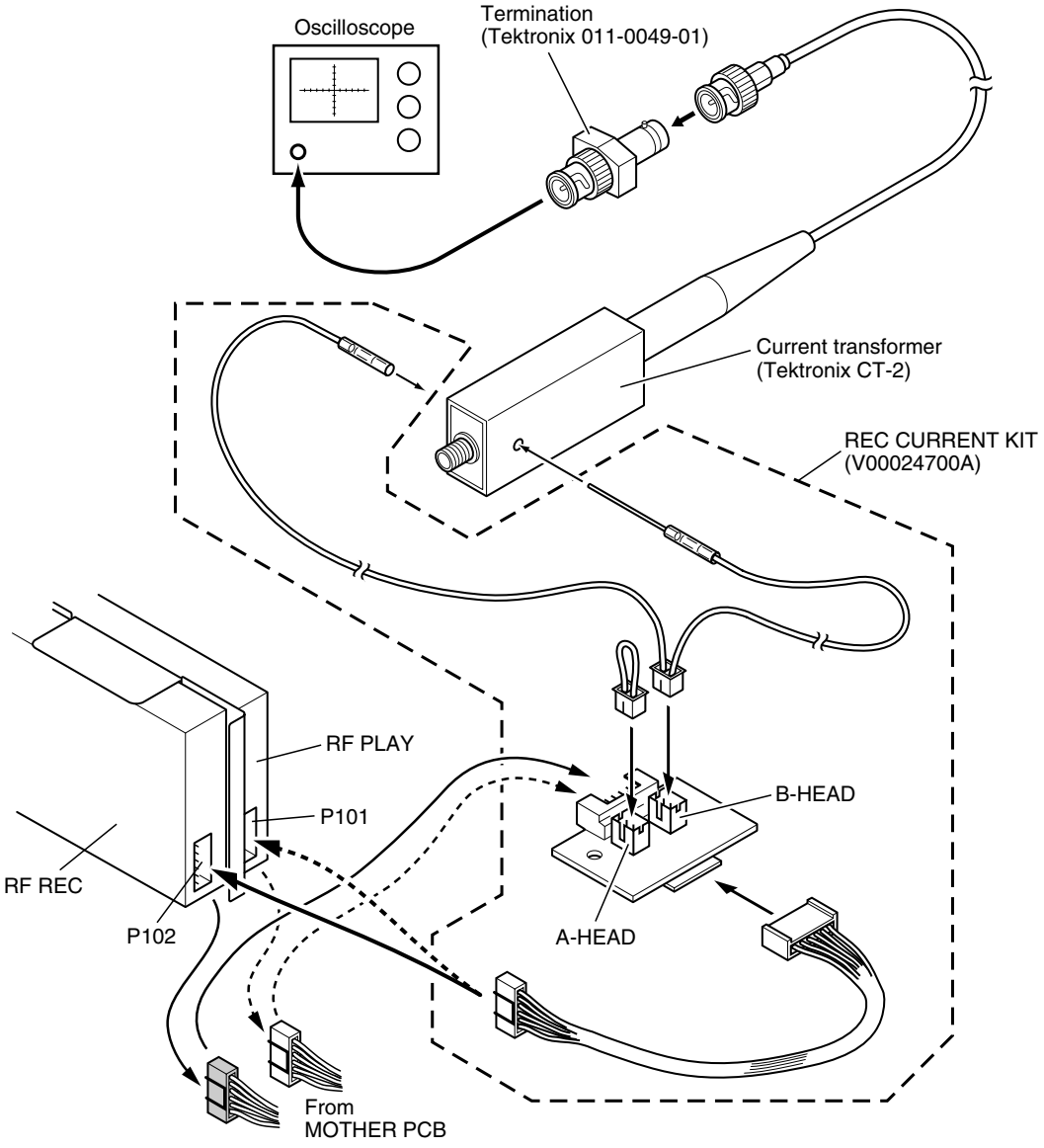


Fig. 5-5

7) Press the ESCAPE key.
8) Enter HR mode and set the REC FUNCTION keys of all channels to ON.
9) Start recording in tape format mode, and adjust R606 on the SYS PCB for 11.2 mAp-p (indication is in voltage) of A-HEAD current.
10) Similarly, adjust R607 for 11.2 mAp-p of B-HEAD current.

Note)
The state in which shorting pins A and B inserted as shown in Fig. 5-5 is one in which current flowing through the B-HEAD is to be measured. The state with shorting pins A and B reversed is one in which current flowing through the A-HEAD is to be measured. For a reference waveform using the oscilloscope, refer to Photo-4.

7）ESCAPEキーを押す。
8）HRモードにし、全CHのREC FUNCTIONキーをONにする。
9）FORMAT 記録状態で、A-HEADの電流値が 11.2 mAp-p（表示は電圧表示）になるようにSYS PCBのR606を調整する。
10）同様に、B-HEADの電流値が 11.2 mAp-pになるようにSYS PCBのR607を調整する。

注）図5-5の様に、ショートピンA, Bを差した状態がB-HEADの電流値測定の状態です。
ショートピンA, Bの差す位置を逆にした状態が、A-HEADの電流値測定の状態です。尚、オシロスコープの参考波形として、写真-4を参照してください。

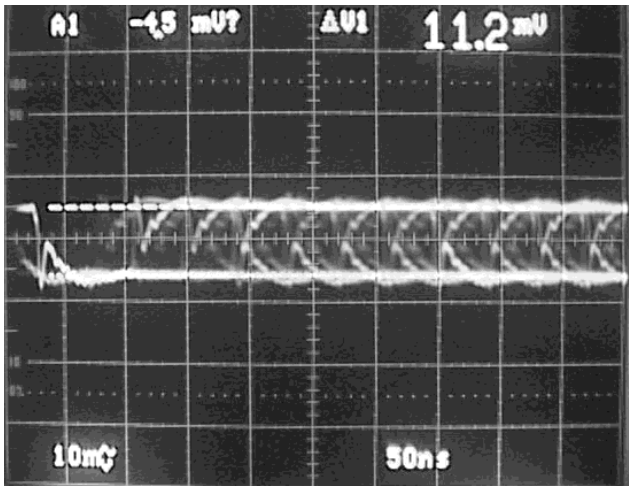


Photo-4

2. ME tape
Load ME blank tape MTT-88202 and check the current values at A-HEAD and B-HEAD in the same way as a MP tape. The current values should be 12.4 ± 0.6 mAp-p.

5-9-2. Checks in Confidence mode

1. Set the Confidence mode on, and connect the REC CURRENT KIT (P/N:V00024700A) between P9 on the MOTHER PCB and P101 on the RF REC PCB.
2. Perform the same check and adjustment as discussed in 5-9-1. Use R608 (A-HEAD) and R609 (B-HEAD) on SYS PCB for adjustment.

2. MEテープ
ME生テープ MTT-88202を装着し、MPテープと同様にA-HEAD, B-HEADの電流値を確認する。
電流値は 12.4±0.6 mAp-p であること。

5-9-2. コンフィデンスモードでの確認

1. コンフィデンスモードに切換え、REC CURRENT KIT（品番V00024700A）をMOTHER PCBのP9とRF PLAY PCBの P101間に接続する。
2. 5-9-1項と同様に確認、調整する。
調整は、SYS PCBのR608（A-HEAD）、R609（B-HEAD）で行う。

5-10. Recording/playback RF level check

5-10-1. Checks in Normal mode

1. After adjusting the recording current following section 5-9, rewind the tape section where format recording was executed in HR mode, and overwrite a signal on that section.
2. Rewind the tape section recorded in 1 above and play it.
3. In the same was as section 5-7, ensure that the RF level is 1200 mV minimum and that the waveform ratio is 80% minimum (with both ME and MP tapes).

5-10-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-10-1.

5-11. Recording/playback error rate check

5-11-1. Checks in Normal mode

Play back the recording you made as per instructions in paragraph 5-10, and check for less than 200 x 10^{-4} of error rate (with both ME and MP tapes).

5-11-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-11-1.

5-10. 記録再生RFレベル確認

5-10-1. ノーマルモードでの確認

1. 5-9項で記録電流調整後、HRモードで FORMAT記録した部分を巻き戻し、その部分にオーバーライト記録する。
2. 1項で記録した部分を巻き戻し、その部分を再生する。
3. 5-7項と同様に、RFレベルが 最小部で 1200mV以上、波形比 80%以上であることを確認する。
（ME, MPテープ共）

5-10-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-10-1項と同様の確認を行う。

5-11. 記録再生エラーレート確認

5-11-1. ノーマルモードでの確認

5-10項で記録した部分を再生する。
このときのエラーレートは、200×10^{-4}以下であること。
（ME, MPテープ共）

5-11-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-11-1項と同様の確認を行う。

PARTS LIST SECTION

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with ∗ require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in the manual.
- ⚠Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J]: JAPAN [US/C]: U.S.A./CANADA [E]: EUROPE [K]: KOREA
  [UK]: U.K. [A]: AUSTRALIA

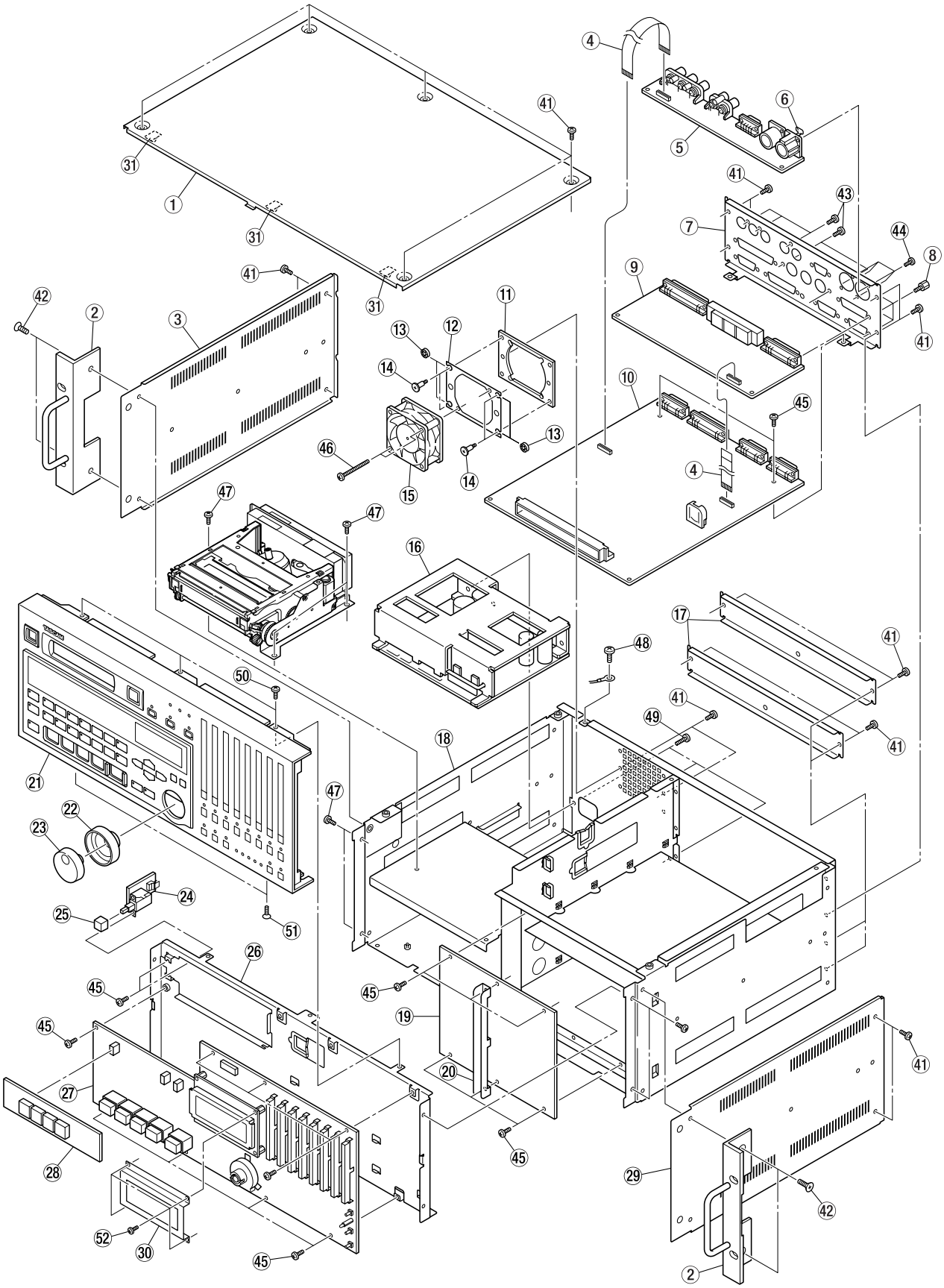
注 意

- プリント基板は部品面が示されています。
- ∗印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品及び品番のない部品は供給しません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠は安全重要部品です。
  交換する時は必ずティアック指定の部品を使用してください。
- 仕向先
  [J]: JAPAN [US/C]: U.S.A./CANADA [E]: EUROPE [K]: KOREA
  [UK]: U.K. [A]: AUSTRALIA

6. EXPLODED VIEWS AND PARTS LIST

分解図とパーツリスト

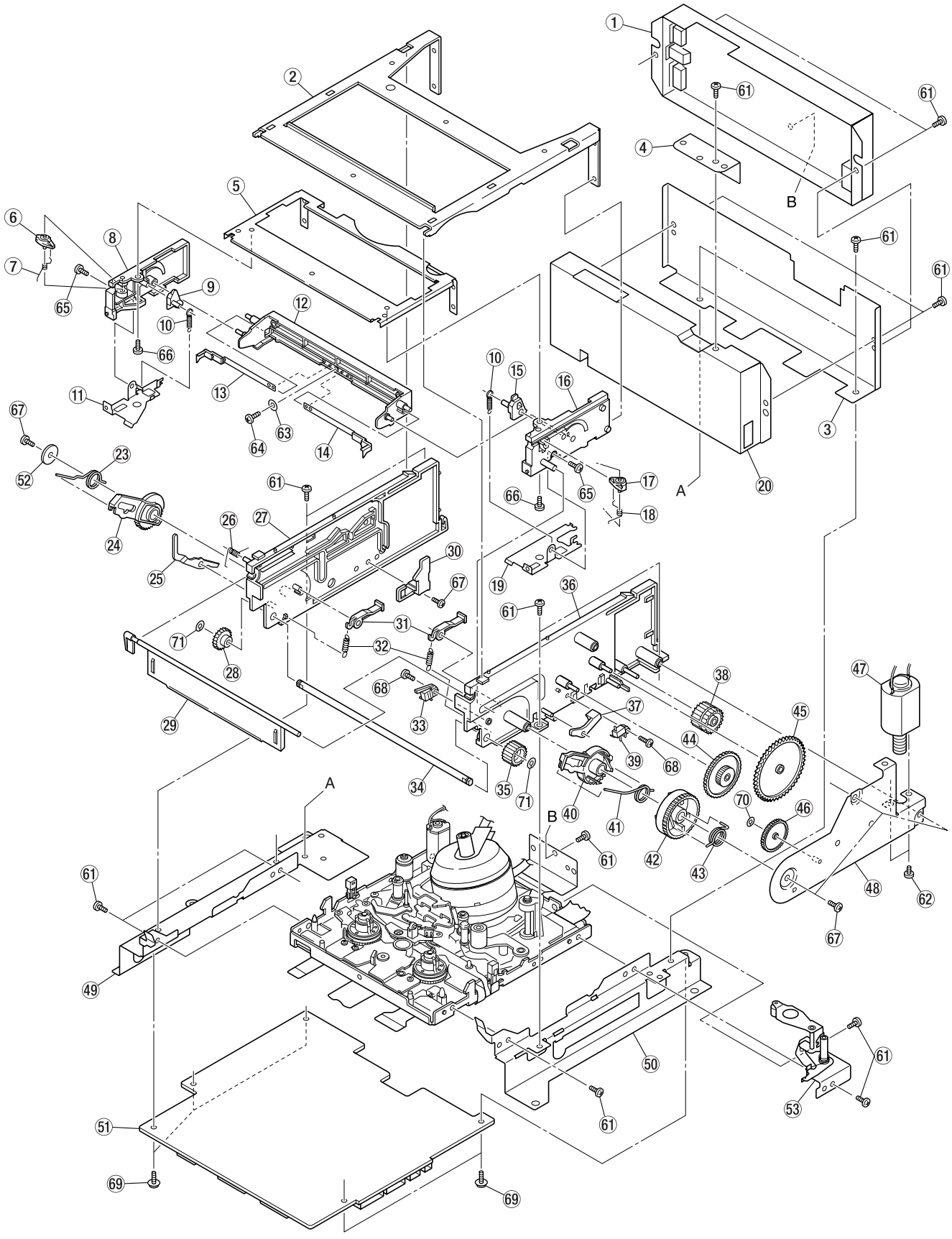
EXPLODED VIEW-1



EXPLODED VIEW-1

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	*M01074900A	COVER,TOP	
1- 2	*M01074800A	ANGLE ASSY	
1- 3	*M01075000A	COVER,SIDE L	
1- 4	*E00556300A	FLAT CABLE,DSUB16	
1- 5	*E95105500A	PCB ASSY,BNC	
1- 6	5334075900	CLAMP,CANNON CONNECTOR SOCKET	
1- 7	*M01075400A	REAR PANEL,SYS	
1- 8	5801536400	SCREW,DSUB LOCK M2.6X0.45	
1- 9	*E95105600A	PCB ASSY,DSUB	
1-10	*E95106300A	PCB ASSY,SYS	
1-11	*M01075700A	BRACKET,FAN A	
1-12	*M01075900A	BRACKET,FAN B	
1-13	*M00039100A	DAMPER	
1-14	*M00039000A	PIN,STEP	
1-15	*E0051380	DC FAN MOT,FBA06A12L	
1-16	*E00345500C	SW RGLTD PS [J,US/C]	
	*E00345540C	SW RGLTD PS [E,K,UK,A]	
1-17	*M01075600A	REAR PANEL,BLANK	
1-18	*M01075300B	CHASSIS ASSY	
1-19	*E95106400A	PCB ASSY,MOTHER	
1-20	*M00617200A	BRACKET	
1-21	*M01073500B	FRONT PANEL ASSY	
1-22	M01074700A	KNOB,SHUTTLE N64	
1-23	M01074600A	KNOB,JOG N64	
1-24	*E95103200A	PCB ASSY,SW	
1-25	M00001500A	BUTTON,C	
1-26	*M01075100B	CHASSIS,FRONT	
1-27	*E95103000A	PCB ASSY,KEY	
1-28	*E95103100A	PCB ASSY,COUNTER	
1-29	*M01075001A	COVER,SIDE R	
1-30	*M01217300A	SHIELD SHEET,LCD	
1-31	5801599400	GASKET	
1-41	5780023006	SCREW,BIND M3X6 (BLK NI)	
1-42	5780224008	SCREW,FLAT M4X8 (BLK NI)	
1-43	5783543008	SCREW,BIND P-TITE M3X8 (BLK NI)	
1-44	*5780112605	SCREW,PAN M2.6X5 (NI)	
1-45	5780003006	SCREW,BIND M3X6	
1-46	5780003030	SCREW,BIND M3X30	
1-47	5780103006	SCREW,PAN M3X6	
1-48	5780004008	SCREW,BIND M4X8	
1-49	5780023010	SCREW,BIND M3X10 (BLK NI)	
1-50	*B00049700A	SCREW,BPAR3*6FZC	
1-51	5780203006	SCREW,FLAT M3X6	
1-52	5780002604	SCREW,BIND M2.6X4	

EXPLODED VIEW-2

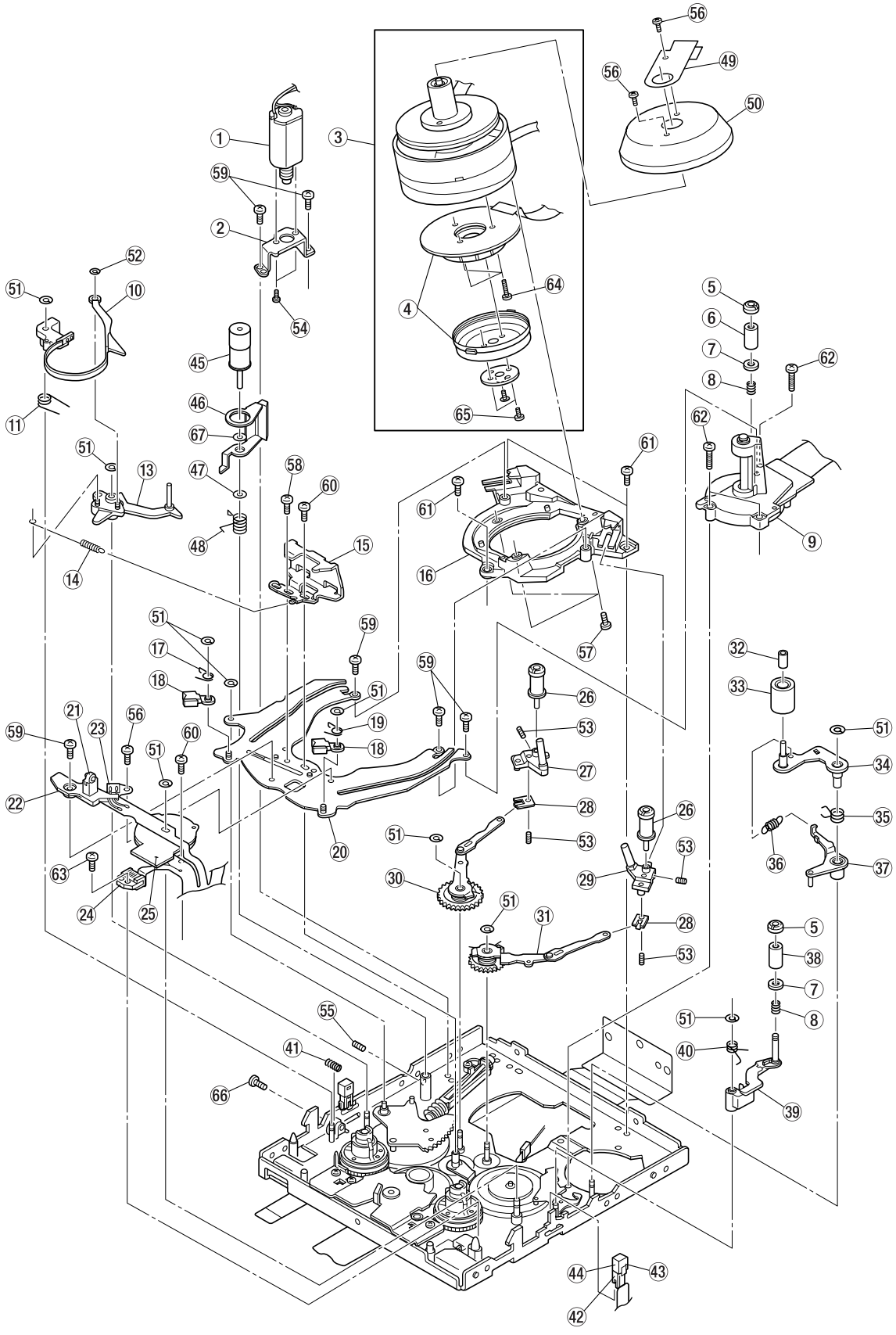


EXPLODED VIEW-2

REF.NO.	PARTS NO.	DESCRIPTION
2- 1	*E95106000A	PCB ASSY,RF PLAY
2- 2	5801527902	BRACKET,CAM PLATE
2- 3	*M01101300A	BRACKET,RF
2- 4	*M01101600A	SHIELD PLATE,FPC
2- 5	M00434400A	HOLDER,MAIN
2- 6	5801525500	LEVER L,CASSETTE PRESS
2- 7	5801525600	SPRING,COIL LLCP
2- 8	5801525300	BASE L,SLIDE
2- 9	5801525700	LEVER L,BRAKE
2-10	5801525800	SPRING T,BRAKE
2-11	5801525400	SUB HOLDER L
2-12	5801524601	OPENER,LID
2-13	5801524700	LEVER L ASSY,LOCK
2-14	5801525000	LEVER R ASSY,LOCK
2-15	5801526300	LEVER R,BRAKE
2-16	5801525900	BASE R,SLIDE
2-17	5801526100	LEVER R,CASSETTE PRESS
2-18	5801526200	SPRING,COIL LRCP
2-19	5801526000	SUB HOLDER R
2-20	*E95106100A	PCB ASSY,RF REC
2-21	Vacant	
2-22	Vacant	
2-23	5801526800	SPRING,COIL CPL
2-24	5801526700	GEAR L,TRANSFER
2-25	5801528000	LEVER,FRONT LID
2-26	5801529200	SPRING,COIL LID
2-27	*5801526503	PLATE L,CAM
2-28	5801528700	GEAR L,SYNCRONIZE
2-29	M00365790B	DOOR,LID FRONT 78
2-30	5801526601	CAM,LID OPENER
2-31	5801528900	LEVER,LOCK
2-32	5801529000	SPRING T,LOCK LEVER
2-33	5300060200	SW,PUSH SPPB21
2-34	5801528600	SHAFT,SYNCRONIZE
2-35	5801528800	GEAR R,SYNCRONIZE
2-36	5801526902	PLATE R,CAM
2-37	5801527000	LEVER,SWITCH
2-38	5801528200	GEAR A,REDUCTION
2-39	5300060100	SW,PUSH SPPB12
2-40	5801527100	GEAR R,TRANSFER
2-41	5801527200	SPRING,COIL CPR
2-42	5801527300	GEAR,RELEASE
2-43	5801527400	SPRING,COIL GR
2-44	5801528400	GEAR C,REDUCTION
2-45	5801528300	GEAR B,REDUCTION
2-46	5801528500	GEAR D,REDUCTION
2-47	5600165100	MOTOR SUB ASSY,CASSETTE
2-48	5801527601	BRACKET ASSY,C MOTOR
2-49	*M00434100A	BRACKET,L
2-50	*M00434200A	BRACKET,R

REF.NO.	PARTS NO.	DESCRIPTION
2-51	*E95106200B	PCB ASSY,SERVO
2-52	5801528100	PLATE,TRANSFER GEAR
2-53	M00435600A	CLEANER ASSY,HEAD
2-61	5780012004	SCREW,BIND M2X4 (NI)
2-62	5782522028	SCREW,PAN 1# M2X2.8 (NI)
2-63	5785022200	WASHER,2X6X0.4T
2-64	5782551640	SCREW,PAN BT 3# M1.6X4 (NI)
2-65	5782521630	SCREW,PAN 3# M1.6X3 (NI)
2-66	5782521625	SCREW,PAN 3# M1.6X2.5 (NI)
2-67	5782552040	SCREW,PAN BT 3# M2X4 (NI)
2-68	5782552080	SCREW,PAN BT 3# M2X8 (NI)
2-69	B0005020	SCREW,PPAB 2X5FNI
2-70	5785341200	WASHER,POLYS. 1.7X4X0.25T
2-71	5785343000	WASHER,POLYS. 3.2X5.5X0.25T

EXPLODED VIEW-3

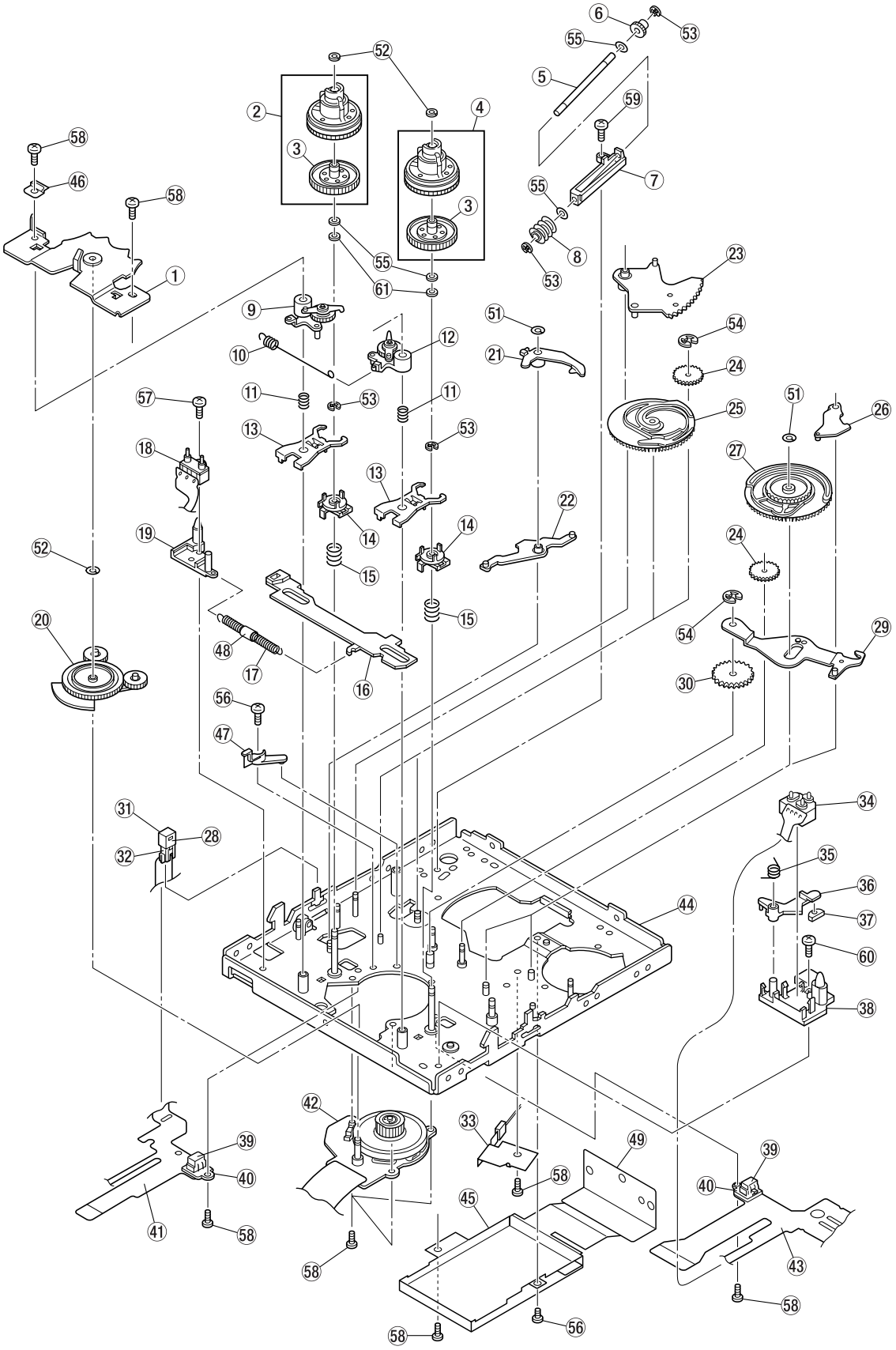


EXPLODED VIEW-3

REF.NO.	PARTS NO.	DESCRIPTION
3- 1	*M00438800A	LD MOTOR ASSY,DTRS
3- 2	M00434000A	HOLDER,LD MOTOR
3- 3	M01101100A	DRUM ASSY,98HR
3- 4	1473407500	MOTOR ASSY,DRAM
3- 5	1676742500	FLANGE,NUT
3- 6	1676744900	GUIDE,CAPSTAN
3- 7	1676742300	FRANGE,GUIDE
3- 8	1638547600	SPRING C
3- 9	1473407700	MOTOR,CAPSTAN
3-10	M00822300A	BRAKE ASSY,BAND
3-11	1638913401	SPRING,COIL 01
3-12	Vacant	
3-13	1796821300	LEVER ASSY,BACK TENSION
3-14	1638209100	SPRING T
3-15	1680464800	PLATE,PROTECTOR
3-16	1615405600	BASE ASSY,DRAM
3-17	1638913800	SPRING,COIL
3-18	1796826300	LEVER ASSY,SOFT BRAKE
3-19	M00256300A	TORSION SPRING,20G
3-20	1615405700	PLATE ASSY,GUIDE RAIL
3-21	13419521	PHOTO ELEMENT,GL450
3-22	1678872150	BRACKET,LED (BRACK)
3-23	13299679	SENSOR,DEW HDP-07-C2
3-24	14771017	SOLENOID,LUTCH 6V 240 OHM
3-25	1796822901	MODE SW ASSY (01)
3-26	1796826900	ROLLER ASSY,M GUIDE
3-27	1796822700	SLIDE MGS ASSY
3-28	1680461900	BRACKET MG
3-29	1796822800	SLIDE MGT ASSY
3-30	1796821100	LEVER ASSY,L THREAD
3-31	1796821200	LEVER ASSY,R THREAD
3-32	1678871800	SLEEVE,PINCH ROLLER
3-33	1796821900	ROLLER ASSY,PINCH
3-34	1796821700	LEVER ASSY,PINCH
3-35	1638913500	SPRING,COIL
3-36	1638209200	SPRING T
3-37	1796821800	LINK ASSY,PINCH
3-38	1676742400	GUIDE,FINAL
3-39	1796822200	LEVER ASSY,GUIDE
3-40	1638913600	SPRING,COIL
3-41	1638547500	SPRING,C
3-42	1678872700	HOLDER,TE SENSOR
3-43	13419660	PHOTO ELEMENT,RPM-20PB-T
3-44	1680472902	PLATE,SLIT 02
3-45	1796822600	ROLLER ASSY,IMPEADANCE
3-46	M00123400A	CLEANER ASSY,TAPE
3-47	M0090610	WASHER,1.63X3X0.13
3-48	M00122100A	TORSION SPRING,ARM T
3-49	M00433900A	SHIELD PLATE,FPC
3-50	M00433800A	SHIELD PLATE,S

REF.NO.	PARTS NO.	DESCRIPTION
3-51	16499908	WASHER,SLIT 1.57X4X0.3
3-52	16499907	WASHER,SLIT 1.2X3X0.3
3-53	B0001450	SPBOLT,NO.0 PAN1.2X2.5FNB
3-54	16502019	SCREW,PAN NO.0 3# 2X2
3-55	B0001540	SPBOLT,NO.0 TP3P1.4X2FNB
3-56	16499864	SCREW,PAN NO.0 M1.6X2
3-57	16499873	SCREW,PAN NO.0 M1.6X5.5
3-58	16499772	SCREW,PAN NO.0 3# 2X2
3-59	16499773	SCREW,PAN NO.0 3# 2X2.5
3-60	16499909	SCREW,PAN NO.0 3# 2X3.5
3-61	16499776	SCREW PAN NO.0 3# 2X5
3-62	16499910	SCREW PAN NO.0 3# 2X8
3-63	16502031	SCREW,TAP TITE ETP 1.4X3.5
3-64	16502044	SCREW,PAN NO.0 1.6X6.5
3-65	*16499870	SCREW PAN NO.0 M1.6X4
3-66	B0000430	SCREW,PAN NO.0 3 2X4.5
3-67	M0090660	WASHER,3.85X6X0.2

EXPLODED VIEW-4



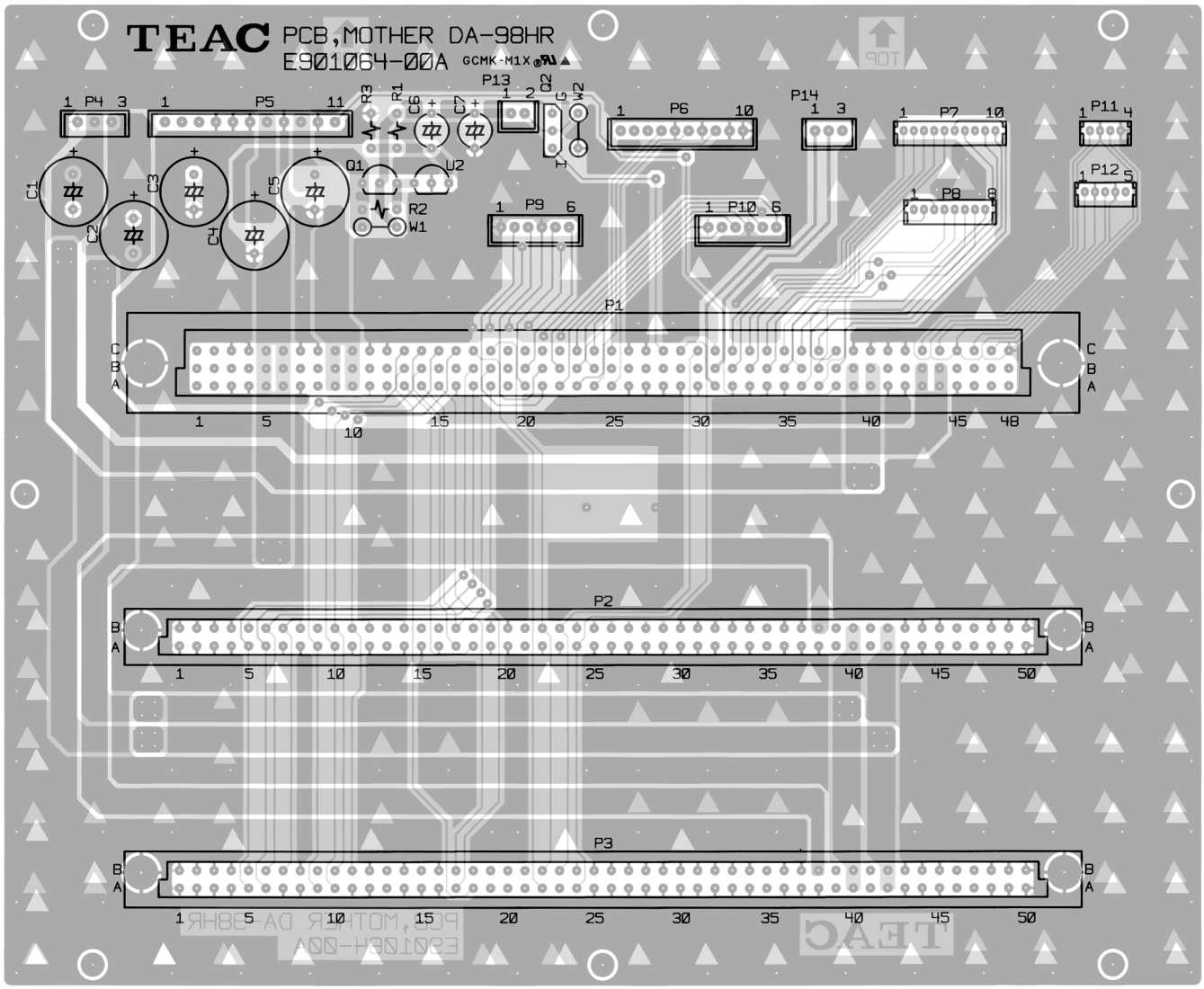
EXPLODED VIEW-4

REF.NO.	PARTS NO.	DESCRIPTION
4- 1	1680462100	BRACKET,T OPENER
4- 2	M00607100A	REEL TABLE ASSY,S
4- 3	1796826600	DISC ASSY,REFRECTOR
4- 4	M00607200B	REEL TABLE ASSY,T
4- 5	1676741400	SHAFT,LOADING GEAR
4- 6	1678870600	WORM WHEEL,LOADING
4- 7	1680460800	BRACKET,GEAR
4- 8	1678870700	WORM,LOADING
4- 9	M00877600A	BRAKE ASSY,S
4-10	1638209000	SPRING T
4-11	1638547400	SPRING C
4-12	M00877700A	BRAKE ASSY,T
4-13	1680460600	LEVER,CLUTCH
4-14	1796820200	CLUTCH ASSY
4-15	1638547300	SPRING C
4-16	1678870001	SLIDE,REEL OPERATING CAM
4-17	1638208900	SPRING T
4-18	13222478	SW,PUSH SPPW62 SPPW62
4-19	1678872500	HOLDER,SWL
4-20	1796826100	GEAR ASSY,CENTER
4-21	1678871700	LEVER,REEL LOCK
4-22	1796820701	LEVER ASSY,SLIDE (-01)
4-23	1796821003	GEAR ASSY,SECTOR (-03)
4-24	1678871000	GEAR B,COUPLING
4-25	1678870800	CAM L,LOGIC
4-26	1796822000	CAM FOLLOWER ASSY,PINCH
4-27	1678871100	CAM R,LOGIC
4-28	1680472902	PLATE,SLIT 02
4-29	1796822300	LEVER ASSY,GUIDE CARRY
4-30	1678870900	GEAR A,COUPLING
4-31	13419660	PHOTO ELEMENT,RPM-20PB-T
4-32	1678872700	HOLDER,TE SENSOR
4-33	M00914300A	BRUSH ASSY
4-34	13222479	SW,PUSH SW-101-2P
4-35	1638913100	SPRING,COIL
4-36	1678870402	LEVER,SLID KEEP (02)
4-37	14771018	SOLENOID,LUTCH
4-38	1678872601	HOLDER,SWR (01)
4-39	13419663	PHOTO ELEMENT,NJL5165KA
4-40	1678872400	HOLDER,REEL SENSOR
4-41	1336133600	PCB,SENSOR L
4-42	1473407800	MOTER,REEL
4-43	1336133700	PCB,SENSOR R
4-44	1796823001	MECHA CHASSIS ASSY (01)
4-45	*M01101700A	COVER,BRUSH
4-46	1630187000	STOPPER TB
4-47	1678889500	SUPPORT,TR BAND
4-48	13090294	TUBE,F 2 PHI
4-49	*M01101600A	SHIELD PLATE,FPC

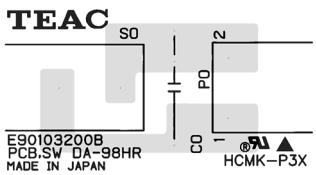
REF.NO.	PARTS NO.	DESCRIPTION
4-51	16499908	WASHER,SLIT 1.57X4X0.3
4-52	16499907	WASHER,SLIT 1.2X3X0.3
4-53	16351100	E-RING,1.2J
4-54	16351150	E-RING,2.5J
4-55	16496335	WASHER,1.7X3.2X0.25
4-56	16499864	SCREW,PAN NO.0 M1.6X2
4-57	16499873	SCREW,PAN NO.0 M1.6X5.5
4-58	16499773	SCREW,PAN NO.0 3# 2X2.5
4-59	16499909	SCREW,PAN NO.0 3# 2X3.5
4-60	16499776	SCREW PAN NO.0 3# 2X5
4-61	16496604	WASHER,1.7X3.2X0.13

7. PC BOARDS AND PARTS LIST
基板図とパーツリスト

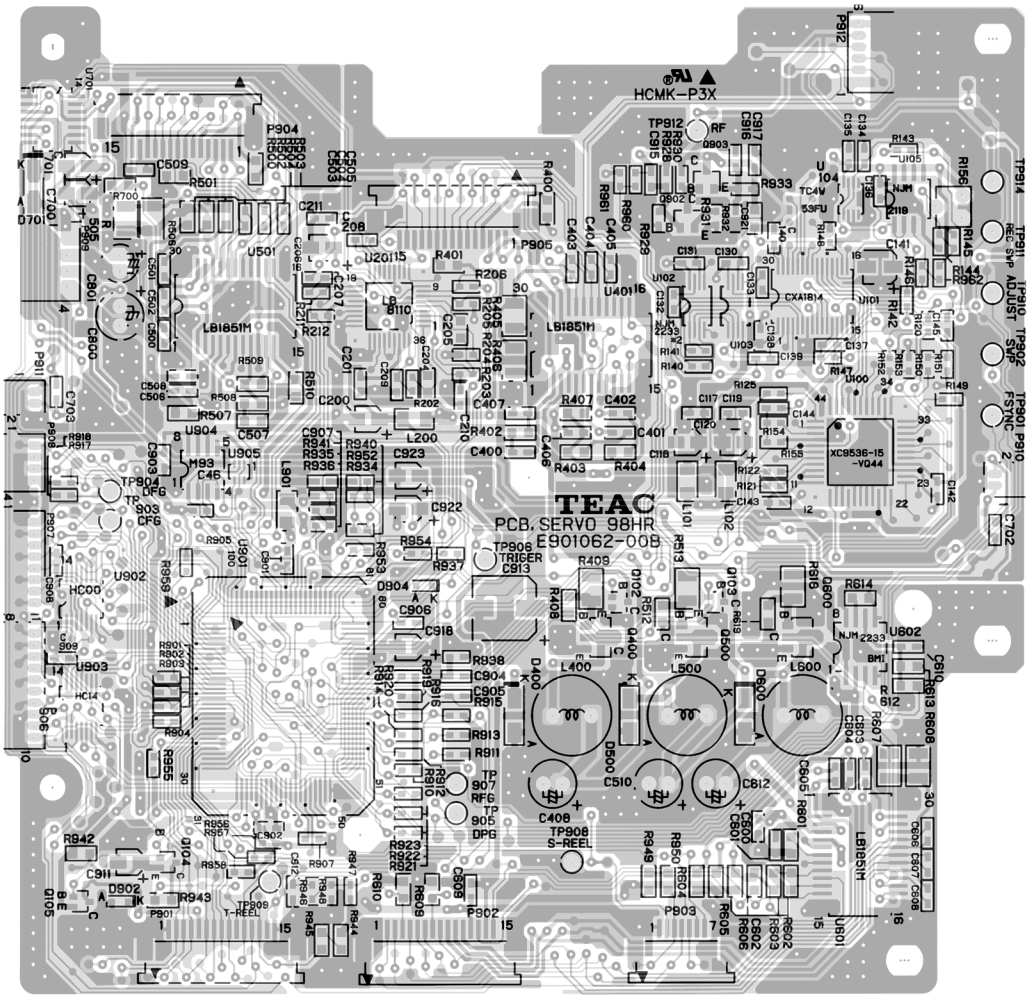
MOTHER PCB



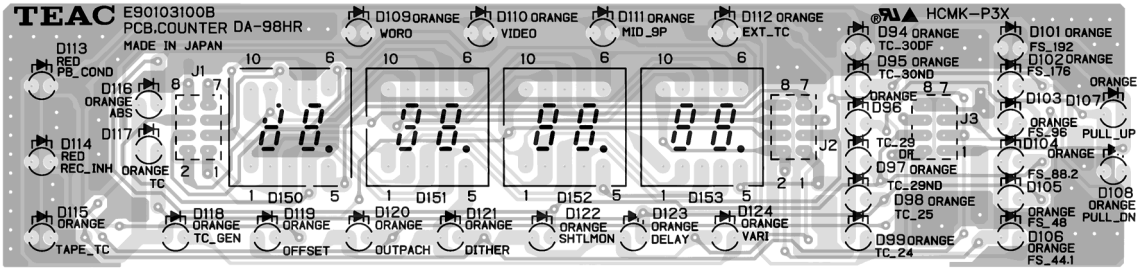
SW PCB



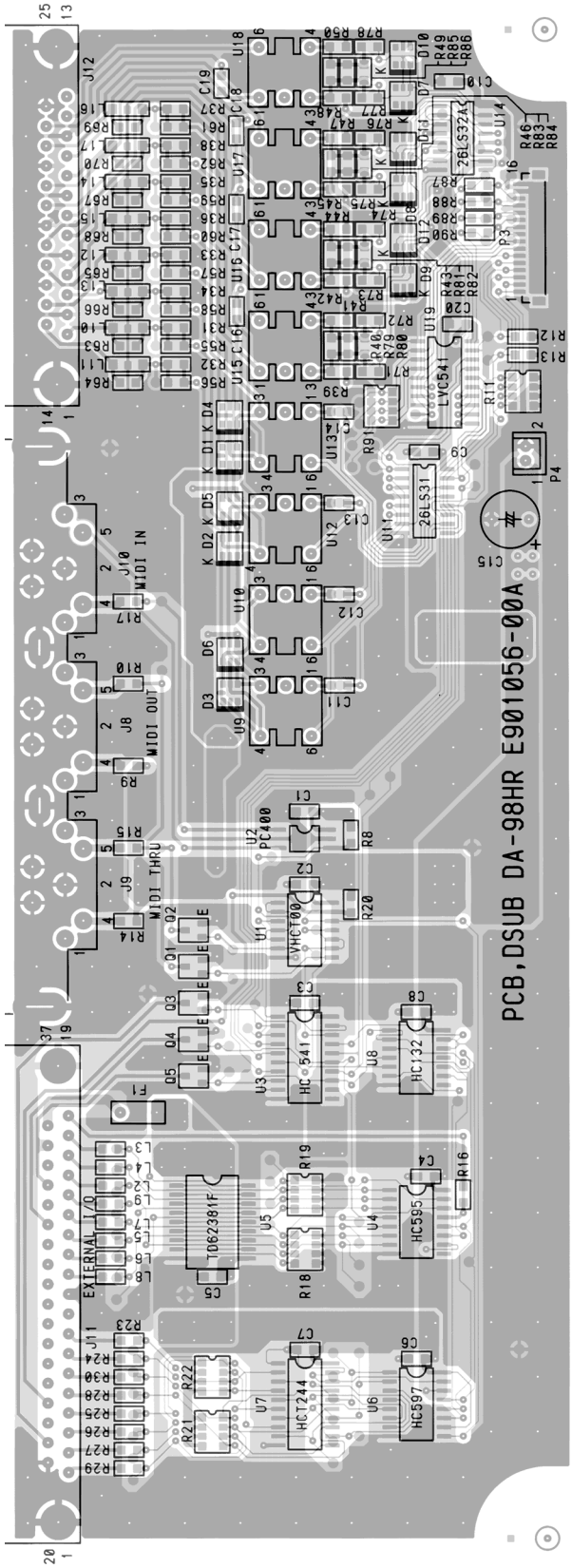
SERVO PCB



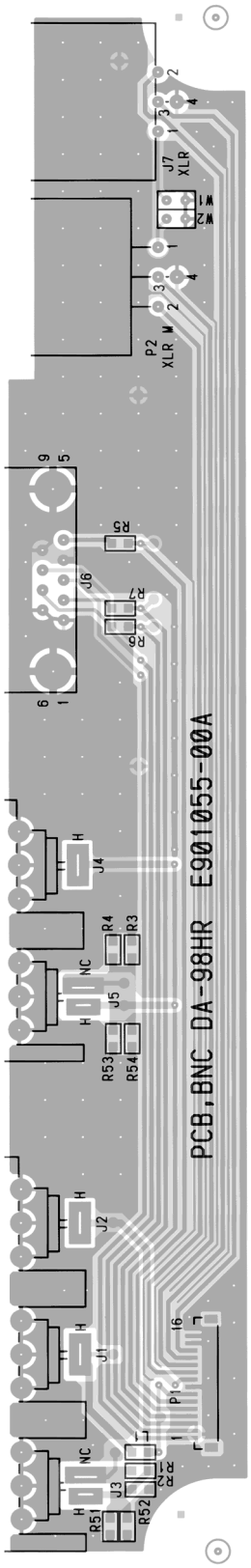
COUNTER PCB



DSUB PCB

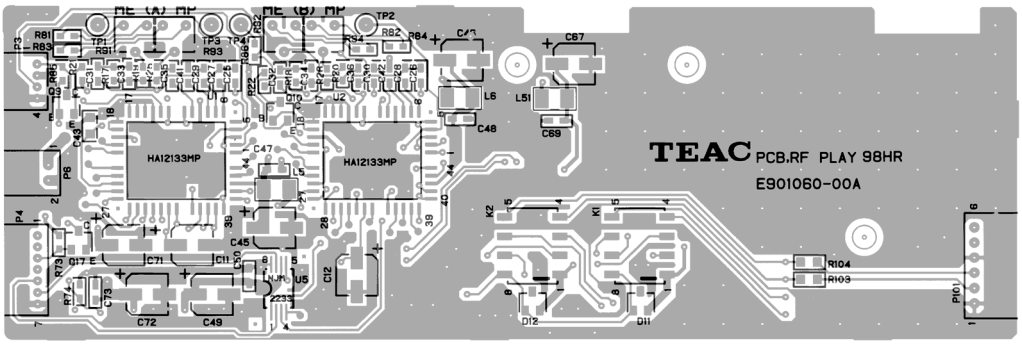


BNC PCB



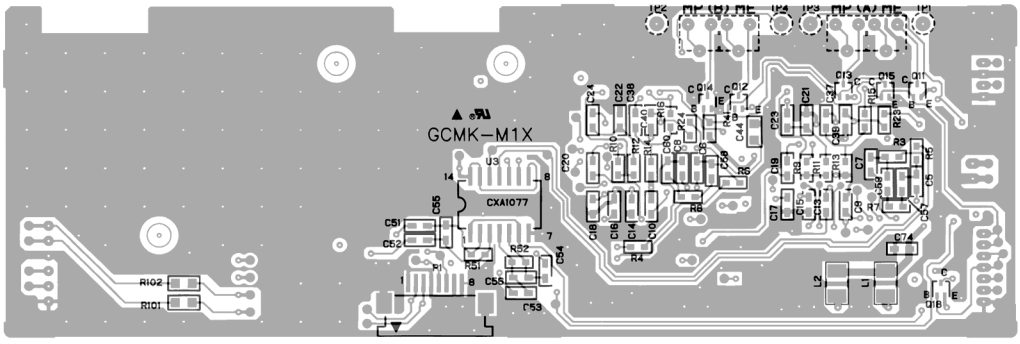
RF PLAY PCB

SIDE A



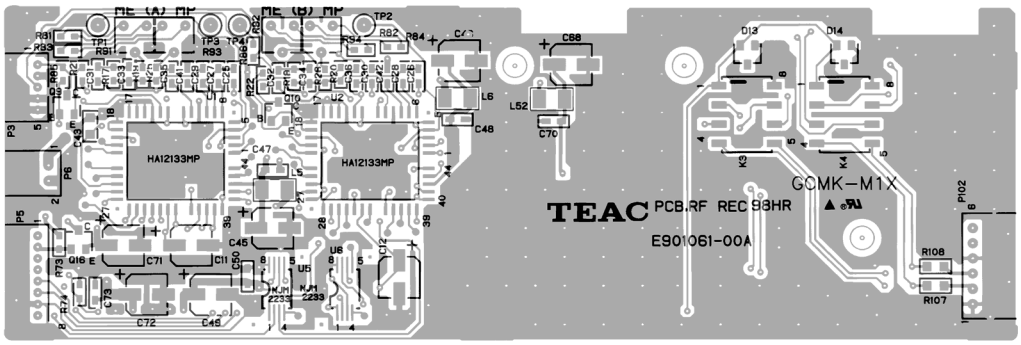
RF PLAY PCB

SIDE B



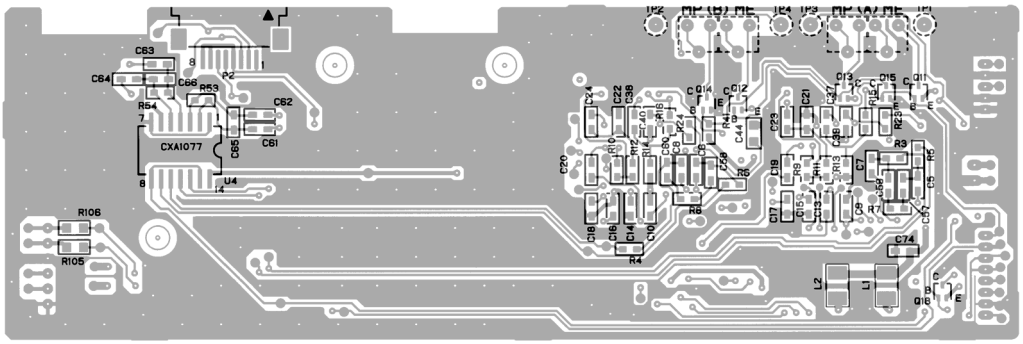
RF REC PCB

SIDE A



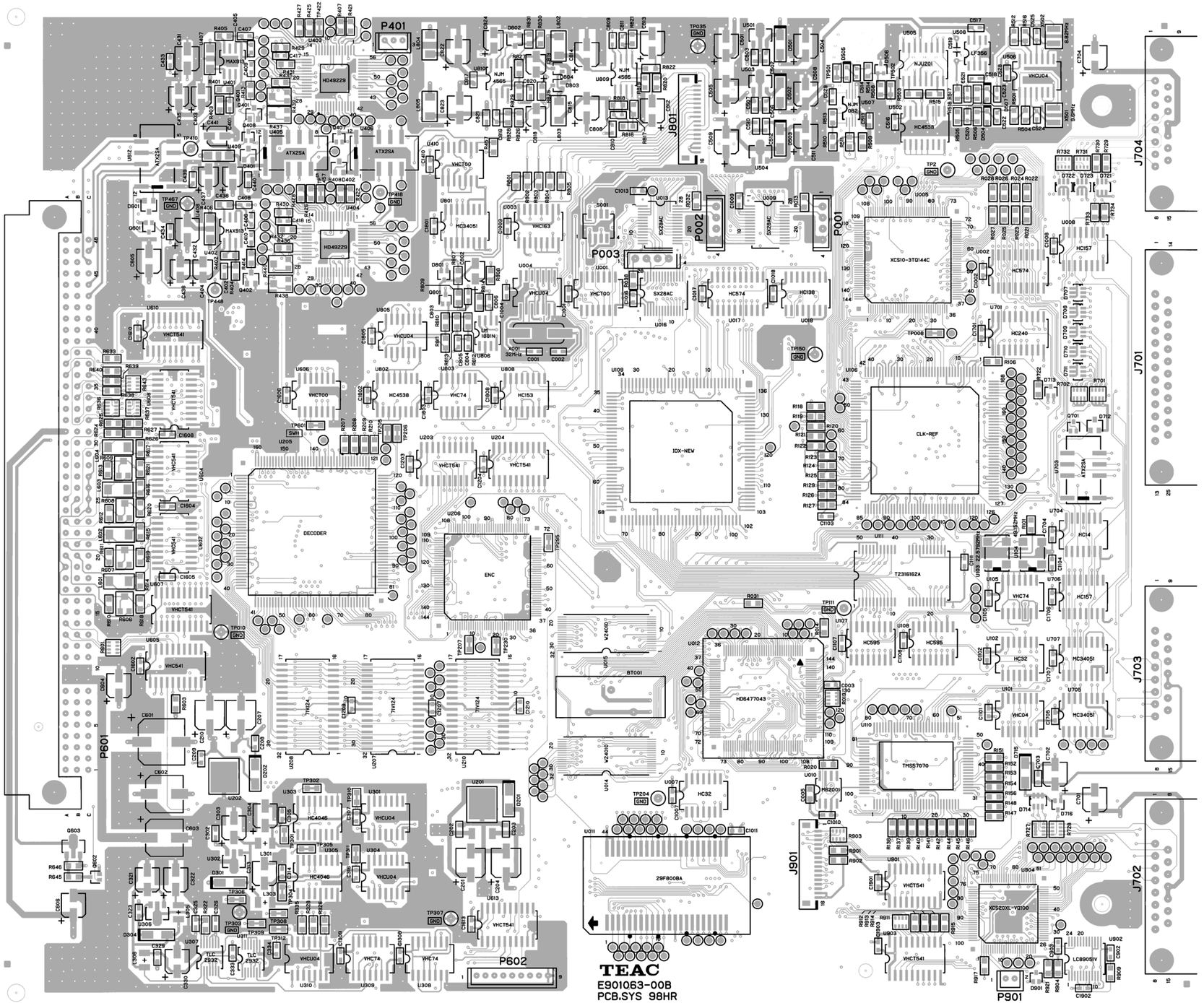
RF REC PCB

SIDE B



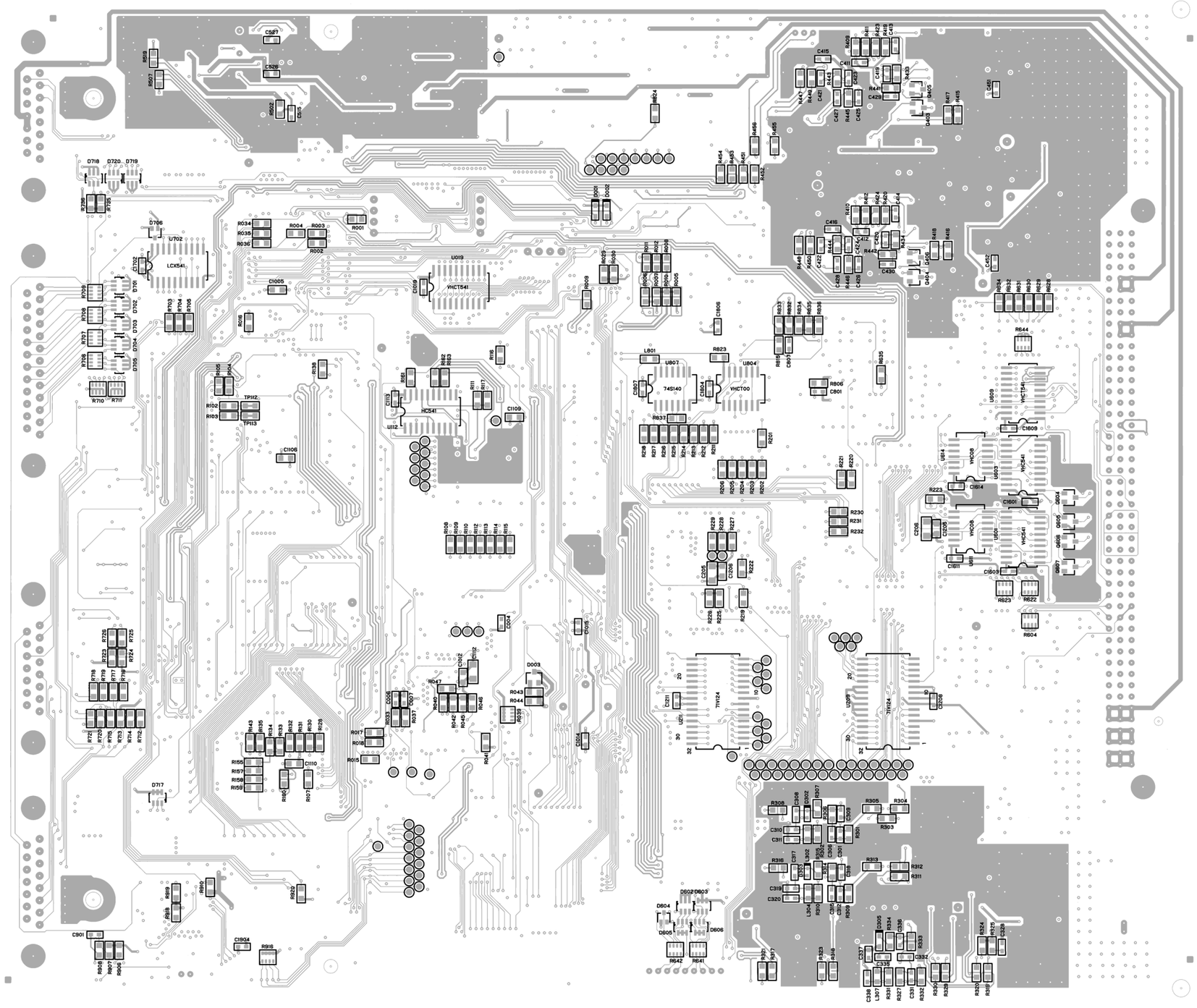
SYS PCB

SIDE A

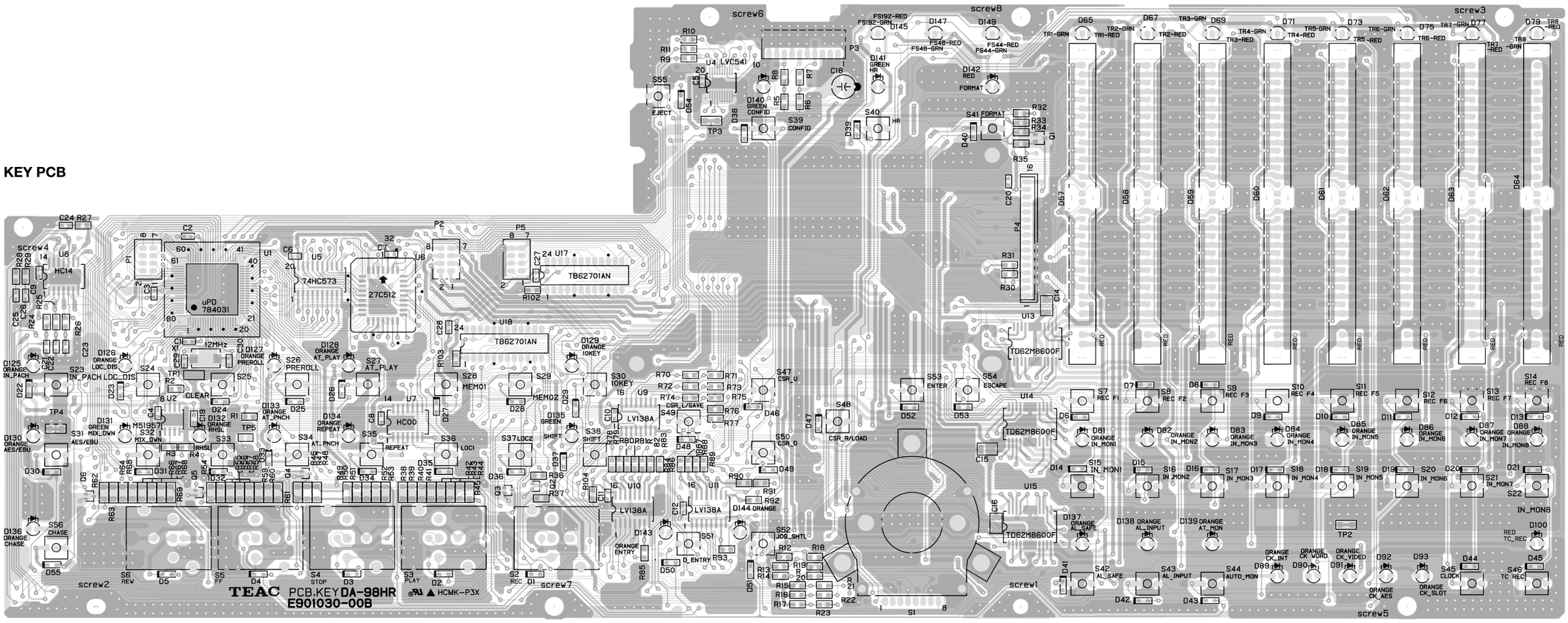


SYS PCB

SIDE B

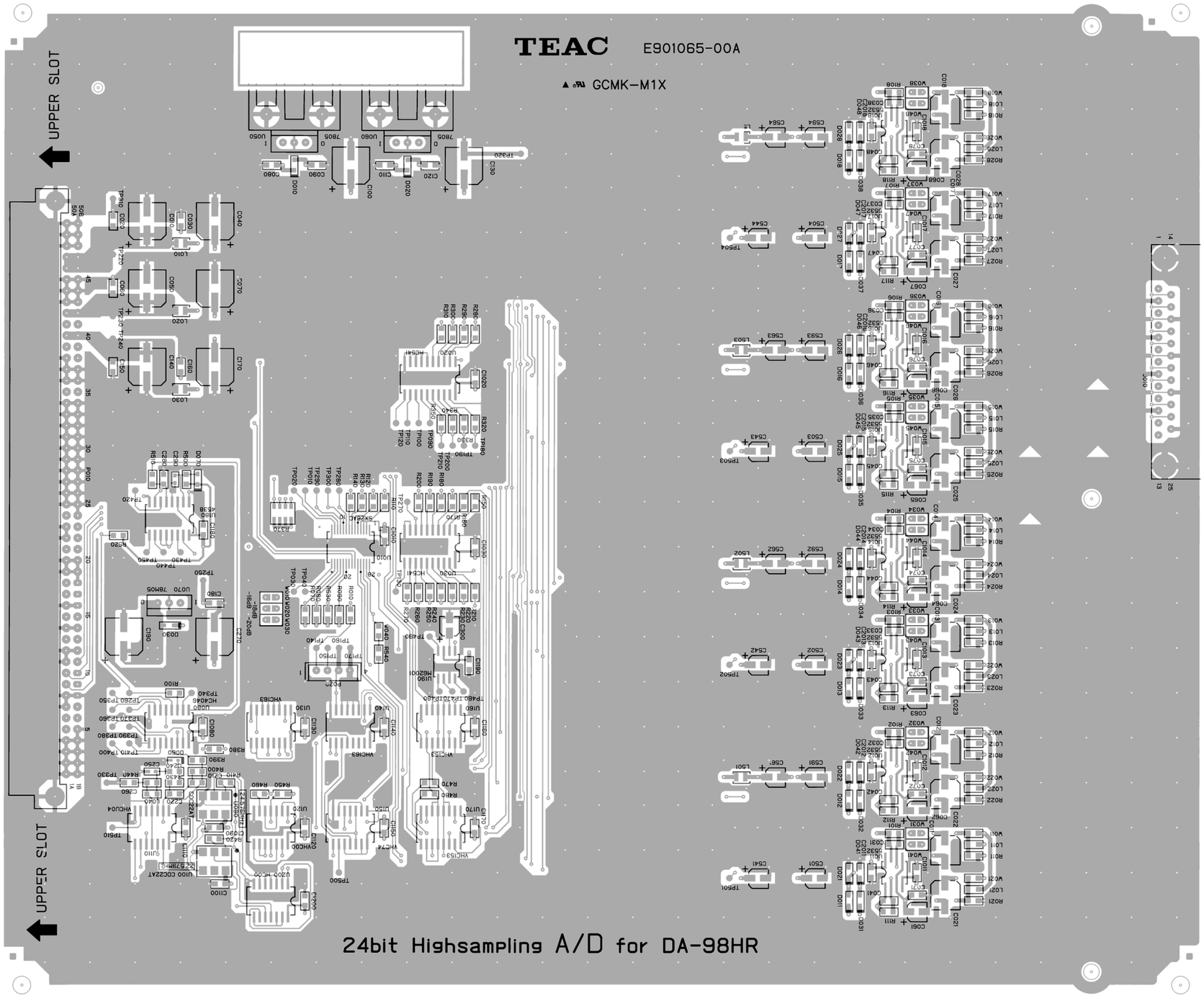


KEY PCB


screw6
screw8
screw3
screw4
screw2
screw7
screw1
screw5
P1
P2
P3
P4
P5
U1 uPD 784031
U2 CLEAR
U4 LVC541
U5 74HC573
U6 27C512
U7 HC00
U9 10KEY
U10 LV138A
U11 LV138A
U13 TD62MB600F
U14 TD62MB600F
U15 TD62MB600F
U17 TB62701AN
U18 TB62701AN
X1 12MHz
S1 JOG_SHTL
S2 REC
S3 PLAY
S4 STOP
S5 FF
S6 REW
S7 REC F1
S8 REC F2
S9 REC F3
S10 REC F4
S11 REC F5
S12 REC F6
S13 REC F7
S14 REC F8
S15 IN_MON1
S16 IN_MON2
S17 IN_MON3
S18 IN_MON4
S19 IN_MON5
S20 IN_MON6
S21 IN_MON7
S22 IN_MON8
S23 IN_PACH
S24 LOC_DIS
S25 CLEAR
S26 PREROLL
S27 AT_PLAY
S28 MEM01
S29 MEM02
S30 10KEY
S31 AES/EBU
S32 MIX_DWN
S33 RHSL
S34 AT_PNCH
S35 REPEAT
S36 LOC1
S37 LOC2
S38 SHIFT
S39 CONFID
S40 HR
S41 FORMAT
S42 AL_SAFE
S43 AL_INPUT
S44 AUTO_MON
S45 CLOCK
S46 TC REC
S47 CSR_U
S48 CSR_R/LOAD
S49 CSR_L/SAVE
S50 CSR_D
S51 D_ENTRY
S52 JOG_SHTL
S53 ENTER
S54 ESCAPE
S55 EJECT
S56 CHASE
D1 REC
D2 PLAY
D3 STOP
D4 FF
D5 REW
D6 LOC_DIS
D7 REC F1
D8 REC F2
D9 REC F3
D10 REC F4
D11 REC F5
D12 REC F6
D13 REC F7
D14 IN_MON1
D15 IN_MON2
D16 IN_MON3
D17 IN_MON4
D18 IN_MON5
D19 IN_MON6
D20 IN_MON7
D21 IN_MON8
D22 IN_PACH
D23 LOC_DIS
D24 CLEAR
D25 PREROLL
D26 AT_PLAY
D27 MEM01
D28 MEM02
D29 10KEY
D30 AES/EBU
D31 MIX_DWN
D32 RHSL
D33 AT_PNCH
D34 REPEAT
D35 LOC1
D36 LOC2
D37 SHIFT
D38 CONFID
D39 HR
D40 FORMAT
D41 AL_SAFE
D42 AL_INPUT
D43 AUTO_MON
D44 CLOCK
D45 TC REC
D46 CSR_U
D47 CSR_L/SAVE
D48 CSR_R/LOAD
D49 CSR_D
D50 D_ENTRY
D52 ENTER
D53 ESCAPE
D54 EJECT
D55 CHASE
D57 TR1-GRN
D58 TR1-RED
D59 TR2-GRN
D60 TR2-RED
D61 TR3-GRN
D62 TR3-RED
D63 TR4-GRN
D64 TR4-RED
D65 TR5-GRN
D67 TR5-RED
D69 TR6-GRN
D71 TR6-RED
D73 TR7-GRN
D75 TR7-RED
D77 TR8-GRN
D79 TR8-RED
D81 IN_MON1
D82 IN_MON2
D83 IN_MON3
D84 IN_MON4
D85 IN_MON5
D86 IN_MON6
D87 IN_MON7
D88 IN_MON8
D89 CK_INT
D90 CK_WORD
D91 CK_VIDEO
D92 CK_AES
D93 CK_SLOT
D100 TC_REC
D125 IN_PACH
D126 LOC_DIS
D127 PREROLL
D128 AT_PLAY
D129 10KEY
D130 AES/EBU
D131 MIX_DWN
D132 RHSL
D133 AT_PNCH
D134 REPEAT
D135 SHIFT
D136 CHASE
D137 AL_SAFE
D138 AL_INPUT
D139 AT_MON
D140 CONFID
D141 HR
D142 FORMAT
D143 ENTRY
D144 ORANGE
D145 FS192-GRN
D147 FS48-GRN
D149 FS44-GRN
TP1
TP2
TP3
TP4
TP5
TEAC PCB,KEY DA-98HR
E901030-00B
HCMK-P3X

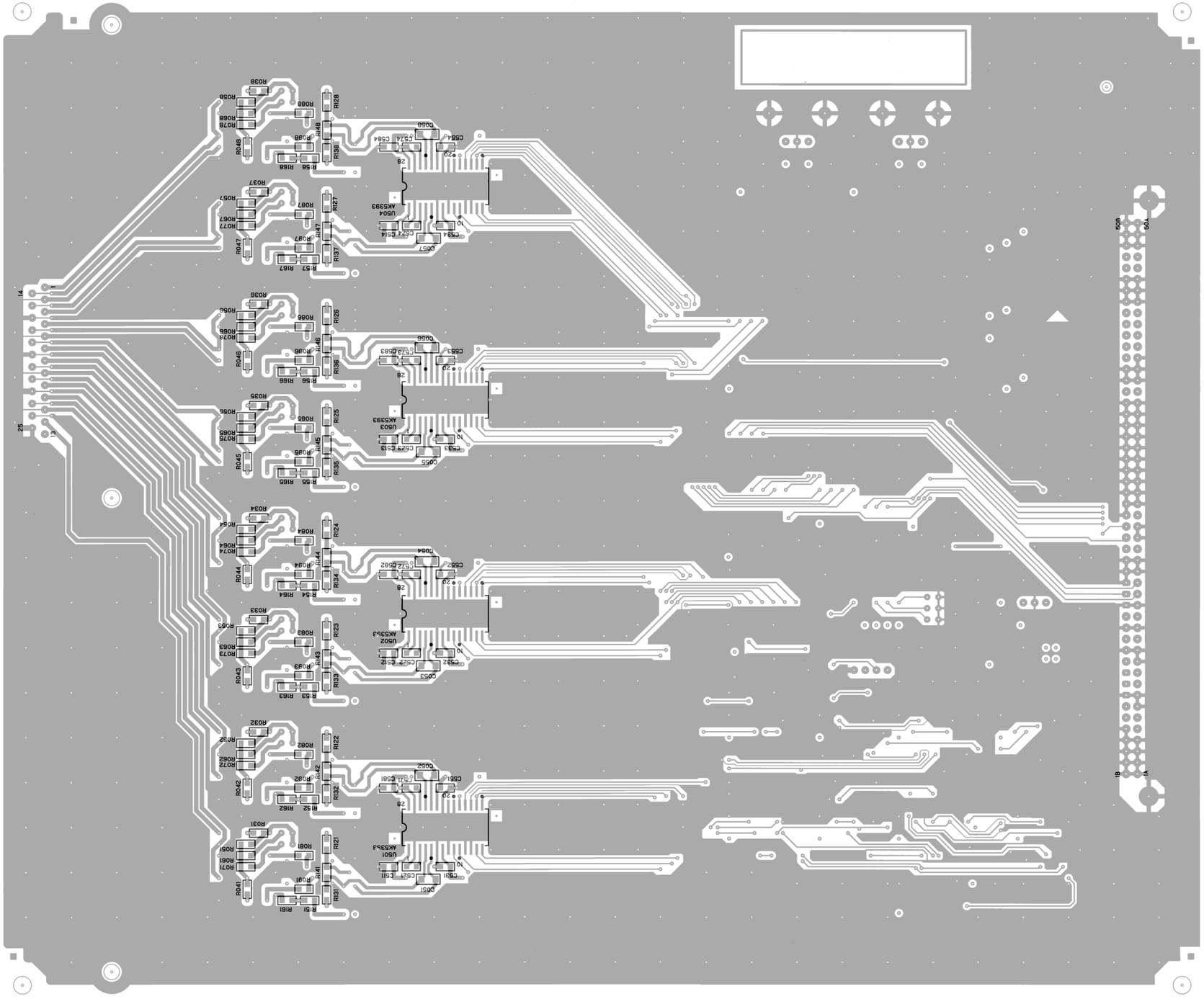
IF98AD PCB (IF-AN98HR)

SIDE A



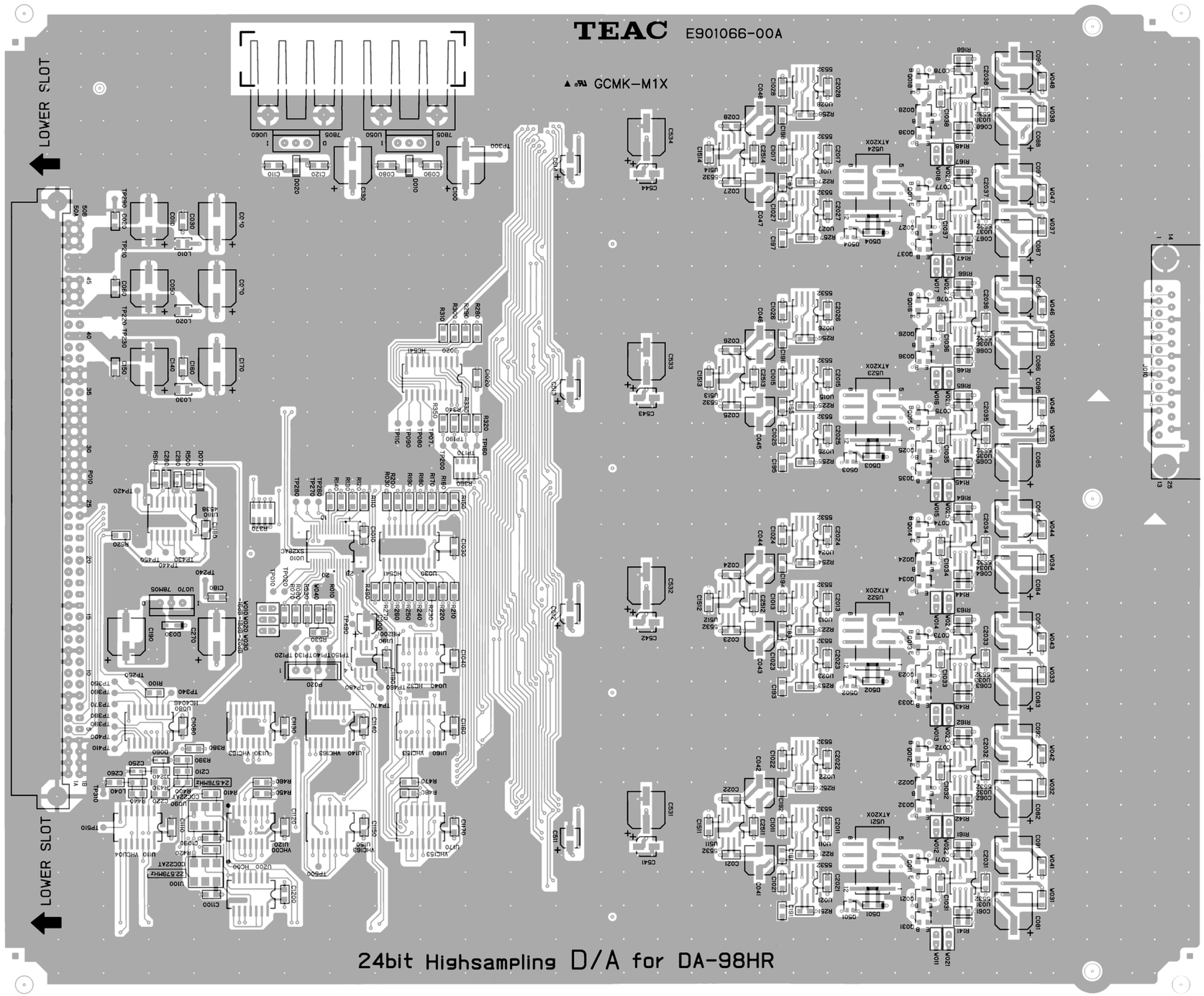
IF98AD PCB (IF-AN98HR)

SIDE B



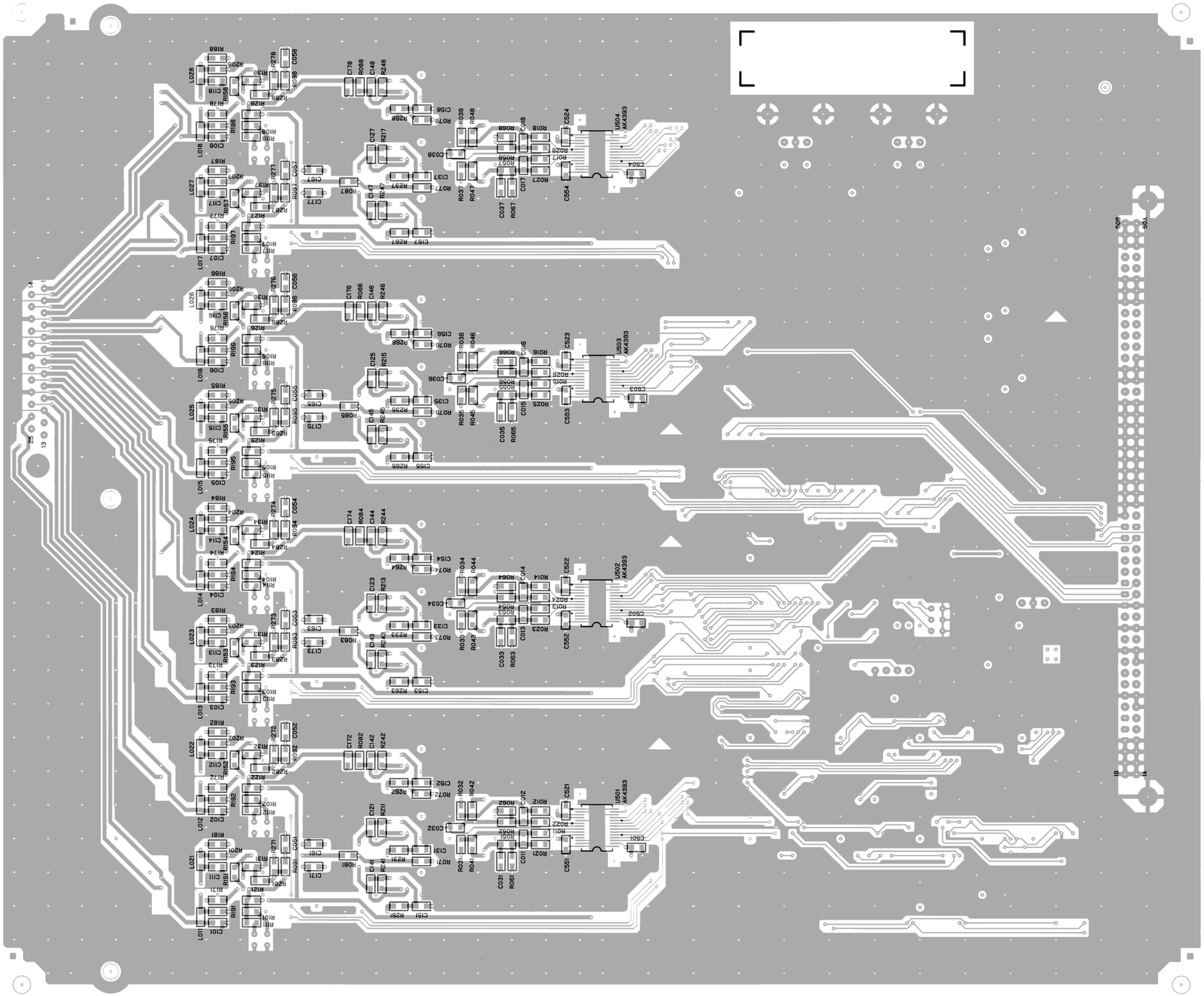
IF98DA PCB (IF-AN98HR)

SIDE A



IF98DA PCB (IF-AN98HR)

SIDE B



MOTHER PCB ASSY

REF.NO.		PARTS NO.	DESCRIPTION
		*E95106400A	PCB ASSY,MOTHER
		*E90106400A	PCB,MOTHER
P1		E0033030	CONNECTOR,PCN10MA-144S
P2,3		5334079500	SOCKET,CONN. 100P
P4		5336303300	PLUG,CONN. B3B-EH(WHT)
P5		5336304100	PLUG,CONN. B11B-EH(WHT)
P6		5336250000	PLUG,CONN. B10B-PH-K-S(WHT)
P7		13124432	CONNECTOR,ZH B 10B-ZR
P8		13124430	CONNECTOR,ZH B 8B-ZR
P9		5336251600	PLUG,CONN. B06B-PH-K-R(RED)
P10		5336249600	PLUG,CONN. B06B-PH-K-S(WHT)
P11		13124426	CONNECTOR,ZH B 4B-ZR
P12		13124427	CONNECTOR,ZH B 5B-ZR
P13		5336249200	PLUG,CONN. B02B-PH-K-S(WHT)
P14		5336249300	PLUG,CONN. B03B-PH-K-S(WHT)
Q1		S0031562	TR,2SB1592
U2		5220446100	IC,M5237L

SW PCB ASSY

REF.NO.		PARTS NO.	DESCRIPTION
		*E95103200A	PCB ASSY,SW
		*E90103200B	PCB,SW
C0	⚠	E0022570	SPK KILLER,0.0047UF 250V
P0		E0042990	CONNECTOR,S2P3-VH
S0	⚠	E0038520	SW,PUSH SDDLB14000

SERVO PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106200B	PCB ASSY,SERVO
	*E90106200B	PCB,SERVO
D400	5224019200	DIODE,EC10QS04TE12L
D500	5224019200	DIODE,EC10QS04TE12L
D600	5224019200	DIODE,EC10QS04TE12L
D701	S0021554	DIODE,RB070L-40TE25
D902,904	S0022094	DIODE,1SS355
L101,102	E0022854	COIL,CHIP 100UF
L200	E0022854	COIL,CHIP 100UF
L400,500	14728449	COIL,390UH 10%
L600	14728444	COIL,150UH 10%
L901	E0022854	COIL,CHIP 100UF
P901	13153693	CONNECTOR,52271-1590
P902	13153479	CONNECTOR,15P
P903	5336379500	CONNECTOR,7P 52271-0790
P904,905	13153693	CONNECTOR,52271-1590
P906	13124443	CONNECTOR,ZH S10B-ZR
P907	13124025	CONNECTOR,ZN S 8B-ZR
P908	13124021	CONNECTOR,ZN S 4B-ZR
P909	5336287400	PLUG,CONN. S4B-PH-K-S(WHT)

SERVO PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
P910	13124435	CONNECTOR,ZH S 2B-ZR
P911	13124435	CONNECTOR,ZH S 2B-ZR
P912	13124439	CONNECTOR,ZH S 6B-ZR
Q102,103	S0000674	TR,DTC123JUA
Q104,105	S0019894	TR,DTA114EUA-T106
Q400	5230020200	TR,2SA1314B-TE12L,C
Q500	5230020200	TR,2SA1314B-TE12L,C
Q600	5230020200	TR,2SA1314B-TE12L,C
Q902,903	13427337	TR,2SC2412K
R156	R0016720	VAR RES,4.7KB RH0422C
U100	S00381800A	IC,ATF-CTRL
U101	S0038383	IC,CXA1814N
U102,103	S0020414	IC,NJM2233BV-TE1
U104	S0001204	IC,TC4W53FU-TE12L
U105	S0038394	IC,NJM2119M
U201	5220448800	IC,LB8110M
U401,501	5220448900	IC,LB1851M
U601	5220448900	IC,LB1851M
U602	5220450800	IC,TL5001CPS-T
U701	5220449000	IC,LB1836M
U901	S00241900A	IC,UPD78146GF-025-3BA
U902	S0033274	IC,SN74LV00APW
U903	S0020454	IC,SN74LV14PW
U904	S0033414	IC,M93C46-MN6T
U905	S0034654	IC,TC7S08FU

COUNTER PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95103100A	PCB ASSY,COUNTER
	*E90103100B	PCB,COUNTER
D101-112	5225018500	LED,SLR-34DU3F
D101A-108A	M00608701A	SPACER,LH-5 L=2
D109A-112A	M00608701A	SPACER,LH-5 L=2
D113-114	5225013500	LED,SLR-34VR3F (RED)
D113A-124A	M00608701A	SPACER,LH-5 L=2
D115-124	5225018500	LED,SLR-34DU3F
D150-153	5225028400	LED,INDICATOR,LB-302DF
D94-99	5225018500	LED,SLR-34DU3F
D94A-99A	M00608701A	SPACER,LH-5 L=2
J1-3	5336372000	SOCKET,CONN. 8P BTK 8S-2S

DSUB PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95105600A	PCB ASSY,DSUB
	*E90105600A	PCB,DSUB
D1-12	13411596	DIODE,IMN10
F1	E0039020	CKT PTCT,RXE010
J8-10	E0022450	CONNECTOR,DIN5 YKF51-5040
J11	E0032230	CONNECTOR,DSUB 37PIN
J12	E0032220	CONNECTOR,DSUB 25PIN
L2-9	5347027700	FERRITE BEADS,CHIP BK2125HS121
L10-17	5292810900	EMI FILTER,CHIP 100PFT
P3	E0032364	CONNECTOR,FMN 16BMT
P4	5336249200	PLUG,CONN. B02B-PH-K-S(WHT)
Q1-5	13428287	TR,DTC124EKAT-146
R11	11985206	RES ARRAY,CHIP 4X10K J
R18,19	11985206	RES ARRAY,CHIP 4X10K J
R21,22	11985206	RES ARRAY,CHIP 4X10K J
R91	11985206	RES ARRAY,CHIP 4X10K J
U1	S0024314	IC,TC74VHCT00F(EL)
U2	S0024184	PHOTO COUPLER,PC400
U3	S0000584	IC,HD74HC541FPEL
U4	5220121100	IC,HD74HC595FPEL
U5	S0036924	TR,TD62381F TP
U6	5220117000	IC,HD74HC597FP
U7	S0038234	IC,TC74HCT244AF
U8	5220111400	IC,HD74HC132FP
U9-10	E00595800A	TRANS,PULSE 400UH
U11	S0038974	IC,DS26C31TMX
U12-13	E00595800A	TRANS,PULSE 400UH
U14	S0038984	IC,DS26C32ATMX
U15-18	E00595800A	TRANS,PULSE 400UH
U19	S0020344	IC,TC74VHC541

BNC PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95105500A	PCB ASSY,BNC
	*E90105500A	PCB,BNC
J1-3	E0033070	JACK,P2286-A BNC3P(1SW)
J4-5	E0033060	JACK,P2360 BNC2P(1SW)
J6	E0032200	CONNECTOR,DSUB 9PIN
J7	5334076000	SOCKET,CANNON CONNECTOR
L1	5347027700	FERRITE BEADS,CHIP BK2125HS121
P1	E0032364	CONNECTOR,FMN 16BMT
P2	5334072800	PLUG,CANNON CONNECTOR

RF PLAY PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106000A	PCB ASSY,RF PLAY
	*E90106000A	PCB,RF PLAY
	*M01101400A	SHIELD COVER,RF P
D11,12	S0023224	DIODE,DAN217 T146
K1,2	E0054744	RELAY,G6K-2F
L1,2	14728152	COIL,CHIP 47UF 10%
L5,6	14728152	COIL,CHIP 47UH 10%
L51	14728152	COIL,CHIP 47UH 10%
P1	13153472	CONNECTOR,8P
P3	13124021	CONNECTOR,ZN S 4B-ZR
P4	13124440	CONNECTOR,ZH S 7B-ZR
P6	5336287200	PLUG,CONN. S2B-PH-K-S(WHT)
P101	5336287600	PLUG,CONN. S6B-PH-K-S(WHT)
Q9,10	13427337	TR,2SC2412K
Q11-15	S0020404	TR,DTC124EEATL
Q17	13427256	TR,DTD123YK
Q18	S0024374	TR,DTA124EETL
R91-94	R0016700	VAR RES,2.2KB RH0422C
U1,2	5220449300	IC,HA12133MP
U3	13448164	IC,CXA1077M-T4
U5	S0020414	IC,NJM2233BV-TE1

RF REC PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106100A	PCB ASSY,RF REC
	*E90106100A	PCB,RF REC
	*M01101500A	SHIELD COVER,RF R
D13,14	S0023224	DIODE,DAN217 T146
K3,4	E0054744	RELAY,G6K-2F
L1,2	14728152	COIL,CHIP 47UH 10%
L5,6	14728152	COIL,CHIP 47UH 10%
L52	14728152	COIL,CHIP 47UH 10%
P2	13153472	CONNECTOR,8P
P3	13124438	CONNECTOR,ZH S 5B-ZR
P5	13124025	CONNECTOR,ZN S 8B-ZR
P6	5336287200	PLUG,CONN. S2B-PH-K-S(WHT)
P102	5336291600	PLUG,CONN. S6B-PH-K-R(RED)
Q9,10	13427337	TR,2SC2412K
Q11-15	S0020404	TR,DTC124EEATL
Q16	13427250	TR,DTB123YK
Q18	S0024374	TR,DTA124EETL
R91-94	R0016700	VAR RES,2.2KB RH0422C
U1,2	5220449300	IC,HA12133MP
U4	13448164	IC,CXA1077M-T4
U5	S0020414	IC,NJM2233BV-TE1
U6	S0020414	IC,NJM2233BV-TE1

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106300A	PCB ASSY,SYS
	*E90106300B	PCB,SYS
	*M00473600A	HEATSINK,IOX
	*M00473900A	SPACER,IOX
	*5780002606	SCREW,BIND M2.6X6
BT1	E0055380	BATTERY,CR2032
BT1A	E0055390	HOLDER,BCR20V4
D001,002	13411644	DIODE,CHIP 1SS355 TE-17
D003	S0035734	DIODE,1SS377(TE85L)
D201,202	13411667	DIODE,CHIP HRF22
D301	13411667	DIODE,CHIP HRF22
D302,303	S0035214	DIODE,HVC376B-TRF
D304	13411667	DIODE,CHIP HRF22
D305	5228018100	C,VARI HVU17TR
D402	S0023224	DIODE,DAN217 T146
D501-503	13411667	DIODE,CHIP HRF22
D504	5228018100	C,VARI HVU17TR
D505	S0020814	ZENER DIODE,UDZ 5.1B
D506	S0025274	DIODE,RB706F-40
D507	5228018100	C,VARI HVU17TR
D601	S0023224	DIODE,DAN217 T146
D602,603	13411596	DIODE,IMN10
D604	S0025274	DIODE,RB706F-40
D605,606	13411596	DIODE,IMN10
D701-705	13411596	DIODE,IMN10
D706	S0025274	DIODE,RB706F-40
D707-711	13411596	DIODE,IMN10
D712	S0023224	DIODE,DAN217 T146
D713	S0025274	DIODE,RB706F-40
D714	13411596	DIODE,IMN10
D715	13411667	DIODE,CHIP HRF22
D716	S0025274	DIODE,RB706F-40
D717-723	13411596	DIODE,IMN10
D801	S0025274	DIODE,RB706F-40
D802	S0023224	DIODE,DAN217 T146
D803,804	S0025274	DIODE,RB706F-40
D901	S0025274	DIODE,RB706F-40
J701	E0032220	CONNECTOR,DSUB 25PIN
J702-704	E0032210	CONNECTOR,DSUB 15PIN
J801,901	E0032364	CONNECTOR,FMN 16BMT
L301	14728209	COIL,CHIP 47UH
L302,304	5286051500	COIL,CHIP 2.7UH K LK2125
L303	14728209	COIL,CHIP 47UH
L305,306	14728209	COIL,CHIP 47UH
L307	5286051300	COIL,CHIP 2.2UH K LK2125
L601-604	E0055364	COIL,CHIP 1000UH 5%
L801	E0031304	BEAD COIL,BLM21A601S
L802-805	E0055364	COIL,CHIP 1000UH 5%
P001-003	5336303400	PLUG,CONN. B4B-EH(WHT)
P401	5336249300	PLUG,CONN. B03B-PH-K-S(WHT)

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
P601	E0033020	CONNECTOR,PCN10MA-144P
P602	5336249900	PLUG,CONN. B09B-PH-K-S(WHT)
P901	5336249200	PLUG,CONN. B02B-PH-K-S(WHT)
Q403-406	13428287	TR,DTC124EKAT-146
Q407	S0019224	TR,DTC143XUA T106
Q601	S0019224	TR,DTC143XUA T106
Q604-607	13428287	TR,DTC124EKAT-146
Q701	S0019224	TR,DTC143XUA T106
Q801	S0019204	TR,2SC4081 T106R
R019	R0067304	RES ARRAY,1/16W 4X10K J
R039	R0067224	RES ARRAY,1/16W 4X4.7K J
R437-440	R0066374	VAR RES,EVM3VSX50B54
R601	R0092704	RES ARRAY,1/16W 4X47 J
R604	R0067304	RES ARRAY,1/16W 4X10K J
R606-609	R0092754	VAR RES,1KB RH03ADC
R622,623	R0092704	RES ARRAY,1/16W 4X47 J
R636	R0067304	RES ARRAY,1/16W 4X10K J
R637	R0092704	RES ARRAY,1/16W 4X47 J
R641-643	R0092704	RES ARRAY,1/16W 4X47 J
R644	R0067304	RES ARRAY,1/16W 4X10K J
R701,702	R0092714	RES ARRAY,1/16W 4X2.2K J
R706-709	R0092704	RES ARRAY,1/16W 4X47 J
R710,711	R0067224	RES ARRAY,1/16W 4X4.7K J
R727	R0067304	RES ARRAY,1/16W 4X10K J
R728	R0092704	RES ARRAY,1/16W 4X47 J
R731,732	R0092704	RES ARRAY,1/16W 4X47 J
R903	R0092704	RES ARRAY,1/16W 4X47 J
R911	R0092704	RES ARRAY,1/16W 4X47 J
R916	R0067304	RES ARRAY,1/16W 4X10K J
S001	E0031074	SW,SLIDE CHS-04TA
U001	S0024314	IC,TC74VHCT00F(EL)
U002	13444685	IC,74HC 574F
U003	S0025594	IC,TC74VHC163FEL
U004	S0018944	IC,TC74VHCU04F(EL)
U005	S0035143	IC,XCS10-3TQ144C
U007	5220118000	IC,TC74HC32AF-TP2
U008	5220103800	IC,TC74HC157AF-TP2
U009	S00396800B	IC,SX28AC SC2
U010	S0024464	IC,M62001FP-600D
U011	S00396700A	IC,SYS V1.00 MBM29F800BA-70PF
U011	E0033093	SOCKET,44PIN SOP IC179
U012	S0035133	IC,HD6437043AE00F
U013	S00351700C	IC,SA28AC/SS TC
U014,015	S0037443	IC,BS62LV1024TC-70
U016	S00397100A	IC,SX28AC TCR
U017	13444685	IC,74HC 574F
U018	5220116400	IC,HD74HC138FP
U019	S0025614	IC,TC74VHCT541AFEL
U101	S0020334	IC,TC74VHC04
U102	5220118000	IC,TC74HC32AF-TP2

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
U103	E0013344	CRYSTAL OSC,22.5792MHZ
U104	E00546900A	CRYSTAL OSC,49.152MHZ
U105	S0020354	IC,TC74VHC74
U106	S00177600A	IC,CLK1
U107,108	5220104000	IC,TC74HC595AF-TP2
U109	S00190600A	IC,IOX
U110	S0024353	IC,DSP TMS57070FFT
U111	S0036203	IC,T2316162A-45S
U112	S0020344	IC,TC74VHC541
U201,202	S0035714	IC,BA033FP
U203,204	S0025614	IC,TC74VHCT541AFEL
U205	S00335600A	IC,DTRS-HR DEC
U206	S00335500A	IC,DTRS-HR ENC
U207-211	S0035204	IC,71V124SA15PH-T&R
U301	S0018944	IC,TC74VHCU04F(EL)
U302	13447922	IC,NJM78L05UA-TE1
U303	5220123500	IC,MC74HC4046AF-FR1
U304	S0018944	IC,TC74VHCU04F(EL)
U305	5220123500	IC,MC74HC4046AF-FR1
U306	13447922	IC,NJM78L05UA-TE1
U307	S0029674	IC,TLC2932IPWR
U308,309	S0020354	IC,TC74VHC74
U310	S0018944	IC,TC74VHCU04F(EL)
U311	S0029674	IC,TLC2932IPWR
U401,402	S0035274	IC,MAX913CSA
U403,404	5220101800	IC,HD49229
U406	E0042034	RELAY,ATX206SA 2C,SMT
U407-409	5292811400	EMI FILTER,CHIP 10000PFT
U410	S0024314	IC,TC74VHCT00F(EL)
U501	13447922	IC,NJM78L05UA-TE1
U502	S0020064	IC,MC74HC4538AF LEFT
U503	S0024284	IC,NJM 78L09UA-TE1
U504	S0024294	IC,NJM 79L09UA-TE1
U505	S0024304	IC,NJU201AM-TE2
U506	S0018944	IC,TC74VHCU04F(EL)

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
U507	S0032804	IC,NJM082BV(TE1)
U508	S0004244	IC,LF356MX
U601-605	S0020344	IC,TC74VHC541
U606	S0024314	IC,TC74VHCT00F(EL)
U607-610	S0025614	IC,TC74VHCT541AFEL
U611	S0019594	IC,TC74VHC08F(EL)
U612	E0042034	RELAY,ATX206SA 2C,SMT
U613	S0025614	IC,TC74VHCT541AFEL
U614	S0019594	IC,TC74VHC08F(EL)
U701	5220116700	IC,HD74HC240FP
U702	S0037124	IC,TC74LCX541F(EL)
U703	E0042034	RELAY,ATX206SA 2C,SMT
U704	5220115800	IC,MC74HC14AF
U705	S0026540	IC,M5M34051FP
U706	5220103800	IC,TC74HC157AF-TP2
U707	S0026540	IC,M5M34051FP
U801	S0026540	IC,M5M34051FP
U802	S0020064	IC,MC74HC4538AF LEFT
U803	S0020354	IC,TC74VHC74
U804	S0024314	IC,TC74VHCT00F(EL)
U805	S0018944	IC,TC74VHCU04F(EL)
U806	13448089	IC,LM1881M
U807	5220102000	IC,SN74S140NS
U808	5220120700	IC,HD74HC153FPEL
U809,810	S0023994	IC,NJM4565M-T1
U901	S0025614	IC,TC74VHCT541AFEL
U902	S0036964	IC,LC89051V
U903	S0025614	IC,TC74VHCT541AFEL
U904	S0036913	IC,XCS20XL-4VQ100C
X001	E00547000A	RESONATOR,SD3 32MHZ
X501	E00331100B	RESONATOR,9.60MHZ SMT
X502	E00331000B	RESONATOR,8.82MHZ SMT

KEY PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95103000A	PCB ASSY,KEY
	*E90103000B	PCB,KEY
	E0054840	LCD,MC2004E-SYL-2
	M01077400A	COLLAR,LCD DA-98HR
	E00351400A	HARNESS ASSY,FRONT DA98
	E00620000A	HARNESS ASSY,FRONTJOG98HR
D1-55	S0022094	DIODE,1SS355
D57-64	M00572500A	LED ASSY,BAR METER 15DOT
D65	S0038240	LED,LT3ED87
D65A	M00608702A	SPACER,LH-5 L=10
D67	S0038240	LED,LT3ED87
D67A	M00608702A	SPACER,LH-5 L=10
D69	S0038240	LED,LT3ED87
D69A	M00608702A	SPACER,LH-5 L=10
D71	S0038240	LED,LT3ED87
D71A	M00608702A	SPACER,LH-5 L=10
D73	S0038240	LED,LT3ED87
D73A	M00608702A	SPACER,LH-5 L=10
D75	S0038240	LED,LT3ED87
D75A	M00608702A	SPACER,LH-5 L=10
D77	S0038240	LED,LT3ED87
D77A	M00608702A	SPACER,LH-5 L=10
D79	S0038240	LED,LT3ED87
D79A	M00608702A	SPACER,LH-5 L=10
D81-93	5225018500	LED,SLR-34DU3F
D81A-93A	5801550400	SPACER,LH-5 L=14.0
D100	5225013500	LED,SLR-34VR3F (RED)
D100A	5801550400	SPACER,LH-5 L=14.0
D125-130	5225018500	LED,SLR-34DU3F
D131	5225013600	LED,SLR-34MG3F (GRN)
D132-134	5225018500	LED,SLR-34DU3F
D135	5225013600	LED,SLR-34MG3F (GRN)
D136-139	5225018500	LED,SLR-34DU3F
D125A-136A	M00608702A	SPACER,LH-5 L=10
D137A-139A	5801550400	SPACER,LH-5 L=14.0
D140	5225013600	LED,SLR-34MG3F (GRN)
D140A	5801550400	SPACER,LH-5 L=14.0
D141	5225013600	LED,SLR-34MG3F (GRN)
D141A	5801550400	SPACER,LH-5 L=14.0
D142	5225013500	LED,SLR-34VR3F (RED)

KEY PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
D142A	5801550400	SPACER,LH-5 L=14.0
D143,144	5225018500	LED,SLR-34DU3F
D143A,144A	M00608702A	SPACER,LH-5 L=10
D145	S0038240	LED,LT3ED87
D145A	5801550400	SPACER,LH-5 L=14.0
D147	S0038240	LED,LT3ED87
D147A	5801550400	SPACER,LH-5 L=14.0
D149	S0038240	LED,LT3ED87
D149A	5801550400	SPACER,LH-5 L=14.0
P1,2	5336370000	PLUG.CONN. 8P BTK-2S-H
P3	5336288000	PLUG,CONN. S10B-PH-K-S(WHT)
P4	5336242600	PLUG,CONN. B16B-PH-K-S
P5	5336370000	PLUG,CONN. 8P BTK-2S-H
Q1	S0001054	TR,2SD1757K
Q2-6	S0001664	TR,DTC114TU-106
S1	E0000460	ENCODER,SRGPHJ
S2	E0057520	SW,LC1B-L1R-1400-11
S3	5300059900	SW,PUSH (LED GRN) PLAY
S4	5300059800	SW,PUSH (LED WHT) STOP
S5,6	E00412700A	SW,LC1B-L1W-1400-12-FF
S7-56	E0021092	SW,SKHVBH
TP5	13122939	CONN.,2P IMSA-9210B-1-02-T
U1	S0024873	IC,UPD784031GC-8BT
U2	S0022434	IC,M51957AFP-600C
U4	S0028234	IC,HD74LVC541A TSSOP
U5	13445670	IC,HD74HC573F
U6	S00384100A	IC,FRONT V1.00 M27C512-12C1
U6A	E0003273	SOCKET,IC160-0324-240*
U7	5220093300	IC,TC74HC00AF-TP2
U8	5220115800	IC,MC74HC14AF
U9-11	S0029394	IC,SN74LV138ANST-EL
U13-15	S0033394	IC,TD62M8600F-EL
U17,18	S0035690	IC,TB62701AN
X1	E0060344	RESONATOR,29.4912MHZ

IF98AD PCB ASSY (IF-AN98HR)

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106500A	PCB ASSY,IF98AD
	*E90106500A	PCB,IF98AD
	*M00319700A	WASHER,ADHESIVE 5X12X0.1T
	*5730042700	HEAT SINK,OSH-2025-SPL
	*M00617300B	REAR PANEL,AD
	*5780003006	SCREW,BIND M3X6
	*5801536400	SCREW,DSUB LOCK M2.6X0.45
	*5780023006	SCREW,BIND M3X6 (BLK NI)
D010-018	13411644	DIODE,CHIP 1SS355 TE-17
D020-028	13411644	DIODE,CHIP 1SS355 TE-17
D030-038	13411644	DIODE,CHIP 1SS355 TE-17
D041-048	13411644	DIODE,CHIP 1SS355 TE-17
D060	S0035214	DIODE,HVC376B-TRF
D070	13411644	DIODE,CHIP 1SS355 TE-17
J010	E0032220	CONNECTOR,DSUB 25PIN
L010	E0054724	COIL,LQH3C100K24
L011-018	E0054804	BEAD COIL,BLM21B121SDPT
L020	E0054724	COIL,LQH3C100K24
L021-028	E0054804	BEAD COIL,BLM21B121SDPT
L030	E0054724	COIL,LQH3C100K24
L040	5286051500	COIL,CHIP 2.7UH K LK2125
L501-504	E0054724	COIL,LQH3C100K24
P010	5334079300	PLUG,CONN. 100P
P020	5336303400	PLUG,CONN. B4B-EH (WHT)
R370	11985206	R,ARRAY CHIP 4X10K J
U010	S00396900C	IC,SX28AC AIO
U011-018	5220450400	IC,NJM5532M-T2
U020,030	13444677	IC,74HC541F
U050,060	13447952	IC,NJM7805FA
U070	13447952	IC,NJM7805FA
U080	5220123500	IC,MC74HC4046AF-FR1
U090	E00581800A	RESONATOR,COC22AT24.57MHZ
U100	E00581900A	RESONATOR,COC22AT22.57MHZ
U110	S0018944	IC,TC74VHCU04F(EL)
U120	S0022470	IC,TC74VHC00F
U130,140	S0025594	IC,TC74VHC163FEL
U150	S0020354	IC,TC74VHC74
U160,170	S0019610	IC,TC74VHC153F
U180	13445582	IC HD74HC4538FP
U190	S0024464	IC,M62001FP-600D
U200	S0022470	IC,TC74VHC00F
U501-504	S0035284	IC,AK5393

IF98DA PCB ASSY (IF-AN98HR)

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106600A	PCB ASSY,IF98DA
	*E90106600A	PCB,IF98DA
	*5730042700	HEAT SINK,OSH-2025-SPL
	*M00617301B	REAR PANEL,DA
	*5780003006	SCREW,BIND M3X6
	*5801536400	SCREW,DSUB LOCK M2.6X0.45
	*5780023006	SCREW,BIND M3X6 (BLK NI)
D010	13411644	DIODE,CHIP 1SS355 TE-17
D020	13411644	DIODE,CHIP 1SS355 TE-17
D030	13411644	DIODE,CHIP 1SS355 TE-17
D060	S0035214	DIODE,HVC376B-TRF
D070	13411644	DIODE,CHIP 1SS355 TE-17
D501-504	13411644	DIODE,CHIP 1SS355 TE-17
J010	E0032220	CONNECTOR,DSUB 25PIN
L010	E0054724	COIL,LQH3C100K24
L011-018	E0054804	BEAD COIL,BLM21B121SDPT
L020	E0054724	COIL,LQH3C100K24
L021-028	E0054804	BEAD COIL,BLM21B121SDPT
L030	E0054724	COIL,LQH3C100K24
L040	5286051500	COIL,CHIP 2.7UH K LK2125
P010	5334079300	PLUG,CONN. 100P
P020	5336303400	PLUG,CONN. B4B-EH (WHT)
Q011-018	S0016434	TR,2SD1328T/S
Q021-028	13428276	TR,DTA114EKAT-146
Q031-038	13428286	TR,DTC114EKAT-146
Q501-504	S0019224	TR,DTC143XUA T106
R360,370	11985206	R,ARRAY CHIP 4X10K J
U010	S00396900C	IC,SX28AC AIO
U011	5220450400	IC,NJM5532M-T2
U013	5220450400	IC,NJM5532M-T2
U015	5220450400	IC,NJM5532M-T2
U017	5220450400	IC,NJM5532M-T2
U020	13444677	IC 74HC 541F
U021-028	5220450400	IC,NJM5532M-T2
U030	13444677	IC 74HC 541F
U031-038	5220450400	IC,NJM5532M-T2
U040	5220118000	IC,TC74HC32AF-TP2
U050,060	13447952	IC,NJM7805FA
U070	13447952	IC,NJM7805FA
U080	5220123500	IC,MC74HC4046AF-FR1
U090	E00581800A	RESONATOR,COC22AT24.57MHZ
U100	E00581900A	RESONATOR,COC22AT22.57MHZ
U110	S0018944	IC,TC74VHCU04F(EL)
U120	S0022470	IC,TC74VHC00F
U130,140	S0025594	IC,TC74VHC163FEL
U150	S0020354	IC,TC74VHC74
U160,170	S0019610	IC,TC74VHC153F
U180	13445582	IC HD74HC4538FP
U190	S0024464	IC,M62001FP-600D
U200	S0022470	IC,TC74VHC00F
U501-504	S0035234	IC,AK4393
U511-514	5220450400	IC,NJM5532M-T2
U521-524	E0058404	RELAY,ATX203SA(12V)

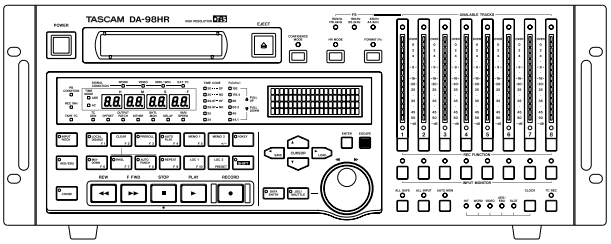
8. INCLUDED ACCESSORIES
付属品

INCLUDED ACCESSORIES (DA-98HR)

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	*D00539500A	OWNER'S MANUAL,JAPANESE [J]	
	*D00539600A	OWNER'S MANUAL,ENGLISH [EXCEPT J]	
	*D00563400A	OUTLINE MANUAL,ENGLISH [EXCEPT J]	
	*T00030500A	CLEANING TAPE,HC-8	
	5740004100	MOUNT SCREW KIT,DX-2D	
	5350014400	AC CORD ASSY [J]	
	5350018800	AC CORD SET,W/PLUG [US/C]	
	15922303	3-WIRED CORD SET [E,K]	
	5350018500	3-WIRED CORD SET (13A FUSE) [UK]	
	5350018600	3-WIRED CORD SET [A]	
	5347009000	ADAPTOR,KPR-18 [J]	

INCLUDED ACCESSORIES (IF-AN98HR)

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	*D00562700A	OWNER'S MANUAL,JAPANESE IF-AN98HR [J]	
	*D00562800A	OWNER'S MANUAL,ENGLISH IF-AN98HR [EXCEPT J]	



TASCAM
TEAC Professional Division

SERVICE MANUAL

DA-98HR

Digital Multitrack Recorder

INSTRUCTIONS FOR SERVICE PERSONNEL

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

Effective : October, 2000 4A3489

S-0029

CONTENTS

1. SPECIFICATIONS ····· 3
2. TECHNICAL INFORMATION ····· 7
2-1. Activation of test mode ····· 7
2-2. Activation of VTR mode ····· 7
2-3. Displaying ROM version numbers ····· 7
2-4. Displaying SUB MPU version numbers ····· 7
2-5. Displaying the voltage of battery ····· 7
2-6. Displaying the hed drum utilized time ····· 7
2-7. Displaying the servo error history ····· 7
2-8. KEY PCB check mode ····· 8
2-9. How to use the built-in oscillator ····· 8
2-10. Removing the FRONT MPU ····· 8
2-11. Removing the SYS ROM ····· 8
2-12. Checking the optional IF-AN98HR (A/D board and D/A board) ····· 9
2-13. Changeover of Reference level ····· 9
2-14. EXTERNAL CONTROL I/O ····· 12
3. ASSEMBLING THE MECHANISM ASS'Y ····· 19
3-1. Flowchart of assembling ····· 19
3-2. Installation of the mechanical parts ····· 20
4. MECHANISM ADJUSTMENTS ····· 26
4-1. Preparation ····· 27
4-2. Test tape ····· 27
4-3. Adjusting the tension arm position ····· 28
4-4. Adjusting the torque ····· 28
4-5. Adjusting the tape travel ····· 29
4-6. Confirming the travel in F.FWD, REW and REV mode ····· 32
5. ELECTRICAL ADJUSTMENTS ····· 35
5-1. Check and adjustment points ····· 35
5-2. Test tape ····· 36
5-3. +5 V supply check ····· 36
5-4. P.G. (Phase generator) position adjustment ····· 36
5-5. Offset adjustment in the VCO free-running frequency automatic compensation circuit ····· 37
5-6. Playback equalizer adjustment ····· 38
5-7. RF level check ····· 39
5-8. Playback error rate check ····· 40
5-9. Recording current adjustment ····· 41
5-10. Recording/playback RF level check ····· 43
5-11. Recording/playback error rate check ····· 43
6. EXPLODED VIEWS AND PARTS LIST ····· 45
7. PC BOARDS AND PARTS LIST ····· 53
8. INCLUDED ACCESSORIES ····· 71

目 次

1. 仕様 ····· 3
2. テクニカルインフォメーション ····· 7
2-1. テストモードの起動 ····· 7
2-2. VTRモードの起動 ····· 7
2-3. ROMのバージョン表示 ····· 7
2-4. SUB MPUのバージョン表示 ····· 7
2-5. バッテリーの電圧表示 ····· 7
2-6. ドラム回転積算時間の表示 ····· 7
2-7. サーボエラー履歴の表示 ····· 7
2-8. KEY PCBチェックモード ····· 8
2-9. 内臓オシレーターの使用方法 ····· 8
2-10. FRONT MPUの外し方 ····· 8
2-11. SYS ROMの外し方 ····· 8
2-12. オプション IF-AN98HR（A/Dボード, D/Aボード）のチェックについて ····· 9
2-13. リファレンスレベルの変更について ····· 9
2-14. EXTERNAL CONTROL I/Oについて ····· 12
3. メカ ASS'Yの組立 ····· 19
3-1. 組立のフローチャート ····· 19
3-2. メカ部品の取付け ····· 20
4. 機構部調整 ····· 26
4-1. 準備 ····· 27
4-2. テストテープ ····· 27
4-3. テンションアーム位置調整 ····· 28
4-4. トルク調整 ····· 28
4-5. テープ走行調整 ····· 29
4-6. FF, REW, REV モードでの走行確認 ····· 32
5. 電気系調整 ····· 35
5-1. 測定箇所および調整箇所 ····· 35
5-2. テストテープ ····· 36
5-3. 電源＋5Vの確認 ····· 36
5-4. PG（Phase Generator）位置調整 ····· 36
5-5. VCOフリーラン周波数自動補正回路のオフセット調整 ····· 37
5-6. 再生イコライザー調整 ····· 38
5-7. RFレベル確認 ····· 39
5-8. 再生エラーレート確認 ····· 40
5-9. 記録電流調整 ····· 41
5-10. 記録再生 RFレベル確認 ····· 43
5-11. 記録再生エラーレート確認 ····· 43
6. 分解図とパーツリスト ····· 45
7. 基板図とパーツリスト ····· 53
8. 付属品 ····· 71

1. SPECIFICATIONS
仕様

Tape recorder section

Format:	DTRS format
Recording method:	Rotary-head, helical-scan method
Tape type:	Hi8 MP tape / Hi8 ME
Head construction:	2 x record, 2 x playback
Tracking method:	ATF (Automatic Track Finding)
Erasure method:	Overwrite
Drum speed:	2,000 r.p.m.
Tape speed:	15.955 mm/sec.
Equivalent tape speed:	4.2 m/sec.
Maximum recording time:	108 min. (using P6-120 tape)
Time to play from stop:	Less than 2 seconds
Fast forward/rewind time:	80 seconds (using P6-120 tape)
Search speed:	Maximum of 100 x play speed
Shuttle speed:	Forward and reverse at 8.0, 4.0, 2.0, 1.0, 0.5 and 0.25 play speed (1.0 speed available only in forward shuttle mode)
Vari speed:	±6% (0.1% steps)
Positioning accuracy:	To 1 sample
Positioning lock time:	Within 8 seconds (when locating 2 DA-98HRs synced together)
Number of recording tracks:	8
Sub-code:	ABS track, SMPTE/EBU timecode facility
Error correction:	Double- encoded Reed-Solomon code
Sampling frequency:	44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz
Recording resolution:	16/24 bits linear
Cross-fade time:	10 ms to 200 ms (10 ms increments)
Track delay:	–200 to +7,200 samples (–4 to +150 ms) in single-unit increments. Can be set in samples or ms.
Offset:	±2 hours (to frame accuracy)
Sync clock:	Internal, WORD or VIDEO
MIDI function:	MMC (MIDI Machine control) MTC (MIDI timecode) output TASCAM System Exclusive (track delay, etc.) Control Cahnge (mixdown)
Supported timecode formats:	SMPTE 30, 29.97 drop, 29.97 non-drop, EBU 25 and Film 24 fps with telecine pull-up and pull-down facilities

定格

録音フォーマット：	DTRSフォーマット
記録方式：	回転ヘッド式ヘリカルスキャン方式
使用テープ：	Hi8-ME および Hi8-MPテープ
ヘッド構成：	記録用×2　再生用×2
トラッキング方式：	ATF (Automatic Track Finding)
消去方法：	オーバーライト消去
ドラム回転数：	2,000 rpm.
テープ速度：	15.955 mm/sec
記録相対速度：	4.2 m/sec
記録時間：	108分（P6-120分テープ使用時）
再生立ち上がり時間：	2秒以内
早送り／巻き戻し時間：	約80秒（P6-120分テープ使用時）
サーチ速度：	最大100倍
シャトル速度：	正方向：×8,4,2,1,1/2,1/4 倍 逆方向：×8,4,2,1/2,1/4 倍
ピッチコントロール：	±6%（0.1%単位）
調整精度：	1 サンプル未満
調相時ロック時間：	8秒以内（DA-98HR 2 台同期時）
記録チャンネル数：	最大8チャンネル
サブコード：	ABSタイム、SMPTE/EBUタイムコード記録可能
誤り訂正方式：	ダブルエンコーデッドリードソロモンコード
サンプリング周波数：	44.1kHz、48kHz、88.2kHz、96kHz、176.4kHz、192kHz
録音ビット：	16ビット、24ビット
基準レベル：	フルビット ー16、ー18、ー20dB 切替可能
エンファシス時定数：	50 μsec／15 μsec（再生時のみ自動選択）
クロスフェード時間：	10～200 msec（10msec 単位）
トラックディレイ：	ー200～+7200サンプル（1 サンプル単位）またはー4msec～+150msec（1msec 単位）
ABSタイムオフセット：	±2時間（フレーム単位）
シンククロック：	INT／WORD／VIDEO
MMCコントロール：	トラックディレイ、トラックコピー（システムエクスクルーシブメッセージ）
対応タイムコード：	SMPTE 30、29.97ドロップfps、29.97ノンドロップfps、EBU 25fps、フィルム 24fps

Inputs and outputs

TDIF-1 (DIGITAL I/O):	25-pin D-sub TDIF-1 format
DIGITAL (AES/EBU):	25-pin D-sub PRO AES3-1992 Amendment 3-1999
REMOTE IN/SYNC IN:	15-pin D-sub Conforms to REMOTE IN/SYNC IN protocol
SYNC OUT:	15-pin D-sub Conforms to REMOTE IN/SYNC IN protocol
WORD SYNC IN/THRU:	BNC connector, 75 Ω at TTL level ON/OFF (THRU auto-terminated)
WORD SYNC OUT:	BNC connector, 75 Ω at TTL level
TIME CODE IN:	XLR-3 balanced Input impedance: 10 kΩ Input level: 0.5 Vp-p to 10.0 Vp-p
TIME CODE OUT:	XLR-3 balanced Output impedance: 100Ω Output level: 2.0 Vp-p
MIDI:	IN, OUT, THRU
VIDEO IN/THRU:	NTSC or PAL Negative Sync Composite video, Sync Composite Video or Frame Pulse (auto detect) 1 Vp-p, ±0.2 V (Negative Sync Composite video or Sync Composite Video) TTL Level (Frame pulse) THRU autmatically terminated (75 Ω)
CONTROL I/O:	37-pin D-sub
RS-422:	9-pin D-sub Comforms to RS-422 specifications
METER UNIT:	15-pin D-sub

Physical specifications

Size (exc feet): w x h x d	482 x 176 x 356 (mm) 19 x 6.9 x 14 (in)
Weight:	11 kg (24 lb)

Power specifications

Power requirements:	USA/Canada 120 VAC, 60 Hz U.K./Europe 230 VAC, 50 Hz Australia 240 VAC, 50 Hz
Power consumption:	30 W (IF-AN98HR installed: 46 W)
Applicable electromagnetic environment:	E4
Peak inrush current:	15.5 A (230 V, all options fitted)

入出力

TDIF-1（DIGITAL I/O）:	TDIF-1［不平衡、D－Sub 25ピン、メス］
DIGITAL (AES/EBU) :	PRO AES3-1992 Amendment 3-1999準拠［D-Sub 25ピン］
REMOTE IN/SYNC IN :	REMOTE IN/SYNC IN プロトコル［D-Sub 15ピン、メス］
SYNC OUT :	REMOTE IN/SYNC IN プロトコル［D-Sub 15ピン、メス］
WORD SYNC IN :	TTLレベル相当／75Ωターミネート［BNC］
WORD SYNC OUT :	TTLレベル相当［BNC］
WORD SYNC THRU :	接続時、WORD SYNC INのターミネートオフを自動認識 自動オン／オフ方式［BNC］
TIME CODE IN :	0.5Vp-p ～ 10Vp-p／10kΩ ［平衡、XLR-3-31］
TIME CODE OUT :	2Vp-p／100Ω［平衡、XLR-3-32］
MIDI IN :	[DIN 5ピン]
MIDI OUT :	[DIN 5ピン]
MIDI THRU :	[DIN 5ピン]
VIDEO IN :	NTSC/PAL 75Ωターミネート [BNC] ネガティブシンクコンポジットビデオ、シンクコンポジットビデオ、フレームパルス（自動検出）、1Vp-p ±0.2V（ネガティブシンクコンポジットビデオ、シンクコンポジットビデオ）、TTLレベル相当（フレームパルス）
VIDEO THRU :	接続時、VIDEO INのターミネートオフを自動認識 自動オン／オフ方式「BNC]
CONTROL I/O :	[D-Sub 37ピン]
RS-422 :	[D-Sub 9ピン]
METER UNIT :	[D-Sub 15ピン、メス]

一般

電源：	100V AC 50-60Hz
消費電力：	30W（IF-AN98HR 装着時 46W）
質量：	11kg
外形寸法：	幅482×高さ176×奥行き356 mm（足を除く）

IF-AN98HR (Option)

All specifications refer to both D/A and A/D unless otherwise specified and are measured using Audio Precision System TWO cascade:

DTRS-HR mode

Sampling frequency:	44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz (±6%)
Sampling resolution:	24 bits
Frequency response:	
Fs=44.1 kHz, 48 kHz	20 Hz — 20,000 Hz (±0.5 dB)
Fs=96 kHz	20 Hz — 40,000 Hz (±1 dB)
THD:	< 0.004% (1 kHz, Fs=48 kHz) *
S/N, dynamic range:	> 110 dB (1 kHz, Fs=48 kHz) *
Channel separation:	> 95 dB (1 kHz)
De-emphasis:	50/15 µs
Nominal output level:	+4 dBu
Output impedance:	< 100 kΩ
Maximum output level:	20 dBu, 22 dBu, 24 dBu (selectable)
Nominal input level:	+4 dBu
Input impedance:	> 10 kΩ
Maximum input level:	20 dBu, 22 dBu, 24 dBu (selectable)

DTRS mode

As for DTRS-HR mode, except:

S/N, dynamic range:	> 100 dB (1 kHz, Fs=48 kHz) *

＊: These values are obtained with the I/O clock set to the Narrow setting.

IF-AN98HR（オプション）

● 特に明記していない項目はA/D ボード、D/A ボード共通の仕様です。
● Audio Precision System TWO cascade にて測定しています。

DTRS-HR モード

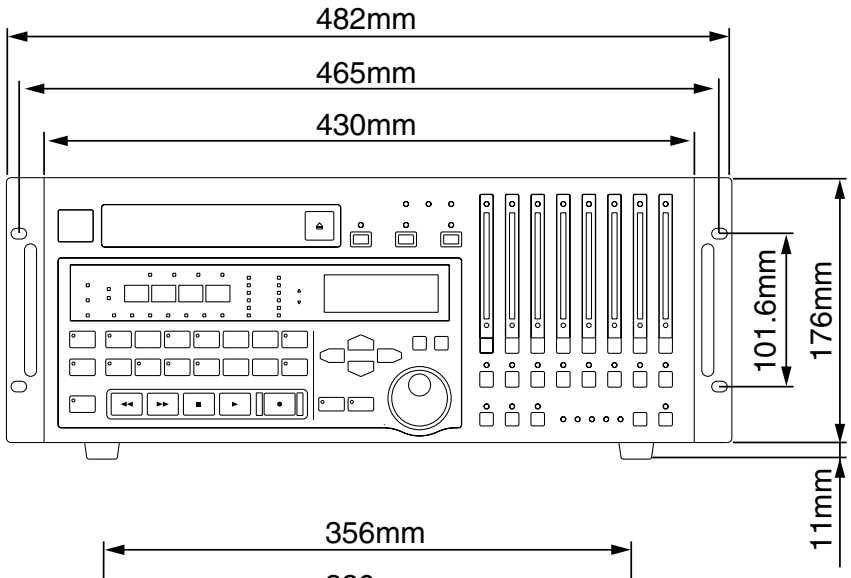
サンプリング周波数：	44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz (±6%)
サンプリング解像度：	24 ビット
録音再生周波数特性：	
Fs=44.1 kHz,48 kHz	20 Hz ～20,000 Hz (±0.5 dB)
Fs=96 kHz,88.2 kHz	20 Hz ～40,000 Hz (±1 dB)
THD＋N［22K LPF］：	0.004%以下 [1 kHz, Fs=48 kHz] * ［録音／再生時］
S/N 比、ダイナミックレンジ［22K LPF / A-Weight ］：	110 dB 以上 [1 kHz, Fs=48 kHz] * ［録音／再生時］
チャンネルセパレーション：	95 dB 以上[1 kHz]
デエンファシス：	50/15 µs
規定出力レベル：	+4 dBu
出力インピーダンス：	100 Ω以下
最大出力レベル：	20 dBu,22 dBu,24 dBu（選択可）
規定入力レベル：	+4 dBu
入力インピーダンス：	10 k Ω以上
最大入力レベル：	20 dBu,22 dBu,24 dBu（選択可）

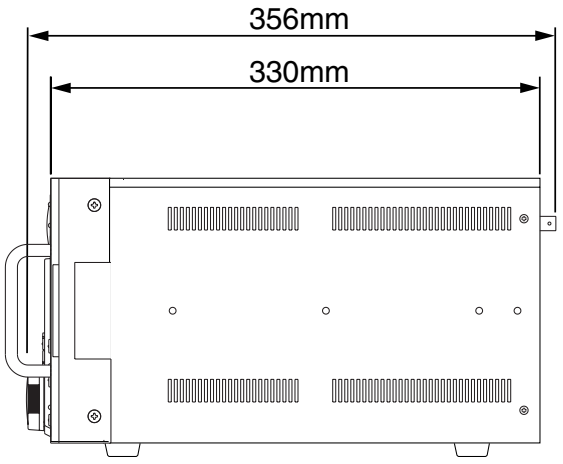
DTRS モード

［以下の項目を除いてDTRS-HR モード時と同じ］

S/N 比、ダイナミックレンジ［22K LPF / A-Weight］：	100 dB 以上 [1 kHz, Fs=48 kHz] * ［録音／再生時］

＊： I/O クロック＝Narrow 設定時の値


482mm
465mm
430mm
101.6mm
176mm
11mm


356mm
330mm

2. TECHNICAL INFORMATION

テクニカルインフォメーション

2-1. Activation of test mode

1. Hold down F.FWD + STOP + PLAY keys and press POWER key, and when "Select Mode" is displayed, let go of the three keys and, before 2 seconds is up, press STOP key. (TEST MODE should be displayed.)
2. The test mode is released when power is turned off.

2-2. Activation of VTR mode

1. Hold down F.FWD + STOP + PLAY keys and press POWER key, and when "Select Mode" is displayed, let go of the three keys and, before 2 seconds is up, press PLAY key. (VTR MODE should be displayed.)
2. The VTR mode is released when power is turned off.

2-3. Displaying ROM version numbers

1. Select the menu group F in the menu screen.
2. Move the cursor to the items shown below.
   Sys Ver : SYS ROM version
   Front Ver : FRONT MPU version
   Servo Ver : SERVO MPU version

2-4. Displaying SUB MPU version numbers

1. Enter the test mode.
2. Select the menu group N in the menu screen.
3. Move the cursor to "SubMpuVer" and press ENTER key.

2-5. Displaying the voltage of battery

1. Enter the test mode.
2. Select the menu group N in the menu screen.
3. Move the cursor to "Battery".

2-6. Displaying the hed drum utilized time

1. Select the menu group F in the menu screen.
2. Move the cursor to the items shown below.
   Dr Total : Total utilized time
   Dr Search : Fast-winded time

2-7. Displaying the servo error history

1. Enter the test mode.
2. Select the menu group M in the menu screen.
3. Move the cursor to "ServoErr" and press ENTER key.

Note)
Servo error data is stored in the SERVO PCB's EEPROM memory. As the power is unstable immediately after being turned ON, data written to the EEPROM at this time will be incorrect. To ensure accuracy, the DA-98HR prohibits data from being written to the EEPROM for 10 seconds after POWER ON. If an error occurs just 10 seconds, the error data is not stored in memory. As a result, the servo error history stored in the memory may differ from actual phenomena.

2-1. テストモードの起動

1. F FWDキー＋STOPキー＋PLAYキーを押しながら電源をONにし、“Select Mode”表示後 一旦手を離し、2秒以内にSTOPキーを押す。(TEST MODEと表示)
2. 電源をOFFにすると、テストモードが解除される。

2-2. VTRモードの起動

1. F FWDキー＋STOPキー＋PLAYキーを押しながら電源をONにし、“Select Mode”表示後 一旦手を離し、2秒以内にPLAYキーを押す。(VTR MODEと表示)
2. 電源をOFFにすると、VTRモードが解除される。

2-3. ROMのバージョン表示

1. メニュー画面で、メニューグループFを選択する。
2. カーソルを以下の項目に合わせる。
   Sys Ver : SYS ROMのバージョン
   Front Ver : FRONT MPUのバージョン
   Servo Ver : SERVO MPUのバージョン

2-4. SUB MPUのバージョン表示

1. テストモードにする。
2. メニュー画面で、グループNを選択する。
3. “SubMpuVer”にカーソルを合わせて、ENTERキーを押す。

2-5. バッテリーの電圧表示

1. テストモードにする。
2. メニュー画面で、グループNを選択する。
3. “Battery”にカーソルを合わせる。

2-6. ドラム回転積算時間の表示

1. メニュー画面で、メニューグループFを選択する。
2. カーソルを以下の項目に合わせる。
   Dr Total : トータル積算時間
   Dr Search : サーチ時 (PLAY, REC 以外) の積算時間

2-7. サーボエラー履歴の表示

1. テストモードにする。
2. メニュー画面で、メニューグループMを選択する。
3. “ServoErr”にカーソルを合わせて、ENTERキーを押す。

注)
サーボエラーはSERVO PCB内のEEPROMに記憶されていますが、POWER ON直後はまだ電源が十分安定しておらず、そのような状態でEEPROMにデータの書き込みを行うと誤ったデータを書き込んでしまいます。
そのため、DA-98HRではPOWER ON後10秒間はEEPROMへのデータの書き込みを禁止しています。したがって、POWER ON直後にサーボエラーが発生してから10秒経過する前にPOWER OFFした場合などでは、そのサーボエラーは経歴として記憶されませんので、実際の現象と記憶された情報とで差異が生じてしまう可能性があります。

2-8. KEY PCB check mode

1. While holding the PLAY, STOP, F FWD and REW key pressed, turn the power ON. In this case, all LED's light.
2. Press the STOP, F FWD, REW, PLAY or RECORD key. All LEDs go out.
3. When each key is pressed, the corresponding LED lights.

2-9. How to use the built-in oscillator

1. Enter the test mode.
2. Select the menu group 2 in the menu screen.
3. Move the cursor to "Sine Osc" and press ENTER key.
4. Use the ▲ and ▼ keys to select the output frequency (OFF, 440 Hz, 1 kHz, 10 kHz, 20 kHz, 20 Hz, wite noise). (The level is full scale.)

2-10. Removing the FRONT MPU

As shown in Fig. 2-1, hold the FRONT MPU (KEY PCB:U6) with the PLCC EXTRACTOR (P/N: 16910101) to remove it.

2-11. Removing the SYS ROM

Detach the socket cover to remove the SYS ROM (SYS PCB:U011). To remove the socket cover, slide it as shown in Fig. 2-2.

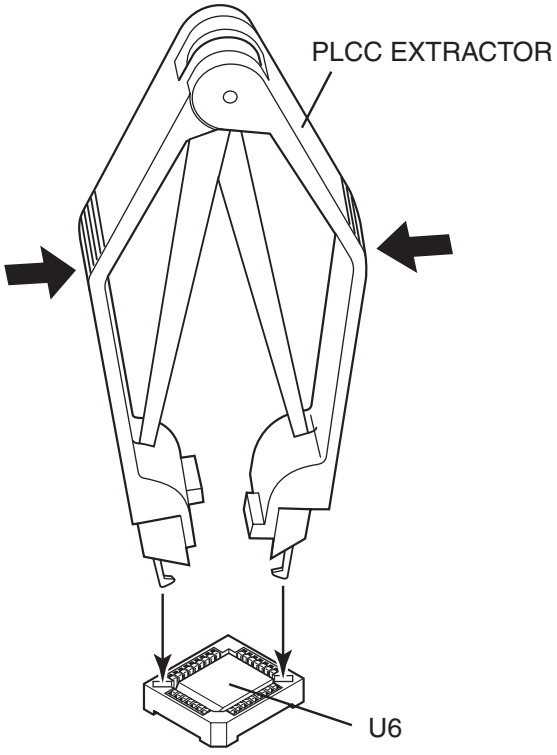


Fig. 2-1

2-8. KEY PCBチェックモード

1. PLAYキー＋STOPキー＋F FWDキー＋REWキーを押しながら電源をONにするとチェックモードに入る。このとき、LEDが全灯する。
2. STOP, F FWD, REW, PLAY, RECORDのいずれかのキーを押すと、LEDが全て消灯する。
3. その後、それぞれのキーを押すと、そのキーに対応するLEDが点灯する。

2-9. 内臓オシレーターの使用方法

1. テストモードにする。
2. メニュー画面で、メニューグループ2を選択する。
3. “Sine Osc”にカーソルを合わせてENTERキーを押す。
4. ▲キー/▼キーで、出力する周波数（OFF, 440Hz, 1kHz, 10kHz, 20kHz, 20Hz, White noise）を選択する。（レベルはフルスケール）

2-10. FRONT MPUの外し方

図2-1のように、PLCC EXTRACTOR（品番:16910101）でFRONT MPU（KEY PCB:U6)を挟んで取り外します。

2-11. SYS ROMの外し方

SYS ROM（SYS PCB:U011）はソケットカバーを取り外すことにより、外すことができます。
ソケットカバーは、図2-2のようにスライドさせることにより取り外します。

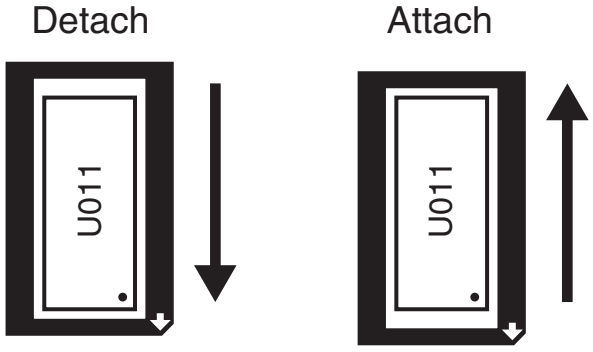


Fig. 2-2

2-12. Checking the optional IF-AN98HR (A/D board and D/A board)

To check the A/D board and D/A board, connect the EXTENSION PCB (P/N : 5200353800) to each board.
Note)
The EXTENSION PCB cannot be connected to the SYS PCB.

2-13. Changeover of Reference level

By replacing jumpers on the A/D and D/A boards, you can set the unit for one of the following reference levels.

Standard	Reference level	Nominal level	Maximum lelel
TASCAM	–16 dBFS	+4 dBu	+20 dBu
European	–18 dBFS	+4 dBu	+22 dBu
SMPTE	–20 dBFS	+4 dBu	+24 dBu

Depending on the required reference level, plug in jumpers as shown below. (See also figures 2-3 and 2-4.)

A/D board (ANALOG INPUT)

	–16 dBFS	–18 dBFS	–20 dBFS
W031 – 038	–	●	●
W041 – 048	–	–	●
W010	●	–	–
W020	–	●	–
W030	–	–	●

D/A board (ANALOG OUTPUT)

	–16 dBFS	–18 dBFS	–20 dBFS
W011 – 018	●	●	–
W021 – 028	●	–	–
W010	●	–	–
W020	–	●	–
W030	–	–	●

● : jumper plugged in (closed)
ー : jumper not plugged in (open)

2-12. オプション IF-AN98HR（A/Dボード, D/Aボード）のチェックについて

A/Dボード, D/Aボードのチェックの際は、EXTENSION PCB（品番:5200353800）を各PCBに接続してください。
注）EXTENSION PCBはSYS PCBには接続できません。

2-13. リファレンスレベルの変更について

A/Dボード, D/Aボード上のショートピンを差し換えることにより、以下の3種類の中からリファレンスレベルを選択することができます。

スタンダード	リファレンスレベル	基準レベル	最大レベル
TASCAM	－16 dBFS	+4 dBu	+20 dBu
ヨーロッパ	－18 dBFS	+4 dBu	+22 dBu
SMPTE	－20 dBFS	+4 dBu	+24 dBu

リファレンスレベルに応じて、ショートピンを下表のように設定します。（図2-3, 2-4 参照）

A/Dボード（ANALOG INPUT）

	－16 dBFS	－18 dBFS	－20 dBFS
W031～038	–	●	●
W041～048	–	–	●
W010	●	–	–
W020	–	●	–
W030	–	–	●

D/Aボード（ANALOG OUTPUT）

	－16 dBFS	－18 dBFS	－20 dBFS
W011～018	●	●	–
W021～028	●	–	–
W010	●	–	–
W020	–	●	–
W030	–	–	●

●：ショートピンを差す（クローズ）
ー：ショートピンを差さない（オープン）

A/D board

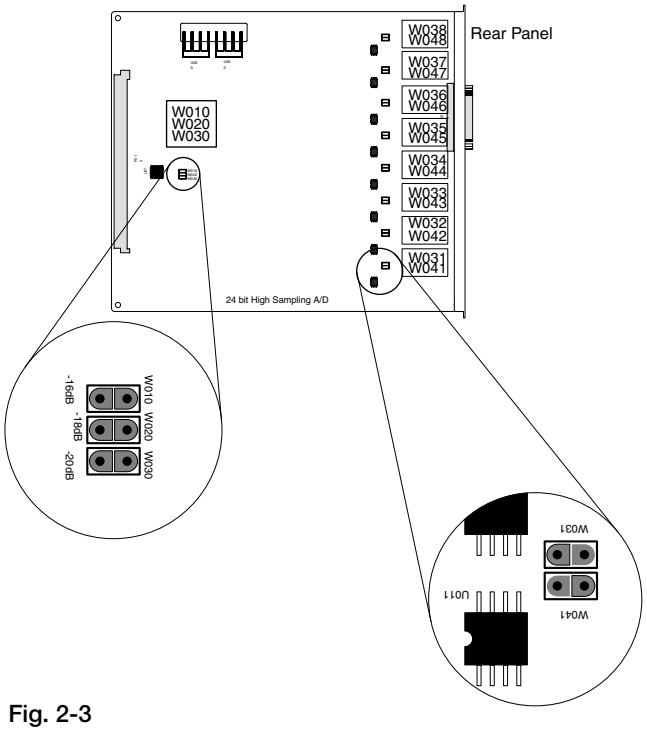
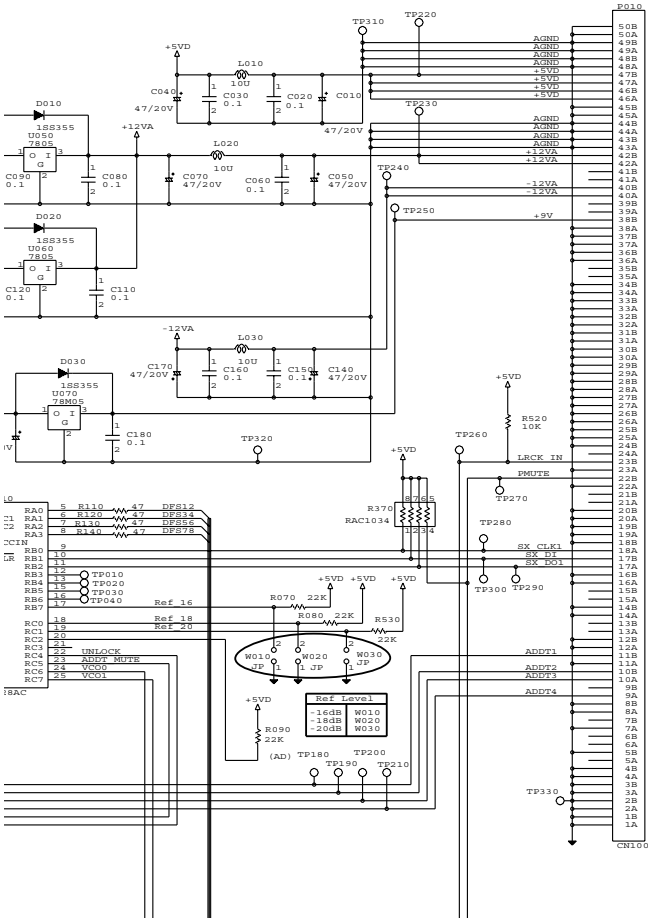
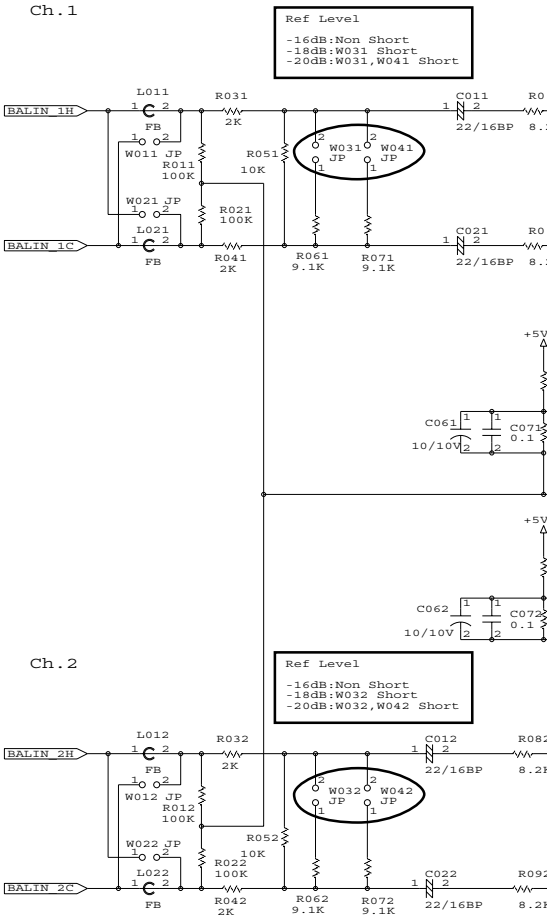


Fig. 2-3





D/A board

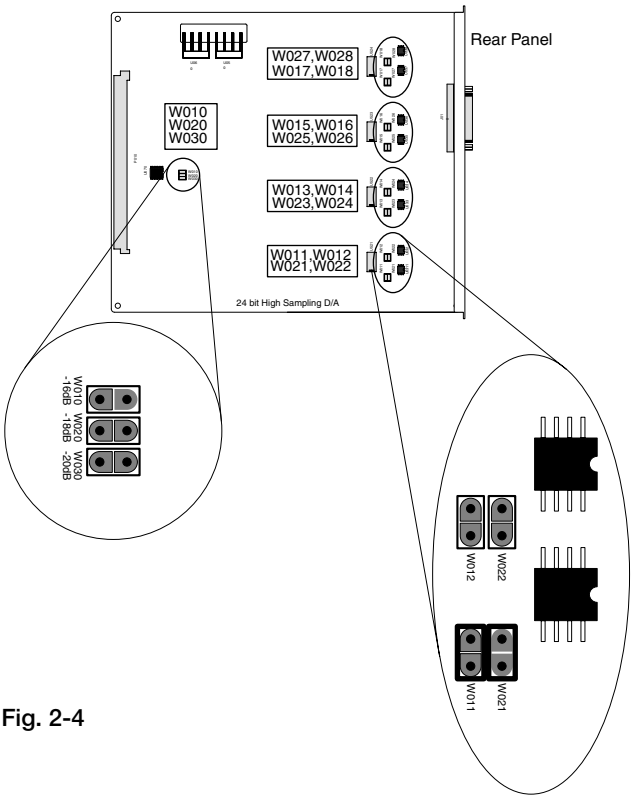
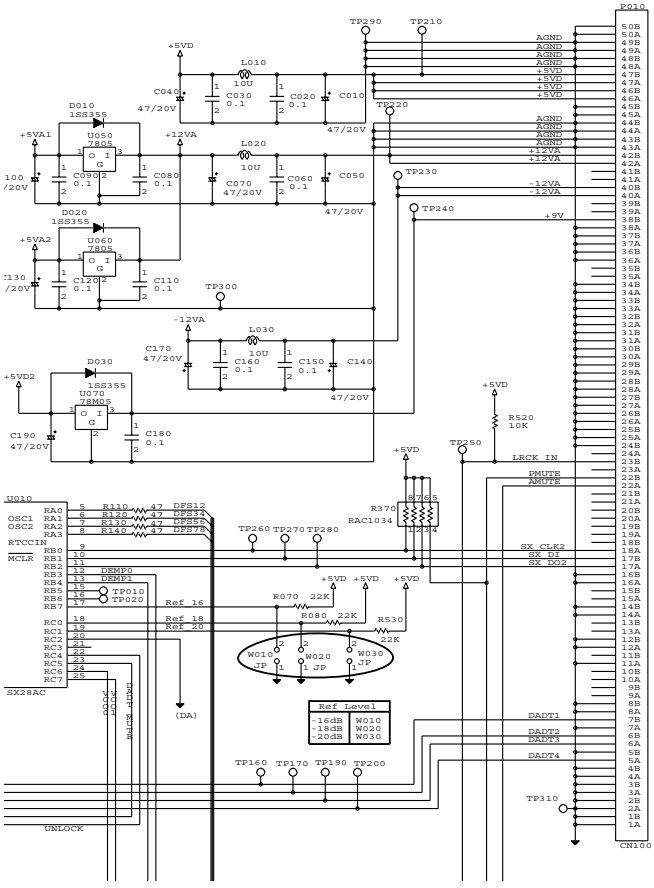
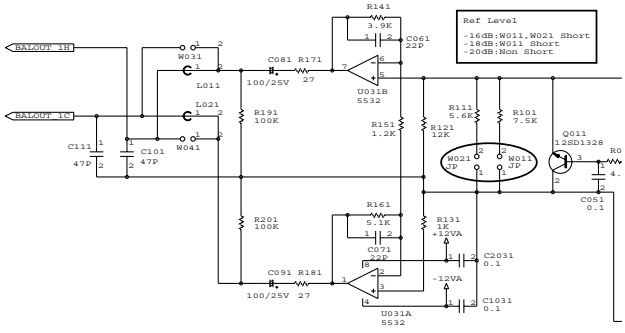


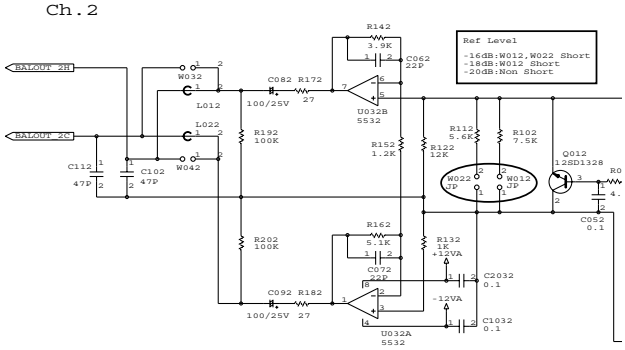
Fig. 2-4



Ch.1



Ch.2



2-14. EXTERNAL CONTROL I/O

A CONTROL I/O connector is provided to enable external control of the DA-98HR. Transport control (+Chase) inputs and related tally (+Lock) outputs are readily available.
To enable further capability of REC FUNCTION and INPUT MONITOR inputs and its related tally outputs, the CONTROL I/O also consists of signals for serial communication data.

- The connector is a 37-pin D-sub and the output is an open collector. Each transistor supports a current of up to 50 mA.
  Input is at TTL level with 74LS240 of the LS-TTL used as a buffer (with Schmitt trigger).
- Power supplied from the DA-98HR is up to 50 mA at DC 5 V.
- The control system data output is 32-bit serial sync, of which 8 bits are output in parallel simultaneously.
  Input is 32-bit serial sync. The preceding 8 bits are merged with the parallel input.

The pin assignment, serial input/output signal format and recommended circuits for a controlling device are described here in after.

2-14. EXTERNAL CONTROL I/Oについて

CONTROL I/Oは外部からDA-98HRをコントロールするために設けられた端子です。トランスポートコントロール（＋チェース）入力と、そのタリー（＋ロック）を出力します。また、REC FUNCTION、INPUT MONITORのキー入力と、そのタリーを出力することを可能とするために、シリアル通信用信号も用意されています。

- 端子は D-sub 37pin、出力はオープンコレクターで各トランジスターは 50mAまで電流を流すことができます。
  入力はTTLレベルで、バッファとしてLS-TTLの74LS240を使用（シュミットトリガ付き）しています。
- DA-98HRから供給できる電源は DC5Vで 50mAまで可能です。
- コントロール系のデータの出力は、シリアル同期式 32ビット、そのうち 8ビットがパラレル出力され、入力はシリアル同期式 32ビット、先行 8ビットがパラレル入力とマージされます。

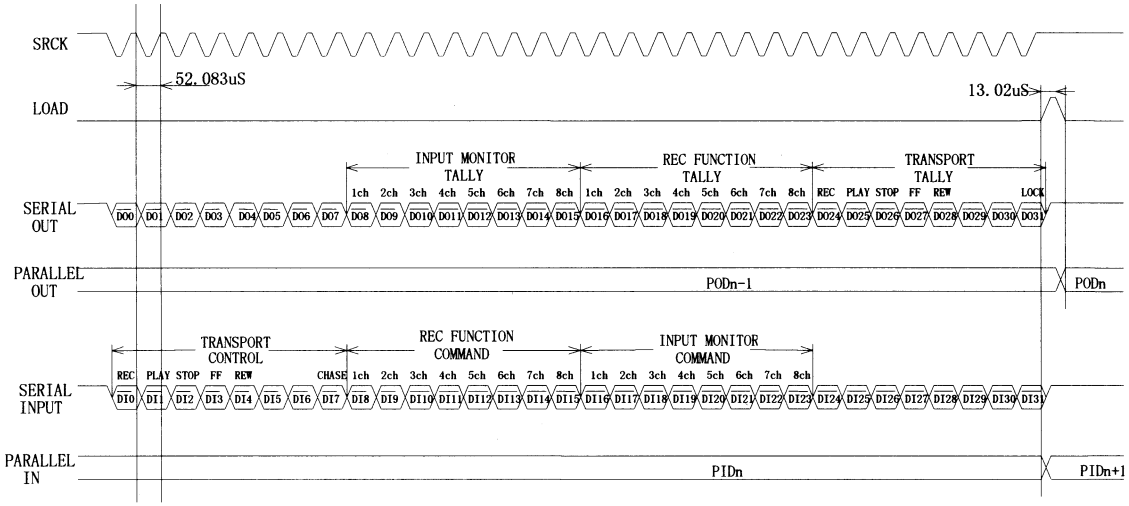
以下に、ピンアサイン、シリアル入出力信号フォ-マット、リモコンを作るときの推奨回路を記載します。

J11 Pin Assignment

Pin No.	Pin No.	Signal	Function	Input/output state
1		PLAY	PLAY command input	TTL
	20	GND	GND	GND
2		FF	FF command input	TTL
	21	SERIAL OUT	Serial data output	Open Collector
3		REW	REW command input	TTL
	22	NC	No connection　未使用端子	
4		AUX1	Auxiliary 1 input　予備1 入力	TTL
	23	SERIAL IN	Serial data input	TTL
5		STOP	Stop command input	TTL
	24	NC	No connection　未使用端子	
6		REC	REC command input	TTL
	25	NC	No connection　未使用端子	
7		AUX2	Auxiliary 2 input　予備2 入力	TTL
	26	NC	No connection　未使用端子	
8		CHASE	CHASE command input	TTL
	27	NC	No connection　未使用端子	
9		NC	No connection　未使用端子	
	28	NC	No connection　未使用端子	
10		GND	GND	GND
	29	NC	No connection　未使用端子	
11		PLAY TALLY	PLAY tally output	Open collector
	30	NC	No connection　未使用端子	
12		FF TALLY	FF tally output	Open collector
	31	NC	No connection　未使用端子	
13		REW TALLY	REW tally output	Open collector
	32	SRCK	Shift resister clock output	Open collector
14		STOP TALLY	STOP tally output	Open collector
	33	NC	No connection　未使用端子	
15		REC TALLY	REC tally output	Open collector
	34	LOAD	Load pulse output	Open collector
16		LOCK TALLY	LOCK tally output	Open collector
	35	NC	No connection　未使用端子	
17		AUX 1 TALLY	Auxiliary 1 output　予備1 出力	Open collector
	36	GND	GND	GND
18		AUX 2 TALLY	Auxiliary 2 ouput　予備2 出力	Open collector
	37	VCC +5V	Power supply DC +5V	DC5V
19		ACTIVE SENSE	Active sensse input ＊	TTL

＊: is to be connected to GND in the controlling device side to activate any tally output.
＊: はタリー出力を有効とするために、リモコン側でGNDに接続するものです。

CONTROL I/O Serial Input/output signal format



DA-98HR OUTPUT DATA（OPEN COLLECTOR）

DO0～DO7 : Undefined　未定義
DO8～DO15 : TALLY OF INPUT MONITOR（1ch, 2ch .... 8ch）
DO16～DO23 : TALLY OF REC FUNCTION（1ch, 2ch .... 8ch）
DO24 : REC TALLY
DO25 : PLAY TALLY
DO26 : STOP TALLY
DO27 : FF TALLY
DO28 : REW TALLY
DO29, DO30 : Undefined　未定義
DO31 : LOCK TALLY

DA-98HR INPUT DATA（TTL LEVEL）

DI0 : REC COMMAND
DI1 : PLAY COMMAND
DI2 : STOP COMMAND
DI3 : FF COMMAND
DI4 : REW COMMAND
DI5, DI6 : Undefined　未定義
DI7 : CHASE COMMAND
DI8～DI15 : REC FUNCTION COMMAND（1ch, 2ch .... 8ch）
DI16～DI23 : INPUT MONITOR COMMAND（1ch, 2ch .... 8ch）
DI24～DI31 : Undefined　未定義

Recommended circuit for a controlling device

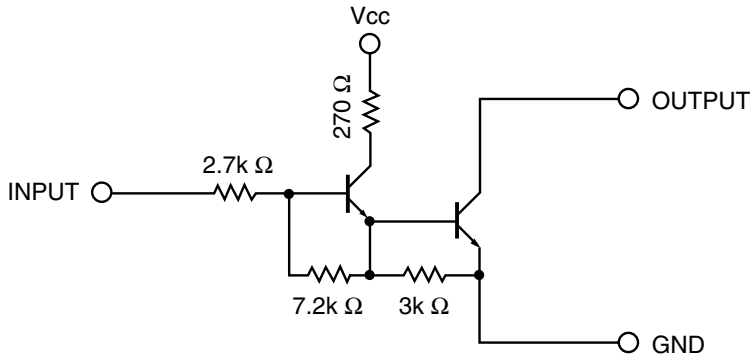
For detailed schematics of the circuit, refer to Figs. 2-5 and 2-6.

- The equivalent circuit (for one gate) of the transistor array TD62381F (P/N: S0036924) which is used for the CONTROL I/O parallel output is shown below.

リモコンの推奨回路について

具体的な回路については、図2-5, 2-6を参照してください。

- CONTROL I/Oのパラレル出力に使用されているトランジスターアレー TD62381F（品番: S0036924）の等価回路（1回路分）は以下の通りです。



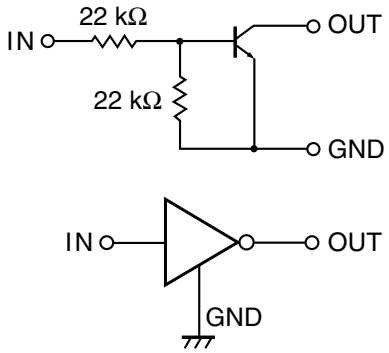
Contents 内 容		Condition 条 件	Min. 最小	Max. 最大
I_{OUT}	Current for one gate when 8 circuits operate 8回路動作時の1回路あたりの電流	Duty=10 %	0 mA	400 mA
		Duty=50 %	0 mA	330 mA
$V_{ce\ (sat)}$	Saturation voltage between collector and emitter コレクターエミッタ間飽和電圧	I_{OUT}=500 mA		0.9 V
		I_{OUT}=350 mA		0.7 V

Note) When using the power supply (DC 5 V) from the DA-98HR, suppres all curent consumption to less than 50 mA.

注) DA-98HRからの電源（DC 5V)を使用する場合は、全消費電流を50 mA以下に抑えてください。

● The equivalent circuit of the transistor DTC124EKA (P/N: 13428287) which is used for the CONTROL I/O serial output is shown below.

● CONTROL I/Oのシリアル出力に使用されているトランジスター DTC124EKA（品番: 13428287）の等価回路は以下の通りです。



	Typ. 標 準	Max. 最 大	Conditon 条 件
V_O	0.1 V	0.3 V	I_O=10 mA, I_I=0.5 mA
I_I		0.36 mA	V_{II}=5 V
I_O		0.5 μA	V_{CC}=50 V, V_I=0 V

Note) When connecting more than one unit or when this unit incorporated in a system with high power comsumption, isolate the inputs/outputs from DA-98HR with a photo-coupler.

注）複数台の機器を接続する場合や消費電力の大きな機器に組み込む場合は、入出力をフォトカプラでアイソレーションしてください。

Recommended Circuit (For Basic Control)　推奨回路 1（BASIC CONTROL用）

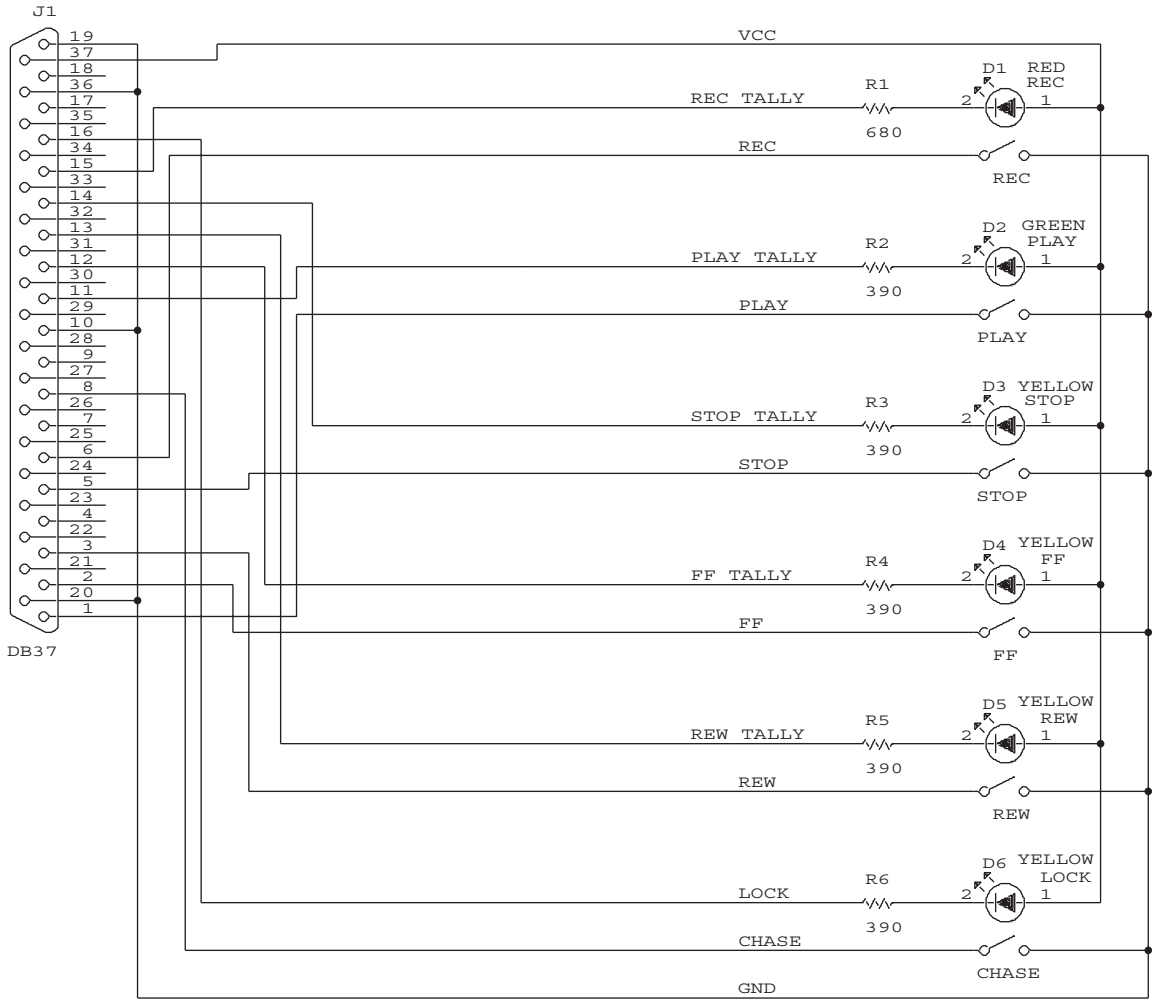


Fig. 2-5

Recommended Circuit (For Full Function)　推奨回路 2（FULL FUNCTION用）

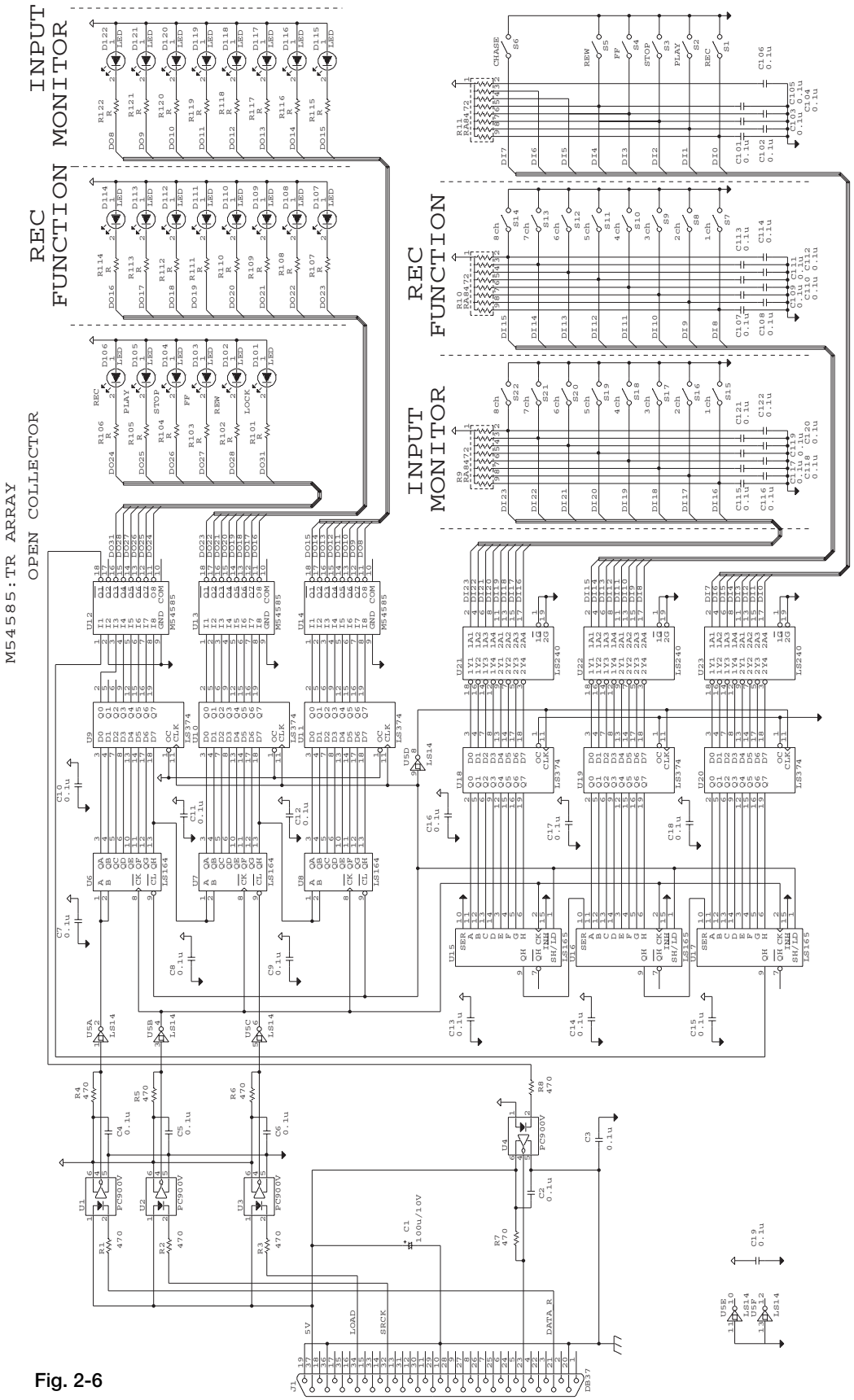


Fig. 2-6

3. ASSEMBLING THE MECHANISM ASS'Y

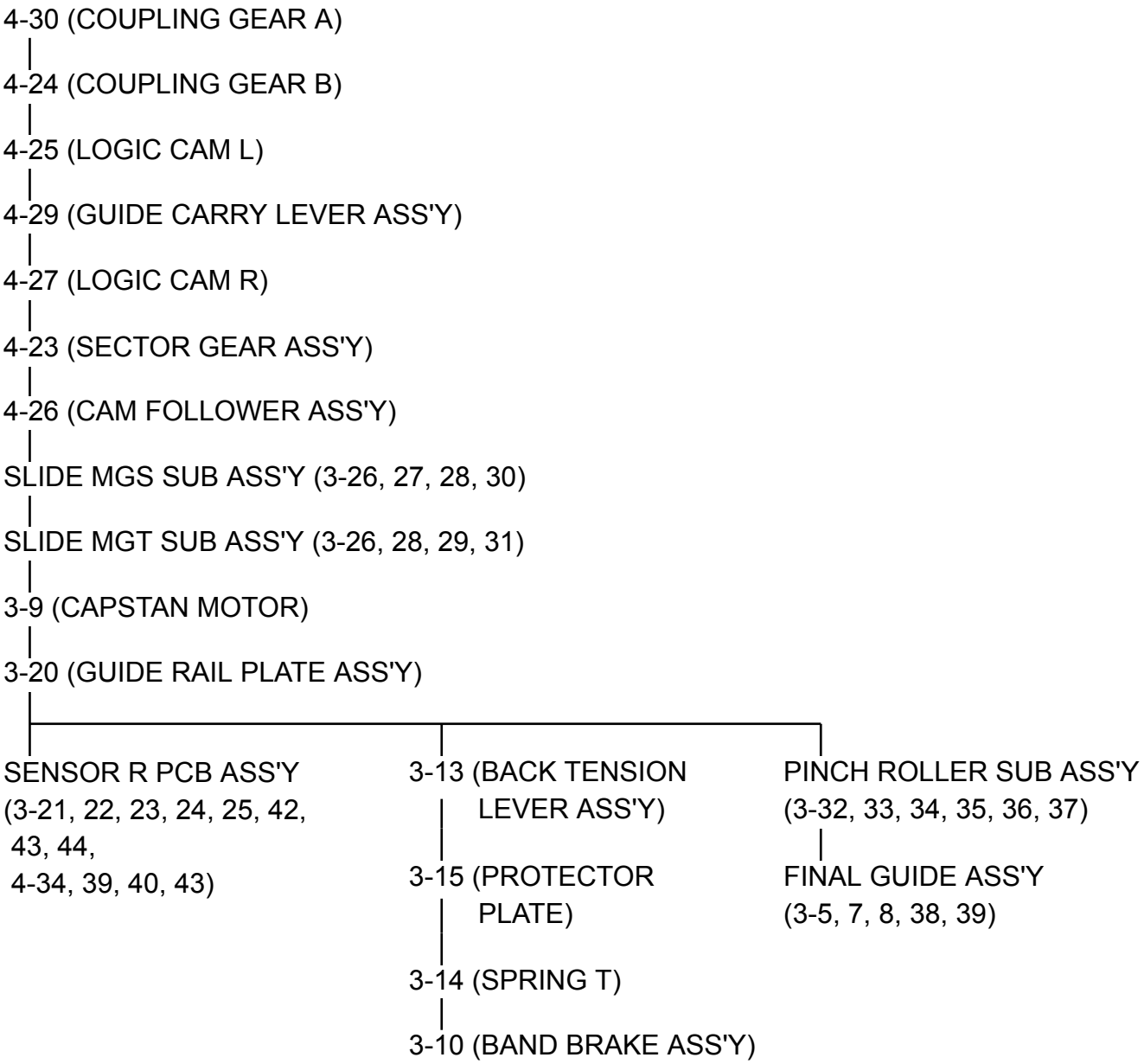
メカ ASS'Yの組立

3-1. Flowchart of assembling

For parts that require caution when reassembling the mechanism ass'y (especially critical gear meshes), a flowchart showing the order of installation is showed below. Disassembly should be performed in the reverse order of reassembly. As parts are indicated using reference numbers, refer to EXPLODED VIEWS -3 and -4 (☞ pages 49 & 51) for identification.

3-1. 組立のフローチャート

メカASS'Yの組立の際、取付け時に注意が必要な部品（特にギヤの噛み合わせ位置が重要）について、取付けの順番を示したフローチャートを以下に記します。
尚、分解は取付けの逆の順番で行って下さい。
また、部品は部番で示しますので、部番につきましては、EXPLODED VIEW-3, -4（☞ 49, 51ページ）を参照してください。



3-2. Installation of the mechanical parts

For parts that require caution when reassembling the mechanism ass'y(especially critical gear meshes), the following is showed.

[For order of installation, see flowchart (☞ page 19) and EXPLODED VIEWS -3 and -4 (☞ pages 49 & 51).]

1. Installing COUPLING GEAR B (4-24), and COUPLING GEAR A (4-30)

   As shown in Fig. 3-1, install 4-24 and 4-30 so that the two marks are visible.

2. Installing LOGIC CAM L (4-25) , and GUIDE CARRY LEVER ASS'Y (4-29)

   1) Install 4-25 so that hole ⓒ in 4-25 in Fig. 3-2 is aligned with hole ⓐ (Fig. 3-1) in the mechanism chassis. (Using a 1 mm dia. rod, pass it through the both holes to see if they are aligned with each other. Whenever checking holes for alignment hereafter, employ this method.)
   2) Similarly, install 4-29 so that hole ⓓ in 4-29 in Fig. 3-2 is aligned with hole ⓑ (Fig. 3-1) in the mechanism chassis.

3. Installing LOGIC CAM R (4-27)

   Install 4-27 so that hole ⓔ in 4-27 in Fig. 3-3 is aligned with the holes (hole ⓓ in 4-29 aligned in 2) of 2 with hole ⓑ in the mechanism chassis).
   At this time, recheck that the holes aligned in 1) of 2 (hole ⓒ in 4-25 and hole ⓐ in the mechanism chassis) are aligned with each other.

3-2. メカ部品の取付け

メカASSYの組立の際、取付け時に注意が必要な部品（特にギヤの噛み合わせ位置が重要）について述べます。

[取付けの順番については、フローチャート（☞ 19ページ）およびEXPLODED VIEW-3, -4（☞ 49, 51ページ）を参照してください。]

1. COUPLING GEAR B（4-24）、COUPLING GEAR A（4-30）の取付け

   4-24, 4-30は図3-1のように、マーク2個が表側になるように取り付ける。

2. LOGIC CAM L（4-25）、GUIDE CARRY LEVER ASS'Y（4-29）の取付け

   1）図3-2の4-25の穴 ⓒとメカシャーシの穴 ⓐ（図3-1）が一致するように、4-25を取り付ける。
   （1mm径の棒で両方の穴を貫通させるようにすると一致したかを確認することができます。以下、穴位置の一致を確認するときは、この方法で行ってください。）
   2）同様に、図3-2の4-29の穴 ⓓとメカシャーシの穴 ⓑ（図3-1）が一致するように、4-29を取り付ける。

3. LOGIC CAM R（4-27）の取付け

   図3-3の4-27の穴 ⓔと、2の2）で一致させた穴（4-29の穴 ⓓとメカシャーシの穴 ⓑ）が一致するように、4-27を取り付ける。
   このとき、2の1）で一致させた穴（4-25の穴 ⓒとメカシャーシの穴 ⓐ）が一致していることを再度確認する。

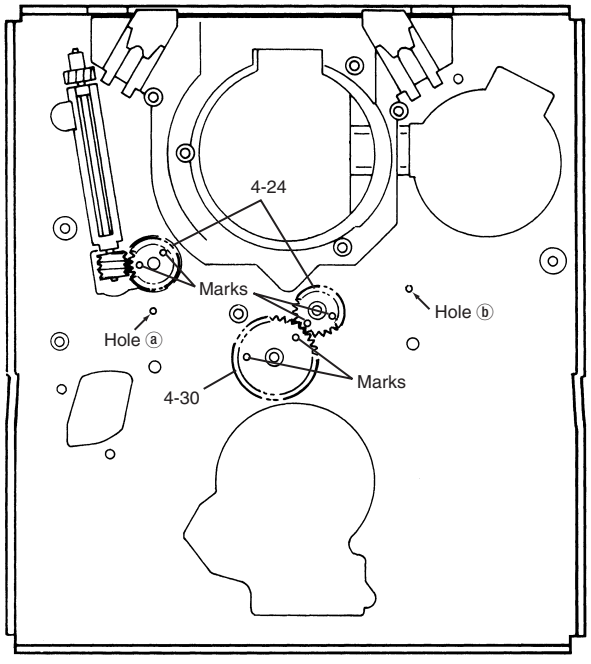


Fig. 3-1

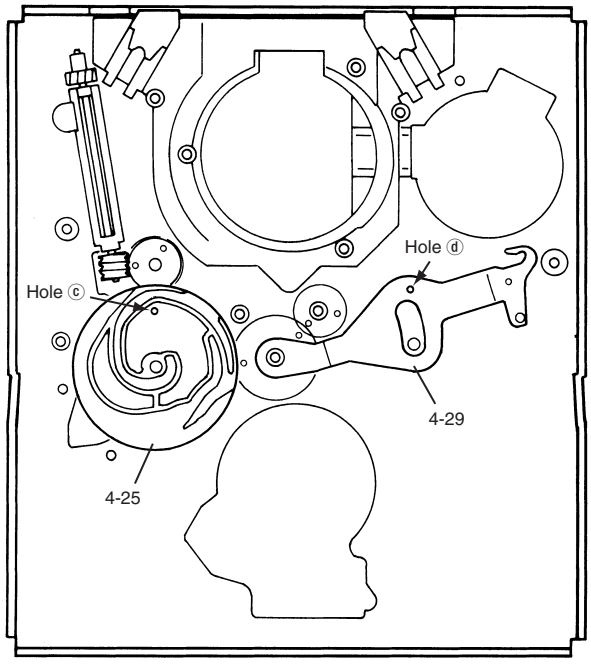


Fig. 3-2

4. Installing SECTOR GEAR ASS'Y (4-23)

Install 4-23 so that hole ⓕ in 4-23 in Fig. 3-3 is aligned with the holes (hole ⓒ in 4-25 aligned in 1) of 2 with hole ⓐ in the mechanism chassis).

5. Installing SLIDE MGS SUB ASS'Y (3-26, 27, 28, 30)

1) As shown in Fig. 3-4, install 3-30 so that mark ⓗ on 3-30 is aligned with mark ⓖ on 4-23.
2) Insert SLIDE MGS into the groove of catcher ⓞ by pushing it from the direction of arrow ⓚ.
(While retracting the lever of 3-30 in the direction of arrow ⓛ with one hand, then with the other hand, push SLIDE MGS towards the groove of catcher ⓞ and release the hands.)

6. Installing SLIDE MGT SUB ASS'Y (3-26, 28, 29, 31)

1) As shown in Fig. 3-4, install 3-31 so that mark ⓙ on 3-31 is aligned with mark ⓘ on 3-30.
2) Insert SLIDE MGT into the groove of catcher ⓟ by pushing it from the direction of arrow ⓜ.
(While retracting the lever of 3-31 in the direction of arrow ⓝ with one hand, then with the other hand, push SLIDE MGT towards the groove of catcher ⓟ and release the hands.)

4. SECTOR GEAR ASS'Y (4-23) の取付け

図3-3の4-23の穴 ⓕと、2の1) で一致させた穴（4-25の穴 ⓒとメカシャーシの穴 ⓐ）が一致するように4-23を取り付ける。

5. SLIDE MGS SUB ASS'Y (3-26, 27, 28, 30) の取付け

1) 図3-4のように、3-30のマーク ⓗと4-23のマーク ⓖが一致するように3-30を取り付ける。
2) SLIDE MGSを矢印 ⓚの方向からキャッチャー ⓞの溝に挿入する。(3-30のレバーを片方の指で矢印 ⓛの方向に戻しながら他方の指でSLIDE MGSをキャッチャー ⓞの溝に挿入し、指を離す。)

6. SLIDE MGT SUB ASS'Y (3-26, 28, 29, 31)の取付け

1) 図3-4のように、3-31のマーク ⓙと3-30のマーク ⓘが一致するように3-31を取り付ける。
2) SLIDE MGTを矢印 ⓜの方向からキャッチャー ⓟの溝に挿入する。(3-31のレバーを片方の指で矢印 ⓝの方向に戻しながら他方の指でSLIDE MGTをキャッチャー ⓟの溝に挿入し、指を離す。)

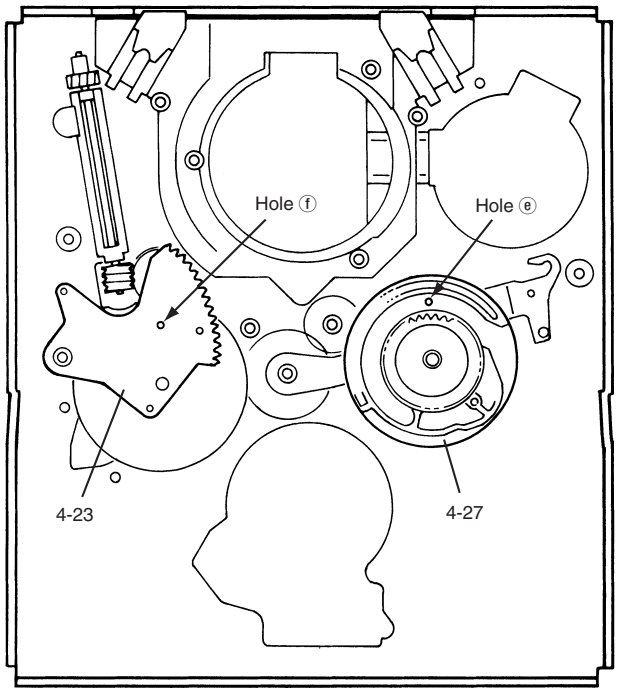


Fig. 3-3

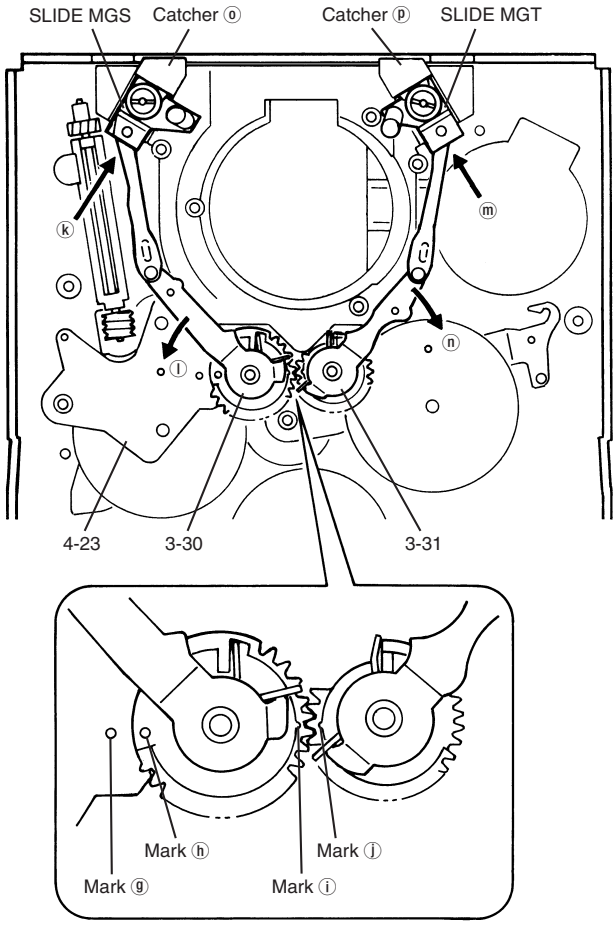


Fig. 3-4

7. Installing MODE SW ASS'Y (3-25)

See Fig. 3-5.

1) Align the U groove in the PCB on the back of the gear of 3-25 with the V groove in the gear by turning the gear.
Note)
For reasons of explanation the illustration shows a view from the gear, but in practice, you cannot see them clearly unless you see them from the PCB.
As a rule of thumb, align the mark on the gear with the U groove in the PCB behind the gear to facilitate the above positioning.
2) Fit 3-25 over the boss on the chassis.

7. MODE SW ASS'Y（3‐25）の取付け

図3-5参照。

1）3-25のギヤの裏面にあるPCBのU溝にギヤのV溝がくるように、ギヤを回してセットする。
注）図では、説明のためギヤ面から見たイラストが書いてありますが、実際にはPCB面から見ないとよく確認することはできません。
尚、図のギヤのマークをギヤの裏面にあるPCBのU溝の位置に合わせるようにすると、上記位置合わせの目安になります。
2）3-25をシャーシの軸に挿入する。

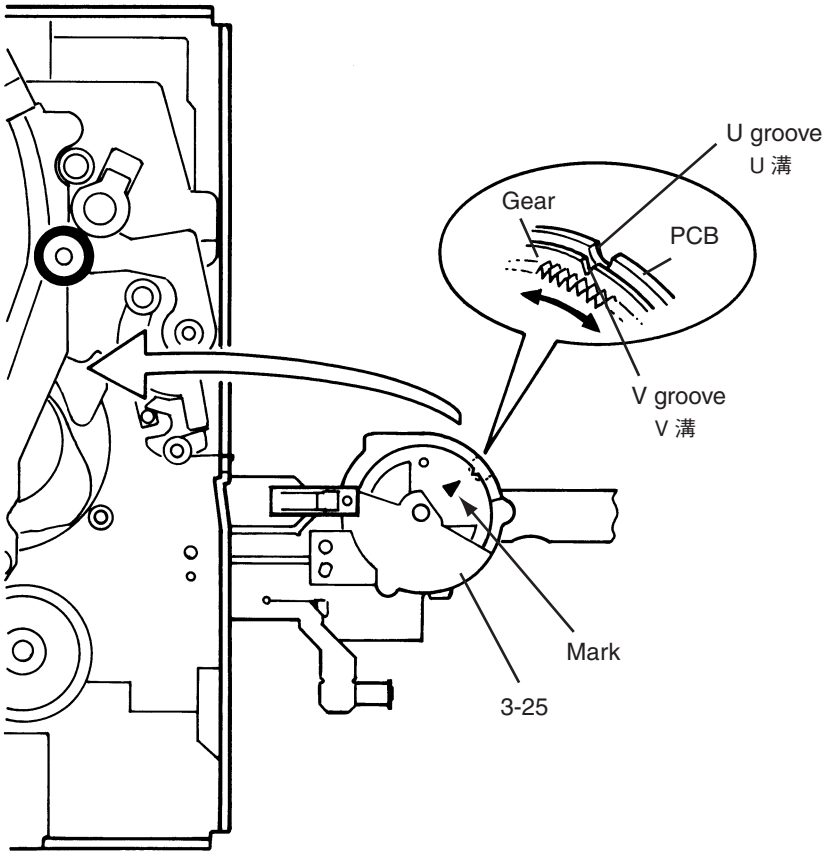


Fig. 3-5

8. Installing BAND BRAKE ASS'Y (3-10)

1) Before installing 3-10, fit COIL SPRING (3-11) to 3-10 as shown in Fig. 3-6.
2) After installing 3-10 as shown in Fig. 3-7, push portion A of 3-11 downward with a rod to disengage it, then hook it over the hook of REEL LOCK LEVER (4-21).

8. BAND BRAKE ASS'Y（3-10）の取付け

1）3-10を取り付ける前に、COIL SPRING（3-11）を図3-6のように3-10に取り付ける。
2）3-10を図3-7のように取り付けた後、3-11のA部を棒で下側に押して外し、その下にあるREEL LOCK LEVER（4-21）のフックに掛ける。

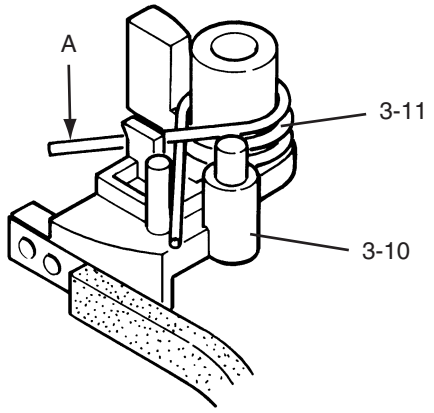


Fig. 3-6

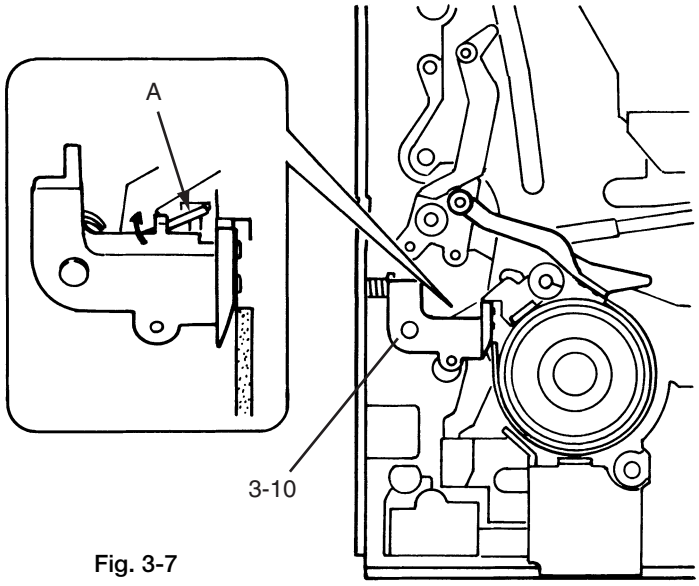


Fig. 3-7

9. Installing PINCH ROLLER SUB ASS'Y

See Fig. 3-8

Fit PINCH ROLLER SUB ASS'Y over the boss on the mechanism chassis, then hook spring edge A over hook B at the edge of the mechanism chassis.

9. PINCH ROLLER SUB ASS'Y の取付け

PINCH ROLLER SUB ASS'Yをメカシャーシの軸に取り付けた後、バネ端Aを図3-8のようにメカシャーシ側面のフックBに掛ける。

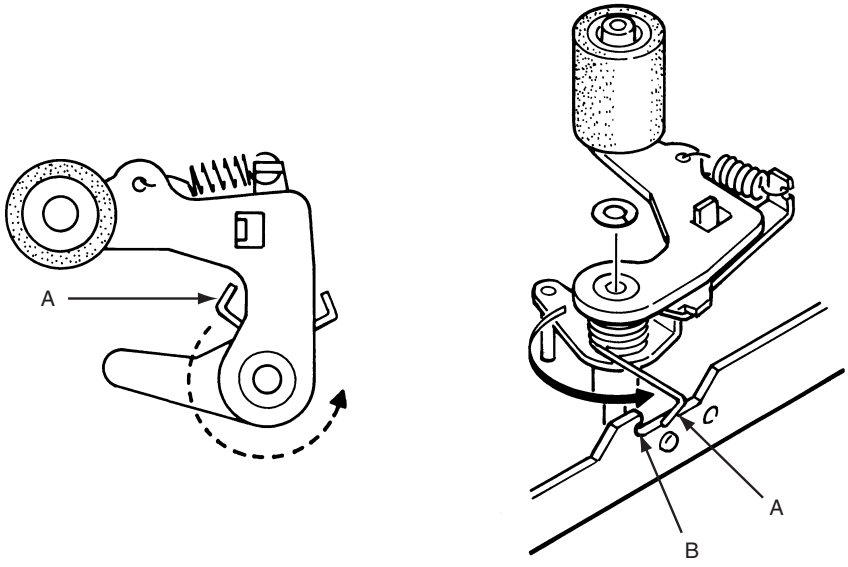


Fig. 3-8

10. Final checking of gear meshes

After installation of all mechanical parts is complete, check to see if gear meshes (items 1 to 7) are proper as follows:

1) Insert a 1 mm dia. rod into hole ' in Fig. 3-9, and check to see if it passes through up to the hole in the mechanism chassis.
2) Insert a 1 mm dia. rod into hole , in Fig. 3-9, and check to see if it passes through up to the hole in the mechanism chassis.
3) Check to see if the mark of 4-27 is aligned with the V groove in the MODE SW ASS'Y (3-25) gear as shown in Fig. 3-9.

10. ギヤの噛み合わせ位置最終確認

すべてのメカ部品を取り付けた後、ギヤの噛み合わせ（1～7項）が正しく行われたかを以下のように確認する。

1）図3-9の穴 ⓠに1mm径の棒を差し込んだとき、メカシャーシの穴まで貫通することを確認する。
2）図3-9の穴 ⓡに1mm径の棒を差し込んだとき、メカシャーシの穴まで貫通することを確認する。
3）図3-9のように、4-27のマークがMODE SW ASS'Y（3-25）のギアのV溝に合っていることを確認する。

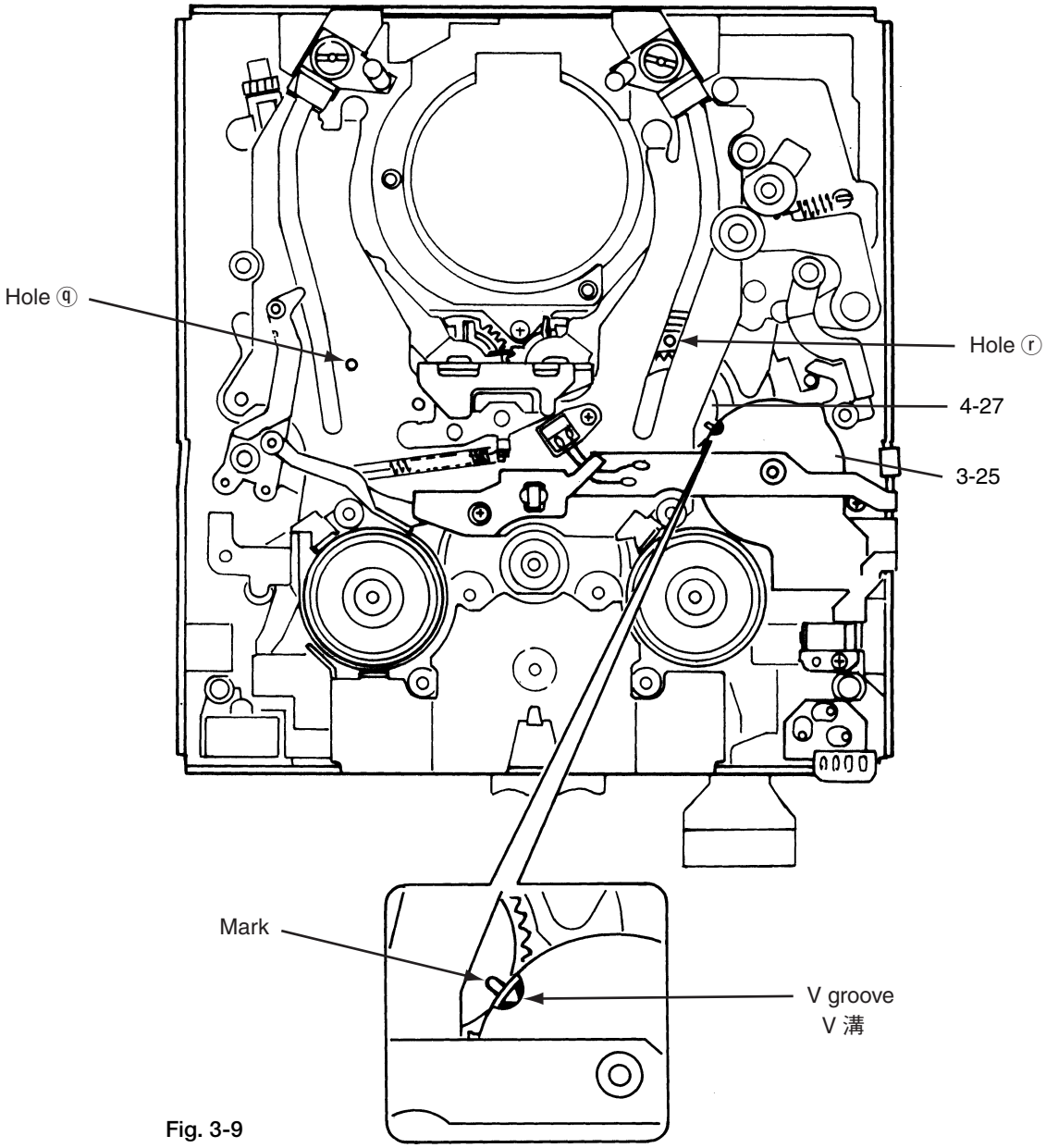


Fig. 3-9

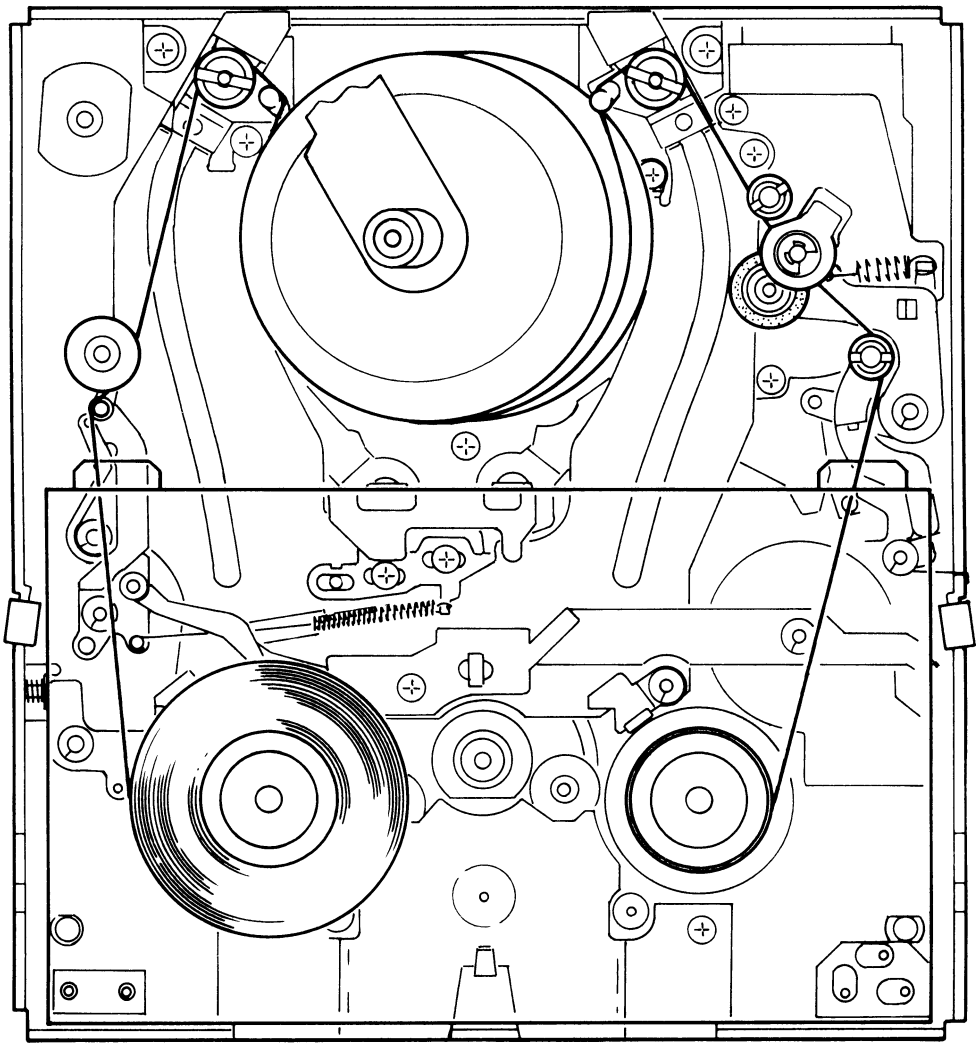
11. Replacing BRUSH ASS’Y (4-33)

With the DA-98HR, the drum is grounded through the sliding action of a slip ring and brush in place of through a single contact point which is the case with previous DTRSs. Therefore, when BRUSH ASS’Y (4-33) has been used for the specified hours, its performance can no longer be guaranteed, eventually leading to fracture of the brush. To prevent this, make sure to replace BRUSH ASS’Y when replacing DRUM ASS’Y.
The replacement timing is about 1000 hours which is the same as that of DRUM ASS’Y.
As the worn debris is accepted by COVER, BRUSH (4-45), also be sure to remove the debris when replacing BRUSH ASS’Y.

11. BRUSH ASS'Y（4-33）の交換について

DA-98HRのドラムアースは、従来のDTRSのような接点式ではなく、スリップリングとブラシの摺動によっています。従って、BRUSH ASS'Y（4-33）の使用時間が限度を超えると磨耗により性能が保証できなくなり、最終的には切断してしまいます。そこで、ドラムASS'Y交換時には、必ずこのBRUSH ASS'Yの交換を行ってください。
交換周期は、ドラムASS'Y交換周期と同じ約1000時間です。
また、磨耗粉をCOVER, BRUSH（4-45）で受けるようになっていますので、BRUSH ASS'Y交換の際は磨耗粉の除去も行ってください。

4. MECHANISM ADJUSTMENTS
機構部調整



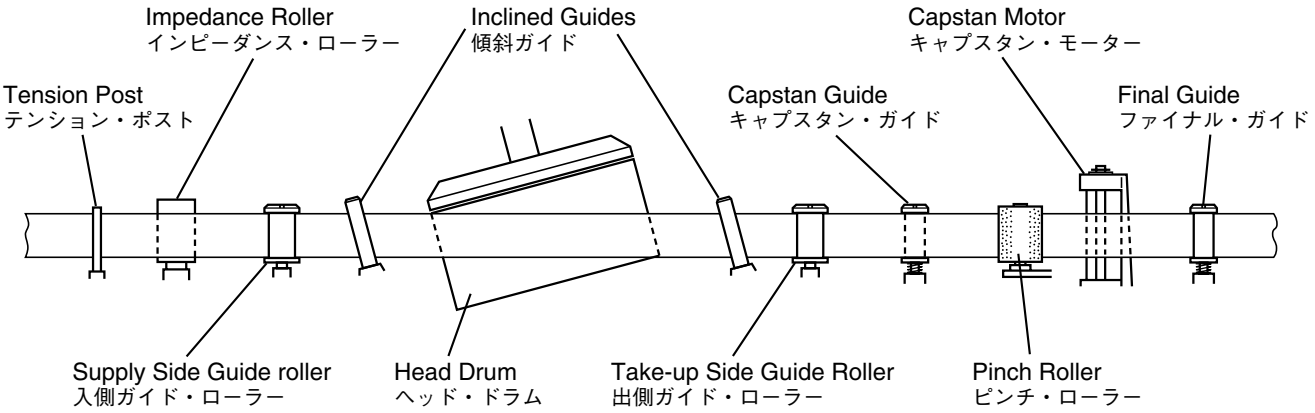


Fig. 4-1

4-1. Preparation

1. Cleaning the head drum (See Fig. 4-2)
   Press a cloth moistened with alcohol against the surface of the head drum, and clean the drum by turning it counter-clockwise with the fingers.
   Notes)
   - To turn the drum, insert a clip (or other appropriate piece) into the hole (ϕ1) in the drum shaft, and turn the clip, as shown in the figure.
   - When cleaning the head drum, be careful not to damage the head chip. It might be damaged if you apply a longitudinal force to it or turn it clockwise.
   - After cleaning the head drum, use a dry cloth to wipe off any residual alcohol (because when it vaporizes, condensation could occur). The tape would stick to the drum if its surface is wet, causing damage to the tape.

4-1. 準備

1. ヘッドドラムのクリーニング（図4-2参照）
   ヘッドドラムの表面にアルコールで浸した布をあて、ドラムを反時計方向に指で回してクリーニングする。
   注）
   - ドラムは、図のようにシャフトの穴（ϕ1）にクリップ等を差し込み、それを回すことにより回ります。
   - クリーニングするとき、ヘッドチップを破損しないように充分注意すること。ヘッドチップの上下方向に力を加えたり、ドラムを時計方向に回すと破損の可能性があります。
   - アルコールでクリーニングした場合は、アルコールが充分乾燥してからテープをローディングしてください。アルコールでクリーニングした後、乾いた布で乾拭きすることをお勧めします。（アルコールの気化時に結露が発生する可能性があるため）
     ドラム表面が濡れていると、ドラムにテープがはりつきテープダメージの原因となります。

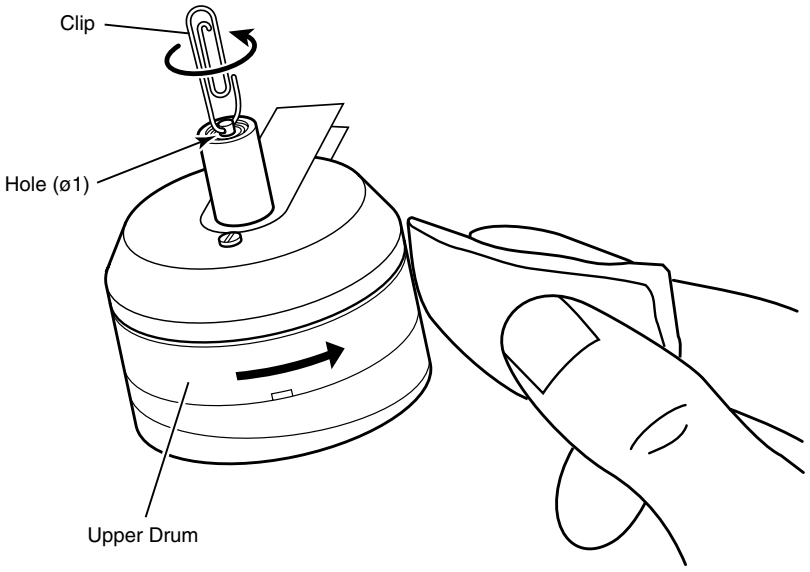


Fig. 4-2

2. Connecting the oscilloscope
   Connect CH1 of the oscilloscope to TP3 (RF A-HEAD) or TP4 (RF B-HEAD) on the RF PLAY PCB and CH2 to TP601 (SWP) on the SYS PCB. (See Fig. 5-1)

2. オシロスコープの接続
   オシロスコープのCH1をRF PLAY PCBのTP3（RF A-HEAD）またはTP4（RF B-HEAD）に、CH2をSYS PCBのTP601（SWP）に接続する。（図5-1参照）

4-2. Test tape

1. TEAC MTT-86131 : For adjusting the torque
2. TEAC MTT-88101(Fs=44.1 kHz):
   For adjusting the error rate and the RF level

4-2. テストテープ

1. TEAC MTT-86131 : トルク調整用
2. TEAC MTT-88101（Fs=44.1 kHz）:
   エラーレート、RFレベル調整用

4-3. Adjusting the tension arm position

1. Load a torque cassette MTT-86131, then set the DA-98HR to PLAY mode.
2. Using a Phillips screwdriver, turn adjust screw A (Fig. 4-3), then align the center of the semicircular portion of the tension arm to the guide rail edge.
   This should fall within range A to C (see Fig. 4-3).

4-4. Adjusting the torque

1. Load a torque cassette MTT-86131, then set the DA-98HR to PLAY mode.
2. Confirming the FWD back tension
   1) Read the torque value at the supply-reel (white) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard value: 10 to 12 g.cm
      Fluctuation range: 3 g.cm or less
   2) If the standard value is not satisfied, remove the torque cassette, loosen screws B (two) in Fig. 4-3 and adjust by moving the protector plate to the left and right. If moved to the left, the torque is reduced, whereas if moved to the right, it increases.
   3) Repeat 1 to 3 until the values fall within the standard.

4-3. テンションアーム位置調整

1. トルクカセットMTT-86131を装着し、PLAYモードにする。
2. プラスドライバーで調整ネジA（図4-3）を回し、テンションアームの半月部の中心をガイドレールエッジに合わせる。
   変動はA ～ Cの範囲であること。（図4-3参照）

4-4. トルク調整

1. トルクカセットMTT-86131を装着し、PLAYモードにする。
2. FWDバックテンションの確認
   1）サプライリール台（白）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。
      規格値: 10 ～ 12 g･cm
      変動幅: 3 g･cm以下
   2）もし規定値を満足しないときは、トルクカセットを外し、図4-3のネジB 2本を緩めプロテクタプレートを左右に動かして調整する。左に動かすとトルクが弱くなり、右に動かすと強くなります。
   3）1～3項を規格に入るまで繰り返す。

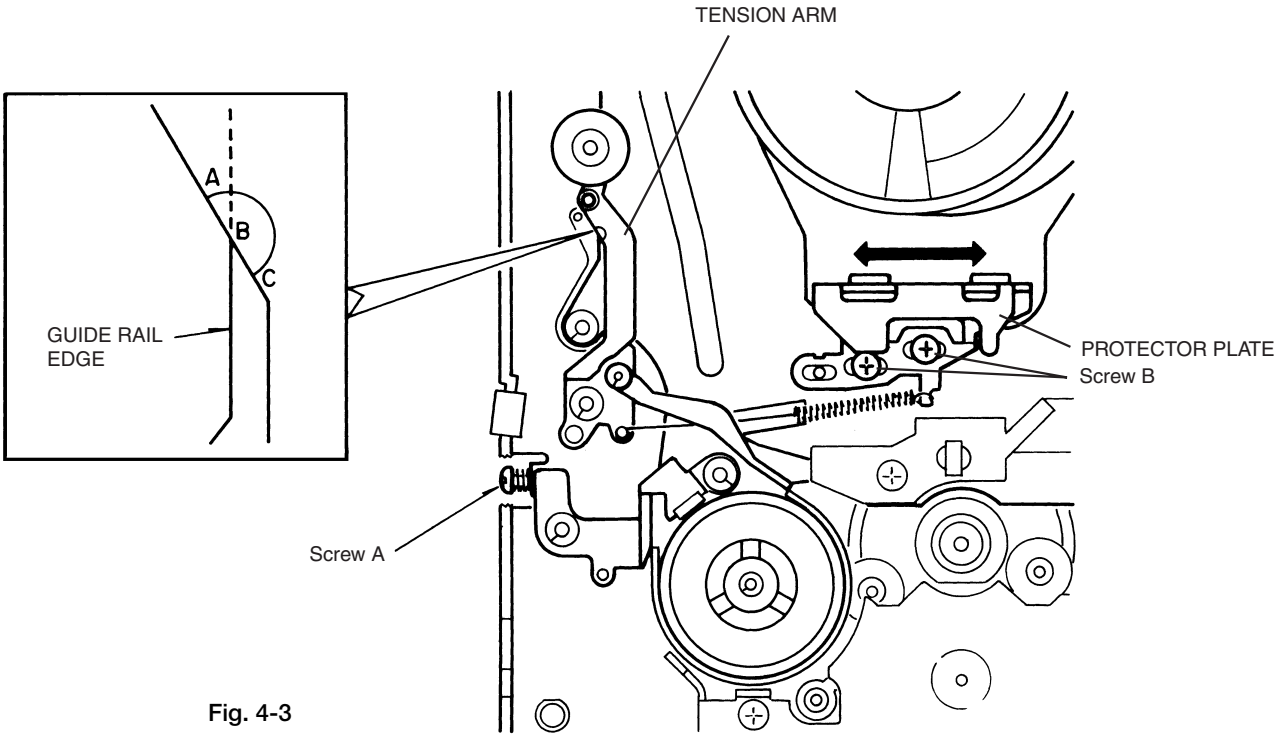


Fig. 4-3

3. Confirming the take-up torque of the take-up reel
   1) Read the torque value at the take-up reel (black) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard value: 8 to 15 g·cm
      Fluctuation value: 3 g·cm or less
   2) If the standard value is not satisfied, remove the torque cassette, replace the take-up reel table (black), and repeat 1 to 4 until the values fall within the standard.
      Note)
      When reinstalling, be sure not to forget to reinstall the cut washer.
4. Confirming the REV take-up torque
   1) Press the SHUTTLE switch, then turn the SHUTTLE knob to the left. Read the torque value at the supply-reel (white) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard range: 18 to 28 g·cm
      Fluctuation range: 3 g·cm or less
   2) If the standard value is not satisfied, remove the torque cassette, replace the supply-reel table (white), and repeat 1 to 5 until the values fall within the standard.
      Note)
      When reinstalling, be sure not to forget to reinstall the cut washer.
   3) Read the torque value at the take-up reel (black) side, then confirm that the center value of the torque fluctuations falls within the following range:
      Standard range: 8 to 25 g·cm
      Fluctuation range: 3 g·cm or less

＊Cautions when replacing the reel table

When removing the supply-reel table or take-up reel table, the disk reflector (4-3 on page 51) beneath the reel table may also be disengaged as well.

In such a case, see that the polyethylene slider washer (4-55 on page 51) remains on the reel table shaft (mechanism chassis) without fail.

If the disk reflector is affixed over the reel table shaft with the polyethylene slider washer stuck on the backside of the disk reflector, the polyethylene slider washer may NOT fit over the reel table shaft but enter the mechanism chassis.

4-5. Adjusting the tape travel

When adjusting the height of each roller guide, be sure to slightly loosen the screws securing the guide beforehand.

After adjustment is complete, tighten the screws using a torque driver. Observe a tightening torque of 200 g·cm.

Torque driver: 0.2 to 1.5 kg; parts No. 5772827800

(Torque driver bit: M2 (+); parts No. 5772828000)

3. テイクアップリール巻取りトルクの確認
   1）テイクアップリール台（黒）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。

      規定値：8 〜15 g・cm
      変動幅：3 g・cm以下

   2）もし規定値を満足しないときは、トルクカセットを外し、テイクアップリール台（黒）を交換し、1〜4項を規格に入るまで繰り返す。
      注）取付け時、カットワッシャーの取付を忘れないこと。
4. REV巻取りトルクの確認
   1）SHUTTLEキーを押し、SHUTTLEノブを左に回す。そのときのサプライリール台（白）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。

      規定値: 18 〜 28 g・cm
      変動幅: 3 g・cm以下

   2）もし規定値を満足しないときは、トルクカセットを外し、サプライリール台（白）を交換し、1〜5項を規格に入るまで繰り返す。
      注）取付け時、カットワッシャーの取付を忘れないこと。
   3）テイクアップリール台（黒）側のトルク値を読み、トルク変動の中心値が下記の値に入っていることを確認する。

      規格値: 8 〜 25g・cm
      変動幅: 3 g・cm以下

＊リール台交換時の注意

サプライリール台またはテイクアップリール台を外すとき、リール台の下のディスクリフレクタ（51ページ 4-3）が一緒に外れることがあります。

その場合は、必ずポリスライダワッシャ(51ページ 4-55)がリール台軸（メカシャーシ）に残っていることを確認してください。

ディスクリフレクタの裏側にポリスライダワッシャがついたまま、リール台軸にディスクリフレクタを挿入すると、ポリスライダワッシャがリール台軸に挿入されずメカシャーシに混入してしまうおそれがあります。

4-5. テープ走行調整

各回転ガイドの高さを調整する場合は、必ず回転ガイドを止めているネジを少し緩めてから行ってください。

調整後は、そのネジをトルクドライバーにより締め付けること。締め付けトルクは、200g・cm厳守のこと。

トルクドライバー 0.2〜1.5kg : 品番 5772827800

（トルクドライバー用ビット M2（＋）: 品番 5772828000）

1. Load the test tape MTT-88101, then set the DA-98HR to PLAY mode.
2. While observing the A-HEAD waveform using the oscilloscope, fine-adjust the heights of the roller guides at the supply side and take-up side of the drum using a wrench, so that the leading and trailing edges of the RF waveform have virtually the same level as that of the peak portion on the center of the waveform. (See Fig. 4-4)

   Note)

   Be careful not to hold down the roller guide at the supply side too much by way of making the leading edge of the RF waveform flat. Otherwise, it may lead to rounding of the RF waveform during REV mode.
3. So that the tape travels on the lower edge of the capstan guide, adjust the height of the capstan guide.

   The adjustment method is as follows:

   1) Turn the adjustment screw counterclockwise to raise the lower flange.
   2) If tape is curled, turn the screw clockwise to lower the lower flange. Stop turning the screw when the tape curl dissolves.

   Notes)

   - It is acceptable in principle if the tape is confirmed to be free from curl at the lower edge of the guide.
   - Prior to adjustment, be sure to dissolve the screw-locking compound applied to the head of the guide using alcohol. After the adjustment is complete, reapply screw-locking compound.
4. Adjust the height of the final guide so that the tape is free from curl between the take-up side of the capstan and the final guide, and that the tape is NOT curled by the upper and lower edges of the final guide.

   Notes)

   - It is acceptable in principle if confirmation is made only.
   - Prior to adjustment, be sure to dissolve the screw-locking compound applied to the head of the guide using alcohol. After the adjustment is complete, reapply screw-locking compound.

1. テストテープ MTT-88101を装着し、PLAYモードにする。
2. オシロスコープでA-HEADの波形を観測しながらドラム入口、出口の回転ガイドの高さを二股レンチにより調整し、RF波形の入口、出口が中央の最大部分とほぼ同じ高さ（フラット）になるように（図4-4）、ドラム入口、出口の回転ガイドの高さを微調整する。

   注）RF波形の入口側をフラットにするために入口の回転ガイドを押さえすぎないこと。REV時のRF波形のつぶれの原因となります。

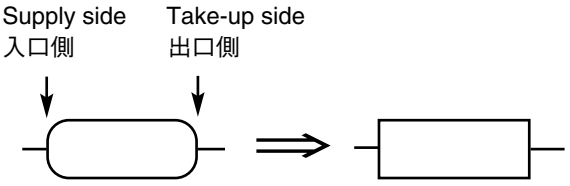


Fig. 4-4

3. キャプスタンガイドの下エッジをテープが走行するように、キャプスタンガイドの高さを調整する。

   調整方法は以下の通り。

   1）下フランジを一度上に上げるように調整ネジを左に回す。
   2）テープのカールが確認できたらネジを右に回して下フランジを下げてゆき、テープのカールがなくなった時点で調整を止める。

   注）調整する場合は、必ずガイド頭部のネジロックをアルコールで溶かしてから行ってください。
   調整後は、必ずネジロックをすること。
4. キャプスタン出口からファイナルガイドの間でテープのよじれがなく、またファイナルガイドの上下エッジでテープがカールしないように、ファイナルガイドの高さを調整する。

   注）
   - 原則は確認のみでOKです。
   - 調整する場合は、必ずガイド頭部のネジロックをアルコールで溶かしてから行ってください。
     調整後は、必ずネジロックをすること。

5. Linearity check
   1) Set the unit to the VTR mode (☞ page 7).
   2) When the unit is in the VTR mode, the level fluctuates spontaneously.
      At this time, check that the shape of the waveform remains consistent while the level is changes.
      If it doesn't, fine-adjust the guide rollers located at the entrance and exit of the drum.
      If the level stops varying, set the unit to the track-off mode so that the level continues to vary. (see below.)

   (How to Set the Track-Off Mode)
   ① Set the unit to the VTR mode.
   ② Select the menu group M in the menu screen, then press ENTER key.
   ③ Move the cursor to "Track Off" and press ENTER key. (The display shows "Track off Mode : off".)
   ④ Press the ▲ key to change the "off" to "manual +0.0".
   ⑤ Press the ▶ key. ("+0.0" will start blinking.)
   ⑥ Using the ▲ and ▼keys, change the display within the limits of from -0.5 to +0.5.

6. Final checking of each guide
   1) Confirm that the upper edge travel regulation is observed for the roller guide at the supply side of the drum.
   2) Confirm that the upper edge travel regulation is observed for the roller guide at the take-up side of the drum.
      Note)
      - Gently push the head of the roller guides at the supply side and the take-up side of the drum in the direction of the rear of the mechanism using a bamboo skewer, then confirm that the waveform in 2 will resume soon (within one second) when the bamboo skewer is released. If the waveform does NOT quickly resume, upper edge tape travel regulation is roughly made; fine-adjustment is necessary.
      - If dirt is adhered to the roller guides, the level will fluctuate while they turn.
        In such a case, moisten a cotton swab with alcohol, and clean the roller guides.
   3) Confirm the lower edge travel regulation for the capstan guide.
      Note) Play an ME tape and make adjustments as described in item 3 on page 30, then check again.
   4) Confirm the upper and lower edge travel regulation for the final guide (the tape should be free from curl).

5. 直線性の確認
   1）VTRモードにする。（☞ 7ページ）
   2）VTRモードにすると、レベルがかってに大きくなったり小さくなったりします。このときの波形が形を変えずにレベルだけが大小することを確認する。そうでない場合は、ドラム入口、出口の回転ガイドを微調整する。
      もし、レベルが大小を繰り返さないようならば、以下の方法でトラックオフさせるとレベルが変化するよになります。

   （トラックオフのさせ方）
   ① VTRモードにする。
   ② メニュー画面で、メニューグループMを選択し、ENTERキーを押す。
   ③ “Track Off”にカーソルを合わせて ENTERキーを押す。（Track off Mode : off 表示）
   ④ ▲キーを押す。（off → manual +0.0 表示）
   ⑤ ▶キーを押す。（+0.0 点滅）
   ⑥ ▲または▼キーにより、表示を－0.5 ～ ＋0.5の範囲で変化させる。

6. 各ガイドの最終チェック
   1）ドラム入口回転ガイドの上エッジ走行規制を確認する。
   2）ドラム出口回転ガイドの上エッジ走行規制を確認する。
   注）● 入口回転ガイドおよび出口回転ガイドの上部をメカ後部方向に竹串で軽く押し、竹串を離したとき、すぐ（1秒以内）に2項の波形に戻ることを確認する。波形がすぐに戻らない場合は、上エッジテープ走行規制が甘いので微調整する必要があります。
      ● 回転ガイドにゴミが付着しているとガイド回転時にレベル変動を生じます。この場合は、綿棒にアルコール塗布し、回転ガイドをクリーニングしてください。
   3）キャプスタン部ガイドの下エッジ走行規制を確認する。
      注）MEテープを走行させ、30ページの3項の調整を再度行って確認する。
   4）ファイナルガイドの上下エッジ走行規制（テープのカールが無いこと）を確認する。

4-6. Confirming the travel in F.FWD, REW and REV modes

1. In all modes, including F.FWD, REW and REV/SHUTTLE, confirm that the tape is free from damage at each guide.
   Note)
   - If, in F.FWD mode, the impedance roller generates a strange noise, replace it.
   - If the leading edge of the playback RF waveform is slow to rise up (the waveform gradually increases in level), or the tape curl is excessive during reverse mode, choose a polyethylene slider washer (beneath the impedance roller) from the following three washers and adjust the height of the impedance roller.
     - 0.13 mm(P/N M00221900A)
     - 0.20 mm(P/N M00222000A)
     - 0.25 mm(P/N M00222100A)
     - No washer

     Observe a screw tightening torque of 500 g·cm.
     Torque driver: 0.2 to 1.5 kg; parts No. 5772827800
     (Torque driver bit: M2 (+); parts No. 5772828000)
2. Load the test tape MTT-88101, then confirm the counter indication in F.FWD and REW modes from the beginning to the end of the tape. See that the counter indication is not a continuous bar indication "---". (Momentary bar indication is acceptable.)

   In the case of a continuous bar indication, refer to the following:

4-6. FF, REW, REVモードでの走行確認

1. FFモード、REWモード、REV/SHUTTLEモードなどすべてのモードで、各ガイドでのテープダメージが無いことを確認する。
   注）● FF時、インピーダンスローラーの回転異音がある場合は交換する。
   ● 再生RF波形の立ち上りが遅い（波形が徐々に大きくなる）場合や、リバース時にテープのカールが著しい場合は、インピーダンスローラーの下に敷いてあるポリスライダワッシャを次の4種類のうちから選択し、インピーダンスローラーの高さを調整する。

     ・0.13mm(品番M00221900A)
     ・0.20mm(品番M00222000A)
     ・0.25mm(品番M00222100A)
     ・ワッシャ無し

     ネジの締め付けトルクは、500g·cm 厳守のこと。
     トルクドライバー 0.2～1.5kg：品番5772827800
     （トルクドライバー用ビットM2（+）：品番5772828000）
2. テストテープ MTT-88101を装着して、FFおよび REWをテープの巻始めから巻終りまで通してカウンタ表示を確認する。カウンタ表示が連続してバー表示“---"にならないことを確認する。（一瞬のバー表示はOKです）連続してバー表示がでる場合は、以下を参照してください。

① Fig. 4-5 shows the normal RF waveform (for both A-HEAD and B-HEAD) in F.FWD or REW mode (reel speed:100 times).

② Fig. 4-6 shows the RF waveform in which the indication will result in a bar indication in 1 mode (the ABS time CANNOT be read due to a missing or distorted waveform).

In such a case, the following measures are required:

- If the waveform is as in Fig. 4-6 in F.FWD mode, replace the soft brake (3-18 on page 49) or coil spring (3-17 on page 49) at the supply reel side.
- If the waveform is as in Fig. 4-6 in REW mode, replace the soft brake (3-18 on page 49) or torsion spring (3-19 on page 49) at the take-up reel side.

③ Fig. 4-7 shows the normal RF waveform in REV mode (capstan feed).

④ Fig. 4-8 shows the RF waveform in which the indication will result in a bar indication in 3 mode (the ABS time CANNOT be read due to a missing or distorted waveform).

In such a case, the following causes are conceivable:

- The roller guide at the supply side of the drum is held down too much. The roller guide needs readjustment.
- The REV take-up torque at the supply reel pad is low. It should be replaced with a reel table with a REV take-up torque of approx. 30 g.cm.

① 図4-5は、FFまたはREWモード（リール送り, 100倍速）時のRF通常波形（A-HEAD, B-HEADとも）です。

② 図4-6は、①のモード時にバー表示（ABSタイムが読めない）になってしまう場合（波形抜けまたは波形つぶれ）のRF波形です。

この場合は、下記の処置が必要です。

- FF時に図4-6の波形になる場合は、サプライリール台側のSOFT BRAKE LEVER ASS'Y（49ページ 3-18）またはCOIL SPRING（49ページ 3-17）を交換してください。
- REW時に図4-6の波形になる場合は、テイクアップリール台側のSOFT BRAKE LEVER ASS'Y（49ページ 3-18）またはTORSION SPRING（49ページ 3-19）を交換してください。

③ 図4-7は、REVモード（キャプスタン送り）時のRF通常波形です。

④ 図4-8は、③ のモード時にバー表示（ABSタイムが読めない）になってしまう場合（波形抜けまたは波形つぶれ）のRF波形です。

この場合は、下記の原因が考えられます。

- ドラム入口の回転ガイドの押さえすぎ。回転ガイドの再調整が必要です。
- サプライリール台のREV巻取りトルクが弱い。REV巻取りトルクが、30g.cm前後のリール台と交換が必要です。

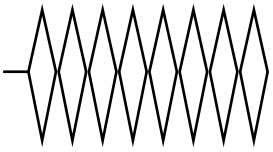


Fig. 4-5

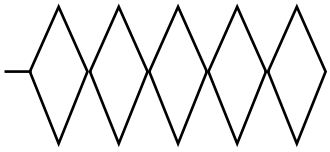
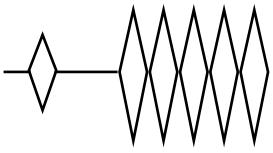


Fig. 4-7



or

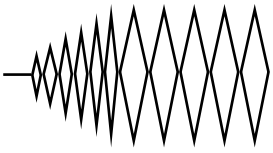
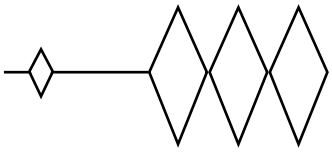


Fig. 4-6



or

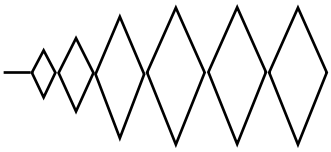


Fig. 4-8

＊ Cautions when replacing the drum

When the drum is replaced, be sure to confirm and adjust the following items other than tape travel adjustments.
As for adjustment methods, refer to 5 (ELECTRICAL ADJUSTMENTS):

- Adjustment of the P.G. (phase generator) position
- Playback error rate (MP tape and ME tape)
- Adjustment of the recording current
- R/P error rate (MP tape and ME tape)

Be also sure to replace BRUSH ASS'Y when replacing the drum. (☞ page 25)

＊ドラム交換時の注意

ドラムを交換した場合は、テープ走行調整以外に下記項目の確認・調整を必ず行ってください。
調整方法については、5項（電気系調整）を参照してください。

・P.G.（PHASE GENERATOR）位置調整
・再生エラーレート（MPテープおよびMEテープ）
・記録電流調整
・録再エラーレート（MPテープおよびMEテープ）

また、ドラム交換時には、必ずBRUSH ASS'Yの交換も行ってください。（☞ 25ページ）

5. ELECTRICAL ADJUSTMENTS

電気系調整

5-1. Check and adjustment points

5-1. 測定箇所および調整箇所

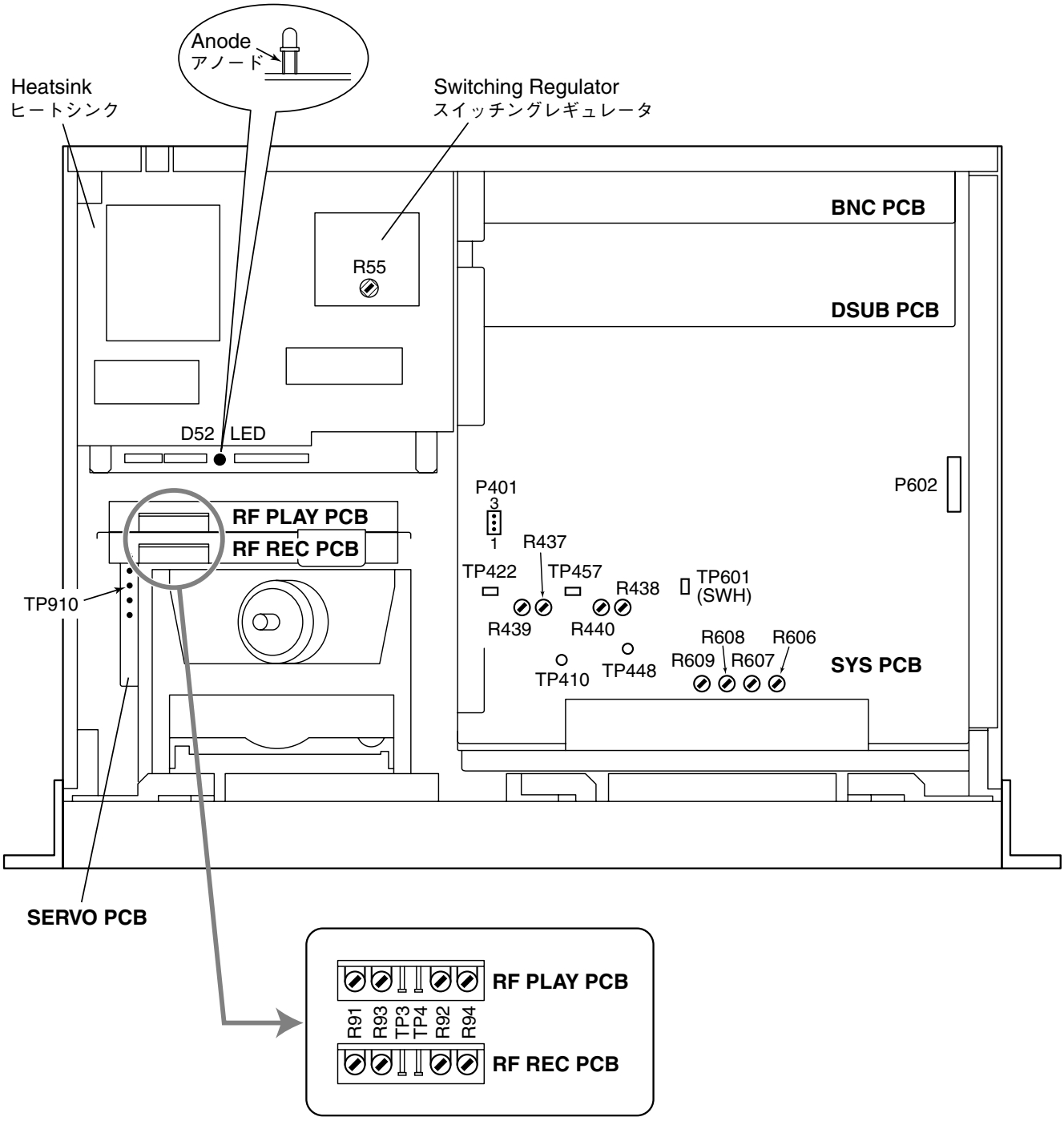


Fig. 5-1

5-2. Test tape

1. TEAC MTT-88101 (Fs=44.1 kHz):
   For adjusting the error rate and the RF level
2. TEAC MTT-88102 (Fs=48 kHz):
   For adjusting the error rate, the RF level,
   and the P.G. position
3. TEAC MTT-88201 : For recording (blank MP tape)
4. TEAC MTT-88202 : For recording (blank ME tape)

5-3. +5 V supply check

1. Connect a digital tester between the heat sink in the switching regulator and the anode of the LED for +5 V supply (D52).
2. Check that the DC voltage reading is +5.1 ± 0.1 V.
3. If voltage is not within these limits, adjust the semi-fixed resistor R55 until correct.

5-4. P.G. (Phase generator) position adjustment

1. Connect CH1 of the oscilloscope to TP410 (RF A-HEAD) on the SYS PCB and CH2 to TP910 (SWP) on the SERVO PCB.
2. Load the test tape MTT-88102.
3. Set the DA-98HR to test mode. (☞ page 7)
4. Select the menu group M in the menu screen.
5. Move the cursor to "PG.AdJuSt" and press ENTER key.
6. Enter the play mode and, using the ▲ and ▼ keys, adjust the lag between the fall of the switching pulse and the end of ATF portion of the RF wave for 250 µsec, as shown in Photo-1.
7. Press STOP, then switch power off to save the setting.
8. Switch on power again, then enter the play mode to check that the lag of 250 µsec is maintained.

5-2. テストテープ

1. TEAC MTT-88101（Fs=44.1 kHz）:
   エラーレート、RFレベル
2. TEAC MTT-88102（Fs=48 kHz）:
   エラーレート、RFレベル、記録位置調整用
3. TEAC MTT-88201 : 記録用MP生テープ（未記録）
4. TEAC MTT-88202 : 記録用ME生テープ（未記録）

5-3. 電源 +5Vの確認

1. スイッチングレギュレーター内のヒートシンクと＋5V用LED（D52）のアノード側間にデジタルテスターを接続する。
2. DC電圧が、＋5.1V±0.1Vであることを確認する。
3. 上記規格内に入っていない場合は、スイッチングレギュレーター内の半固定抵抗 R55で調整する。

5-4. PG（Phase Generator）位置調整

1. オシロスコープのCH1をSYS PCBのTP410（RF A-HEAD）に、CH2をSERVO PCBのTP910（SWP）に接続する。
2. テストテープ MTT-88102を装着する。
3. テストモードにする。（☞ 7ページ）
4. メニュー画面で、メニューグループMを選択する。
5. “PG AdJuSt”にカーソルを合わせ ENTERキーを押す。
6. PLAYモードにして、スイッチングパルスの立ち下がりからRF波形のATF部分の終わりまでが 250 μ secになるように、▲または▼キーを押して調整する。
   （写真-1参照）
7. STOP後、一度電源をOFFして値を記憶させる。
8. 再度電源をONにし、PLAYモードにして250 μ secが変化していないことを確認する。

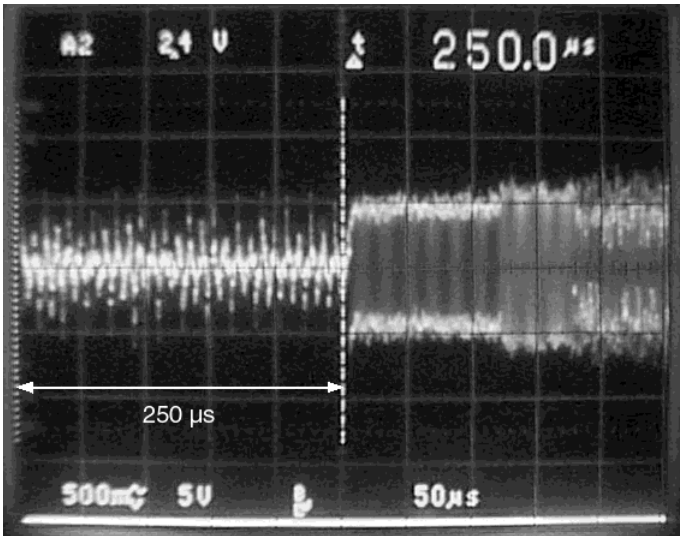


Photo-1

5-5. Offset adjustment in the VCO free-running frequency automatic compensation circuit

1. DTRS mode
   1) Play the MTT-88101 or MTT-88102 test tape.
   2) Short-circuit P401's 1 and 2 on the SYS PCB (A-HEAD placed in test condition).
   3) Connect an oscilloscope to TP422 on the SYS PCB, and adjust the scope range to 1V DC, 0.5 µsec.
   4) Adjust R439 (A-HEAD) on the SYS PCB for 2.5 V DC at TP422.
   5) In a similar way, short-circuit P401's 2 and 3 (B-HEAD placed in test condition), then adjust R440 (B-HEAD) for 2.5 V DC at TP457.
   6) After adjustment is complete, release P401.

   Note)
   In 4) and 5), even if a positive-going or negative-going slight glitch is observed as shown in Fig. 5-2, it should be acceptable. However, perform adjustment to alleviate glitches as much as possible.

5-5. VCOフリーラン周波数自動補正回路のオフセット調整

1. DTRSモード
   1）テストテープ MTT-88101または MTT-88102を再生する。
   2）SYS PCBのP401の1-2間をショートする。
   （A-HEAD テスト状態）
   3）SYS PCBのTP422にオシロスコープを接続し、オシロスコープのレンジをDC 1V, 0.5 μ secにセットする。
   4）TP422のDC電圧が 2.5VになるようにSYS PCBのR439（A-HEAD）を調整する。
   5）同様に、P401の2-3間をショートし（B-HEAD テスト状態)、TP457のDC電圧が 2.5VになるようにR440（B-HEAD）を調整する。
   6）調整後、P401を解放する。

   注）4), 5) 項でオシロスコープの波形が、図5-2のように上または下方向に若干のヒゲが観測されても可とするが、なるべくひげを小さくするように調整する。

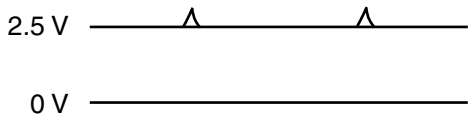


Fig. 5-2

2. HR mode
   1) Play a tape recorded in HR mode.
   2) Short-circuit P401's 1 and 2 on the SYS PCB (A-HEAD placed in test condition).
   3) Connect an oscilloscope to TP422 on the SYS PCB, and adjust the scope range to 1V DC, 0.5 µsec.
   4) Adjust R437 (A-HEAD) on the SYS PCB for 2.5 V DC at TP422.
   5) In a similar way, short-circuit P401's 2 and 3 (B-HEAD placed in test condition), then adjust R438 (B-HEAD) for 2.5 V DC at TP457.
   6) After adjustment is complete, release P401.

2. HRモード
   1）HRモードで記録したテープを再生する。
   2）SYS PCBのP401の1-2間をショートする。
   （A-HEAD テスト状態）
   3）SYS PCBのTP422にオシロスコープを接続し、オシロスコープのレンジをDC 1V, 0.5 μ secにセットする。
   4）TP422のDC電圧が 2.5VになるようにSYS PCBのR437（A-HEAD）を調整する。
   5）同様に、P401の2-3間をショートし（B-HEAD テスト状態)、TP457のDC電圧が 2.5VになるようにR438（B-HEAD）を調整する。
   6）調整後、P401を解放する。

5-6. Playback equalizer adjustment

5-6-1. Checks in Normal mode

1. ME tape
   1) Load Sony ME tape.
   2) Connect the oscilloscope to TP3 (RF A-HEAD) on the RF PLAY PCB , then set the oscilloscope range to 500 mV AC, 50 nsec.
   3) Set REC FUNCTION ON (All channels) and execute format recording in HR mode.
   4) Rewind and play the tape, and observe the eye pattern of A-HEAD.
   5) Adjust R91 on RF PLAY PCB so that the 3.1 MHz waveform is almost flat at top and bottom as shown in Photo-3.
      * Photo-2 shows the eye pattern when the oscilloscope is set to the 50 nsec/div. range.
      * Photo-3 shows the eye pattern when the oscilloscope is set to the 100 nsec/div. range.
   6) Similarly, connect the oscilloscope to TP4 (RF B-HEAD) on the RF PLAY PCB, then observe the eye pattern of B-HEAD.
      For adjustment, use R92 on the RF PLAY PCB.

2. MP tape
   1) Load Sony MP tape.
   2) In the same way as in 1 (adjusting the equalizer using an ME tape), adjust R93 (A-HEAD) and R94 (B-HEAD) on the RF PLAY PCB.

5-6-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-6-1. (The same check, but test points and adjustments not on RF PLAY PCB, but on RF REC PCB.)

5-6. 再生イコライザー調整

5-6-1. ノーマルモードでの確認

1. MEテープ
   1）SONY MEテープを装着する。
   2）RF PLAY PCBのTP3（RF A-HEAD）にオシロスコープを接続し、オシロスコープのレンジを AC 500mV, 50nsecにする。
   3）REC FUNCTION ON（全ch）にし、HRモードでFORMAT記録する。
   4）巻戻して再生したときの A-HEADのアイパターンを観測する。
   5）写真-3のように 3.1MHzの波形の凸凹がほぼフラットになるように RF PLAY PCBの R91を調整する。
      ＊写真-2は、オシロスコープレンジが 50nsec/divの状態です。
      ＊写真-3は、オシロスコープレンジが 100nsec/divの状態です。
   6）RF PLAY PCBの TP4（RF B-HEAD）にオシロスコープを接続し、同様にB-HEADのアイパターンを観測する。
      調整は、RF PLAY PCBの R92で行う。

2. MPテープ
   1）SONY MP テープを装着する。
   2）1項（MEテープ イコライザー調整）と同様の方法で RF PLAY PCBの R93（A-HEAD）, R94（B-HEAD）を調整する。

5-6-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-6-1項と同様の確認を行う。（但し、テストポイント、調整箇所はRF PLAY PCBではなくてRF REC PCBとなります。）

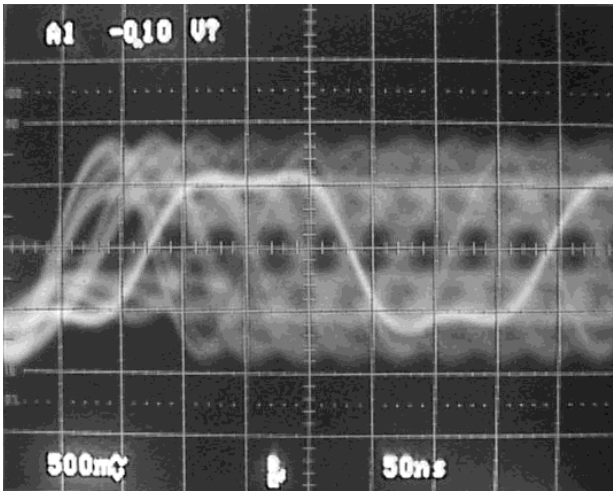


Photo-2. eye pattern (50 nsec/div)

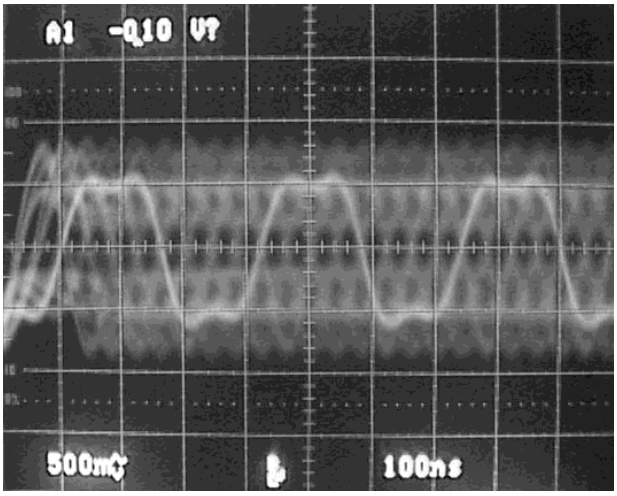


Photo-3. eye pattern (100 nsec/div)

5-7. RF level check

5-7-1. Checks in Normal mode

1. Connect the oscilloscope's CH1 to TP3 (RF A-HEAD) on the RF PLAY PCB and CH2 to TP601 (SWH) on the SYS PCB.
2. Set the oscilloscope's CH1 range to 500 mV AC, 2 msec.
3. Set the oscilloscope's CH2 range to 5 V DC, and (-) trigger.
4. Play the test tape MTT-88101.
5. Observe the waveform at TP3 (RF A-HEAD) , and see that the following standard is satisfied.

   Standard value (see Fig. 5-3):
   B, C (minimum) : 1000 mV or more
   B/A, C/A : 80 % or more

5-7. RFレベル確認

5-7-1. ノーマルモードでの確認

1. オシロスコープのCH1をRF PLAY PCBのTP3（RF A-HEAD）に、CH2をSYS PCBのTP601（SWH）に接続する。
2. オシロスコープの CH1のレンジをAC 500mV, 2msecにセットする。
3. オシロスコープの CH2のレンジをDC 5Vにセットし、（−）トリガーとする。
4. テストテープ MTT-88101を再生する。
5. TP3（RF A-HEAD）の波形を観測し、下記の規格値を満足すること。

   規格値（図5-3参照）
   B, C（最小部）: 1000mV以上
   B/A, C/A　　: 80%以上

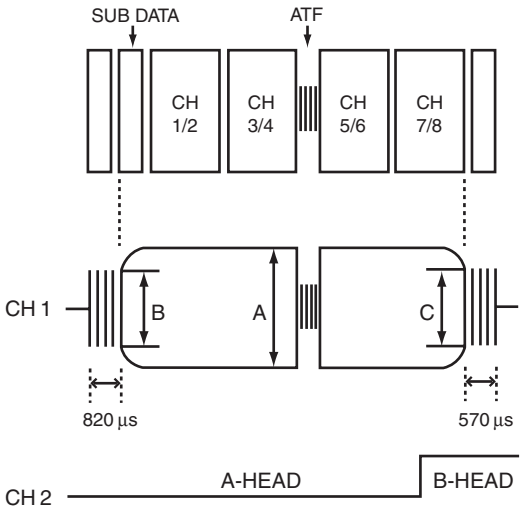


Fig. 5-3

6. Next, set the oscilloscope's CH2 to (+) triggering.
7. Connect the oscilloscope's CH1 to TP4 (RF B-HEAD) on the RF PLAY PCB, then observe the B-HEAD waveform, see that the standard is satisfied:

5-7-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-7-1.

6. 次にオシロスコープのCH2を（+）トリガーにセットする。
7. オシロスコープのCH1をRF PLAY PCBのTP4（RF B-HEAD）に接続して B-HEADの波形を観測し、A-HEADと同様に規格値を満足すること。

5-7-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-7-1項と同様の確認を行う。

5-8. Playback error rate check

5-8-1. Checks in Normal mode

1. ME tape
   1) As shown in Fig. 5-4, connect the ERC-88 error rate counter (P/N:5772926600) to P602 on the SYS PCB via the ERC-78HR adaptor (P/N:V00089100A).
      Note) To supply power to the ERC-88, use the PS-P2 AC adaptor.
   2) Play the MTT-88102 test tape, and check error rate (for both A- and B-HEADS).
      If error rate is out of the following specifications, readjust R91 (A-HEAD) or R92 (B-HEAD) on the RF PLAY PCB. (see paragraph 5-6)

      Standard value : less than 200 x 10^{-4}

5-8. 再生エラーレート確認

5-8-1. ノーマルモードでの確認

1. MEテープ
   1）図5-4のように、SYS PCBのP602にアダプターERC-78HR（品番:V00089100A）を介してエラーレートカウンターERC-88（品番:5772926600）を接続する。
      注）ERC-88には、ACアダプター PS-P2より電源を供給してください。
   2）テストテープ MTT-88102を再生してエラーレート（A-HEAD, B-HEAD共）を確認する。
      エラーレートが下記規格を満足していない場合は、RF PLAY PCBの R91（A-HEAD）または R92（B-HEAD）を再調整する。（5-6項参照）

      規格値 : 200×10^{-4}以下

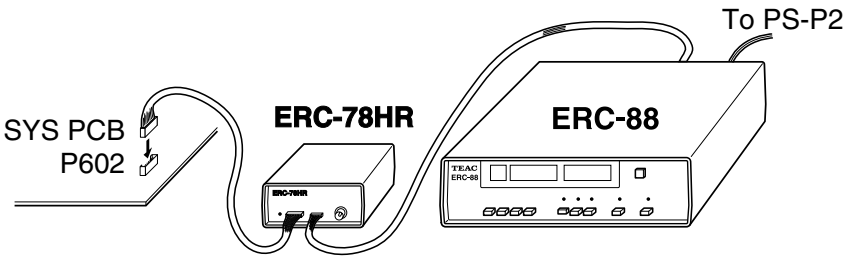


Fig. 5-4

2. MP tape
   Play the MTT-88101 test tape, and confirm the error rate (for both A- and B-HEADS) in the same way as with an ME tape.
   If error rate is out of the following specifications, readjust R93 (A-HEAD) or R94 (B-HEAD) on the RF PLAY PCB. (see paragraph 5-6)

   Standard value : less than 200 x 10^{-4}

2. MPテープ
   テストテ-プ MTT-88101を再生して、MEテープと同様にエラーレート（A-HEAD, B-HEAD共）を確認する。
   エラーレートが下記規格を満足していない場合は、RF PLAY PCBの R93（A-HEAD）または R94（B-HEAD）を再調整する。（5-6項参照）

   規格値 : 200×10^{-4}以下

5-8-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-8-1.

5-8-2. コンフィデンスモードでの確認

コンフフィデンスモードに切換えて、5-8-1項と同様の確認を行う。

5-9. Recording current adjustment

5-9-1. Checks in Normal mode

1. MP tape
   1) Load MP blank tape MTT-88201.
   2) As shown in the Fig. 5-5, connect the REC CURRENT KIT (P/N:V00024700A) between P10 on the MOTHER PCB and P102 on the RF REC PCB.
   3) Set the oscilloscope to 10 mV DC, 50 ns.
   4) Select the menu group 2 in the menu screen.
   5) Move the cursor to "Sine Osc" and press ENTER key.
   6) Press the ▲ key to display "Sine Oscillator 440".

5-9. 記録電流調整

5-9-1. ノーマルモードでの確認

1. MPテープ
   1）MP生テープ MTT-88201を装着する。
   2）図5-5の様に REC CURRENT KIT（品番V00024700A）をMOTHER PCBのP10とRF REC PCBの P102間に接続する。
   3）オシロスコープは、DC 10mV, 50nsに設定する。
   4）メニュー画面で、メニューグループ2を選択する。
   5）“Sine Osc”にカーソルを合わせ、ENTERキーを押す。
   6）▲キーを押して、“Sine Oscillator 440”表示にする。

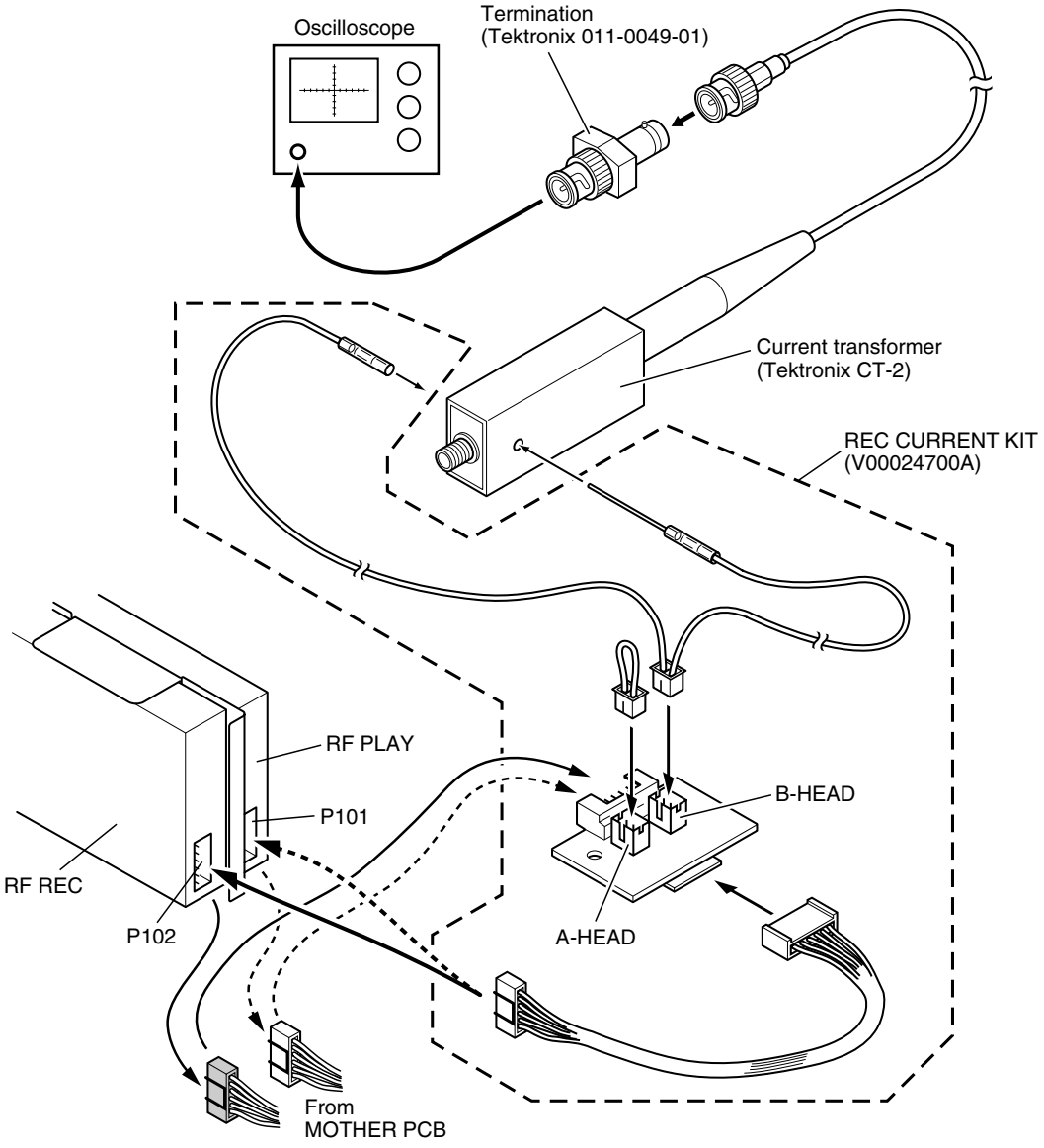


Fig. 5-5

7) Press the ESCAPE key.
8) Enter HR mode and set the REC FUNCTION keys of all channels to ON.
9) Start recording in tape format mode, and adjust R606 on the SYS PCB for 11.2 mAp-p (indication is in voltage) of A-HEAD current.
10) Similarly, adjust R607 for 11.2 mAp-p of B-HEAD current.

Note)
The state in which shorting pins A and B inserted as shown in Fig. 5-5 is one in which current flowing through the B-HEAD is to be measured. The state with shorting pins A and B reversed is one in which current flowing through the A-HEAD is to be measured. For a reference waveform using the oscilloscope, refer to Photo-4.

7）ESCAPEキーを押す。
8）HRモードにし、全CHのREC FUNCTIONキーをONにする。
9）FORMAT 記録状態で、A-HEADの電流値が 11.2 mAp-p（表示は電圧表示）になるようにSYS PCBのR606を調整する。
10）同様に、B-HEADの電流値が 11.2 mAp-pになるようにSYS PCBのR607を調整する。

注）図5-5の様に、ショートピンA, Bを差した状態がB-HEADの電流値測定の状態です。
ショートピンA, Bの差す位置を逆にした状態が、A-HEADの電流値測定の状態です。尚、オシロスコープの参考波形として、写真-4を参照してください。

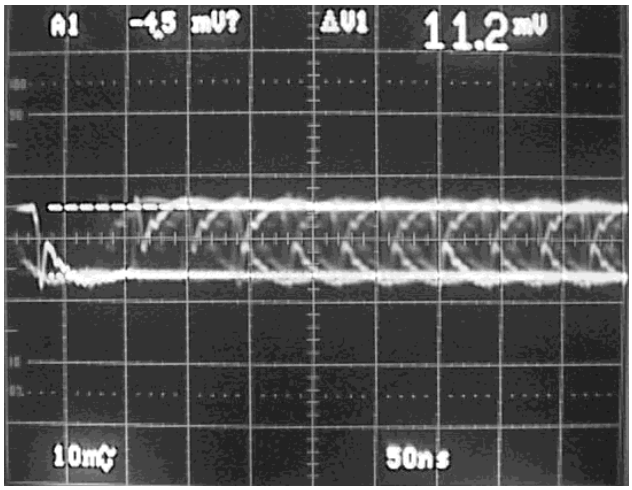


Photo-4

2. ME tape
Load ME blank tape MTT-88202 and check the current values at A-HEAD and B-HEAD in the same way as a MP tape. The current values should be 12.4 ± 0.6 mAp-p.

5-9-2. Checks in Confidence mode

1. Set the Confidence mode on, and connect the REC CURRENT KIT (P/N:V00024700A) between P9 on the MOTHER PCB and P101 on the RF REC PCB.
2. Perform the same check and adjustment as discussed in 5-9-1. Use R608 (A-HEAD) and R609 (B-HEAD) on SYS PCB for adjustment.

2. MEテープ
ME生テープ MTT-88202を装着し、MPテープと同様にA-HEAD, B-HEADの電流値を確認する。
電流値は 12.4±0.6 mAp-p であること。

5-9-2. コンフィデンスモードでの確認

1. コンフィデンスモードに切換え、REC CURRENT KIT（品番V00024700A）をMOTHER PCBのP9とRF PLAY PCBの P101間に接続する。
2. 5-9-1項と同様に確認、調整する。
調整は、SYS PCBのR608（A-HEAD）、R609（B-HEAD）で行う。

5-10. Recording/playback RF level check

5-10-1. Checks in Normal mode

1. After adjusting the recording current following section 5-9, rewind the tape section where format recording was executed in HR mode, and overwrite a signal on that section.
2. Rewind the tape section recorded in 1 above and play it.
3. In the same was as section 5-7, ensure that the RF level is 1200 mV minimum and that the waveform ratio is 80% minimum (with both ME and MP tapes).

5-10-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-10-1.

5-11. Recording/playback error rate check

5-11-1. Checks in Normal mode

Play back the recording you made as per instructions in paragraph 5-10, and check for less than 200 x 10^{-4} of error rate (with both ME and MP tapes).

5-11-2. Checks in Confidence mode

Set the Confidence mode on, and perform the same check as discussed in 5-11-1.

5-10. 記録再生RFレベル確認

5-10-1. ノーマルモードでの確認

1. 5-9項で記録電流調整後、HRモードで FORMAT記録した部分を巻き戻し、その部分にオーバーライト記録する。
2. 1項で記録した部分を巻き戻し、その部分を再生する。
3. 5-7項と同様に、RFレベルが 最小部で 1200mV以上、波形比 80%以上であることを確認する。
（ME, MPテープ共）

5-10-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-10-1項と同様の確認を行う。

5-11. 記録再生エラーレート確認

5-11-1. ノーマルモードでの確認

5-10項で記録した部分を再生する。
このときのエラーレートは、200×10^{-4}以下であること。
（ME, MPテープ共）

5-11-2. コンフィデンスモードでの確認

コンフィデンスモードに切換えて、5-11-1項と同様の確認を行う。

PARTS LIST SECTION

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with ∗ require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in the manual.
- ⚠Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J]: JAPAN [US/C]: U.S.A./CANADA [E]: EUROPE [K]: KOREA
  [UK]: U.K. [A]: AUSTRALIA

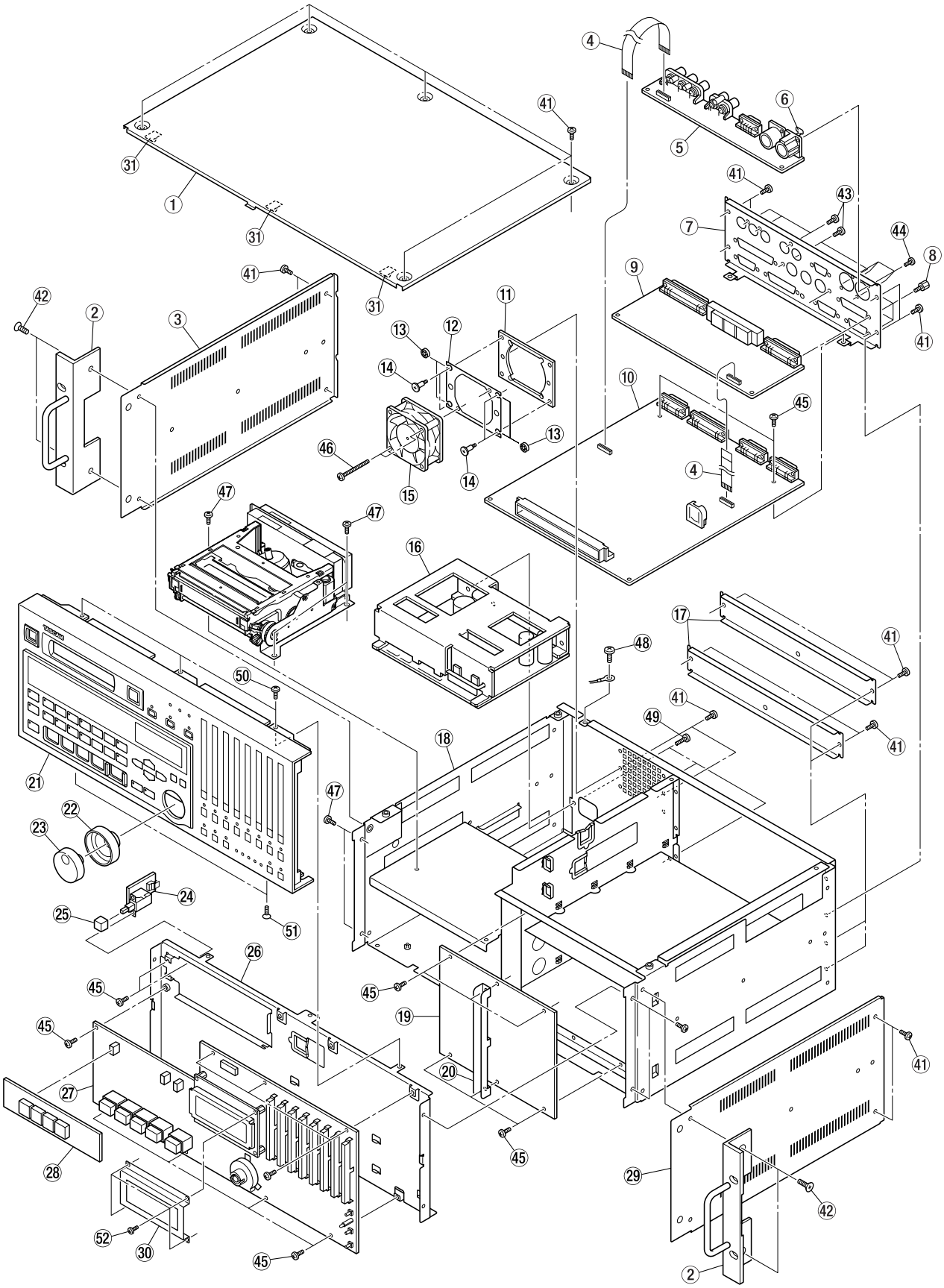
注 意

- プリント基板は部品面が示されています。
- ∗印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品及び品番のない部品は供給しません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠は安全重要部品です。
  交換する時は必ずティアック指定の部品を使用してください。
- 仕向先
  [J]: JAPAN [US/C]: U.S.A./CANADA [E]: EUROPE [K]: KOREA
  [UK]: U.K. [A]: AUSTRALIA

6. EXPLODED VIEWS AND PARTS LIST

分解図とパーツリスト

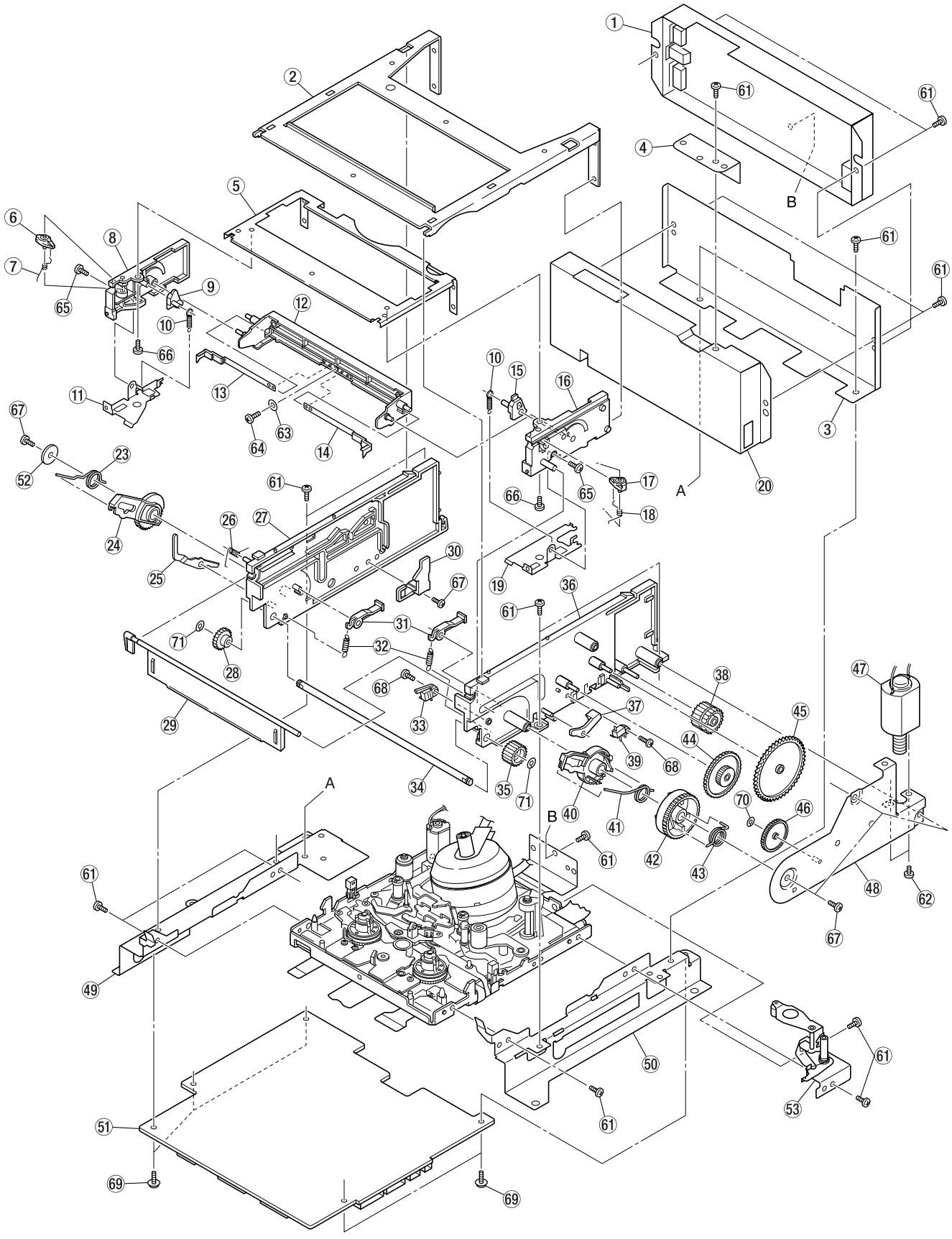
EXPLODED VIEW-1



EXPLODED VIEW-1

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	*M01074900A	COVER,TOP	
1- 2	*M01074800A	ANGLE ASSY	
1- 3	*M01075000A	COVER,SIDE L	
1- 4	*E00556300A	FLAT CABLE,DSUB16	
1- 5	*E95105500A	PCB ASSY,BNC	
1- 6	5334075900	CLAMP,CANNON CONNECTOR SOCKET	
1- 7	*M01075400A	REAR PANEL,SYS	
1- 8	5801536400	SCREW,DSUB LOCK M2.6X0.45	
1- 9	*E95105600A	PCB ASSY,DSUB	
1-10	*E95106300A	PCB ASSY,SYS	
1-11	*M01075700A	BRACKET,FAN A	
1-12	*M01075900A	BRACKET,FAN B	
1-13	*M00039100A	DAMPER	
1-14	*M00039000A	PIN,STEP	
1-15	*E0051380	DC FAN MOT,FBA06A12L	
1-16	*E00345500C	SW RGLTD PS [J,US/C]	
	*E00345540C	SW RGLTD PS [E,K,UK,A]	
1-17	*M01075600A	REAR PANEL,BLANK	
1-18	*M01075300B	CHASSIS ASSY	
1-19	*E95106400A	PCB ASSY,MOTHER	
1-20	*M00617200A	BRACKET	
1-21	*M01073500B	FRONT PANEL ASSY	
1-22	M01074700A	KNOB,SHUTTLE N64	
1-23	M01074600A	KNOB,JOG N64	
1-24	*E95103200A	PCB ASSY,SW	
1-25	M00001500A	BUTTON,C	
1-26	*M01075100B	CHASSIS,FRONT	
1-27	*E95103000A	PCB ASSY,KEY	
1-28	*E95103100A	PCB ASSY,COUNTER	
1-29	*M01075001A	COVER,SIDE R	
1-30	*M01217300A	SHIELD SHEET,LCD	
1-31	5801599400	GASKET	
1-41	5780023006	SCREW,BIND M3X6 (BLK NI)	
1-42	5780224008	SCREW,FLAT M4X8 (BLK NI)	
1-43	5783543008	SCREW,BIND P-TITE M3X8 (BLK NI)	
1-44	*5780112605	SCREW,PAN M2.6X5 (NI)	
1-45	5780003006	SCREW,BIND M3X6	
1-46	5780003030	SCREW,BIND M3X30	
1-47	5780103006	SCREW,PAN M3X6	
1-48	5780004008	SCREW,BIND M4X8	
1-49	5780023010	SCREW,BIND M3X10 (BLK NI)	
1-50	*B00049700A	SCREW,BPAR3*6FZC	
1-51	5780203006	SCREW,FLAT M3X6	
1-52	5780002604	SCREW,BIND M2.6X4	

EXPLODED VIEW-2

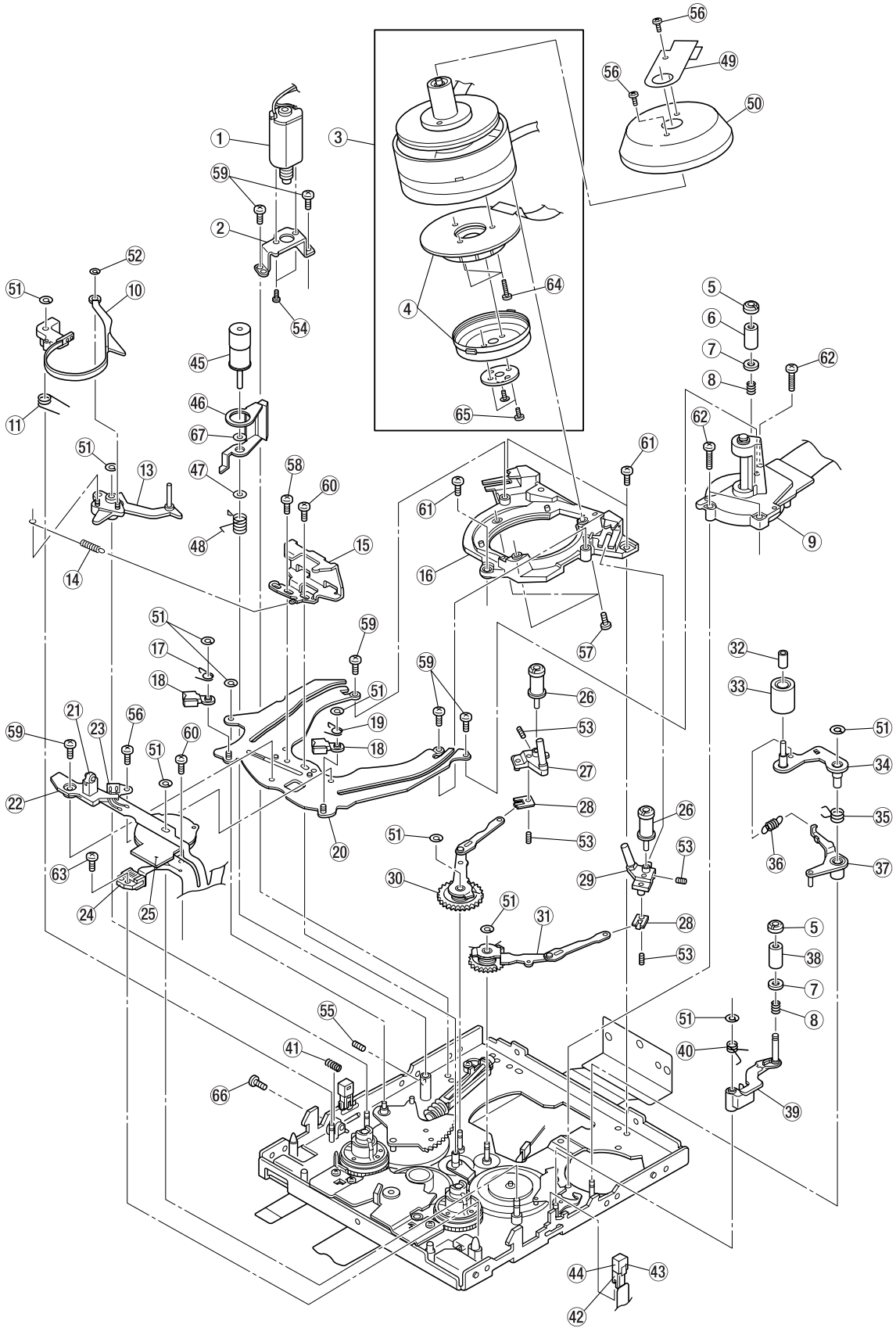


EXPLODED VIEW-2

REF.NO.	PARTS NO.	DESCRIPTION
2- 1	*E95106000A	PCB ASSY,RF PLAY
2- 2	5801527902	BRACKET,CAM PLATE
2- 3	*M01101300A	BRACKET,RF
2- 4	*M01101600A	SHIELD PLATE,FPC
2- 5	M00434400A	HOLDER,MAIN
2- 6	5801525500	LEVER L,CASSETTE PRESS
2- 7	5801525600	SPRING,COIL LLCP
2- 8	5801525300	BASE L,SLIDE
2- 9	5801525700	LEVER L,BRAKE
2-10	5801525800	SPRING T,BRAKE
2-11	5801525400	SUB HOLDER L
2-12	5801524601	OPENER,LID
2-13	5801524700	LEVER L ASSY,LOCK
2-14	5801525000	LEVER R ASSY,LOCK
2-15	5801526300	LEVER R,BRAKE
2-16	5801525900	BASE R,SLIDE
2-17	5801526100	LEVER R,CASSETTE PRESS
2-18	5801526200	SPRING,COIL LRCP
2-19	5801526000	SUB HOLDER R
2-20	*E95106100A	PCB ASSY,RF REC
2-21	Vacant	
2-22	Vacant	
2-23	5801526800	SPRING,COIL CPL
2-24	5801526700	GEAR L,TRANSFER
2-25	5801528000	LEVER,FRONT LID
2-26	5801529200	SPRING,COIL LID
2-27	*5801526503	PLATE L,CAM
2-28	5801528700	GEAR L,SYNCRONIZE
2-29	M00365790B	DOOR,LID FRONT 78
2-30	5801526601	CAM,LID OPENER
2-31	5801528900	LEVER,LOCK
2-32	5801529000	SPRING T,LOCK LEVER
2-33	5300060200	SW,PUSH SPPB21
2-34	5801528600	SHAFT,SYNCRONIZE
2-35	5801528800	GEAR R,SYNCRONIZE
2-36	5801526902	PLATE R,CAM
2-37	5801527000	LEVER,SWITCH
2-38	5801528200	GEAR A,REDUCTION
2-39	5300060100	SW,PUSH SPPB12
2-40	5801527100	GEAR R,TRANSFER
2-41	5801527200	SPRING,COIL CPR
2-42	5801527300	GEAR,RELEASE
2-43	5801527400	SPRING,COIL GR
2-44	5801528400	GEAR C,REDUCTION
2-45	5801528300	GEAR B,REDUCTION
2-46	5801528500	GEAR D,REDUCTION
2-47	5600165100	MOTOR SUB ASSY,CASSETTE
2-48	5801527601	BRACKET ASSY,C MOTOR
2-49	*M00434100A	BRACKET,L
2-50	*M00434200A	BRACKET,R

REF.NO.	PARTS NO.	DESCRIPTION
2-51	*E95106200B	PCB ASSY,SERVO
2-52	5801528100	PLATE,TRANSFER GEAR
2-53	M00435600A	CLEANER ASSY,HEAD
2-61	5780012004	SCREW,BIND M2X4 (NI)
2-62	5782522028	SCREW,PAN 1# M2X2.8 (NI)
2-63	5785022200	WASHER,2X6X0.4T
2-64	5782551640	SCREW,PAN BT 3# M1.6X4 (NI)
2-65	5782521630	SCREW,PAN 3# M1.6X3 (NI)
2-66	5782521625	SCREW,PAN 3# M1.6X2.5 (NI)
2-67	5782552040	SCREW,PAN BT 3# M2X4 (NI)
2-68	5782552080	SCREW,PAN BT 3# M2X8 (NI)
2-69	B0005020	SCREW,PPAB 2X5FNI
2-70	5785341200	WASHER,POLYS. 1.7X4X0.25T
2-71	5785343000	WASHER,POLYS. 3.2X5.5X0.25T

EXPLODED VIEW-3

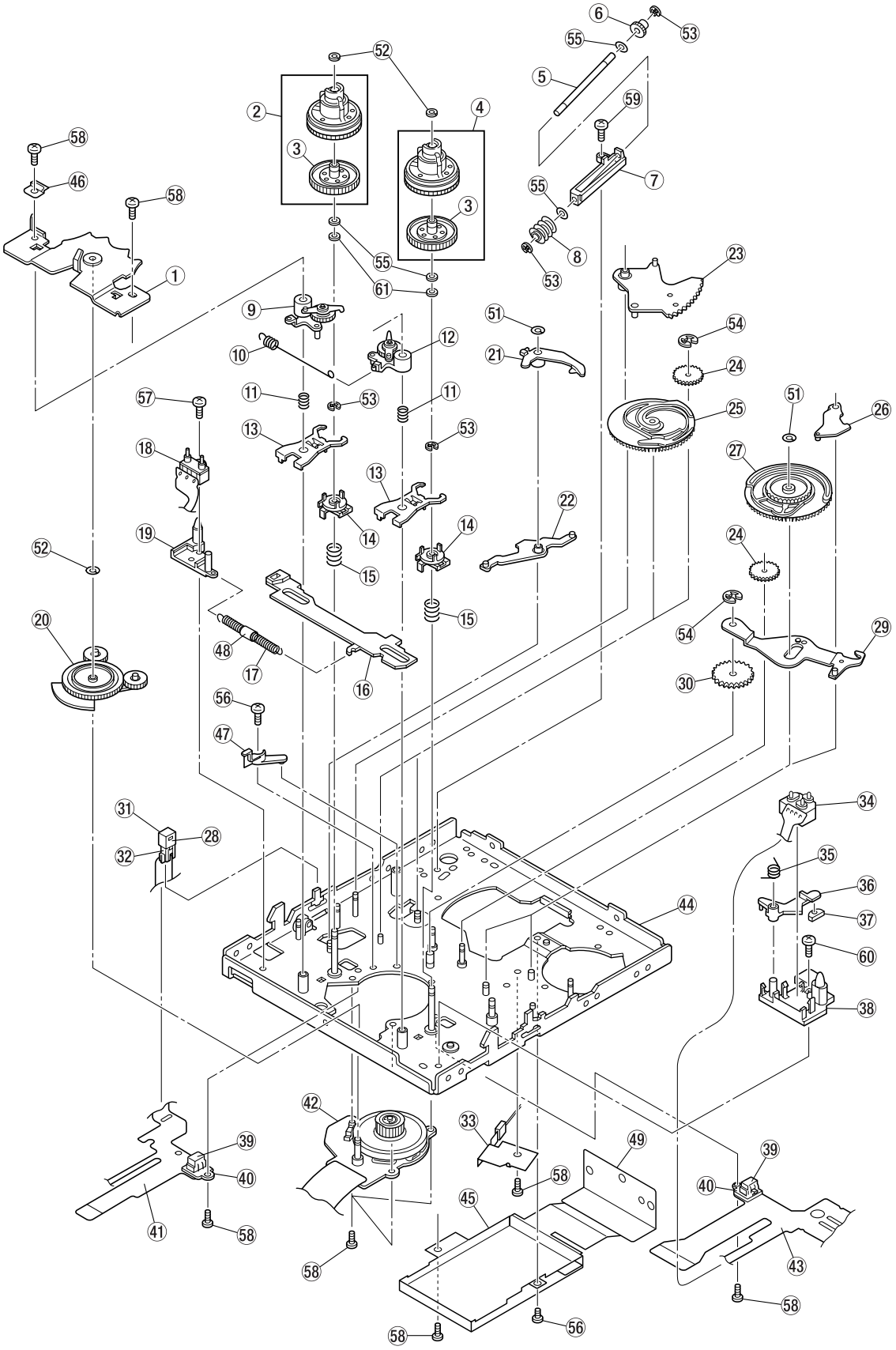


EXPLODED VIEW-3

REF.NO.	PARTS NO.	DESCRIPTION
3- 1	*M00438800A	LD MOTOR ASSY,DTRS
3- 2	M00434000A	HOLDER,LD MOTOR
3- 3	M01101100A	DRUM ASSY,98HR
3- 4	1473407500	MOTOR ASSY,DRAM
3- 5	1676742500	FLANGE,NUT
3- 6	1676744900	GUIDE,CAPSTAN
3- 7	1676742300	FRANGE,GUIDE
3- 8	1638547600	SPRING C
3- 9	1473407700	MOTOR,CAPSTAN
3-10	M00822300A	BRAKE ASSY,BAND
3-11	1638913401	SPRING,COIL 01
3-12	Vacant	
3-13	1796821300	LEVER ASSY,BACK TENSION
3-14	1638209100	SPRING T
3-15	1680464800	PLATE,PROTECTOR
3-16	1615405600	BASE ASSY,DRAM
3-17	1638913800	SPRING,COIL
3-18	1796826300	LEVER ASSY,SOFT BRAKE
3-19	M00256300A	TORSION SPRING,20G
3-20	1615405700	PLATE ASSY,GUIDE RAIL
3-21	13419521	PHOTO ELEMENT,GL450
3-22	1678872150	BRACKET,LED (BRACK)
3-23	13299679	SENSOR,DEW HDP-07-C2
3-24	14771017	SOLENOID,LUTCH 6V 240 OHM
3-25	1796822901	MODE SW ASSY (01)
3-26	1796826900	ROLLER ASSY,M GUIDE
3-27	1796822700	SLIDE MGS ASSY
3-28	1680461900	BRACKET MG
3-29	1796822800	SLIDE MGT ASSY
3-30	1796821100	LEVER ASSY,L THREAD
3-31	1796821200	LEVER ASSY,R THREAD
3-32	1678871800	SLEEVE,PINCH ROLLER
3-33	1796821900	ROLLER ASSY,PINCH
3-34	1796821700	LEVER ASSY,PINCH
3-35	1638913500	SPRING,COIL
3-36	1638209200	SPRING T
3-37	1796821800	LINK ASSY,PINCH
3-38	1676742400	GUIDE,FINAL
3-39	1796822200	LEVER ASSY,GUIDE
3-40	1638913600	SPRING,COIL
3-41	1638547500	SPRING,C
3-42	1678872700	HOLDER,TE SENSOR
3-43	13419660	PHOTO ELEMENT,RPM-20PB-T
3-44	1680472902	PLATE,SLIT 02
3-45	1796822600	ROLLER ASSY,IMPEADANCE
3-46	M00123400A	CLEANER ASSY,TAPE
3-47	M0090610	WASHER,1.63X3X0.13
3-48	M00122100A	TORSION SPRING,ARM T
3-49	M00433900A	SHIELD PLATE,FPC
3-50	M00433800A	SHIELD PLATE,S

REF.NO.	PARTS NO.	DESCRIPTION
3-51	16499908	WASHER,SLIT 1.57X4X0.3
3-52	16499907	WASHER,SLIT 1.2X3X0.3
3-53	B0001450	SPBOLT,NO.0 PAN1.2X2.5FNB
3-54	16502019	SCREW,PAN NO.0 3# 2X2
3-55	B0001540	SPBOLT,NO.0 TP3P1.4X2FNB
3-56	16499864	SCREW,PAN NO.0 M1.6X2
3-57	16499873	SCREW,PAN NO.0 M1.6X5.5
3-58	16499772	SCREW,PAN NO.0 3# 2X2
3-59	16499773	SCREW,PAN NO.0 3# 2X2.5
3-60	16499909	SCREW,PAN NO.0 3# 2X3.5
3-61	16499776	SCREW PAN NO.0 3# 2X5
3-62	16499910	SCREW PAN NO.0 3# 2X8
3-63	16502031	SCREW,TAP TITE ETP 1.4X3.5
3-64	16502044	SCREW,PAN NO.0 1.6X6.5
3-65	*16499870	SCREW PAN NO.0 M1.6X4
3-66	B0000430	SCREW,PAN NO.0 3 2X4.5
3-67	M0090660	WASHER,3.85X6X0.2

EXPLODED VIEW-4



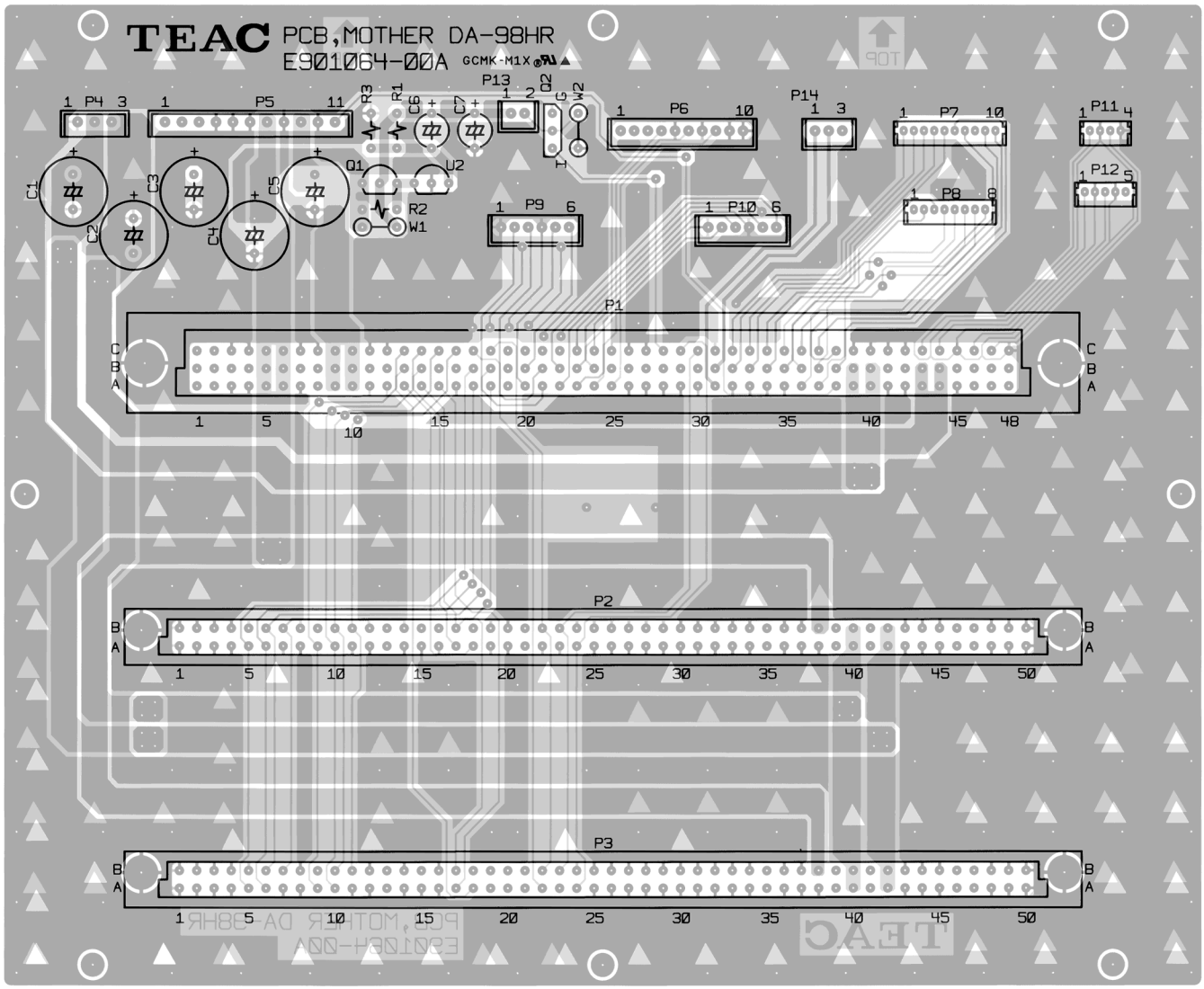
EXPLODED VIEW-4

REF.NO.	PARTS NO.	DESCRIPTION
4- 1	1680462100	BRACKET,T OPENER
4- 2	M00607100A	REEL TABLE ASSY,S
4- 3	1796826600	DISC ASSY,REFRECTOR
4- 4	M00607200B	REEL TABLE ASSY,T
4- 5	1676741400	SHAFT,LOADING GEAR
4- 6	1678870600	WORM WHEEL,LOADING
4- 7	1680460800	BRACKET,GEAR
4- 8	1678870700	WORM,LOADING
4- 9	M00877600A	BRAKE ASSY,S
4-10	1638209000	SPRING T
4-11	1638547400	SPRING C
4-12	M00877700A	BRAKE ASSY,T
4-13	1680460600	LEVER,CLUTCH
4-14	1796820200	CLUTCH ASSY
4-15	1638547300	SPRING C
4-16	1678870001	SLIDE,REEL OPERATING CAM
4-17	1638208900	SPRING T
4-18	13222478	SW,PUSH SPPW62 SPPW62
4-19	1678872500	HOLDER,SWL
4-20	1796826100	GEAR ASSY,CENTER
4-21	1678871700	LEVER,REEL LOCK
4-22	1796820701	LEVER ASSY,SLIDE (-01)
4-23	1796821003	GEAR ASSY,SECTOR (-03)
4-24	1678871000	GEAR B,COUPLING
4-25	1678870800	CAM L,LOGIC
4-26	1796822000	CAM FOLLOWER ASSY,PINCH
4-27	1678871100	CAM R,LOGIC
4-28	1680472902	PLATE,SLIT 02
4-29	1796822300	LEVER ASSY,GUIDE CARRY
4-30	1678870900	GEAR A,COUPLING
4-31	13419660	PHOTO ELEMENT,RPM-20PB-T
4-32	1678872700	HOLDER,TE SENSOR
4-33	M00914300A	BRUSH ASSY
4-34	13222479	SW,PUSH SW-101-2P
4-35	1638913100	SPRING,COIL
4-36	1678870402	LEVER,SLID KEEP (02)
4-37	14771018	SOLENOID,LUTCH
4-38	1678872601	HOLDER,SWR (01)
4-39	13419663	PHOTO ELEMENT,NJL5165KA
4-40	1678872400	HOLDER,REEL SENSOR
4-41	1336133600	PCB,SENSOR L
4-42	1473407800	MOTER,REEL
4-43	1336133700	PCB,SENSOR R
4-44	1796823001	MECHA CHASSIS ASSY (01)
4-45	*M01101700A	COVER,BRUSH
4-46	1630187000	STOPPER TB
4-47	1678889500	SUPPORT,TR BAND
4-48	13090294	TUBE,F 2 PHI
4-49	*M01101600A	SHIELD PLATE,FPC

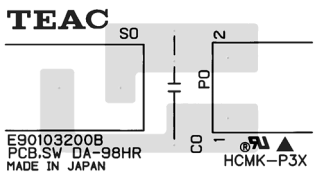
REF.NO.	PARTS NO.	DESCRIPTION
4-51	16499908	WASHER,SLIT 1.57X4X0.3
4-52	16499907	WASHER,SLIT 1.2X3X0.3
4-53	16351100	E-RING,1.2J
4-54	16351150	E-RING,2.5J
4-55	16496335	WASHER,1.7X3.2X0.25
4-56	16499864	SCREW,PAN NO.0 M1.6X2
4-57	16499873	SCREW,PAN NO.0 M1.6X5.5
4-58	16499773	SCREW,PAN NO.0 3# 2X2.5
4-59	16499909	SCREW,PAN NO.0 3# 2X3.5
4-60	16499776	SCREW PAN NO.0 3# 2X5
4-61	16496604	WASHER,1.7X3.2X0.13

7. PC BOARDS AND PARTS LIST
基板図とパーツリスト

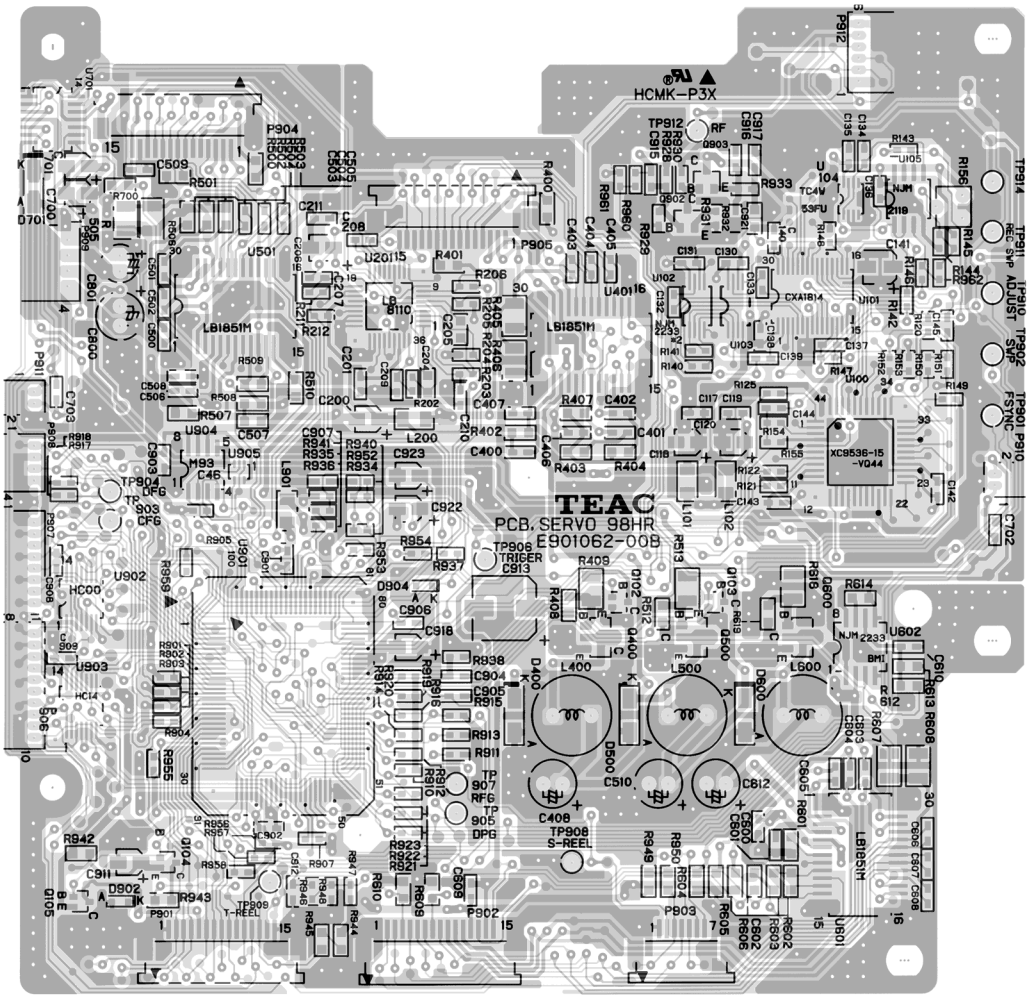
MOTHER PCB



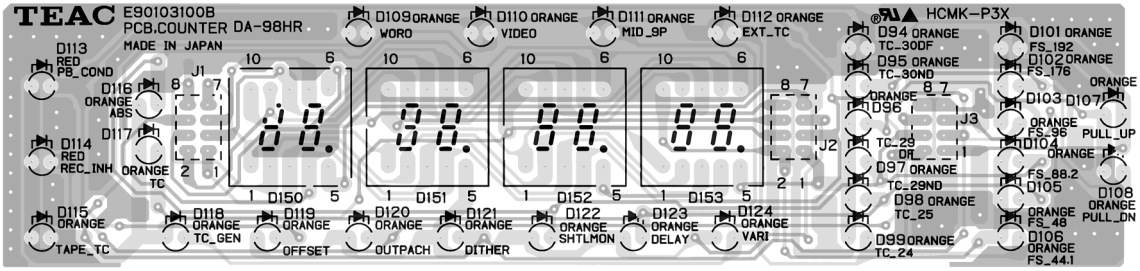
SW PCB



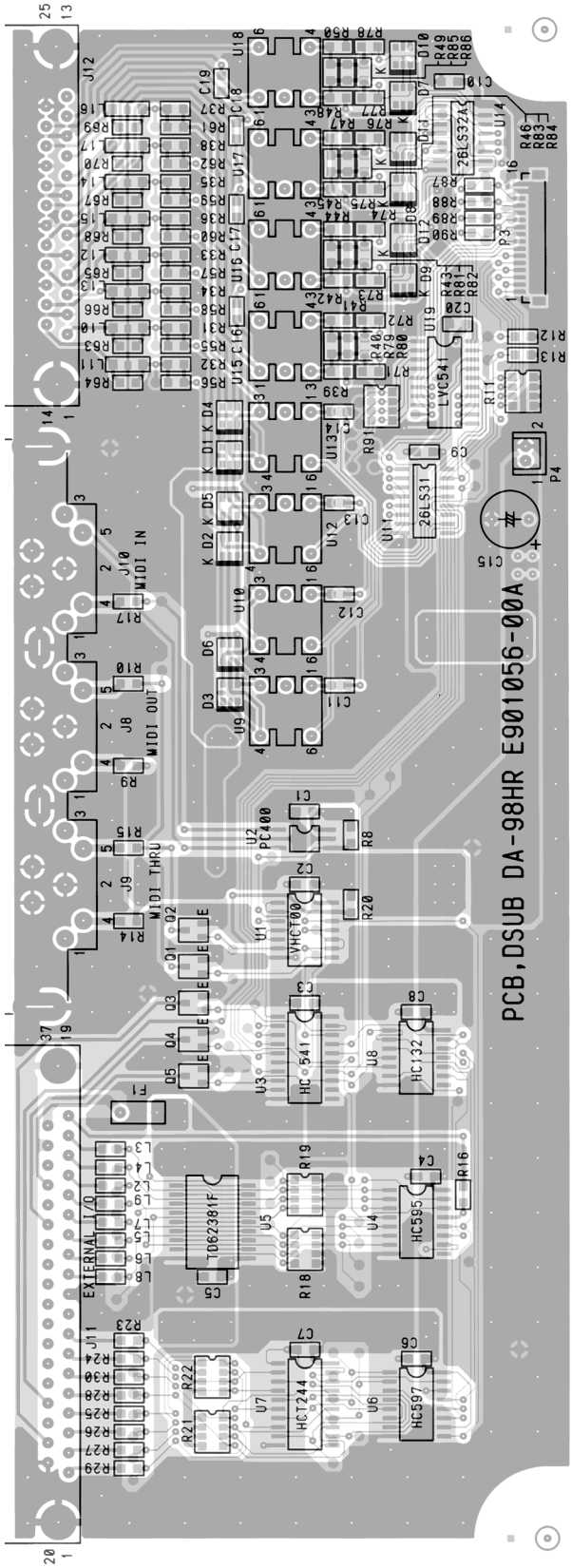
SERVO PCB



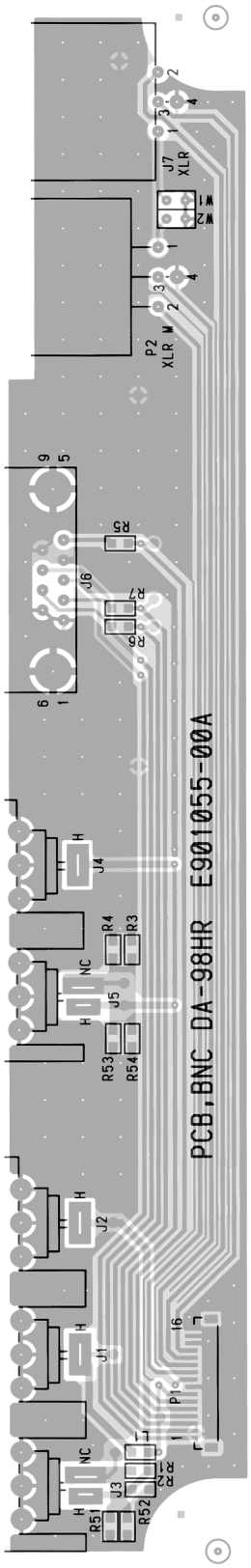
COUNTER PCB



DSUB PCB

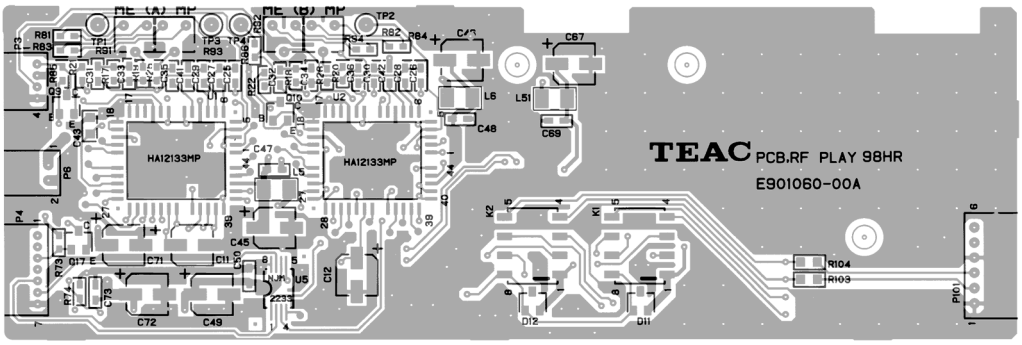


BNC PCB



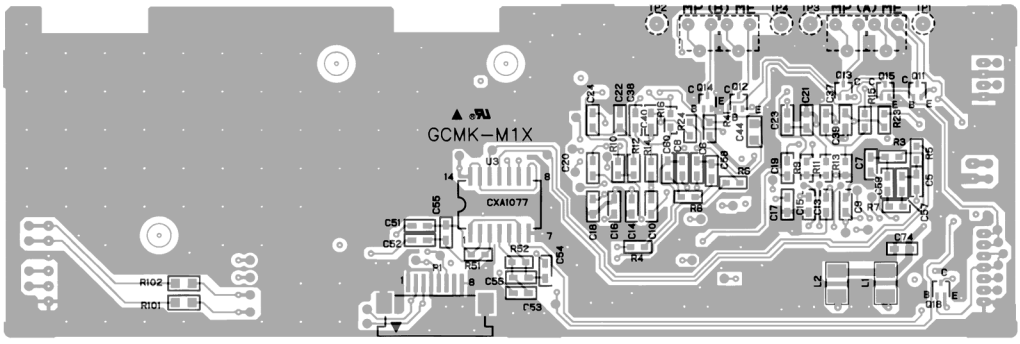
RF PLAY PCB

SIDE A



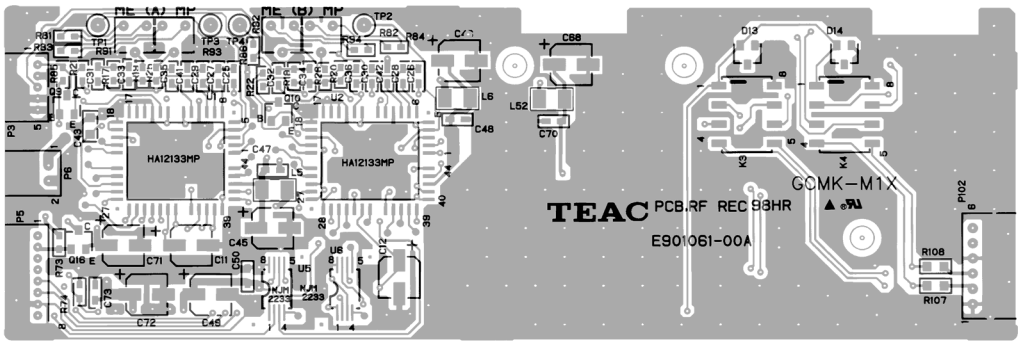
RF PLAY PCB

SIDE B



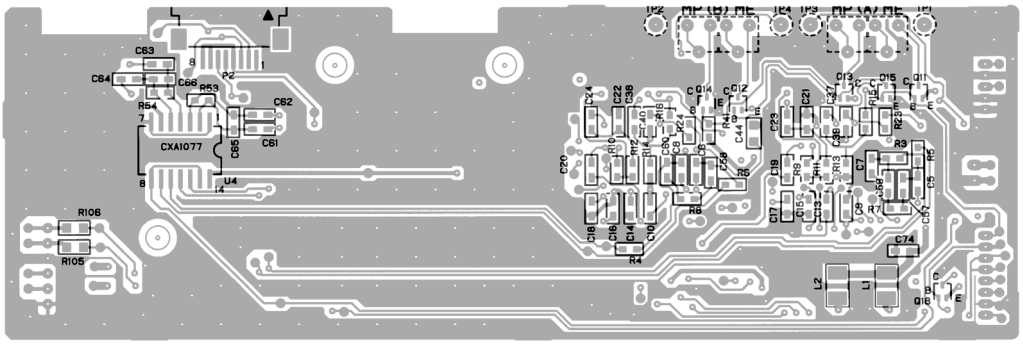
RF REC PCB

SIDE A



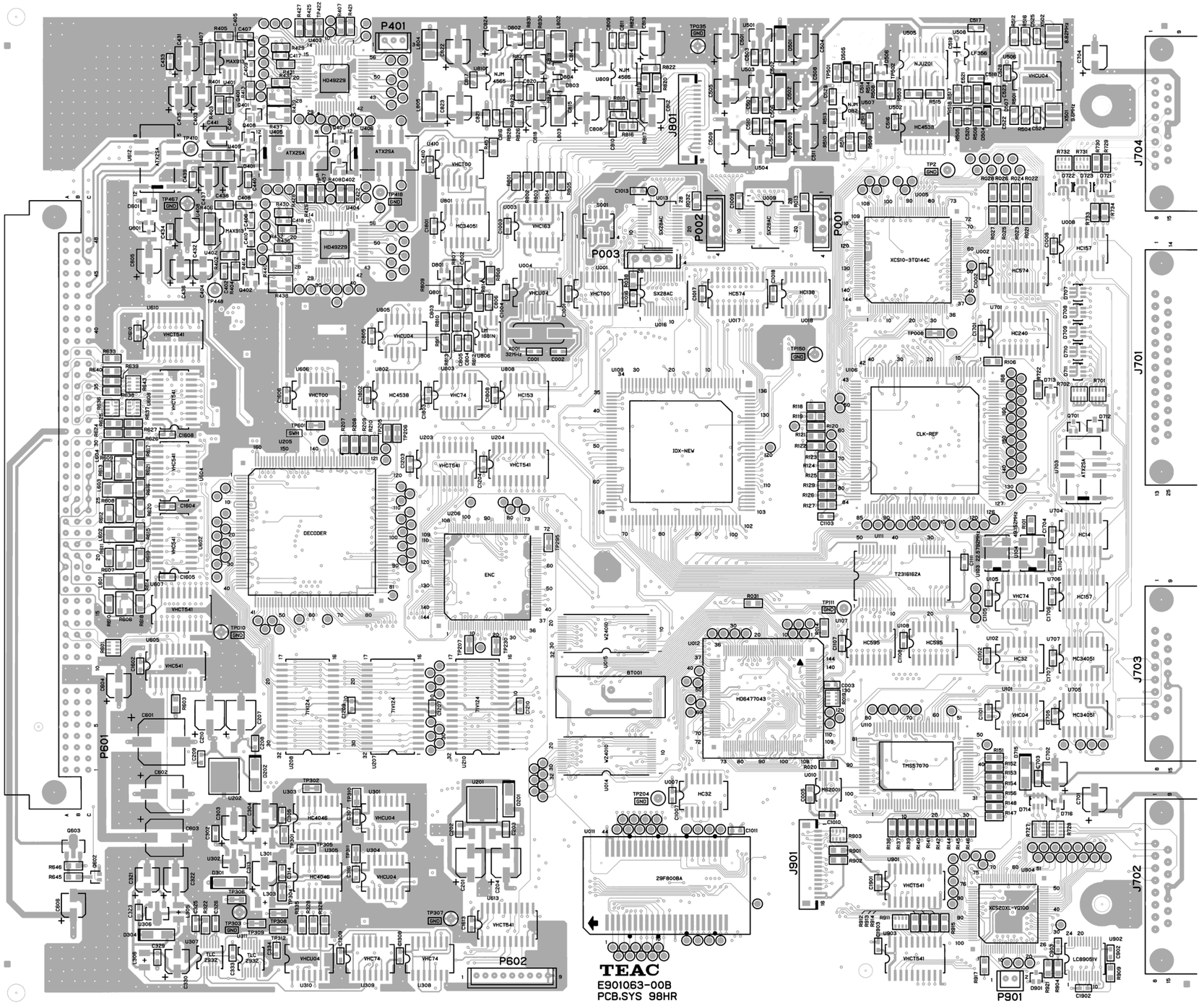
RF REC PCB

SIDE B



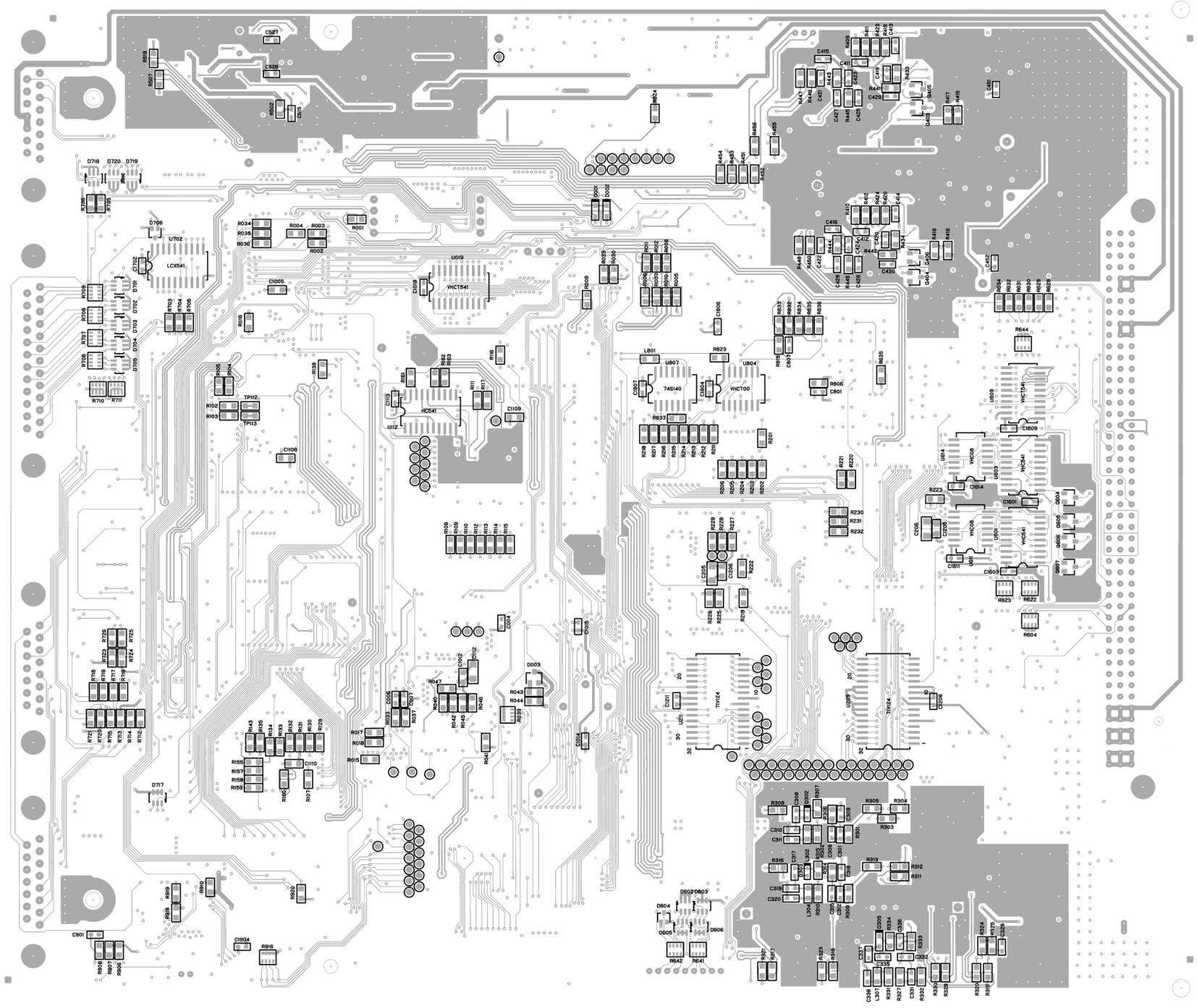
SYS PCB

SIDE A

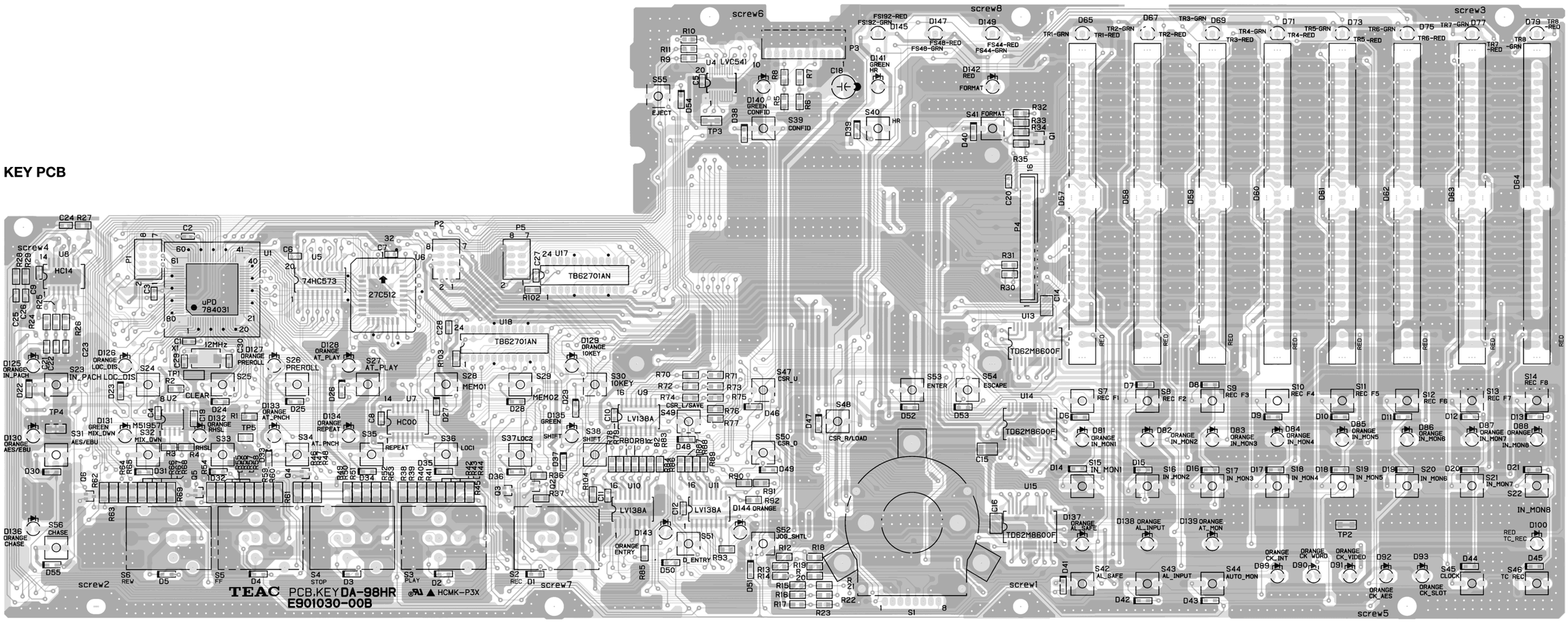


SYS PCB

SIDE B



KEY PCB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screw8
screw3
screw4
screw2
screw7
screw1
screw5
P1
P2
P3
P4
P5
U1 uPD 784031
U2 CLEAR
U4 LVC541
U5 74HC573
U6 27C512
U7 HC00
U9 10KEY
U10 LV138A
U11 LV138A
U13 TD62MB600F
U14 TD62MB600F
U15 TD62MB600F
U17 TB62701AN
U18 TB62701AN
X1 12MHz
S1 JOG_SHTL
S2 REC
S3 PLAY
S4 STOP
S5 FF
S6 REW
S7 REC F1
S8 REC F2
S9 REC F3
S10 REC F4
S11 REC F5
S12 REC F6
S13 REC F7
S14 REC F8
S15 IN_MON1
S16 IN_MON2
S17 IN_MON3
S18 IN_MON4
S19 IN_MON5
S20 IN_MON6
S21 IN_MON7
S22 IN_MON8
S23 IN_PACH
S24 LOC_DIS
S25 CLEAR
S26 PREROLL
S27 AT_PLAY
S28 MEM01
S29 MEM02
S30 10KEY
S31 AES/EBU
S32 MIX_DWN
S33 RHSL
S34 AT_PNCH
S35 REPEAT
S36 LOC1
S37 LOC2
S38 SHIFT
S39 CONFID
S40 HR
S41 FORMAT
S42 AL_SAFE
S43 AL_INPUT
S44 AUTO_MON
S45 CLOCK
S46 TC REC
S47 CSR_U
S48 CSR_R/LOAD
S49 CSR_L/SAVE
S50 CSR_D
S51 D_ENTRY
S52 JOG_SHTL
S53 ENTER
S54 ESCAPE
S55 EJECT
S56 CHASE
D1 REC
D2 PLAY
D3 STOP
D4 FF
D5 REW
D6 LOC_DIS
D7 REC F1
D8 REC F2
D9 REC F3
D10 REC F4
D11 REC F5
D12 REC F6
D13 REC F7
D14 IN_MON1
D15 IN_MON2
D16 IN_MON3
D17 IN_MON4
D18 IN_MON5
D19 IN_MON6
D20 IN_MON7
D21 IN_MON8
D22 IN_PACH
D23 LOC_DIS
D24 CLEAR
D25 PREROLL
D26 AT_PLAY
D27 MEM01
D28 MEM02
D29 10KEY
D30 AES/EBU
D31 MIX_DWN
D32 RHSL
D33 AT_PNCH
D34 REPEAT
D35 LOC1
D36 LOC2
D37 SHIFT
D38 CONFID
D39 HR
D40 FORMAT
D41 AL_SAFE
D42 AL_INPUT
D43 AUTO_MON
D44 CLOCK
D45 TC REC
D46 CSR_U
D47 CSR_L/SAVE
D48 CSR_R/LOAD
D49 CSR_D
D50 D_ENTRY
D52 ENTER
D53 ESCAPE
D54 EJECT
D55 CHASE
D57 TR1-GRN
D58 TR1-RED
D59 TR2-GRN
D60 TR2-RED
D61 TR3-GRN
D62 TR3-RED
D63 TR4-GRN
D64 TR4-RED
D65 TR5-GRN
D67 TR5-RED
D69 TR6-GRN
D71 TR6-RED
D73 TR7-GRN
D75 TR7-RED
D77 TR8-GRN
D79 TR8-RED
D81 IN_MON1
D82 IN_MON2
D83 IN_MON3
D84 IN_MON4
D85 IN_MON5
D86 IN_MON6
D87 IN_MON7
D88 IN_MON8
D89 CK_INT
D90 CK_WORD
D91 CK_VIDEO
D92 CK_AES
D93 CK_SLOT
D100 TC_REC
D125 IN_PACH
D126 LOC_DIS
D127 PREROLL
D128 AT_PLAY
D129 10KEY
D130 AES/EBU
D131 MIX_DWN
D132 RHSL
D133 AT_PNCH
D134 REPEAT
D135 SHIFT
D136 CHASE
D137 AL_SAFE
D138 AL_INPUT
D139 AT_MON
D140 CONFID
D141 HR
D142 FORMAT
D143 ENTRY
D144 ORANGE
D145 FS192-GRN
D147 FS48-GRN
D149 FS44-GRN
TP1
TP2
TP3
TP4
TP5
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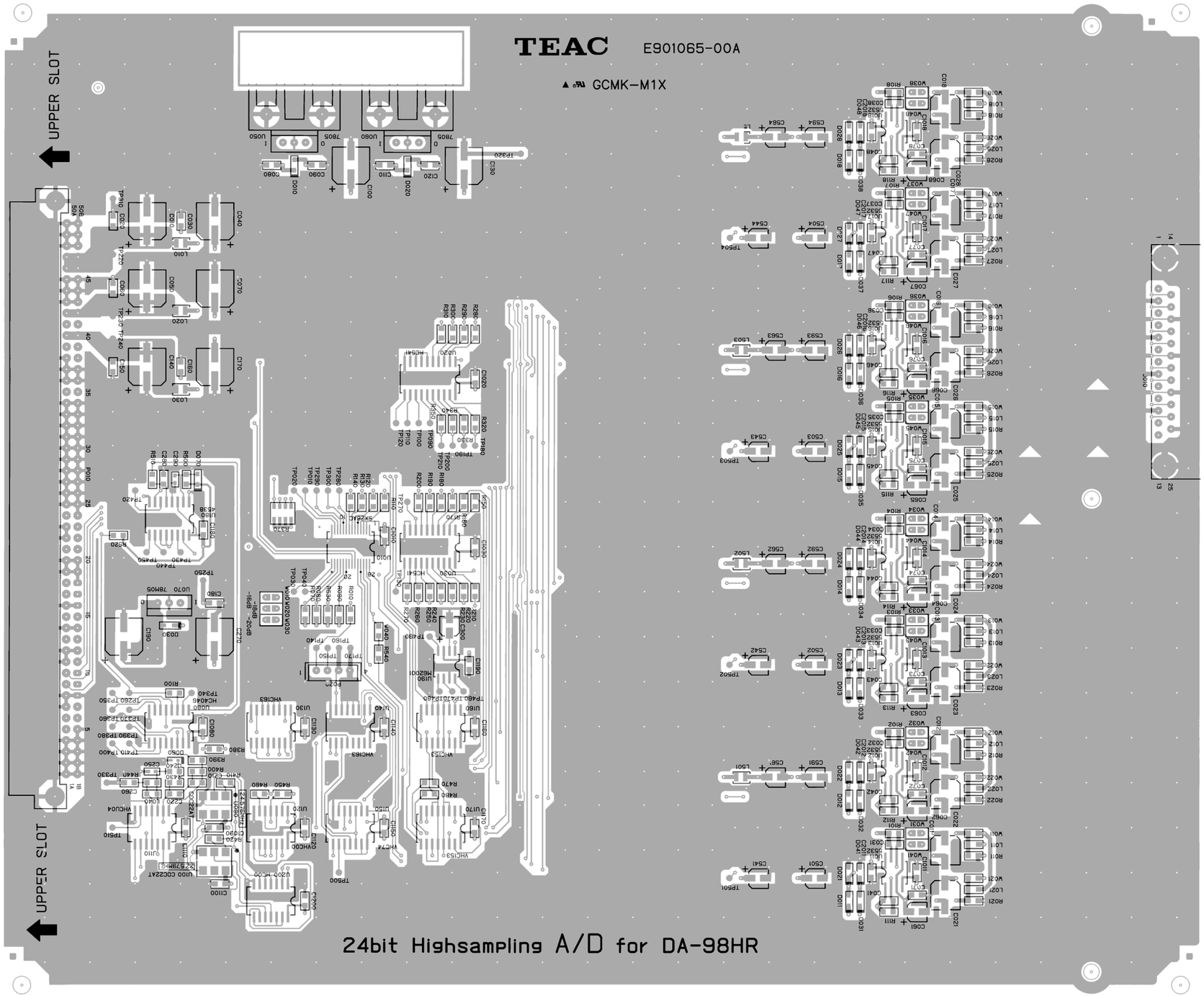
E901030-00B
HCMK-P3X

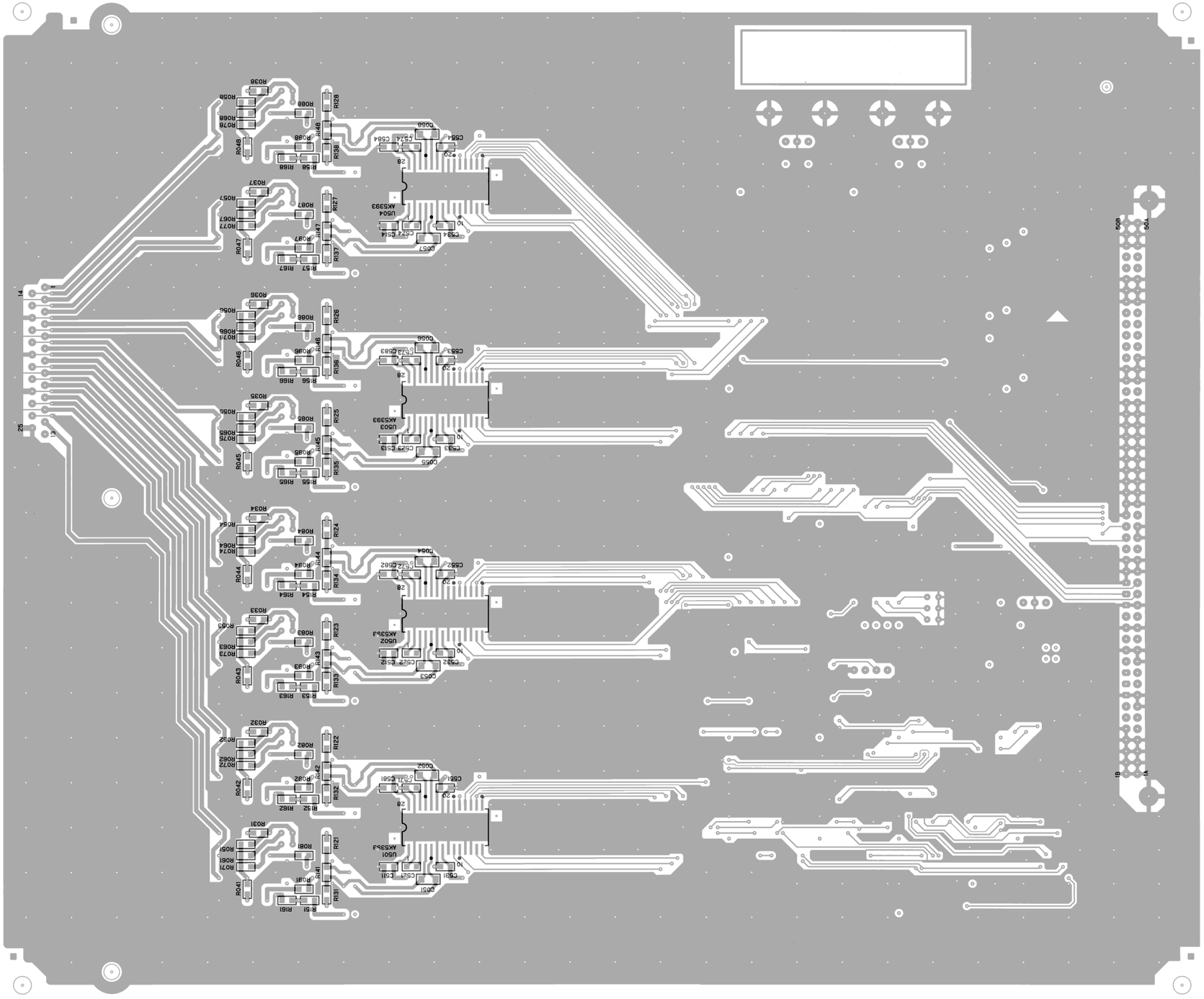
IF98AD PCB (IF-AN98HR)

SIDE A



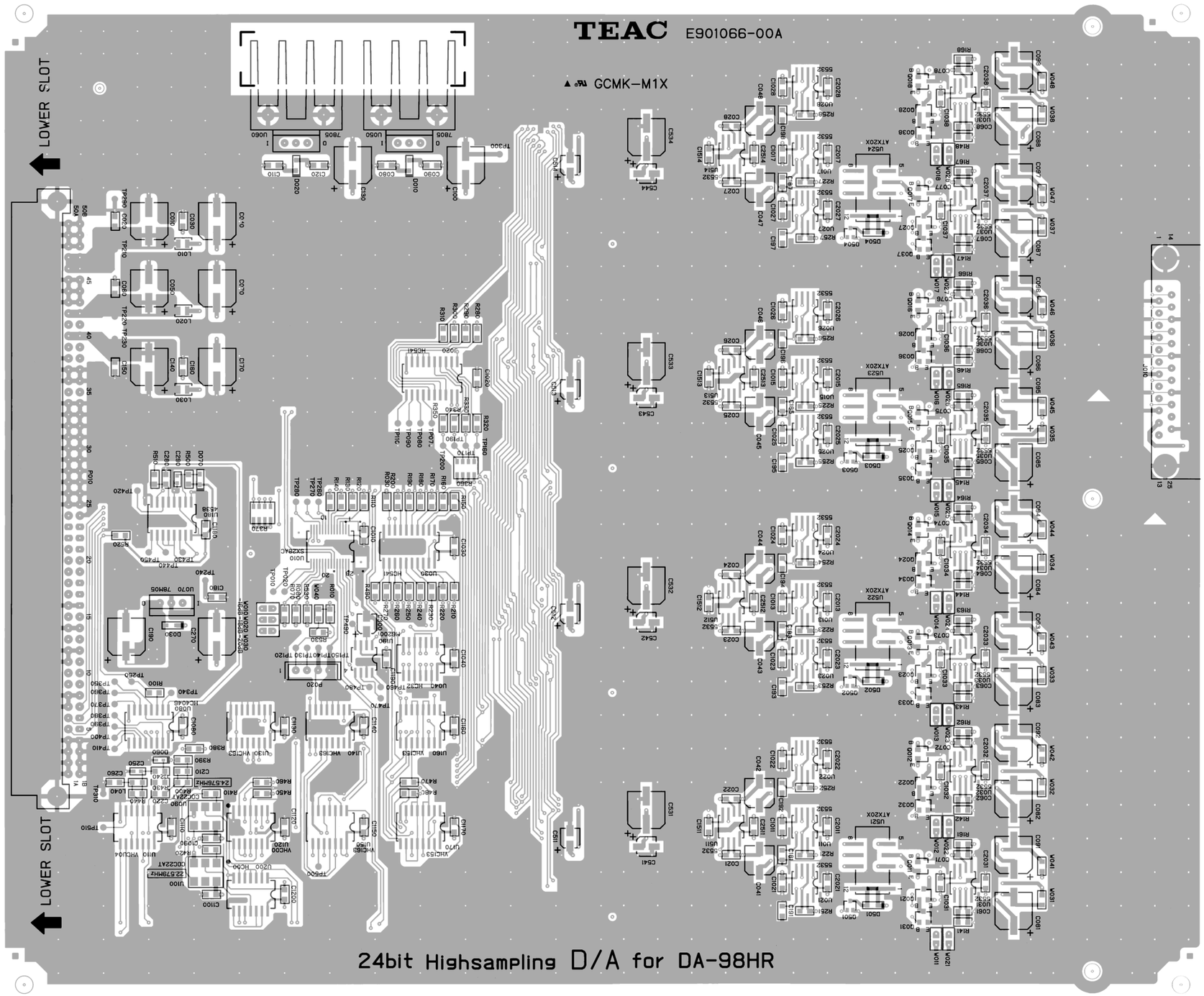
IF98AD PCB (IF-AN98HR)

SIDE B



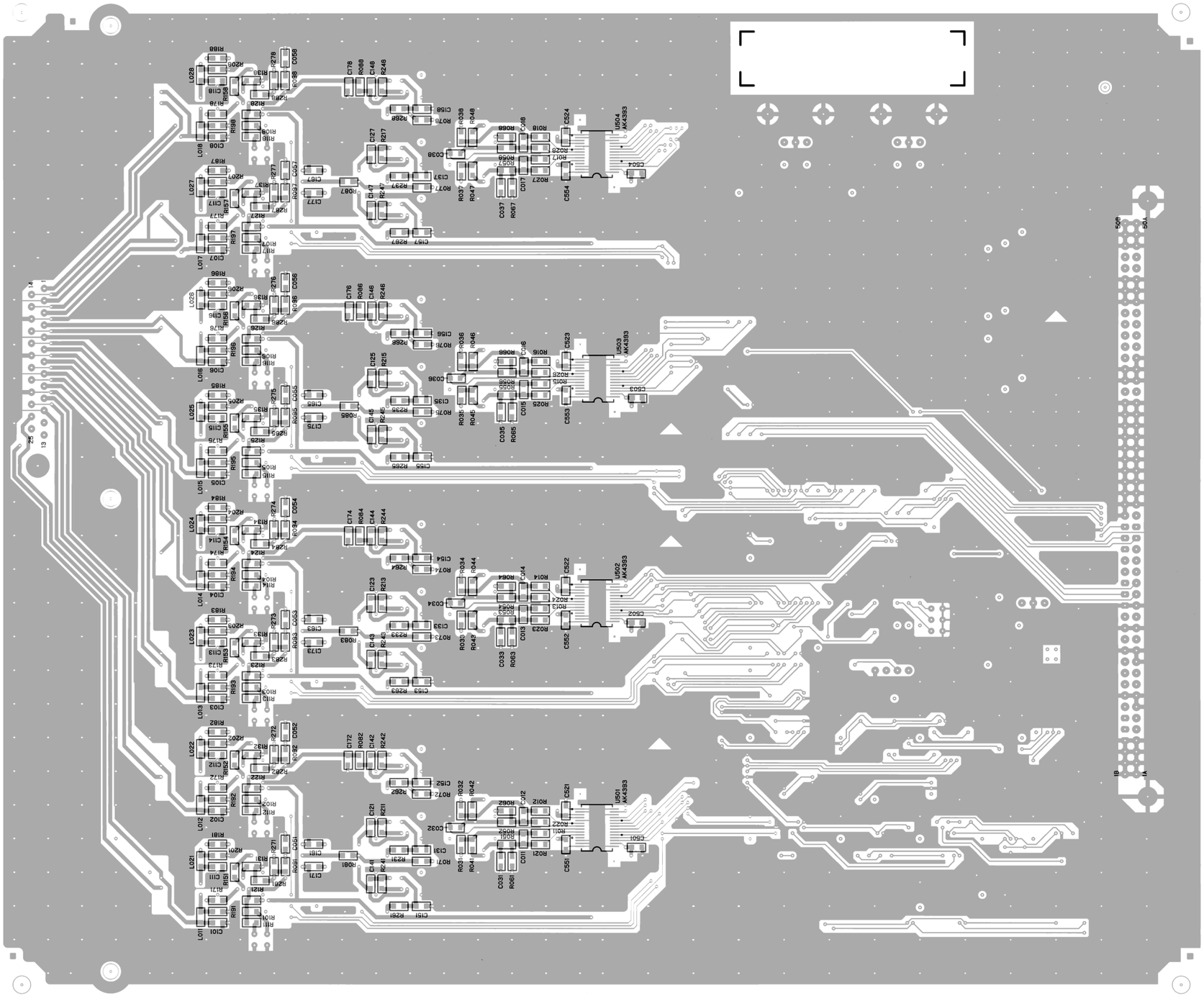
IF98DA PCB (IF-AN98HR)

SIDE A



IF98DA PCB (IF-AN98HR)

SIDE B



MOTHER PCB ASSY

REF.NO.		PARTS NO.	DESCRIPTION
		*E95106400A	PCB ASSY,MOTHER
		*E90106400A	PCB,MOTHER
P1		E0033030	CONNECTOR,PCN10MA-144S
P2,3		5334079500	SOCKET,CONN. 100P
P4		5336303300	PLUG,CONN. B3B-EH(WHT)
P5		5336304100	PLUG,CONN. B11B-EH(WHT)
P6		5336250000	PLUG,CONN. B10B-PH-K-S(WHT)
P7		13124432	CONNECTOR,ZH B 10B-ZR
P8		13124430	CONNECTOR,ZH B 8B-ZR
P9		5336251600	PLUG,CONN. B06B-PH-K-R(RED)
P10		5336249600	PLUG,CONN. B06B-PH-K-S(WHT)
P11		13124426	CONNECTOR,ZH B 4B-ZR
P12		13124427	CONNECTOR,ZH B 5B-ZR
P13		5336249200	PLUG,CONN. B02B-PH-K-S(WHT)
P14		5336249300	PLUG,CONN. B03B-PH-K-S(WHT)
Q1		S0031562	TR,2SB1592
U2		5220446100	IC,M5237L

SW PCB ASSY

REF.NO.		PARTS NO.	DESCRIPTION
		*E95103200A	PCB ASSY,SW
		*E90103200B	PCB,SW
C0	⚠	E0022570	SPK KILLER,0.0047UF 250V
P0		E0042990	CONNECTOR,S2P3-VH
S0	⚠	E0038520	SW,PUSH SDDLB14000

SERVO PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106200B	PCB ASSY,SERVO
	*E90106200B	PCB,SERVO
D400	5224019200	DIODE,EC10QS04TE12L
D500	5224019200	DIODE,EC10QS04TE12L
D600	5224019200	DIODE,EC10QS04TE12L
D701	S0021554	DIODE,RB070L-40TE25
D902,904	S0022094	DIODE,1SS355
L101,102	E0022854	COIL,CHIP 100UF
L200	E0022854	COIL,CHIP 100UF
L400,500	14728449	COIL,390UH 10%
L600	14728444	COIL,150UH 10%
L901	E0022854	COIL,CHIP 100UF
P901	13153693	CONNECTOR,52271-1590
P902	13153479	CONNECTOR,15P
P903	5336379500	CONNECTOR,7P 52271-0790
P904,905	13153693	CONNECTOR,52271-1590
P906	13124443	CONNECTOR,ZH S10B-ZR
P907	13124025	CONNECTOR,ZN S 8B-ZR
P908	13124021	CONNECTOR,ZN S 4B-ZR
P909	5336287400	PLUG,CONN. S4B-PH-K-S(WHT)

SERVO PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
P910	13124435	CONNECTOR,ZH S 2B-ZR
P911	13124435	CONNECTOR,ZH S 2B-ZR
P912	13124439	CONNECTOR,ZH S 6B-ZR
Q102,103	S0000674	TR,DTC123JUA
Q104,105	S0019894	TR,DTA114EUA-T106
Q400	5230020200	TR,2SA1314B-TE12L,C
Q500	5230020200	TR,2SA1314B-TE12L,C
Q600	5230020200	TR,2SA1314B-TE12L,C
Q902,903	13427337	TR,2SC2412K
R156	R0016720	VAR RES,4.7KB RH0422C
U100	S00381800A	IC,ATF-CTRL
U101	S0038383	IC,CXA1814N
U102,103	S0020414	IC,NJM2233BV-TE1
U104	S0001204	IC,TC4W53FU-TE12L
U105	S0038394	IC,NJM2119M
U201	5220448800	IC,LB8110M
U401,501	5220448900	IC,LB1851M
U601	5220448900	IC,LB1851M
U602	5220450800	IC,TL5001CPS-T
U701	5220449000	IC,LB1836M
U901	S00241900A	IC,UPD78146GF-025-3BA
U902	S0033274	IC,SN74LV00APW
U903	S0020454	IC,SN74LV14PW
U904	S0033414	IC,M93C46-MN6T
U905	S0034654	IC,TC7S08FU

COUNTER PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95103100A	PCB ASSY,COUNTER
	*E90103100B	PCB,COUNTER
D101-112	5225018500	LED,SLR-34DU3F
D101A-108A	M00608701A	SPACER,LH-5 L=2
D109A-112A	M00608701A	SPACER,LH-5 L=2
D113-114	5225013500	LED,SLR-34VR3F (RED)
D113A-124A	M00608701A	SPACER,LH-5 L=2
D115-124	5225018500	LED,SLR-34DU3F
D150-153	5225028400	LED,INDICATOR,LB-302DF
D94-99	5225018500	LED,SLR-34DU3F
D94A-99A	M00608701A	SPACER,LH-5 L=2
J1-3	5336372000	SOCKET,CONN. 8P BTK 8S-2S

DSUB PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95105600A	PCB ASSY,DSUB
	*E90105600A	PCB,DSUB
D1-12	13411596	DIODE,IMN10
F1	E0039020	CKT PTCT,RXE010
J8-10	E0022450	CONNECTOR,DIN5 YKF51-5040
J11	E0032230	CONNECTOR,DSUB 37PIN
J12	E0032220	CONNECTOR,DSUB 25PIN
L2-9	5347027700	FERRITE BEADS,CHIP BK2125HS121
L10-17	5292810900	EMI FILTER,CHIP 100PFT
P3	E0032364	CONNECTOR,FMN 16BMT
P4	5336249200	PLUG,CONN. B02B-PH-K-S(WHT)
Q1-5	13428287	TR,DTC124EKAT-146
R11	11985206	RES ARRAY,CHIP 4X10K J
R18,19	11985206	RES ARRAY,CHIP 4X10K J
R21,22	11985206	RES ARRAY,CHIP 4X10K J
R91	11985206	RES ARRAY,CHIP 4X10K J
U1	S0024314	IC,TC74VHCT00F(EL)
U2	S0024184	PHOTO COUPLER,PC400
U3	S0000584	IC,HD74HC541FPEL
U4	5220121100	IC,HD74HC595FPEL
U5	S0036924	TR,TD62381F TP
U6	5220117000	IC,HD74HC597FP
U7	S0038234	IC,TC74HCT244AF
U8	5220111400	IC,HD74HC132FP
U9-10	E00595800A	TRANS,PULSE 400UH
U11	S0038974	IC,DS26C31TMX
U12-13	E00595800A	TRANS,PULSE 400UH
U14	S0038984	IC,DS26C32ATMX
U15-18	E00595800A	TRANS,PULSE 400UH
U19	S0020344	IC,TC74VHC541

BNC PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95105500A	PCB ASSY,BNC
	*E90105500A	PCB,BNC
J1-3	E0033070	JACK,P2286-A BNC3P(1SW)
J4-5	E0033060	JACK,P2360 BNC2P(1SW)
J6	E0032200	CONNECTOR,DSUB 9PIN
J7	5334076000	SOCKET,CANNON CONNECTOR
L1	5347027700	FERRITE BEADS,CHIP BK2125HS121
P1	E0032364	CONNECTOR,FMN 16BMT
P2	5334072800	PLUG,CANNON CONNECTOR

RF PLAY PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106000A	PCB ASSY,RF PLAY
	*E90106000A	PCB,RF PLAY
	*M01101400A	SHIELD COVER,RF P
D11,12	S0023224	DIODE,DAN217 T146
K1,2	E0054744	RELAY,G6K-2F
L1,2	14728152	COIL,CHIP 47UF 10%
L5,6	14728152	COIL,CHIP 47UH 10%
L51	14728152	COIL,CHIP 47UH 10%
P1	13153472	CONNECTOR,8P
P3	13124021	CONNECTOR,ZN S 4B-ZR
P4	13124440	CONNECTOR,ZH S 7B-ZR
P6	5336287200	PLUG,CONN. S2B-PH-K-S(WHT)
P101	5336287600	PLUG,CONN. S6B-PH-K-S(WHT)
Q9,10	13427337	TR,2SC2412K
Q11-15	S0020404	TR,DTC124EEATL
Q17	13427256	TR,DTD123YK
Q18	S0024374	TR,DTA124EETL
R91-94	R0016700	VAR RES,2.2KB RH0422C
U1,2	5220449300	IC,HA12133MP
U3	13448164	IC,CXA1077M-T4
U5	S0020414	IC,NJM2233BV-TE1

RF REC PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106100A	PCB ASSY,RF REC
	*E90106100A	PCB,RF REC
	*M01101500A	SHIELD COVER,RF R
D13,14	S0023224	DIODE,DAN217 T146
K3,4	E0054744	RELAY,G6K-2F
L1,2	14728152	COIL,CHIP 47UH 10%
L5,6	14728152	COIL,CHIP 47UH 10%
L52	14728152	COIL,CHIP 47UH 10%
P2	13153472	CONNECTOR,8P
P3	13124438	CONNECTOR,ZH S 5B-ZR
P5	13124025	CONNECTOR,ZN S 8B-ZR
P6	5336287200	PLUG,CONN. S2B-PH-K-S(WHT)
P102	5336291600	PLUG,CONN. S6B-PH-K-R(RED)
Q9,10	13427337	TR,2SC2412K
Q11-15	S0020404	TR,DTC124EEATL
Q16	13427250	TR,DTB123YK
Q18	S0024374	TR,DTA124EETL
R91-94	R0016700	VAR RES,2.2KB RH0422C
U1,2	5220449300	IC,HA12133MP
U4	13448164	IC,CXA1077M-T4
U5	S0020414	IC,NJM2233BV-TE1
U6	S0020414	IC,NJM2233BV-TE1

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106300A	PCB ASSY,SYS
	*E90106300B	PCB,SYS
	*M00473600A	HEATSINK,IOX
	*M00473900A	SPACER,IOX
	*5780002606	SCREW,BIND M2.6X6
BT1	E0055380	BATTERY,CR2032
BT1A	E0055390	HOLDER,BCR20V4
D001,002	13411644	DIODE,CHIP 1SS355 TE-17
D003	S0035734	DIODE,1SS377(TE85L)
D201,202	13411667	DIODE,CHIP HRF22
D301	13411667	DIODE,CHIP HRF22
D302,303	S0035214	DIODE,HVC376B-TRF
D304	13411667	DIODE,CHIP HRF22
D305	5228018100	C,VARI HVU17TR
D402	S0023224	DIODE,DAN217 T146
D501-503	13411667	DIODE,CHIP HRF22
D504	5228018100	C,VARI HVU17TR
D505	S0020814	ZENER DIODE,UDZ 5.1B
D506	S0025274	DIODE,RB706F-40
D507	5228018100	C,VARI HVU17TR
D601	S0023224	DIODE,DAN217 T146
D602,603	13411596	DIODE,IMN10
D604	S0025274	DIODE,RB706F-40
D605,606	13411596	DIODE,IMN10
D701-705	13411596	DIODE,IMN10
D706	S0025274	DIODE,RB706F-40
D707-711	13411596	DIODE,IMN10
D712	S0023224	DIODE,DAN217 T146
D713	S0025274	DIODE,RB706F-40
D714	13411596	DIODE,IMN10
D715	13411667	DIODE,CHIP HRF22
D716	S0025274	DIODE,RB706F-40
D717-723	13411596	DIODE,IMN10
D801	S0025274	DIODE,RB706F-40
D802	S0023224	DIODE,DAN217 T146
D803,804	S0025274	DIODE,RB706F-40
D901	S0025274	DIODE,RB706F-40
J701	E0032220	CONNECTOR,DSUB 25PIN
J702-704	E0032210	CONNECTOR,DSUB 15PIN
J801,901	E0032364	CONNECTOR,FMN 16BMT
L301	14728209	COIL,CHIP 47UH
L302,304	5286051500	COIL,CHIP 2.7UH K LK2125
L303	14728209	COIL,CHIP 47UH
L305,306	14728209	COIL,CHIP 47UH
L307	5286051300	COIL,CHIP 2.2UH K LK2125
L601-604	E0055364	COIL,CHIP 1000UH 5%
L801	E0031304	BEAD COIL,BLM21A601S
L802-805	E0055364	COIL,CHIP 1000UH 5%
P001-003	5336303400	PLUG,CONN. B4B-EH(WHT)
P401	5336249300	PLUG,CONN. B03B-PH-K-S(WHT)

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
P601	E0033020	CONNECTOR,PCN10MA-144P
P602	5336249900	PLUG,CONN. B09B-PH-K-S(WHT)
P901	5336249200	PLUG,CONN. B02B-PH-K-S(WHT)
Q403-406	13428287	TR,DTC124EKAT-146
Q407	S0019224	TR,DTC143XUA T106
Q601	S0019224	TR,DTC143XUA T106
Q604-607	13428287	TR,DTC124EKAT-146
Q701	S0019224	TR,DTC143XUA T106
Q801	S0019204	TR,2SC4081 T106R
R019	R0067304	RES ARRAY,1/16W 4X10K J
R039	R0067224	RES ARRAY,1/16W 4X4.7K J
R437-440	R0066374	VAR RES,EVM3VSX50B54
R601	R0092704	RES ARRAY,1/16W 4X47 J
R604	R0067304	RES ARRAY,1/16W 4X10K J
R606-609	R0092754	VAR RES,1KB RH03ADC
R622,623	R0092704	RES ARRAY,1/16W 4X47 J
R636	R0067304	RES ARRAY,1/16W 4X10K J
R637	R0092704	RES ARRAY,1/16W 4X47 J
R641-643	R0092704	RES ARRAY,1/16W 4X47 J
R644	R0067304	RES ARRAY,1/16W 4X10K J
R701,702	R0092714	RES ARRAY,1/16W 4X2.2K J
R706-709	R0092704	RES ARRAY,1/16W 4X47 J
R710,711	R0067224	RES ARRAY,1/16W 4X4.7K J
R727	R0067304	RES ARRAY,1/16W 4X10K J
R728	R0092704	RES ARRAY,1/16W 4X47 J
R731,732	R0092704	RES ARRAY,1/16W 4X47 J
R903	R0092704	RES ARRAY,1/16W 4X47 J
R911	R0092704	RES ARRAY,1/16W 4X47 J
R916	R0067304	RES ARRAY,1/16W 4X10K J
S001	E0031074	SW,SLIDE CHS-04TA
U001	S0024314	IC,TC74VHCT00F(EL)
U002	13444685	IC,74HC 574F
U003	S0025594	IC,TC74VHC163FEL
U004	S0018944	IC,TC74VHCU04F(EL)
U005	S0035143	IC,XCS10-3TQ144C
U007	5220118000	IC,TC74HC32AF-TP2
U008	5220103800	IC,TC74HC157AF-TP2
U009	S00396800B	IC,SX28AC SC2
U010	S0024464	IC,M62001FP-600D
U011	S00396700A	IC,SYS V1.00 MBM29F800BA-70PF
U011	E0033093	SOCKET,44PIN SOP IC179
U012	S0035133	IC,HD6437043AE00F
U013	S00351700C	IC,SA28AC/SS TC
U014,015	S0037443	IC,BS62LV1024TC-70
U016	S00397100A	IC,SX28AC TCR
U017	13444685	IC,74HC 574F
U018	5220116400	IC,HD74HC138FP
U019	S0025614	IC,TC74VHCT541AFEL
U101	S0020334	IC,TC74VHC04
U102	5220118000	IC,TC74HC32AF-TP2

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
U103	E0013344	CRYSTAL OSC,22.5792MHZ
U104	E00546900A	CRYSTAL OSC,49.152MHZ
U105	S0020354	IC,TC74VHC74
U106	S00177600A	IC,CLK1
U107,108	5220104000	IC,TC74HC595AF-TP2
U109	S00190600A	IC,IOX
U110	S0024353	IC,DSP TMS57070FFT
U111	S0036203	IC,T2316162A-45S
U112	S0020344	IC,TC74VHC541
U201,202	S0035714	IC,BA033FP
U203,204	S0025614	IC,TC74VHCT541AFEL
U205	S00335600A	IC,DTRS-HR DEC
U206	S00335500A	IC,DTRS-HR ENC
U207-211	S0035204	IC,71V124SA15PH-T&R
U301	S0018944	IC,TC74VHCU04F(EL)
U302	13447922	IC,NJM78L05UA-TE1
U303	5220123500	IC,MC74HC4046AF-FR1
U304	S0018944	IC,TC74VHCU04F(EL)
U305	5220123500	IC,MC74HC4046AF-FR1
U306	13447922	IC,NJM78L05UA-TE1
U307	S0029674	IC,TLC2932IPWR
U308,309	S0020354	IC,TC74VHC74
U310	S0018944	IC,TC74VHCU04F(EL)
U311	S0029674	IC,TLC2932IPWR
U401,402	S0035274	IC,MAX913CSA
U403,404	5220101800	IC,HD49229
U406	E0042034	RELAY,ATX206SA 2C,SMT
U407-409	5292811400	EMI FILTER,CHIP 10000PFT
U410	S0024314	IC,TC74VHCT00F(EL)
U501	13447922	IC,NJM78L05UA-TE1
U502	S0020064	IC,MC74HC4538AF LEFT
U503	S0024284	IC,NJM 78L09UA-TE1
U504	S0024294	IC,NJM 79L09UA-TE1
U505	S0024304	IC,NJU201AM-TE2
U506	S0018944	IC,TC74VHCU04F(EL)

SYS PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
U507	S0032804	IC,NJM082BV(TE1)
U508	S0004244	IC,LF356MX
U601-605	S0020344	IC,TC74VHC541
U606	S0024314	IC,TC74VHCT00F(EL)
U607-610	S0025614	IC,TC74VHCT541AFEL
U611	S0019594	IC,TC74VHC08F(EL)
U612	E0042034	RELAY,ATX206SA 2C,SMT
U613	S0025614	IC,TC74VHCT541AFEL
U614	S0019594	IC,TC74VHC08F(EL)
U701	5220116700	IC,HD74HC240FP
U702	S0037124	IC,TC74LCX541F(EL)
U703	E0042034	RELAY,ATX206SA 2C,SMT
U704	5220115800	IC,MC74HC14AF
U705	S0026540	IC,M5M34051FP
U706	5220103800	IC,TC74HC157AF-TP2
U707	S0026540	IC,M5M34051FP
U801	S0026540	IC,M5M34051FP
U802	S0020064	IC,MC74HC4538AF LEFT
U803	S0020354	IC,TC74VHC74
U804	S0024314	IC,TC74VHCT00F(EL)
U805	S0018944	IC,TC74VHCU04F(EL)
U806	13448089	IC,LM1881M
U807	5220102000	IC,SN74S140NS
U808	5220120700	IC,HD74HC153FPEL
U809,810	S0023994	IC,NJM4565M-T1
U901	S0025614	IC,TC74VHCT541AFEL
U902	S0036964	IC,LC89051V
U903	S0025614	IC,TC74VHCT541AFEL
U904	S0036913	IC,XCS20XL-4VQ100C
X001	E00547000A	RESONATOR,SD3 32MHZ
X501	E00331100B	RESONATOR,9.60MHZ SMT
X502	E00331000B	RESONATOR,8.82MHZ SMT

KEY PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
	*E95103000A	PCB ASSY,KEY
	*E90103000B	PCB,KEY
	E0054840	LCD,MC2004E-SYL-2
	M01077400A	COLLAR,LCD DA-98HR
	E00351400A	HARNESS ASSY,FRONT DA98
	E00620000A	HARNESS ASSY,FRONTJOG98HR
D1-55	S0022094	DIODE,1SS355
D57-64	M00572500A	LED ASSY,BAR METER 15DOT
D65	S0038240	LED,LT3ED87
D65A	M00608702A	SPACER,LH-5 L=10
D67	S0038240	LED,LT3ED87
D67A	M00608702A	SPACER,LH-5 L=10
D69	S0038240	LED,LT3ED87
D69A	M00608702A	SPACER,LH-5 L=10
D71	S0038240	LED,LT3ED87
D71A	M00608702A	SPACER,LH-5 L=10
D73	S0038240	LED,LT3ED87
D73A	M00608702A	SPACER,LH-5 L=10
D75	S0038240	LED,LT3ED87
D75A	M00608702A	SPACER,LH-5 L=10
D77	S0038240	LED,LT3ED87
D77A	M00608702A	SPACER,LH-5 L=10
D79	S0038240	LED,LT3ED87
D79A	M00608702A	SPACER,LH-5 L=10
D81-93	5225018500	LED,SLR-34DU3F
D81A-93A	5801550400	SPACER,LH-5 L=14.0
D100	5225013500	LED,SLR-34VR3F (RED)
D100A	5801550400	SPACER,LH-5 L=14.0
D125-130	5225018500	LED,SLR-34DU3F
D131	5225013600	LED,SLR-34MG3F (GRN)
D132-134	5225018500	LED,SLR-34DU3F
D135	5225013600	LED,SLR-34MG3F (GRN)
D136-139	5225018500	LED,SLR-34DU3F
D125A-136A	M00608702A	SPACER,LH-5 L=10
D137A-139A	5801550400	SPACER,LH-5 L=14.0
D140	5225013600	LED,SLR-34MG3F (GRN)
D140A	5801550400	SPACER,LH-5 L=14.0
D141	5225013600	LED,SLR-34MG3F (GRN)
D141A	5801550400	SPACER,LH-5 L=14.0
D142	5225013500	LED,SLR-34VR3F (RED)

KEY PCB ASSY

REF.NO.	PARTS NO.	DESCRIPTION
D142A	5801550400	SPACER,LH-5 L=14.0
D143,144	5225018500	LED,SLR-34DU3F
D143A,144A	M00608702A	SPACER,LH-5 L=10
D145	S0038240	LED,LT3ED87
D145A	5801550400	SPACER,LH-5 L=14.0
D147	S0038240	LED,LT3ED87
D147A	5801550400	SPACER,LH-5 L=14.0
D149	S0038240	LED,LT3ED87
D149A	5801550400	SPACER,LH-5 L=14.0
P1,2	5336370000	PLUG.CONN. 8P BTK-2S-H
P3	5336288000	PLUG,CONN. S10B-PH-K-S(WHT)
P4	5336242600	PLUG,CONN. B16B-PH-K-S
P5	5336370000	PLUG,CONN. 8P BTK-2S-H
Q1	S0001054	TR,2SD1757K
Q2-6	S0001664	TR,DTC114TU-106
S1	E0000460	ENCODER,SRGPHJ
S2	E0057520	SW,LC1B-L1R-1400-11
S3	5300059900	SW,PUSH (LED GRN) PLAY
S4	5300059800	SW,PUSH (LED WHT) STOP
S5,6	E00412700A	SW,LC1B-L1W-1400-12-FF
S7-56	E0021092	SW,SKHVBH
TP5	13122939	CONN.,2P IMSA-9210B-1-02-T
U1	S0024873	IC,UPD784031GC-8BT
U2	S0022434	IC,M51957AFP-600C
U4	S0028234	IC,HD74LVC541A TSSOP
U5	13445670	IC,HD74HC573F
U6	S00384100A	IC,FRONT V1.00 M27C512-12C1
U6A	E0003273	SOCKET,IC160-0324-240*
U7	5220093300	IC,TC74HC00AF-TP2
U8	5220115800	IC,MC74HC14AF
U9-11	S0029394	IC,SN74LV138ANST-EL
U13-15	S0033394	IC,TD62M8600F-EL
U17,18	S0035690	IC,TB62701AN
X1	E0060344	RESONATOR,29.4912MHZ

IF98AD PCB ASSY (IF-AN98HR)

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106500A	PCB ASSY,IF98AD
	*E90106500A	PCB,IF98AD
	*M00319700A	WASHER,ADHESIVE 5X12X0.1T
	*5730042700	HEAT SINK,OSH-2025-SPL
	*M00617300B	REAR PANEL,AD
	*5780003006	SCREW,BIND M3X6
	*5801536400	SCREW,DSUB LOCK M2.6X0.45
	*5780023006	SCREW,BIND M3X6 (BLK NI)
D010-018	13411644	DIODE,CHIP 1SS355 TE-17
D020-028	13411644	DIODE,CHIP 1SS355 TE-17
D030-038	13411644	DIODE,CHIP 1SS355 TE-17
D041-048	13411644	DIODE,CHIP 1SS355 TE-17
D060	S0035214	DIODE,HVC376B-TRF
D070	13411644	DIODE,CHIP 1SS355 TE-17
J010	E0032220	CONNECTOR,DSUB 25PIN
L010	E0054724	COIL,LQH3C100K24
L011-018	E0054804	BEAD COIL,BLM21B121SDPT
L020	E0054724	COIL,LQH3C100K24
L021-028	E0054804	BEAD COIL,BLM21B121SDPT
L030	E0054724	COIL,LQH3C100K24
L040	5286051500	COIL,CHIP 2.7UH K LK2125
L501-504	E0054724	COIL,LQH3C100K24
P010	5334079300	PLUG,CONN. 100P
P020	5336303400	PLUG,CONN. B4B-EH (WHT)
R370	11985206	R,ARRAY CHIP 4X10K J
U010	S00396900C	IC,SX28AC AIO
U011-018	5220450400	IC,NJM5532M-T2
U020,030	13444677	IC,74HC541F
U050,060	13447952	IC,NJM7805FA
U070	13447952	IC,NJM7805FA
U080	5220123500	IC,MC74HC4046AF-FR1
U090	E00581800A	RESONATOR,COC22AT24.57MHZ
U100	E00581900A	RESONATOR,COC22AT22.57MHZ
U110	S0018944	IC,TC74VHCU04F(EL)
U120	S0022470	IC,TC74VHC00F
U130,140	S0025594	IC,TC74VHC163FEL
U150	S0020354	IC,TC74VHC74
U160,170	S0019610	IC,TC74VHC153F
U180	13445582	IC HD74HC4538FP
U190	S0024464	IC,M62001FP-600D
U200	S0022470	IC,TC74VHC00F
U501-504	S0035284	IC,AK5393

IF98DA PCB ASSY (IF-AN98HR)

REF.NO.	PARTS NO.	DESCRIPTION
	*E95106600A	PCB ASSY,IF98DA
	*E90106600A	PCB,IF98DA
	*5730042700	HEAT SINK,OSH-2025-SPL
	*M00617301B	REAR PANEL,DA
	*5780003006	SCREW,BIND M3X6
	*5801536400	SCREW,DSUB LOCK M2.6X0.45
	*5780023006	SCREW,BIND M3X6 (BLK NI)
D010	13411644	DIODE,CHIP 1SS355 TE-17
D020	13411644	DIODE,CHIP 1SS355 TE-17
D030	13411644	DIODE,CHIP 1SS355 TE-17
D060	S0035214	DIODE,HVC376B-TRF
D070	13411644	DIODE,CHIP 1SS355 TE-17
D501-504	13411644	DIODE,CHIP 1SS355 TE-17
J010	E0032220	CONNECTOR,DSUB 25PIN
L010	E0054724	COIL,LQH3C100K24
L011-018	E0054804	BEAD COIL,BLM21B121SDPT
L020	E0054724	COIL,LQH3C100K24
L021-028	E0054804	BEAD COIL,BLM21B121SDPT
L030	E0054724	COIL,LQH3C100K24
L040	5286051500	COIL,CHIP 2.7UH K LK2125
P010	5334079300	PLUG,CONN. 100P
P020	5336303400	PLUG,CONN. B4B-EH (WHT)
Q011-018	S0016434	TR,2SD1328T/S
Q021-028	13428276	TR,DTA114EKAT-146
Q031-038	13428286	TR,DTC114EKAT-146
Q501-504	S0019224	TR,DTC143XUA T106
R360,370	11985206	R,ARRAY CHIP 4X10K J
U010	S00396900C	IC,SX28AC AIO
U011	5220450400	IC,NJM5532M-T2
U013	5220450400	IC,NJM5532M-T2
U015	5220450400	IC,NJM5532M-T2
U017	5220450400	IC,NJM5532M-T2
U020	13444677	IC 74HC 541F
U021-028	5220450400	IC,NJM5532M-T2
U030	13444677	IC 74HC 541F
U031-038	5220450400	IC,NJM5532M-T2
U040	5220118000	IC,TC74HC32AF-TP2
U050,060	13447952	IC,NJM7805FA
U070	13447952	IC,NJM7805FA
U080	5220123500	IC,MC74HC4046AF-FR1
U090	E00581800A	RESONATOR,COC22AT24.57MHZ
U100	E00581900A	RESONATOR,COC22AT22.57MHZ
U110	S0018944	IC,TC74VHCU04F(EL)
U120	S0022470	IC,TC74VHC00F
U130,140	S0025594	IC,TC74VHC163FEL
U150	S0020354	IC,TC74VHC74
U160,170	S0019610	IC,TC74VHC153F
U180	13445582	IC HD74HC4538FP
U190	S0024464	IC,M62001FP-600D
U200	S0022470	IC,TC74VHC00F
U501-504	S0035234	IC,AK4393
U511-514	5220450400	IC,NJM5532M-T2
U521-524	E0058404	RELAY,ATX203SA(12V)

8. INCLUDED ACCESSORIES
付属品

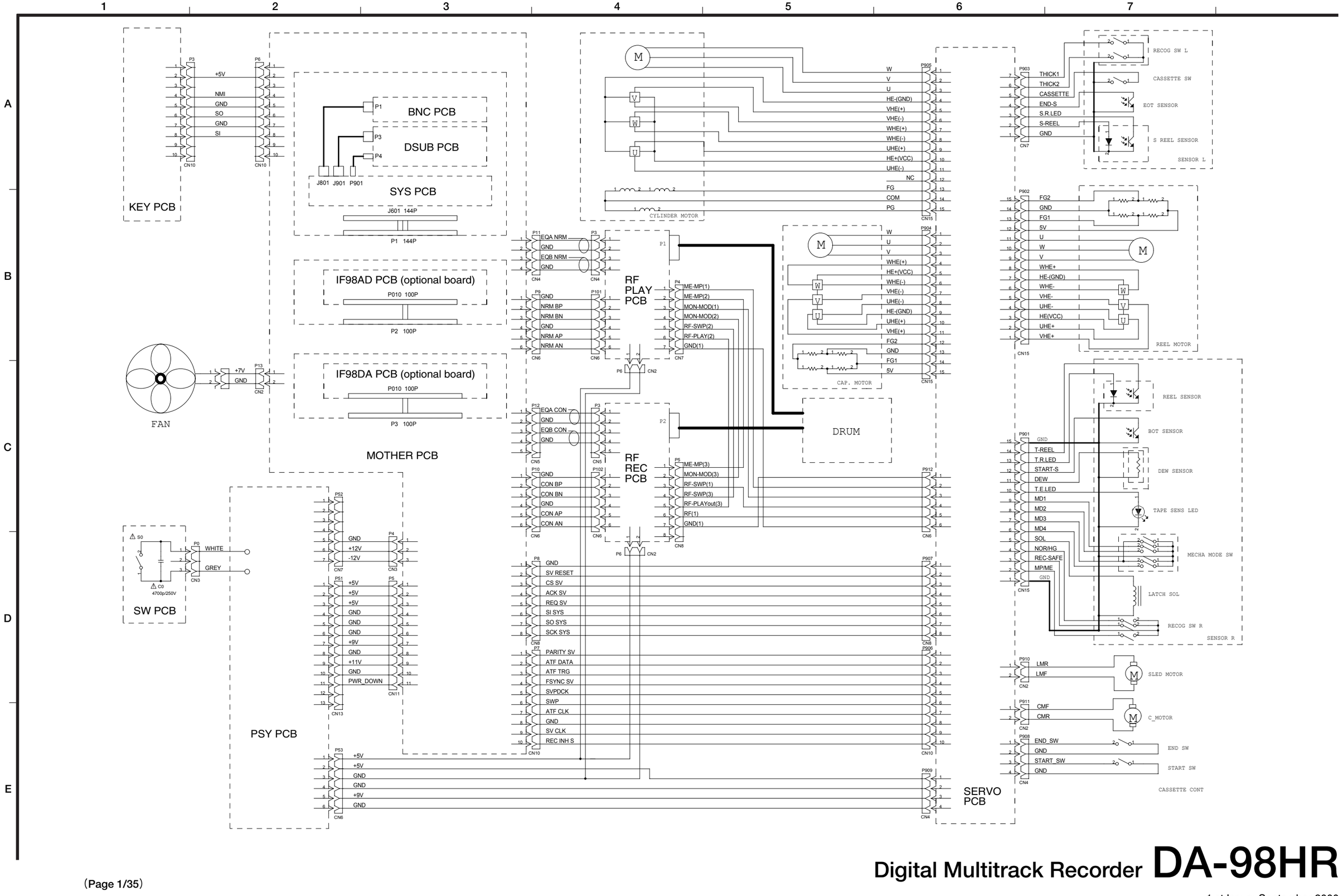
INCLUDED ACCESSORIES (DA-98HR)

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	*D00539500A	OWNER'S MANUAL,JAPANESE [J]	
	*D00539600A	OWNER'S MANUAL,ENGLISH [EXCEPT J]	
	*D00563400A	OUTLINE MANUAL,ENGLISH [EXCEPT J]	
	*T00030500A	CLEANING TAPE,HC-8	
	5740004100	MOUNT SCREW KIT,DX-2D	
	5350014400	AC CORD ASSY [J]	
	5350018800	AC CORD SET,W/PLUG [US/C]	
	15922303	3-WIRED CORD SET [E,K]	
	5350018500	3-WIRED CORD SET (13A FUSE) [UK]	
	5350018600	3-WIRED CORD SET [A]	
	5347009000	ADAPTOR,KPR-18 [J]	

INCLUDED ACCESSORIES (IF-AN98HR)

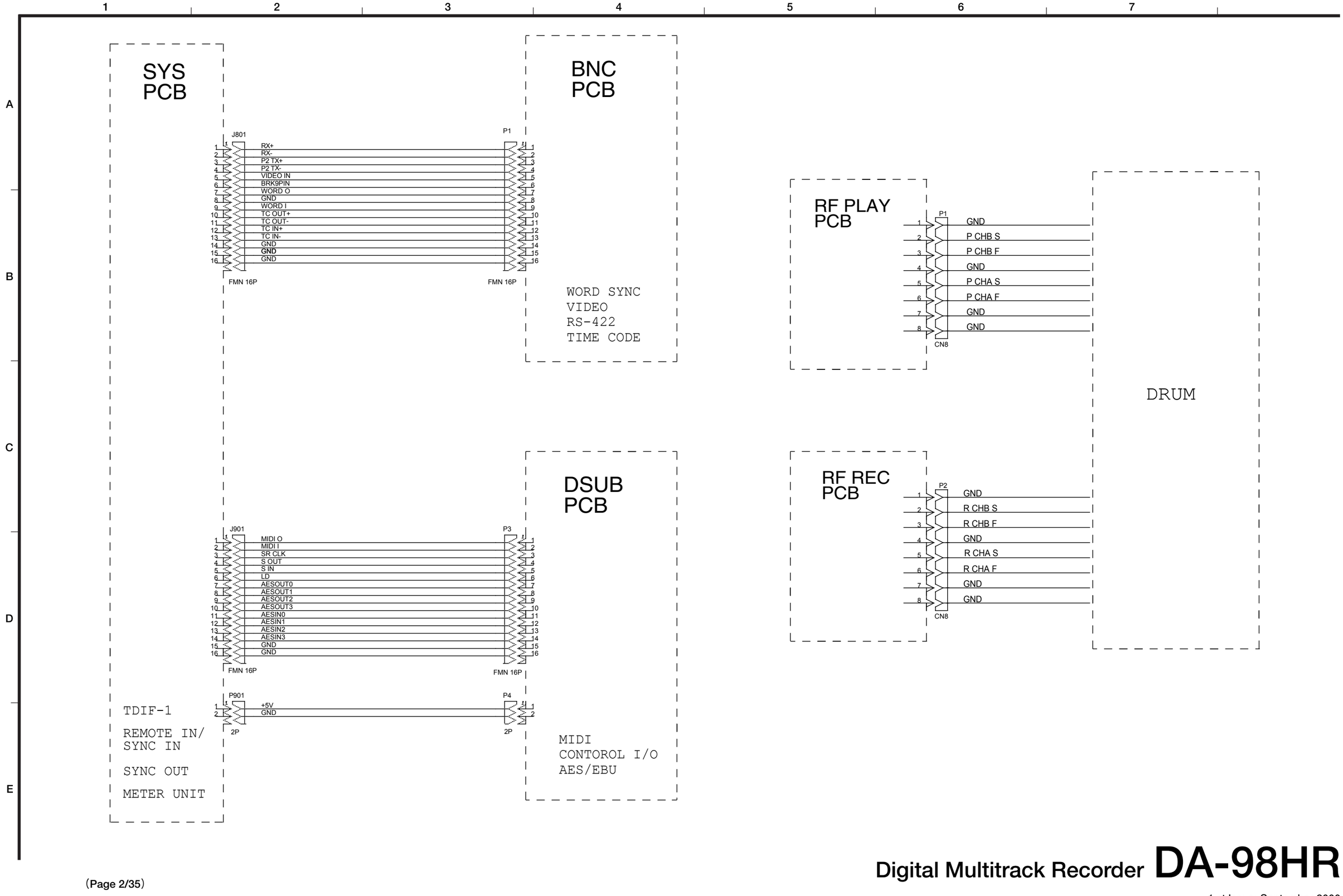
REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	*D00562700A	OWNER'S MANUAL,JAPANESE IF-AN98HR [J]	
	*D00562800A	OWNER'S MANUAL,ENGLISH IF-AN98HR [EXCEPT J]	

SCHEMATIC DIAGRAM DA-98HR WIRING (1/2)

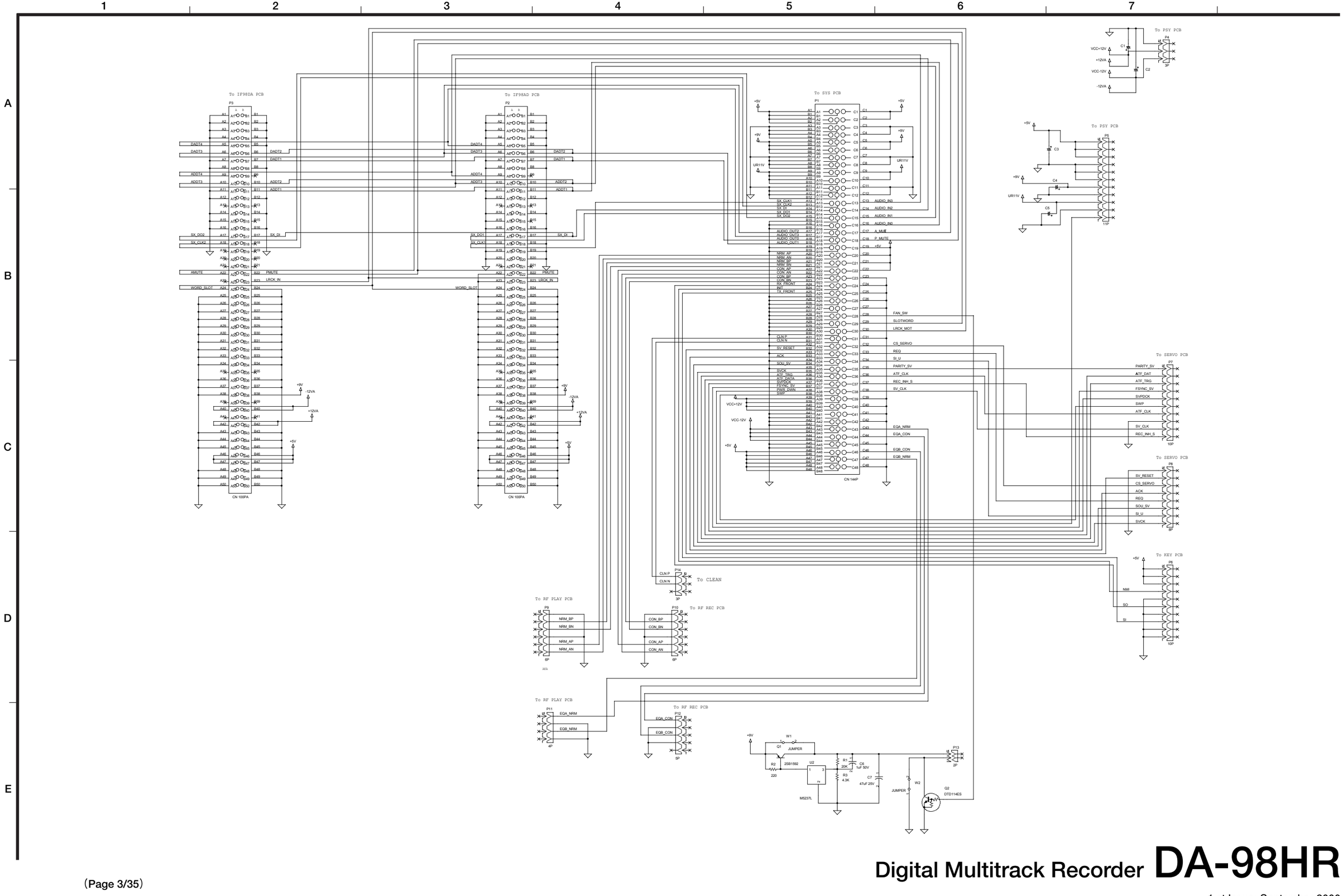


Digital Multitrack Recorder **DA-98HR**

1 st Issue; September 2000



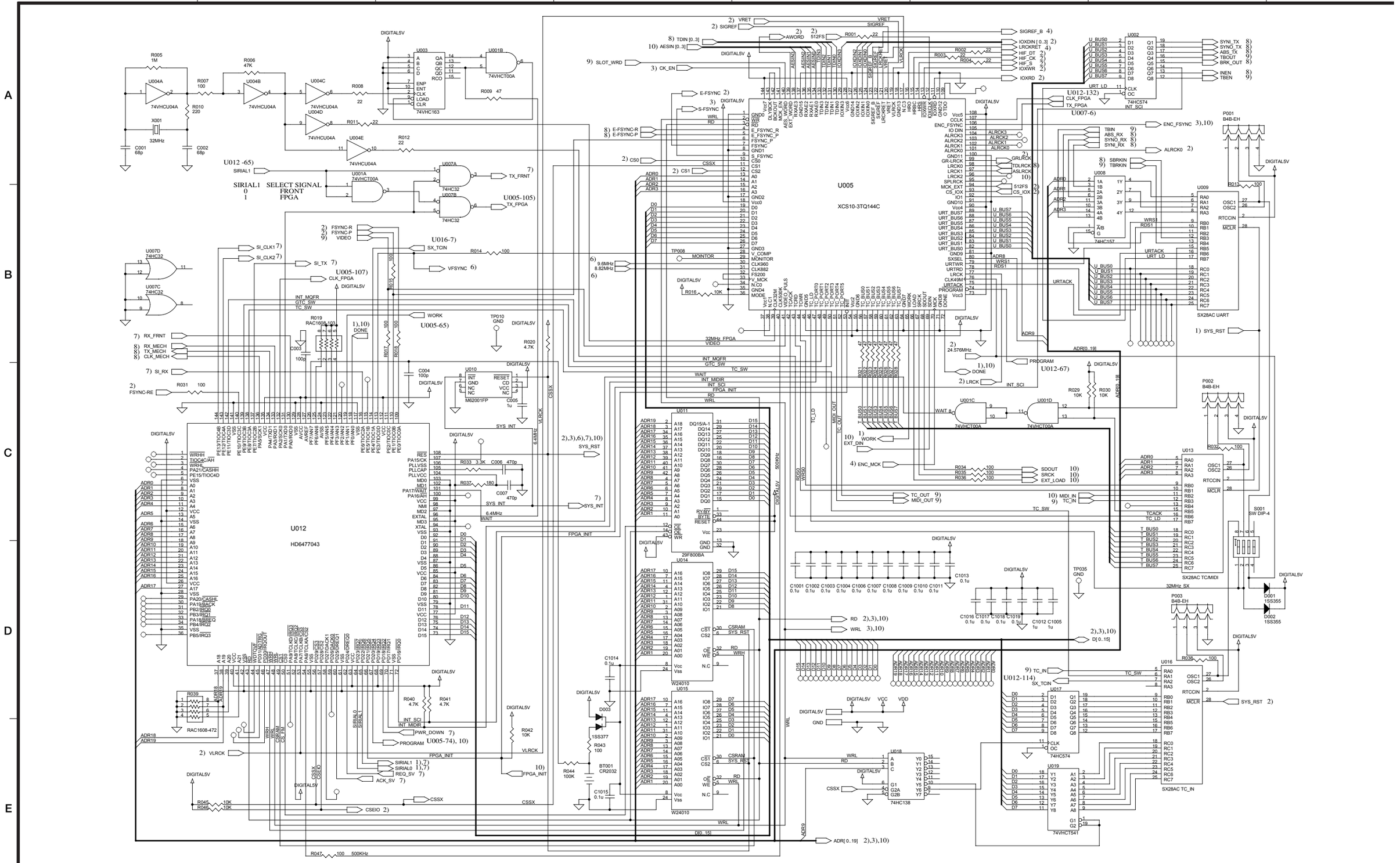
Digital Multitrack Recorder DA-98HR
1 st Issue; September 2000



Digital Multitrack Recorder **DA-98HR**

1 st Issue; September 2000

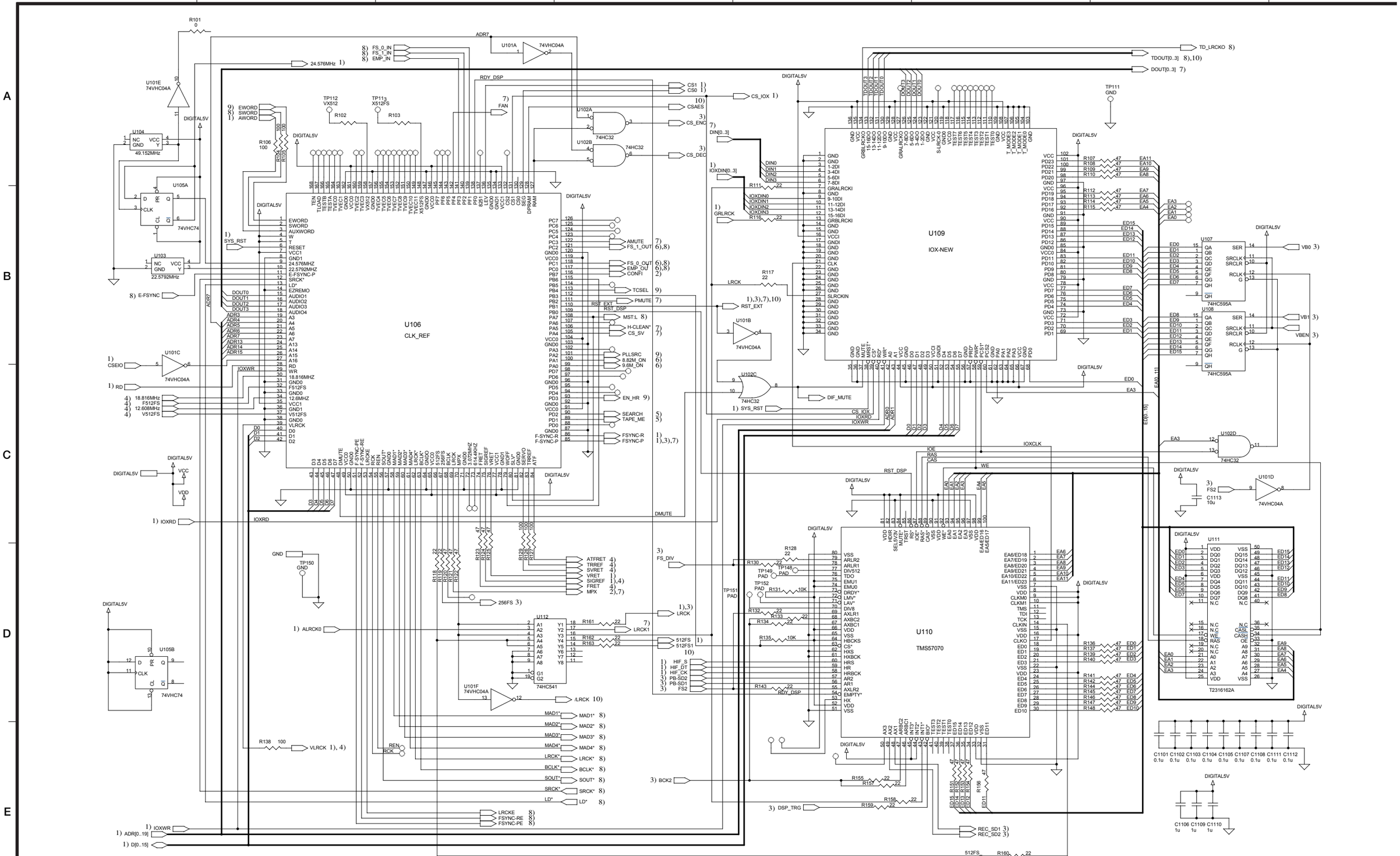
SCHEMATIC DIAGRAM DA-98HR SYS PCB (1/10)



Digital Multitrack Recorder DA-98HR

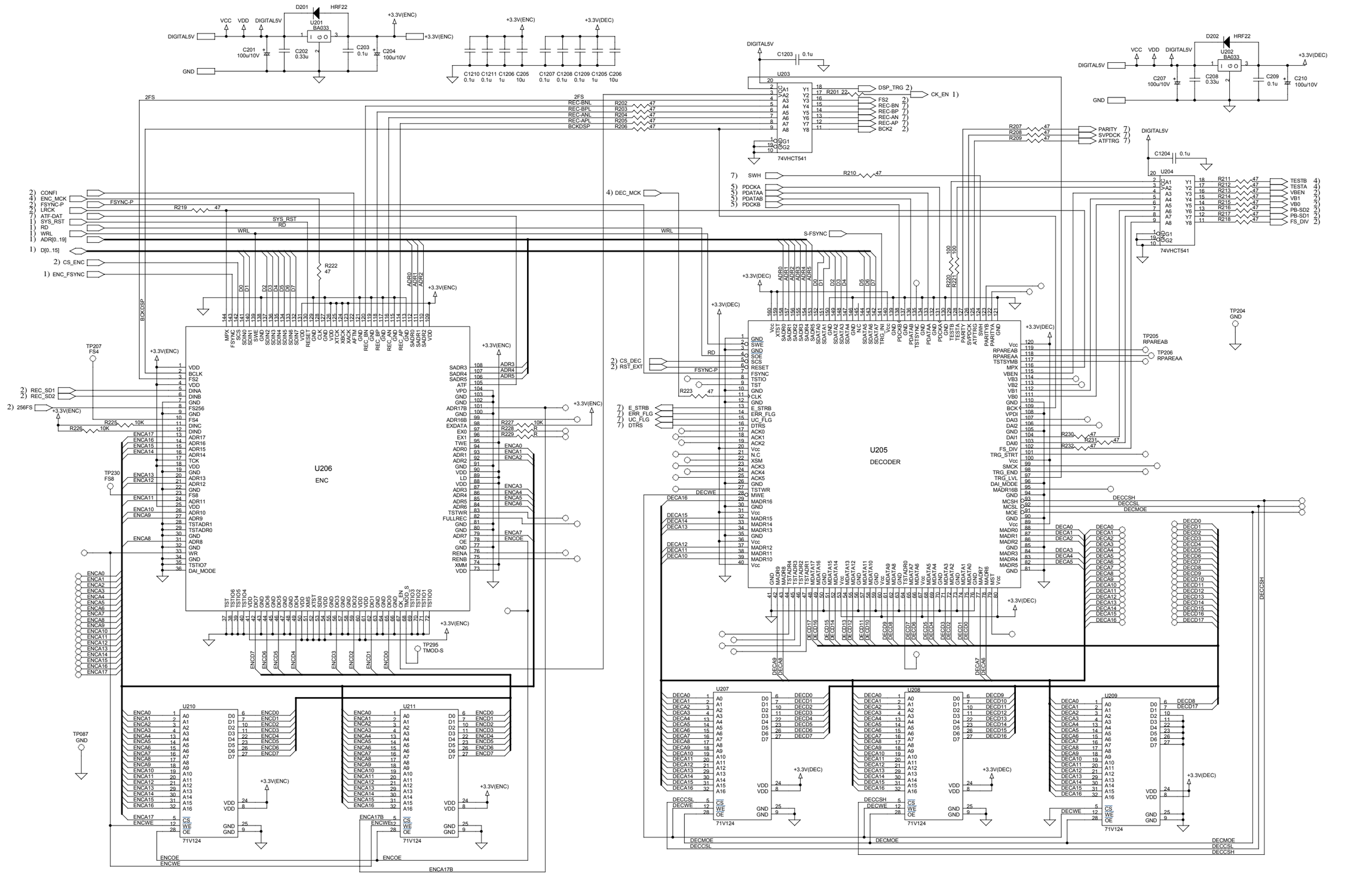
1 st Issue; September 2000

SCHEMATIC DIAGRAM DA-98HR SYS PCB (2/10)



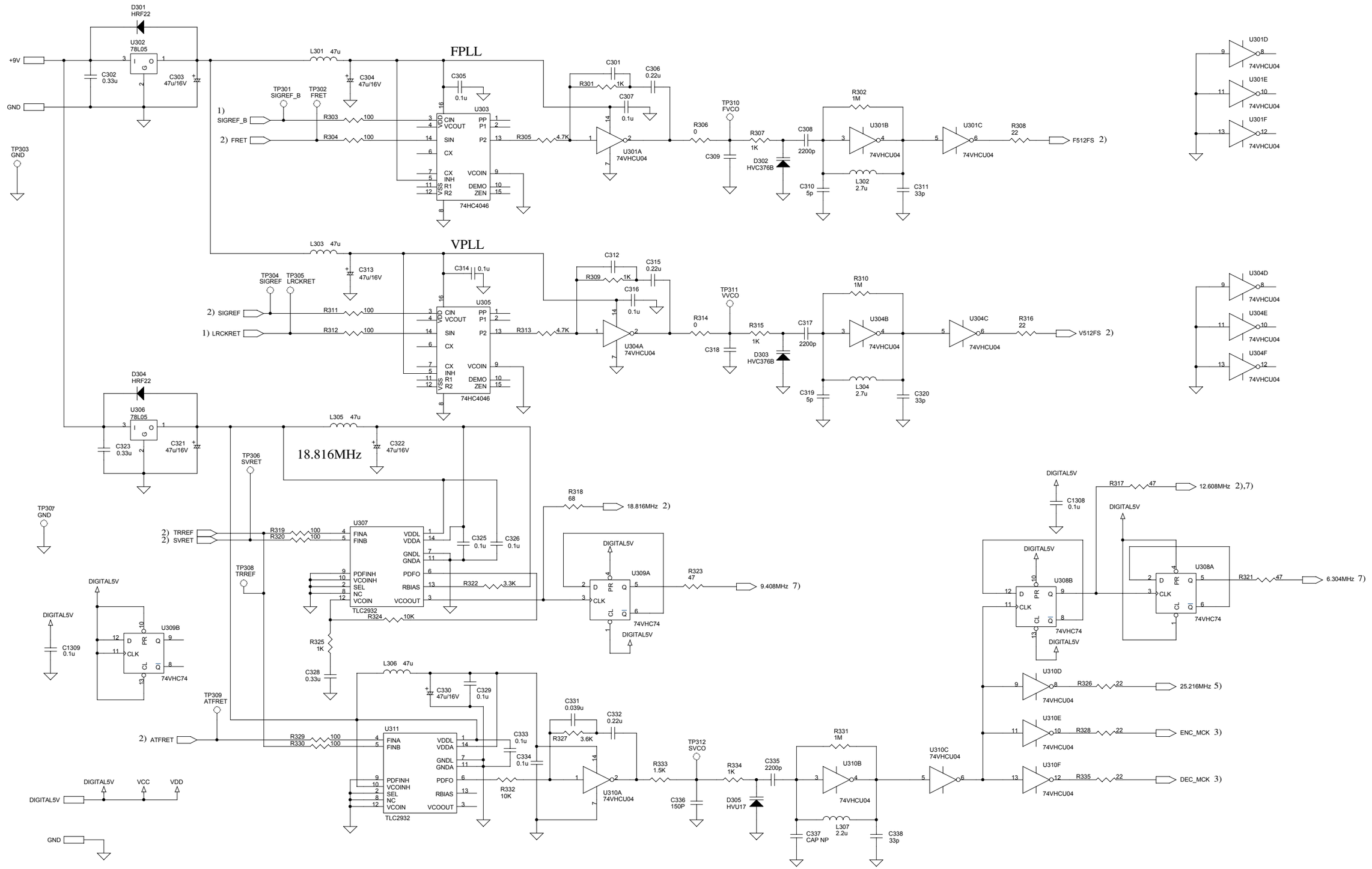
Digital Multitrack Recorder **DA-98HR**

1 st Issue; September 2000



Digital Multitrack Recorder DA-98HR

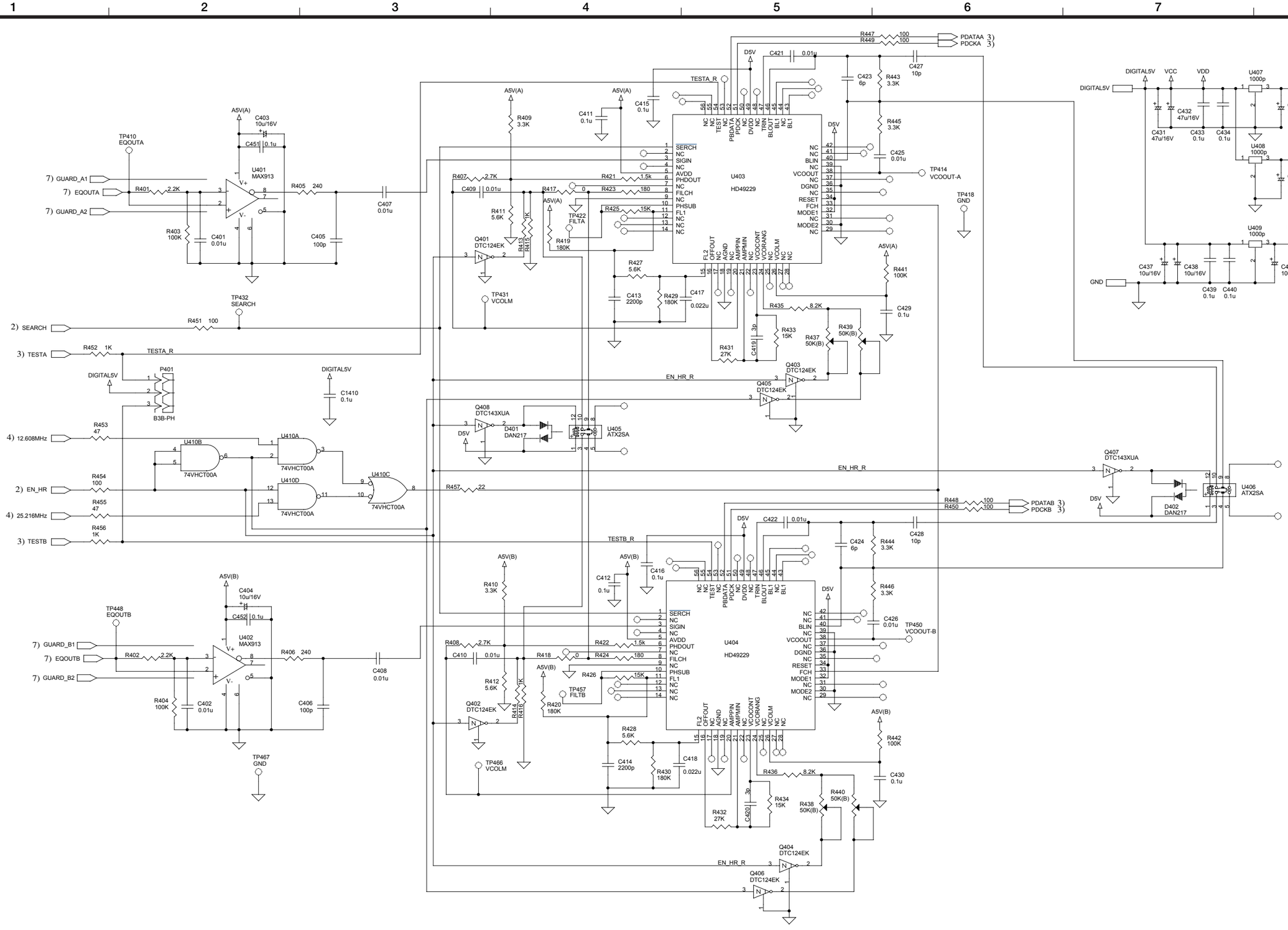
1 st Issue; September 2000



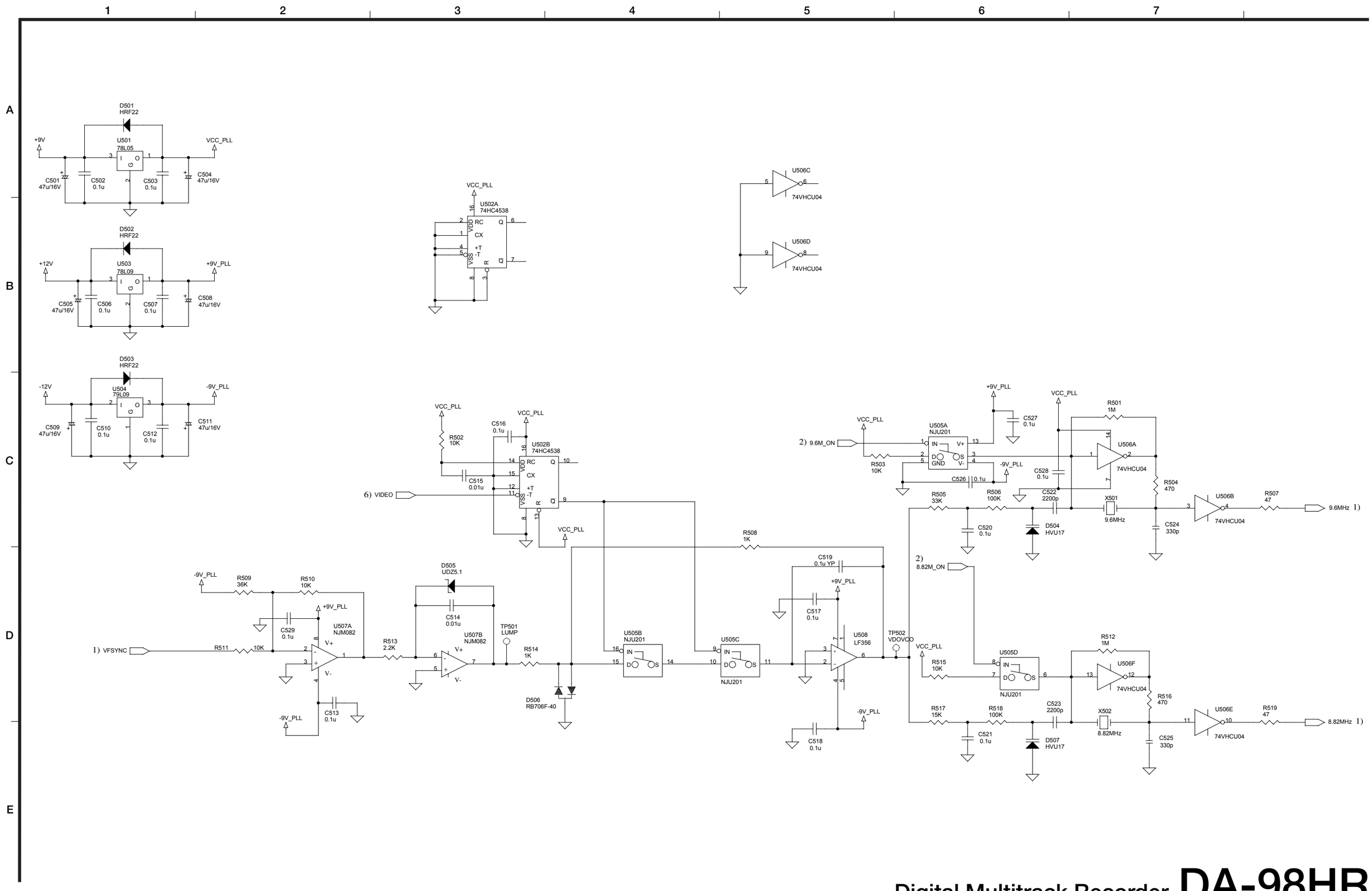
Digital Multitrack Recorder **DA-98HR**

1 st Issue; September 2000

SCHEMATIC DIAGRAM DA-98HR SYS PCB (5/10)

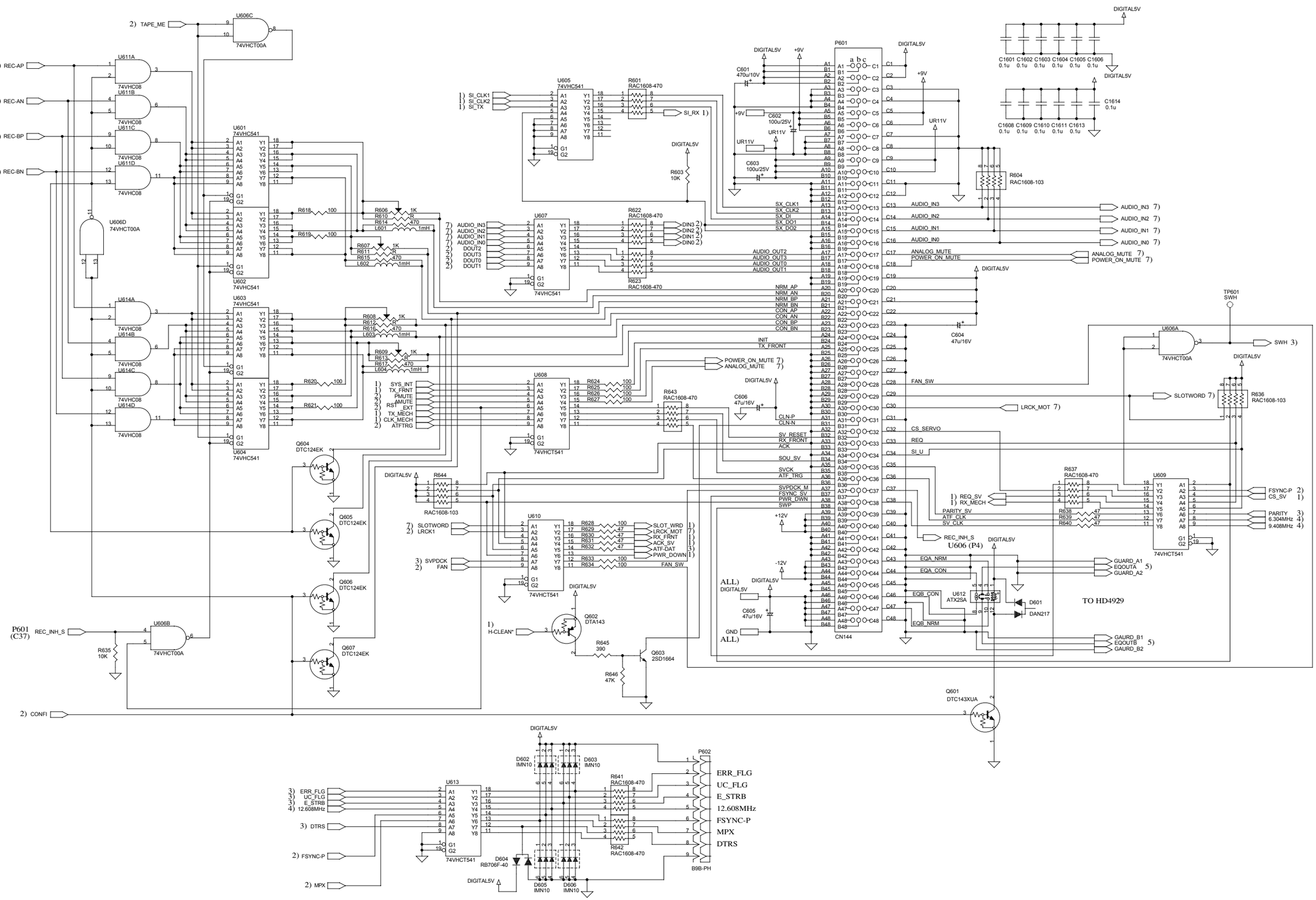


Digital Multitrack Recorder DA-98HR
1 st Issue; September 2000



Digital Multitrack Recorder **DA-98HR**

1 st Issue; September 2000



Digital Multitrack Recorder DA-98HR

1 st Issue; September 2000

TDIF

SYNC IN

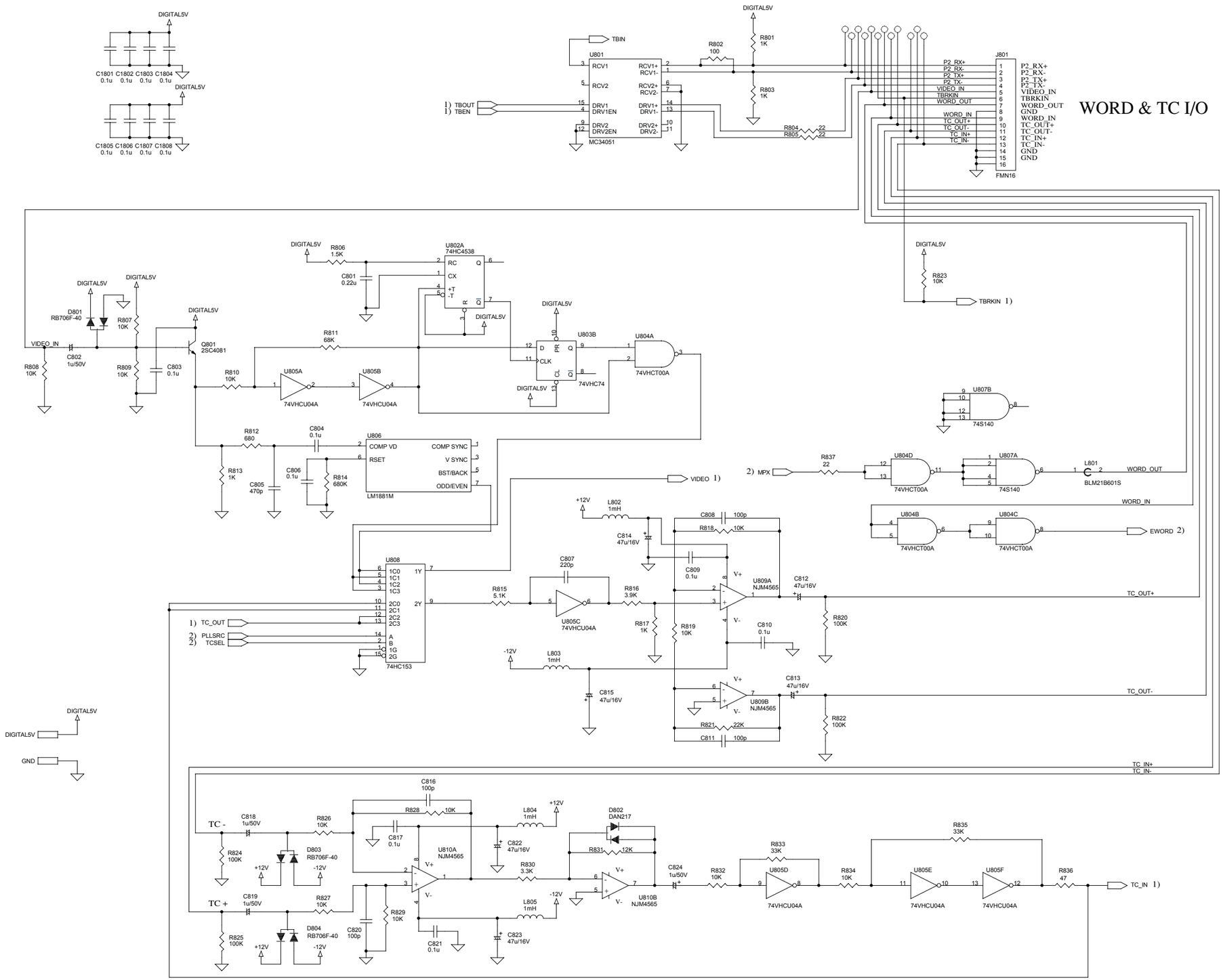
SYNC OUT

MU-8824

1 2 3 4 5 6 7

A B C D E

WORD & TC I/O



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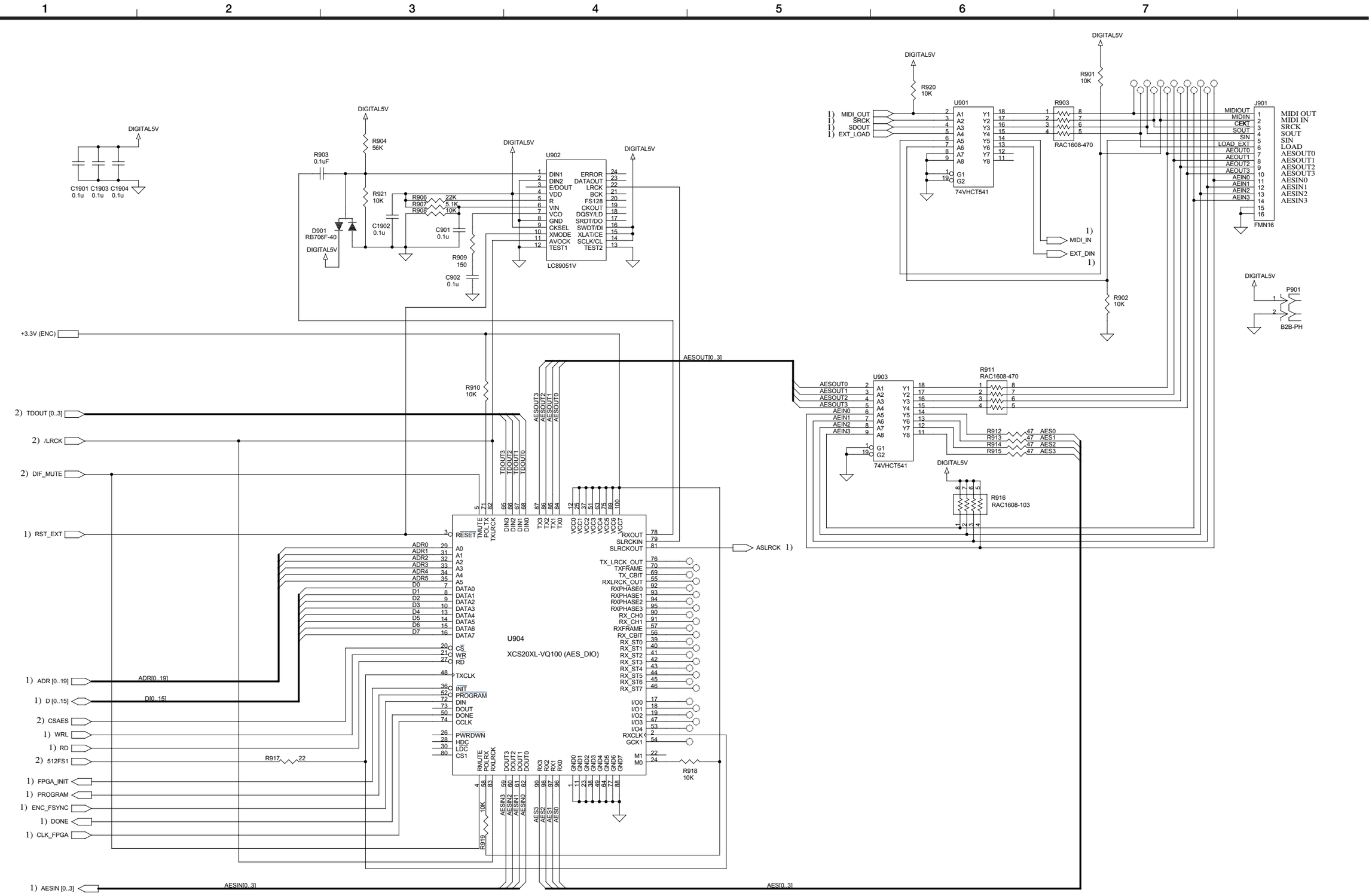
1 st Issue; September 2000



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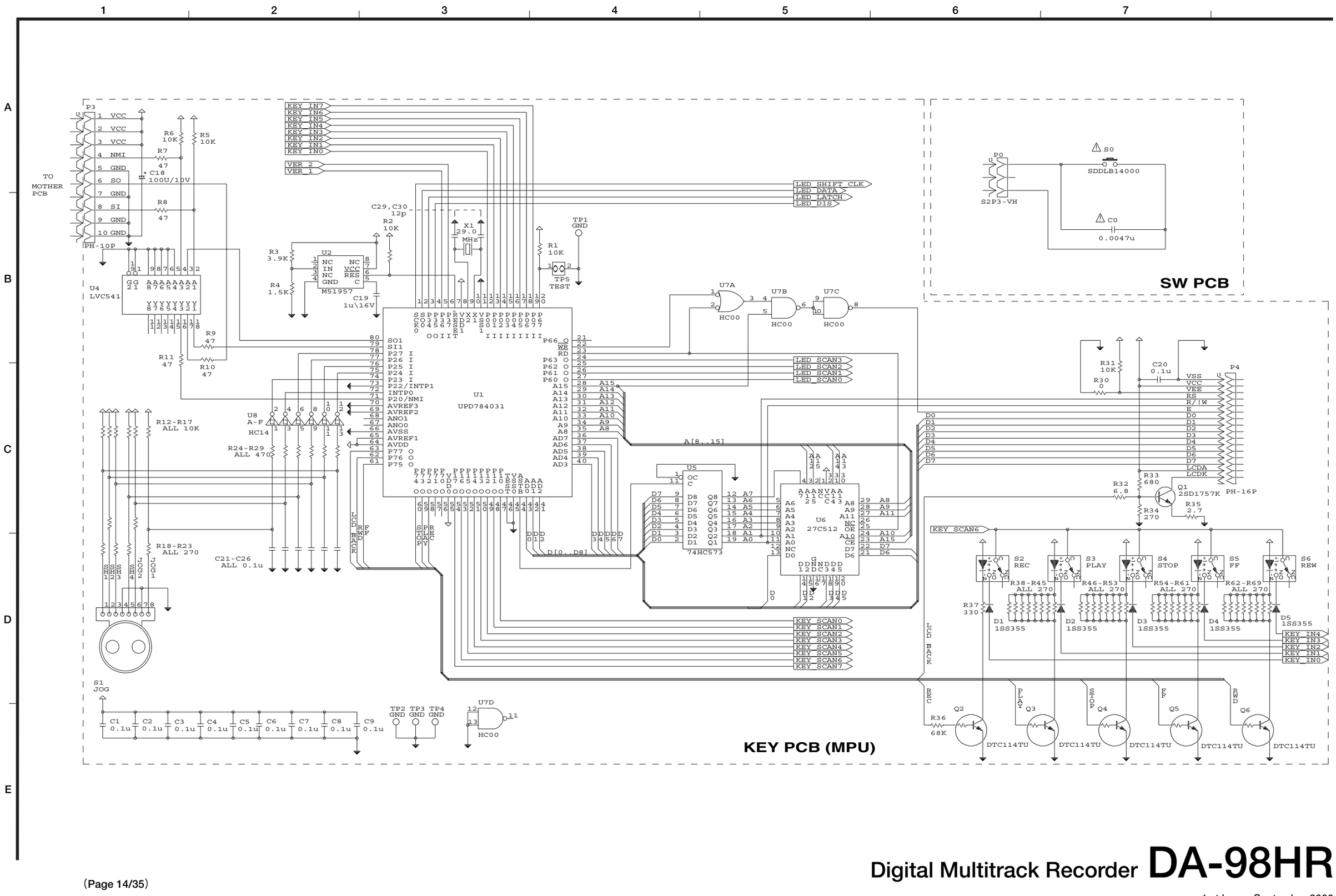
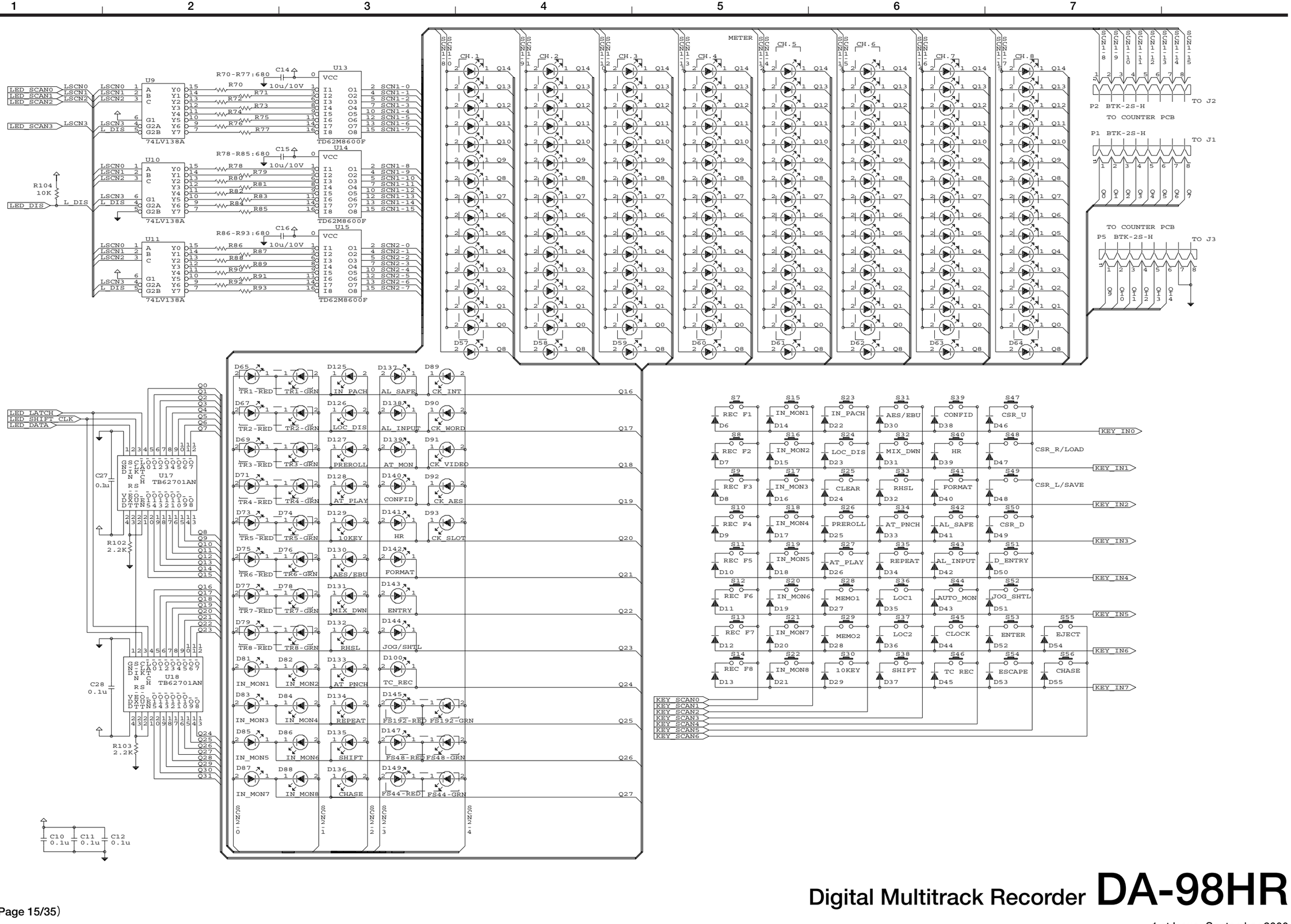
1 st Issue; September 2000



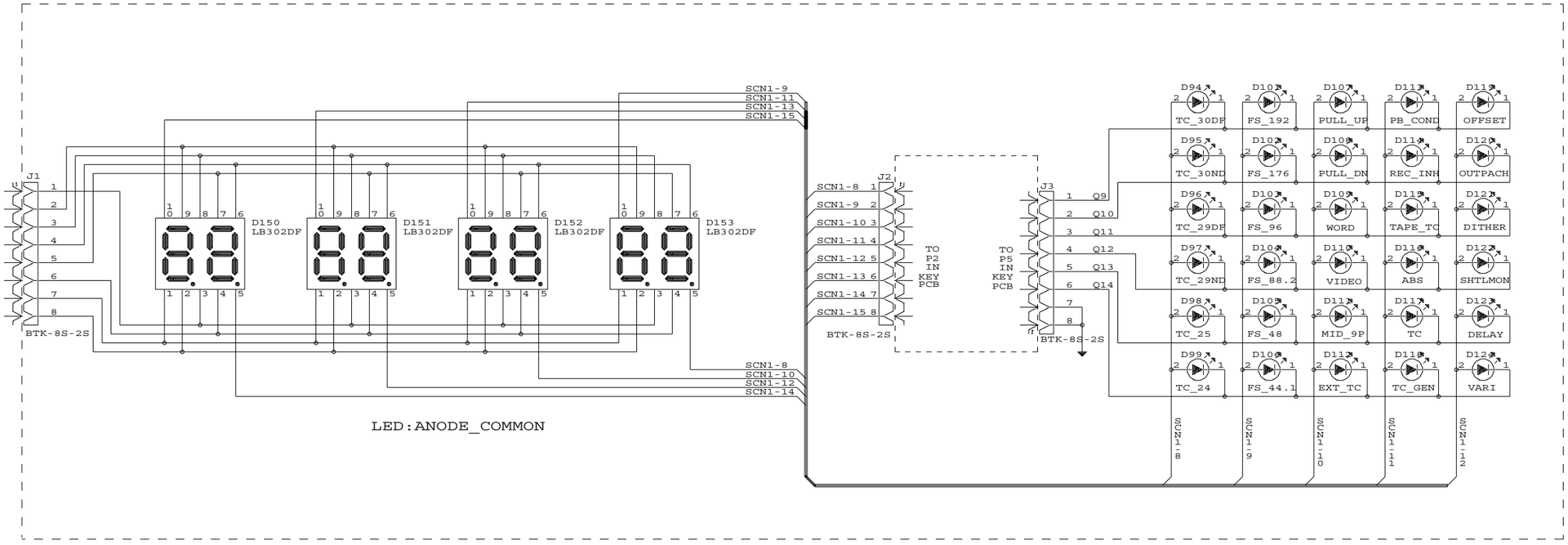
Digital Multitrack Recorder **DA-98HR**

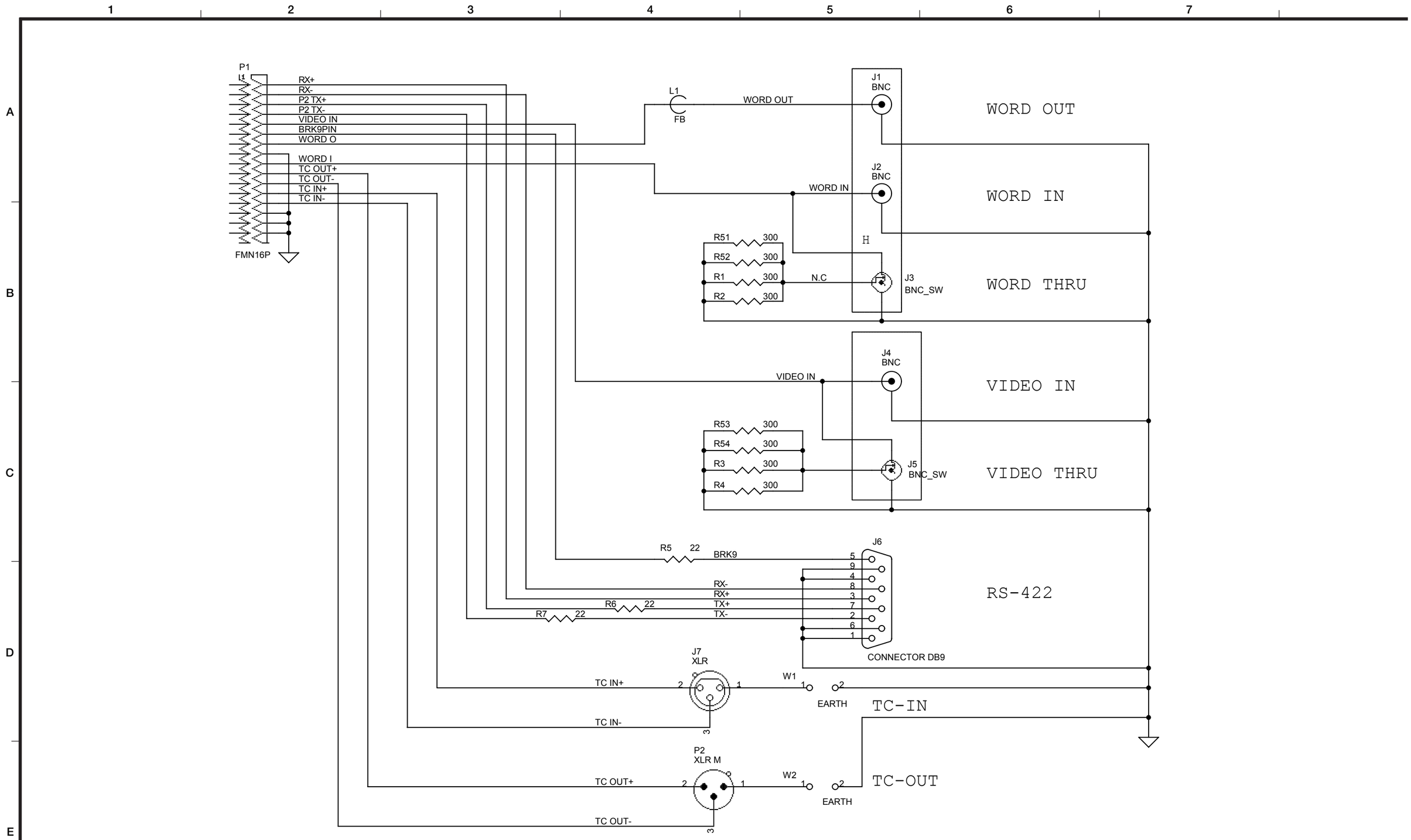
1 st Issue; September 2000

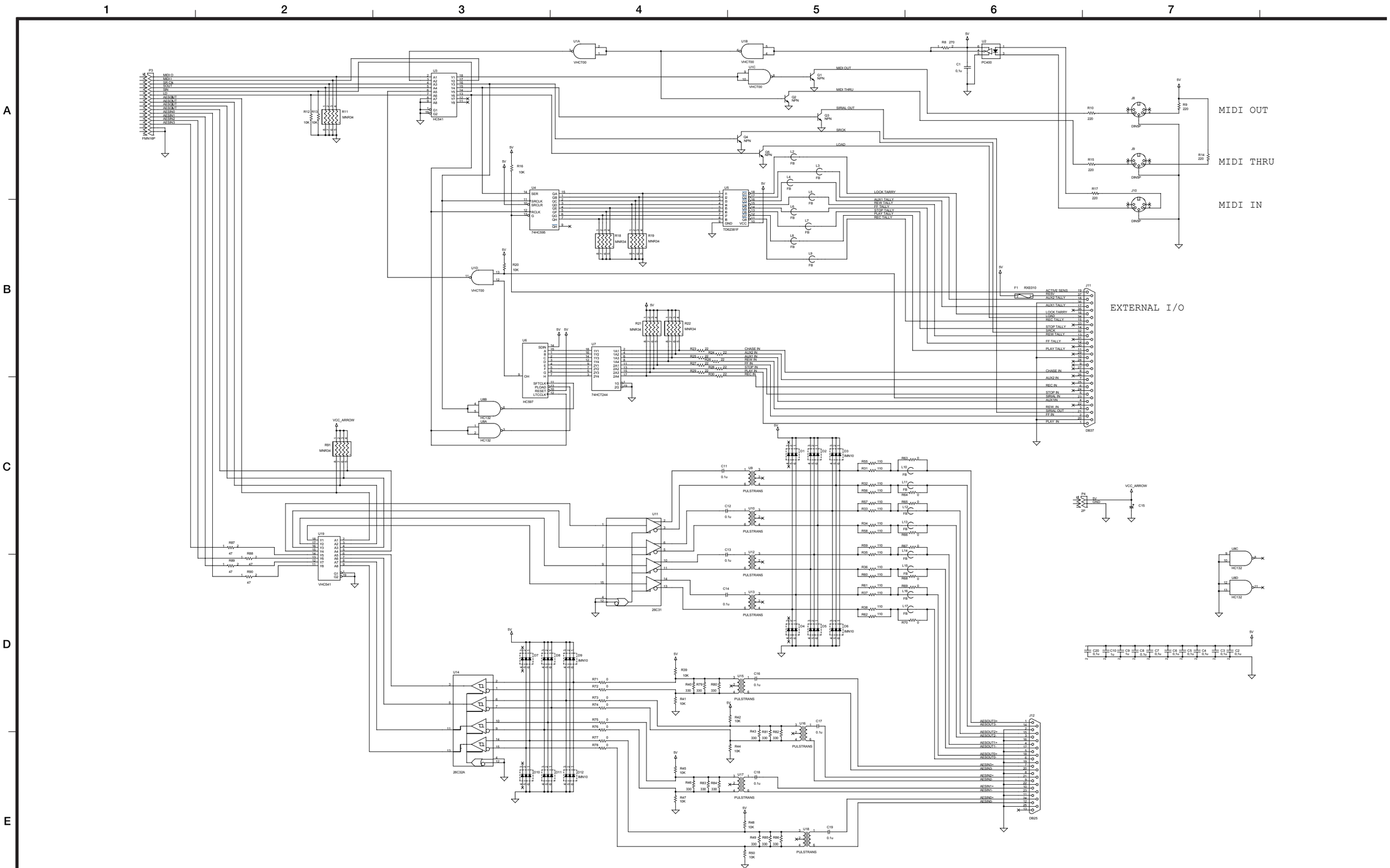


Digital Multitrack Recorder **DA-98HR**

1 st Issue; September 2000

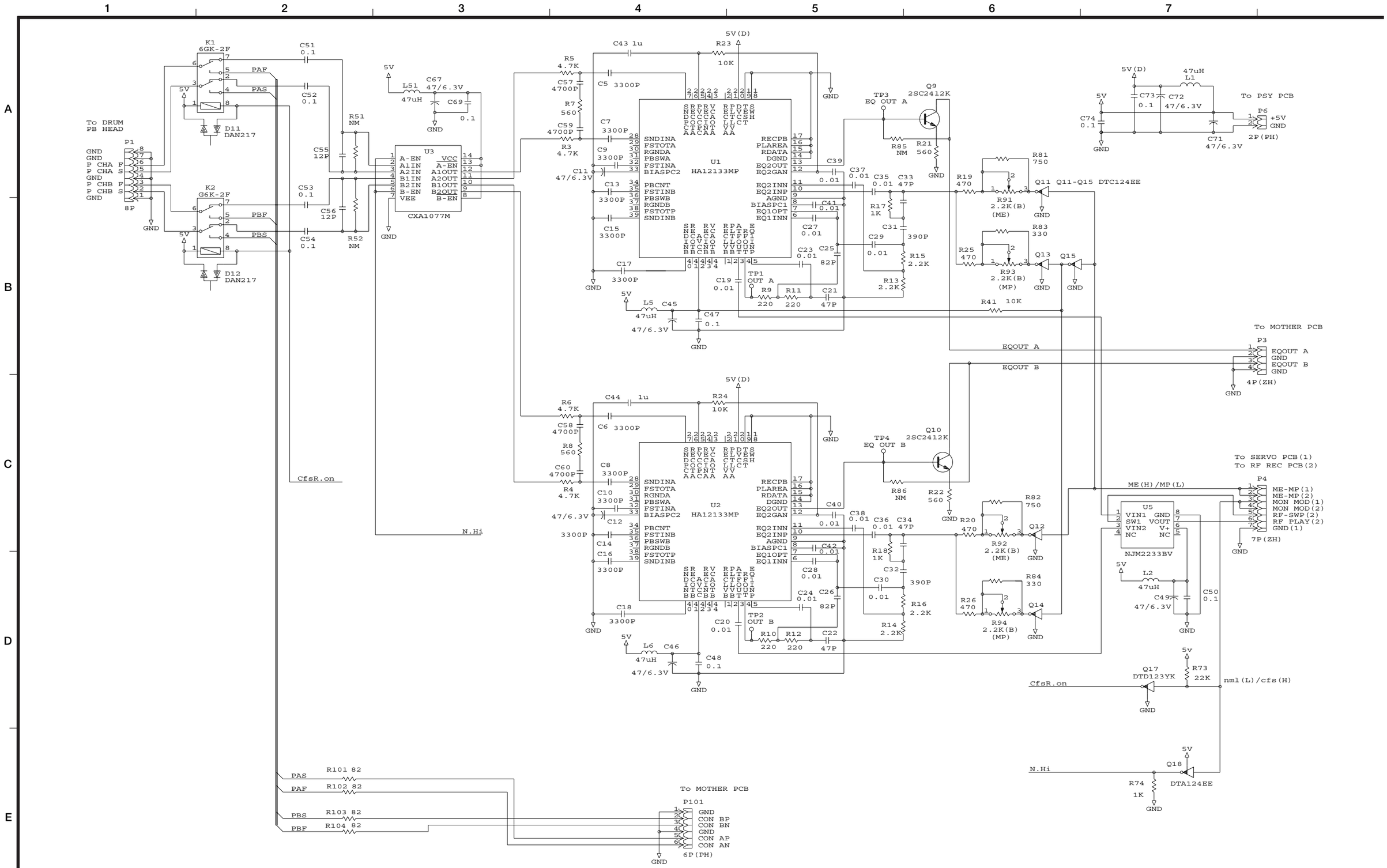

J1
TO P1 IN KEY PCB
BTK-8S-2S
D150 LB302DF
D151 LB302DF
D152 LB302DF
D153 LB302DF
SCN1-9
SCN1-11
SCN1-13
SCN1-15
SCN1-8
SCN1-10
SCN1-12
SCN1-14
LED:ANODE_COMMON
J2
TO P2 IN KEY PCB
SCN1-8 1
SCN1-9 2
SCN1-10 3
SCN1-11 4
SCN1-12 5
SCN1-13 6
SCN1-14 7
SCN1-15 8
J3
TO P5 IN KEY PCB
Q9
Q10
Q11
Q12
Q13
Q14
D94 TC_30DF
D101 FS_192
D107 PULL_UP
D113 PB_COND
D119 OFFSET
D95 TC_30ND
D102 FS_176
D108 PULL_DN
D114 REC_INH
D120 OUTPACH
D96 TC_29DF
D103 FS_96
D109 WORD
D115 TAPE_TC
D121 DITHER
D97 TC_29ND
D104 FS_88.2
D110 VIDEO
D116 ABS
D122 SHTLMON
D98 TC_25
D105 FS_48
D111 MID_9P
D117 TC
D123 DELAY
D99 TC_24
D106 FS_44.1
D112 EXT_TC
D118 TC_GEN
D124 VARI
SCN1-8
SCN1-9
SCN1-10
SCN1-11
SCN1-12


1
2
3
4
5
6
7
A
B
C
D
E
P1
RX+
RX-
P2 TX+
P2 TX-
VIDEO IN
BRK9PIN
WORD O
WORD I
TC OUT+
TC OUT-
TC IN+
TC IN-
FMN16P
L1
FB
WORD OUT
J1
BNC
WORD OUT
WORD IN
J2
BNC
WORD IN
R51 300
R52 300
R1 300
R2 300
H
N.C
J3
BNC_SW
WORD THRU
J4
BNC
VIDEO IN
VIDEO IN
R53 300
R54 300
R3 300
R4 300
J5
BNC_SW
VIDEO THRU
R5 22
BRK9
J6
RX-
RX+
R6 22
TX+
R7 22
TX-
RS-422
CONNECTOR DB9
J7
XLR
TC IN+
TC IN-
W1
EARTH
TC-IN
P2
XLR M
TC OUT+
TC OUT-
W2
EARTH
TC-OUT



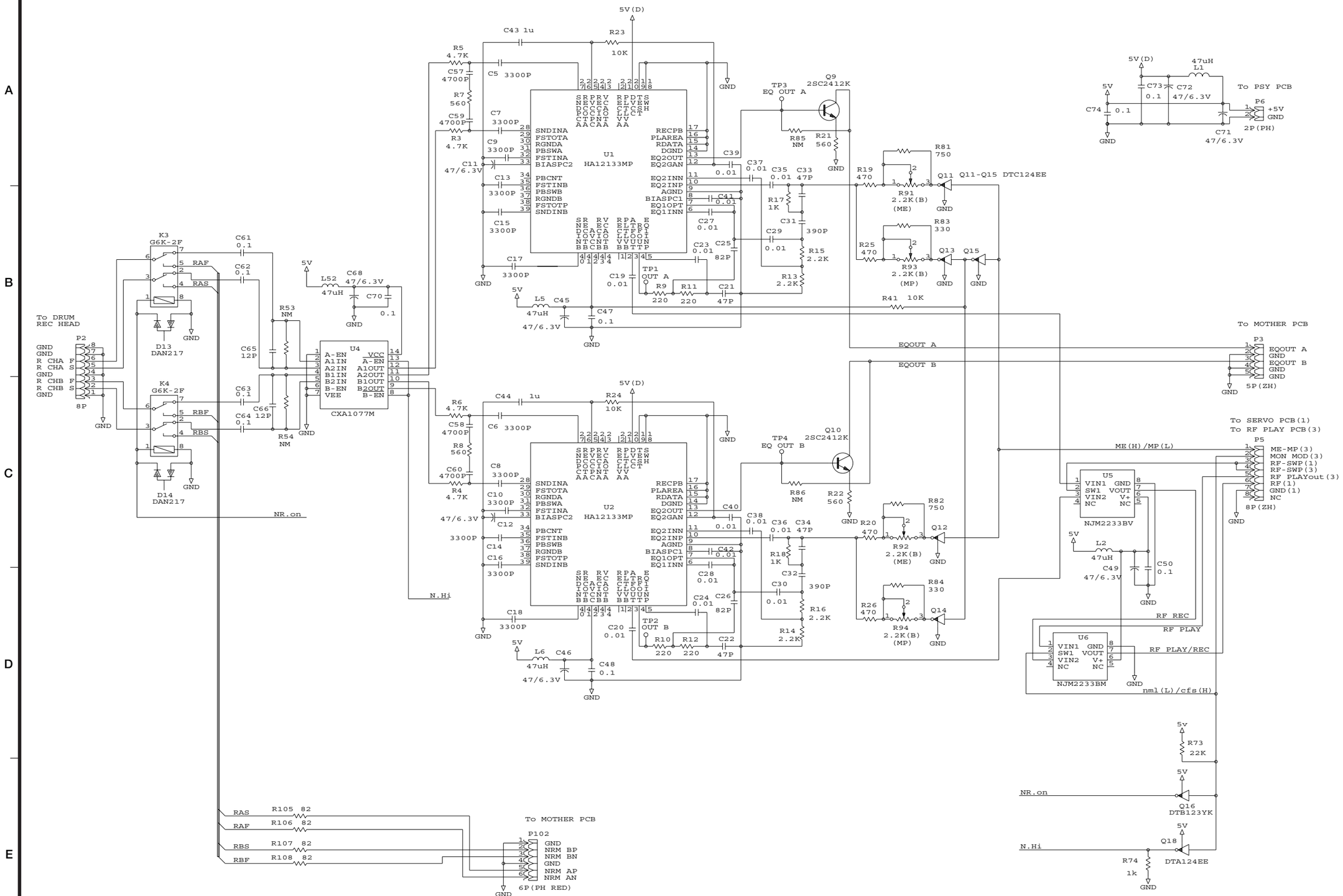
Digital Multitrack Recorder DA-98HR

1 st Issue; September 2000



Digital Multitrack Recorder **DA-98HR**

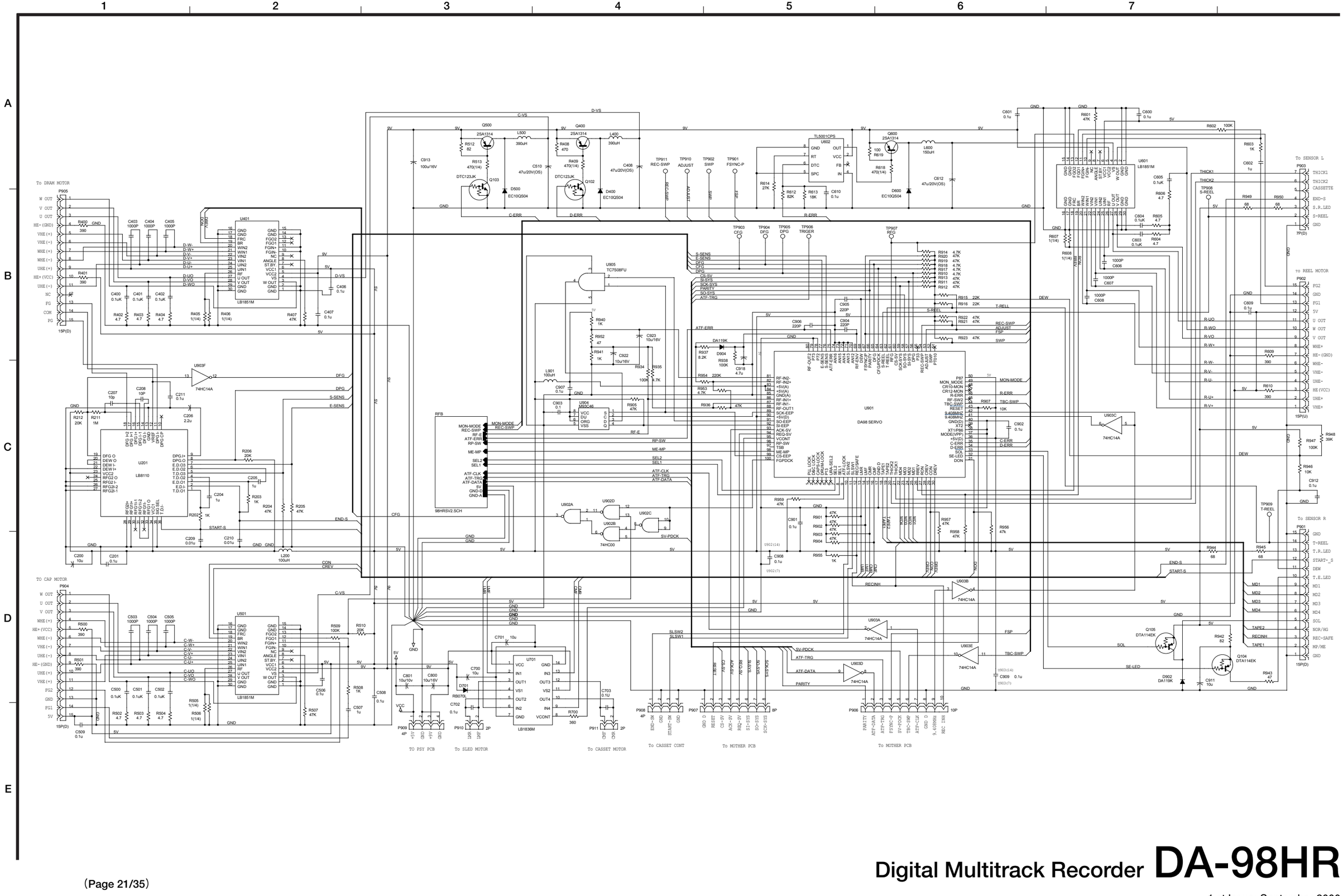
1 st Issue; September 2000



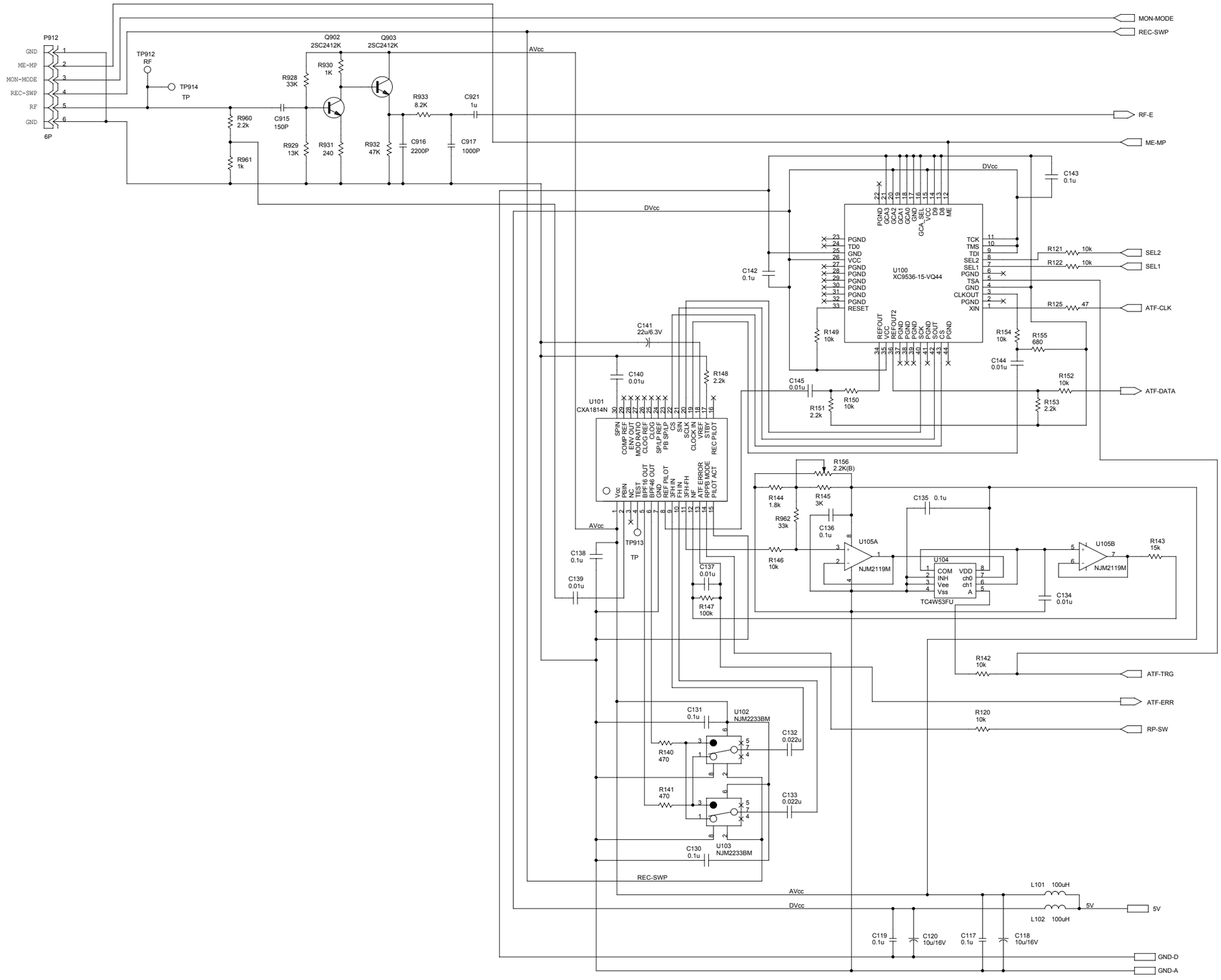
Digital Multitrack Recorder **DA-98HR**

1 st Issue; September 2000

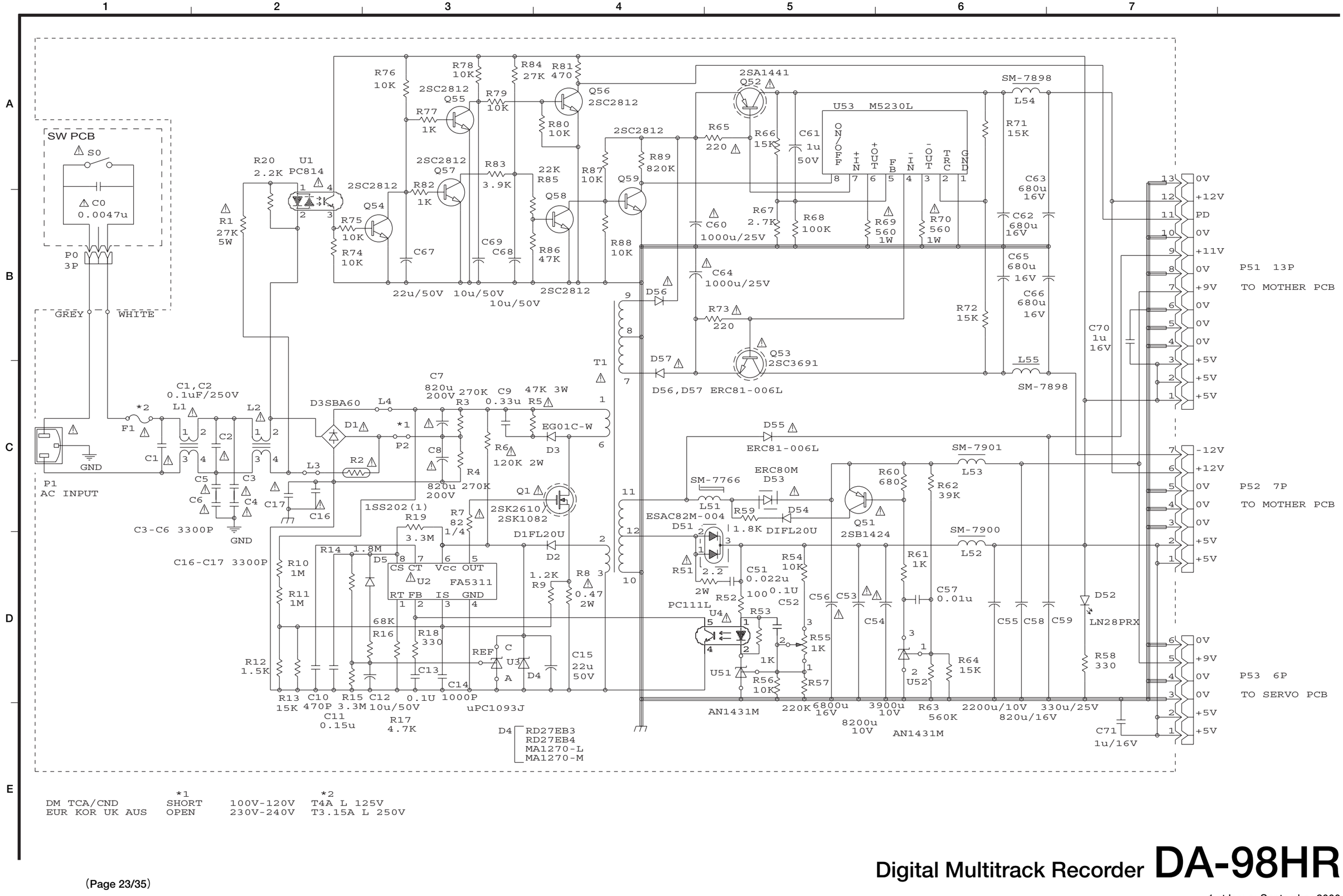
SCHEMATIC DIAGRAM DA-98HR SERVO PCB (1/2)



Digital Multitrack Recorder DA-98HR
1 st Issue; September 2000


P912
GND
ME-MP
MON-MODE
REC-SWP
RF
GND
6P
TP912
RF
TP914
TP
Q902
2SC2412K
Q903
2SC2412K
R928 33K
R930 1K
R933 8.2K
C921 1u
R960 2.2k
C915 150P
R929 13K
R931 240
R932 47K
C916 2200P
C917 1000P
R961 1k
AVcc
DVcc
MON-MODE
REC-SWP
RF-E
ME-MP
C143 0.1u
C142 0.1u
U100
XC9536-15-VQ44
R121 10k
R122 10k
SEL2
SEL1
R125 47
ATF-CLK
R154 10k
R155 680
C144 0.01u
R152 10k
ATF-DATA
R153 2.2k
C141 22u/6.3V
C140 0.01u
R148 2.2k
U101
CXA1814N
C145 0.01u
R151 2.2k
R150 10k
R156 2.2K(B)
R144 1.8k
R145 3K
R962 33k
C136 0.1u
C135 0.1u
U105A
NJM2119M
U105B
NJM2119M
R143 15k
U104
TC4W53FU
C134 0.01u
R146 10k
C137 0.01u
R147 100k
TP913
TP
C138 0.1u
C139 0.01u
R142 10k
ATF-TRG
ATF-ERR
R120 10k
RP-SW
C131 0.1u
U102
NJM2233BM
C132 0.022u
R140 470
R141 470
C133 0.022u
C130 0.1u
U103
NJM2233BM
REC-SWP
L101 100uH
L102 100uH
5V
C119 0.1u
C120 10u/16V
C117 0.1u
C118 10u/16V
GND-D
GND-A

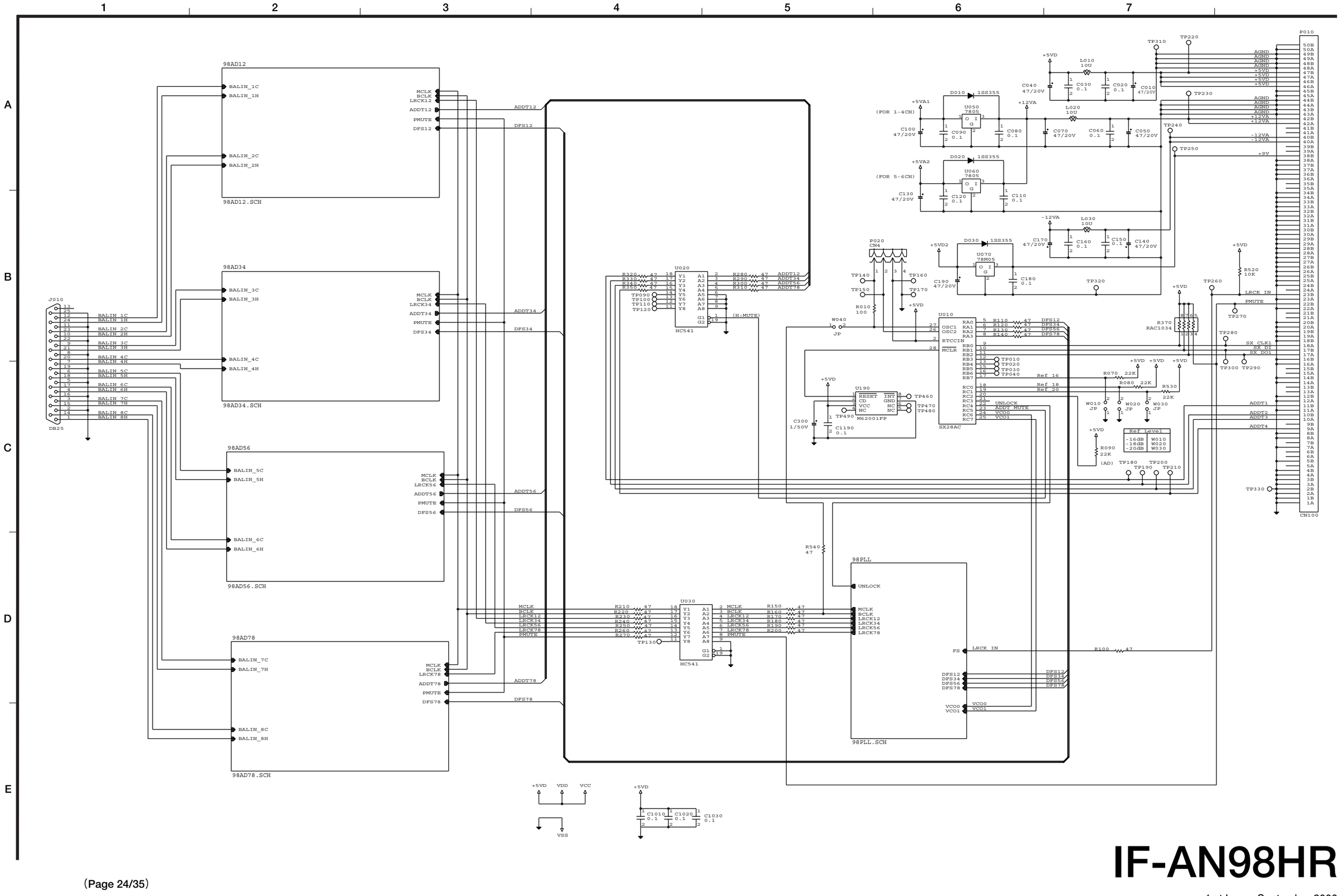
SCHEMATIC DIAGRAM DA-98HR POWER SUPPLY SECTION



Digital Multitrack Recorder **DA-98HR**

1 st Issue; September 2000

SCHEMATIC DIAGRAM IF-AN98HR IF98AD PCB (1/6)

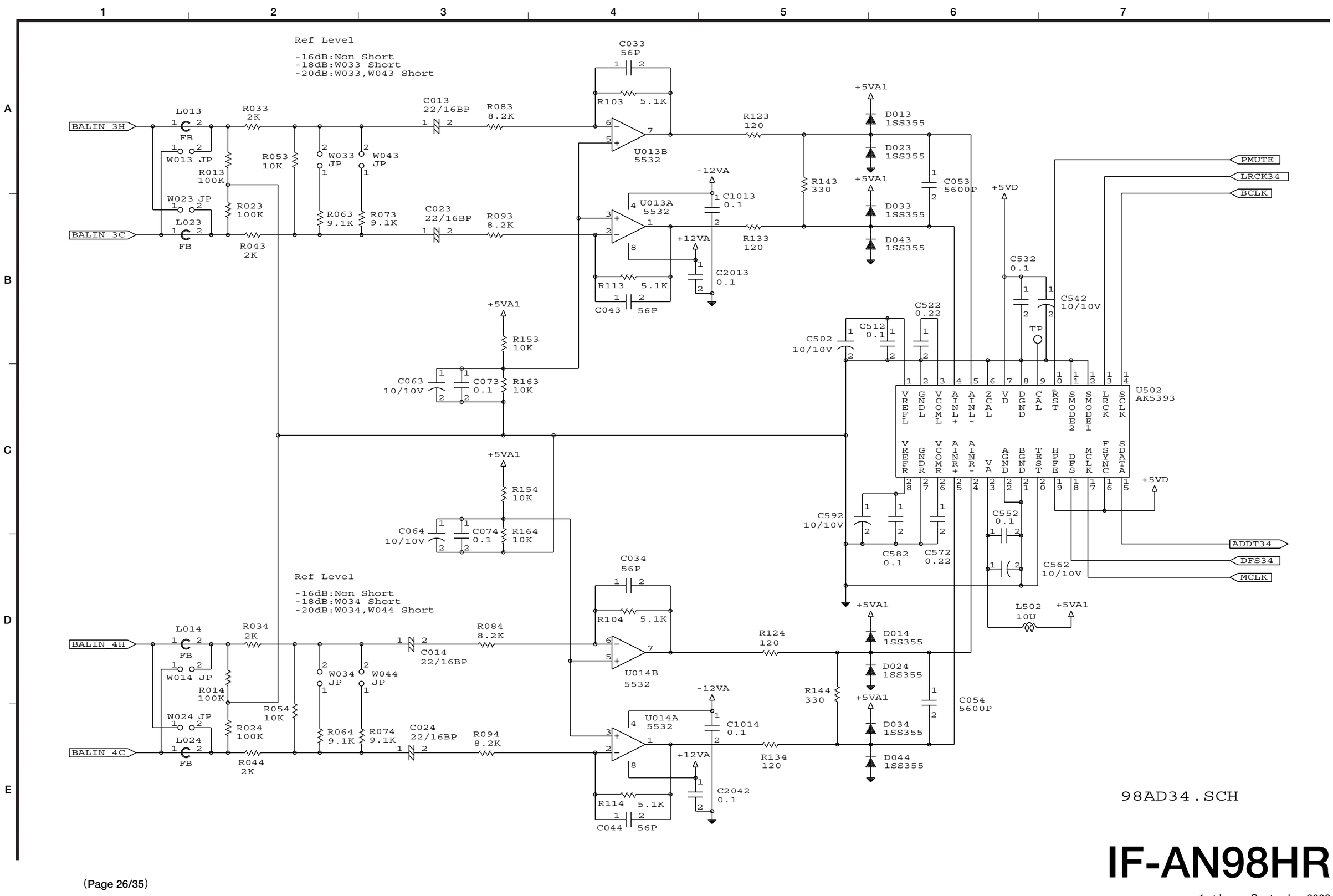


IF-AN98HR

1 st Issue; September 2000

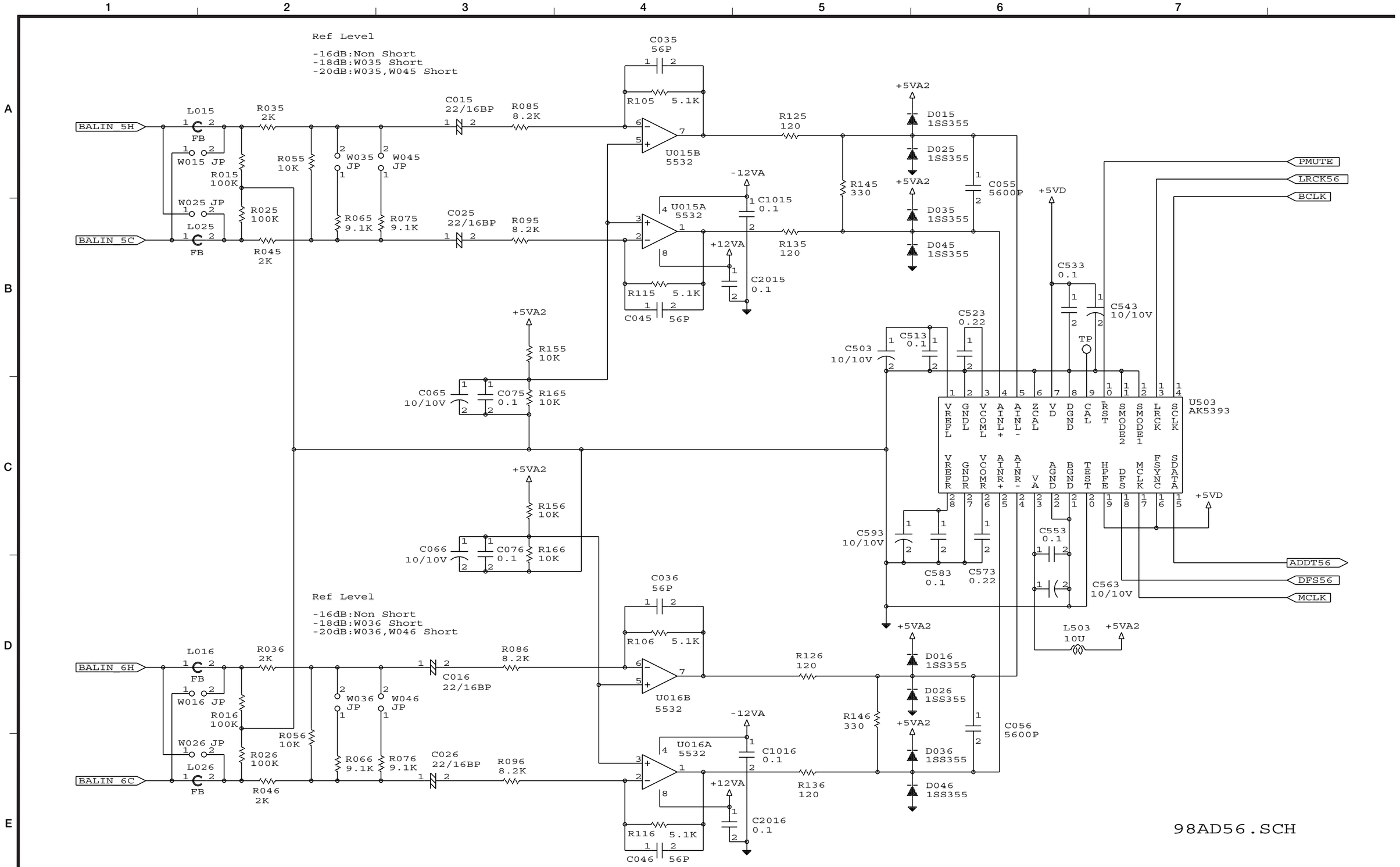
IF-AN98HR

1 st Issue; September 2000



IF-AN98HR

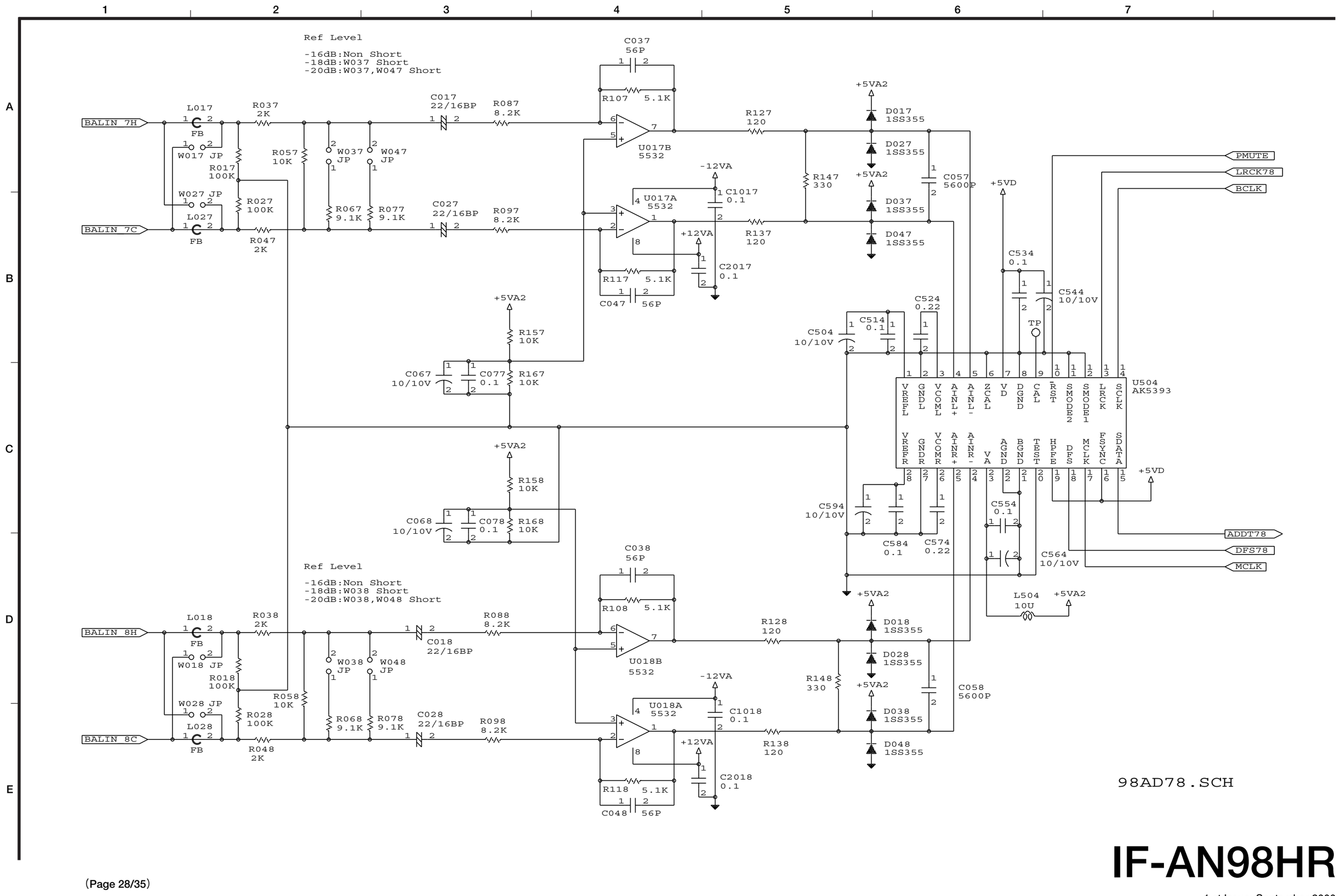
1 st Issue; September 2000



98AD56.SCH

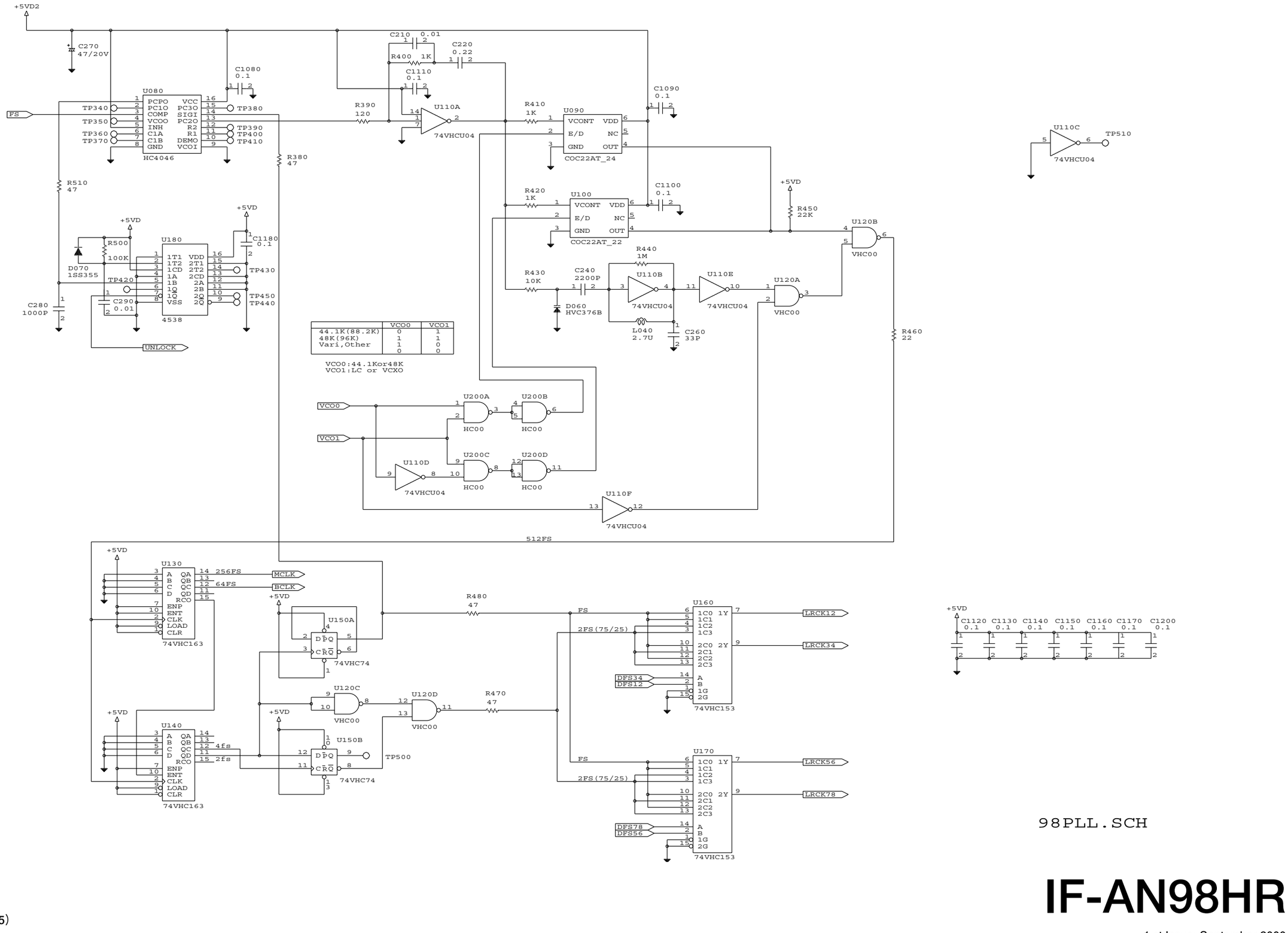
IF-AN98HR

1 st Issue; September 2000



IF-AN98HR

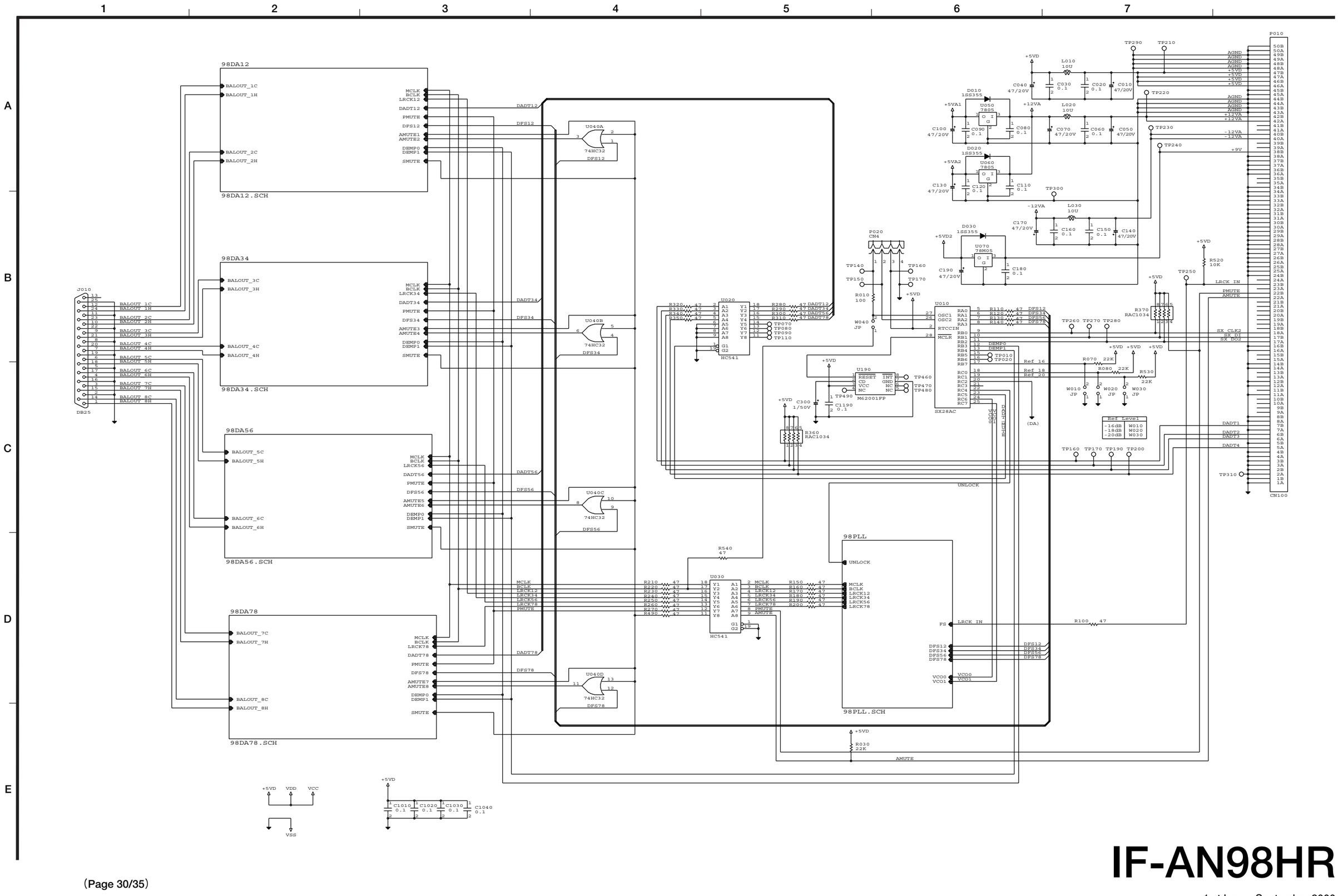
1 st Issue; September 2000



IF-AN98HR

1 st Issue; September 2000

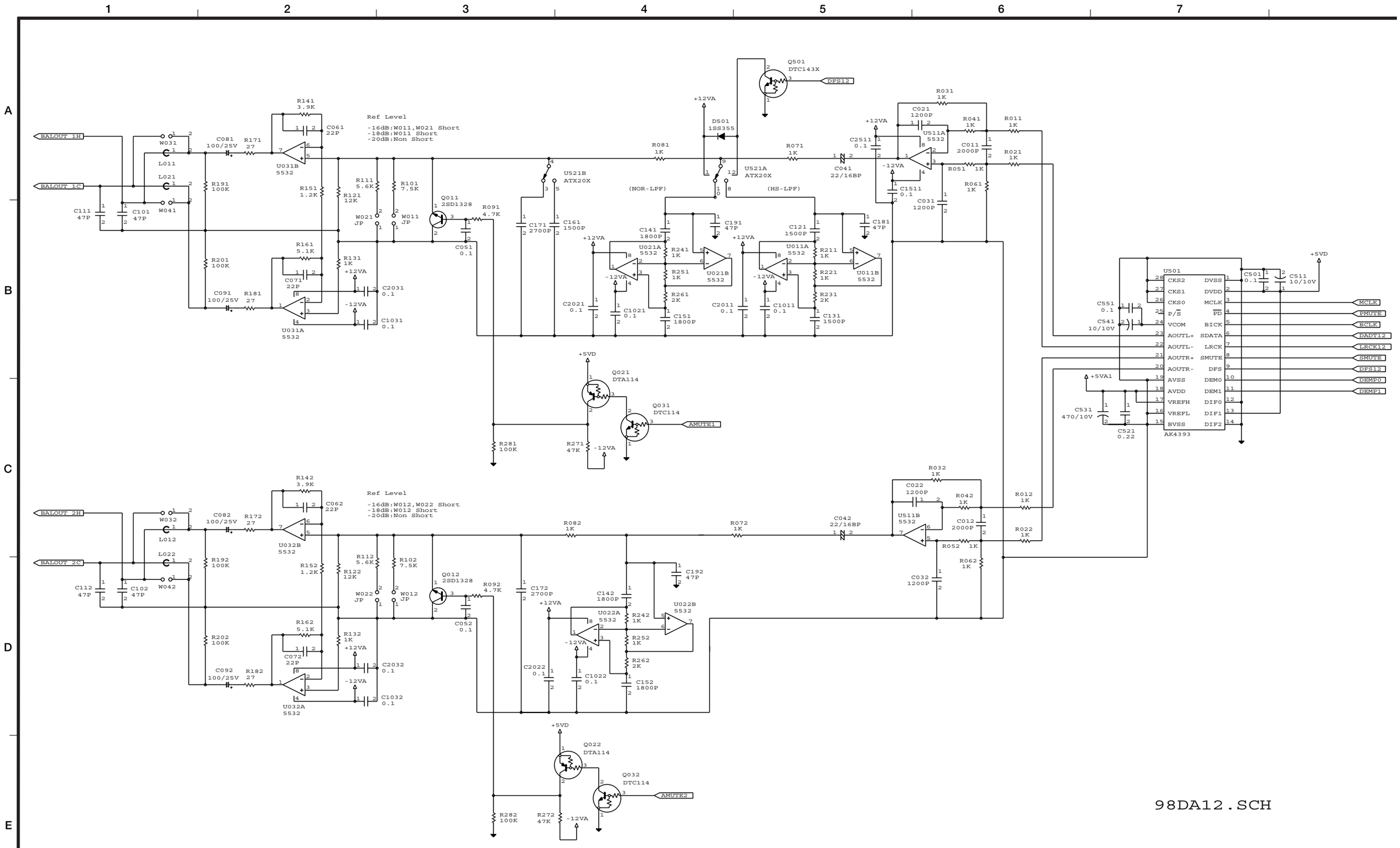
SCHEMATIC DIAGRAM IF-AN98HR IF98DA PCB (1/6)



IF-AN98HR

1 st Issue; September 2000

SCHEMATIC DIAGRAM IF-AN98HR IF98DA PCB (2/6)

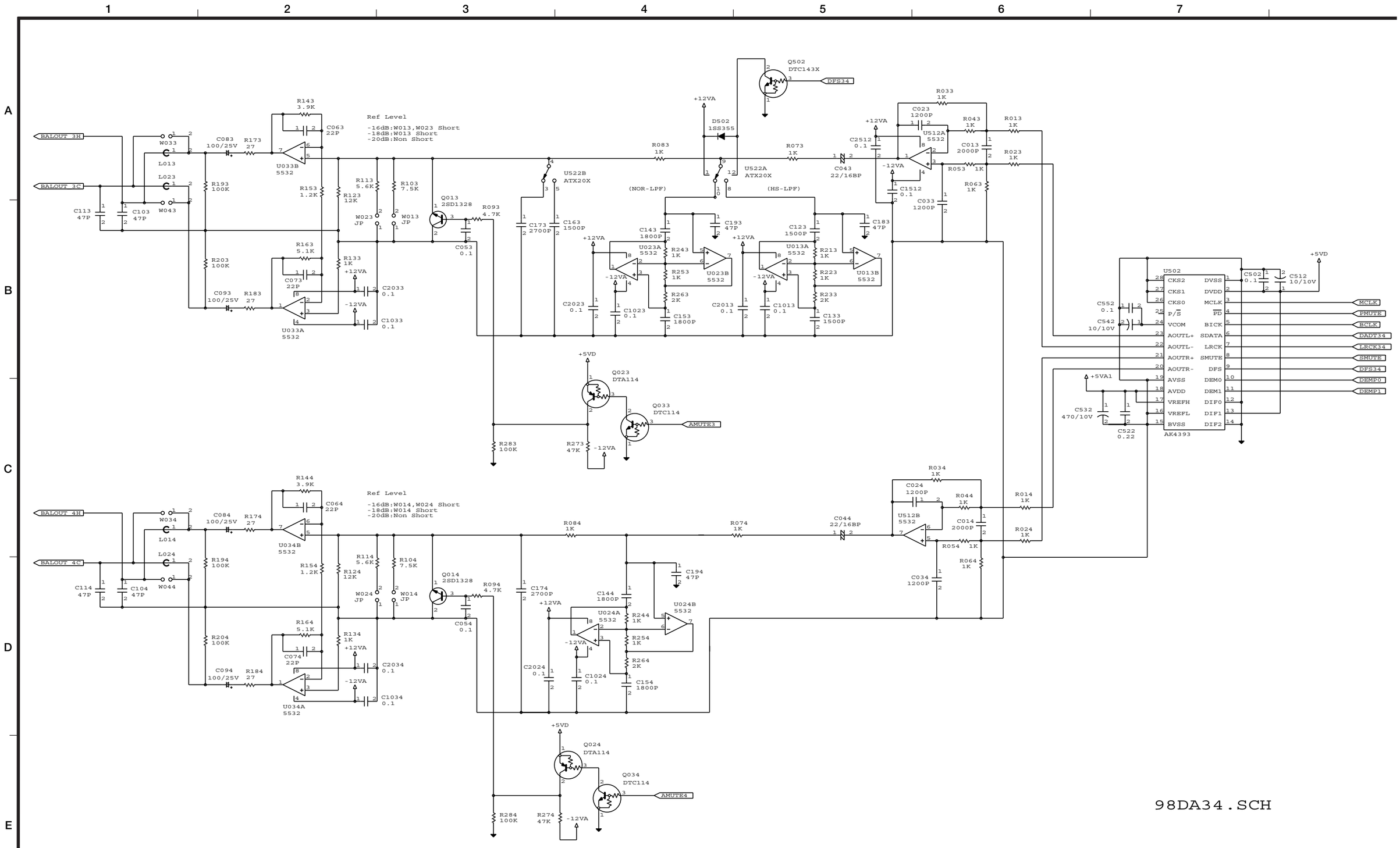


98DA12.SCH

IF-AN98HR

1 st Issue; September 2000

SCHEMATIC DIAGRAM IF-AN98HR IF98DA PCB (3/6)

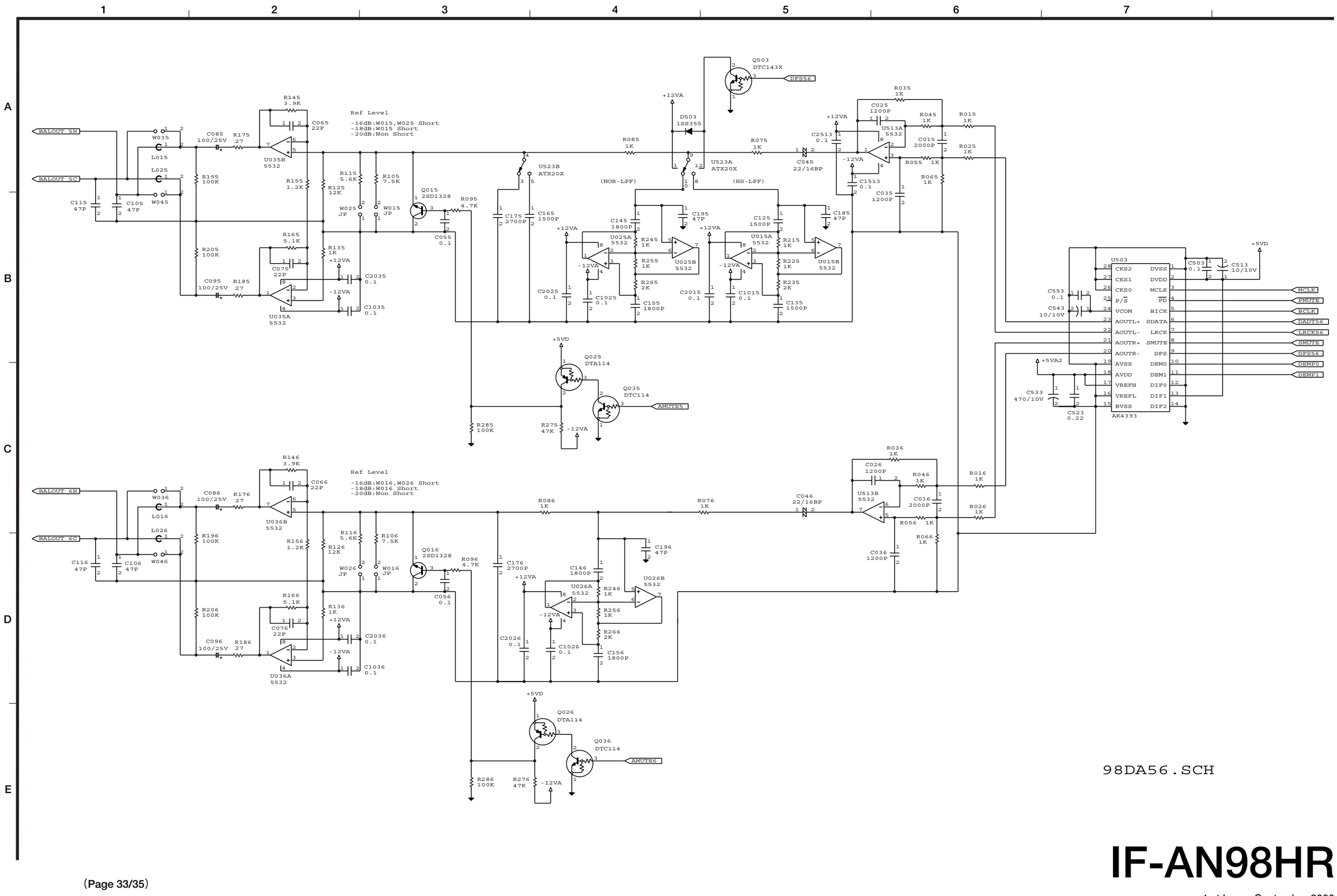


98DA34.SCH

IF-AN98HR

1 st Issue; September 2000

SCHEMATIC DIAGRAM IF-AN98HR IF98DA PCB (4/6)

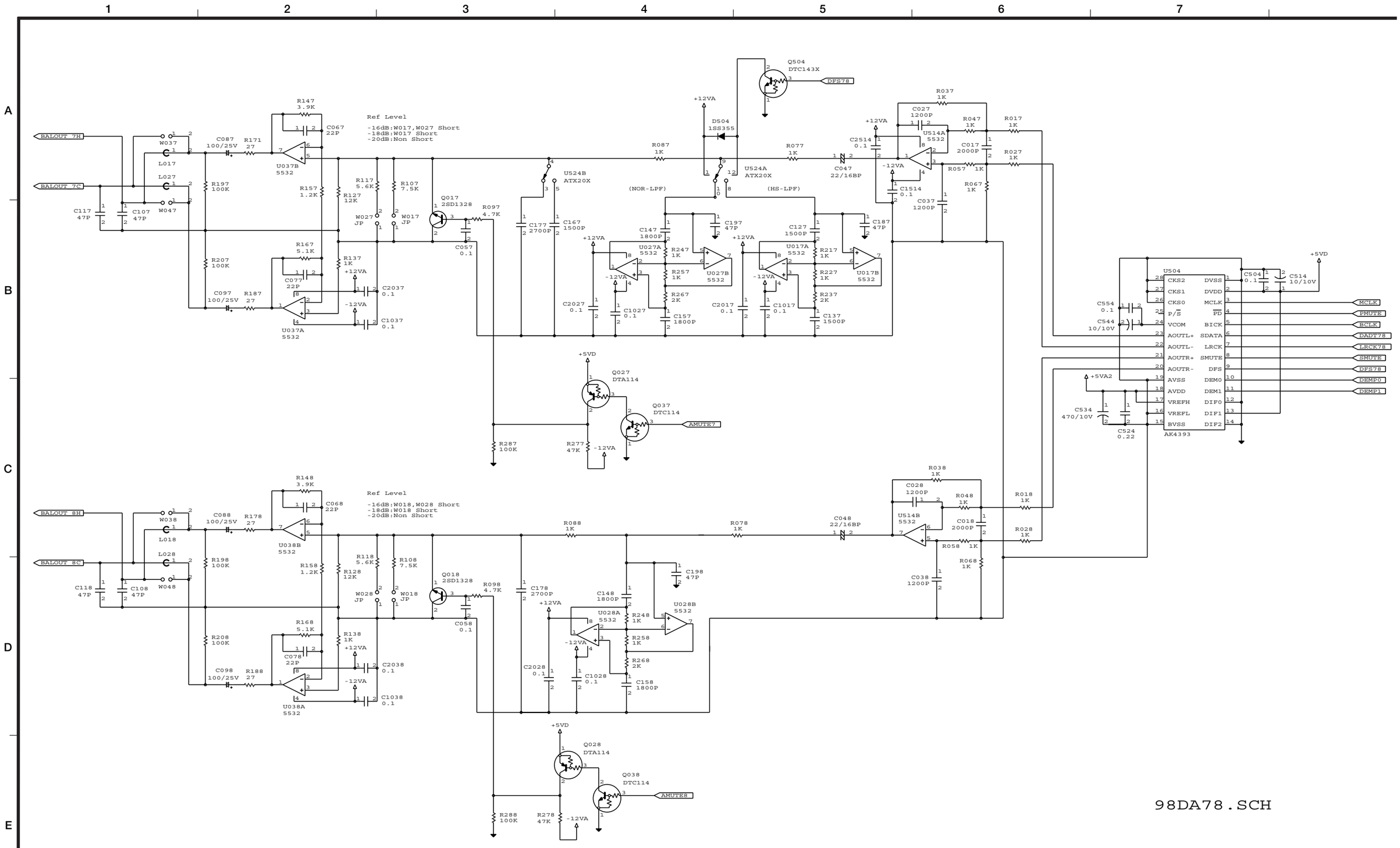


98DA56.SCH

IF-AN98HR

1 st Issue; September 2000

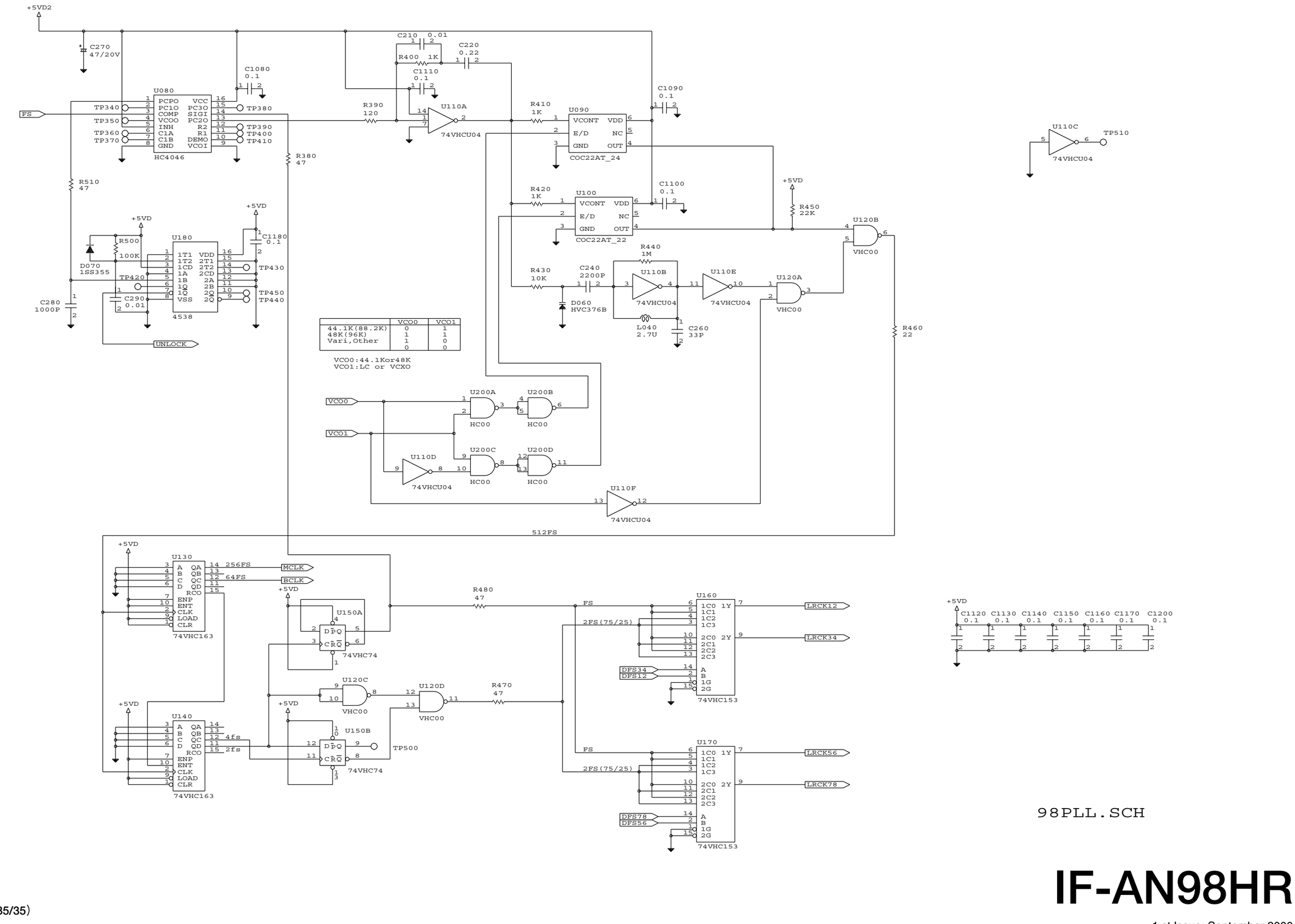
SCHEMATIC DIAGRAM IF-AN98HR IF98DA PCB (5/6)



98DA78.SCH

IF-AN98HR

1 st Issue; September 2000



IF-AN98HR

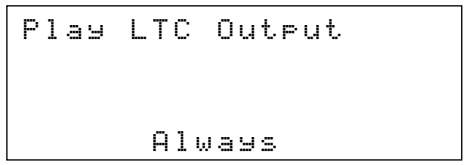
1 st Issue; September 2000

DA-98HR Version 1. 02

お客さまへ

バージョンアップ（SYSバージョン1.02）により以下の機能（メニュー）が追加になりました。
ご活用ください。

Play TC Out（メニューA）



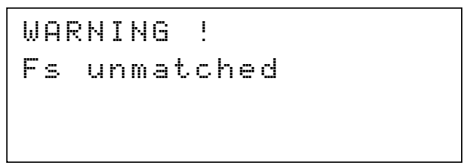
DA-98HRは、チェイスする機器とのロックアップ時間を早めるため、再生を始めるとすぐに（サーボがロックする前に）LTCを出力しています。
これを、サーボがロックしてから出力するモード（"Locked Only"）と、従来モード（"Always"）で切り換えられるようにしました。

Always（初期設定）
　再生を始めると同時にLTCを出力します。
Locked Only
　サーボがロックしてから（音声を出力するタイミングと同じタイミングで）LTCを出力します。

エラーメッセージ

DA-98HRは、等倍の他に2倍または4倍のサンプリング周波数で動作できます。この設定内容を「Track Fs」と呼びます。現在のTDIFでは、従来は使用していなかったビット（Eビット）を使って、このTrack Fs情報を表現しています。

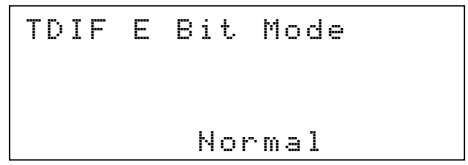
現在のマシン側のTrack Fs設定とTDIF入力の情報が異なっている場合は、以下のエラーメッセージを表示します。



ご注意

このエラーメッセージが表示されている状態では絶対に記録（録音）を行わないでください。
記録を行なっても、そのテープを正しく再生することはできません。

TDIF E Bit Mode（メニューB）



上の項目で説明したように、Eビットは従来使用していなかったため、このビットに意味がない情報を付加して出力する機器があります。
このような機器からデータを受信した場合は、正しいデータであるにも関わらず、上記のエラーメッセージ（WARNING ! Fs unmatched）を表示してしまうことになります。
このため、上記のエラーメッセージを出さないモード（メニュー）を追加しました。

Normal（初期設定）
　エラーメッセージを表示します。
　（Eビットデータを確認します。）
No Warning
　エラーメッセージを表示しません。
　（Eビットデータを確認しません。）

ご注意

No Warningに設定したときは、TDIF入力信号のTrack Fs情報がマシン側のTrack Fs設定状態と一致していることを確認してください。
設定が異なる信号を記録してしまうと、そのテープを正しく再生することはできません。

TEAC **TECHNICAL INFORMATION**

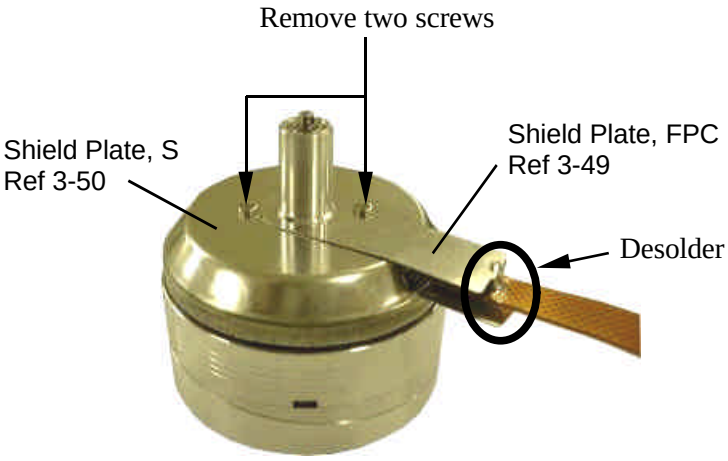
TASCAM DA-38 / DA-98, S-Error 02

No. **9848**
DATE 18th December 1998

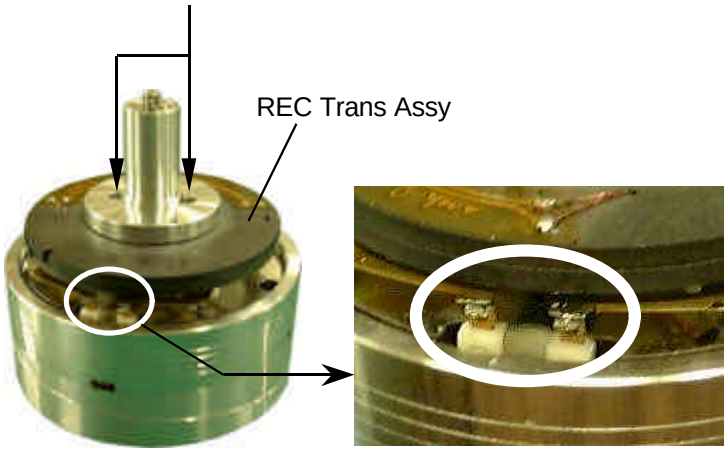
Symptom: Drum hesitates to rotate smoothly. `[S-Err 02]` is displayed.
Cause: Recording Rotary Transformer gets stuck. Gluing was not proper on some Rec Rotary Trans.
Solution: Replace the rotary transformer with Rec Trans Assy (SV), **P/No. V000863-00A**.

Procedure

1 Disassembling



Rotate the REC Trans Assy so that two screws can be found through the holes. Remove those two screws.

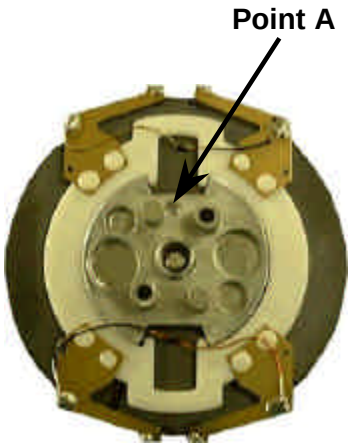


Desolder the head terminals. (There are same terminals at the opposite side.)

2 Assembling

Mount the new Rec Trans Assy onto the drum assy. After mounting, reinstate the all parts.

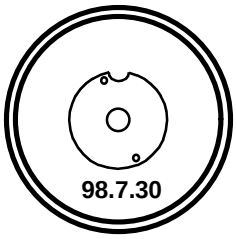
1) Point A and Point B shown below should meet upon assembling.
2) All screws are specified to be tightened by 1.5 kgf.cm.
   Use following tools introduced by Tech-Info No. 9516.
   P/No. 577282780-00 Torque Screwdriver
   P/No. J0025300 Attachment bit (+)



REC Trans Assy
P/No. V000863-00A
(bottom view)

Drum Assy
(top view)

Note:
1) Tokyo stock has been reworked and "8H" has been stamped at the carton box.
2) Following spares stock have been reworked.
   P/No. M004346-00B Drum Assy
   P/No. V000548-00B Drum Assy (RLP)
3) Gluing on the Drum Assy assembled after 30/July/98 has been secured.
   Date of production is indicated on the top of drum assy as shown below.



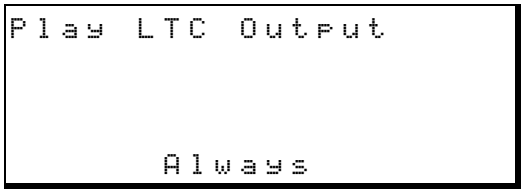
Drum Assy top view

These notes refer to changes and additions in the system version 1.02 of the DA-98HR DTRS recorder.

Please keep this sheet together with the original documentation for the DA-98HR.

Play TC Out (menu group A)

This new feature allows the setting of when LTC will be output by the DA-98HR, which may be found useful when using the DA-98HR with some timecode slave units.



There are two options:

Always (default), which will output LTC as soon as the DA-98HR starts to play back, even before the servo is locked.

Locked Only, which outputs LTC when the unit servo is locked (in the same way that audio data is only output when the unit is servo-locked).

Error message

The DA-98HR can record at base, dual or quad sampling frequency, and this Track Fs information is now included as part of the TDIF data. The "E bit" portion of the TDIF data, previously unused, contains this Track Fs information.

If the unit receives TDIF data with mismatched Track Fs information (that is, the TDIF data and the current settings do not match), the message below is displayed.:

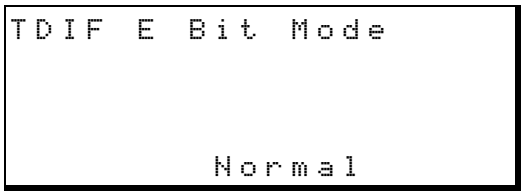
IMPORTANT NOTE

If this message is displayed, you should not record on the tape. Even if it appears that you have recorded on the tape, correct playback will be impossible.

TDIF E Bit mode (menu group B)

This new menu item allows you to ignore E bit data embedded in the incoming TDIF data, which under certain circumstances may be falsely interpreted by the DA-98HR as being sampling frequency errors (for example, when non-HR TDIF data is received from certain units). If such units output E bit data, the message described above will appear, even if the audio data is correct.

This menu item allows any such spurious data to be ignored and the error message suppressed:



There are two options:

Normal (default): the error message is shown.

No Warning: the error message is suppressed. Only select this option if you are completely certain that the sampling frequency of the input TDIF signal matches that of the unit's current settings.

IMPORTANT NOTE

If the input sampling frequency and the current settings do not match, even though it may seem that you can record on the tape, you will not be able to play back the tape correctly.

TECHNICAL INFORMATION

TASCAM DA-98HR/DS-D98, ROM Upgrade (SYS V1.54)

No. **0329**
DATE 29th July 2003

SYS ROM, U011 on the SYS PCB Assy has been upgraded from V1.52 to V1.54 on the following products.

- DA-98HR: S/No. 0160001 and higher
- DS-D98: S/No. 0050001 and higher

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.54	**S003967-00H**	**S0035153**, IC, MBM29F800BA-70PF

Problem corrected by SYS V1.54

1. Timecode output becomes unstable with only following setting.
   - TC Record Source = External TC
   - Output TC Source = Tape (TC Track)
   - TC REC key armed

With above setting, feed external timecode to TC IN.
If TC OUT is observed by measurement tool, jump of TC data is found.

2. In very rare occasion, DSD board cannot be recognized when powering on indicating “No DSD Board”. (DA-98HR does not relate to this problem.)

TECHNICAL INFORMATION

TASCAM DA-98HR/DS-D98, ROM Upgrade (SYS V1.55)

No. **0334**
DATE 09th October 2003

SYS ROM, U011 on the SYS PCB Assy has been upgraded from V1.54 to V1.55 on the following products.

- DA-98HR: S/No. 0180001 and higher
- DS-D98: S/No. 0050001 and higher

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.55	**S003967-00J**	**S0035153**, IC, MBM29F800BA-70PF

Problem corrected by SYS V1.55

On rare occasions, locating does not reach locate point. At this time the transport (time counter) goes back and forth around the locate point. Same thing occurs when chasing external timecode.
- This symptom occurs with only V1.52/V1.54.

TEAC **TECHNICAL INFORMATION**

TASCAM DA-98HR/DS-D98, ROM Upgrade (SYS V1.58)

No. **0403**
DATE 17th March 2004

Two changes have been made simultaneously on the following products.
- DA-98HR: S/No. 0180001 and higher
- DS-D98: S/No. 0050001 and higher

Change 1 Upgrade of SYS ROM (U011 on the SYS PCB Assy), V1.55 → V1.58
SYS V1.58, P/No. S003967-00L (PGMed ROM)

Change 2 Eliminating a noise on SWP (Switching Pulse: 33 Hz).
Adding 100 pF ceramic capacitor (P/No. C0004064) between U609-1 and 2 (SYS PCB Assy) to eliminate a noise on SWP. Refer to Item No. 3 below and page 2.

Problems corrected by V1.58

1. Incorrect IN and OUT point

Following symptom occurs only when the unit is running Auto Punch/Rehearsal mode.
1-1. During Rehearsal mode, unit turns to input monitor approx 30 msec earlier than IN point.
(Note: Recording works at IN point correctly.)
1-2. During Auto Punch mode, unit turns to Punch OUT 10-60 msec earlier than OUT point.
(Note: Rehearsal works at OUT point correctly.)

2. Incorrect time information of timecode output

When TC Offset is set from –5h through –12h, unit outputs "plus 1h" timecode from the TC OUT terminal while the tape is running at correct position.

Example: Now the unit is at 00h00m00s00f. Set TC offset to –05h00m00s00f. Then unit (tape) runs at 19hXXmXXsXXf correctly, however, TC from TC OUT terminal shows 20hXXmXXsXXf.

3. Noise recorded on ABS slave unit

On rare occasions, slave unit(s) in ABS chain would get out of sync resulting in noise recorded. This symptom is almost certain to occur only with DS-D98 running DSD mode, no report on PCM mode/DA-98HR so far.

Note: Small noise exists on the switching pulse (SWP: 33Hz) potentially. When this noise increases for some reason, above symptom occurs. So that the error correction program has been improved. On the hardware side, 100 pF ceramic capacitor has been added to U609-1/2 (SYS PCB Assy) to reduce the noise. See page two for the details.

4. Noise heard at Play Start

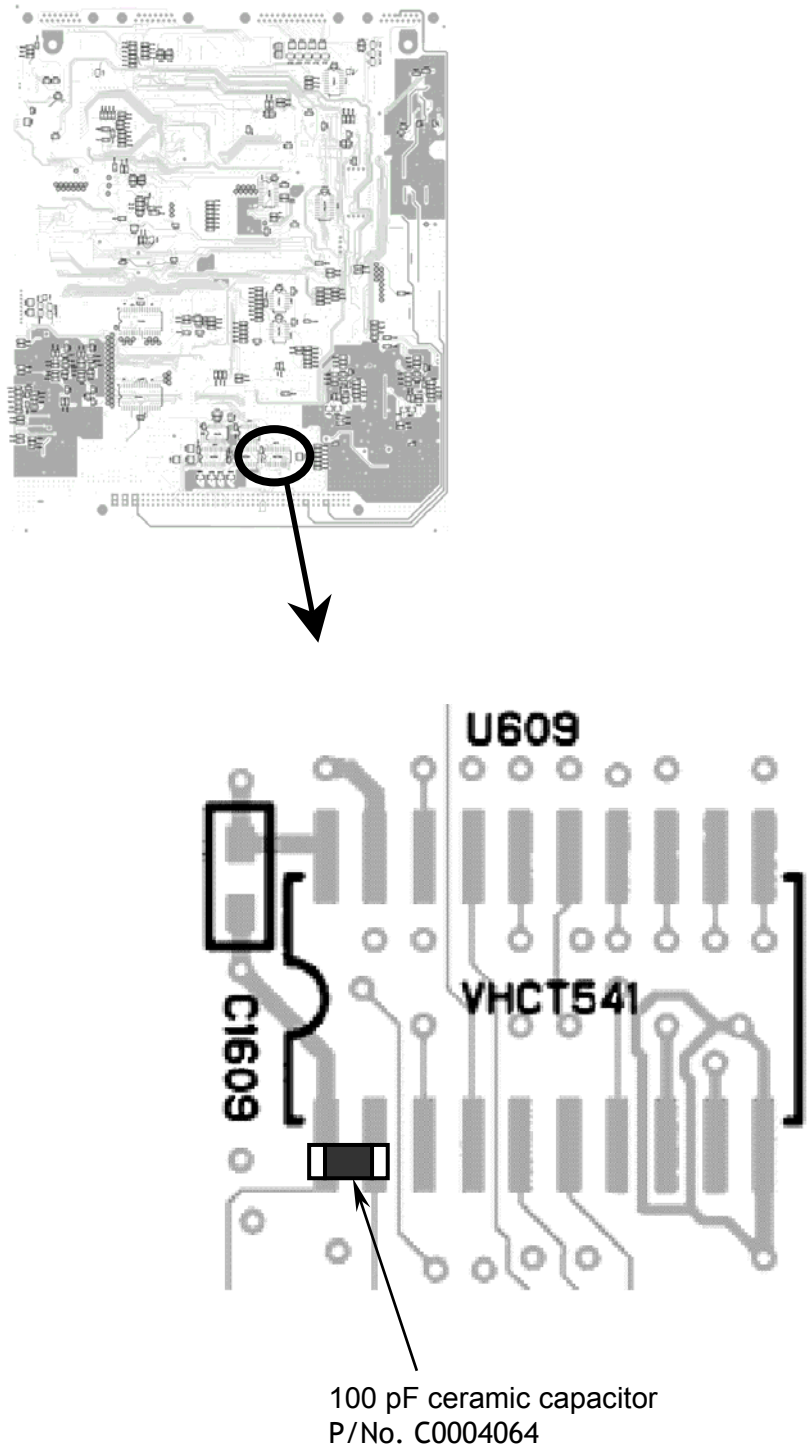
This symptom occurs with DS-D98 running DSD mode. (*No problem on PCM mode/DA-98HR)*
When start to play, sometimes noise is heard.

Note: Originally, audio mute is released 20 msec after the transport runs stably. However, this 20 msec was not enough to hide the internal noise. Prolonged to 400 msec.

Eliminating a noise on SWP (Switching Pulse: 33 Hz)

Add 100 pF ceramic capacitor (P/No. C0004064) between U609-1 and 2 (SYS PCB Assy).

SYS PCB Assy (Bottom Side)



TECHNICAL INFORMATION

TASCAM DS-D98, ROM Upgrade (DSD V1.23)

No. **0404**
DATE 17th March 2004

DSD ROM, U512 on the DSD PCB Assy has been upgraded from V1.21 to V1.23 on the products with S/No. 0050001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
DSD V1.23	**S004434-00E**	**S0031753, MBM29F040C-90PD**

Problem Corrected by DSD V1.23

When the unit is working on the DSD mode, click noise is recorded at the punch in/out point.
This noise has been once improved by V1.21 (Tech-Info No. 0204), however, it was not sufficient.

Notice:

- This upgrade is effective for only the units (S/No. 0020001 and higher) that have the new DSD PCB Assy. (Old DSD PCB Assy does not have above problem.)
- Do not mount the DSD V1.20/V1.21/V1.23 onto the units (S/No. 0010001 to 0019999) that have the old DSD PCB Assy.
- Refer to Tech-Info No. 0125R/0125R2 for the details of the old and the new DSD PCB Assy.

TECHNICAL INFORMATION

TASCAM DS-D98, ROM Upgrade (DSD V1.24)

No. **0407**
DATE 25th May 2004

DSD ROM, U512 on the DSD PCB Assy has been upgraded from V1.23 to V1.24 on the products with S/No. 0050001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
DSD V1.24	**S004434-00F**	**S0031753, MBM29F040C-90PD**

Problem Corrected by DSD V1.24

Now unit is working on the DSD mode. If the Clock Source is set to "SLOT", noise is shown on the meters even if no input signal is connected. This noise can be recorded.

Above problem occurs with DSD V1.23 only.

Notice:

- This upgrade is effective for only the units (S/No. 0020001 and higher) that have the new DSD PCB Assy. (Old DSD PCB Assy does not have above problem.)
- Do not mount the DSD V1.20/V1.21/V1.23/V1.24 onto the units (S/No. 0010001 to 0019999) that have the old DSD PCB Assy.
- Refer to Tech-Info No. 0125R/0125R2 for the details of the old and the new DSD PCB Assy.

To allow the use of the advanced features provided by the HR series of TASCAM DTRS recorders, the DA-98HR and DA-78HR, the RC-898 remote control unit has been updated.

In addition, some other features have been made to reflect changes in the DTRS product line.

Note that when using this version of the RC-898 (2.0), units in the HR series should be at least system version 1.12 (DA-78HR) and system version 1.01 (DA-98HR). It is strongly recommended that it is not used with HR series units with earlier system versions.

The changes are restricted to menus and menu items. In other respects, the operation of the RC-898 is as described in the existing manual.

Track Delay Time (menu group 0)

DA-98HR – Note that although the operation of this function has not changed significantly, when it is used in conjunction with the DA-98HR's higher sampling frequencies (dual-frequency and quad-frequency), the number of samples now accurately reflects the time selected on the DA-98HR (that is, a higher sampling frequency is expressed as a larger number of samples for a given time).

Also note that when fewer than eight tracks are available for recording as the result of selecting a dual or quad sampling frequency, the unavailable tracks are not shown for selection.

For example, if the first DTRS unit in the chain is a DA-98HR which has been set to record at a sampling frequency of 192k (quad-frequency), only tracks 1 and 2 of this unit are available for recording and are shown for selection on the RC-898 screen, and instead of tracks 1 through 8 being available for grouped selection (usually, 1–8 appears in the display), only tracks 1 through 2 are available (1–2).

Track Copy (menu group 0)

DA-98 & DA-38 – Note that this menu item applies only to DA-38 and DA-98 DTRS units.

When it is required to change the input assignment of DA-98HR and DA-78HR units, the new Input Patchbay menu item (see immediately below) should be used.

Input Patchbay (menu group 0)

DA-78HR & DA-98HR – This new menu item allows the assignment of different signal sources to the inputs of the appropriate DTRS machine.

Input Patch						Mon 1		
Trk	1	2	3	4	5	6	7	8
Src	T	M	S	S	D	M	S	S
ch	1	–	3	4	5	–	7	8

There are four different sources that may be selected: T (tape), D (the currently-selected digital source on the DA-98HR), S (the slot source on the DA-98HR) and M (mute—this is not really a source).

Note that when this menu is used to select the input sources of a DA-78HR, the S option can refer only to the analog inputs. The D option refers to the SPDIF input, if this has been selected, otherwise to the TDIF-1 inputs.

If all tracks have been selected for recording at base frequency (DA-98HR), all tracks are shown, otherwise only those tracks available for recording are shown.

1 **Select the machine for editing (SHIFT + ▲ or ▼ keys).**

2 **Use the ◄ and ► cursor keys to move to the appropriate track.**

3 **Use the ▲ or ▼ keys to change the input source.**

4 **To select the source channel, use the ◄ cursor key to move to the extreme left of the screen, (Src) and then move the cursor down to the ch row.**

5 **Use the ► cursor key to select the channel (as defined in the ch row) number.**

To return to the source row, once again move the cursor to the extreme left, and then move up.

Rec Mute (menu group 1)

DA-98, DA-78HR & DA-98HR – The rec mute function can be enabled on a track-by-track basis, as described in the RC-898 manual.

However, note that if a DA-98HR unit is used and the sampling frequency is set to dual- or quad-frequency so that there are fewer than eight tracks available, only those tracks that are available will be shown in this screen.

Analog Reference Level (menu group 2)

DA-98 & DA-98HR – When this screen is selected with a DA-98HR fitted with AD and DA boards such as the optional IF-AN98HR boards, the input and output reference levels can be viewed (the changes are made using jumpers on the IF-AN98HR boards).

```
Analog Ref Level
      Machine  1
   Input    Output
  -16 dB    -16 dB
```

When this screen is selected with a DA-98 unit, the input and output reference levels can be set together to –16 dB, –18 dB or –20 dB.

```
Analog Ref Level
      Machine  1
      In/Out
      -16 dB
```

Video Reference (menu group 3)

DA-98HR – On the DA-98HR, the incoming video reference can be detected automatically (Auto) and this setting will typically work satisfactorily.

However, to improve synchronization in the case of a less-than-perfect video sync source, the rate can be manually set to any of the following: 30F, 29.97F, 25F, or 24F. See the DA-98HR manual for full details of this function.

```
Video Reference
      Machine  1


          Auto
```

1 **Select the machine whose video reference is to be edited.**

2 **Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the value.**

TC Accuracy (menu group 4)

DA-78HR & DA-98HR – When using the RC-898 with the DA-78HR and the DA-98HR, it is possible to change the timecode accuracy on a per-machine basis.

This means that slightly nonstandard timecode input can be accepted and used by the units which have the `Wider` option selected. Typically, all units will use the `Normal` setting, however:

```
TC Accuracy
Wider
Normal
Machine 1 2 3 4 5 6
```

1 Use the ◄ and ► cursor keys to move to the appropriate machine column.

2 Use the ▲ or ▼ keys to move the cursor to the appropriate line for that machine (either the `Wider` or the `Normal` line).

Consult the DTRS unit's manual for full details of this facility.

TC Timing (menu group 5)

DA-98HR, DA-78HR & DA-98 – When using the AD conversion facilities in the optional slot boards for the DA-98HR, and when using the DA-78HR, it is now possible to select either an analog or a digital timing reference for the timecode inputs and outputs independently. With the DA-98, this option is available for timecode output only.

The screen title and display have now changed (the screen shown below refers to a DA-98HR or DA-78HR unit).

```
TC Timing
     Machine  1
  Input   Output
  Analog  Analog
```

1 Select the machine whose timing reference is to be edited.

2 Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the timecode timing value for the input and output of that machine.

Clock (menu group 9)

All units – Although this screen appears the same as in previous versions of the RC-898, the available options have been changed to reflect the new models.

As before, the options for the DA-88 and DA-98 models (as well as for the DA-78HR and DA-98HR) are `Int` (internal), `Word` (word clock) and `Video` (video input).

For the DA-78HR and DA-98HR, the `Dig in` option has been added (digital inputs).

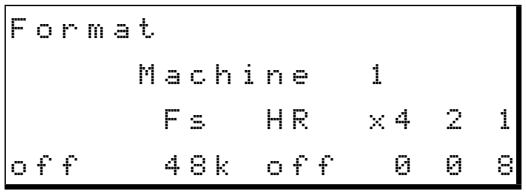
For the DA-98HR only, the `slot` option has been added, allowing certain optional slot boards to be used as the clock master. Note that the same restrictions apply as on the DA-98HR (for example, the IF-AN98HR slot boards cannot act as the master clock source).

Format (menu group 9)

DA-78HR & DA-98HR – This menu has been expanded to recognize the high-resolution and high sampling frequency capacities of the newer models.

In the case of both the DA-78HR and the DA-98HR, a HR (high-resolution) field allows the setting of this parameter to be on (24-bit) or off (16-bit).

In the case of the DA-98HR, the sampling frequency selected acts as the base frequency for the unit. The available track combinations are then displayed on the bottom right of the screen.



When the cursor is moved to this field, use the ▲ and ▼ keys to switch between the following options:

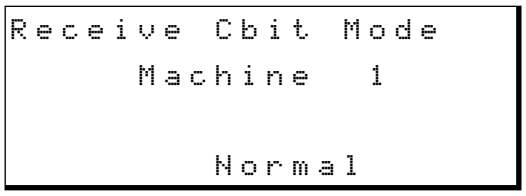
0 0 8	(eight base-frequency tracks)
0 2 4	2 x dual-frequency tracks, 4 base-frequency tracks
0 3 2	3 x dual-frequency tracks, 2 x base-frequency tracks
0 4 0	4 x dual-frequency tracks
2 0 0	2 x quad-frequency tracks

The process of selecting machines for the formatting process, and actually carrying out the format is as described in the RC-898 manual (move the cursor to off, change the message to ready, change the message to on, and then use the **RECORD** and **PLAY** key combination to start the format process).

Consult the DA-98HR manual for full details of the available track functions.

Receive Cbit Mode (menu group A)

DA-98HR – When using the DA-98HR, any mismatches between the received audio data and the data specified by the Cbits in the audio data stream will usually be shown on the DA-98HR display. However, it is possible to turn this off, using the screen here:



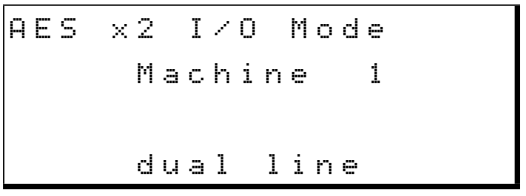
1 **Select the machine to be edited.**

2 **Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the parameter to either** Normal **or** No Warning.

AES x 2IO (menu group A)

DA-98HR – When using a DA-98HR unit when four dual-frequency tracks have been selected as the available tracks, there is a choice of how the signals should be output: either as dual-line or high-frequency signals, as explained more fully in the DA-98HR manual.

The settings are made using the following screen:

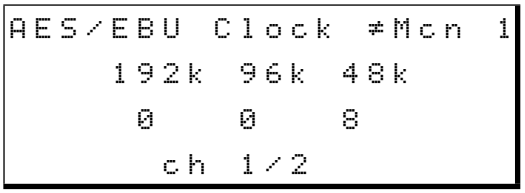


1 **Select the machine to be edited.**

2 **Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the parameter to either** dual line **or** high speed.

AES/EBU Clock (menu group A)

DA-98HR – When recording on the DA-98HR with AES/EBU inputs, you may wish to select one of the options described here as a clock source.

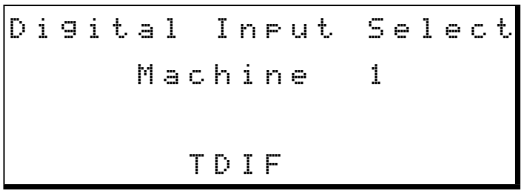


When this screen is shown, the current available track setting for the selected machine is also displayed. This available track setting also affects the choice of clock source, as does the dual AES/EBU mode described above.

Setting	Available clock source channels
Base x 8	1/2, 3/4, 5/6, 7/8
Dual-frequency x 4 (dual channel)	1, 2, 3, 4
Dual-frequency x 4 (high-speed)	1/2, 3/4
Dual-frequency x 2, base x 4	1, 2, 3/4, 5/6
Dual-frequency x 3, base x 2	1, 2, 3, 4/5
Quad-frequency x 2	1, 2

Digital Input Selection (menu group A)

DA-78HR & DA-98HR – This menu item allows the selection of digital sources for these two units in addition to the TDIF-1 input source.

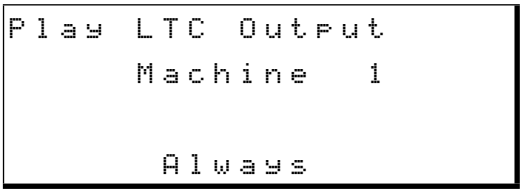


For the DA-98HR, the choice is either `TDIF` or `AES/EBU`.

For the DA-78HR, the choice is either `TDIF` or `SPDIF`.

Play TC Out (menu group A)

DA-78HR & DA-98HR – This menu item allows you to choose whether the selected unit will always output linear timecode (LTC) or will only output such timecode when the unit clock is locked (that is, it outputs LTC only when audio data is output).



The two options here are `Always` and `Locked Only`.

Output Patchbay (menu group B)

DA-78HR & DA-98HR – This screen allows the assignment of a track's audio to any output, simulating a digital patchbay. Only the numerals in the bottom row of the screen can be changed here (that is, the audio track number).

```
Output Patch
      Machine  1
  ch  1 2 3 4 5 6 7 8
 Trk  1 2 3 4 5 6 7 8
```

Mix Input Selection (menu group B)

DA-78HR & DA-98HR – This screen allows the selection of the sources for the internal mixer of DA-98HR and DA-78HR units.

```
Mix Input        Mcn 1
 Trk  1 2 3 4 5 6 7 8
 Src  T M S S D M S S
  ch  1 - 3 4 5 - 7 8
```

1 Select the machine for editing.

NOTE

If the machine selected is not capable of being controlled using this menu (that is, it is neither a DA-98HR nor a DA-78HR) an appropriate message is shown.

2 Use the ◄ and ► cursor keys to move to the appropriate track.

3 Use the ▲ or ▼ keys to change the input source.

4 To select the source channel, use the ◄ cursor key to move to the extreme left of the screen, (`Src`) and then move the cursor down to the `ch` row.

5 Use the ► cursor key to select the channel (as defined in the `ch` row) number.

To return to the source row, once again move the cursor to the extreme left, and then move up.

Output Word Length (menu group B)

DA-78HR & DA-98HR – This menu allows either 16-bit or 24-bit to be selected as the word length of the output audio data.

```
Output Word Length
 16 bit
 24 bit
Machine 1 2 3 4 5 6
```

The rows on this screen represent the bit resolution of the output audio, and the columns represent the machines in the chain.

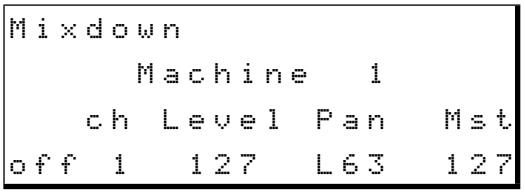
1 Use the ◄ and ► cursor keys to move to the appropriate machine column.

2 Use the ▲ or ▼ keys to move the cursor to the appropriate line for that machine (either the `16 bit` or the `24 bit` line).

Mixdown (menu group B)

DA-78HR & DA-98HR – This screen allows the sources selected for mixdown in the screen described above to be mixed into a stereo pair, with individual level and pan for each channel of the mix, as well as a master level for the whole stereo mix.

Select the machine on which the mixdown is to take place.



The bottom left parameter controls whether the mixdown is on or off for the machine. If this is set to off, no other settings made on this screen will have any effect.

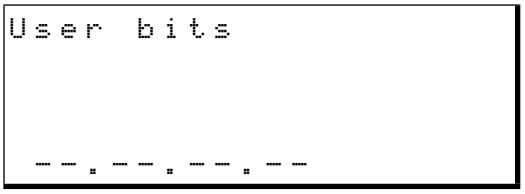
The channel may be selected, and the level adjusted from 0 to 127.

Pan settings are from hard left L- through L63 through C (center) to -R (hard right).

The master mix volume may be adjusted from 0 to 127.

User bits (menu group D)

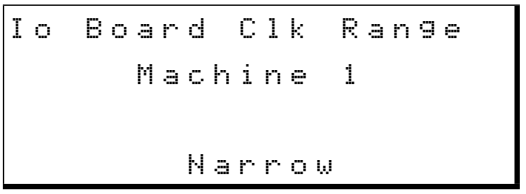
DA-78HR & DA-98HR – There are no parameters to be set in this screen, which simply displays any user bits recorded within the timecode source.



IO Clock range (menu group D)

DA-98HR – When using the DA-98HR with the optional IF-AN98HR slot boards, it may be necessary to adjust the clock width setting.

The Narrow setting enables a crystal oscillator, and suppresses jitter, providing high-quality audio. However, if the clock master accuracy is low, the precision is affected, and the audio quality may suffer. The Wide setting enables an LC oscillator. The jitter level is increased a little compared with the Narrow setting and the audio quality may be slightly diminished, but this setting can be used even with poor-quality input clocks.



For details of the limitations imposed on this setting, consult the appropriate section of the DA-98HR manual.

Tape Load/Save (menu group F)

DA-78HR & DA-98HR – This allows the saving and loading of the RC-898's settings to and from tape. The settings that are saved are:

- Locate Points (Master only)
- Locate Pre-roll
- GPI Setup
- Event
- 9pin Control Mode
- 9pin Rec Acceptable
- Key Mode
- Frame Display
- Display Time

These parameters are stored on tape. They do not affect any audio data on the tape. Only one set of parameters can be stored on one tape.

NOTE

This operation only applies to the tape recorded on the first machine in the chain (ID=1).

1 With a tape loaded in the unit, use the ▲ and ▼ keys to select either `Load` or `Save`. Press SELECT.

2 The display shows `Are you sure ?`. Press SELECT to confirm the operation. To cancel the operation, press either ESCAPE or STOP so the display shows `Cancel`. Press the ESCAPE key to dismiss this message.

While the operation is taking place (either loading or saving the data), the display shows `Executing...`. Any REC FUNCTION indicators will go out.

3 If the operation is successful, the display shows `Complete`. Press the ESCAPE key to dismiss this message.

If an error occurs, one of the following messages may appear. Press the **ESCAPE** key to dismiss these messages:

`Can't start`	A suitable tape is not loaded, etc.
`Data not found`	No data has been recorded on the tape (when loading)
`Read error`	An error occurred when reading the data from tape (when loading)
`Verify error`	An error occurred when certifying the data after writing (when saving)

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TEAC TECHNICAL INFORMATION

TASCAM DA-98, ROM Upgrading, SYNC Version 1.06

No. **9715**
DATE 17th October 1997

SYNC software in flash ROM, U602 on the System PCB Assy has been changed to:
Version 1.06, P/No. S002444-00B.

SYNC Version 1.06 corrects following problems:

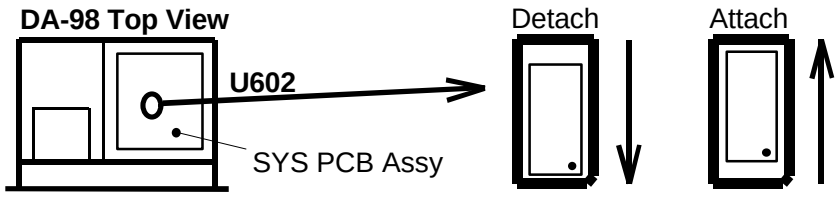
1 If "TC Frame Mode" is changed several times, system of the timecode stops to work.
2 Sometimes unit does not enter pull down mode.

3 Problem on 9 pin Control
3-1 If DA-98 is controlled by Micro Lynx, chase lock up may take time or get out of sync.
3-2 Reply to PAUSE command from control device was "stop" then corrected to "pause".
3-3 When Rec Track Select status on slave unit(s) is changed by Rec Function keys on DA-98/RC-848, "edit data sense" is unrecognized by control device.

4 Problem on Synchronization
4-1 If operation of SHUTTLE → PAUSE is made, display window shows different time data than actual timecode (LTC) output.
4-2 Chase lock up may take time or get out of sync if INT is set for the clock reference.
4-3 Timecode may jump while zero cross point is reproduced. This occurs only when the original frame rate on tape is changed to others and reproduced.

5 Problem on using RC-848
Note: Following phenomenon occurs on slave unit(s) in the multiple DA-98 system.
5-1 Reaction to the command coming from RC-848 V3.00 takes about 4 seconds.
5-2 RC-848 does not update the data when IN point is changed on DA-98.
5-3 RC-848 does not indicate "frame rate on tape", "frame rate on external TC" and "external TC".
5-4 If "Time Mode" is changed by DA-98, it takes 2 seconds to update the data on RC-848.

Locate and replace U602 on the SYS PCB Assy with referring to below.



Products with S/No. up to 0059999 in Tokyo stock have been reworked and replaced with SYNC V1.06.
They can be identified with "**E7**" mark stamped at the right side of S/No. on the carton box.
Products with S/No. 0060001 and higher have been mounted SYNC V1.06 with no mark.

Important Information for Service Stations and Customers

TEAC TECHNICAL INFORMATION

9721

TASCAM DA-98, False Powering On

26th December 1997

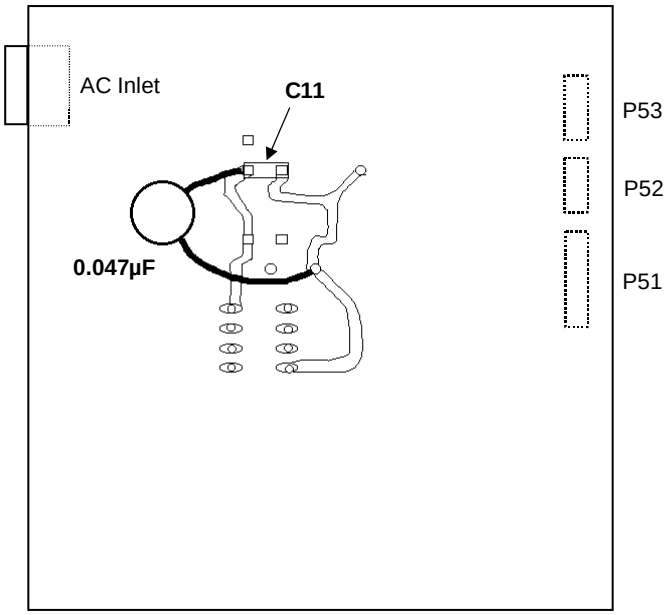
Symptom: When the power switch is turned on immediately after power off, all functions become to disable occasionally.
Cause: Capacitance of C11 (0.1 µF) on the switching regulator unit is small value.
Solution: To increase the capacitance, 0.047 µF capacitor is added to parallel with C11. Then total capacitance becomes approximately 0.15 µF.

P/No. 51734350-00, Ceramic Capacitor, 0.047 µF 50V CK45F T

Procedure

1 Remove a top cover.
2 Remove a switching regulator with referring to 2-12, page 8, DA-38 service manual.
3 Remove a shield plate mounted on the bottom side of the switching regulator.
4 Add 0.047 µF capacitor as shown below.

Switching Regulator Soldering Side



On the products with S/No. 0050001 and higher, C11 has been replaced with 0.15 µF.
A marking of red color dot is applied on a heat sink on the switching regulator unit.

TEAC TECHNICAL INFORMATION

9802

TASCAM DA-98, ROM Upgrade (SYS and SYNC V1.20) 13th February 1998

SYS ROM (U105) and SYNC ROM (U602) on the System PCB Assy have been changed as indicated below:

	Old	New	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS	V1.00	V1.20	**S002439-00B**	**S0018093** (OTP, M27C512-12C1)
SYNC	V1.06	V1.20	**S002444-00C**	**S0024333** (Rewritable, MBM29F400BA)

Note: **SYS** V1.20 should absolutely be combined with SYNC V1.20 or greater otherwise an alert message will be displayed.
SYNC V1.20 can work on related features and corrections even if SYS version is older than V1.20.

SYS and SYNC V1.20 have been mounted on the products with serial number 0080001 and higher.

1. Problem Correction on SYS and SYNC ROM

When punch out is made by REW, a part of syllable erasure at out point occurs on odd (even) track being reproduced while even (odd) track is recorded. This occurs only when clock reference is selected at Internal.

2. Problem Correction on SYS ROM

Unit will not stop (keep FF or REW) at the beginning of locate point in Repeat or Automatic Punch In/Out mode when "Resolve on" is selected.

3. Problem Correction on SYNC ROM

1) Operation with Soundmaster
DA-98 works more reliably in Soundmaster ION Studio Operating Environment.

2) TC chase
a) Rechase window
"Rechase window" function now supported when clock selection is "Internal".

b) Error indication "Can not chase : No tape TC"
During TC chase if the slave unit cannot momentarily read its own timecode, the unit will suddenly stop and show the error message "Cannot chase: No tape TC" in its display. The ability of the DA-98 to recover from this momentary error without stopping has been resolved.

3) 9 pin

a) Auto edit

Repeating auto edit during preview.
Does not auto edit.
Does not review.

b) Track input monitor

Occasionaly a DTRS remote controller can not receive "track input monitor" status from a DA-98 when "Select EE on" or "edit off" (means selected EE off) is selected.

c) Slave unit not changes status

Slave unit does not change its status (slave unit should follow master unit) when master unit receives "full EE on" or "select EE on" command via 9pin.

d) Track arm status

Does not send back the right "track arm status" via 9pin.

4) Video clock

Unit may freeze when a video input signal greater than 1Vp-p is received.

5) Fs shift

Slave unit will not lock (will not go into PLAY even ABS differencial is "0") during TC chase pull down mode.

6) MIDI

a) Track arming via MMC

Can not arm tracks via MMC commands from E-magic Logic Audio V2.6.

b) MTC output

Minimized the tendency of the MTC output to drift.

7) DTRS Remote controller

a) Sin osc on

Can not receive the "sin osc on" command from a DTRS remote controller during stop.

b) TC generator

DA-88's timecode generator cannot be turned of when it it slaving to a DA-98 master.

c) Resolve on

Slave unit could not receive the following settings from master unit during power up or when the master's settings were changed.

rechase mode: free/rechase
rechase window: 1 sec./2 sec
error bypass: 10 F/30
resolve: off/on
resolve mode: free/resync
TC frame mode

New Functions on SYS and SYNC ROM

1) Clock mode: Within this new function " **Auto** " and " **Individual** " selections are available.

Auto: When using multiple DA-98's, the clock source of slave DA-98's will be automatically selected as indicated below.

	Master DA-98	**Slave DA-98**
Time mode = ABS	All clock sources	S-word*
Time mode = TC	Internal	Internal
	Video or Word	S-word*

*S-word : The clock is received from the master DA-98 via the PW-88S cable.

Individual: When using multiple DA-98's, the clock source of each ***individual*** slave DA-98 can be selected manually (like DA-88 version 4) as indicated below.

	Master DA-98	**Slave DA-98**
Time mode = ABS	All clock sources	S-word*
Time mode = TC	Internal	Any clock source can be selected by each individual DA-98
	Video	
	Word	

*S-word : The clock is received from the master DA-98 via the PW-88S cable.

Operation

Enter menu group "A".
Move the cursor to "Clk Mode" and press "ENTER".
Press the ▲ or ▼ key to select the "Auto" or " Individual" mode.

CAUTION

Upon formating or recording, pay attention for the unified clock source thoughtout the DA-98 in "Individual" selection otherwise incompatibility may result.

2) Device Type

When the "MACHINE" key followed by a numeric key (1 corresponding to the MASTER machine, 2 to Slave 2 etc.) is pressed on the RC-848, a "Device Type" is displayed in the green LCD screen (ex. DA-88 Ver. 4 or DA-38). The RC-848 also understands functions that are "unique" to a particular "Device Type". The RC-848 could not recognize the DA-98's "Device Type". Based on the "Device Type" selection, what will be recognized by the RC-848 is indicated in the chart below.

Device Type	**RC-848 Recognition**	**RC-848 Display**
DA-98	Same as pre V4 version DA-88	Machine No.
DA-88	DA-88/SY-88 V4 related TC and TC chase functions available when the DA-98 is a slave unit. (Machine ID 2 or higher)	DA-88 Ver.4
DA-38	Same as pre V4 version DA-88 with the addition of the "track copy" function.	DA-38

Operation

Enter menu group "A".
Move cursor to "DeviceType" and press "ENTER".
Press ▲ or ▼ key to select the "DA-98" or "DA-88" or "DA-38".

3) Version Error indication

SYS and SYNC ROM now have ability to check the version each other. In case one detects the other is old to match, DA-98 LCD shows an alert as indicated below.

WARNING!
ROM is too old.
Please use Ver. .
or later

TEAC TECHNICAL INFORMATION

9802R
20th February 1998

TASCAM DA-98, ROM Upgrade (SYS and SYNC V1.20)

Note: This is the revised edition of Technical Information No. 9802. Revised sections are underlined.

SYS ROM (U105) and SYNC ROM (U602) on the System PCB Assy have been changed as indicated below:

	Old	New	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS	V1.00	V1.20	**S002439-00B**	**S0018093** (OTP, M27C512-12C1)
SYNC	V1.06	V1.20	**S002444-00C**	**S0024333** (Rewritable, MBM29F400BA)

Note: **SYS** V1.20 should absolutely be combined with SYNC V1.20 or greater otherwise an alert message will be displayed.
SYNC V1.20 can work on related features and corrections even if SYS version is older than V1.20.

SYS and SYNC V1.20 have been mounted on the products with serial number 0080001 and higher.

1. Problem Correction on SYS and SYNC ROM

When punch out is made by REW on TC slave unit, a part of syllable erasure at out point occurs even on not armed track of pair channel while the other track of pair channel is recorded.
This occurs only when clock reference is selected at internal.

2. Problem Correction on SYS ROM

When locating to MEMO1 or Pre Roll point, unit will not stop but keep FF or REW.
This occurs only when "Resolve on" is selected and locating is operated at the outside of Repeat (MEMO1 - MEMO2 loop) or Automatic Punch In/Out (Pre Roll - Post Roll loop).
If locating at the inside of the loop, no problem occurs.

3. Problem Correction on SYNC ROM

1) Operation with Soundmaster
DA-98 works more reliably in Soundmaster ION Studio Operating Environment.

2) TC chase
a) Rechase window
"Rechase window" function now supported when clock selection is "Internal".

b) Error indication "Can not chase : No tape TC"

During TC chase if the slave unit gets remarkable error on tape timecode, the unit will suddenly stop and show the error message "Cannot chase: No tape TC" in its display. The ability of the DA-98 to recover from this remarkable error without stopping has been resolved.

3) 9 pin

a) Auto edit

Repeating auto edit during preview.
Does not auto edit.
Does not review.

b) Track input monitor

Occasionally a DTRS remote controller can not receive "track input monitor" status from a DA-98 when "Select EE on" or "edit off" (means selected EE off) is selected.

c) Slave unit not changes status

Slave unit does not change its status (slave unit should follow master unit) when master unit receives "full EE on" or "select EE on" command via 9pin.

d) Track arm status

Does not send back the right "track arm status" via 9pin.

4) Video clock

Unit may freeze when a video input signal greater than 1Vp-p is received.

5) Fs shift

~~Slave~~ unit will not lock (will not go into PLAY even ABS differential is "0") during TC chase pull down mode.

6) MIDI

a) Track arming via MMC

Cannot arm tracks via MMC commands from E-magic Logic Audio V2.6.

b) MTC output

Minimised the tendency of the MTC output to drift.

7) DTRS Remote controller

a) Sin osc on

Cannot receive the "sin osc on" command from a DTRS remote controller during stop.

b) TC generator

DA-88's timecode generator cannot be turned off when it it slaving to a DA-98 master.

c) Resolve on

Slave unit could not receive the following settings from master unit during power up or when the master's settings were changed.

rechase mode: free/rechase
rechase window: 1 sec./2 sec
error bypass: 10 F/30
resolve: off/on
resolve mode: free/resync
TC frame mode

New Functions on SYS and SYNC ROM

1) Clock mode: Within this new function " **Auto** " and " **Individual** " selections are available.

Note: Only **Auto** mode was embedded with the former version, hence there was no menu.

Auto: When using multiple DA-98's, the clock source of slave DA-98's will be automatically selected as indicated below.

	Master DA-98	**Slave DA-98**
Time mode = ABS	All clock sources	S-word*
Time mode = TC	Internal	Internal
	Video or Word	S-word*

*S-word : The clock is received from the master DA-98 via the PW-88S cable.

Individual: When using multiple DA-98's, the clock source of each ***individual*** slave DA-98 can be selected manually (like DA-88 version 4) as indicated below.

	Master DA-98	**Slave DA-98**
Time mode = ABS	All clock sources	S-word*
Time mode = TC	Internal	Any clock source can be selected by each individual DA-98
	Video	
	Word	

*S-word : The clock is received from the master DA-98 via the PW-88S cable.

Operation

Enter menu group "A".
Move the cursor to "Clk Mode" and press "ENTER".
Press the ▲ or ▼ key to select the "Auto" or " Individual" mode.

CAUTION

Upon formatting or recording, pay attention for the unified clock source thought out the DA-98 in "Individual" selection otherwise incompatibility may result.

2) Device Type

When the "MACHINE" key followed by a numeric key (1 corresponding to the MASTER machine, 2 to Slave 2 etc.) is pressed on the RC-848, a "Device Type" is displayed in the green LCD screen (ex. DA-88 Ver. 4 or DA-38). The RC-848 also understands functions that are "unique" to a particular "Device Type". The RC-848 could not recognize the DA-98's "Device Type". Based on the "Device Type" selection, what will be recognized by the RC-848 is indicated in the chart below.

Device Type	**RC-848 Recognition**	**RC-848 Display**
DA-98	Same as pre V4 version DA-88	Machine No.
DA-88	DA-88/SY-88 V4 related TC and TC chase functions available when the DA-98 is a slave unit. (Machine ID 2 or higher)	DA-88 Ver.4
DA-38	Same as pre V4 version DA-88 with the addition of the "track copy" function.	DA-38

Operation

Enter menu group "A".
Move cursor to "DeviceType" and press "ENTER".
Press ▲ or ▼ key to select the "DA-98" or "DA-88" or "DA-38".

3) Version Error indication

SYS and SYNC ROM now have ability to check the version each other. In case one detects the other is old to match, DA-98 LCD shows an alert as indicated below.

WARNING!
ROM is too old.
Please use Ver. .
or later

TEAC **TECHNICAL INFORMATION**

9802R
20th February 1998

TASCAM DA-98, ROM Upgrade (SYS and SYNC V1.20)

Note: This is the revised edition of Technical Information No. 9802. Revised sections are underlined.

SYS ROM (U105) and SYNC ROM (U602) on the System PCB Assy have been changed as indicated below:

	Old	New	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS	V1.00	V1.20	**S002439-00B**	**S0018093** (OTP, M27C512-12C1)
SYNC	V1.06	V1.20	**S002444-00C**	**S0024333** (Rewritable, MBM29F400BA)

Note: **SYS** V1.20 should absolutely be combined with SYNC V1.20 or greater otherwise an alert message will be displayed.
SYNC V1.20 can work on related features and corrections even if SYS version is older than V1.20.

SYS and SYNC V1.20 have been mounted on the products with serial number 0080001 and higher.

1. Problem Correction on SYS and SYNC ROM

When punch out is made by REW on TC slave unit, a part of syllable erasure at out point occurs even on not armed track of pair channel while the other track of pair channel is recorded.
This occurs only when clock reference is selected at internal.

2. Problem Correction on SYS ROM

When locating to MEMO1 or Pre Roll point, unit will not stop but keep FF or REW.
This occurs only when "Resolve on" is selected and locating is operated at the outside of Repeat (MEMO1 - MEMO2 loop) or Automatic Punch In/Out (Pre Roll - Post Roll loop).
If locating at the inside of the loop, no problem occurs.

3. Problem Correction on SYNC ROM

1) Operation with Soundmaster
DA-98 works more reliably in Soundmaster ION Studio Operating Environment.

2) TC chase
a) Rechase window
"Rechase window" function now supported when clock selection is "Internal".

b) Error indication "Can not chase : No tape TC"

During TC chase if the slave unit gets remarkable error on tape timecode, the unit will suddenly stop and show the error message "Cannot chase: No tape TC" in its display. The ability of the DA-98 to recover from this remarkable error without stopping has been resolved.

3) 9 pin

a) Auto edit

Repeating auto edit during preview.
Does not auto edit.
Does not review.

b) Track input monitor

Occasionally a DTRS remote controller can not receive "track input monitor" status from a DA-98 when "Select EE on" or "edit off" (means selected EE off) is selected.

c) Slave unit not changes status

Slave unit does not change its status (slave unit should follow master unit) when master unit receives "full EE on" or "select EE on" command via 9pin.

d) Track arm status

Does not send back the right "track arm status" via 9pin.

4) Video clock

Unit may freeze when a video input signal greater than 1Vp-p is received.

5) Fs shift

~~Slave~~ unit will not lock (will not go into PLAY even ABS differential is "0") during TC chase pull down mode.

6) MIDI

a) Track arming via MMC

Cannot arm tracks via MMC commands from E-magic Logic Audio V2.6.

b) MTC output

Minimised the tendency of the MTC output to drift.

7) DTRS Remote controller

a) Sin osc on

Cannot receive the "sin osc on" command from a DTRS remote controller during stop.

b) TC generator

DA-88's timecode generator cannot be turned off when it it slaving to a DA-98 master.

c) Resolve on

Slave unit could not receive the following settings from master unit during power up or when the master's settings were changed.

rechase mode: free/rechase
rechase window: 1 sec./2 sec
error bypass: 10 F/30
resolve: off/on
resolve mode: free/resync
TC frame mode

The following describe the new functions for the TASCAM DA-98 DTRS recorder, ROM upgrade V1.20.

1 – Clock mode

This new function allows you to set an Individual clock mode on slave DA-98 units, meaning that different units in a chain of DA-98 units can use independent reference clocks when TC time mode is selected

NOTE

Whenever we refer to "DTRS sync", we refer to the clock carried over the PW-88S cable, which connects the **SYNC OUT** and **REMOTE IN/SYNC IN** connectors in a chain of DA-98 units. See section 9.1 of the DA-98 manual for details of these connections.

1.1 Auto mode

When a slave unit is set in this mode, it emulates the behavior of pre-V1.20 DA-98 units

Slave unit's Time Mode	Master DA-98	Slave DA-98 units
ABS	All clock sources	DTRS sync
TC	Internal	Internal
	Video or Word sync	DTRS sync

1.2 Individual mode

Slave unit's Time Mode	Master DA-98	Slave DA-98 units
ABS	All clock sources	DTRS sync
TC		INT, WORD or VIDEO

The main point of the Individual mode is that when the Time Mode of a slave unit is set to TC, that slave unit is now free to use any clock source.

1.3 Making the setting

1) Select menu group A and press ENTER.

2) Select `Clk Mode` and press ENTER.

3) Select either `Auto` or `Individual`, using the UP and DOWN keys.

NOTE

When you are performing formatting or recording operations, you should not use the individual mode to select different reference clocks for the different units in the chain. At these times, all units must be synchronized using the DTRS sync carried over the PW-88S cables.

2 – Device Type

The upgrade to the ROM now enables a DA-98 unit to "emulate" one of three possible units when interrogated by a RC-848 Remote Control Unit, when the **MACHINE** key followed by a number key is pressed on the RC-848.

The DA-98 menu allows the setting of three values:

Value	How recognized	RC-848 display shows
`DA-98`	DA-88 (pre-V4)	The machine number
`DA-88`	DA-88 V4 with SY88. All timecode and timecode chase functions available when ID is 2 or above (DA-98 is a slave unit)	DA-88 Ver.4
`DA-38`	DA-88 (pre V4), but with Track Copy function available	DA-38

NOTE

None of these emulations provides control of all DA-98 facilities from a RC-848 Remote Control Unit. If you need more complete remote control of DA-98 functions, we recommend the use of an RC-898 Remote Control Unit.

2.1 Making the setting

1) Select menu group A and press ENTER.

2) Select `DeviceType` and press ENTER.

3) Select `DA-98`, `DA-88` or `DA-38` using the UP or DOWN keys.

TEAC TECHNICAL INFORMATION

9808
6th March 1998

TASCAM DA-98, Clearing Drum Time

Strictly Confidential

Drum time and times of cleaning can be cleared and newly registered by the following procedure.

1 Enter the DA-98 test mode with referring to 2-3, page 6, service manual.
2 Hold SHIFT + UP + DOWN in order.
3 Move the arrow mark to "RAM Clear".
4 Press SHIFT. SHIFT LED blinks.
5 Hold SHIFT + ESCAPE + ENTER in order. At this time, LCD indication does not change.
6 Press ENTER then "External RAM Clear Ready ?" is indicated.
7 Keep pressing UP for about 2 seconds. Then RAM is cleared.
8 If drum time and times of cleaning are required to be stored, use LEFT and RIGHT to move the cursor and use UP and DOWN to input desired values.
9 Turn the power off.

TEAC TECHNICAL INFORMATION

9815

TASCAM DA-98, VIDEO Unlock

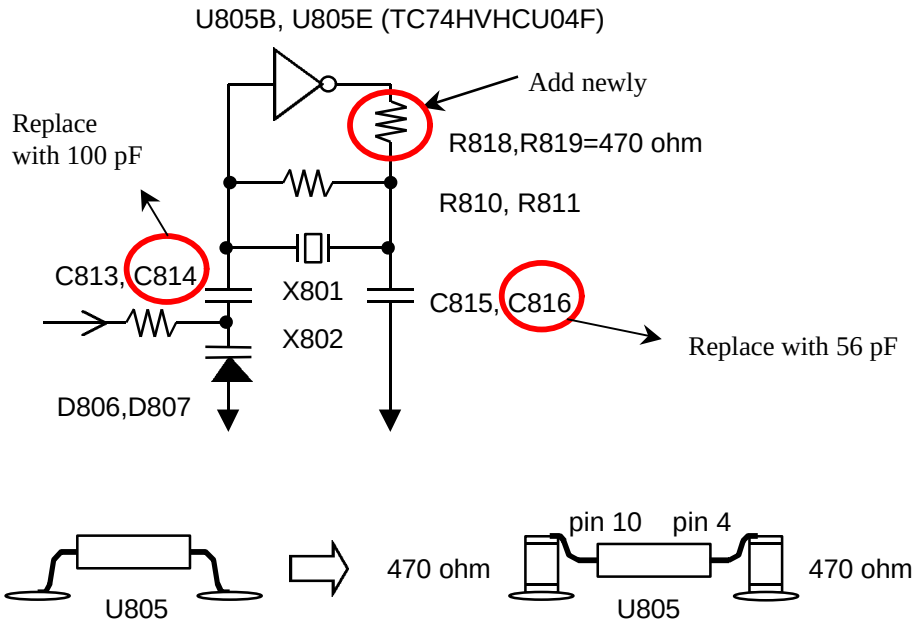
8th April 1998

When the VIDEO is selected for the clock master, there is a possibility that the unit cannot synchronize the external video clock. This causes following:

1 Long chase lock up time or cannot lock.
2 Fluttering audio or mute.

When such is experienced, performing following changes on the SYS PCB Assy is suggested.

Change 1: Replace C816 (100 pF) with 56 pF, ceramic capacitor, **P/No.C0004004**.
Change 2: Replace C814 (220 pF) with 100 pF, ceramic capacitor, **P/No. C0004064**.
Change 3: Newly add R818 and R819, 470 ohm, **P/No. 11152471**.



* Lift U805-4/10 up then insert 470 ohm there.

Change 1 & 2 have been applied on all products with S/No. 0080001 and higher.

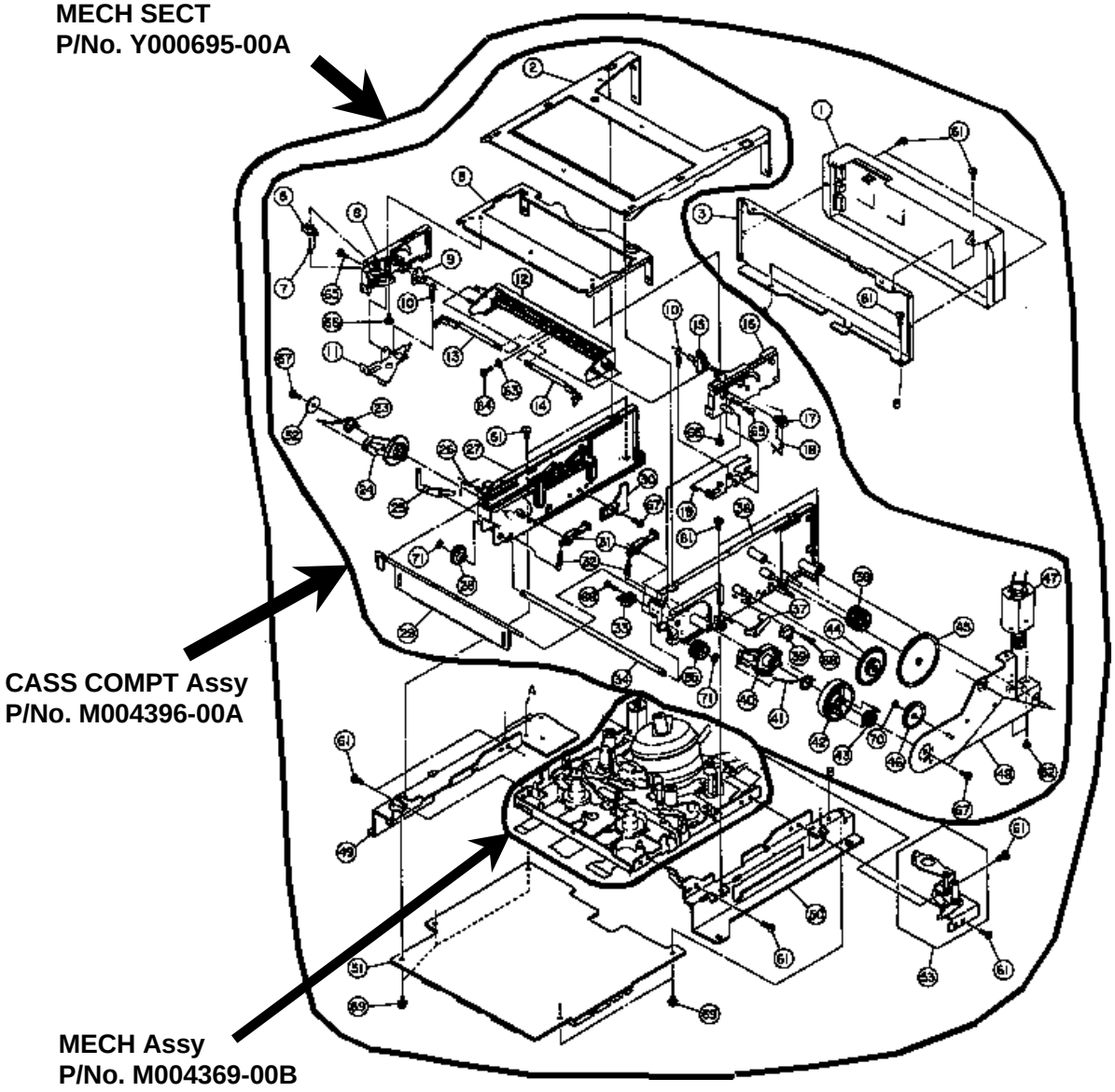
On the production line, video PLL circuit has been checked from the products S/No.0080001 and higher. If no problem found, R818 and R819 are not mounted.

TEAC TECHNICAL INFORMATION

TASCAM DA-98, Mechanism Assy

No. **9824**
DATE 5th June 1998

The following are available as spare parts.



TEAC **TECHNICAL INFORMATION**

TASCAM DA-98HR/DA-78HR, Change of Drum Assy

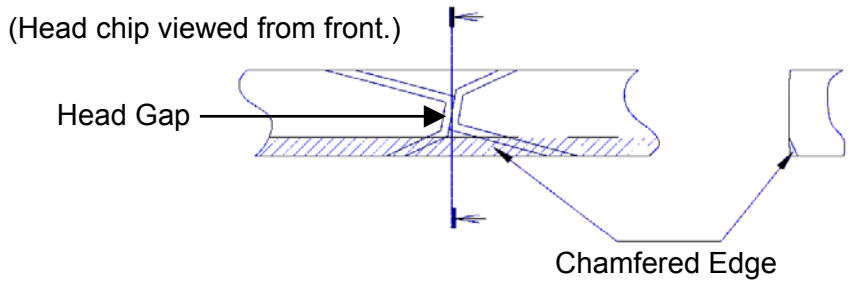
No. **0313**
DATE 12th June 2003

Drum Assy of DA-98HR/DA-78HR has been changed as follows:

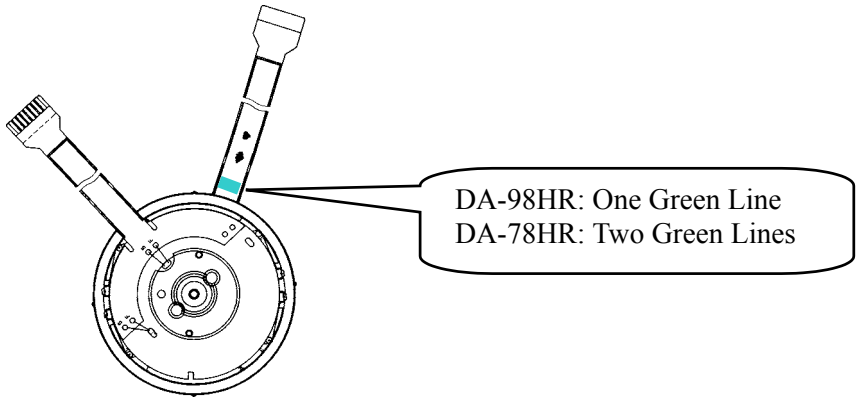
	P/N (former)	**P/N (new)**	S/N Enforced
DA-98HR	M011011-00A (Drum Assy, 98HR)	**M011011-10A** **(Drum Assy, 98HR-10)**	0140001 and up
DA-78HR	M009210-01A (Drum Assy, HR-01)	**M009210-10A** **(Drum Assy, HR-10)**	0240001 and up

Notice: On DA-78HR, in case M009210-00A (*) is replaced with the new one, M009210-10A (Drum Assy, HR-10), Servo PCB Assy (-00A) should be replaced with one (-00B) simultaneously. See Tech Info 0021R.
* M009210-00A (Drum Assy, HR) is former one of M009210-01A (Drum Assy, HR-01).
Note: On DS-D98, the new Drum Assy of DA-98HR has been adopted from S/N 0010001 and up.

In case the former head, error rate may go worse and PB CONDITION LED may light up frequently under low humidity condition. To solve the phenomenon, lower edge of head chip has been chamfered to improve tape contact with around head gap as follows:



The new head can be identified visually as follows:



Following the change of the Drum Assy, P/N of Mech Assy has been changed for spare parts order.

	P/N (former)	**P/N (new)**
DA-98HR	M011063-00A (Mech Assy, DA-98HR)	**M011063-10A** **(Mech Assy, DA-98HR-10)**
DA-78HR	M009273-00B (Mech Assy, DTRS HR)	**M009273-10B** **(Mech Assy, DTRS HR-10)**

TEAC **TECHNICAL INFORMATION**

TASCAM DA-38/88/98, Changes on Mechanism (S-Err 08/31)

No. **9917**
DATE 2nd July 1999

Various changes on the reel section have been made step by step as follows.
All changes intend to reduce the possibilities for S-Err 08/31.

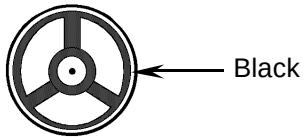
1. Reel Clutch Torq

S & T Reel Base Assy have been changed so that clutch torque becomes more stable.
Note: Only T Reel Base Assy has been changed once again on the item 3.

	Old	New
S Reel Base Assy	17061086-00	M006071-00A
T Reel Base Assy	17061087-00	M006072-00A

Change has been made on:
DA-38 S/No. 0150001 and higher
DA-88 S/No. 0580001 and higher
DA-98 S/No. 0070001 and higher

New Reel Base Assy



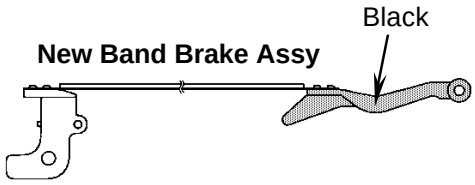
2. Band Brake

Felt pad of some Band Brake Assy's was slightly thick causing that Soft Brake touches the S Reel Base. Thickness of the felt pad has been secured.

	Old	New
Band Brake Assy	17968214-00	M008223-00A

Change has been made on:
DA-38 S/No. 0250001 and higher
DA-88 30/Sep/98 and after
DA-98 S/No. 0110001 and higher

New Band Brake Assy



3. Tape Slack

Tape slack may occur when FF/REW → STOP is operated with following tapes.
maxell P5-90HMBQ / AMPEX 488H-113 / 3M P5-60HXP

Clutch torq for S & T Brake Assy and T Reel Base Assy have been slightly tuned.
Note: There is no identification color or mark on them.

	Old	New
T Reel Base Assy	M006072-00A	M006072-00B
S Brake Assy	17698203-00	M008776-00A
T Brake Assy	17968205-00	M008777-00A

Change has been made on:
DA-38 S/No. 0320001 and higher
DA-88 20/Apr/99 and after
DA-98 S/No. 0150001 and higher

TECHNICAL INFORMATION

TASCAM DA-38/88/98, Changes on Mechanism (S-Err 08/31)

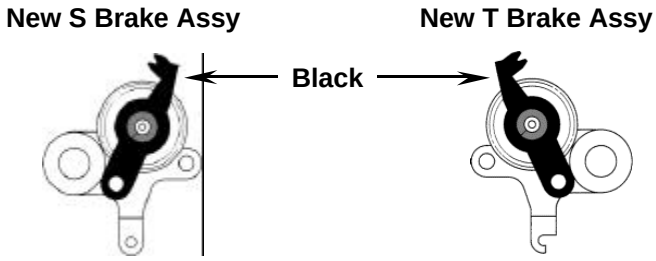
No.	**9917R**
DATE	22nd July 1999

This is an additional information for item 3 of Tech-Info No. 9917.

3. Tape Slack

Clutch torq for S & T Brake Assy has been changed from 45 gf to 20 gf.
Thickness of a magnet mounted on T Reel Base Assy has been changed from 1.39 to 1.45 mm.

~~Note: There is no identification color or mark on them.~~

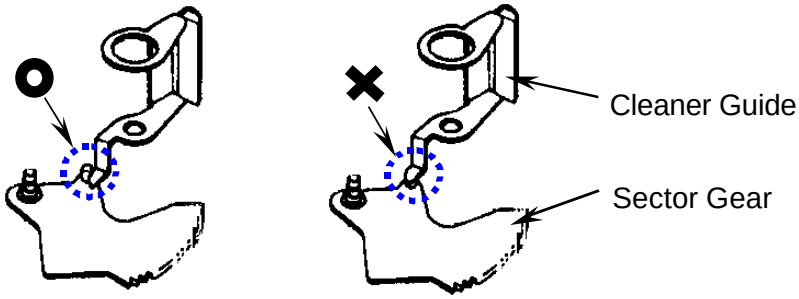


TECHNICAL INFORMATION

TASCAM DA-38/88/98, Impedance Roller Height Adjustment

No.	**9918**
DATE	22nd July 1999

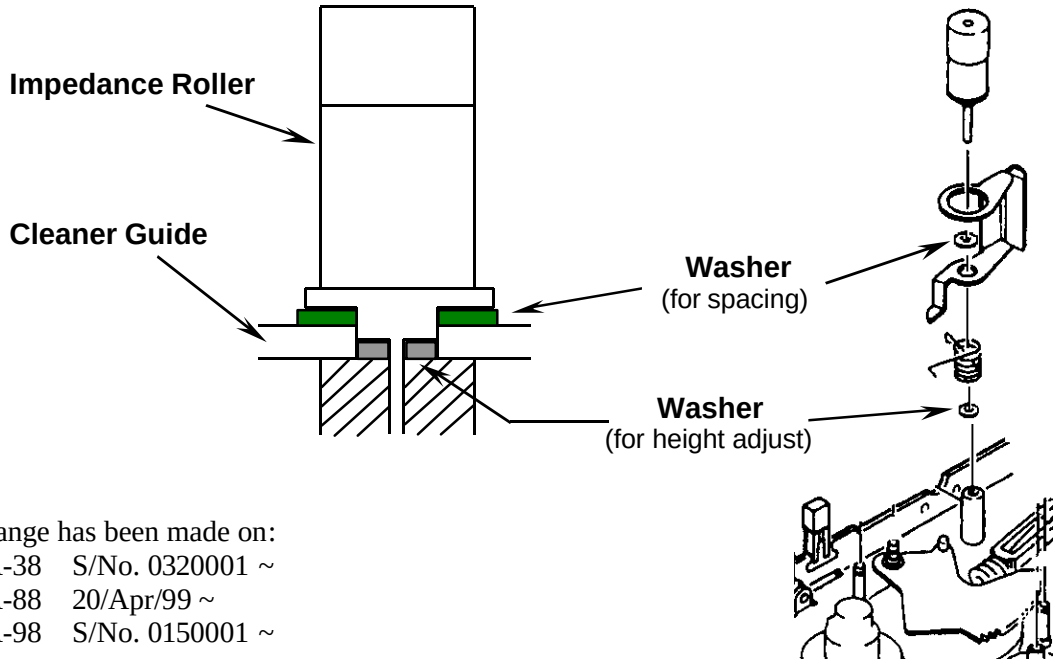
A washer (Procedure 4-6-1, DA-38/98 service manual) has been used to adjust the height of impedance roller. If thicker one is used, there is a possibility that a lever of cleaner guide and a pin of sector gear do not engage causing incomplete tape loading.



To fix the height of cleaner guide uniformly, three pairs of washer have been newly used.

	Pair 1	Pair 2	Pair 3
Washer (for spacing)	M0090660 (3.85×6×t0.2)	M0090670 (3.85×6×t0.25)	M0090680 (3.85×6×t0.3)
Washer (for height adjust)	M0090610 (1.63×3×t0.13)	M0090620 (1.63×3×t0.2)	M0090630 (1.63×3×t0.25)

Notice: Do not mix different pairs.



Change has been made on:
DA-38 S/No. 0320001 ~
DA-88 20/Apr/99 ~
DA-98 S/No. 0150001 ~

TEAC

TECHNICAL INFORMATION

TASCAM DA-98, ROM Upgrade (SYS and SYNC V2.00)

No. **9922**
DATE 3rd September 1999

SYS ROM (U105) and SYNC ROM (U602) on the System PCB Assy have been upgraded on the products with serial number 0150001 and higher.

	Old	New	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS	V1.20	V2.00	**S002439-00C**	**S0018093** (OTP, M27C512-12C1)
SYNC	V1.20	V2.00	**S002444-00D**	**S0024333** (Rewritable, MBM29F400BA)

Note: Both of SYS and SYNC ROM should be upgraded to V2.00 simultaneously.

New Features

Refer to DA-98 V2.00 update attached in the following page.

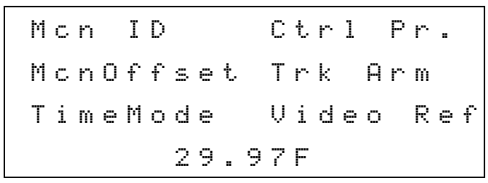
Sheet, V2.00 (English) **P/No. D004952-00A**
Sheet, V2.00 (French/German/Italian/Spanish) **P/No. D004953-00A**

A number of new features have been added and changes have been made to the DA-98 software version 2.00. These are described in this leaflet.

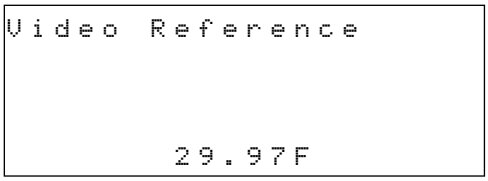
Please keep this sheet in the folder with your DA-98 manual for reference.

1 Video Reference

When syncing the DA-98 to a video frame source, it may be useful to specify the frame rate of the video source, in order to assist the synchronization process. A new menu item, `Video Ref`, has therefore been added to menu group 3:



1 **With menu group 3 displayed, move the cursor to `Video Ref` and press ENTER:**

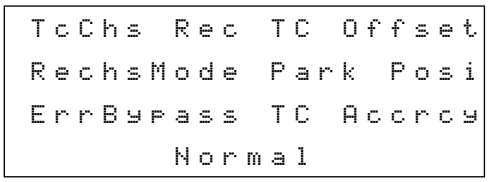


2 **Use the UP and DOWN keys to choose one of the following options: `Auto`, `30F`, `29.97F`, `25F` and `24F`.**

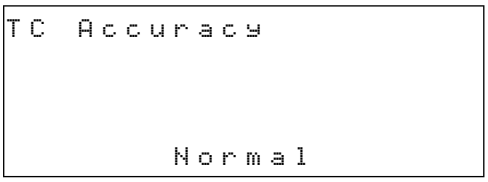
The `Auto` option automatically detects and synchronizes to the incoming video frame rate. This is the same as in pre-2.00 DA-98s. The other options force the DA-98 to attempt synchronization to the specified video frame rate.

2 Timecode Accuracy

The range within which the DA-98 will sync to incoming timecode can be set with a new menu item, `TC Accrcy`, in menu group 4:



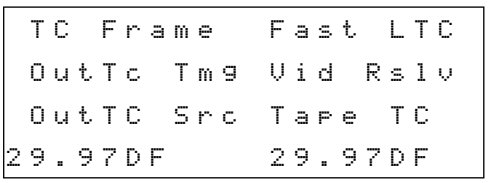
1 **With menu group 4 displayed, move the cursor to `TC Accrcy`, and press ENTER:**



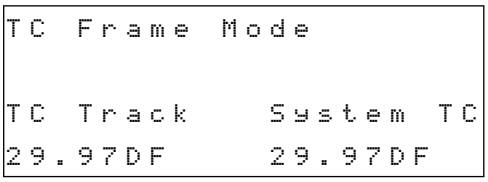
2 **Use the UP and DOWN keys to select either `Normal` (equivalent to the setting on pre-2.00 DA-98s) or `Wide`, allowing slightly wider tolerance in the sync range.**

3 TC Frame Mode

The system timecode frame rate screen, as described in 10.3 “Setting the frame rate” of the DA-98 manual, can now also be used to display the current tape stripe format:



1 **With menu group 5 displayed, move the cursor to `TC Frame`, and press ENTER:**

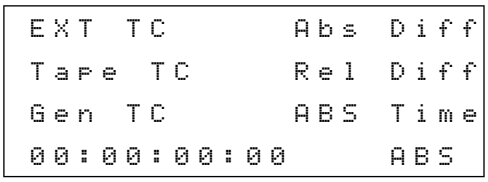


2 **Use the LEFT and RIGHT keys to move the cursor, and the UP and DOWN keys to change the system timecode value, as shown under the `System TC` on the display.**

4 ABS Time display

In addition to the external timecode, tape timecode, etc. which are shown in menu group E, it is now possible to view the ABS time, even when TC timing is selected (see section 10.1 of the manual).

1 **Bring up menu group E, and move the cursor to the new menu item,** `ABS Time:`



The ABS tape time will be shown on the bottom line of the display, together with the word `ABS` **(no timecode time is applicable here, obviously).**

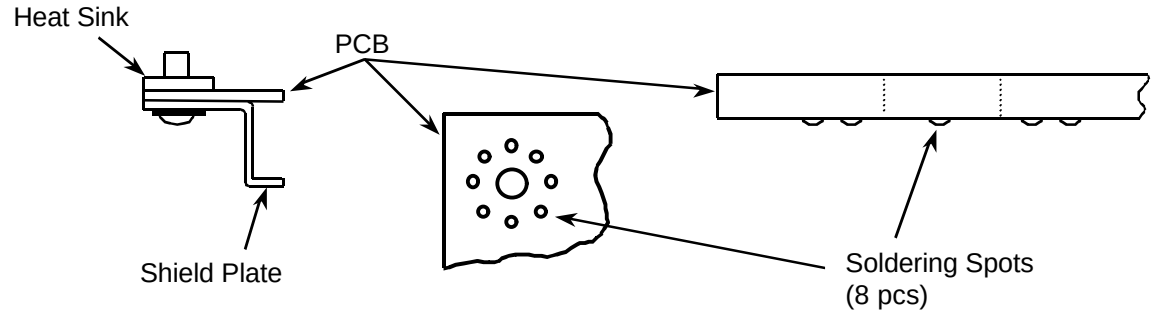
TECHNICAL INFORMATION

TASCAM DA-98, Faulty Playback Error Rate for B Head

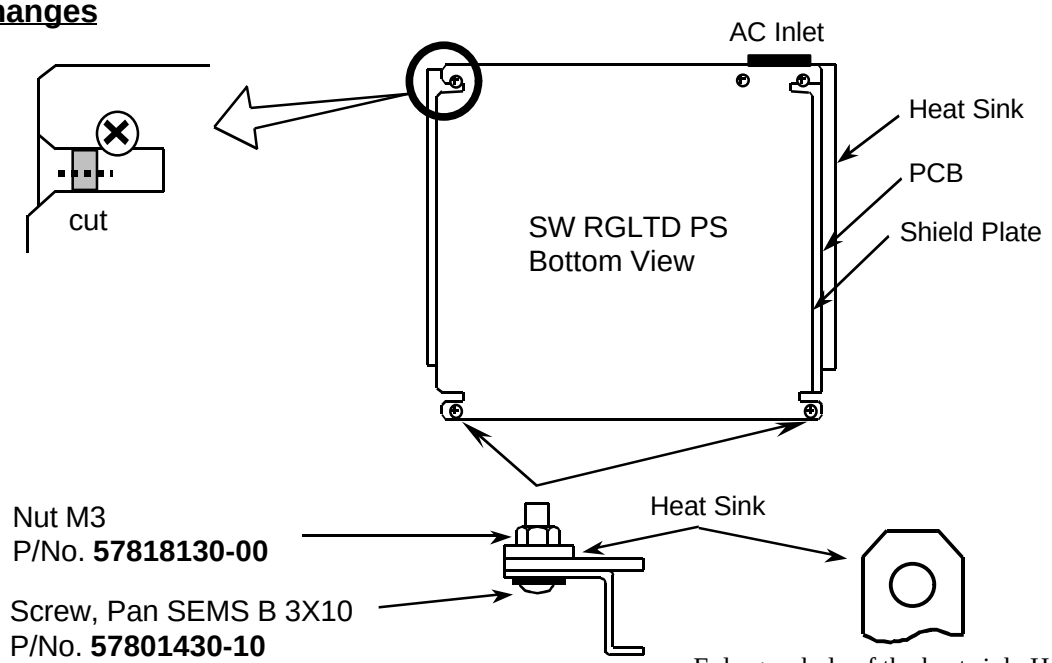
No. **9925**
DATE 15th October 1999

Symptom: Playback error rate for the B head does not satisfy the specification.
Cause: During the transportation, soldering spots on the PCB of the SW RGLTD PS (Ref 1-15) become flat. This causes that screws fixing shield plate, PCB and heat sink loosened, affecting the error rate for the B head.
Solution: Using a nut to fix securely at two points. Cutting GND foil at one point.

Original



Changes



Enlarge a hole of the heat sink. Heat sink is made of aluminum then easy to wrench the hole open by rotating a screw over the limit.

Same changes have been made on the products with S/No. 0150001 and higher.

TEAC

TECHNICAL INFORMATION

TASCAM DA-38/78HR/98, No Drum Time Counting

No. **0001**
DATE 28th March 2000

Symptom: There is a possibility that drum time is erratic or not counted.

Cause: EEPROM (U904 on the Servo PCB Assy) that stores drum time has been changed once on the following products.

DA-38:	S/No. 310113 and up (totally 200 units)
DA-78HR:	S/No. 0010001 to 0049999
DA-98:	S/No. 150001 and up

Original is ST93C46 (P/No. S0002483). New one is M93C46-MN6T (P/No. S0033414). However, with new one, there is a possibility for erratic or no drum time counting.

Solution: Replace new one with original one.

DA-78HR S/No. up to 0049999 in Tokyo stock have been reworked and "D" mark have been stamped on the carton.
All products with S/No. 0050001 and higher have ST93C46 (P/No. S0002483) mounted.

TEAC **TECHNICAL INFORMATION**

TASCAM DA-98HR, ROM Upgrade (SYS V1.02)

No. **0029**
DATE 19th December 2000

SYS ROM, U011 on the SYS PCB Assy has been upgraded from V1.00 to V1.02 on the products with S/No. 0070001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.02	**S003967-00B**	**S0035153**, IC, MBM29F800BA-70PF

Refer to V 1.02 supplemental owner's manual for newly added features.

Problems corrected by V1.02

1. When saving settings to tape, if REC function keys or TC REC are set ON, recording on those tracks are also performed falsely.
2. Problem on TDIF E bit. Refer to below.

Introduction of TDIF E bit

DA-98HR can record and playback at 2X and 4X sampling frequencies: 88.2 kHz and 176.4 kHz, and 96 kHz and 192 kHz. To declare those track Fs information through TDIF, two bits (originally reserved) are newly defined. These bits are named "E bit".

Problem

There are some machines in the market that send wrong information in E bit such as DA-88 and YAMAHA O2R. If those machines are connected, the DA-98HR shows following message even if the Fs on both are the same.

> WARNING !
> Fs unmatched

Solution

With the DA-98HR SYS V1.02, new menu has been added. Refer to the supplemental owner's manual for V1.02 for more details.

menu group	B	
submenu	TDIF E bit	
parameter	Normal (default)	DA-98HR looks at E bit
	No Warning	DA-98HR ignores E bit

Notice: As mentioned in the supplemental owner's manual, if TDIF E bit is set "No Warning", DA-98HR can record the TDIF signal that does not suit to the setting of the tape loaded. Take very care of that and warn customers.

TEAC TECHNICAL INFORMATION

TASCAM RC-898, ROM Upgrade (Main V2.00)

No. **0031**
DATE 19th December 2000

To support DA-78HR and DA-98HR, Main ROM, U28 and U55 on the Main PCB Assy have been upgraded from V1.00 to V2.00 on the products with S/No. 0100001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
V2.00 (U28)	**S002772-00B**	**S0027740,** IC, M27C1001-100 C1
V2.00 (U55)	**S002898-00B**	**S0027740,** IC, M27C1001-100 C1

Note:

1. When RC-898 V2.00 is used,
   DA-78HR should be upgraded to V1.13 or higher. See Tech-Info No. 0030
   DA-98HR should be upgraded to V1.02 or higher. See Tech-Info No. 0029

2. User setup data (Menu F/Setup) is incompatible between V1.00 and V2.00. If the data saved by V1.00 is loaded by V2.00, there may be a possibility that the data is read incorrectly. To avoid this, memory should be cleared after ROM replacement. Before memory clear, explain and get permission from customer that user setup data will be lost completely,

1) Connect the RC-898 to DTRS master unit with remote cable.
2) Hold PRESET and ↑ then turn the power on. LCD shows following:

```
 Memory Clear
Push SELECT Key
```

3) Press PRESET.

TECHNICAL INFORMATION

TASCAM DA-98HR, Low Battery

No. **0109**
DATE 31st May 2001

Following message will be displayed earlier than expected.

```
WARNING !
low battery
```

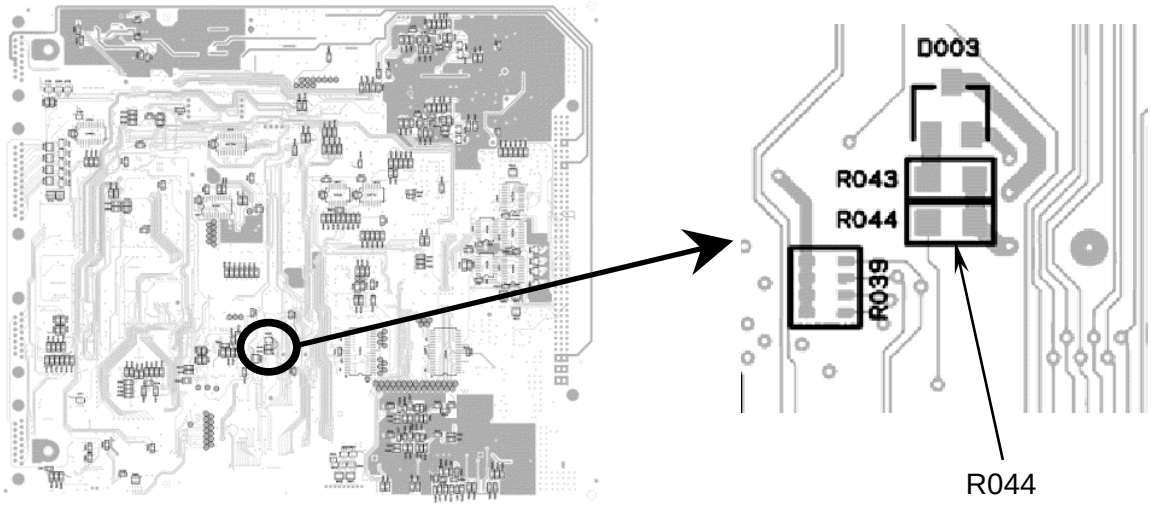
The cause is R044 on the SYS PCB Assy. The small resistor value can cause the battery (BT001) to drain prematurely.

To decrease the current, R044 (100 kΩ) has been changed to 1 MΩ, **P/No. 11152105** on the products with S/No. 0090001 and higher.

After R044 is replaced, it is suggested to also replace the battery with new one. The type of the battery is CR2032 which is a very common battery available at most electronic parts supply.

Note:
1. The battery is only being used when the unit is powered off, so the longer a DA-78HR or DA-98HR sits in a box waiting to be purchased, the shorter the life of the battery will be.
2. Even if the battery has come to its life, drum hours are not cleared as it is memorized on the Servo PCB Assy. Only standard work settings will be lost. Until the battery is replaced with new one, it is suggested to store and load settings to and from tape.
   Refer to the owner's manual, 12.5 Tape storage of settings

SYS PCB Assy (bottom side)



TEAC **TECHNICAL INFORMATION**

TASCAM DA-98HR, Reference Level of IF-AN98HR

No. **0116**
DATE 24th August 2001

This information introduces how to convert the reference level to– 11 dBFS or– 14 dBFS.

* – 11 dBFS (full-scale +15 dBu): Mainly for German, Holland, Belgium
* – 14 dBFS (full-scale +18 dBu): Mainly for North EUR, UK

Replace the resistors as follows:

	AD Board R081–R088, R091–R098	DA Board R121–R128
–11 dBFS	3.9 kΩ	1.3 kΩ
–14 dBFS	6.2 kΩ	3.3 kΩ

Notice:

1) Above change should be done while jumpers on boards are set at – 16 dBFS (factory preset).
2) If above change is done, original – 16 dBFS,– 18 dBFS and– 20 dBFS are becomes invalid.

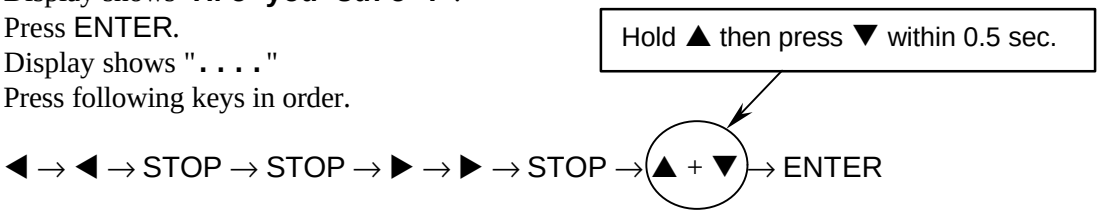
TEAC **TECHNICAL INFORMATION**

TASCAM DA-98HR, Clearing the Drum Time

No. **0119**
DATE 26th September 2001

Strictly Confidential

1. Enter the DA-98HR test mode. See 2-1, page 7, service manual.
2. Go to MENU M/NvRAM Clr.
3. Press ENTER
4. Display shows "**`Are you sure ?`**".
5. Press ENTER.
6. Display shows "**`....`**"
7. Press following keys in order.



Note: In case keys are not pressed correctly, display returns to "Are you sure?".

8. Now data are cleared. Also desired number can be entered by using CURSOR keys.

```
NV RAM Clear

  Clan  DrTtl DrSrch
  0000  0000  0000
```

9. Turn the power off.

TEAC **TECHNICAL INFORMATION**

TASCAM DA-98HR, ROM Upgrade (SYS V1.45)

No. **0123**
DATE 8th November 2001

SYS ROM, U011 on the SYS PCB Assy has been upgraded from V1.02 to V1.45 on the products with S/No. 0110001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.45	**S003967-00D**	**S0035153**, IC, MBM29F800BA-70PF

Problems corrected by SYS V1.42

Note: There are no products that have SYS V1.42 mounted.

[General]

1. After the unit starts playing, TC out may skip 1 frame or repeat the current frame.
2. Locate then play, but unit may not go into play mode.
3. TC and ABS timing is in the play head. Should be in the record head.
4. When internal TC is recorded on the tape without TC, the User Bit will be AAAAAAAA.
5. Master's rechase mode/window is sent to the slave units, but this function is removed because the slave units don't always want it.
6. inPatch LED may be turned on even though set to all digital.
7. Rechase Mode setting is on when ABS chase.
8. Input monitor for each track is supposed to be forced to on while REC, and no button for each input monitor is supposed to work. (like DA-98.)
9. When playing tape reaches to "the point where overwrite format was suspended (that is, "discontinuous format point"), no operation may work (for example, when stop is pressed, LED shows "stop", but unit may continue to play.)
10. PLAY on RC-898 will not blink when it's def'd played from RC-898.
11. Unit may not be located at 0 when format is done.
12. Video Reference, TC Accuracy, and Input TC Timing will return to the default after unit is turned on.

[Soundmaster related]

13. Since DA-98HR has PLL for converter unlike DA-98, it is difficult to control the speed. They changed algorithm on their part to meet the DA-98HR but a few are fixed on DA-98HR too.

[9 pin related]

14. Status information to return to P2 may not be updated even though the mode is changed by some operation from the unit side after unit receives and is working jog command from P2.
15. "Slot PLL not locked" error will happen if the unit is working in speed other than 1x by 9 pin command when I/O board PLL is narrow. Fixed so that it will be forced to "wide."
16. When the unit is in pause mode, the status information to return to 9 pin may not be "still." It will cause the controller not operating.
17. 9 pin shuttle command sometimes may not work in the first try. May work in the second try.
18. Pre-roll time sometimes cannot be set from 9 pin.
19. Fixed so the unit will follow the DMC related command from 9 pin and goes into shuttle mode.
20. When the mode is changed from jog/sht/var to "still," jog/sht/var status is gone, so as a result the status in the controller was changed.
21. Unit sometimes may not pause when received "pause" command during chase locking.
22. Track mapping display "Ana12345678" is wrong. "Ana12341234" is correct. (only display problem.)

Problems corrected by V1.45

[RC-898 related]

1. Reference level is not displayed.
2. TC user bit is not shown.
3. ABS offset sub frame cannot be set.
4. When park position is changed on the unit, it will not be updated on the RC-898.
5. Format may not be started by the RC-898.
6. If, after ABS/TC chase offset is changed from the RC-898, it is changed on the unit, ABS/TC chase offset works based on the value before it is changed from the RC-898.
7. If more than one DTRS machine are used, setting changed on the unit may not be updated on the RC-898.
8. When the format setting is being done, if TRK Fs pattern is kept changing, the display on the unit and the RC-898 may not match.

[Others]

1. When TC is played in different mode from it was recorded, it may show wrong value around 0.
2. After vari is changed A $\rightarrow$ B $\rightarrow$ C, and vari on/off is changed, vari is set to B.

TECHNICAL INFORMATION

TASCAM DS-D98, ROM Upgrade (SYS V1.45)

No. **0124**
DATE 29th November 2001

SYS ROM, U011 on the SYS PCB Assy has been upgraded from original to V1.45 on the products with S/No. 0020001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.45	**S003967-00D**	**S0035153**, IC, MBM29F800BA-70PF

Note:
1. SYS V1.42 is the original of the DS-D98 mounted on the S/No. 0010001 to 0019999.
2. SYS ROM for the DA-98HR and the DS-D98 is the same, compatible.

Problems corrected by V1.45

1. When TC is played in different mode from it was recorded, it may show wrong value around 0.
2. After vari is changed A → B → C, and vari on/off is changed, vari is set to B.

Supporting the new DSD PCB Assy

AD converter on the DSD PCB Assy has been changed from ADMOD79 (ANALOG DEVICES) to PCM1804 (BURR BROWN) on the products with S/No. 0020001 and higher. Reason for this change is that the production of the ADMOD79 has been discontinued.
Therefore, various changes have been made on the DSD PCB Assy to mount the PCM1804.

Note that SYS V1.45 is required to combine with the new DSD PCB Assy. Refer to Tech-Info No. 0125 for the details.

TEAC **TECHNICAL INFORMATION**

TASCAM DS-D98, Change of DSD PCB Assy

No. **0125**
DATE 29th November 2001

DSD PCB Assy has been changed on the products with S/No. 0020001 and higher. Reason for this change is that the original AD converter, ADMOD79 (ANALOG DEVICES) is no longer available. Therefore, PCM1804 (BURR BROWN) is used for the substitution.

Following changes have been made on the DSD PCB Assy to mount the PCM1804.
1. PCB foil pattern.
2. A lot of resistors and capacitors → added/removed.
3. U512, DSD V1.10 (P/No. S004434-00B) → DSD V1.20 (P/No. S004434-00B).

* Basically it is impossible to convert the old (new) DSD PCB Assy to new (old), as there are many differences as listed above.

Old DSD PCB Assy and new can be distinguished visually on the following points:

	AD Converter (U1 on DSD SUB PCB Assy)	DSD Firmware (U512 on DSD PCB Assy)
Old	ADMOD79	V1.10
New	PCM1804	V1.20

Notice:
1. A restriction of SYS/DSD combination.
SYS V1.42 and old DSD PCB Assy cannot be combined. Other ways are ok.

	Old DSD PCB Assy	New DSD PCB Assy
SYS V1.42 (S/No. 0010001~)	O	X
SYS V1.45 (S/No. 0020001~)	O	O

2. Dip-switch setting.
As there is a difference on latency between the ADMOD79 and the PCM1804, it is needed to tell the system control which AD converter is mounted on the DSD PCB Assy.
* On the new DSD PCB Assy, dip-switch SW1-1 should be set “ON”.
* On the old DSD PCB Assy, dip-switch SW1-1 should be set “OFF”.
SYS V1.45 checks above dip-switch setting to set the correct latency. SYS V1.42 does not have this function then the only old DSD PCB Assy should be combined with it.

TECHNICAL INFORMATION

TASCAM DS-D98, Change of DSD/DSD SUB PCB Assy

No. **0125R2**
DATE 26th November 2002

This is the revised edition of Tech-Info No. 0125R to add some information about DSD SUB PCB Assy which has been changed together with DSD PCB Assy.

DSD and DSD SUB PCB Assy have been changed simultaneously on the products with S/N 0020001 and higher as following.

	Old (P/N)	New (P/N)
DSD PCB Assy	E951294-00A	E951294-00B
DSD SUB PCB Assy	E951316-00A	E951316-00B

Notice:
* New (old) DSD PCB Assy must be combined with new (old) DSD SUB PCB Assy.
* Only new DSD and DSD SUB PCB Assy (-00B) are supplied as spare parts.

Reason for this change is that the original AD converter, ADMOD79 (ANALOG DEVICES) is no longer available. Therefore, PCM1804 (BURR BROWN) is used for the substitution.

Following changes have been made on the DSD and DSD SUB PCB Assy to mount the PCM1804.
1. PCB foil pattern.
2. A lot of resistors and capacitors → added/removed.
3. On DSD PCB Assy: U512, DSD V1.10 (P/No. S004434-00B)
→ DSD V1.20 (P/No. S004434-00C).

* Basically it is impossible to convert the old (new) DSD and DSD SUB PCB Assy to new (old), as there are many differences as listed above.

Old DSD and DSD SUB PCB Assy and new can be distinguished visually on the following points:

	DSD PCB Assy		DSD SUB PCB Assy	
	U512 DSD Firmware	P/N printed on PCB	U1 AD Converter	P/N printed on PCB
Old	V1.10	E901294-00A	ADMOD79	E901316-00A
New	V1.20	E901294-00B	PCM1804	E901316-00B

Notice:
1. A restriction of SYS firmware and DSD/DSD SUB PCB Assy combination.
SYS V1.42 and old DSD/DSD SUB PCB Assy cannot be combined. Other ways are ok.

	Old DSD/DSD SUB PCB Assy	New DSD/DSD SUB PCB Assy
SYS V1.42 (S/No. 0010001~)	O	X
SYS V1.45 (S/No. 0020001~)	O	O

2. Dip-switch setting.
As there is a difference on latency between the ADMOD79 and the PCM1804, it is needed to tell the system control which AD converter is mounted on the DSD PCB Assy.
* On the new DSD PCB Assy, dip-switch SW1-1 should be set “ON”.
* On the old DSD PCB Assy, dip-switch SW1-1 should be set “OFF”.
SYS V1.45 checks above dip-switch setting to set the correct latency. SYS V1.42 does not have this function then the only old DSD PCB Assy should be combined with it.

TEAC TECHNICAL INFORMATION

TASCAM RC-898, ROM Upgrade (Main V3.03)

No. **0126**
DATE 29th November 2001

Main ROM, U28 and U55 on the Main PCB Assy have been upgraded from V2.00 to V3.03 on the products with S/No. 0110001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
V3.03 (U28)	**S002772-00C**	**S0027740,** IC, M27C1001-100 C1
V3.03 (U55)	**S002898-00C**	**S0027740,** IC, M27C1001-100 C1

Note:
When RC-898 V3.03 is used,
DA-78HR should be upgraded to V1.13 or higher. See Tech-Info No. 0030.
DA-98HR should be upgraded to V1.45 or higher. See Tech-Info No. 0029.
DS-D98 should be upgraded to V1.45 or higher. See Tech-Info No. 0124.
* RC-898 V3.03 can control the younger version of the DTRS, however, some new functions do not work. Then it is recommended to upgrade the DTRS machines as shown above.

Supporting DS-D98
RC-898 V3.03 can control all functions of the DS-D98.

Problems Corrected by V3.03
1. When Rehearsal or Auto Punch in/out is performed in split mode, DA-98HR chasing external TC will go to CHASE=OFF at the post roll point.
2. Display problem: In “TC Accrcy” menu, indication of Normal/Wider is inversed.
3. Display problem: Track Map “Ana 12345678” is wrong. “12341234” is correct.
4. Output Word Length does not change from 24 bit to 16 bit.
5. Display of Input Patch for the slave unit differs from the DTRS when setup data is loaded from the tape.
6. When the external clock source is disconnected, error message appears on the RC-898. However, this error message does not disappear even if the external clock is re-connected.
7. Display problem: “9pin Rec Mode” is wrong. “9pin Rec Acceptable” is correct.
8. With ON/Off setting (like Trk Arm), “N/A (not available)” may be displayed for machine 1.
9. When ”TC Offset” is changed on the DTRS, indication on the RC-898 does not change.
10. When “Frame Disp” is set OFF, Frame indication blinks momentarily.
11. With DTRS-HR, when TC Offset is changed by sub frame level, OFFSET LED on the RC-898 does not light.
12. When Offset is “-0”, Offset LED lights.

Change of the Feature
1. Supporting the DS-D98 (Format, DSD Digital I/O, DSD Analog Out Filter).
2. Machine Offset is now adjusted by the unit of sub frame.

TEAC TECHNICAL INFORMATION

TASCAM DA-98, ROM Upgrade (SYNC V2.07)

No. **0202**
DATE 1st March 2002

SYNC ROM, U602 on the SYS PCB Assy has been upgraded from V2.00 to V2.07.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYNC V2.07	**S002444-00E**	**S0024333,** MBM29F400BA

Note: There is no product that has SYNC V2.07 mounted as the production had been discontinued.

Problem Corrected by SYNC V2.07

1. Impossible to record/playback the user's bit data included in the incoming external timecode.
2. If the DA-98 receives a speed control command (except 1x) through 9 pin controller, there may be a possibility that:
   2-1 Video Resolve would not work
   2-2 Speed control from the 9 pin controller would not work.
3. If TC Offset is set from the 9 pin controller, wrong number is entered.
4. DA-98 does not go to shuttle mode with 9 pin controller that sends DMC command.
5. During shuttle mode, if the DA-98 receives pause command from the 9 pin controller, communication becomes offline. For instance, pause LED on the 9 pin controller will turn off.
6. In rare occasions, TC reader would freeze if the external TC is disconnected and connected. Real cause of this cannot be found as it is impossible to construct the designing environment for the DA-98 again.
   Therefore, one alternative is added:
   When TC reader freezes, pressing chase key twice will initialize the TC reader.

TEAC **TECHNICAL INFORMATION**

TASCAM DS-D98, ROM Upgrade (DSD V1.21)

No. **0204**
DATE 28th May 2002

DSD ROM, U512 on the DSD PCB Assy has been upgraded from V1.20 to V1.21 on the products with S/No. 0040001 and higher.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
DSD V1.21	**S004434-00D**	**S0031753, MBM29F040C-90PD**

Problem Corrected by V1.21

When the unit is working on the DSD mode, click noise is recorded at the punch in/out point.

Notice:

- This upgrade is effective for only the units (S/No. 0020001 and higher) that have the new DSD PCB Assy.
- Do not mount the DSD V1.20 or V1.21 onto the units (S/No. 0010001 to 0019999) that have the old DSD PCB Assy.
- Refer to Tech-Info No. 0125R for the details of the old and the new DSD PCB Assy.

TECHNICAL INFORMATION

TASCAM DA-98HR/DS-D98, ROM Upgrade (SYS V1.46)

No. **0207**
DATE 21st June 2002

SYS ROM, U011 on the SYS PCB Assy has been upgraded from V1.45 to V1.46 on the following products.

- DA-98HR: S/No. 0120001 and higher
- DS-D98: S/No. 0040001 and higher
- Tokyo stock with "M146" sticker on the carton box.

	P/No. (PGMed ROM)	P/No. (Blank ROM)
SYS V1.46	**S003967-00E**	**S0035153**, IC, MBM29F800BA-70PF

Problem corrected by SYS V1.46

In the chain of DTRS, following occurs.
1. "INPUT MONITOR" on the slave units cannot be operated by the RC-898 correctly.
2. Status of "INPUT MONITOR" of the slave units cannot be displayed on the RC-898 correctly.

Note:
- Above symptom occurs when the master unit has SYS V1.42 or V1.45.
- If the master unit has SYS V1.46, no problem occurs. Version of the slave units does not matter.

TEAC TECHNICAL INFORMATION

TASCAM DS-D98/DA-98HR, Front/Sys MPU Change (Front V1.11/Sys V1.52)

No. **0301**
DATE 16th January 2003

Front and Sys MPU have been changed as follows:

	Current		New		Enforcement
	Ver.	P/N	**Ver.**	**P/N**	
Front MPU	V1.10	S003841-00B	**V1.11**	**S003841-00C**	**DS-D98: S/N 0050001 and up** **DA-98HR: S/N 0150001 and up**
Sys MPU	V1.46	S003967-00E	**V1.52**	**S003967-00F**	**Ditto**

Tokyo stock has been reworked to change only Sys MPU with V1.52. The reworked units have "2N" mark on carton box. Refer to description of Front V1.11 Problem Fixed about reason of changing only Sys MPU upon the rework.

=== Front V1.11 ===

Problem Fixed

Automatic recovery function doesn't operate correctly when an error is found in communication between System MPU and Front's.

Note:
In case the error is found on former Front MPU, unit may show erratic LED lighting that has been absolutely solved by Sys V1.52. This is just for improving reliability of the solution of the erratic LED lighting for future production. Thus, it is needless to replace Front MPU with V1.11 upon your servicing,

=== Sys V1.52 ===

Note:
* Following description, 1) to 8), shows fixed problems from Sys V1.46 to V1.52.
* The V1.46 is the current Sys firmware officially released however some units of DA-98HR have been shipped with the V1.47. S/N 0130001 to 0149999 of DA-98HR have equipped the V1.47.
* The V1.47 hasn't been registered officially thus P/N has been changed for spare parts order as follows:
  Current (Sys V1.46): S003967-00E
  New (Sys V1.52) : S003967-00F
* Following problem 1) and 2) have been fixed by the V1.47.

Problems Fixed

1) Jitter of TC output goes worse momentarily every approx. 2 hours 20 minuets after unit is turned on. This occurs in both using internal TC Generator and playing Tape TC. Slave machine receiving the TC from DS-D98/DA-98HR may not read the TC or escape from chase at the point.

Note: This occurs every approx. 2 hours 20 minuets after powering on, not depends on tape play time. This means that the problem is not avoidable by using 60 minuets length tape, for example.

2) In Video Resolve ON state, Video Resolve is turned off automatically when TC Rec is turned on. (This is not a problem.) However, after that, Video Resolve doesn't return to ON automatically when TC Rec is turned off.

3) Erratic LED Lighting
When BER (Block Error Rate) screen in menu 9 is selected on LCD, erratic LED lighting occurs spontaneously while formatting, playing or recording. For example, Stop key lights while playing, or Rec Function LED lights although it is not turned on.

Note:
* This doesn't adversely affect formatting, playing or recording.
* In case Auto Mon key or etc is pressed, unit returns to correct LED lighting.

4) In Video Resolve ON state, tape is not formatted properly with showing following phenomena.

* Only FF key lights.
* Shows "Warning! Cannot Resolve: No Tape TC".

Note: Unit is originally designed so that Format should operate correctly even if Video Resolve is turned on. In the case, Video Resolve is temporarily turned off automatically while formatting.

5) Tape TC is not read correctly while tape runs at 20x speeds. Unit runs at 20x speed around following points.

* Tape reaches to beginning or end in FF or REW mode.
* Tape reaches to target point in Locate mode.

6) In case "TC Record Source: Not synchronized" is displayed, sound is not recorded (muted) from place to place. This may occur only in following state:

* IF-AN98HR is inserted.
* "IO Board Clk Range" in menu D is set to Narrow.
* Clock source of system (that DA-D98/DA-98HR is connected) is video.
* TC and sound are recorded simultaneously.

7) Erratic sound may be recorded when tape is being formatted to DSD.

This may occur only in following state:

* Confidence mode
* Rec function is off.

To allow the use of the advanced features provided by the HR series of TASCAM DTRS recorders, the DA-98HR and DA-78HR, the RC-898 remote control unit has been updated.

In addition, some other features have been made to reflect changes in the DTRS product line.

Note that when using this version of the RC-898 (2.0), units in the HR series should be at least system version 1.12 (DA-78HR) and system version 1.01 (DA-98HR). It is strongly recommended that it is not used with HR series units with earlier system versions.

The changes are restricted to menus and menu items. In other respects, the operation of the RC-898 is as described in the existing manual.

Track Delay Time (menu group 0)

DA-98HR – Note that although the operation of this function has not changed significantly, when it is used in conjunction with the DA-98HR's higher sampling frequencies (dual-frequency and quad-frequency), the number of samples now accurately reflects the time selected on the DA-98HR (that is, a higher sampling frequency is expressed as a larger number of samples for a given time).

Also note that when fewer than eight tracks are available for recording as the result of selecting a dual or quad sampling frequency, the unavailable tracks are not shown for selection.

For example, if the first DTRS unit in the chain is a DA-98HR which has been set to record at a sampling frequency of 192k (quad-frequency), only tracks 1 and 2 of this unit are available for recording and are shown for selection on the RC-898 screen, and instead of tracks 1 through 8 being available for grouped selection (usually, 1–8 appears in the display), only tracks 1 through 2 are available (1–2).

Track Copy (menu group 0)

DA-98 & DA-38 – Note that this menu item applies only to DA-38 and DA-98 DTRS units.

When it is required to change the input assignment of DA-98HR and DA-78HR units, the new Input Patchbay menu item (see immediately below) should be used.

Input Patchbay (menu group 0)

DA-78HR & DA-98HR – This new menu item allows the assignment of different signal sources to the inputs of the appropriate DTRS machine.

Input Patch						Mon 1		
Trk	1	2	3	4	5	6	7	8
Src	T	M	S	S	D	M	S	S
ch	1	–	3	4	5	–	7	8

There are four different sources that may be selected: T (tape), D (the currently-selected digital source on the DA-98HR), S (the slot source on the DA-98HR) and M (mute—this is not really a source).

Note that when this menu is used to select the input sources of a DA-78HR, the S option can refer only to the analog inputs. The D option refers to the SPDIF input, if this has been selected, otherwise to the TDIF-1 inputs.

If all tracks have been selected for recording at base frequency (DA-98HR), all tracks are shown, otherwise only those tracks available for recording are shown.

1 **Select the machine for editing (SHIFT + ▲ or ▼ keys).**

2 **Use the ◄ and ► cursor keys to move to the appropriate track.**

3 **Use the ▲ or ▼ keys to change the input source.**

4 **To select the source channel, use the ◄ cursor key to move to the extreme left of the screen, (Src) and then move the cursor down to the ch row.**

5 **Use the ► cursor key to select the channel (as defined in the ch row) number.**

To return to the source row, once again move the cursor to the extreme left, and then move up.

Rec Mute (menu group 1)

DA-98, DA-78HR & DA-98HR – The rec mute function can be enabled on a track-by-track basis, as described in the RC-898 manual.

However, note that if a DA-98HR unit is used and the sampling frequency is set to dual- or quad-frequency so that there are fewer than eight tracks available, only those tracks that are available will be shown in this screen.

Analog Reference Level (menu group 2)

DA-98 & DA-98HR – When this screen is selected with a DA-98HR fitted with AD and DA boards such as the optional IF-AN98HR boards, the input and output reference levels can be viewed (the changes are made using jumpers on the IF-AN98HR boards).

```
Analog Ref Level
      Machine  1
   Input    Output
  -16 dB    -16 dB
```

When this screen is selected with a DA-98 unit, the input and output reference levels can be set together to –16 dB, –18 dB or –20 dB.

```
Analog Ref Level
      Machine  1
      In/Out
      -16 dB
```

Video Reference (menu group 3)

DA-98HR – On the DA-98HR, the incoming video reference can be detected automatically (Auto) and this setting will typically work satisfactorily.

However, to improve synchronization in the case of a less-than-perfect video sync source, the rate can be manually set to any of the following: 30F, 29.97F, 25F, or 24F. See the DA-98HR manual for full details of this function.

```
Video Reference
      Machine  1


          Auto
```

1 **Select the machine whose video reference is to be edited.**

2 **Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the value.**

TC Accuracy (menu group 4)

DA-78HR & DA-98HR – When using the RC-898 with the DA-78HR and the DA-98HR, it is possible to change the timecode accuracy on a per-machine basis.

This means that slightly nonstandard timecode input can be accepted and used by the units which have the `Wider` option selected. Typically, all units will use the `Normal` setting, however:

```
TC Accuracy
Wider
Normal
Machine 1 2 3 4 5 6
```

1 Use the ◄ and ► cursor keys to move to the appropriate machine column.

2 Use the ▲ or ▼ keys to move the cursor to the appropriate line for that machine (either the `Wider` or the `Normal` line).

Consult the DTRS unit's manual for full details of this facility.

TC Timing (menu group 5)

DA-98HR, DA-78HR & DA-98 – When using the AD conversion facilities in the optional slot boards for the DA-98HR, and when using the DA-78HR, it is now possible to select either an analog or a digital timing reference for the timecode inputs and outputs independently. With the DA-98, this option is available for timecode output only.

The screen title and display have now changed (the screen shown below refers to a DA-98HR or DA-78HR unit).

```
TC Timing
     Machine  1
  Input   Output
  Analog  Analog
```

1 Select the machine whose timing reference is to be edited.

2 Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the timecode timing value for the input and output of that machine.

Clock (menu group 9)

All units – Although this screen appears the same as in previous versions of the RC-898, the available options have been changed to reflect the new models.

As before, the options for the DA-88 and DA-98 models (as well as for the DA-78HR and DA-98HR) are `Int` (internal), `Word` (word clock) and `Video` (video input).

For the DA-78HR and DA-98HR, the `Dig in` option has been added (digital inputs).

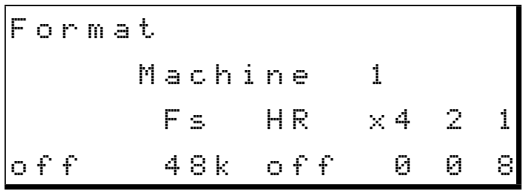
For the DA-98HR only, the `slot` option has been added, allowing certain optional slot boards to be used as the clock master. Note that the same restrictions apply as on the DA-98HR (for example, the IF-AN98HR slot boards cannot act as the master clock source).

Format (menu group 9)

DA-78HR & DA-98HR – This menu has been expanded to recognize the high-resolution and high sampling frequency capacities of the newer models.

In the case of both the DA-78HR and the DA-98HR, a HR (high-resolution) field allows the setting of this parameter to be on (24-bit) or off (16-bit).

In the case of the DA-98HR, the sampling frequency selected acts as the base frequency for the unit. The available track combinations are then displayed on the bottom right of the screen.



When the cursor is moved to this field, use the ▲ and ▼ keys to switch between the following options:

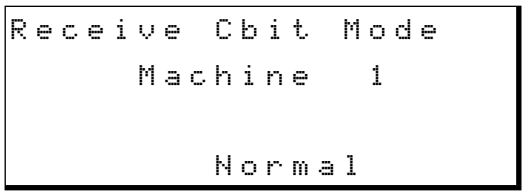
0 0 8	(eight base-frequency tracks)
0 2 4	2 x dual-frequency tracks, 4 base-frequency tracks
0 3 2	3 x dual-frequency tracks, 2 x base-frequency tracks
0 4 0	4 x dual-frequency tracks
2 0 0	2 x quad-frequency tracks

The process of selecting machines for the formatting process, and actually carrying out the format is as described in the RC-898 manual (move the cursor to off, change the message to ready, change the message to on, and then use the **RECORD** and **PLAY** key combination to start the format process).

Consult the DA-98HR manual for full details of the available track functions.

Receive Cbit Mode (menu group A)

DA-98HR – When using the DA-98HR, any mismatches between the received audio data and the data specified by the Cbits in the audio data stream will usually be shown on the DA-98HR display. However, it is possible to turn this off, using the screen here:



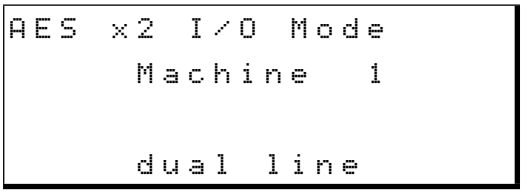
1 **Select the machine to be edited.**

2 **Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the parameter to either** Normal **or** No Warning.

AES x 2IO (menu group A)

DA-98HR – When using a DA-98HR unit when four dual-frequency tracks have been selected as the available tracks, there is a choice of how the signals should be output: either as dual-line or high-frequency signals, as explained more fully in the DA-98HR manual.

The settings are made using the following screen:

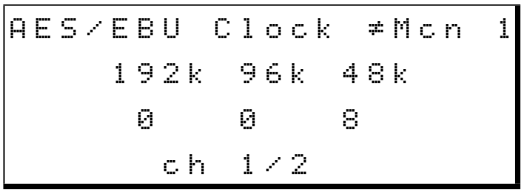


1 **Select the machine to be edited.**

2 **Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the parameter to either** dual line **or** high speed.

AES/EBU Clock (menu group A)

DA-98HR – When recording on the DA-98HR with AES/EBU inputs, you may wish to select one of the options described here as a clock source.

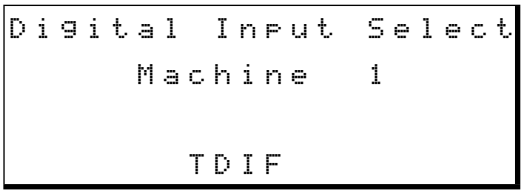


When this screen is shown, the current available track setting for the selected machine is also displayed. This available track setting also affects the choice of clock source, as does the dual AES/EBU mode described above.

Setting	Available clock source channels
Base x 8	1/2, 3/4, 5/6, 7/8
Dual-frequency x 4 (dual channel)	1, 2, 3, 4
Dual-frequency x 4 (high-speed)	1/2, 3/4
Dual-frequency x 2, base x 4	1, 2, 3/4, 5/6
Dual-frequency x 3, base x 2	1, 2, 3, 4/5
Quad-frequency x 2	1, 2

Digital Input Selection (menu group A)

DA-78HR & DA-98HR – This menu item allows the selection of digital sources for these two units in addition to the TDIF-1 input source.

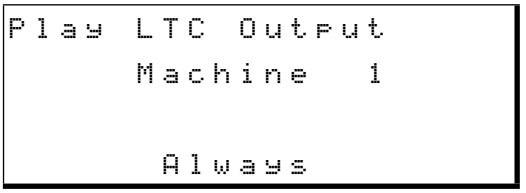


For the DA-98HR, the choice is either `TDIF` or `AES/EBU`.

For the DA-78HR, the choice is either `TDIF` or `SPDIF`.

Play TC Out (menu group A)

DA-78HR & DA-98HR – This menu item allows you to choose whether the selected unit will always output linear timecode (LTC) or will only output such timecode when the unit clock is locked (that is, it outputs LTC only when audio data is output).



The two options here are `Always` and `Locked Only`.

Output Patchbay (menu group B)

DA-78HR & DA-98HR – This screen allows the assignment of a track's audio to any output, simulating a digital patchbay. Only the numerals in the bottom row of the screen can be changed here (that is, the audio track number).

```
Output Patch
      Machine  1
  ch  1 2 3 4 5 6 7 8
 Trk  1 2 3 4 5 6 7 8
```

Mix Input Selection (menu group B)

DA-78HR & DA-98HR – This screen allows the selection of the sources for the internal mixer of DA-98HR and DA-78HR units.

```
Mix Input        Mcn 1
 Trk  1 2 3 4 5 6 7 8
 Src  T M S S D M S S
  ch  1 - 3 4 5 - 7 8
```

1 Select the machine for editing.

NOTE

If the machine selected is not capable of being controlled using this menu (that is, it is neither a DA-98HR nor a DA-78HR) an appropriate message is shown.

2 Use the ◄ and ► cursor keys to move to the appropriate track.

3 Use the ▲ or ▼ keys to change the input source.

4 To select the source channel, use the ◄ cursor key to move to the extreme left of the screen, (`Src`) and then move the cursor down to the `ch` row.

5 Use the ► cursor key to select the channel (as defined in the `ch` row) number.

To return to the source row, once again move the cursor to the extreme left, and then move up.

Output Word Length (menu group B)

DA-78HR & DA-98HR – This menu allows either 16-bit or 24-bit to be selected as the word length of the output audio data.

```
Output Word Length
 16 bit
 24 bit
Machine 1 2 3 4 5 6
```

The rows on this screen represent the bit resolution of the output audio, and the columns represent the machines in the chain.

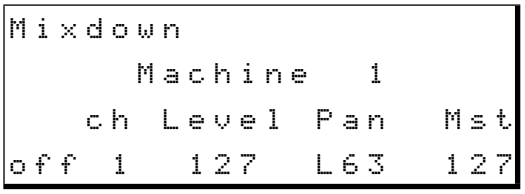
1 Use the ◄ and ► cursor keys to move to the appropriate machine column.

2 Use the ▲ or ▼ keys to move the cursor to the appropriate line for that machine (either the `16 bit` or the `24 bit` line).

Mixdown (menu group B)

DA-78HR & DA-98HR – This screen allows the sources selected for mixdown in the screen described above to be mixed into a stereo pair, with individual level and pan for each channel of the mix, as well as a master level for the whole stereo mix.

Select the machine on which the mixdown is to take place.



The bottom left parameter controls whether the mixdown is on or off for the machine. If this is set to off, no other settings made on this screen will have any effect.

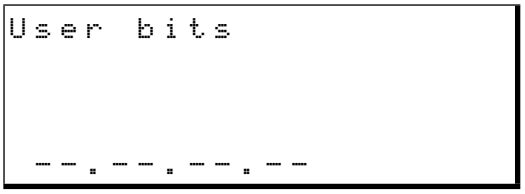
The channel may be selected, and the level adjusted from 0 to 127.

Pan settings are from hard left L- through L63 through C (center) to -R (hard right).

The master mix volume may be adjusted from 0 to 127.

User bits (menu group D)

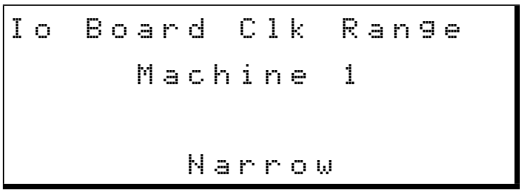
DA-78HR & DA-98HR – There are no parameters to be set in this screen, which simply displays any user bits recorded within the timecode source.



IO Clock range (menu group D)

DA-98HR – When using the DA-98HR with the optional IF-AN98HR slot boards, it may be necessary to adjust the clock width setting.

The Narrow setting enables a crystal oscillator, and suppresses jitter, providing high-quality audio. However, if the clock master accuracy is low, the precision is affected, and the audio quality may suffer. The Wide setting enables an LC oscillator. The jitter level is increased a little compared with the Narrow setting and the audio quality may be slightly diminished, but this setting can be used even with poor-quality input clocks.



For details of the limitations imposed on this setting, consult the appropriate section of the DA-98HR manual.

Tape Load/Save (menu group F)

DA-78HR & DA-98HR – This allows the saving and loading of the RC-898's settings to and from tape. The settings that are saved are:

- Locate Points (Master only)
- Locate Pre-roll
- GPI Setup
- Event
- 9pin Control Mode
- 9pin Rec Acceptable
- Key Mode
- Frame Display
- Display Time

These parameters are stored on tape. They do not affect any audio data on the tape. Only one set of parameters can be stored on one tape.

NOTE

This operation only applies to the tape recorded on the first machine in the chain (ID=1).

1 With a tape loaded in the unit, use the ▲ and ▼ keys to select either `Load` or `Save`. Press SELECT.

2 The display shows `Are you sure ?`. Press SELECT to confirm the operation. To cancel the operation, press either ESCAPE or STOP so the display shows `Cancel`. Press the ESCAPE key to dismiss this message.

While the operation is taking place (either loading or saving the data), the display shows `Executing...`. Any REC FUNCTION indicators will go out.

3 If the operation is successful, the display shows `Complete`. Press the ESCAPE key to dismiss this message.

If an error occurs, one of the following messages may appear. Press the **ESCAPE** key to dismiss these messages:

`Can't start`	A suitable tape is not loaded, etc.
`Data not found`	No data has been recorded on the tape (when loading)
`Read error`	An error occurred when reading the data from tape (when loading)
`Verify error`	An error occurred when certifying the data after writing (when saving)

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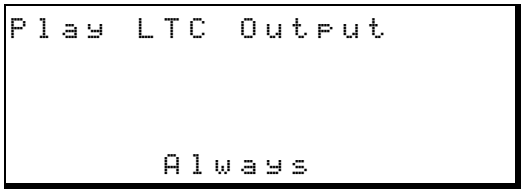
These notes refer to changes and additions in the system version 1.02 of the DA-98HR DTRS recorder.

Please keep this sheet together with the original documentation for the DA-98HR.

Play TC Out (menu group A)

This new feature allows the setting of when LTC will be output by the DA-98HR, which may be found useful when using the DA-98HR with some timecode slave units.



There are two options:

Always (default), which will output LTC as soon as the DA-98HR starts to play back, even before the servo is locked.

Locked Only, which outputs LTC when the unit servo is locked (in the same way that audio data is only output when the unit is servo-locked).

Error message

The DA-98HR can record at base, dual or quad sampling frequency, and this Track Fs information is now included as part of the TDIF data. The "E bit" portion of the TDIF data, previously unused, contains this Track Fs information.

If the unit receives TDIF data with mismatched Track Fs information (that is, the TDIF data and the current settings do not match), the message below is displayed.:

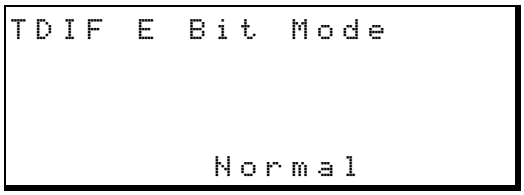
IMPORTANT NOTE

If this message is displayed, you should not record on the tape. Even if it appears that you have recorded on the tape, correct playback will be impossible.

TDIF E Bit mode (menu group B)

This new menu item allows you to ignore E bit data embedded in the incoming TDIF data, which under certain circumstances may be falsely interpreted by the DA-98HR as being sampling frequency errors (for example, when non-HR TDIF data is received from certain units). If such units output E bit data, the message described above will appear, even if the audio data is correct.

This menu item allows any such spurious data to be ignored and the error message suppressed:



There are two options:

Normal (default): the error message is shown.

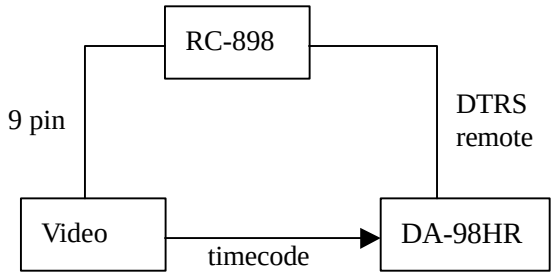
No Warning: the error message is suppressed. Only select this option if you are completely certain that the sampling frequency of the input TDIF signal matches that of the unit's current settings.

IMPORTANT NOTE

If the input sampling frequency and the current settings do not match, even though it may seem that you can record on the tape, you will not be able to play back the tape correctly.

RC-898, Known problem

Configuration



Symptom

DA-98HR chases timecode coming from video machine.
Now perform REHAERSAL or AUTO IN/OUT.
After out point, all machines stop at post-roll point.
Sometimes chase mode on DA-98HR goes off falsely.

Both of V1.00 and V2.00 have same problem.

This problem has been solved by RC-898 beta V32.01 running under the reliability test.
V2.01(?) will be officially released January 2000.

ANALOG DEVICES

Dual-Channel ΣΔ Modulator

ADMOD79*

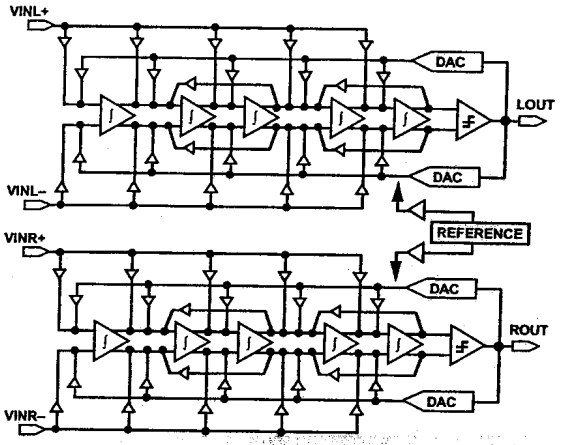
FEATURES

- High-Performance ΣΔ ADC Building Block
- Fifth-Order, 64 Times Oversampling Modulator with Patented Noise-Shaping
- Modulator Clock Rate to 3.57 MHz
- 103 dB Dynamic Range (for 20 kHz Input Bandwidth)
- Differential Architecture for Superior SNR and Dynamic Range
- Dual-Channel Differential Analog Inputs (±6.2 V Differential Input Voltage)
- On-Chip Voltage Reference

APPLICATIONS

- Digital Audio
- Medical Electronics
- Electronic Imaging
- Sonar Signal Processing
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT OVERVIEW

The ADMOD79 Sigma-Delta (ΣΔ) modulator is a building block which can be used to build a superior analog-to-digital conversion system customized to a particular application's requirement. The ADMOD79 is a two-channel, fully differential modulator. Each channel consists of a fifth-order one-bit noise shaping modulator. An on-chip voltage reference provides a voltage source to both channels that is stable over temperature and time. There are separate single-bit digital outputs for each channel. The ADMOD79 accepts a $64 \times F_S$ input master clock (SMPCLK) that can range from 2.5 kHz to 3.57 MHz.

Input signals are sampled at $64 \times F_S$ on switched-capacitors, eliminating external sample-and-hold amplifiers and minimizing the requirements for antialias filtering at the input. With simplified antialiasing, linear phase can be preserved across the passband. The ADMOD79's proprietary fifth-order differential switched-capacitor modulator architecture shapes the one-bit comparator's quantization noise out of the passband. The high order of the modulator randomizes the modulator output, reducing idle tones in the output spectrum to very low levels. The ADMOD79's differential architecture provides increased dynamic range and excellent common-mode rejection characteristics. Because its modulator is single-bit, the ADMOD79 is inherently monotonic and has no mechanism for producing differential linearity errors. Analog and digital supply connections are separated to isolate the analog circuitry from the digital supplies.

The ADMOD79 is fabricated in a BiCMOS process and is supplied in a 0.6" wide 28-lead cerdip package. The ADMOD79 operates from ±5 V power supplies over the temperature range of -25°C to +70°C.

*Protected by U.S. Patent Numbers 5055843, 5126653, and others pending.

REV. 0

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Tel: 617/329-4700 Fax: 617/326-8703

ADMOD79–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED					
Supply Voltages	±5	V	Input Signal	974	Hz
Ambient Temperature	25	°C		-0.5	dB Full-Scale
Input Clock (SMPCLK)	3.072	MHz	Passband	0 to 20	kHz

	Min	Typ	Max	Units
ANALOG PERFORMANCE				
Dynamic Range (0 Hz to 20 kHz, -60 dB Input)				
No A-Weight Filter	100	103		dB
With A-Weight Filter		105		
Signal to (Distortion + Noise)				
Full-Scale Input	90	96		dB
-20 dB Input		83		
Trimmed[1] Signal to (Distortion + Noise)				
Full-Scale Input	93	98		dB
-20 dB Input		83		dB
Trimmed[1] Signal to Total Harmonic Distortion				
Full-Scale Input		98		dB
-20 dB Input		100		dB
Analog Inputs				
Differential Input Range[2]	±5.89	±6.2	±6.51	V
Input Impedance at Each Input Pin		7.0		kΩ
DC Accuracy				
Gain Error			±5	%
Interchannel Gain Mismatch			±0.15	dB
Gain Drift		±200		ppm/°C
Offset Error (Referrred to Input)		±0.057	±0.343	% of FS
Offset Drift (Referred to Input)		±13		ppm/°C
Voltage Reference*	2.4	2.8	3.2	V
Crosstalk (EIAJ Method)	100			dB
Interchannel Phase Deviation		±0.001		Degrees
DIGITAL TIMING (Guaranteed over 0°C ≤ T_A ≤ 70°C, AV_{SS} = -5.0 V ± 5%, AV_{DD} = DV_{DD} = +5.0 V ± 5%)				
t_{SCP} SMPCLK Period	0.28		400	µs
t_{SCPWL} SMPCLK LO Pulse Width	140			ns
t_{SCPWH} SMPCLK HI Pulse Width	140			ns
t_{OPD} Propagation Delay, SMPCLK Falling Edge to ROUT, LOUT			100	ns
t_{RPD} Propagation Delay, SMPCLK Rising Edge to $\overline{RRESET}$, $\overline{LRESET}$			125	ns
DIGITAL I/O (Guaranteed over 0°C ≤ T_A ≤ 70°C, AV_{SS} = -5.0 V ± 5%, AV_{DD} = DV_{DD} = +5.0 V ± 5%)				
Input Voltage HI (V_{IH})	3.4			V
Input Voltage LO (V_{IL})			0.8	V
I_{IH} @ V_{IH} = 5 V			10	µA
I_{IL} @ V_{IL} = 0 V			10	µA
Output Voltage HI (V_{OH} @ I_{OH} = 360 µA)	4.0			V
Output Voltage LO (V_{OL} @ I_{OL} = 1.6 mA)			0.5	V
POWER SUPPLIES				
Current, DV_{DD}		1.0	1.5	mA
Current, $AV_{DD}1$, $AV_{SS}1$		76	95	mA
Current, $AV_{DD}2$, $AV_{SS}2$		8	12	mA
Current, $AV_{DD}1$, $AV_{SS}1$ - Power Down		14	20	mA
Dissipation				
Operation (All Supplies)		845	1078	mW
Power Down (All Supplies)		225	328	mW
Power Supply Rejection				
1 kHz 300 mV p-p Signal at Analog Supply Pins		102		dBFS
TEMPERATURE RANGE				
Specifications Guaranteed		+25		°C
Functionality Guaranteed	-25		+70	°C
Storage	-60		+100	°C

NOTES

[1]Differential gain imbalance manually trimmed to eliminate second harmonic. See "Application Issues" below.

[2]The differential input range is twice the range seen at each input pin. The input range corresponds to the full-scale digital output range.

*Guaranteed, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

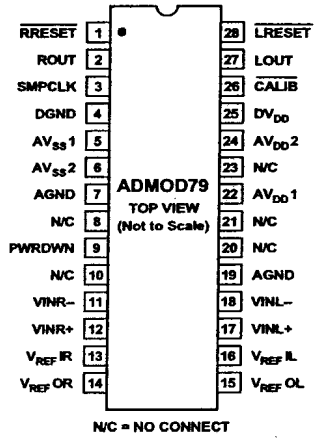
	Min	Max	Units
DVDD to DGND and $AV_{DD}1/AV_{DD}2$ to AGND	0	6	V
$AV_{SS}1/AV_{SS}2$ to AGND	-6	0	V
$AV_{SS}2$ to $AV_{SS}1$	-0.3		V
Digital Input to DGND	-0.3	DV_{DD} + 0.3	V
Analog Inputs	$AV_{SS}1$ - 0.3	$AV_{SS}1$ + 0.3	V
AGND to DGND	-0.3	0.3	V
Reference Voltage	Indefinite Short Circuit to Ground		
Soldering		+300	°C
		10	sec

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADMOD79JQ	0°C to +70°C	Cerdip	Q-28

PIN CONFIGURATIONS



N/C = NO CONNECT

PIN DESCRIPTIONS

Pin Number	Mnemonic	Input/ Output	Description
1	$\overline{\text{RRESET}}$	O	Right Modulator Reset
2	ROUT	O	Right Bitstream Modulator Output
3	SMPCLK	I	3.072 MHz (Nominal) Modulator Input Clock
4	DGND	I	Digital Ground
5	$AV_{SS}1$	I	-5 V Analog Supply
6	$AV_{SS}2$	I	-5 V Analog Logic Supply
7	AGND	I	Analog Ground
8	N/C		No Connect
9	PWRDWN	I	Power Down
10	N/C		No Connect
11	VINR-	I	Right Inverting Input
12	VINR+	I	Right Noninverting Input
13	$V_{REF}IR$	I	Right Reference Input
14	$V_{REF}OR$	O	Right Reference Output
15	$V_{REF}OL$	O	Left Reference Output
16	$V_{REF}IL$	I	Left Reference Input
17	VINL+	I	Left Noninverting Input
18	VINL-	I	Left Inverting Input
19	AGND	I	Analog Ground
20	N/C		No Connect
21	N/C		No Connect
22	$AV_{DD}1$	I	+5 V Analog Supply
23	N/C		No Connect
24	$AV_{DD}2$	I	+5 V Analog Logic Supply
25	DV_{DD}	I	+5 V Digital Supply
26	$\overline{\text{CALIB}}$	I	Calibration
27	LOUT	O	Left Bitstream Modulator Output
28	$\overline{\text{LRESET}}$	O	Left Modulator Reset Signal

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADMOD79 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS

Dynamic Range
The ratio of a full-scale output signal to the integrated output noise in the passband (0 kHz to 20 kHz with a 3.072 MHz modulator clock rate), expressed in decibels (dB). Dynamic range is measured with a -60 dB input signal and is equal to (S/[THD+N]) +60 dB.

Signal to (Distortion + Noise) (or S/[THD+N])
The ratio of the root-mean-square (rms) value of the fundamental input signal to the rms sum of all spectral components in the passband, expressed in decibels (dB).

Signal to Total Harmonic Distortion (or S/THD)
The ratio of the rms value of the fundamental input signal to the rms sum of all harmonically related spectral components in the passband, expressed in decibels (dB).

Gain Error
With a near full-scale input, the ratio of actual output to expected output, expressed as a percentage.

Interchannel Gain Mismatch
With near full-scale inputs, the ratio of outputs of the two stereo channels, expressed in decibels.

Gain Drift
Change in response to a near full-scale input with a change in temperature, expressed as parts-per-million (ppm) per °C.

Midscale Offset Error
Output response to a midscale input (i.e., zero volts dc), expressed as a percentage of full scale.

Midscale Drift
Change in midscale offset error with a change in temperature, expressed as parts-per-million (ppm) of full scale per °C.

Crosstalk
Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine-wave input on the other channel, expressed in decibels.

Interchannel Phase Deviation
Difference in input sampling times between stereo channels, expressed as a phase difference in degrees between 1 kHz inputs.

Power Supply Rejection
With analog inputs grounded, energy at the output when a 300 mV p-p signal applied to the power supply pins, expressed in decibels of full scale.

THEORY OF OPERATION

Resonators in the proprietary fifth-order ADMOD79 modulator architecture place zeros in the noise-shaping spectrum, reducing the quantization noise at lower frequencies. (See Figure 1.) The ADMOD79's fully differential architecture increases its signal-to-noise ratio performance. Completely independent right and left channels with separate references minimize crosstalk. Modulator clock rates as high as 3.57 MHz are supported.

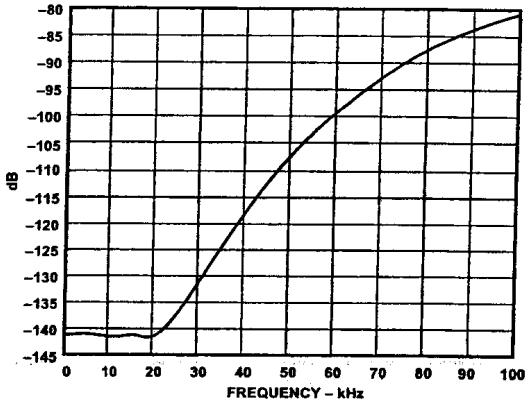


Figure 1. Noise Spectrum per 5 Hz (3.072 MHz Modulator Clock)

User-supplied digital decimation filters allow for a broad range of performance and filter functions. For standard, brick-wall digital low-pass filters with sufficient stopband attenuation, the following performance can be achieved with the ADMOD79 running at a 3.072 MHz modulator clock rate:

Filter Cut-Off Frequency	Oversampling Ratio	Signal-to-Noise Ratio
20 kHz	64	103 dB
10 kHz	128	106 dB
5 kHz	256	109 dB
2.5 kHz	512	112 dB
1.25 kHz	1024	115 dB
625 Hz	2048	118 dB

In general, since the noise is spectrally white in the passband, each halving of the input bandwidth with a constant modulator clock frequency will increase the SNR across the bandwidth by 3 dB.

Power consumption of the ADMOD79 is 1078 mW maximum. However, in power-down mode, consumption is reduced to 328 mW (with a 3.072 MHz modulator clock). Note that the ADMOD79 will still function in this mode. In the power-down mode, the ADMOD79 will operate with a slower modulator clock over a more limited bandwidth. The SNR over the band of interest is reduced relative to that possible with a full-speed modulator clock.

Typical modulator noise integrated across the passband of the modulator as shown in Figure 1 is always 103 dB, regardless of modulator clock rate. The width of that passband, however, scales down linearly with a slower clock. For example, if the modulator clock is slowed by a factor of two, noise will begin to rise at 10 kHz instead of 20 kHz. Since the same inband noise is now spread across a narrower passband, the noise per one Hz bin will also increase accordingly. Thus, the passband of Figure 1 will narrow and its floor will rise.

Modulator Clock	Modulator Passband	SNR	SNR per One Hz Bin
3.072 MHz	20 kHz	103 dB	145 dB
1.536 MHz	10 kHz	103 dB	142 dB
768 kHz	5 kHz	103 dB	139 dB
384 kHz	**2.5 kHz**	**103 dB**	**136 dB**
192 kHz	1.25 kHz	103 dB	133 dB
96 kHz	625 Hz	103 dB	130 dB

The power-down mode will support modulator clocks as fast as 384 kHz, shown above in bold.

As described above, the SNR can always be increased at a constant modulator clock rate by limiting the input bandwidth with a brick-wall digital decimation filter. This same technique can be used in the power-down mode. Thus, with a 384 kHz clock in the power-down mode, 105 dB would be achievable over a 1.25 kHz bandwidth (128 times oversampling) and 108 dB over a 625 Hz band of interest (256 times oversampling).

The ADMOD79's fifth-order modulators use a distinctive architecture of feed-forward and feed-back signal paths to achieve a high performance level. Gain is controlled by switched capacitors. Resonator loops feeding back from the third and fifth stage outputs allow the placement of zeros in the quantization-noise transfer function. These zeros have been chosen to further reduce noise in the passband. The noise floor is dominated by spectrally flat thermal circuit noise in the passband.

OPERATING FEATURES

The ADMOD79 produces a pair of noise-shaped bitstreams (LOUT and ROUT) from a pair of differential analog inputs (+VINL & -VINL and +VINR & -VINR). The analog input signal range at any given signal input pin is ±3.1 V. This implies that voltage difference across each differential pair can range ±6.2 V. The modulator clock oversamples the analog input at a rate much higher than the input bandwidth, significantly reducing the requirements on antialiasing filters. Only signals with frequency components near the very high modulator clock rate will alias into the passband. The high clock rate also eliminates the requirement for a sample-and-hold amplifier.

Holding the calibration input, $\overline{\text{CALIB}}$, LO disconnects the input from the modulators, regardless of the signal applied to the input pins. This feature allows for system calibration. Allow at least ten modulator clock cycles after asserting $\overline{\text{CALIB}}$ before reading the output bit streams.

Should an input overdrive the modulator to instability, the ADMOD79 will reset itself within 25 modulator clock cycles. Each modulator independently produces an output signal on pins $\overline{\text{LRESET}}$ and $\overline{\text{RRESET}}$, respectively, indicating the initiation of a reset sequence. These pins, normally HI, will go LO for one cycle should instability occur.

The pair of modulator outputs are TTL-compatible but are in fact driven to CMOS logic levels. Digital output data is valid on the rising edge of SMPCLK. For highest performance, the ADMOD79 modulator has been designed so that the full-scale range of the one's density is from 20% to 80% (i.e., -dc full scale = 20% one's density, +dc full scale = 80% one's density). The user's decimator should effectively gain up the modulator's output by a factor of 5/3 to produce a full-scale output corresponding to a full-scale input.

The ADMOD79 contains a pair of +2.8 V voltage references. The user has the option of using these internal references or supplying an external reference. In the former case, two external capacitors and two external resistors are required for voltage reference noise reduction. These capacitors and resistors should be connected between reference inputs (V_{REF}IL and V_{REF}IR) and analog ground as shown in Figure 2. The reference outputs (V_{REF}OL and V_{REF}OR) should be connected directly to the reference input pair. To use external reference(s), bypass the reference(s) to analog ground and connect to the reference inputs (V_{REF}IL and V_{REF}IR). The reference outputs become no connects.

The ADMOD79 requires a ±5 V analog supply and a +5 V digital supply. The analog supply should be connected to the two sets of analog supply pins, which should be decoupled from each other. (The $AV_{SS}1$ and $AV_{DD}1$ pins power the amplifiers and other active analog circuitry; the $AV_{SS}2$ and $AV_{DD}2$ pins provide voltage for the modulator's switches.) See Figure 4 for the recommended bypassing configuration.

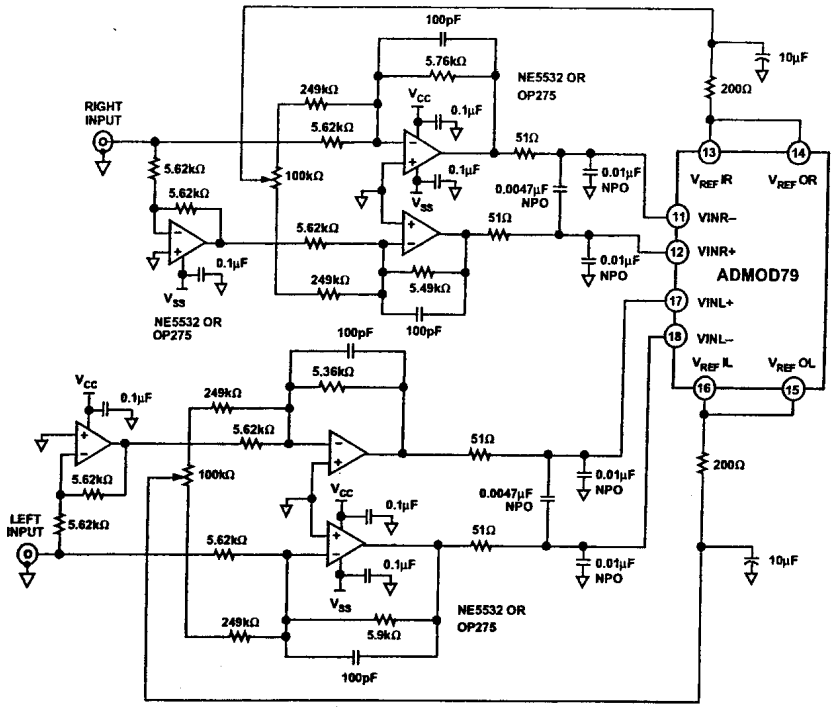


Figure 2. Recommended Input Structure

APPLICATIONS ISSUES

Recommended Input Structure

The ADMOD79 input structure is fully differential for improved common-mode rejection properties and increased dynamic range. Since each input pin sees ±3.1 V swings, each channel's input signal effectively swings ±6.2 V, i.e., across a 12.4 V range.

In most cases, a single-ended-to-differential input circuit is required. Shown in Figure 2 is the recommended circuit, based on extensive experimentation. Note that to maximize signal swing, the op amps in this circuit are powered by ±12 V or greater supplies. The ADMOD79 itself requires ±5 V supplies. If ±5 V supplies are not available in the target system, Figure 3 illustrates the recommended circuit for generating these supplies.

The trim potentiometers shown in Figure 2 connecting the minus (–) inputs of the driving op amps permit trimming out dc offset, if desired.

Note that the driving op amp feedback resistors all have slightly different values. These values produce a slight differential gain imbalance and were derived empirically to minimize second harmonic distortion on average and produce the lowest overall THD without part-by-part trimming. Replacing one of these feedback resistors in each channel with a trim potentiometer allows trimming the differential gain imbalance for part-by-part optimal performance. Analog Devices has done this in the lab by paralleling 100 kΩ trim potentiometers around the 5.49 kΩ and 5.36 kΩ input feedback resistors for the VINR+ and VINL+ signals that can be found in Figure 2. By trimming gain imbalance, second harmonic distortion can always be eliminated. In the "Specifications" section of this data sheet, a

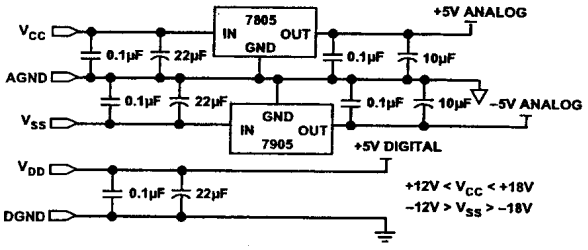


Figure 3. ADMOD79 Recommended Power Conditioning Circuit

distinction is drawn between trimmed and untrimmed signal-to-(noise + distortion) and trimmed and untrimmed total harmonic distortion. The untrimmed specifications are tested with the input structure shown in Figure 2. The trimmed specifications are based on a part-by-part trim of this differential gain to eliminate the second harmonic.

The input circuit of Figure 2 could be implemented with a single pair of operational amplifiers per channel, one inverting and one noninverting. The recommended architecture shown in Figure 2 using three inverting op amps per channel provides isolation of the op amp inputs from charge dumped back from

the ADMOD79's input capacitors when these large capacitors switch. The performance from a two op amp per channel input structure may be adequate in many applications.

Layout and Decoupling Considerations

Obtaining the best possible performance from a state-of-the-art modulator like the ADMOD79 requires close attention to board layout. From extensive experimentation, Analog Devices has discovered principles that produce typical values of 103 dB dynamic range and 98 dB S/(THD+N) in target systems with an oversampling ratio of 64. The principles and their rationales are listed below in descending order of importance. The first two pertain to bypassing and are illustrated in Figure 4.

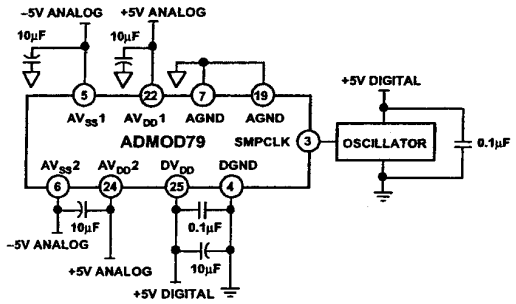


Figure 4. Recommended Bypassing and Oscillator Circuits

The digital bypassing of the ADMOD79 is a critical item on the board layout. The user should tie a bypass capacitor set (0.1 µF ceramic and 10 µF tantalum) on the DV_{DD} supply pin as close to the pin as possible. The trace between the package pin and the capacitors should be as short and as wide as possible. This will prevent digital supply current transients from being inductively transmitted to the inputs of the part.

The analog input bypassing is a second critical item. Use 0.01 µF NPO ceramic capacitors from each input pin to the analog ground plane, with a clear ground path from the bypass capacitor to the AGND pin on the same side of the package (Pins 7 and 19). The trace between this package pin and the capacitor should be as short and as wide as possible. A 0.0047 µF NPO ceramic capacitor should be placed between each set of input pins (11 to 12, and 17 to 18) to complete the input bypassing. This input bypassing minimizes the RF transmission and reception capability of the ADMOD79 inputs.

The ADMOD79 should be placed on a split ground plane as illustrated in Figure 5. The digital ground plane should be placed under the top end of the package and the analog ground plane should be placed under the bottom end of the package as shown in Figure 5. The split should be between Pins 4 and 5 and between Pins 24 and 25. The ground planes should be tied together at one spot underneath the center of the package. This ground plane technique also minimizes RF transmission and reception.

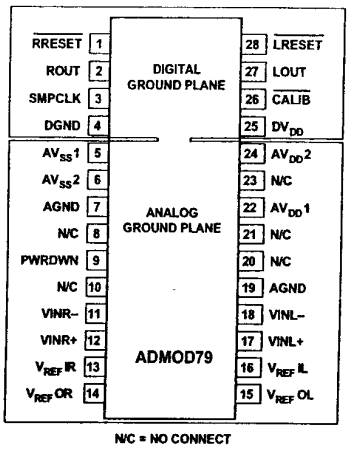


Figure 5. ADMOD79 Recommended Ground Plane

Each reference input pin (13 and 16) should be bypassed with a 200 Ω resistor and a 10 µF capacitor as shown in Figure 2. One end of the resistor should be placed as close to the package pin as possible, and the trace to it from the reference pin should be as short and as wide as possible. Keep this trace away from input pin traces! Coupling between input and reference traces will cause second harmonic distortion. The resistor is used to reduce the high-frequency coupling into the references from the board.

Wherever possible, minimize the capacitive load on digital outputs of the part. This will reduce the digital spike currents drawn from the digital supply pins.

Digital Timing

The delay from a SMPCLK falling edge to ROUT and LOUT data valid is t_{OPD}. The minimum SMPCLK LO pulse width is t_{SCPWL}, and the minimum SMPCLK HI pulse width is t_{SCPWH}. The minimum SMPCLK period is t_{SCP}. The delay from a SMPCLK rising edge to $\overline{\text{RRESET}}$ or $\overline{\text{LRESET}}$ is t_{RPD}. These timing relationships are shown in Figure 6.

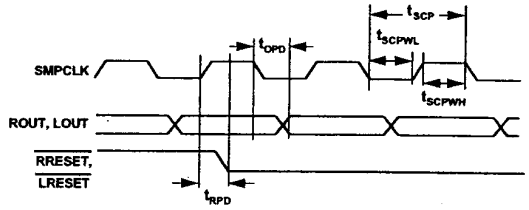
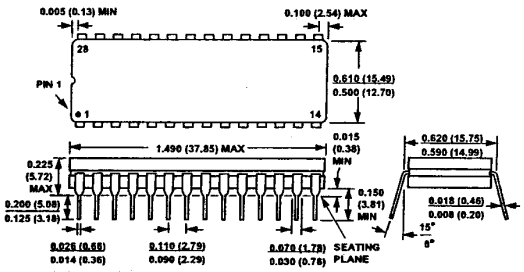


Figure 6. Digital Timing Diagram

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Q-28
28-Lead Cerdip



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AK4393

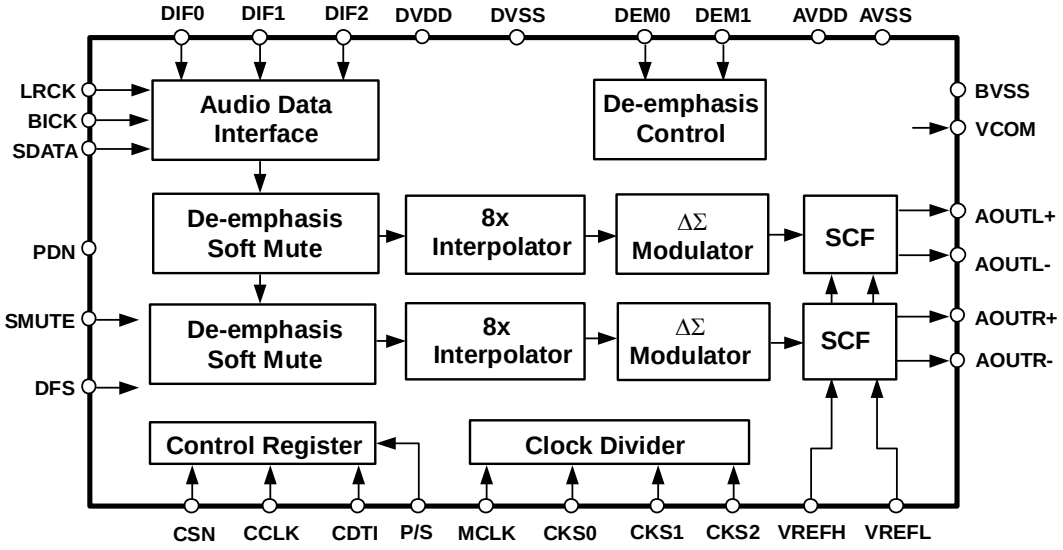
Advanced Multi-Bit 96kHz 24-Bit ΔΣ DAC

GENERAL DESCRIPTION

The AK4393 is a high performance stereo DAC for the 96kHz sampling mode of DAT, DVD including a 24bit digital filter. The AK4393 introduces the advanced multi-bit system for ΔΣ modulator. This new architecture achieves the wider dynamic range, while keeping much the same superior distortion characteristics as conventional Single-Bit way. In the AK4393, the analog outputs are filtered in the analog domain by switched-capacitor filter (SCF) with high tolerance to clock jitter. The analog outputs are full differential output, so the device is suitable for hi-end applications. The operating voltages support analog 5V and digital 3.3V, so it is easy to I/F with 3.3V logic IC.

FEATURES

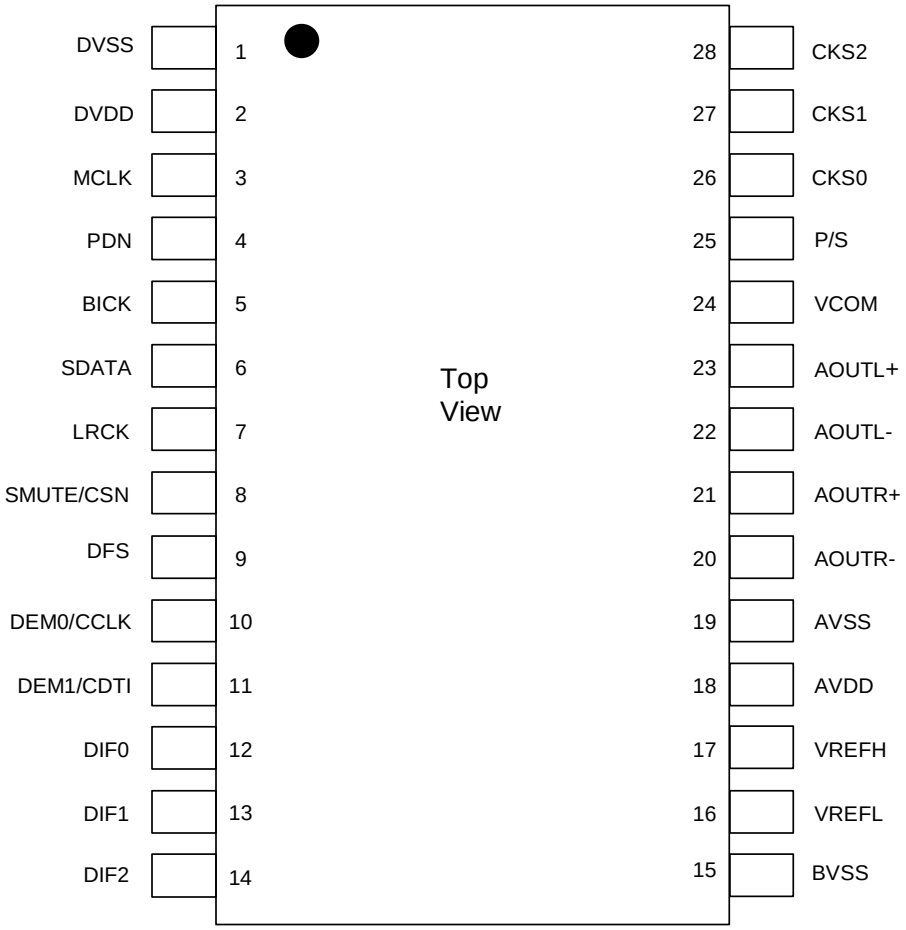
- **128x Oversampling**
- **Sampling Rate up to 108kHz**
- **24Bit 8x Digital Filter**
  Ripple: ±0.005dB, Attenuation: 75dB
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **Digital de-emphasis for 32, 44.1, 48 & 96kHz sampling**
- **Soft Mute**
- **THD+N: -100dB**
- **DR, S/N: 120dB**
- **I/F format : MSB justified, 16/20/24bit LSB justified, I^2S**
- **Master Clock: Normal Speed: 256fs, 384fs, 512fs or 768fs**
  Double Speed: 128fs, 192fs, 256fs or 384fs
- **Power Supply: 4.75 to 5.25V (Analog), 3 to 5.25V (Digital)**
- **Small Package: 28pin VSOP**



■ Ordering Guide

AK4393VF	-40 ~ +85 °C	28pin VSOP (0.65mm pitch)
AKD4393	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVSS	-	Digital Ground Pin
2	DVDD	-	Digital Power Supply Pin, 3.3V or 5.0V
3	MCLK	I	Master Clock Input Pin
4	PDN	I	Power-Down Mode Pin When at "L", the AK4393 is in power-down mode and is held in reset. The AK4393 should always be reset upon power-up.
5	BICK	I	Audio Serial Data Clock Pin The clock of 64fs or more than is recommended to be input on this pin.
6	SDATA	I	Audio Serial Data Input Pin 2's complement MSB-first data is input on this pin.
7	LRCK	I	L/R Clock Pin
8	SMUTE	I	Soft Mute Pin in parallel mode When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CSN	I	Chip Select Pin in serial mode
9	DFS	I	Double Speed Sampling Mode Pin (Internal pull-down pin) "L": Normal Speed , "H": Double Speed
10	DEM0	I	De-emphasis Enable Pin in parallel mode
	CCLK	I	Control Data Clock Pin in serial mode
11	DEM1	I	De-emphasis Enable Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode
12	DIF0	I	Digital Input Format Pin
13	DIF1	I	Digital Input Format Pin
14	DIF2	I	Digital Input Format Pin
15	BVSS	-	Substrate Ground Pin, 0V
16	VREFL	I	Low Level Voltage Reference Input Pin
17	VREFH	I	High Level Voltage Reference Input Pin
18	AVDD	-	Analog Power Supply Pin, 5.0V
19	AVSS	-	Analog Ground Pin, 0V
20	AOUTR-	O	Rch Negative analog output Pin
21	AOUTR+	O	Rch Positive analog output Pin
22	AOUTL-	O	Lch Negative analog output Pin
23	AOUTL+	O	Lch Positive analog output Pin
24	VCOM	O	Common Voltage Output Pin, 2.6V
25	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
26	CKS0	I	Master Clock Select Pin
27	CKS1	I	Master Clock Select Pin
28	CKS2	I	Master Clock Select Pin

Note: All input pins except internal pull-up/down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, BVSS, DVSS = 0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	| BVSS-DVSS | (Note 2)	Δ GND	-	0.3	V
Input Current , Any pin Except Supplies		IIN	-	±10	mA
Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Operating Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Notes: 1. All voltages with respect to ground.
2. AVSS, BVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, BVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog	AVDD	4.75	5.0	5.25	V
(Note 3)	Digital	DVDD	3.0	3.3	5.25	V
Voltage Reference	"H" voltage reference	VREFH	AVDD-0.5	-	AVDD	V
(Note 4)	"L" voltage reference	VREFL	AVSS	-	-	V
	VREFH-VREFL	Δ VREF	3.0	-	AVDD	V

Notes: 3. The power up sequence between AVDD and DVDD is not critical.
4. Analog output voltage scales with the voltage of (VREFH-VREFL).
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = ±2.4Vpp×(VREFH-VREFL)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta = 25°C; AVDD = 5V, DVDD = 3.3V; AVSS, BVSS, DVSS = 0V, VREFH = AVDD, VREFL = AVSS;
fs = 44.1kHz; BICK = 64fs; Signal Frequency = 1kHz; 24bit Input Data; Measurement Bandwidth = 20Hz~20kHz;
$R_L \geq 600\Omega$; External circuit: Figure 11; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					24	Bits
Dynamic Characteristics (Note 5)						
THD+N	fs=44.1kHz	0dBFS		-100	-90	dB
	BW=20kHz	-60dBFS		-53	-	dB
	fs=96kHz	0dBFS		-97	-86	dB
	BW=40kHz	-60dBFS		-51	-	dB
Dynamic Range (-60dBFS with A-weighted)	fs=44.1kHz	(Note 6)	112	117		dB
		(Note 7)	-	120		dB
	fs=96kHz		111	116		dB
		(Note 7)	-	118		dB
S/N (A-weighted	fs=44.1kHz	(Note 8)	112	117		dB
		(Note 7)	-	120		dB
	fs=96kHz		111	116		dB
		(Note 7)	-	118		dB
Interchannel Isolation (1kHz)			100	120		dB
DC Accuracy						
Interchannel Gain Mismatch				0.15	0.3	dB
Gain Drift		(Note 9)		20	-	ppm/°C
Output Voltage		(Note 10)	±2.25	±2.4	±2.55	Vpp
Load Resistance		(Note 11)	600			Ω
Output Current					3.5	mA
Power Supplies						
Power Supply Current						
Normal Operation (PDN = "H")						
AVDD				60	-	mA
DVDD(fs=44.1kHz)				3	-	mA
DVDD(fs=96kHz)				5	-	mA
AVDD + DVDD					90	mA
Power-Down Mode (PDN = "L")						
AVDD + DVDD		(Note 12)		10	50	μA
Power Supply Rejection		(Note 13)		50		dB

Notes: 5. At 44.1kHz, measured by Audio Precision, System Two. Averaging mode.
At 96kHz, measured by ROHDE & SCHWARZ, UPD. Averaging mode.
Refer to the eva board manual.
6. 101dB at 16bit data and 116dB at 20bit data.
7. By Figure12. External LPF Circuit Example 2.
8. S/N does not depend on input bit length.
9. The voltage on (VREFH-VREFL) is held +5V externally.
10. Full-scale voltage (0dB). Output voltage scales with the voltage of (VREFH-VREFL).
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = ±2.4Vpp×(VREFH-VREFL)/5.
11. For AC-load. 1kΩ for DC-load.
12. In the power-down mode. P/S = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.
13. PSR is applied to AVDD, DVDD with 1kHz, 100mVpp. VREFH pin is held +5V.

FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; fs = 44.1kHz; Normal Speed Mode; DEM = OFF)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband ±0.01dB (Note 14)		PB	0		20.0	kHz
-6.0dB			-	22.05	-	kHz
Stopband (Note 14)		SB	24.1			kHz
Passband Ripple		PR			± 0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 15)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response 0 ~ 20.0kHz			-	± 0.2	-	dB

Note: 14. The passband and stopband frequencies scale with fs.
For example, PB = 0.4535×fs (@±0.01dB), SB = 0.546×fs.

15. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

FILTER CHARACTERISTICS (fs = 96kHz)

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; fs = 96kHz; Double Speed Mode; DEM = OFF)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband ±0.01dB (Note 14)		PB	0		43.5	kHz
-6.0dB			-	48.0	-	kHz
Stopband (Note 14)		SB	52.5			kHz
Passband Ripple		PR			± 0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 15)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response 0 ~ 40.0kHz			-	± 0.3	-	dB

DC CHARACTERISTICS

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%DVDD	V
Input Leakage Current	(Note 16)	Iin	-	-	± 10	μA

Note: 16. DFS and P/S pins have internal pull-down or pull-up devices, nominally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; C_L = 20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing (Note 17)					
Normal Speed: 256fs, Double Speed: 128fs	fCLK	7.7		13.824	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
Normal Speed: 384fs, Double Speed: 192fs	fCLK	11.5		20.736	MHz
Pulse Width Low	tCLKL	20			ns
Pulse Width High	tCLKH	20			ns
Normal Speed: 512fs, Double Speed: 256fs	fCLK	15.4		27.648	MHz
Normal Speed: 768fs, Double Speed: 384fs	fCLK	23.0		41.472	MHz
Pulse Width Low	tCLKL	7			ns
Pulse Width High	tCLKH	7			ns
LRCK Frequency (Note 18)					
Normal Speed Mode (DFS = "L")	fsn	30	44.1	54	kHz
Double Speed Mode (DFS = "H")	fsd	60	88.2	108	kHz
Duty Cycle	Duty	45		55	%
Serial Interface Timing					
BICK Period	tBCK	140			ns
BICK Pulse Width Low	tBCKL	60			ns
Pulse Width High	tBCKH	60			ns
BICK "↑" to LRCK Edge (Note 19)	tBLR	20			ns
LRCK Edge to BICK "↑" (Note 19)	tLRB	20			ns
SDATA Hold Time	tSDH	20			ns
SDATA Setup Time	tSDS	20			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Reset Timing					
PDN Pulse Width (Note 20)	tPW	150			ns

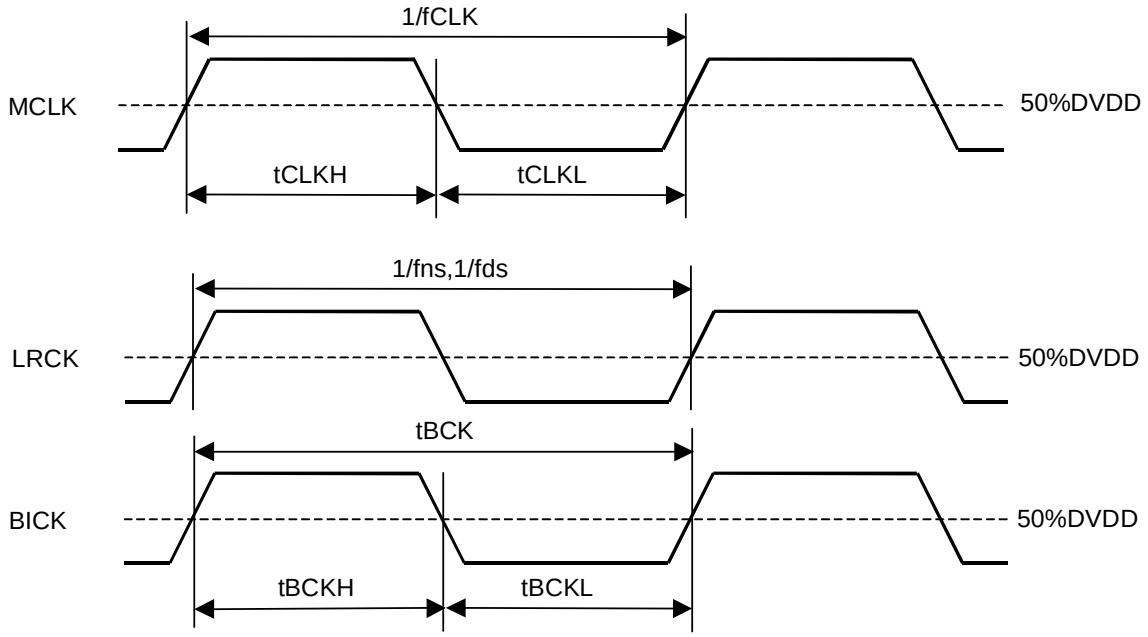
Notes: 17. **For Double Speed mode please see Appendix A for relationship of MCLK and BCLK/LRCK.**

18. When the normal and double speed modes are switched, AK4393 should be reset by PDN pin or RSTN bit.

19. BICK rising edge must not occur at the same time as LRCK edge.

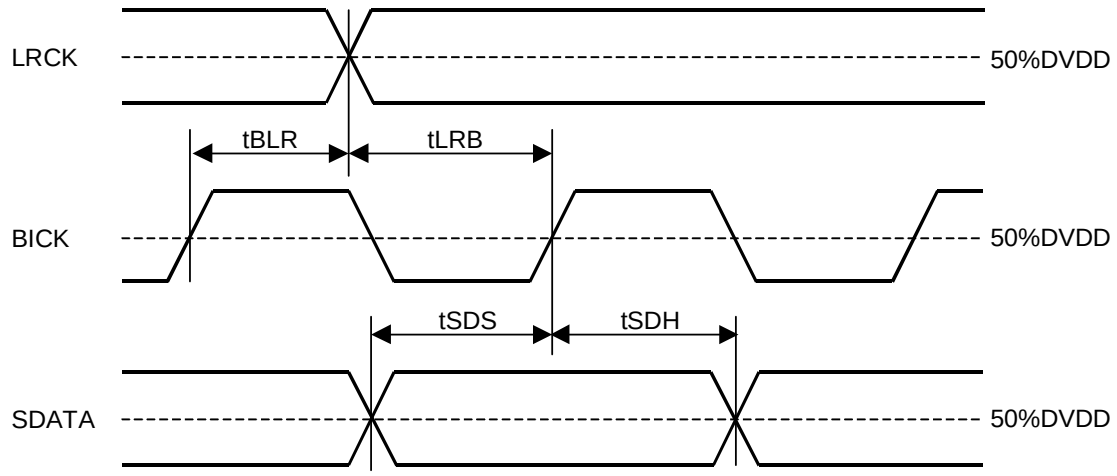
20. The AK4393 can be reset by bringing PDN "L" to "H".
When the states of CKS2-0 or DFS change, the AK4393 should be reset by PDN pin or RSTN bit.

■ **Timing Diagram**

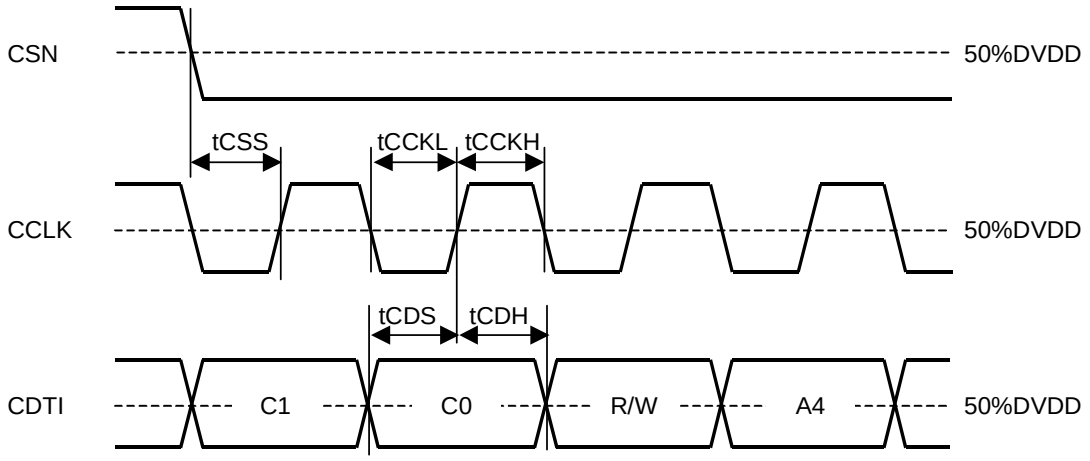


Clock Timing

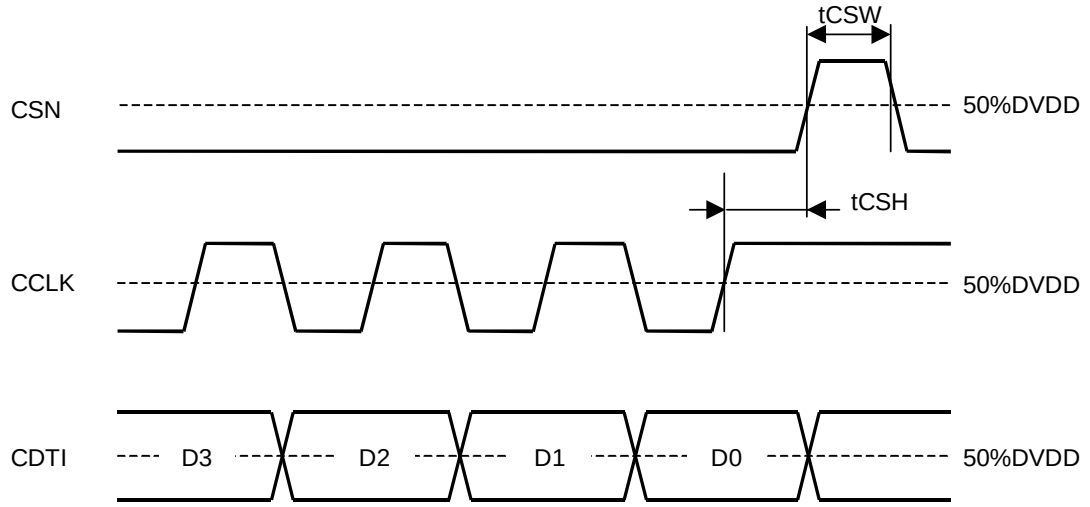
For Double Speed mode timing please see Appendix A for relationship of MCLK and BCLK/LRCK.



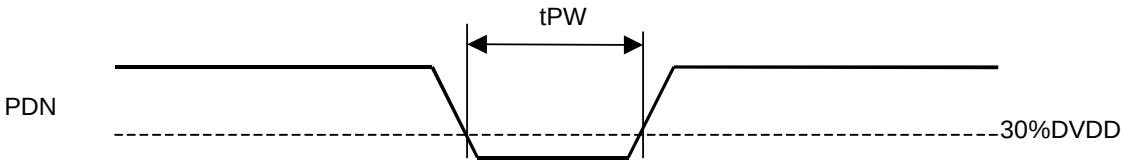
Audio Interface Timing



WRITE Command Input Timing



WRITE Data Input Timing



Power-down Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4393, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. **However, in Double Speed Mode, the phase relationship between MCLK and LRCK/BICK is limited. (Refer to Appendix A).** The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The sampling speed is set by DFS (Table 1). The sampling rate (LRCK), CKS0/1/2 and DFS determine the frequency of MCLK (Table 2).

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4393 is in normal operation mode (PDN = "H"). If these clocks are not provided, the AK4393 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4393 should be in the power-down mode (PDN = "L") or in the reset mode (RSTN = "0"). After exiting reset at power-up etc., the AK4393 is in power-down mode until MCLK and LRCK are input.

DFS	Sampling Rate (fs)		
0	Normal Speed Mode	30kHz~54kHz	Default
1	Double Speed Mode	60kHz~108kHz	

Table 1. Sampling Speed

Mode	CKS2	CKS1	CKS0	Normal	Double	
0	0	0	0	256fs	128fs	Default
1	0	0	1	256fs	256fs	
2	0	1	0	384fs	192fs	
3	0	1	1	384fs	384fs	
4	1	0	0	512fs	256fs	
5	1	0	1	512fs	N/A	
6	1	1	0	768fs	384fs	
7	1	1	1	768fs	N/A	

Table 2. System Clocks

LRCK	MCLK				BICK
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz

Table 3. System clock example (Normal Speed Mode)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 4. System clock example (Double Speed Mode)

■ Audio Serial Interface Format

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Five data formats are supported and selected by the DIF0-2 as shown in Table 5. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	Mode	BICK	Figure
0	0	0	0	0: 16bit LSB Justified	≥32fs	Figure 1
1	0	0	1	1: 20bit LSB Justified	≥40fs	Figure 2
2	0	1	0	2: 24bit MSB Justified	≥48fs	Figure 3
3	0	1	1	3: I^2S Compatible	≥48fs	Figure 4
4	1	0	0	4: 24bit LSB Justified	≥48fs	Figure 2

Table 5. Audio Data Formats

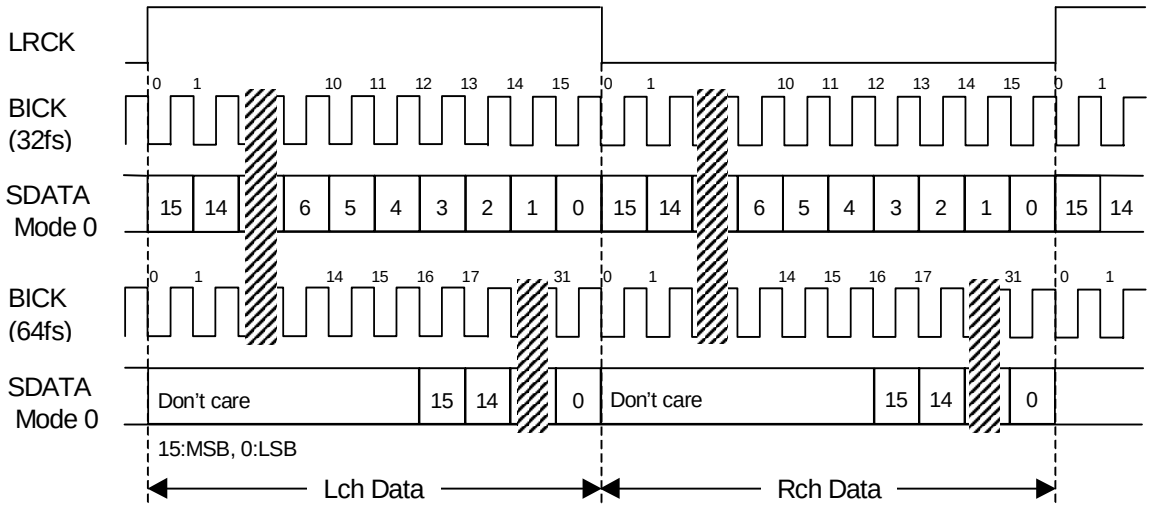


Figure 1. Mode 0 Timing

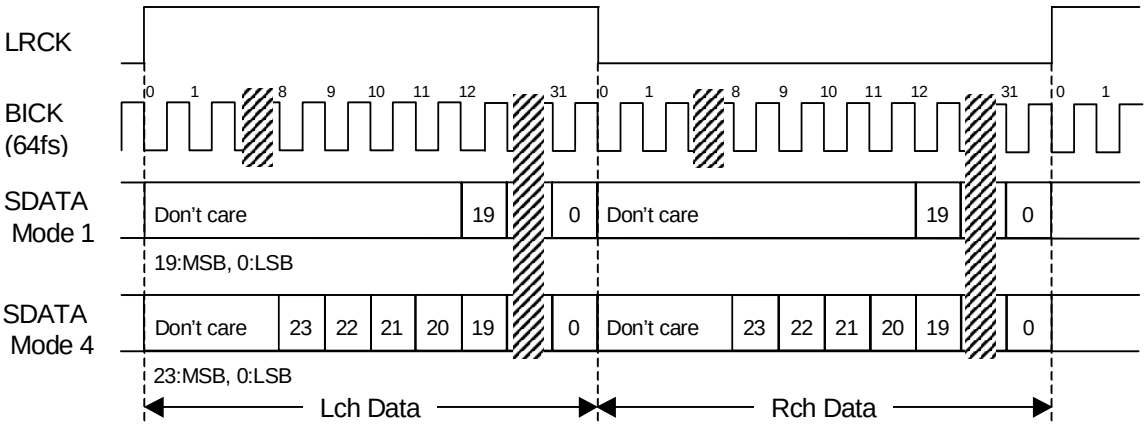


Figure 2. Mode 1,4 Timing

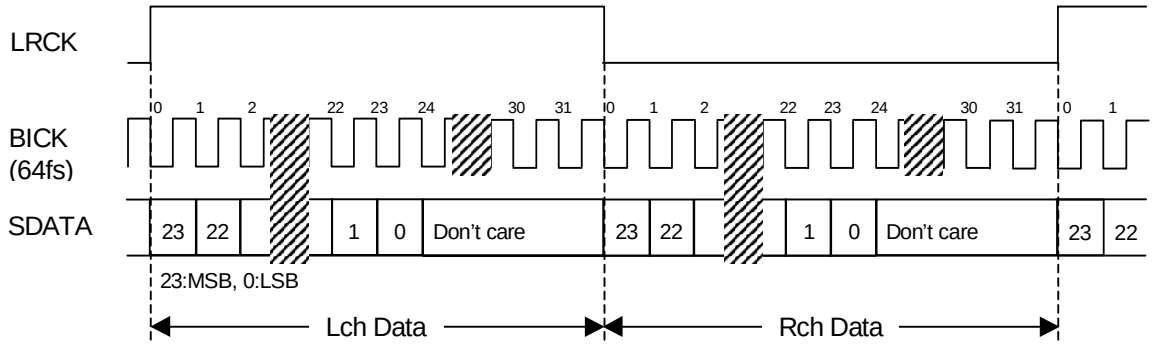


Figure 3. Mode 2 Timing

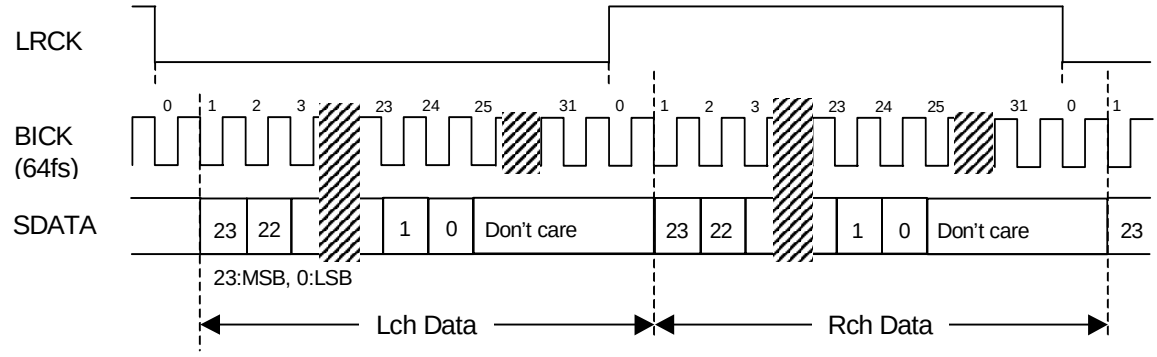


Figure 4. Mode 3 Timing

■ De-emphasis filter

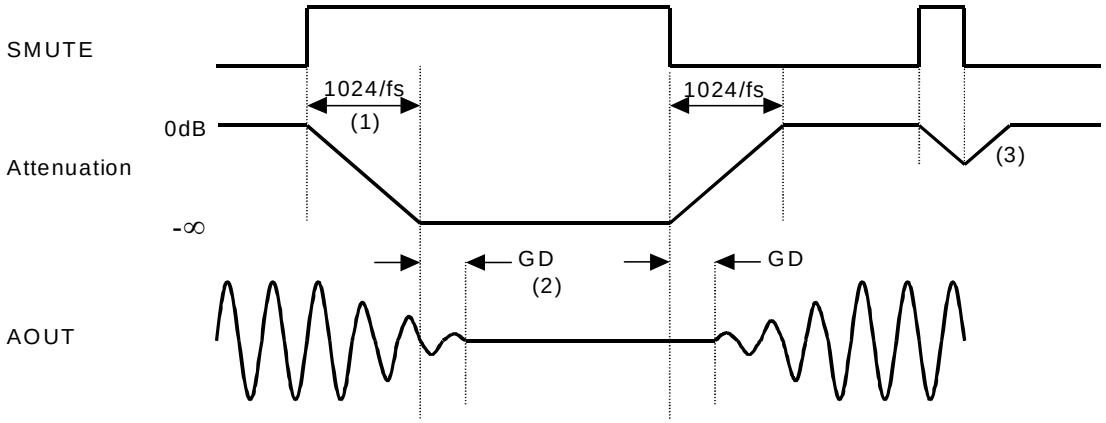
A digital de-emphasis filter is available for 32, 44.1, 48 or 96kHz sampling rates (tc = 50/15μs) and is enabled or disabled with the DEM0, DEM1 and DFS input pins.

DEM1	DEM0	DFS	Mode	
0	0	0	44.1kHz	Default
0	1	0	OFF	
1	0	0	48kHz	
1	1	0	32kHz	
0	0	1	OFF	
0	1	1	OFF	
1	0	1	96kHz	
1	1	1	OFF	

Table 6. De-emphasis filter control

■ Soft mute operation

Soft mute operation is performed at digital domain. When SMUTE goes to "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

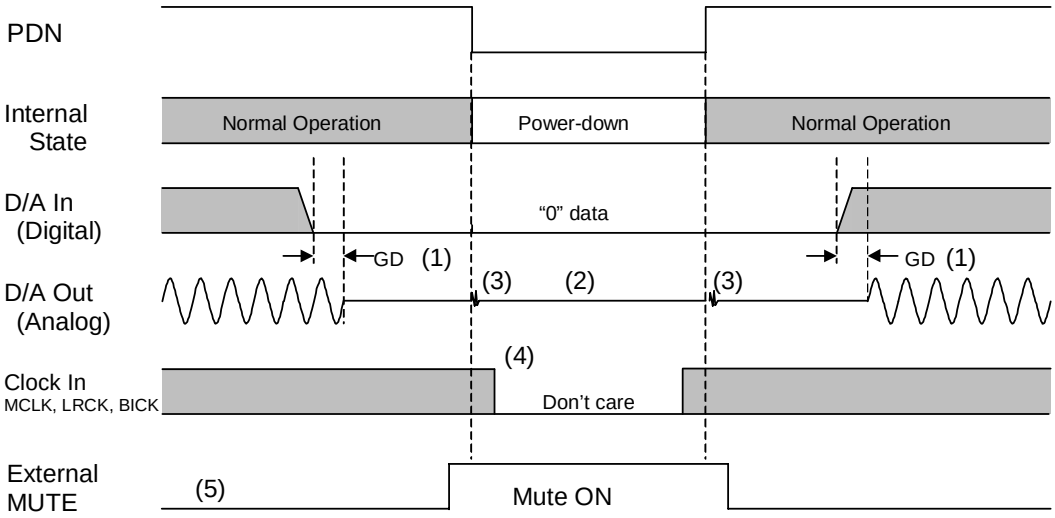
Figure 5. Soft mute operation

■ System Reset

The AK4393 should be reset once by bringing PDN = "L" upon power-up. The AK4393 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4393 is in the power-down mode until MCLK and LRCK are input.

■ Power-Down

The AK4393 is placed in the power-down mode by bringing PDN pin "L" and the anlog outputs are floating (Hi-Z). Figure 6 shows an example of the system timing at the power-down and power-up.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = "L").
(5) Please mute the analog output externally if the click noise (3) influences system application. The timing example is shown in this figure.

Figure 6. Power-down/up sequence example

■ Click Noise from analog output

Click noise occurs from analog output in the following cases.

1) When switching de-emphasis mode by DEM0, DEM1 and DFS pins,
2) When switching serial data mode by DIF0, DIF1 and DIF2 pins,
3) When going and exiting power down mode by PDN pin,
4) When switching normal speed and double speed by DFS pin,

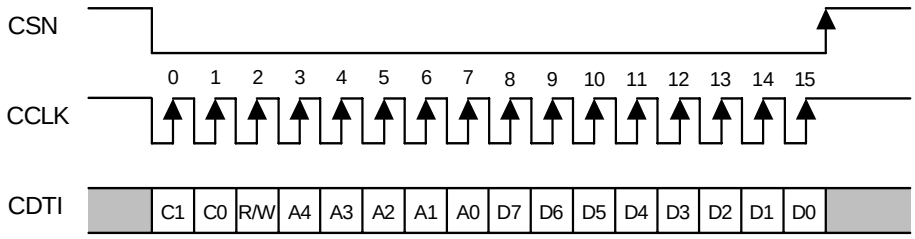
However in case of 1) & 2), If the input data is "0" or the soft mute is enabled (after 1024 LRCK cycles from SMUTE = "H"), no click noise occur except for switching DFS pin.

■ Mode Control Interface

Pins (parallel control mode) or registers (serial control mode) can control each functions of the AK4393. For DIF2-0, CKS2-0 and DFS, the setting of pin and register are "ORed" internally. So, even serial control mode, pin setting can also control these functions.

The serial control interface is enabled by the P/S pin = "L". In this mode, pin setting must be all "L". Internal registers may be written by 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2bits, C1/0; fixed to "01"), Read/Write (1bit; fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). The AK4393 latches the data on the rising edge of CCLK, so data should be clocked in on the falling edge. The writing of data becomes valid by CSN "↑". The clock speed of CCLK is 5MHz(max). The CSN and CCLK must be fixed to "H" when the register does not be accessed.

PDN = "L" resets the registers to their default values. When the state of P/S pin is changed, the AK4393 should be reset by PDN = "L". In serial mode, the internal timing circuit is reset by RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 7. Control I/F Timing

*The AK4393 does not support the read command and chip address. C1/0 and R/W are fixed to "011"
*When the AK4393 is in the power down mode (PDN = "L") or the MCLK is not provided, writing into the control register is inhibited.
*For setting the registers, the following sequence is recommended.

- Control 1 register
  (1) Writing RSTN = "0" and other bits (D6-D1) to the register at the same time.
  (2) Writing RSTN = "1" to the register. The other bits are no change.
- Control 2 register
  This writing sequence has no limitation like control 1 register.

*When RSTN = "0", the click noise is output from AOUT pins.
*If the mode setting is done without setting RSTN = "0", large noise may be output from AOUT pins. (Especially when CKS0/1/2 are changed.)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	CKS2	CKS1	CKS0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	0	0	DFS	DEM1	DEM0	SMUTE
02H	Test	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0

Notes:

For addresses from 03H to 1FH, data must not be written.

When PDN pin goes to "L", the registers are initialized to their default values. When RSTN bit goes to "0", the only internal timing is reset and the registers are not initialized to their default values. DIF2-0, CKS2-0 and DFS bits are ORed with pins respectively.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	CKS2	CKS1	CKS0	DIF2	DIF1	DIF0	RSTN
default		0	0	0	0	0	0	0	1

RSTN: Internal timing reset

0: Reset. All registers are not initialized.

1: Normal Operation

When the states of CKS2-0 or DFS change, the AK4393 should be reset by PDN pin or RSTN bit.

DIF2-0: Audio data interface modes (see Table 5)

Initial: "000", Mode 0

Register bits are ORed with DIF2-0 pins if P/S = "L".

CKS2-0: Master Clock Frequency Select (see Table 2)

Initial: "000", Mode 0

Register bits are ORed with CKS2-0 pins if P/S = "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	0	0	DFS	DEM1	DEM0	SMUTE
default		0	0	0	0	0	0	0	0

SMUTE: Soft Mute Enable

0: Normal operation

1: DAC outputs soft-muted

DEM1-0: De-emphasis response (see Table 6)

Initial: "00", 44.1kHz

DFS: Sampling speed control (see Table 1)

0: Normal speed

1: Double speed

Register bit is ORed with DFS pin if P/S = "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Test	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
default		0	0	0	0	0	0	0	0

TEST7-0: Test mode. Do not write any data to 02H.

SYSTEM DESIGN

Figure 8 and 9 show the system connection diagram. An evaluation board (AKD4393) is available which demonstrates the optimum layout, power supply arrangements and measurement results.

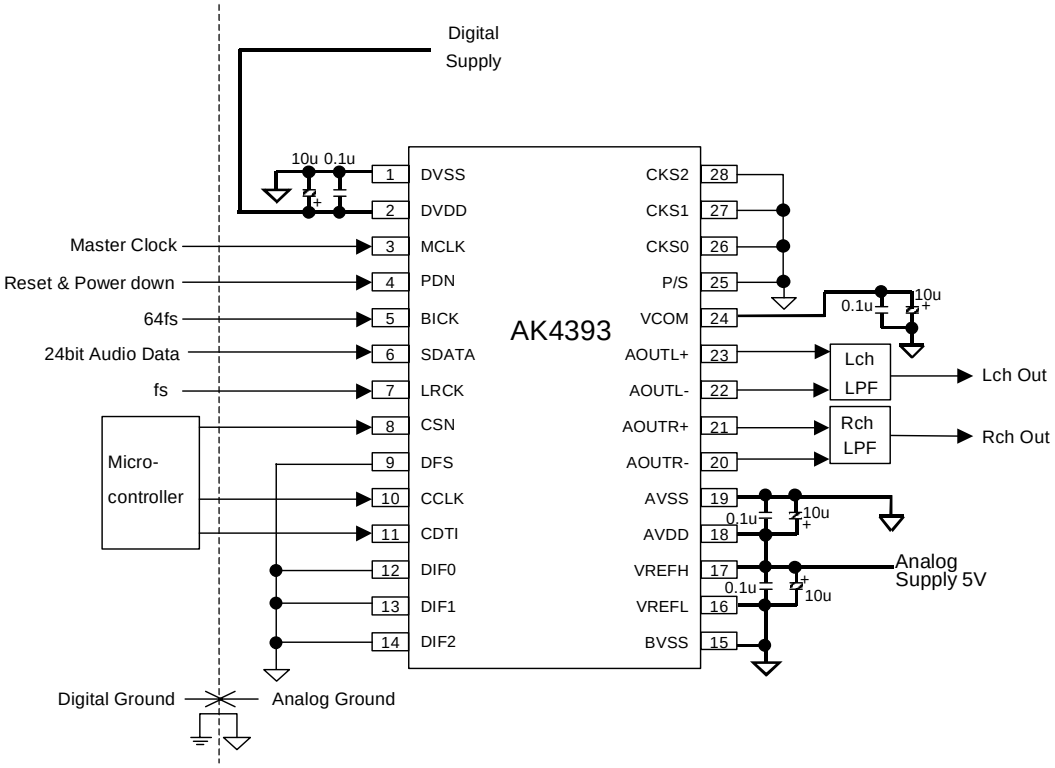


Figure 8. Typical Connection Diagram (Serial mode)

Notes:

- LRCK = fs, BICK = 64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS, BVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

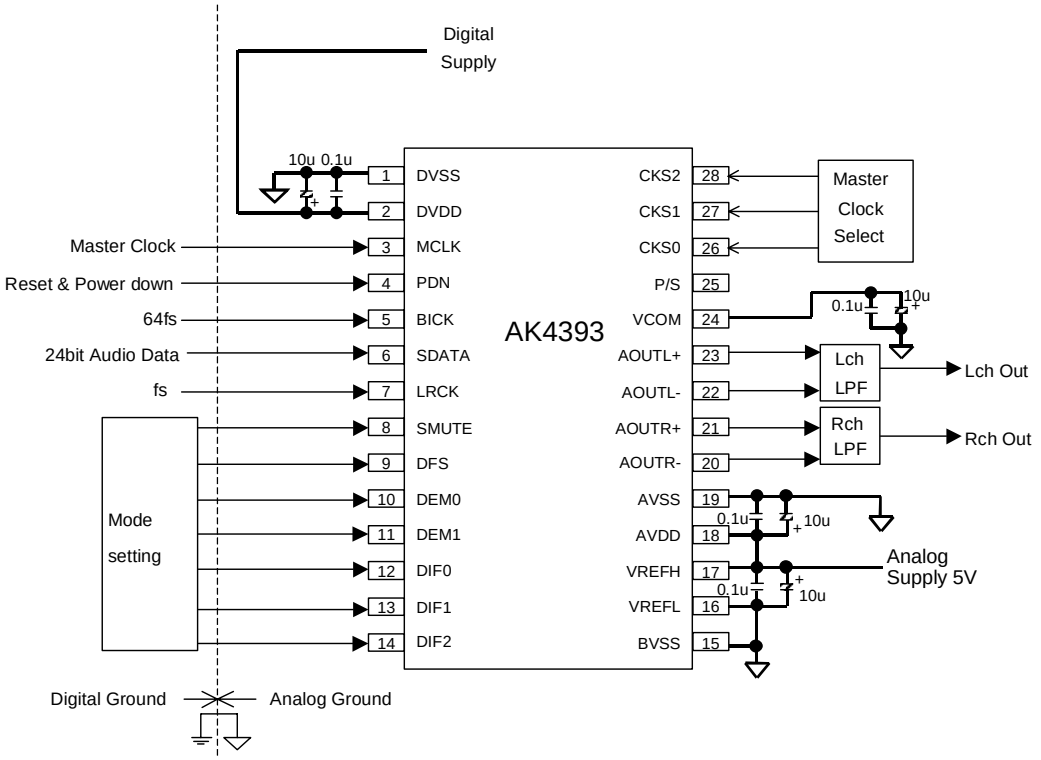


Figure 9. Typical Connection Diagram (Parallel mode)

Notes:

- LRCK = fs, BICK = 64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS, BVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

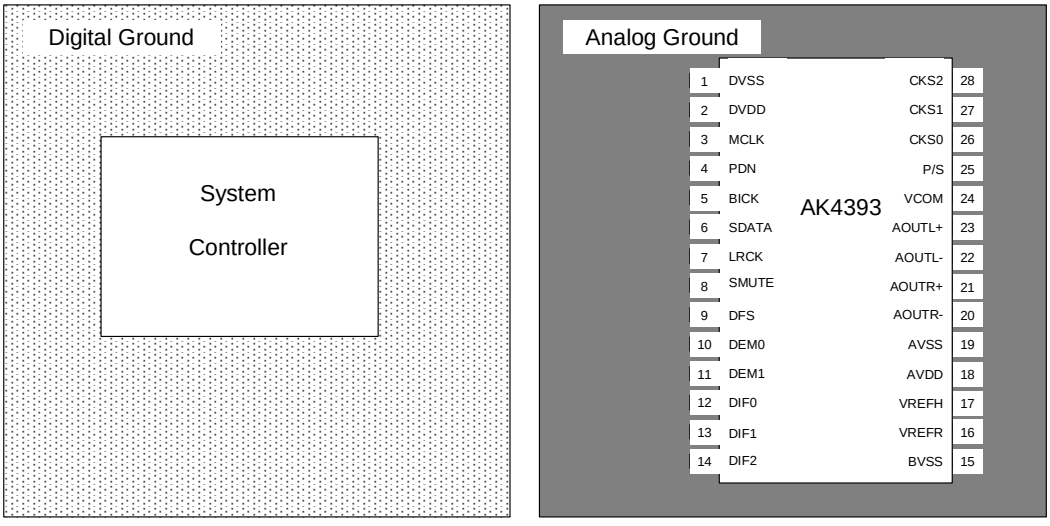


Figure 10. Ground Layout

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from digital supply in system. If AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS, BVSS and DVSS must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible.

2. Voltage Reference

The differential Voltage between VREFH and VREFL set the analog output range. VREFH pin is normally connected to AVDD and VREFL pin is normally connected to AVSS. VREFH and VREFL should be connected with a 0.1µF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH, VREFL and VCOM pins in order to avoid unwanted coupling into the AK4393.

3. Analog Outputs

The analog outputs are full differential outputs and 2.4Vpp (typ@VREF=5V) centered around VCOM. The differential outputs are summed externally, V_{AOUT} = (AOUT+) - (AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 4.8Vpp (typ@VREF=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage (V_{AOUT}) is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal V_{AOUT} is 0V for 000000H(@24bit).

The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

Figure 11 shows an example of external LPF circuit summing the differential outputs by an op-amp.
Figure 12 shows an example of differential outputs and LPF circuit example by three op-amps.

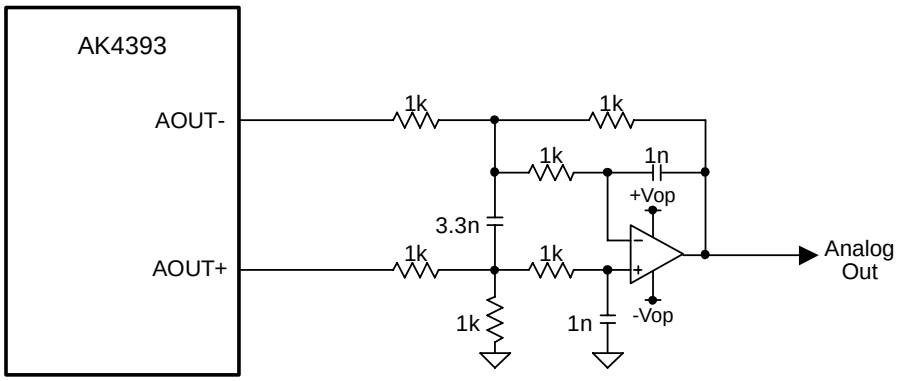


Figure 11. External LPF Circuit Example 1

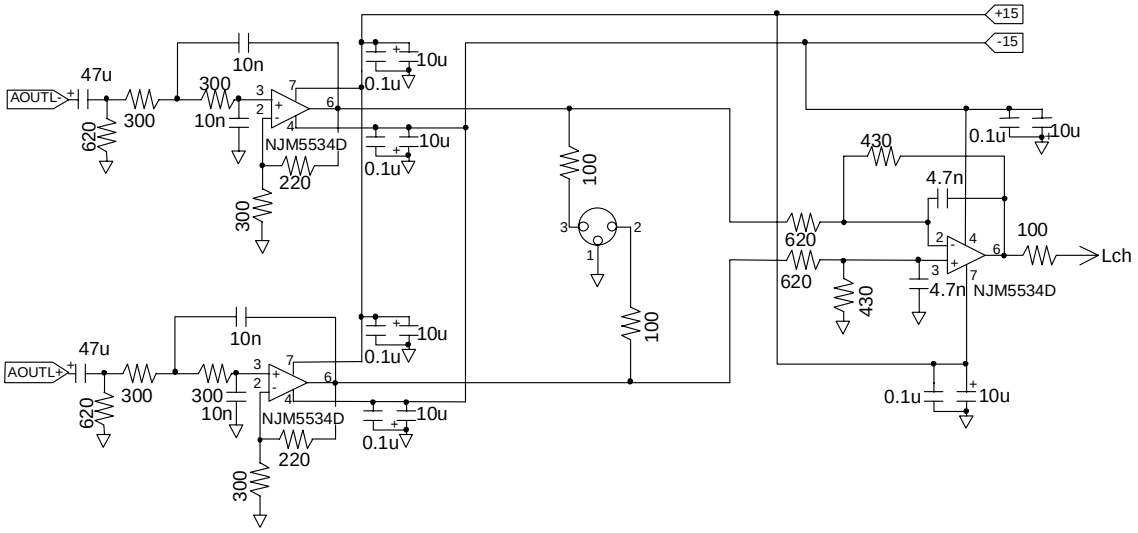
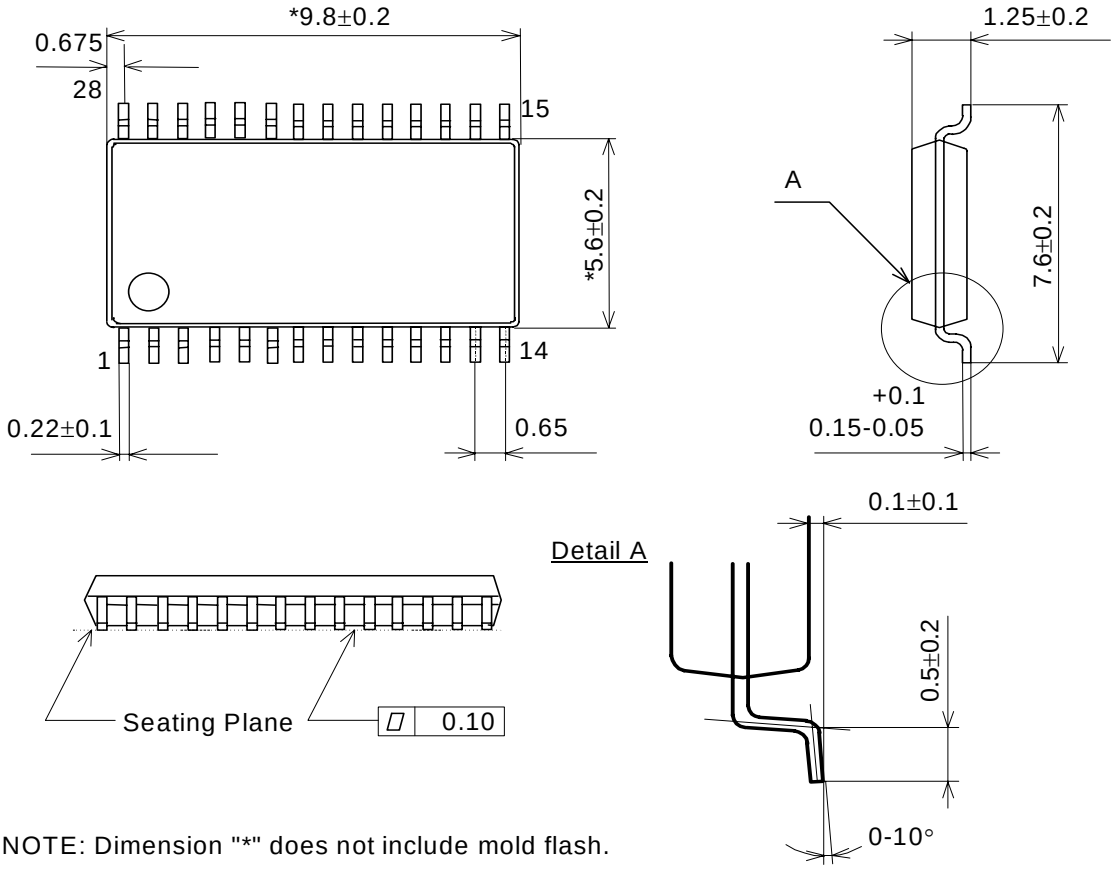


Figure 12. External LPF Circuit Example 2

PACKAGE

28pin VSOP (Unit: mm)

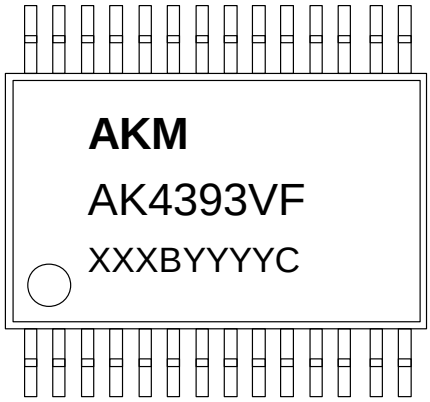


NOTE: Dimension "*" does not include mold flash.

■ **Material & Lead finish**

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

MARKING



XXXXBYYYYC data code identifier

XXXB: Lot number (X : Digit number, B : Alpha character)
YYYYC: Assembly date (Y : Digit number C : Alpha character)

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Appendix A

In Double Speed Mode, the phase relationship between MCLK and LRCK/BICK is limited (Table 7). If the phase relationship happens during this prohibited period, it is possible to occur the inverse of output channel. The phase relationship must be set to avoid the prohibited period when the AK4393 operates at Double Speed Mode. The prohibited period is specified by the combination of digital power supply voltage (DVDD), MCLK frequency and audio data format (Table 5). When the audio data formats are 16/20/24bit LSB Justified (Mode 0,1,4) and 24bit MSB Justified (Mode 2), the phase relationship (tLRM: Figure 11) between the rising edge of LRCK and the rising edge of MCLK has the prohibited period of min to max in Table 7. In case of I^2S Compatible (Mode 3), the relationship between the falling edge of BICK and the rising edge of MCLK has the prohibited period (tBCM: Figure 12)

Sampling Mode	Digital Power Supply, DVDD	MCLK Frequency	Mode Setting				Prohibited Period		Units
			CKS2	CKS1	CKS0	DFS	min	max	
Double Speed	3.0 to 5.25V	128fs	0	0	0	1	0.4	1.7	ns
Double Speed	3.0 to 5.25V	192fs	0	1	0	1	-0.5	0.8	ns
Double Speed	3.0 to 5.25V	256fs	0	0	1	1	-0.7	0.7	ns
Double Speed	3.0 to 5.25V	256fs	1	0	0	1	-0.7	0.7	ns
Double Speed	3.0 to 5.25V	384fs	0	1	1	1	-1.7	-0.3	ns
Double Speed	3.0 to 5.25V	384fs	1	1	0	1	-1.7	-0.3	ns
Double Speed	4.75 to 5.25V	128fs	0	0	0	1	0.8	1.5	ns
Double Speed	4.75 to 5.25V	192fs	0	1	0	1	-0.2	0.5	ns
Double Speed	4.75 to 5.25V	256fs	0	0	1	1	-0.3	0.4	ns
Double Speed	4.75 to 5.25V	256fs	1	0	0	1	-0.3	0.4	ns
Double Speed	4.75 to 5.25V	384fs	0	1	1	1	-1.0	-0.3	ns
Double Speed	4.75 to 5.25V	384fs	1	1	0	1	-1.0	-0.3	ns

Table **7**. Prohibited Period

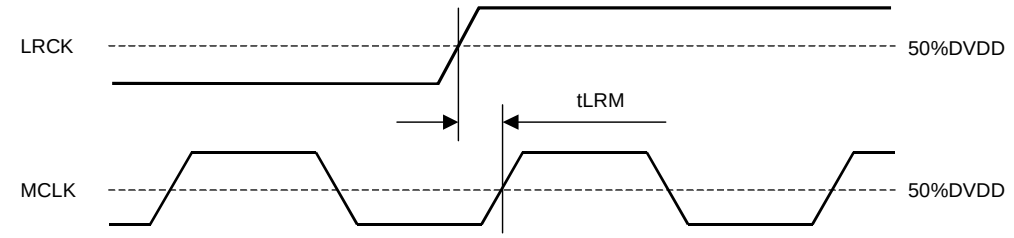


Figure 11. 16/20/24bit LSB Justified, 24bit MSB Justified

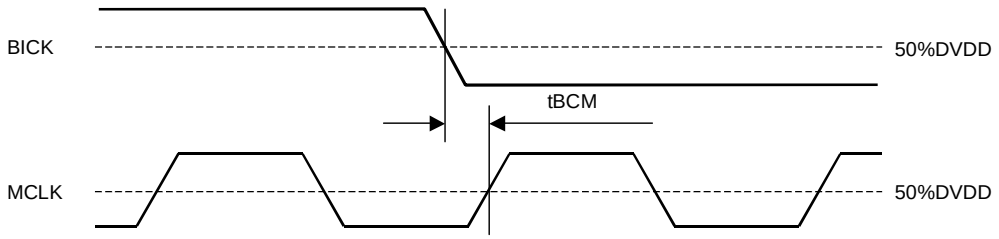


Figure 12. I^2S Compatible

AK5393

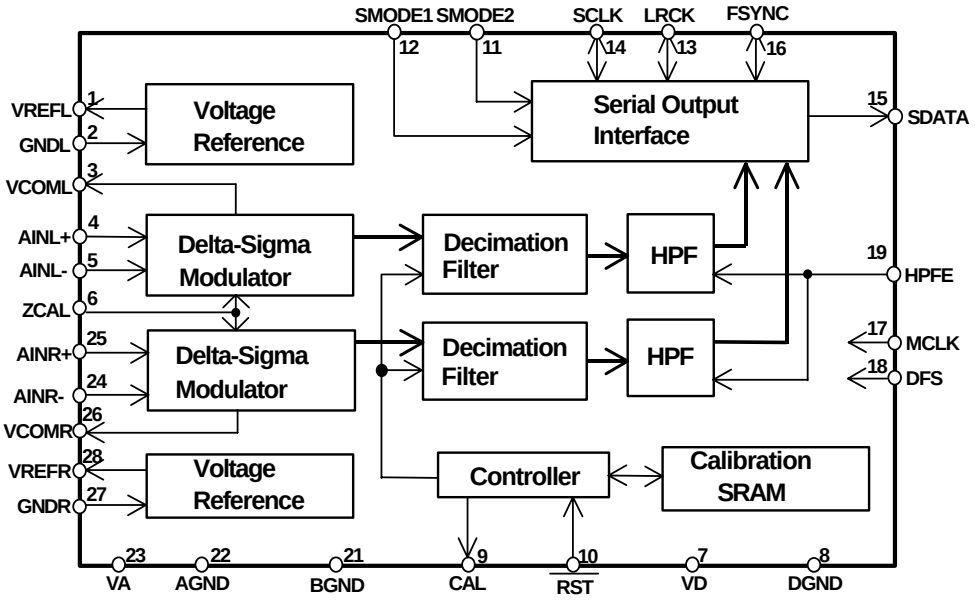
Enhanced Dual Bit ΔΣ 96kHz 24-Bit ADC

GENERAL DESCRIPTION

The AK5393 is a 24bit, 128x oversampling 2ch A/D Converter for professional digital audio systems. The modulator in the AK5393 uses the new developed Enhanced Dual Bit architecture. This new architecture achieves the wide dynamic range, while keeping much the same superior distortion characteristics as conventional Single Bit way. The AK5393 performs 117dB dynamic range, so the device is suitable for professional studio equipment such as digital mixer, digital VTR etc.

FEATURES

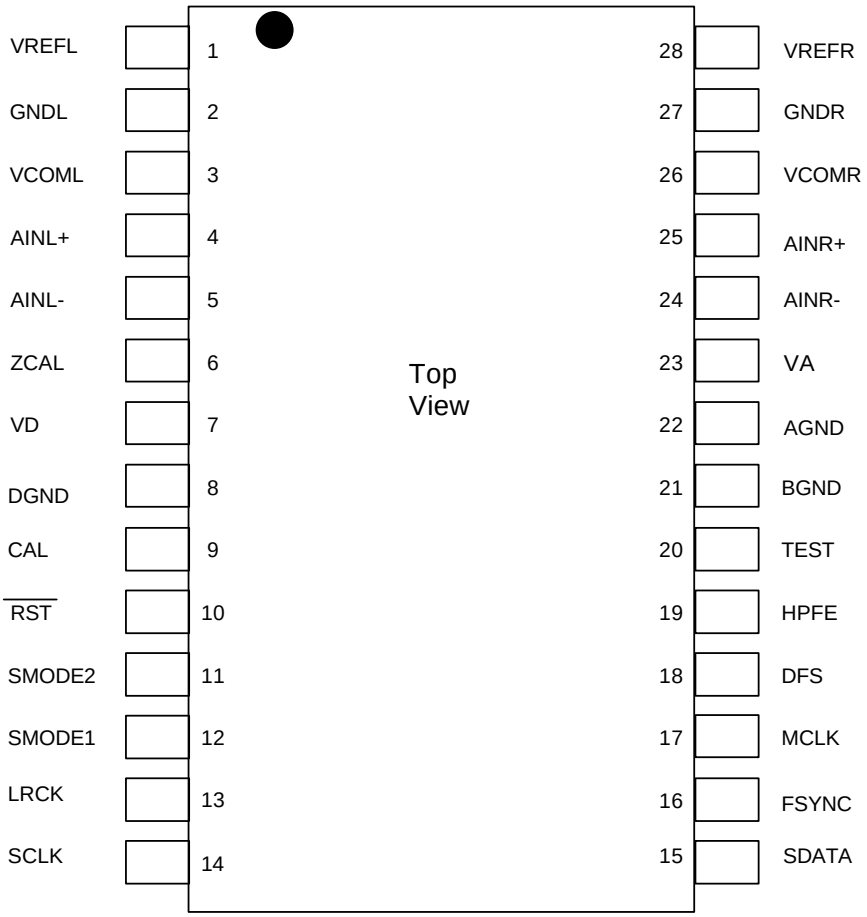
- **Enhanced Dual Bit ADC**
- **Sampling Rate: 1kHz~108kHz**
- **Full Differential Inputs**
- **S/(N+D): 105dB**
- **DR: 117dB**
- **S/N: 117dB**
- **High Performance Linear Phase Digital Anti-Alias filter**
  - **Passband: 0~21.768kHz(@fs=48kHz)**
  - **Ripple: 0.001dB**
  - **Stopband: 110dB**
- **Digital HPF & Offset Calibration for Offset Cancel**
- **Power Supply: 5V±5%(Analog), 3~5.25V(Digital)**
- **Power Dissipation: 470mW**
- **Package: 28pin SOP**
- **AK5392 Pin compatible**



■ Ordering Guide

AK5393-VS	–10 ~ +70°C	28pin SOP
AKD5393	AK5393 Evaluation Board	

■ Pin Layout



■ Compatibility with AK5392

	AK5392	AK5393
Pin 18	CMODE	DFS
fs (max)	54kHz	108kHz
MCLK (DFS ="L"@fs=48kHz)	256fs/384fs	256fs
MCLK (DFS ="H"@fs=96kHz)	N/A	128fs

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VREFL	O	Lch Reference Voltage Pin, 3.75V Normally connected to GNDL with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.
2	GNDL	-	Lch Reference Ground Pin, 0V
3	VCOML	O	Lch Common Voltage Pin, 2.75V
4	AINL+	I	Lch Analog positive input Pin
5	AINL-	I	Lch Analog negative input Pin
6	ZCAL	I	Zero Calibration Control Pin This pin controls the calibration reference signal. "L" :VCOML and VCOMR "H" : Analog Input Pins (AINL±, AINR±)
7	VD	-	Digital Power Supply Pin, 3.3V
8	DGND	-	Digital Ground Pin, 0V
9	CAL	O	Calibration Active Signal Pin "H" means the offset calibration cycle is in progress. Offset calibration starts when $\overline{\text{RST}}$ goes "H". CAL goes "L" after 8704 LRCK cycles for DFS="L", 17408 LRCK cycles for DFS ="H".
10	$\overline{\text{RST}}$	I	Reset Pin When "L", Digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up.
11 12	SMODE2 SMODE1	I I	Serial Interface Mode Select Pin MSB first, 2's compliment. SMODE2 SMODE1 MODE LRCK L L Slave mode : MSB justified : H/L L H Master mode : Similar to I^2S : H/L H L Slave mode : I^2S : L/H H H Master mode : I^2S : L/H
13	LRCK	I/O	Left/Right Channel Select Clock Pin LRCK goes "H" at SMODE2="L" and "L" at SMODE2="H" during reset when SMODE1 "H".

14	SCLK	I/O	Serial Data Clock Pin Data is clocked out on the falling edge of SCLK. Slave mode: SCLK requires more than 48fs clock. Master mode: SCLK outputs a 128fs(DFS="L") or 64fs(DFS="H") clock. SCLK stays "L" during reset.
15	SDATA	O	Serial Data Output Pin MSB first, 2's complement. SDATA stays "L" during reset.
16	FSYNC	I/O	Frame Synchronization Signal Pin Slave mode: When "H", the data bits are clocked out on SDATA. In I^2S mode, FSYNC is don't care. Master mode: FSYNC outputs 2fs clock. FSYNC stays "L" during reset.
17	MCLK	I	Master Clock Input Pin 256fs at DFS="L", 128fs at DFS="H".
18	DFS	I	Double Speed Sampling Mode Pin "L": Normal Speed "H": Double Speed
19	HPFE	I	High Pass Filter Enable Pin "L": Disable "H": Enable
20	TEST	I	Test Pin (pull-down pin) Should be connected to GND.
21	BGND	-	Substrate Ground Pin, 0V
22	AGND	-	Analog Ground Pin, 0V
23	VA	-	Analog Supply Pin, 5V
24	AINR-	I	Rch Analog negative input Pin
25	AINR+	I	Rch Analog positive input Pin
26	VCOMR	O	Rch Common Voltage Pin, 2.75V
27	GNDR	-	Rch Reference Ground Pin, 0V
28	VREFR	O	Rch Reference Voltage Pin, 3.75V Normally connected to GNDR with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor

Note: All digital inputs should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AGND,BGND,DGND=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	VA	-0.3	6.0	V
Digital	VD	-0.3	6.0	V
|BGND-DGND| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Analog Input Voltage	VINA	-0.3	VA+0.3	V
Digital Input Voltage	VIND	-0.3	VD+0.3	V
Ambient Temperature (power applied)	Ta	-10	70	°C
Storage Temperature	Tstg	-65	150	°C

Notes: 1. All voltages with respect to ground.
2. AGND, BGND and DGND must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND,BGND,DGND=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog	VA	4.75	5.0	5.25	V
(Note 3) Digital	VD	3.0	3.3	5.25	V

Notes: 1. All voltages with respect to ground.
3. The power up sequence between VA and VD is not critical.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA=5.0V; VD=3.3V; AGND,BGND,DGND=0V; fs=48kHz; Signal Frequency=1kHz;
24bit Output; Measurement frequency=10Hz~20kHz; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					24	Bits
Analog Input Characteristics:						
S/(N+D)	fs=48kHz	-1dBFS	98	105		dB
		-20dBFS	-	94		dB
		-60dBFS	-	54		dB
	fs=96kHz	-1dBFS	96	103		dB
	BW=40kHz	-20dBFS	-	85		dB
		-60dBFS	-	45		dB
Dynamic Range (-60dBFS with A-Weighted)			112	117		dB
S/N (A-Weighted)			112	117		dB
Interchannel Isolation			110	120		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift					150	ppm/°C
Offset Error	after calibration, HPF=OFF			±200	±1000	LSB_{24}
	after calibration, HPF=ON			±1		LSB_{24}
Offset Drift	(HPF=OFF)		-	±10	-	LSB_{24}/°C
Offset Calibration Range	(HPF=OFF)			±50		mV
Input Voltage (AIN+)-(AIN-)			±2.3	±2.45	±2.6	V
Input Impedance			2.4	4		kΩ
Power Supplies						
Power Supply Current						
VA				90	130	mA
VD (fs=48kHz; DFS="L")				6	9	mA
(fs=96kHz; DFS="H")				9	14	mA
Power Dissipation				470	680	mW
Power Supply Rejection (Note 4)				70		dB

Note: 4. DC to 26kHz. 110dB(typ) beyond 26kHz.

FILTER CHARACTERISTICS(fs=48kHz)

(Ta=25°C; VA=5.0V±5%; VD=3.0~5.25V; fs=48kHz, DFS="L")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband (Note 5)		PB	0		21.768	kHz
Stopband (Note 5)		SB	26.232			kHz
Passband Ripple		PR			±0.001	dB
Stopband Attenuation (Note 6)		SA	110			dB
Group Delay Distortion		ΔGD		0		us
Group Delay (Note 7)		GD		38.7		1/fs
ADC Digital Filter(HPF):						
Frequency response (Note 5)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz

FILTER CHARACTERISTICS(fs=96kHz)

(Ta=25°C; VA=5.0V±5%; VD=3.0~5.25V; fs=96kHz, DFS="H")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband (Note 5)		PB	0		43.536	kHz
Stopband (Note 5)		SB	52.464			kHz
Passband Ripple		PR			±0.003	dB
Stopband Attenuation (Note 8)		SA	110			dB
Group Delay Distortion		ΔGD		0		us
Group Delay (Note 7)		GD		38.8		1/fs
ADC Digital Filter(HPF):						
Frequency response (Note 5)	-3dB	FR		2.0		Hz
	-0.1dB			13.0		Hz

Notes: 5. The passband and stopband frequencies scale with fs.

6. The analog modulator samples the input at 6.144MHz for an output word rate of 48kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 6.144MHz ± 21.768kHz, where n=1,2,3…).
7. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register. 40.7/fs(DFS="L"),40.8/fs(DFS="H")typ. at HPF:ON.
8. The analog modulator samples the input at 6.144MHz for an output word rate of 96kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 6.144MHz ± 43.536kHz, where n=1,2,3…).

DIGITAL CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage Iout=-20µA	VOH	VD-0.1	-	-	V
Low-Level Output Voltage Iout=20µA	VOL	-		0.1	V
Input Leakage Current	Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V; C_L=20pF)

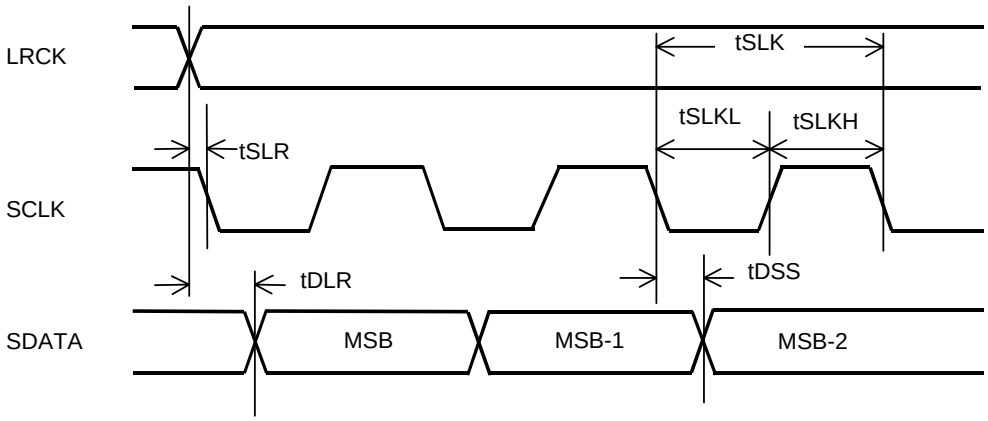
Parameter	Symbol	min	typ	max	Units
Control Clock Frequency					
Master Clock 256fs:	fCLK	0.256	12.288	13.824	MHz
Pulse width Low	tCLKL	29			ns
Pulse width High	tCLKH	29			ns
Serial Data Output Clock (SCLK)	fSLK		6.144	6.912	MHz
Channel Select Clock (LRCK)	fs	1	48	108	kHz
duty cycle		25		75	%
Serial Interface Timing (Note 9)					
Slave Mode(SMODE1="L")					
SCLK Period	tSLK	144.7			ns
SCLK Pulse width Low	tSLKL	65			ns
Pulse width High	tSLKH	65			ns
SCLK falling to LRCK Edge (Note 10)	tSLR	-45		45	ns
LRCK Edge to SDATA MSB Valid	tDLR			45	ns
SCLK falling to SDATA Valid	tDSS			45	ns
SCLK falling to FSYNC Edge	tSF	-45		45	ns
Master Mode(SMODE1="H")					
SCLK Frequency (DFS="L")	fSLK		128fs		Hz
SCLK Frequency (DFS="H")	fSLK		64fs		Hz
duty cycle			50		%
FSYNC Frequency	fFSYNC		2fs		Hz
duty cycle			50		%
SCLK falling to LRCK Edge	tSLR	-20		20	ns
LRCK Edge to FSYNC rising	tLRF		1		tslk
SCLK falling to SDATA Valid	tDSS			45	ns
SCLK falling to FSYNC Edge	tSF	-20		20	ns
Reset/Calibration timing					
$\overline{\text{RST}}$ Pulse width	tRTW	150			ns
$\overline{\text{RST}}$ falling to CAL rising	tRCR			50	ns
$\overline{\text{RST}}$ rising to CAL falling (Note 11)	tRCF		8704		1/fs
$\overline{\text{RST}}$ rising to SDATA Valid (Note 11)	tRTV		8960		1/fs

Notes: 9. Refer to Serial Data interface.

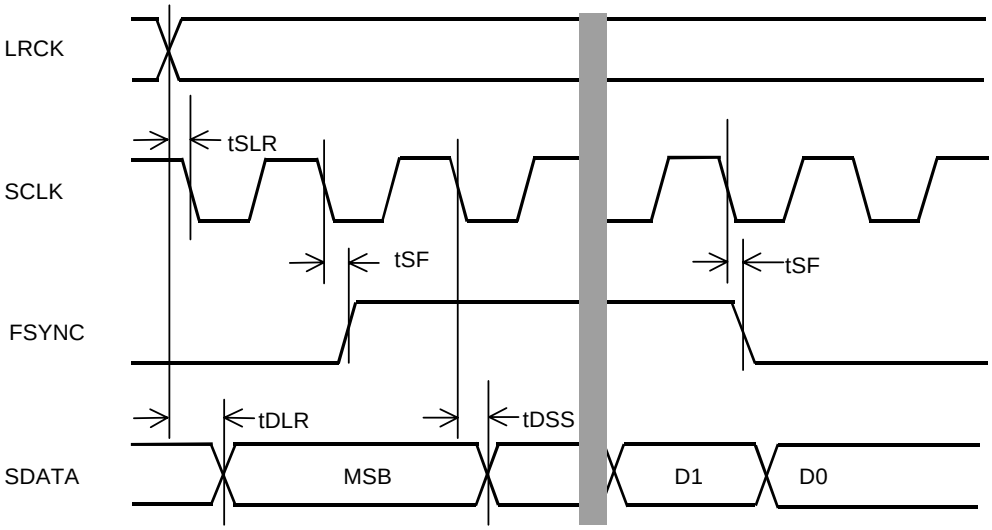
10. Specified LRCK edges not to coincide with the rising edges of SCLK.

11. The number of the LRCK rising edges after $\overline{\text{RST}}$ brought high at DFS="L". The value is in master mode. In slave mode it becomes one LRCK clock(1/fs) longer. When DFS="H", tRCF=17408 and tRTV=17920.

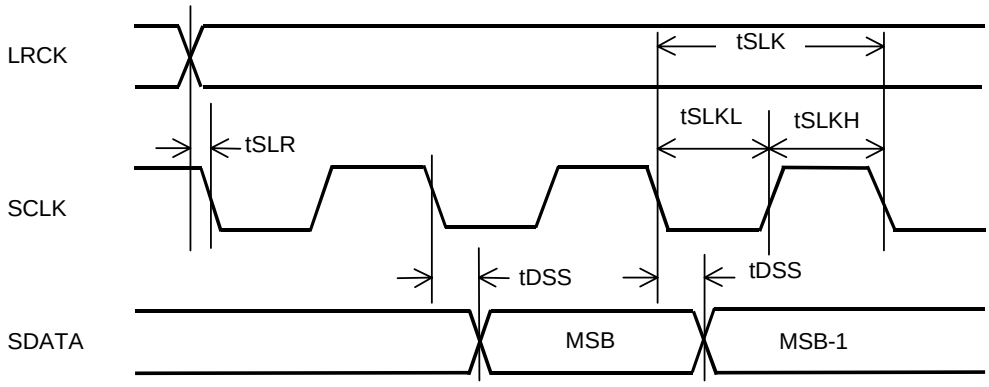
■ Timing Diagram



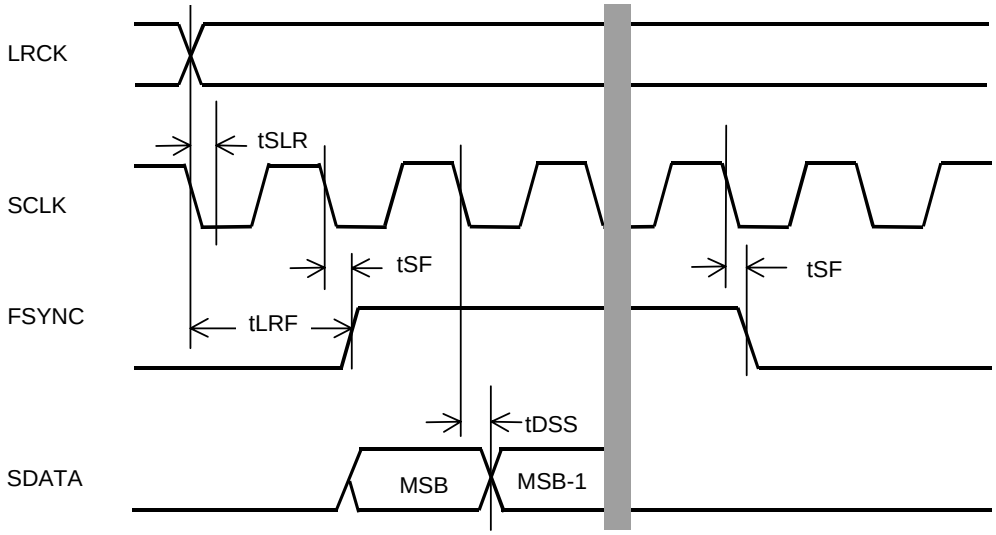
Serial Data Timing (Slave Mode, FSYNC="H")



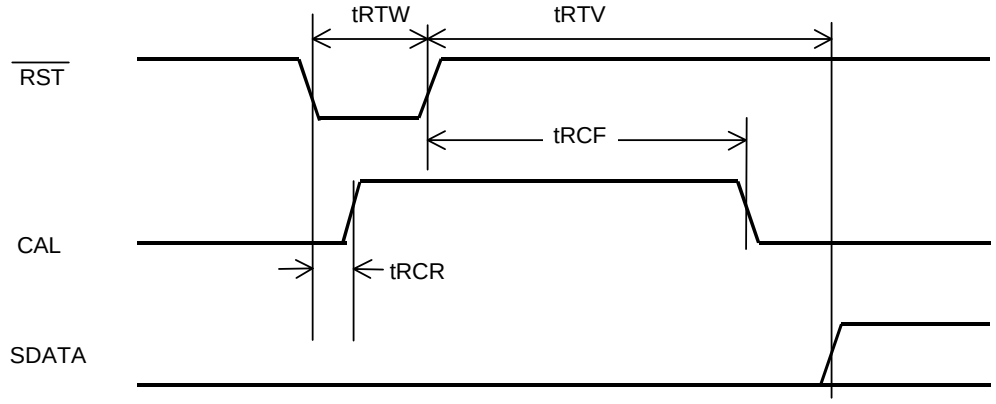
Serial Data Timing (Slave Mode)



Serial Data Timing (I^2S Slave Mode, FSYNC = Don't Care)



Serial Data Timing (Master Mode & I^2S Master Mode, DFS ="L")



Reset & Calibration Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK5393 are MCLK, LRCK(fs), SCLK. MCLK should be synchronized with LRCK but the phase is free of care. MCLK should be 256fs in normal sampling mode(DFS="L") and double sampling mode needs 128fs as MCLK. Table 2 illustrates standard audio word rates and corresponding frequencies used in the AK5393.

As the AK5393 includes the phase detect circuit for LRCK, the AK5393 is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is only needed for power-up.

All external clocks must be present unless $\overline{\text{RST}}$ ="L", otherwise excessive current may result from abnormal operation of internal dynamic logic.

Speed	Normal(DFS ="L")	Double(DFS ="H")
LRCK (max)	54kHz	108kHz
SCLK	~128fs	~64fs
MCLK	256fs	128fs

Table 1. System Clocks

fs	MCLK	SCLK
32.0kHz	8.1920MHz	4.0960MHz
44.1kHz	11.2896MHz	5.6448MHz
48.0kHz	12.2880MHz	6.1440MHz
96.0kHz	12.2880MHz	6.1440MHz

Table 2. Examples of System Clock Frequency

■ Serial Data Interface

The AK5393 supports four serial data formats which can be selected via SMODE1 and SMODE2 pins(Table 3). The data format is MSB-first, 2's complement.

Figure	SMODE2	SMODE1	Mode	LRCK
Figure 1	L	L	Slave Mode	Lch = H, Rch =L
Figure 2	L	H	Master Mode	Lch =H, Rch =L
Figure 3	H	L	I^2S Slave Mode	Lch =L, Rch =H
Figure 4	H	H	I^2S Master Mode	Lch =L, Rch =H

Table 3. Serial I/F Format

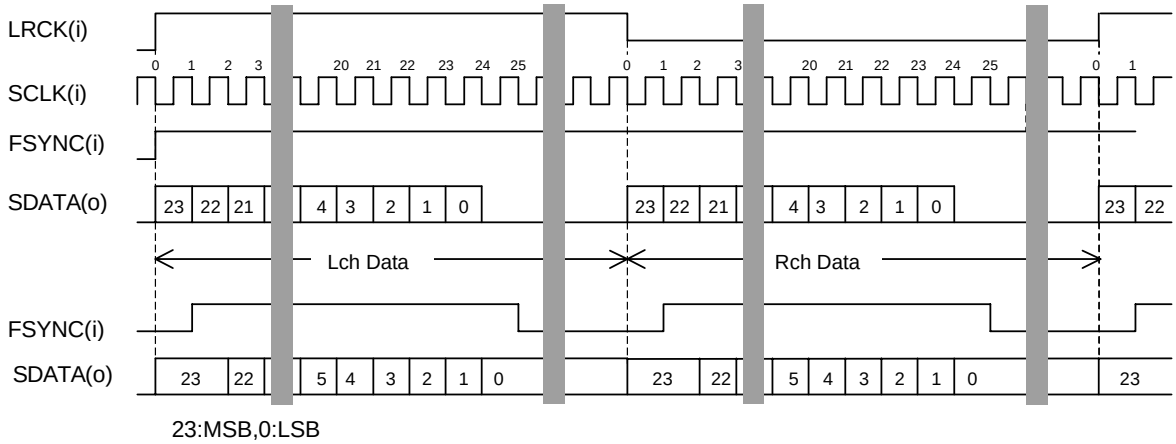


Figure 1. Serial Data Timing (Slave Mode)

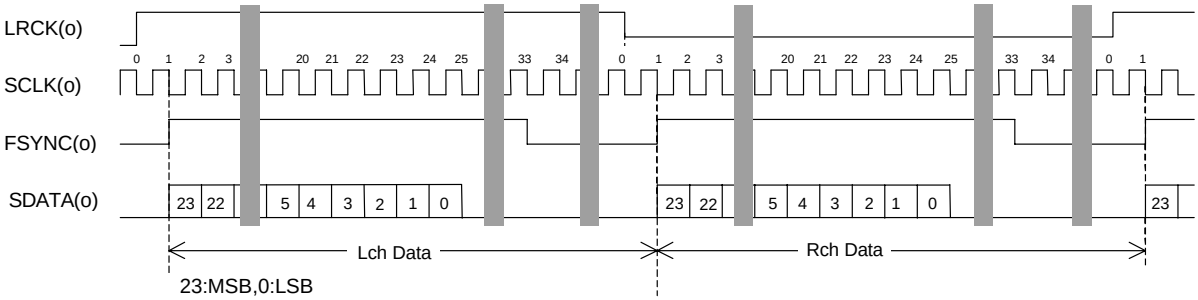


Figure 2. Serial Data Timing (Master mode, DFS="L")

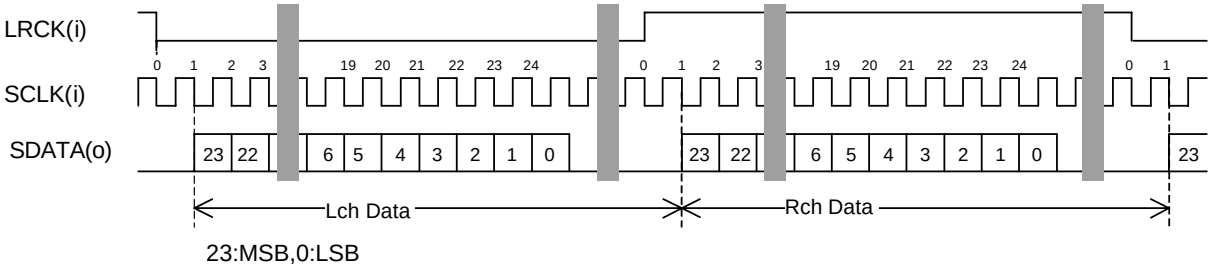


Figure 3. Serial Data Timing (I^2S Slave mode, FSYNC: Don't care.)

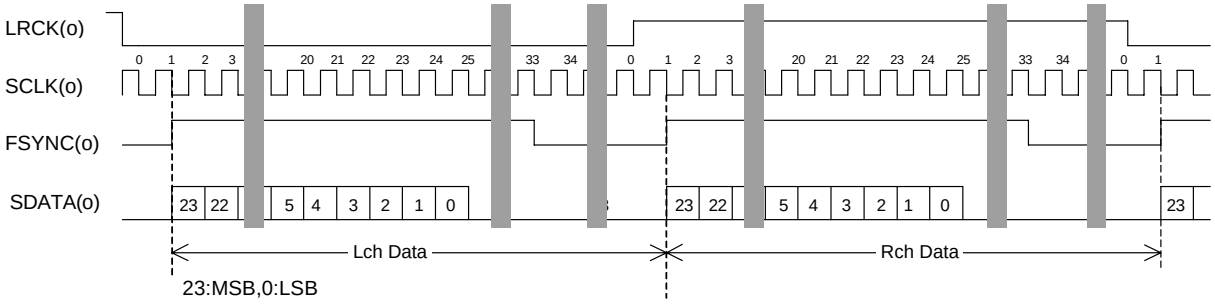


Figure 4. Serial Data Timing (I^2S Master mode, DFS="L")

■ Offset Calibration

When $\overline{\text{RST}}$ pin goes to "L", the digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up.

During the offset calibration cycle, the digital section of the part measures and stores the values of calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AIN+/-) or the VCOM pins depending on the state of the ZCAL pin. With ZCAL "H", the analog input pin voltages are measured, and with ZCAL "L", the VCOM pin voltages are measured. The CAL output is "H" during calibration.

■ Digital High Pass Filter

The AK5393 also has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 1Hz at fs=48kHz and also scales with sampling rate(fs).

SYSTEM DESIGN

Figure 5 and 6 show the system connection diagram. An evaluation board[AKD5393] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

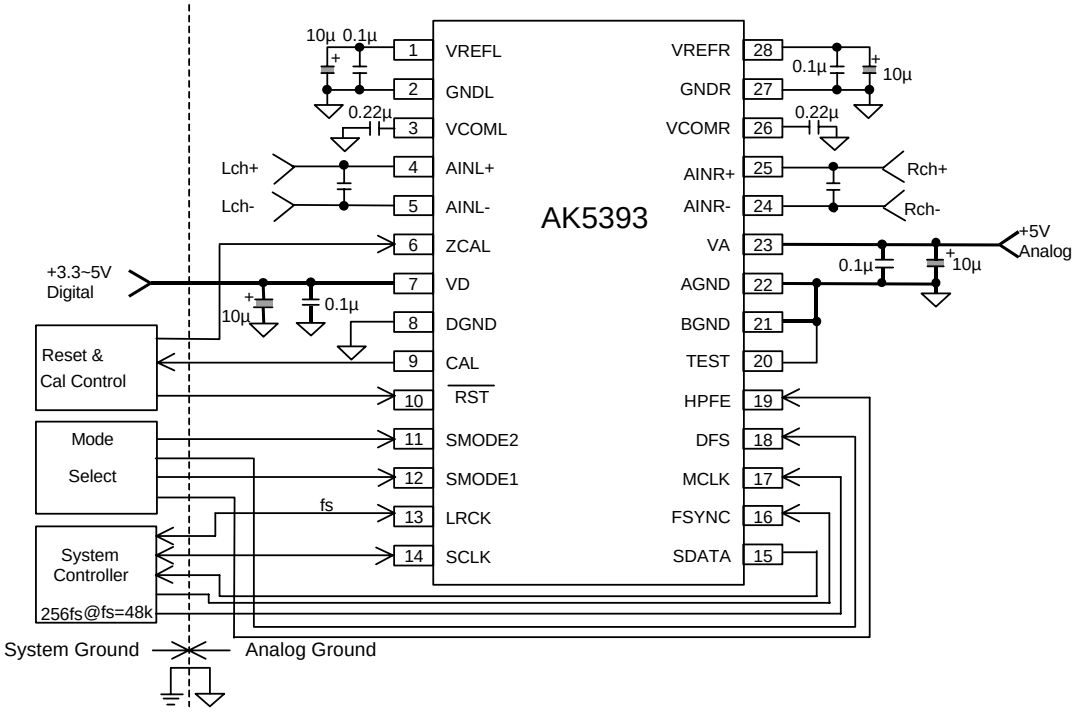


Figure 5. Typical Connection Diagram

Notes:
- LRCK = fs, SCLK=64fs.
- Power lines of VA and VD should be distributed separately from the point with low impedance of regulator etc.
- GND, BGND and DGND must be connected to the same analog ground plane.
- All input pins except pull-down/pull-up pins should not be left floating.

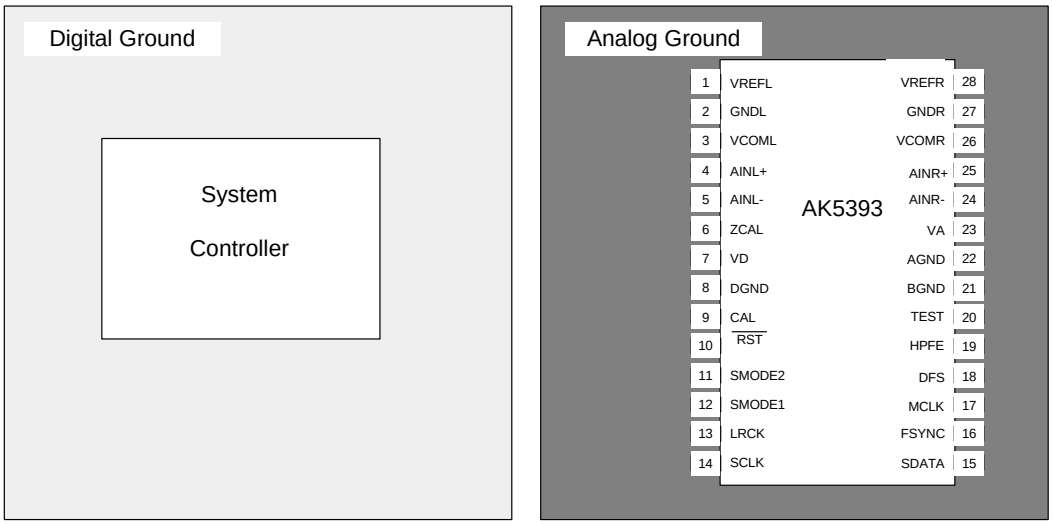


Figure 6 Ground layout

1. Grounding and Power Supply Decoupling

The AK5393 requires careful attention to power supply and grounding arrangements. Analog ground and digital ground should be separate and connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5393 as possible, with the small value ceramic capacitor being the nearest.

2. On-chip voltage reference and VCOM

The reference voltage for A/D converter is a differential voltage between the VREFL/R output voltage and the GNDL/R input voltage. The GNDL/R are connected to AGND and a 10µF electrolytic capacitor parallel with a 0.1µF ceramic capacitor between the VREFL/R and the GNDL/R eliminate the effects of high frequency noise. Especially a ceramic capacitor should be as near to the pins as possible. And all digital signals, especially clocks, should be kept away from the VREFL/R pins in order to avoid unwanted coupling into the AK5393. No load current may be taken from the VREFL/R pins.

VCOM is a common voltage of the analog signal. In order to eliminate the effects of high frequency noise, a 0.22µF ceramic capacitor should be connected as near to the VCOM pin as possible. And all signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5393. No load current may be drawn from the VCOM pin.

3. Analog Inputs

Analog signal is differentially input into the modulator via the AIN+ and the AIN- pins. The input voltage is the difference between AIN+ and AIN- pins. The full-scale of each pin is nominally ± 2.45Vpp(typ). The AK5393 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFFH(@24bit) for input above a positive full scale and 800000H(@24bit) for input below a negative full scale. The ideal code is 000000H (@24bit) with no input signal. The DC offset is removed by the offset calibration.

The AK5393 samples the analog inputs at 128fs(6.144MHz @fs=48kHz,DFS="L"). The digital filter rejects noise above the stop band except for multiples of 128fs. A simple RC filter may be used to attenuate any noise around 128fs and most audio signals do not have significant energy at 128fs.

The AK5393 accepts +5V supply voltage. Any voltage which exceeds the upper limit of VA+0.3V and lower limit of AGND-0.3V and any current beyond 10mA for the analog input pins(AIN+ /-) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution specially in case of using ±15V in other analog circuits.

Figure 7shows an input buffer circuit example 1. This is a full-differential input buffer circuit with an inverted-amp (gain :-10dB). The capacitor of 10nF between AIN+ /- decreases the clock feed through noise of modulator, and composes a 1st order LPF(fc=360kHz) with 22ohm resistor before the capacitor. This circuit also has a 1st order LPF(fc=370kHz) composed of op-amp. In this example, the internal offset is removed by self calibration. The evaluation board should be referred about the detail.

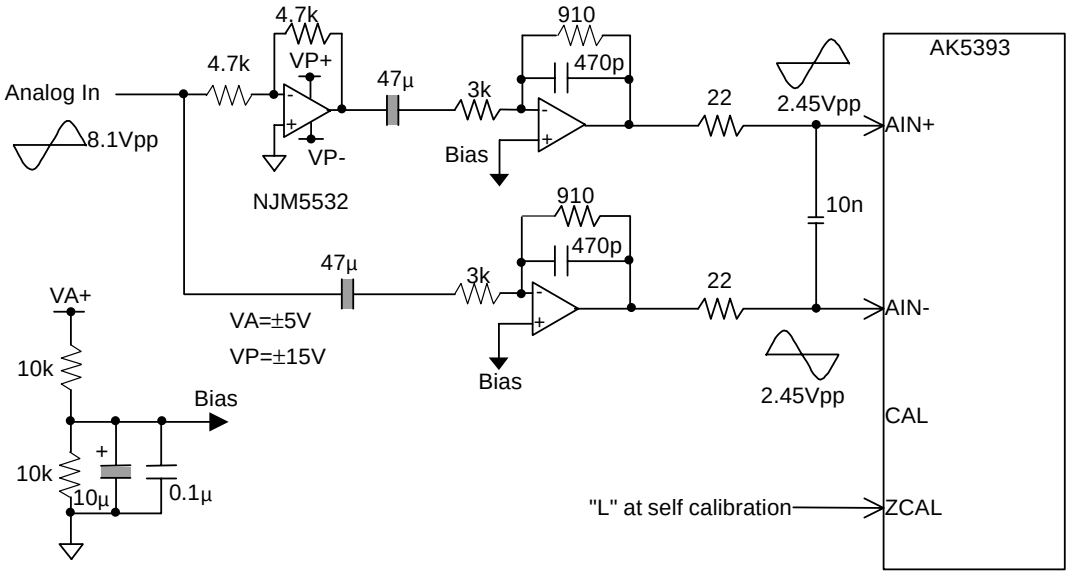


Figure 7 Differential Input Buffer Example 1

Figure 8 shows an input buffer circuit example 2. (1st order HPF; fc=0.66Hz, Table 4, 1st order LPF; fc=590kHz, gain=-14dB, Table 5). The analog signal is able to input through XLR or BNC connectors. (short JP1 and JP2 for BNC input, open JP1 and JP2 for XLR input). The input level of this circuit is +/-12.4Vpp (AK5393: +/-2.45Vpp Typ.).

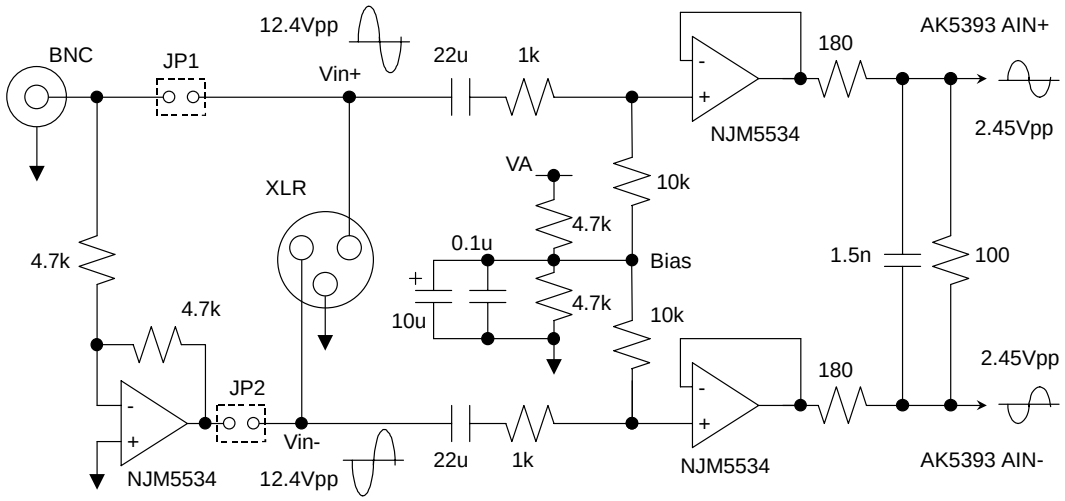


Figure 8 Differential Input Buffer Example 2

fin	1Hz	10Hz
Frequency Response	-1.56dB	-0.02dB

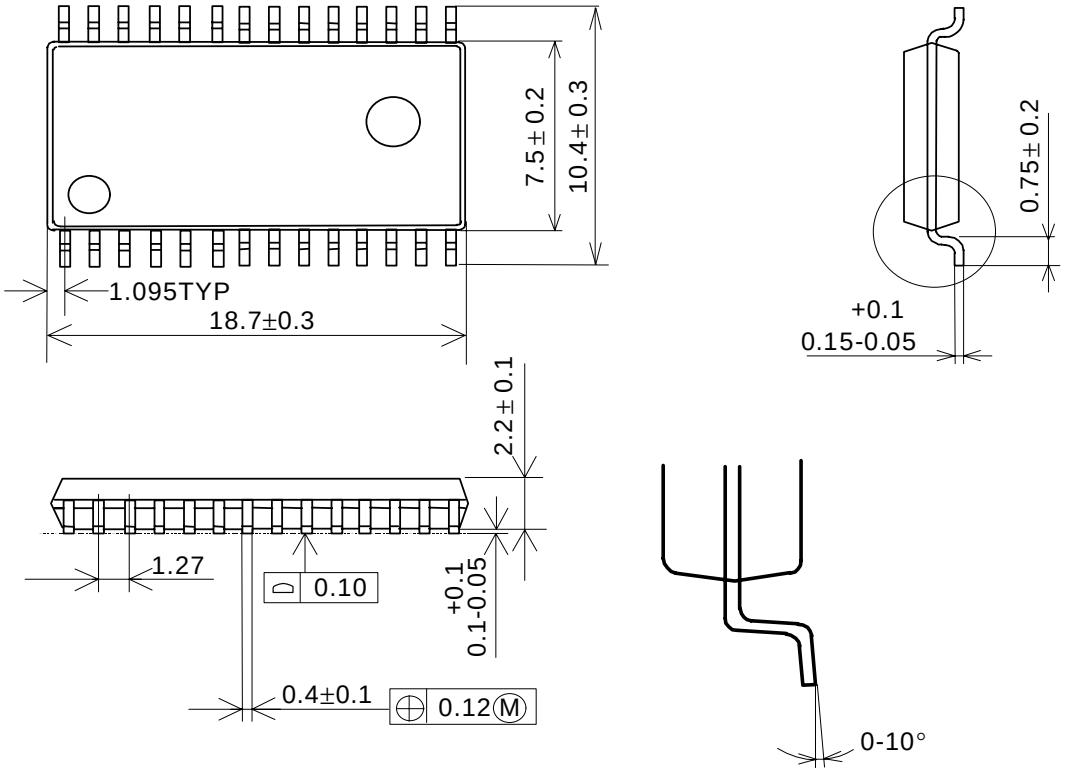
Table 4. Frequency Response of HPF

fin	20kHz	40kHz	6.144MHz
Frequency Response	-0.005dB	-0.02dB	-15.6dB

Table 5. Frequency Response of LPF

PACKAGE

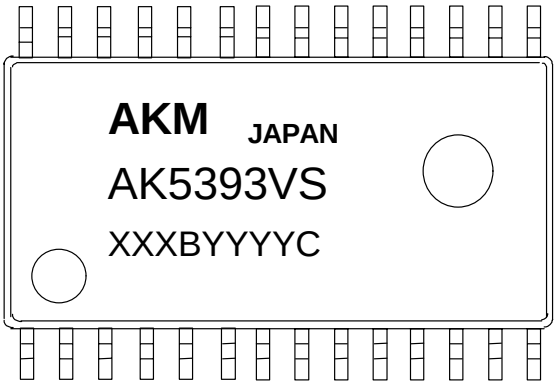
28pin SOP (Unit: mm)



■ **Package & Lead frame material**

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

MARKING



Contents of XXXBYYYYC

XXXB:	Lot # (X : numbers, B : alphabet)
YYYYC:	Data Code (Y : numbers, C : alphabet)

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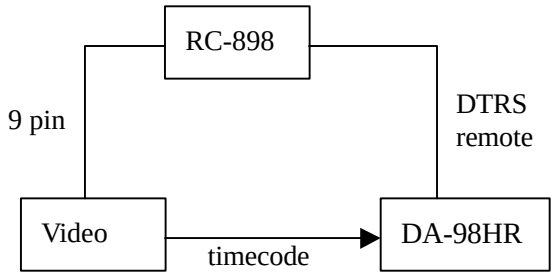
RC-898, Known problem

Configuration



Symptom

DA-98HR chases timecode coming from video machine.
Now perform REHAERSAL or AUTO IN/OUT.
After out point, all machines stop at post-roll point.
Sometimes chase mode on DA-98HR goes off falsely.

Both of V1.00 and V2.00 have same problem.

This problem has been solved by RC-898 beta V32.01 running under the reliability test.
V2.01(?) will be officially released January 2000.

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DSD1700

For most current data sheet and other product information, visit www.burr-brown.com

Direct Stream Digital™ (DSD™) SoundPLUS™ Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **DIRECT TRANSFER OF DSD DATA STREAM TO ANALOG OUTPUT SIGNAL**
- **DUAL DIFFERENTIAL ANALOG FIR FILTER**
- **DIRECT, CMOS LOGIC INTERFACE TO DSD™ DECODER IC**
  - **Data Clock: 2.8224 MHz (64 • 44.1kHz)**
  - **System Clock: 11.2896 MHz (256 • 44.1kHz)**
- **EXCELLENT DYNAMIC PERFORMANCE**
  - **THD+N: 0.001% (typ)**
  - **Dynamic Range: 110dB (typ)**
  - **SNR: 110dB (typ)**
  - **Frequency Response (–3dB): 100kHz**
- **SINGLE +5V SUPPLY OPERATION**
- **SMALL 28-LEAD SSOP PACKAGE**

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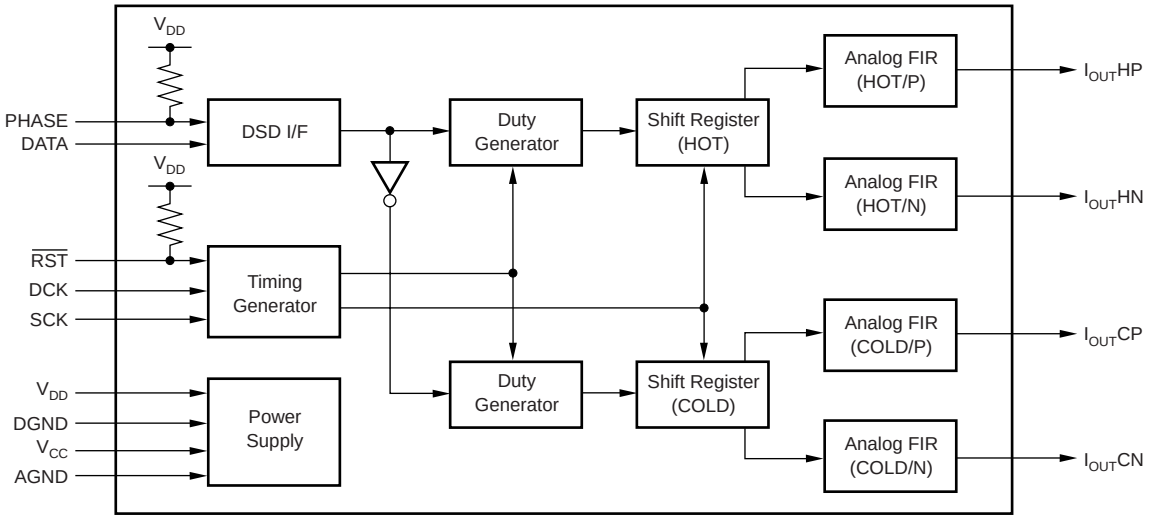
APPLICATIONS

- **SUPER AUDIO CD (SACD™) PLAYERS**
- **PROFESSIONAL DSD PROCESSORS**
- **PROFESSIONAL DSD CONSOLES**

DESCRIPTION

The DSD1700 is a unique digital-to-analog converter designed for DSD audio applications. The DSD1700 consists of a single-channel, 8-tap analog FIR filter constructed using a double differential circuit architecture, ensuring excellent dynamic performance and high power- supply noise rejection. The DSD1700 also includes the necessary logic required to interface directly to a DSD decoder IC.

The overall features and performance of the DSD1700 make it an ideal choice for high-performance Super Audio CD players and DSD studio applications.



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PDS-1555A
Printed in U.S.A. December, 1999
SBAS132

SPECIFICATIONS

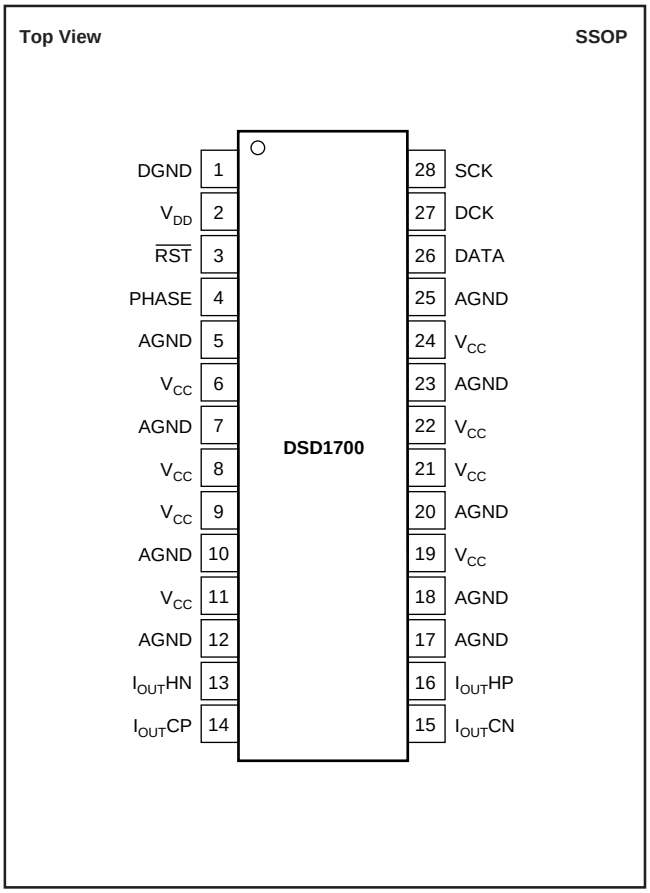
All specifications T_A = +25°C, V_{DD} = V_{CC} = 5.0V, f_S = 44.1kHz, data clock = 64f_S, system clock = 256f_S, unless otherwise specified. (Although the sampling frequency of Direct Stream Digital is 2.8224MHz, for convenience, in this specification sheet, it is described that the sampling frequency (f_S) is 44.1kHz and the 2.8224MHz clock is 64f_S).

PARAMETER		CONDITIONS	DSD1700E MIN	DSD1700E TYP	DSD1700E MAX	UNITS
INPUT CLOCK						
Data Clock Frequency (DCK)		64f_S		2.8224		MHz
System Clock Frequency (SCK)		256f_S		11.2896		MHz
SCK AC REQUIREMENT(1)						
Input Clock Duty Cycle				50		%
DIGITAL INPUT						
High Level Input Voltage	V_{IH}		0.7V_{DD}			V
Low Level Input Voltage	V_{IL}				0.3V_{DD}	V
High Level Input Current	I_{IH}				±10	µA
Low Level Input Current	I_{IL}(2)				±10	µA
	I_{IL}(3)				–120	µA
ANALOG OUTPUT(5)						
Full-Scale Voltage				4.1V_{CC}		Vp-p
Gain Error				±4	±10	% of FSR
Offset Error				±0.1	±1	% of FSR
Output Impedance(4)				2		kΩ
DYNAMIC PERFORMANCE(5)						
THD+N, V_{OUT} = 0dB		with 30kHz GIC Filter		0.001		%
Dynamic Range		with 30kHz GIC Filter		110		dB
Signal-to-Noise Ratio		with 30kHz GIC Filter		110		dB
Frequency Response, –3dB				100		kHz
POWER SUPPLY REQUIREMENTS						
Voltage Range		V_{CC}, V_{DD}	4.5	5	5.5	VDC
Supply Current	I_{CC}+I_{DD}	V_{CC} = V_{DD} = 5.0V		5.5	8.0	mA
Power Dissipation		V_{CC} = V_{DD} = 5.0V		27.5	40	mW
TEMPERATURE RANGE						
Operating			–25		+85	°C
Storage			–55		+125	°C
Thermal Resistance	θ_{JA}	28-Pin SSOP		100		°C/W

NOTES: (1) See description of system clock in the Functional Description section of this data sheet. (2) Pins 26, 27, 28: DATA. DCK. SCK. (3) Pins 3, 4: $\overline{RST}$, PHASE (with internal pull-up). (4) Pins 13, 14, 15, 16: I_{OUT}HN, I_{OUT}CP, I_{OUT}CN, I_{OUT}HP. (5) Measure DSD signal modulated f_{SIG} = 1kHz with 50% scaling factor through standard differential to single-ended converter (see Figure 10) using Audio Precision System II in rms mode with 20kHz LPF and 400Hz HPF.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	DGND	—	Digital Ground
2	V_{DD}	—	Digital Power Supply: +5V
3	$\overline{RST}$	IN	Reset Control Input, Active LOW(1)
4	PHASE	IN	Select data phase (LOW = Normal; HIGH = Invert)
5	AGND	—	Analog Ground
6	V_{CC}	—	Analog Power Supply: +5V
7	AGND	—	Analog Ground
8	V_{CC}	—	Analog Power Supply: +5V
9	V_{CC}	—	Analog Power Supply: +5V
10	AGND	—	Analog Ground
11	V_{CC}	—	Analog Power Supply: +5V
12	AGND	—	Analog Ground
13	I_{OUT}HN	OUT	Analog Output from DAC (Hot Negative)
14	I_{OUT}CP	OUT	Analog Output from DAC (Cold Positive)
15	I_{OUT}CN	OUT	Analog Output from DAC (Cold Negative)
16	I_{OUT}HP	OUT	Analog Output from DAC (Hot Positive)
17	AGND	—	Analog Ground
18	AGND	—	Analog Ground
19	V_{CC}	—	Analog Power Supply: +5V
20	AGND	—	Analog Ground
21	V_{CC}	—	Analog Power Supply: +5V
22	V_{CC}	—	Analog Power Supply: +5V
23	AGND	—	Analog Ground
24	V_{CC}	—	Analog Power Supply: +5V
25	AGND	—	Analog Ground
26	DATA	IN	Direct Stream Digital Data Input
27	DCK	IN	Data Clock Input
28	SCK	IN	System Clock Input

NOTE: (1) With internal pull-up resistor

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage(2)	+6.5V
Supply Voltage Differences(3)	±0.1V
Ground Voltage Differences(4)	±0.1V
Digital Input Voltage	–0.3V to V_{DD} +0.3V
Input Current (any pins except supplies)	±10mA
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, peak, 10s)	+235°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) V_{CC}, V_{DD}. (3) Among V_{CC}, V_{DD}. (4) Among AGND, DGND.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
DSD1700E	28-Lead SSOP	324	0°C to +70°C	DSD1700E	DSD1700E	Rails
"	"	"	"	"	DSD1700E/2K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of “DSD1700E/2K” will get a single 2000-piece Tape and Reel.

GENERAL INFORMATION

The DSD1700 is designed solely for use in DSD and SACD applications. It is not compatible with standard CD audio transports, or DVD/MPEG-2 decoders. Burr-Brown manufacturers a wide array of products for these applications. Please refer to our audio brochure and product data sheets, available from our web site (www.burr-brown.com) and local sales offices.

FUNCTIONAL DESCRIPTION

The concept of Direct Stream Digital (DSD) conversion is simple. An analog audio input is digitized by a 1-bit, 64x oversampled delta-sigma modulator. The 1-bit data stream is then stored and may be transferred to a SACD disc at a later time. For playback, the 1-bit, 64x oversampled data is then presented to the DSD1700 directly by a DSD decoder IC. The DSD1700 then low-pass filters the oversampled data to reconstruct the original analog audio waveform. The recording and playback functions are illustrated in Figures 1 and 2 respectively.

To perform the digital-to-analog conversion, the DSD1700 includes both the decoder interface logic and an analog FIR filter. The following paragraphs provide a summary of these functions.

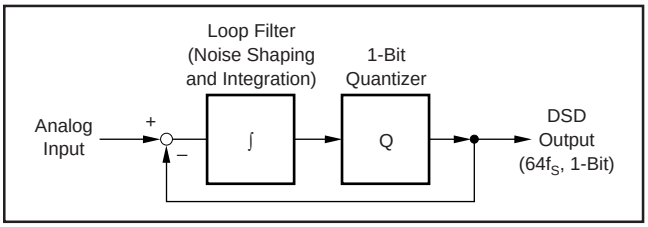


FIGURE 1. DSD Recording.

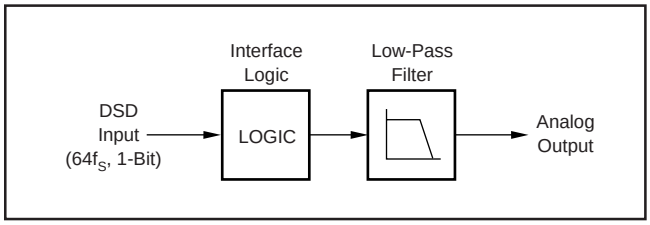
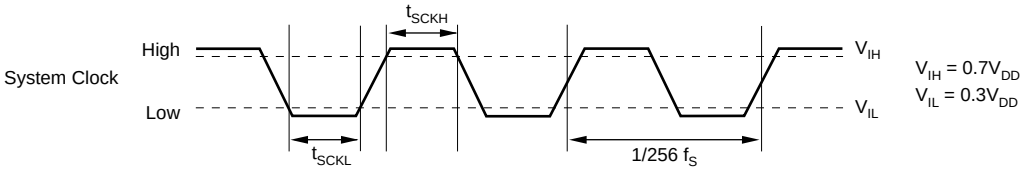


FIGURE 2. DSD Playback.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SCKH}	System Clock Pulse Width High	10			ns
t_{SCKL}	System Clock Pulse Width Low	10			ns

FIGURE 3. System Clock Timing.

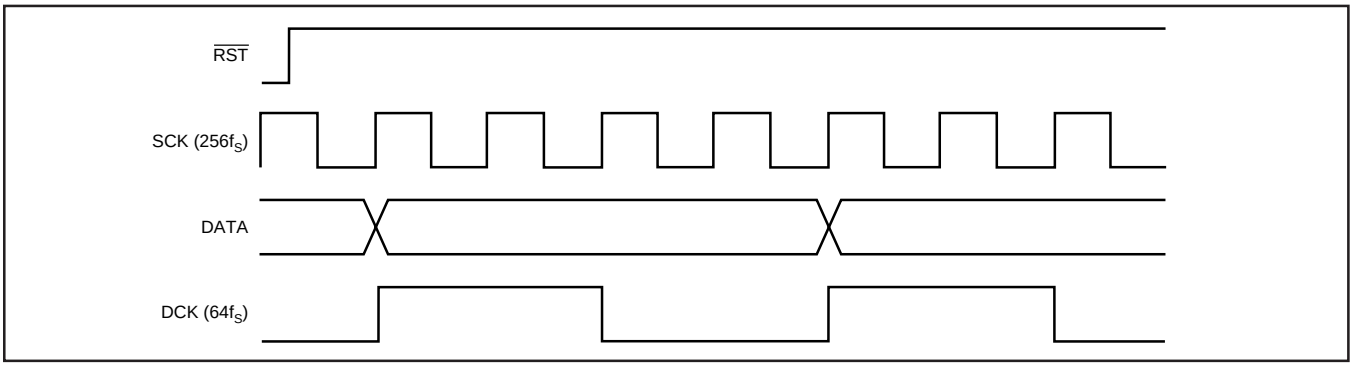


FIGURE 4. Input Signal Timing.

DECODER INTERFACE

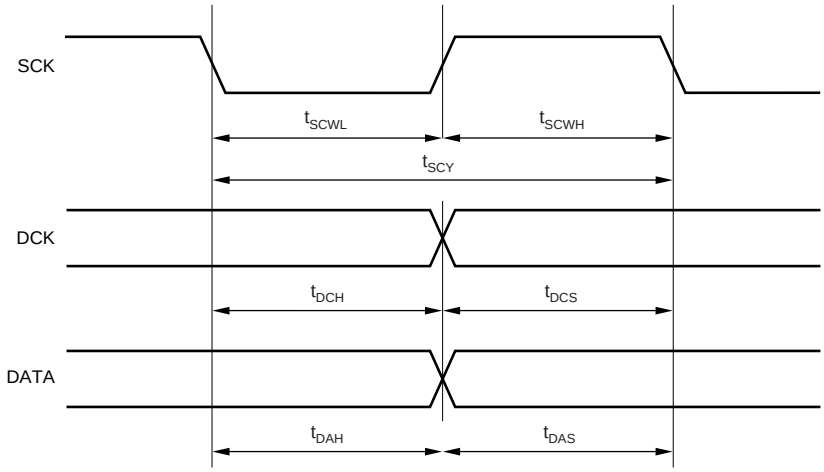
The decoder interface consists of several CMOS logic inputs. The system clock input, SCK (pin 28), operates at 11.2896MHz (256 • 44.1kHz). The data bit clock, DCK (pin 27), operates at 2.8244 MHz (64 • 44.1kHz) and is the 64x oversampled data clock. The 1-bit, 64x oversampled data stream is input at DATA (pin 26). DATA and DCK are synchronized to the SCK falling edge.

The DSD1700 generates HOT and COLD data internally for use with the double differential analog FIR filter. The PHASE input (pin 4) is used to determine the polarity of the HOT and COLD data (normal or inverted). The PHASE input is synchronized to the rising edge of SCK.

The $\overline{RST}$ input (pin 3) is used for system reset purposes. $\overline{RST}$ should be High for normal operation, and Low for reset operation. When $\overline{RST}$ is held Low, the current outputs of the analog FIR filter are set to the bipolar zero (BPZ) level. The $\overline{RST}$ signal is synchronized to the rising edge of SCK.

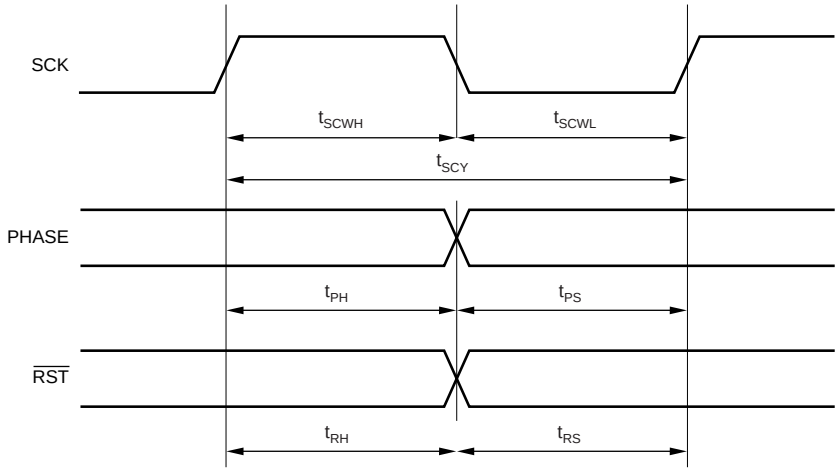
TIMING

Figures 3 though 6 show the timing diagrams for the DSD1700 interface signals. Figure 3 shows the system clock (SCK) timing requirements. Figure 4 shows the general timing for the data input. Figures 5 and 6 show the detailed timing for the DSD data and control data inputs.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SCWH}	SCK Pulse Width High	10			ns
t_{SCWL}	SCK Pulse Width Low	10			ns
t_{SCY}	SCK Pulse Cycle Time		$1/(256f_S)$		sec
t_{DCS}	DCK Setup Time	15			ns
t_{DCH}	DCK Hold Time	5			ns
t_{DAS}	DATA Setup Time	15			ns
t_{DAH}	DATA Hold Time	5			ns

FIGURE 5. DSD Data Input Timing.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SCWH}	SCK Pulse Width High	10			ns
t_{SCWL}	SCK Pulse Width Low	10			ns
t_{SCY}	SCK Pulse Cycle Time		$1/(256f_S)$		sec
t_{PS}	PHASE Setup Time	15			ns
t_{PH}	PHASE Hold Time	5			ns
t_{RS}	$\overline{RST}$ Setup Time	15			ns
t_{RH}	$\overline{RST}$ Hold Time	5			ns

FIGURE 6. Control Data Input Timing.

ANALOG FIR FILTER

The low-pass filter function for the DSD1700 is constructed by using four 8-tap, analog FIR filters with current outputs. The four filters include one each for HOT and COLD positive, and one each for HOT and COLD negative. This is referred to as a double differential architecture. These filters use resistors to set the filter coefficients, as shown in Figure 7. Prior to the analog FIR filters, the duty cycle of the DSD input signal is set to 75% by the DSD1700's duty generators.

Plots of the analog FIR filter response is shown in Figure 8. The stop-band attenuation of the filters dictates that additional low-pass filtering is required at the output of the external current-to-voltage converter circuit (see Figure 10).

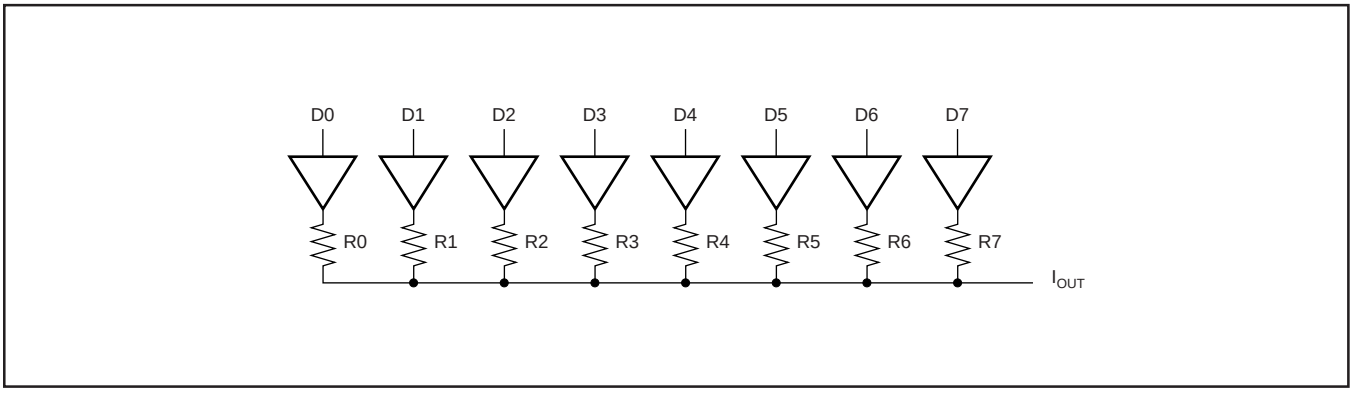


FIGURE 7. Analog FIR Filter Structure.

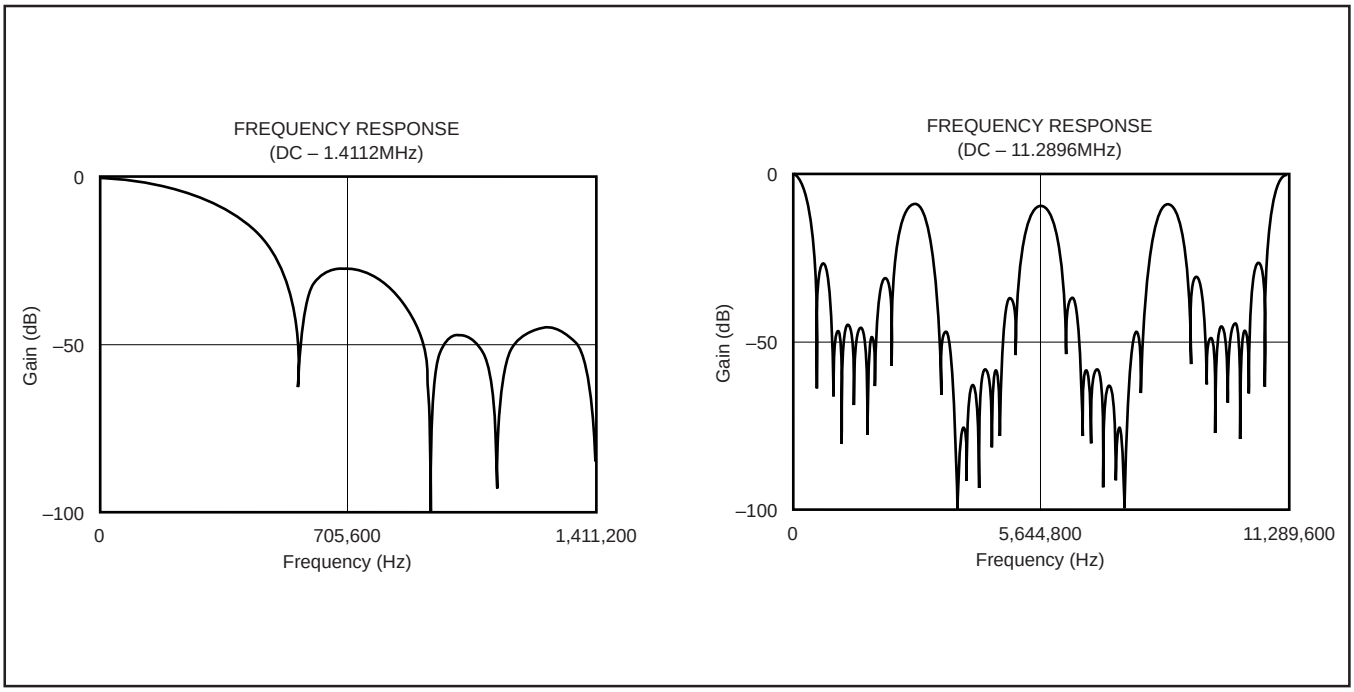


FIGURE 8. Analog FIR Filter Frequency Response.

APPLICATIONS INFORMATION

TYPICAL CONNECTIONS

Figure 9 shows the basic connection diagram for the DSD1700. A significant number of power supply bypass capacitors are required, and Burr-Brown recommends the indicated values for optimal performance.

CURRENT-TO-VOLTAGE (I/V) CONVERTER CIRCUIT

The DSD1700 is a current output device, and requires an I/V conversion circuit to transform the double-differential outputs into a usable voltage output. The circuit in Figure 10 is recommended for this purpose. Op amps are OPA134 or equivalent.

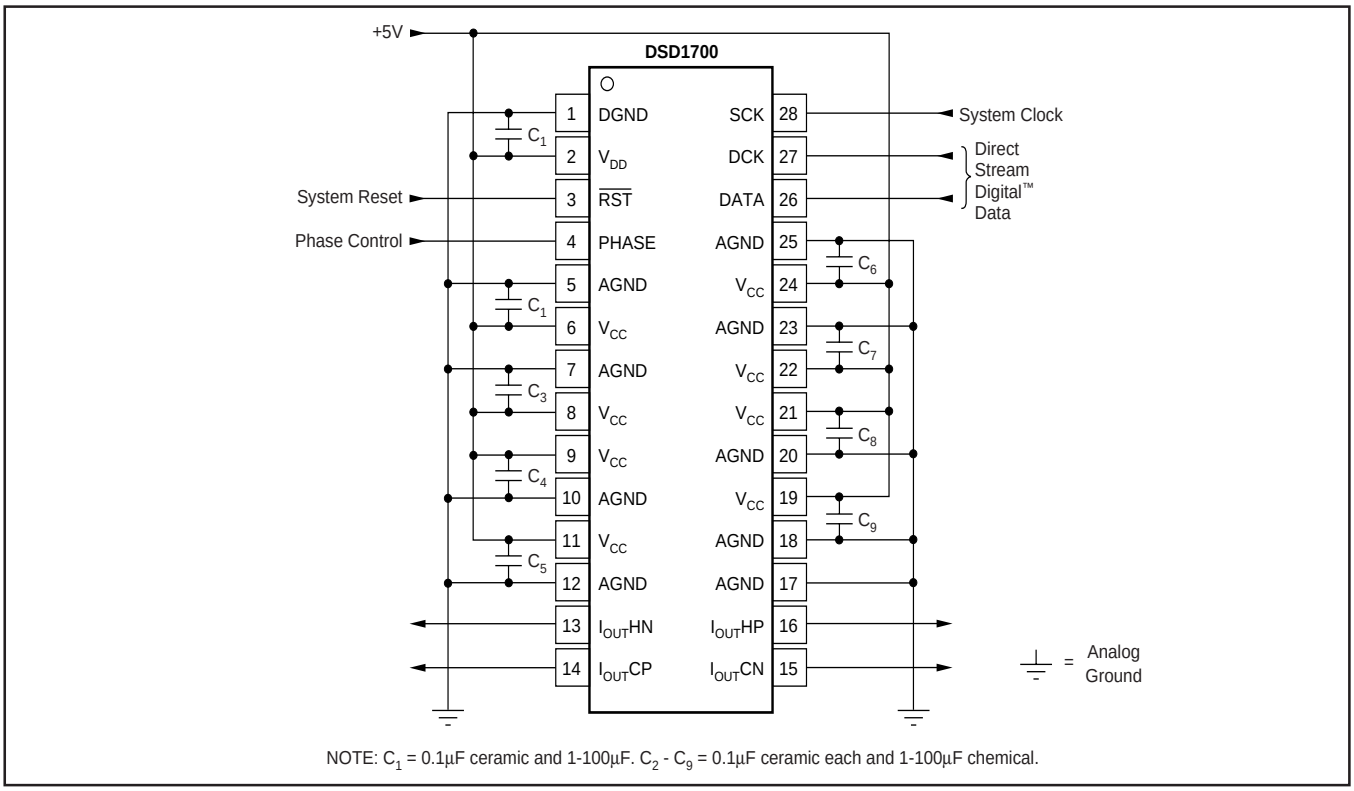


FIGURE 9. Basic Connection Diagram.

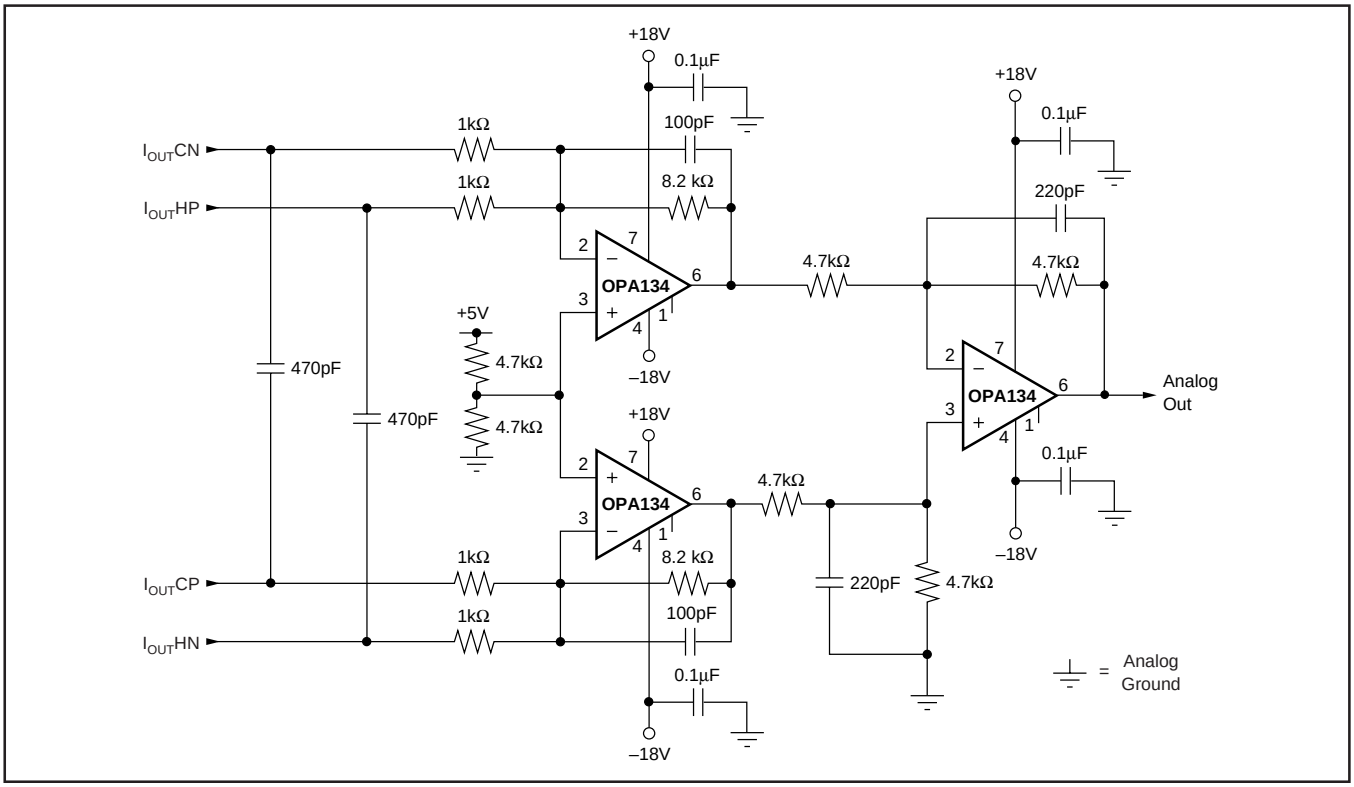


FIGURE 10. Recommended I/V Conversion Circuit.

PRINTED CIRCUIT BOARD LAYOUT

A typical PCB floor plan for the DSD1700 is shown in Figure 11. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split in the plane. The DSD1700 should be oriented with the digital I/O pins facing the ground plane split/cut, allowing for direct connection to the DSD decoder and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the DSD1700.

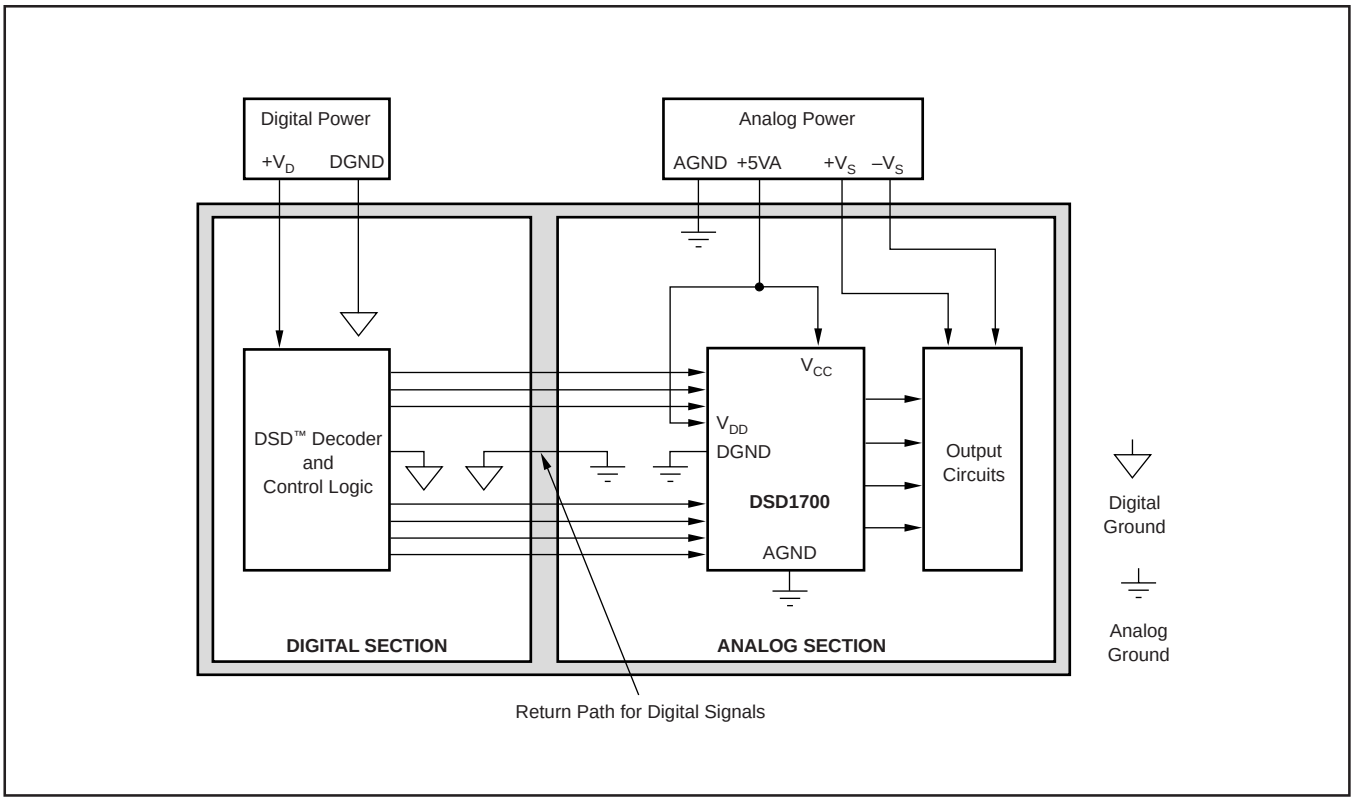


FIGURE 11. Recommended PCB Layout Technique.

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DA-98HR, Error Message List

No.	Message	Problem	Solution
1	WARNING ! Clock Error: no clock from AES/EBU input	No signal from clock source or different Fs. Item 5 relates to clock feeding from mater to slave through PW-88S cable. It is automatically selected in the following cases. * Machine ID is not "1" + "Time Mode"="ABS". Or, * "Time Mode"="TC" , "Clock Mode"="Auto" and clock source of master unit is not INT.	Check source unit, Fs setting,
2	WARNING ! Clock Error: no clock from I/O slot		
3	WARNING ! Clock Source: No Word Signal		
4	WARNING ! Clock Source: No Video Signal		
5	WARNING ! No clock from MASTER Check connections and settings		
6	WARNING ! Clock Source: Video frame mode doesn't match.	Incoming video clock (or pulse) does not macth the system frame. DA-98HR defines the frame rate of incoming signal as follows: When “Video Reference”=”Auto”, the unit automatically detect the frame rate of incoming signal. Or, frame rate can be defined by manual setting. Result of above and setting of “TC Frame Mode”: system timecode should match.	Check the frame rate of system timecode. In case incoming video clock affects “Auto” mode, try to set the frame rate manually.
7	WARNING ! Clock Source: Video PLL unlock	Incoming video clock is fluctuating or frequency is deviated so that digital audio clock cannot be generated. This message will appear if setting of “Video Reference” is wrong.	-
8	WARNING ! Clock Error: input slot PLL not locked	IF-AN98HR re-generates the clock by using own PLL. If the external clock source is unstable, PLL cannot lock to it.	Try “IO Board Clk Range”=”Wide”. Use more reliable clock source.
9	WARNING ! Clock Error: output slot PLL not locked		
10	WARNING ! AES/EBU cable not connected	When “digital” is selected at “Input Patch bay”, there is no digital input at that track.	-
11	WARNING ! TDIF(dubbing)cable not connected		

12	WARNING ! Fs unmatched	Fs of incoming signal does not match.	-
13	WARNING ! emphasis can't record digital data with emp.ON	DA-98HR cannot record the digital audio signal with the emphasis.	-
14	WARNING ! Cannot Record TC: No Timecode from Selected Source	No timecode to be recorded. Generator is not running when “TC Record Source”=”Generator”. External TC is not fed when “TC Record Source”=”External TC”. Unit cannot read the data from tape when “TC Record Source”=”TC Tape”, “TC Tape”=”TC Track”. Unit will overwrite the TC track even if this error occurred.	-
15	WARNING ! TC Record Source: Not Synchronized	Speed of the external incoming TC is not synchronizing to the digital audio clock of the DA-98HR.	Refer to Section 9, “Operations related to timecode” of the owner7s manual.
16	WARNING ! Cannot Chase: No Master ABS	There is no time information from the master.	-
17	WARNING ! Cannot Chase: No Master TC		
18	WARNING ! Cannot Chase: No Tape TC	Tape TC is not present. There is no TC recorded in the TC Track in case “Tape TC”=”TC Track”.	
19	WARNING ! Cannot Chase: Master frame mode doesn't match	Frame rate of the external TC does not match the system frame of the DA-98HR.	Choice the same frame rate at “TC Frame mode”.
20	WARNING ! Cannot Resolve No Video Signal	No video clock fed when the DA-98HR starts with “Video resolve”=”ON”.	-
21	WARNING ! Cannot Resolve: Video frame mode doesn't match	Frame rate of external video clock is different from the system frame of te DA-98HR.	-
22	WARNING ! Cannot Resolve: No Tape TC	Tape TC is not present. There is no TC recorded in the TC Track in case “Tape TC”=”TC Track”.	-
23	WARNING ! Broken tape: Replace the tape	Tape is cut.	-
24	WARNING ! Condensation on drum	Condensation on drum.	Leave the unit for 1-2 hours with powering on.
25	WARNING ! low battery	Voltage of the backup battery is getting lower.	-

26	WARNING ! Servo error [xx] Cycle the power		-
	xx=00	Main CPU cannot communicate with Servo CPU.	-
	xx=02	The drum motor could not work correctly in time.	-
	xx=04	The capstan motor could not work correctly in time.	-
	xx=08, 59, 68	The reel motor could not work correctly in time.	-
	xx=11	Unable to shift mechanism mode within the five seconds of command reception.	-
	xx=21	Tape is not wound into cassette half even Eject is commanded.	-
	xx=31	Occurrence of tape slack during tape runs.	-
	xx=41	Unable to latch solenoid on FF/REW winding.	-
27	WARNING ! DSP communication error	Main CPU cannot communicate with DSP.	-

BURR - BROWN®

PCM1702P
PCM1702U

BiCMOS Advanced Sign Magnitude 20-Bit DIGITAL-TO-ANALOG CONVERTER

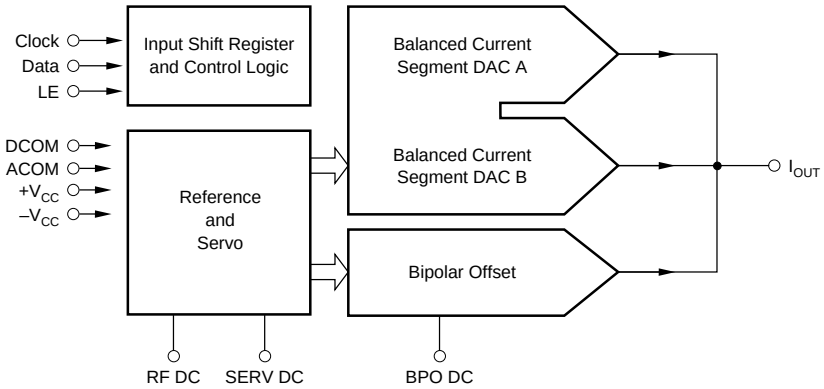
FEATURES

- **ULTRA LOW –96dB max THD+N (No External Adjustment Required)**
- **NEAR-IDEAL LOW LEVEL OPERATION**
- **GLITCH-FREE OUTPUT**
- **120dB SNR TYP (A-Weight Method)**
- **INDUSTRY STD SERIAL INPUT FORMAT**
- **FAST (200ns) CURRENT OUTPUT (±1.2mA)**
- **CAPABLE OF 16X OVERSAMPLING**
- **COMPLETE WITH REFERENCE**
- **LOW POWER (150mW typ)**

DESCRIPTION

The PCM1702 is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB typ with a full scale output). Incorporated into the PCM1702 is an advanced sign magnitude architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM1702 also features a very low noise (120dB typ SNR: A-weighted method) and fast settling current output (200ns typ, 1.2mA step) which is capable of 16X oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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Printed in U.S.A. June, 1995

SPECIFICATIONS

All specifications at 25°C, $\pm V_{CC}$ and $+V_{DD}$ = ±5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM1702P/U, -J, -K MIN	TYP	MAX	UNITS
RESOLUTION		20			Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale, with A-weight			110		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.4		$+V_{DD}$	V
V_{IL}		0		0.8	V
I_{IH}	$V_{IH} = +V_{DD}$			±10	µA
I_{IL}	V_{IL} = 0V			±10	µA
Data Format			Serial, MSB First, BTC(1)		
Input Clock Frequency			12.5	20.0	MHz
TOTAL HARMONIC DISTORTION + N(2)					
P/U V_O = 0dB	f_S = 352.8kHz(3), f = 1002Hz(4)		–92	–88	dB
V_O = –20dB	f_S = 352.8kHz(3), f = 1002Hz(4)		–82	–74	dB
V_O = –60dB	f_S = 352.8kHz(3), f = 1002Hz(4)		–46	–40	dB
P/U, -J V_O = 0dB	f_S = 352.8kHz(3), f = 1002Hz(4)		–96	–92	dB
V_O = –20dB	f_S = 352.8kHz(3), f = 1002Hz(4)		–83	–76	dB
V_O = –60dB	f_S = 352.8kHz(3), f = 1002Hz(4)		–48	–42	dB
P/U, -K V_O = 0dB	f_S = 352.8kHz(3), f = 1002Hz(4)		–100	–96	dB
V_O = –20dB	f_S = 352.8kHz(3), f = 1002Hz(4)		–84	–80	dB
V_O = –60dB	f_S = 352.8kHz(3), f = 1002Hz(4)		–50	–44	dB
ACCURACY					
Level Linearity	At –90dB Signal Level		±0.5		dB
Gain Error			±0.5	±3	%
Bipolar Zero Error(5)			±0.25		%
Gain Drift	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±5		ppm of FSR/°C
Warm-up Time			1		minute
IDLE CHANNEL SNR(6)	Bipolar Zero, A-weighted Filter	110	120		dB
ANALOG OUTPUT					
Output Range			±1.2		mA
Output Impedance			1.0		kΩ
Settling Time	(±0.003% of FSR, 1.2mA Step)		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
Supply Voltage Range: $+V_{CC} = +V_{DD}$		+4.75	+5.00	+5.25	V
$-V_{CC} = -V_{DD}$		–4.75	–5.00	–5.25	V
Combined Supply Current: $+I_{CC}$	$+V_{CC} = +V_{DD} = +5V$		+5.00	+9.0	mA
Combined Supply Current: $-I_{CC}$	$-V_{CC} = -V_{DD} = -5V$		–25.00	–41.0	mA
Power Dissipation	$\pm V_{CC} = \pm V_{DD} = \pm 5V$		150	250	mW
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+125	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (4) D/A converter output frequency (signal level). (5) Offset error at bipolar zero. (6) Measured using an OPA627 and 5kΩ feedback and an A-weighted filter.

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ABSOLUTE MAXIMUM RATINGS (DIP Package)

Power Supply Voltage	±6.5VDC
Input Logic Voltage	DGND—0.3V~+V_{DD}+0.3V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Power Dissipation	500mW
Lead Temperature (soldering, 10s)	260°C

ABSOLUTE MAXIMUM RATINGS (SOP Package)

Power Supply Voltage	±6.5VDC
Input Logic Voltage	DGND—0.3V~+V_{DD}+0.3V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Power Dissipation	300mW
Lead Temperature (soldering, 5s)	260°C

PIN ASSIGNMENTS (DIP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	9	+V_{CC}
2	CLOCK	10	BPO DC
3	+V_{DD}	11	I_{OUT}
4	DCOM	12	ACOM
5	–V_{DD}	13	ACOM
6	LE	14	SERV DC
7	NC	15	REF DC
8	NC	16	–V_{CC}

PIN ASSIGNMENTS (SOP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	11	+V_{CC}
2	CLOCK	12	BPO DC
3	NC	13	NC
4	+V_{DD}	14	I_{OUT}
5	DCOM	15	ACOM
6	–V_{DD}	16	ACOM
7	LE	17	SERV DC
8	NC	18	NC
9	NC	19	RFE DC
10	NC	20	–V_{CC}

PACKAGE INFORMATION[1]

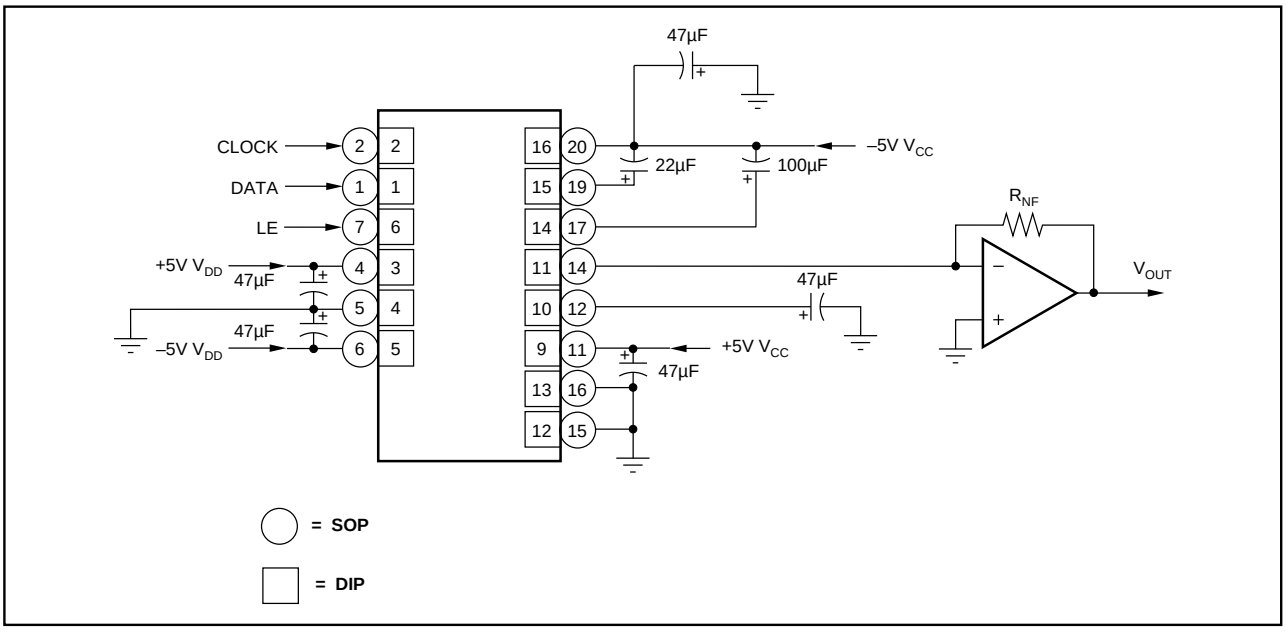
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1702P	16-Pin Plastic DIP	180
PCM1702U	20-Pin Plastic SOP	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

GRADE MARKING (SOP Package)

MODEL	PACKAGE
PCM1702U	Marked PCM1702.
PCM1702U-J	Marked with white dot by pin 10.
PCM1702U-K	Marked with red dot by pin 10.

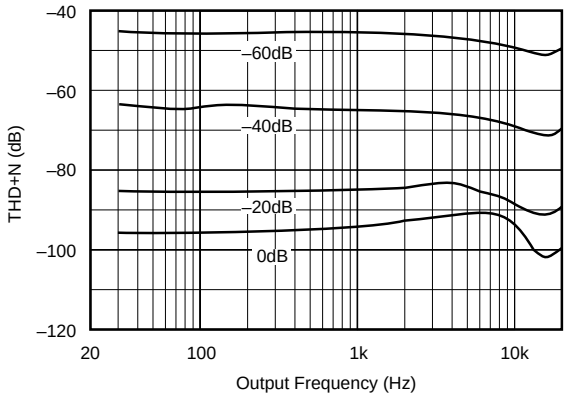
CONNECTION DIAGRAM



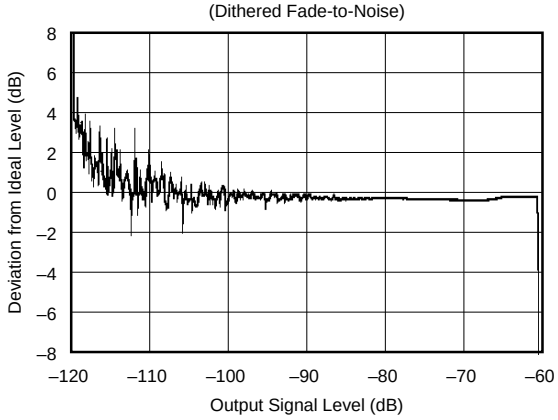
TYPICAL PERFORMANCE CURVES

All specifications at 25°C, $\pm V_A$ and $\pm V_D$ = ±5.0V unless otherwise noted.

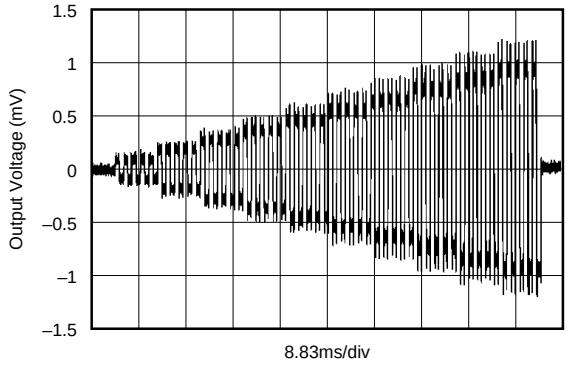
THD+N vs FREQUENCY



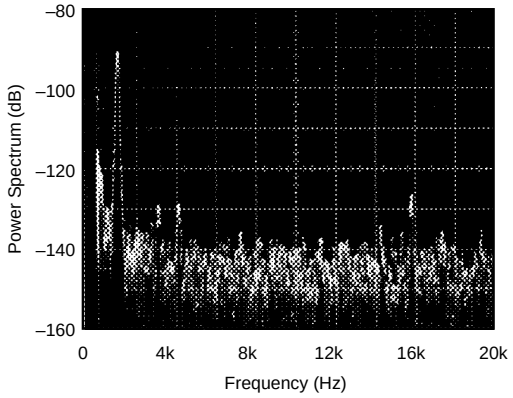
16-BIT LEVEL LINEARITY
(Dithered Fade-to-Noise)



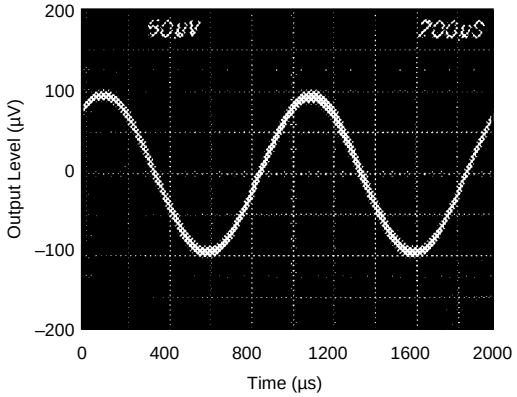
16-BIT MONOTONICITY



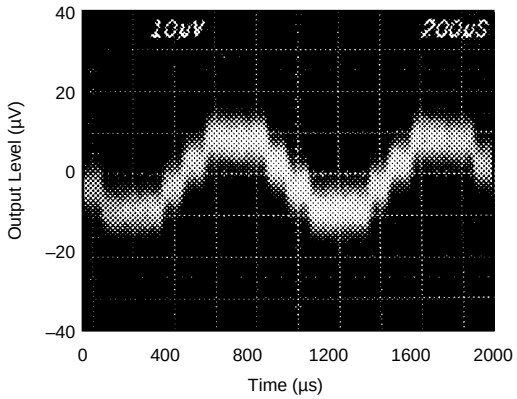
–90dB SIGNAL SPECTRUM
(100Hz Bandwidth)



–90dB SIGNAL
(10Hz to 20kHz Bandwidth)



–110dB SIGNAL
(10Hz to 20kHz Bandwidth)



THEORY OF OPERATION

ADVANCED SIGN MAGNITUDE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However, even the best of these suffer from potential low-level nonlinearity due to errors at the major carry bipolar zero transition. More recently, DACs employing a different architecture which utilizes noise shaping techniques and very high over-sampling frequencies, have been introduced ("Bitstream", "MASH", or 1-bit DAC). These DACs overcome the low level linearity problem, but only at the expense of signal-to-noise performance, and often to the detriment of channel separation and intermodulation distortion if the succeeding circuitry is not carefully designed.

The PCM1702 is a new solution to the problem. It combines all the advantages of a conventional DAC (excellent full scale performance, high signal-to-noise ratio and ease of use) with superior low-level performance. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference, and a common R-2R ladder for bit current sources by dual balanced current segments to ensure perfect tracking under all conditions. By interleaving the individual bits of each DAC and employing precise laser trimming of resistors, the highly accurate match required between DACs is achieved.

This new, complementary linear or advanced sign magnitude approach, which steps away from zero with small steps in both directions, avoids any glitching or "large" linearity errors and provides an absolute current output. The low level performance of the PCM1702 is such that real 20-bit resolution can be realized, especially around the critical bipolar zero point.

Table 1 shows the conversion made by the internal logic of the PCM1702 from binary two's complement (BTC). Also, the resulting internal codes to the upper and lower DACs (see front page block diagram) are listed. Notice that only the LSB portions of either internal DAC are changing around bipolar zero. This accounts for the superlative performance of the PCM1702 in this area of operation.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

The key specifications for the PCM1702 is total harmonic distortion plus noise (THD+N).

Digital data words are read into the PCM1702 at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 1002Hz is realized.

For production testing, the output of the DAC goes to an I to V converter, then through a 40kHz low pass filter, and then to a programmable gain amplifier to provide gain at lower signal output test levels before being fed into an analog-type distortion analyzer. Figure 1 shows a block diagram of the production THD+N test setup.

For the audio bandwidth, THD+N of the PCM1702 is essentially flat for all frequencies. The typical performance curve, "THD+N vs Frequency", shows four different output signal levels: 0dB, –20dB, –40dB, and –60dB. The test signals are derived from a special compact test disk (the CBS CD-1). It is interesting to note that the –20dB signal falls only about 10dB below the full scale signal instead of the expected 20dB. This is primarily due to the superior low level signal performance of the advanced sign magnitude architecture of the PCM1702.

In terms of signal measurement, THD+N is the ratio of $Distortion_{RMS} + Noise_{RMS} / Signal_{RMS}$ expressed in dB. For the PCM1702, THD+N is 100% tested at all three specified output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. All specifications are achieved without the use of external deglitchers.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD+N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The advanced sign magnitude architecture of the PCM1702, with its ideal performance around bipolar zero, provides a more usable dynamic range, even using the strict audio definition, than any previously available D/A converter.

ANALOG OUTPUT	INPUT CODE (20-bit Binary Two's Complement)	LOWER DAC CODE (19-bit Straight Binary)	UPPER DAC CODE (19-bit Straight Binary)
+Full Scale	011...111	111...111+1LSB(1)	111...111
+Full Scale –1LSB	011...110	111...111+1LSB(1)	111...110
Bipolar Zero +2LSB	000...010	111...111+1LSB(1)	000...010
Bipolar Zero +1LSB	000...001	111...111+1LSB(1)	000...001
Bipolar Zero	000...000	111...111+1LSB(1)	000...000
Bipolar Zero –1LSB	111...111	111...111	000...000
Bipolar Zero –2LSB	111...110	111...110	000...000
–Full Scale +LSB	100...001	000...001	000...000
–Full Scale	100...000	000...000	000...000

NOTE: (1) The extra weight of 1LSB is added at this point to make the transfer function symmetrical around bipolar zero.

TABLE I. Binary Two's Complement to Sign Magnitude Conversion Chart.

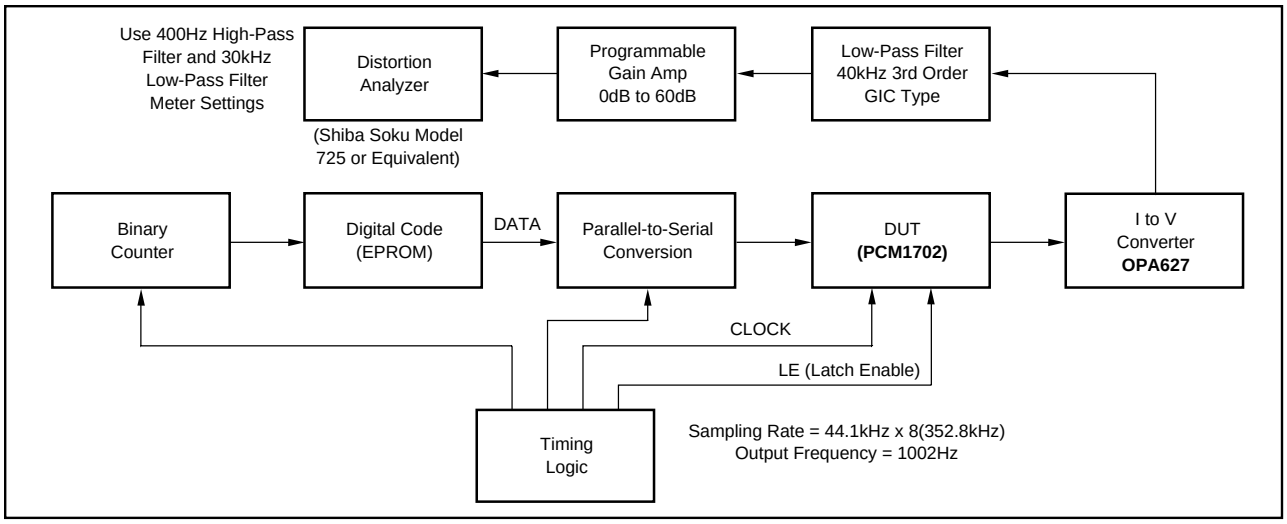


FIGURE 1. Production THD+N Test Setup.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. See the "–90dB Signal Spectrum" plot in the Typical Performance Curves section for the power spectrum of a PCM1702 at a –90dB output level. (The "–90dB Signal" plot shows the actual –90dB output of the DAC). The deviation from ideal for PCM1702 at this signal level is typically less than ±0.3dB. For the "–110dB Signal" plot in the Typical Performance Curves section, true 20-bit digital code is used to generate a –110dB output signal.

This type of performance is possible only with the low-noise, near-theoretical performance around bipolar zero of the PCM1702 advanced sign magnitude.

A commonly tested digital audio parameter is the amount of deviation from ideal of a 1kHz signal when its amplitude is decreased form –60dB to –120dB. A digitally dithered input signal is applied to reach effective output levels of –120dB using only the available 16-bit code from a special compact disk test input. See the "16-bit Level Linearity" plot in the Typical Performance Curves section for the results of a PCM1702 tested using this 16-bit dithered fade-to-noise signal. Note the very small deviation from ideal as the signal goes from –60dB to –100dB.

DC SPECIFICATION

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero, while the output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied. The idle channel SNR for the PCM1702 is typically greater than 120dB, making it ideal for low-noise applications.

Monotonicity

Because of the unique advanced sign magnitude architecture of the PCM1702, increasing values of digital input will always result in increasing values of DAC output as the signal moves away from bipolar zero in one-LSB steps (in either direction). The "16-bit Monotonicity" plot in the Typical Performance Curves section was generated using 16-bit digital code from a test compact disk. The test starts with 10 periods of bipolar zero. Next are 10 periods of alternating 1LSBs above and below zero, and then 10 periods of alternating 2LSBs above and below zero, and so on until 10LSBs above and below zero are reached. The signal pattern then begins again at bipolar zero.

With PCM1702, the low-noise steps are clearly defined and increase in near-perfect proportion. This performance is achieved without any external adjustments. By contrast, sigma-delta ("Bit-stream", "MASH", or 1-bit DAC) architectures are too noisy to even see the first 3 or 4 bits change (at 16 bits), other than by a change in the noise level.

Absolute Linearity

Even though absolute integral and differential linearity specs are not given for the PCM1702, the extremely low THD+N performance is typically indicative of 17-bit integral linearity in the DAC. The relationship between THD+N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

Offset, Gain, and Temperature Drift

Although the PCM1702 is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain and offset drift.

DIGITAL INPUT

Timing Considerations

The PCM1702 accepts TTL compatible logic input levels. The data format of the PCM1702 is binary two's complement (BTC) with the most significant bit (MSB) being first

in the serial input bit stream. Table II describes the exact relationship of input data to voltage output coding. Any number of bits can precede the 20 bits to be loaded, since only the last 20 will be transferred to the parallel DAC register after Latch Enable (Pin6 <PCM1702P>, Pin7 <PCM1702U>, LE) has gone low.

All DAC serial input data (Pin1, DATA) bit transfers are triggered on positive clock (Pin2, CLOCK), edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Latch Enable. The change in the output of the DAC occurs at a rising edge of the 4th clock of the CLOCK after the falling edge of Latch Enable. Refer to Figure 2 for graphical relationships of these signals.

Maximum Clock Rate

A typical clock rate of 16.9MHz for the PCM1702 is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16X over-sampling) the standard audio word bit length of 24 bits (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 20 bits are actually being used. The setup and hold timing relationships are shown in Figure 3.

"Stopped Clock" Operation

The PCM1702 is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 20 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until Latch Enable goes low. Latch Enable must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In any case, the setup and hold times for Data and LE must be observed as shown in Figure 3.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT
1,048,576LSBs	Full Scale Range	2.40000000mA
1LSB	NA	2.28882054nA
$7FFFF_{HEX}$	+Full Scale	–1.19999771mA
00000_{HEX}	Bipolar Zero –1LSB	0.00000000mA
80000_{HEX}	–Full Scale	+1.20000000mA

TABLE II. Digital Input/Output Relationships.

INSTALLATION

POWER SUPPLIES

Refer to CONNECTION DIAGRAM for proper connection of the PCM1702. The PCM1702 only requires a ±5V supply. Both positive supplies should be tied together at a single point. Similarly, both negative supplies should be connected together. No real advantage is gained by using separate analog and digital supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in CONNECTION DIAGRAM regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM1702 as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in CONNECTION DIAGRAM, various size decoupling capacitors can be used, with no special tolerances being required. The size of the offset decoupling capacitor is not critical either, with larger values (up to 100µF) giving slightly better SNR readings. All capacitors should be as close to the appropriate pins of the PCM1702 as possible to reduce noise pickup from surrounding circuitry.

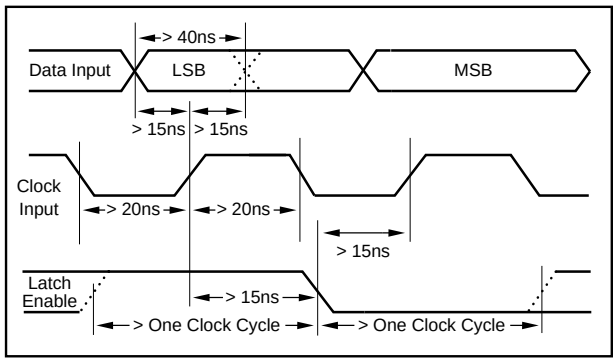
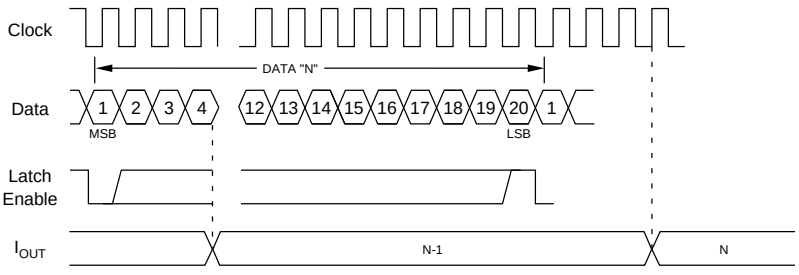


FIGURE 3. Setup and Hold Timing Diagram.



NOTES : (1) If clock is stopped between input of 20-bit data words, "Latch" Enable (LE) must remain low until after the first clock cycle of the next 20-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch Enable (LE) must remain low at least one clock cycle after going negative. (4) Latch Enable (LE) must be high for at least one clock cycle before going negative. (5) I_{OUT} changes on positive going edge of the 4th clock after negative going edge of Latch Enable (LE).

FIGURE 2. Timing Diagram.

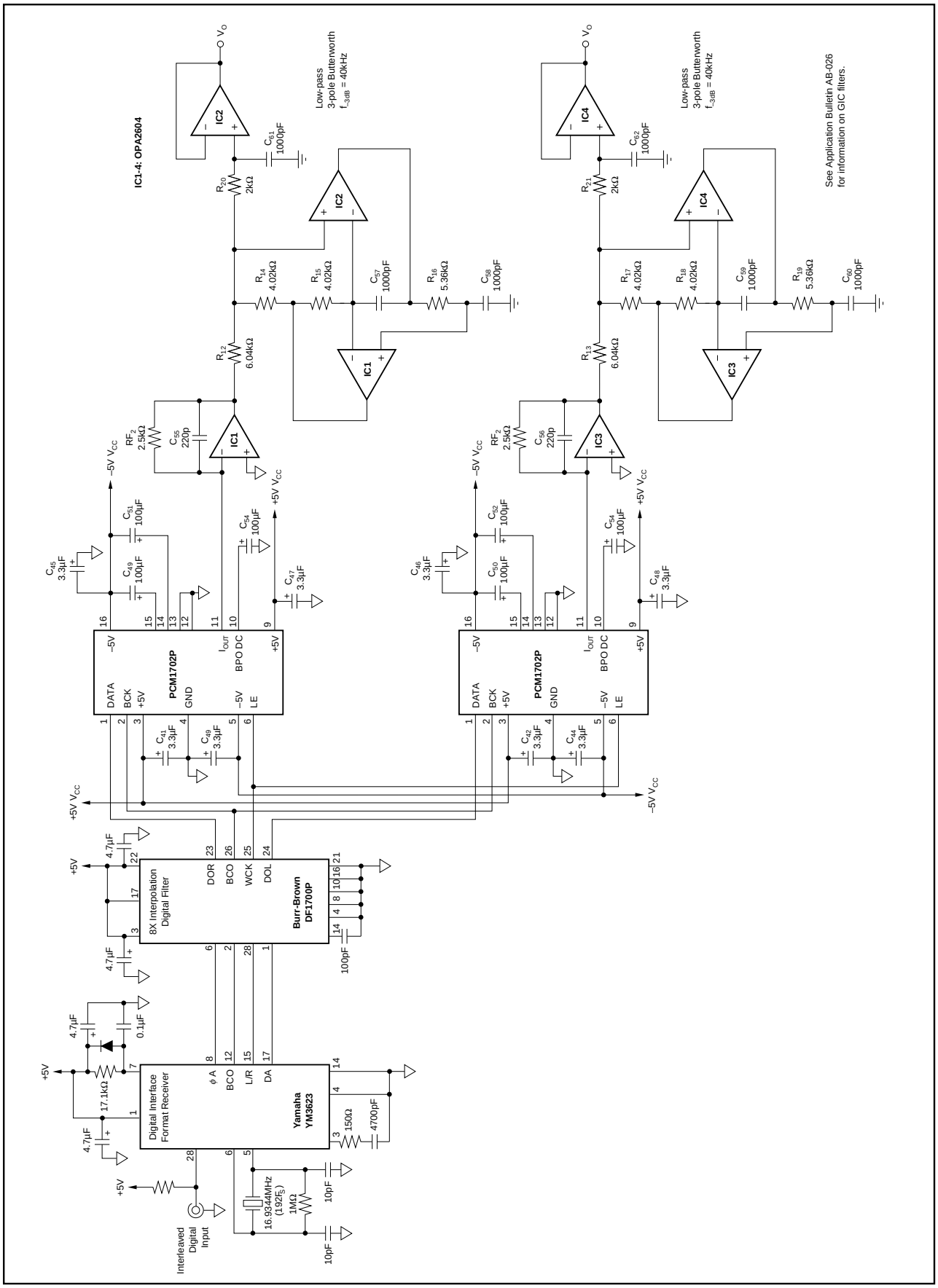


FIGURE 4. Typical Application for Stereo Audio 8X Oversampling system.

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FULL DIFFERENTIAL ANALOG INPUT 24-BIT, 192-kHz STEREO A/D CONVERTER

FEATURES

- **24-Bit Delta-Sigma Stereo A/D Converter**
- **High Performance:**
  - **Dynamic Range: 112 dB (Typical)**
  - **SNR: 111 dB (Typical)**
  - **THD+N: –102 dB (Typical)**
- **High-Performance Linear Phase Antialias Digital Filter:**
  - **Pass-Band Ripple: ±0.005 dB**
  - **Stop-Band Attenuation: –100 dB**
- **Fully Differential Analog Input: ±2.5 V**
- **Audio Interface: Master- or Slave-Mode Selectable**
- **Data Formats: Left-Justified, I^2S, Standard 24-Bit, and DSD**
- **Function:**
  - **Peak Detection**
  - **High-Pass Filter (HPF): –3 dB at 1 Hz, f_S = 48 kHz**
- **Sampling Rate up to 192 kHz**
- **System Clock: 128 f_S, 256 f_S, 384 f_S, 512 f_S, or 768 f_S**
- **Dual Power Supplies:**
  - **5 V for Analog**
  - **3.3 V for Digital**
- **Power Dissipation: 225 mW**
- **Small 28-Pin SSOP**
- **DSD Output: 1 Bit, 64 f_S**

APPLICATIONS

- **AV Amplifier**
- **MD Player**
- **Digital VTR**
- **Digital Mixer**
- **Digital Recorder**

DESCRIPTION

The PCM1804 is a high-performance, single-chip stereo A/D converter with fully differential analog voltage input. The PCM1804 uses a precision delta-sigma modulator and includes a linear phase antialias digital filter and high-pass filter (HPF) that removes dc offset from the input signal. The PCM1804 is suitable for a wide variety of mid- to high-grade consumer and professional applications, where excellent performance and 5-V analog supply and 3.3-V digital power-supply operation are required. The PCM1804 can achieve both PCM audio and DSD format due to the precision delta-sigma modulator. The PCM1804 is fabricated using an advanced CMOS process and is available in a small 28-pin SSOP package.

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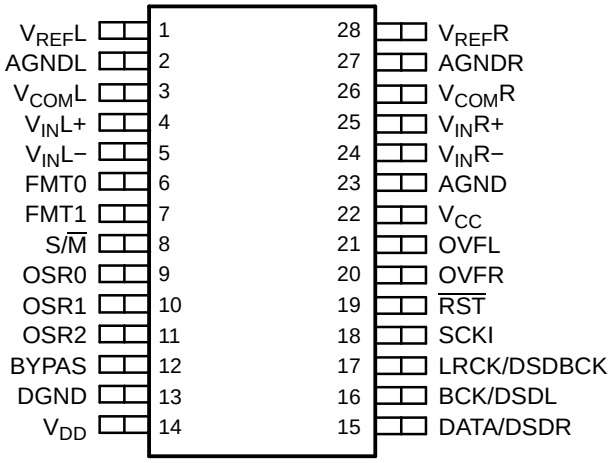
This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Electrostatic Discharge (ESD)* (SSYA008), available from Texas Instruments.

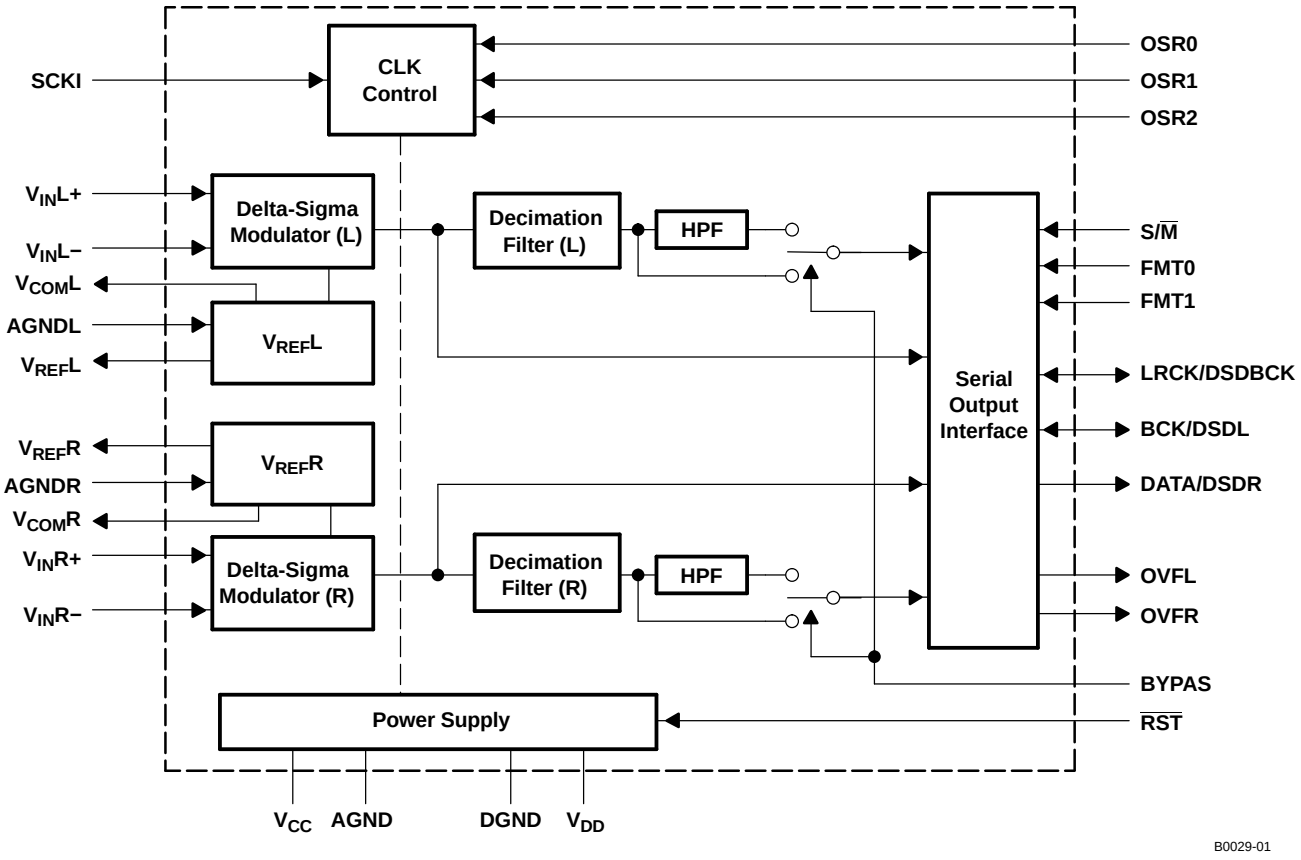
PIN ASSIGNMENTS

PCM1804 PACKAGE
(TOP VIEW)



P0007-02

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL PIN	I/O	DESCRIPTIONS
AGND	23	–	Analog ground
AGNDL	2	–	Analog ground for $V_{REF}L$
AGNDR	27	–	Analog ground for $V_{REF}R$
BCK/DSDL	16	I/O	Bit clock input/output in PCM mode. L-channel audio data output in DSD mode. (1)
BYPAS	12	I	HPF bypass control. High: HPF disabled, Low: HPF enabled (1)
DATA/DSDR	15	O	L-channel and R-channel audio data output in PCM mode. R-channel audio data output in DSD mode. (DSD output, when in DSD mode)
DGND	13	–	Digital ground
FMT0	6	I	Audio data format 0. See Table 5. (2)
FMT1	7	I	Audio data format 1. See Table 5. (2)
LRCK/DSDBCK	17	I/O	Sampling clock input/output in PCM and DSD modes. (1)
OSR0	9	I	Oversampling ratio 0. See Table 1 and Table 2. (2)
OSR1	10	I	Oversampling ratio 1. See Table 1 and Table 2. (2)
OSR2	11	I	Oversampling ratio 2. See Table 1 and Table 2. (2)
OVFL	21	O	Overflow signal of L-channel in PCM mode. This is available in PCM mode only.
OVFR	20	O	Overflow signal of R-channel in PCM mode. This is available in PCM mode only.
$\overline{RST}$	19	I	Reset, power-down input, active-low (2)
SCKI	18	I	System clock input; 128 f_S, 256 f_S, 384 f_S, 512 f_S, or 768 f_S. (3)
S/$\overline{M}$	8	I	Slave/master mode selection. See Table 4. (2)
V_{CC}	22	–	Analog power supply
$V_{COM}L$	3	–	L-channel analog common-mode voltage (2.5 V)
$V_{COM}R$	26	–	R-channel analog common-mode voltage (2.5 V)
V_{DD}	14	–	Digital power supply
$V_{IN}L–$	5	I	L-channel analog input, negative pin
$V_{IN}L+$	4	I	L-channel analog input, positive pin
$V_{IN}R–$	24	I	R-channel analog input, negative pin
$V_{IN}R+$	25	I	R-channel analog input, positive pin
$V_{REF}L$	1	–	L-channel voltage reference output, requires capacitors for decoupling to AGND
$V_{REF}R$	28	–	R-channel voltage reference output, requires capacitors for decoupling to AGND

(1) Schmitt-trigger input
(2) Schmitt-trigger input with internal pulldown (51 kΩ typically), 5-V tolerant.
(3) Schmitt-trigger input, 5-V tolerant.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	Supply voltage	V_{CC}	–0.3 V to 6.5 V
		V_{DD}	–0.3 V to 4 V
	Ground voltage differences	AGND, AGNDL, AGNDR, DGND	±0.1 V
	Supply voltage difference	V_{CC}, V_{DD}	$V_{CC} - V_{DD} < 3$ V
	Digital input voltage	FMT0, FMT1, S/$\overline{M}$, OSR0, OSR1, OSR2, SCKI, $\overline{RST}$	–0.3 V to 6.5 V
		BYPAS, DATA/DSDR, BCK/DSDL, LRCK/DSDBCK, OVFL, OVFR	–0.3 V to (V_{DD} + 0.3 V)
	Analog input voltage	$V_{REF}L$, $V_{REF}R$, $V_{COM}L$, $V_{COM}R$, $V_{IN}L+$, $V_{IN}R+$, $V_{IN}L–$, $V_{IN}R–$	–0.3 V to (V_{CC} + 0.3 V)
	Input current (any pins except supplies)		±10 mA
T_A	Ambient temperature under bias		–40°C to 125°C
T_{stg}	Storage temperature		–55°C to 150°C
T_J	Junction temperature		150°C
	Lead temperature (soldering)		260°C, 5 s
	Package temperature (IR reflow, peak)		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

		MIN	NOM	MAX	UNIT
Analog supply voltage, V_{CC}		4.75	5	5.25	V
Digital supply voltage, V_{DD}		3	3.3	3.6	V
Analog input voltage, full-scale (–0 dB), differential input			5		Vp-p
Digital input logic family			TTL compatible		
Digital input clock frequency	System clock	8.192		36.864	MHz
	Sampling clock	32		192	kHz
Digital output load capacitance				10	pF
Operating free-air temperature, T_A		–10		70	°C

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1804DB			UNIT
			MIN	TYP	MAX	
	Resolution			24		Bits
DATA FORMAT						
	Audio data interface format			Standard, I^2S, left-justified		
	Audio data bit length			24		Bits
	Audio data format			MSB first, 2s complement, DSD		
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	High-level input voltage	(1)(2)	2		5.5	Vdc
		(3)	2		V_{DD}	
V_{IL}	Low-level input voltage	(1)(2)(3)			0.8	Vdc
I_{IH}	High-level input current	$V_{IN} = V_{DD}$ (1)		65	100	µA
		$V_{IN} = V_{DD}$ (2)			±10	
		$V_{IN} = V_{DD}$ (3)			±100	
I_{IL}	Low-level input current	V_{IN} = 0 V (1)(2)			±10	µA
		V_{IN} = 0 V (3)			±50	
V_{OH}	High-level output voltage	I_{OH} = –1 mA (4)	2.4			Vdc
V_{OL}	Low-level output voltage	I_{OL} = 1 mA (4)			0.4	Vdc
CLOCK FREQUENCY						
f_S	Sampling frequency		32		192	kHz
	System clock frequency	256 f_S, single rate (5)		12.288		MHz
		384 f_S, single rate (5)		18.432		
		512 f_S, single rate (5)		24.576		
		768 f_S, single rate (5)		36.864		
		256 f_S, dual rate (6)		24.576		
		384 f_S, dual rate (6)		36.864		
		128 f_S, quad rate (7)		24.576		
		192 f_S, quad rate (7)		36.864		
DC ACCURACY						
	Gain mismatch, channel-to-channel				±3	% of FSR
	Gain error (V_{IN} = –0.5 dB)				±4	% of FSR
	Bipolar zero error	HPF bypass		±0.2		% of FSR

(1) Pins 6–11, 19: FMT0, FMT1, S/$\overline{M}$, OSR0, OSR1, OSR2, $\overline{RST}$ [Schmitt-trigger input with internal pulldown (51 kΩ typically), 5-V tolerant]
(2) Pin 18: SCKI (Schmitt-trigger input, 5-V tolerant)
(3) Pins 12, 16–17: BYPAS, BCK/DSDL, LRCK/DSDBCK (in slave mode, Schmitt-trigger input)
(4) Pins 15–17, 20, and 21: DATA/DSDR, BCK/DSDL, LRCK/DSDBCK (in master mode), OVFR, OVFL
(5) Single rate, f_S = 48 kHz
(6) Dual rate, f_S = 96 kHz
(7) Quad rate, f_S = 192 kHz

ELECTRICAL CHARACTERISTICS (continued)

all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS		PCM1804DB			UNIT
				MIN	TYP	MAX	
DYNAMIC PERFORMANCE (8)							
THD+N	Total harmonic distortion plus noise	V_{IN} = –0.5 dB	f_S = 48 kHz, system clock = 256 f_S		–102	–95	dB
		V_{IN} = –60 dB			–49		
		V_{IN} = –0.5 dB	f_S = 96 kHz, system clock = 256 f_S		–101		
		V_{IN} = –60 dB			–47		
		V_{IN} = –0.5 dB	f_S = 192 kHz, system clock = 128 f_S		–101		
		V_{IN} = –60 dB			–47		
		V_{IN} = –0.5 dB	DSD mode		–100		
	Dynamic range (A-weighted)	V_{IN} = –60 dB	f_S = 48 kHz, system clock = 256 f_S	106	112		dB
			f_S = 96 kHz, system clock = 256 f_S		112		
			f_S = 192 kHz, system clock = 128 f_S		112		
		DSD mode			112		
	SNR (A-weighted)	f_S = 48 kHz, system clock = 256 f_S		105	111		dB
		f_S = 96 kHz, system clock = 256 f_S			111		
		f_S = 192 kHz, system clock = 128 f_S			111		
		DSD mode			111		
	Channel separation	f_S = 48 kHz, system clock = 256 f_S		97	109		dB
		f_S = 96 kHz, system clock = 256 f_S			107		
		f_S = 192 kHz, system clock = 128 f_S			107		
ANALOG INPUT							
	Input voltage	Differential input			±2.5		V
	Center voltage				2.5		Vdc
	Input impedance	Single-ended			10		kΩ
DIGITAL FILTER PERFORMANCE							
	Pass-band edge	Single rate, dual rate				0.453 f_S	Hz
	Stop-band edge	Single rate, dual rate		0.547 f_S			Hz
	Pass-band ripple	Single rate, dual rate				±0.005	dB
	Stop-band attenuation	Single rate, dual rate		–100			dB
	Pass-band edge (–0.005 dB)	Quad rate				0.375 f_S	Hz
	Pass-band edge (–3 dB)	Quad rate				0.49 f_S	Hz
	Stop-band edge	Quad rate		0.77 f_S			Hz
	Pass-band ripple	Quad rate				±0.005	dB
	Stop-band attenuation	Quad rate		–135			dB
	Group delay				37/f_S		s
	HPF frequency response	–3 dB			f_S/48000		Hz

(8) f_{IN} = 1 kHz, using System Two™ audio measurement system by Audio Precision™ in RMS mode, with 20-kHz LPF and 400-Hz HPF in calculation for single rate, or with 40-kHz LPF in calculation for dual and quad rates.

ELECTRICAL CHARACTERISTICS (continued)

all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1804DB			UNIT
			MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS						
V_{CC}	Supply voltage range		4.75	5	5.25	Vdc
V_{DD}			3	3.3	3.6	
I_{CC}	Supply current	V_{CC} = 5 V (9)(10)(11)		35	45	mA
I_{DD}		V_{DD} = 3.3 V (9)(12)		15	20	
		V_{DD} = 3.3 V (10)(12)		27		
		V_{DD} = 3.3 V (11)(12)		18		
P_D	Power dissipation	Operation, V_{CC} = 5 V, V_{DD} = 3.3 V (9)(12)		225	290	mW
		Operation, V_{CC} = 5 V, V_{DD} = 3.3 V (10)(12)		265		
		Operation, V_{CC} = 5 V, V_{DD} = 3.3 V (11)(12)		235		
		Power down, V_{CC} = 5 V, V_{DD} = 3.3 V		5		
TEMPERATURE RANGE						
	Operation temperature		–10		70	°C
θ_{JA}	Thermal resistance			100		°C/W

(9) Single rate, f_S = 48 kHz
(10) Dual rate, f_S = 96 kHz
(11) Quad rate, f_S = 192 kHz
(12) Minimum load on DATA/DSDR (pin 15)

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data, unless otherwise noted.

SINGLE RATE

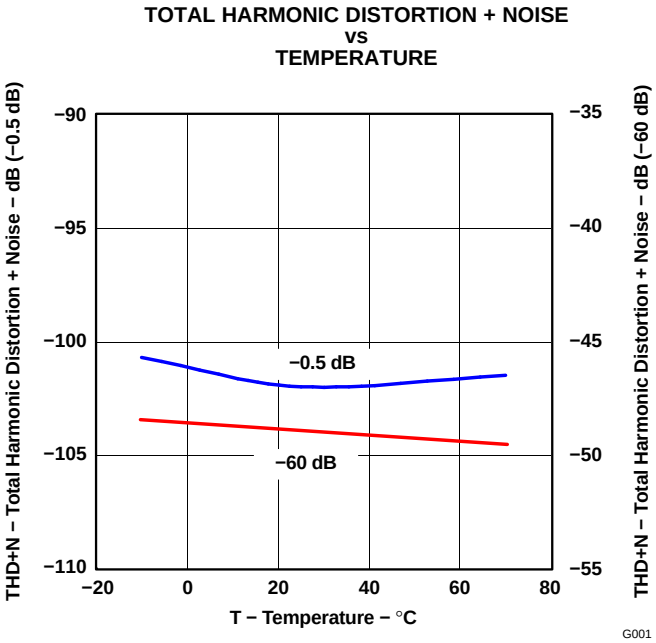


Figure 1.

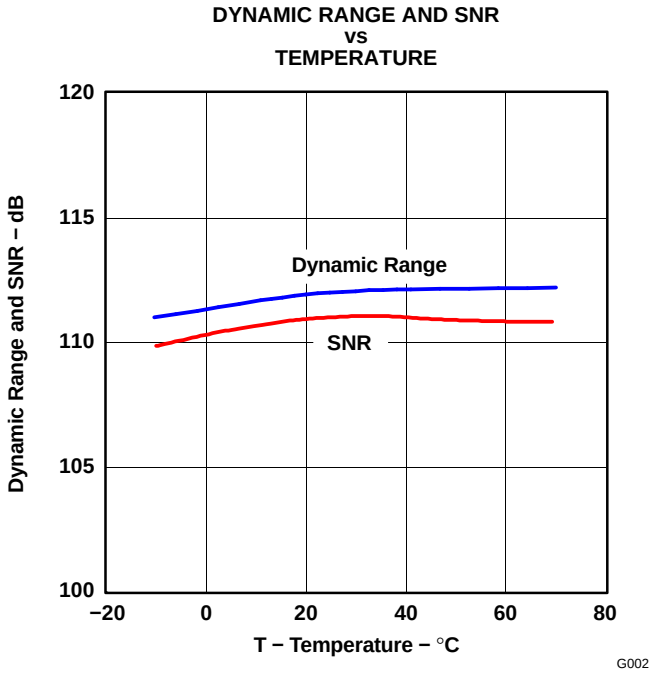


Figure 2.

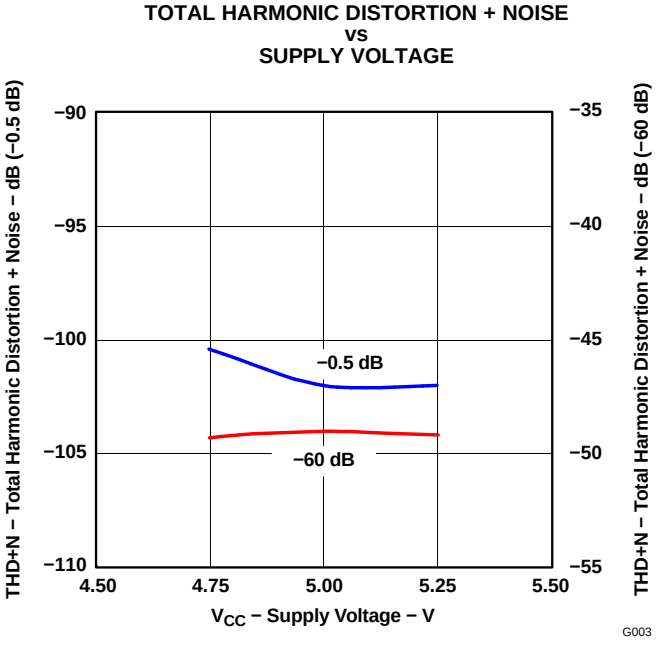


Figure 3.

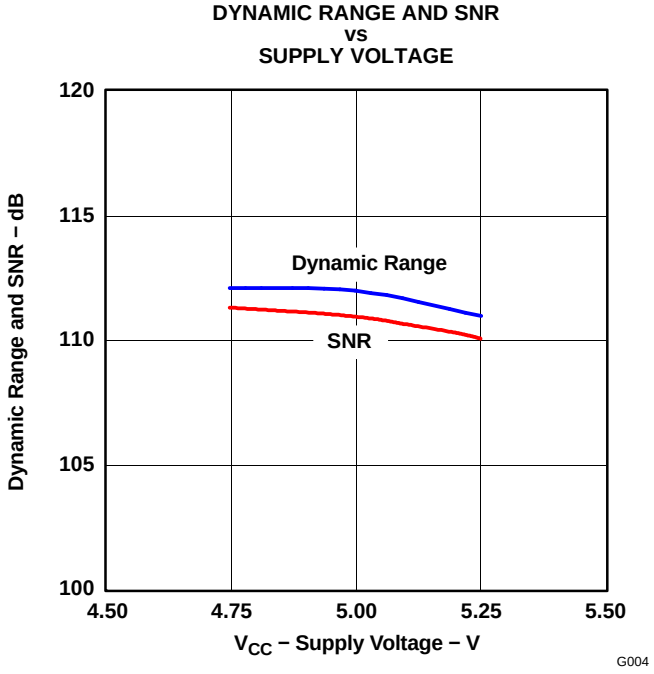


Figure 4.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data, unless otherwise noted.

SINGLE RATE (Continued)

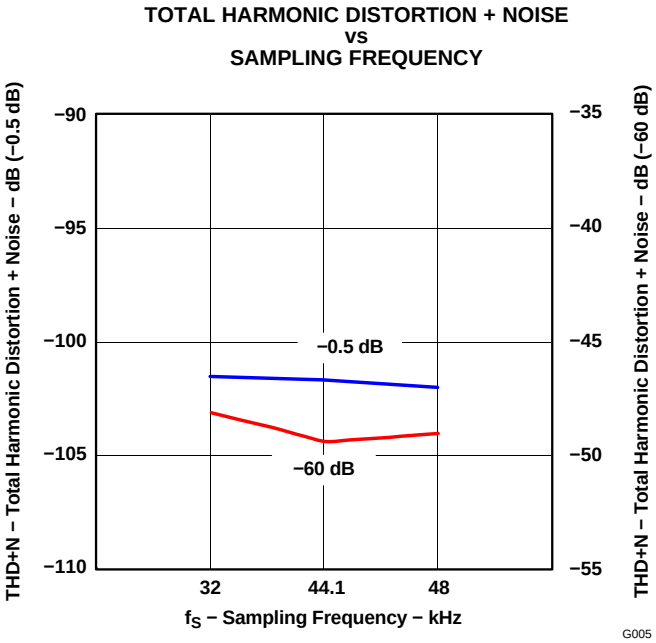


Figure 5.

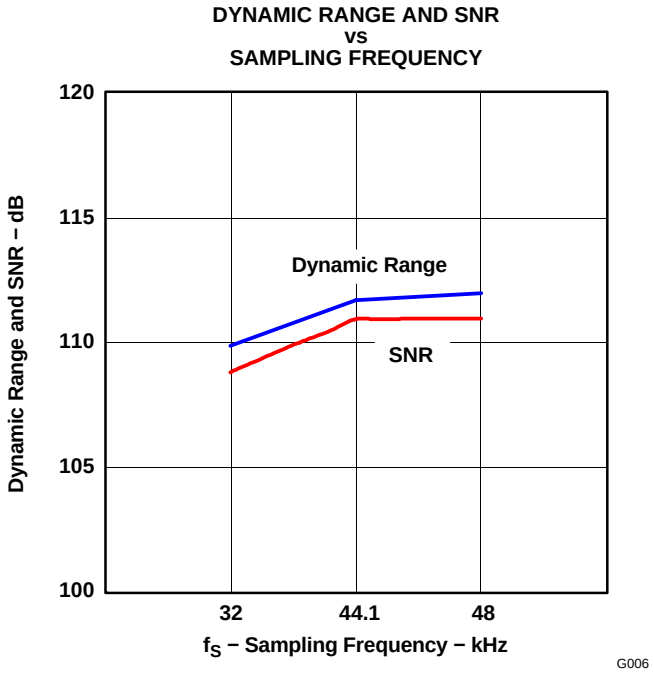


Figure 6.

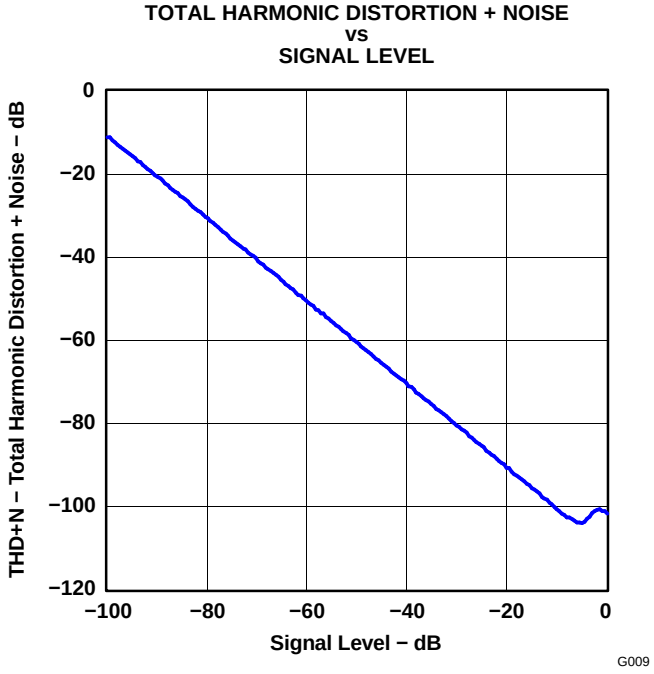


Figure 7.

TYPICAL PERFORMANCE CURVES (continued)

SINGLE RATE (Continued)

All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data, unless otherwise noted.

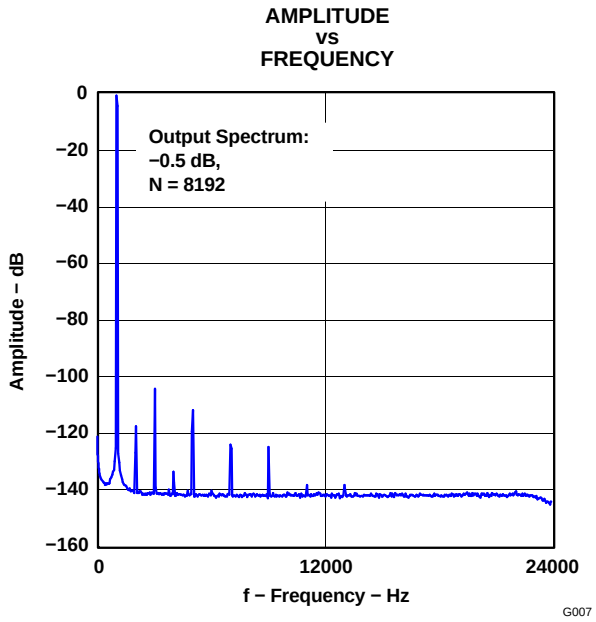


Figure 8.

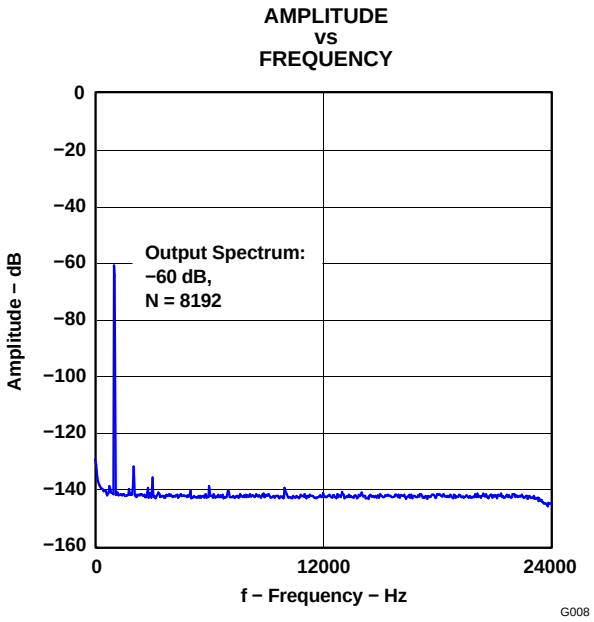


Figure 9.

DUAL RATE

All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, and 24-bit data, unless otherwise noted.

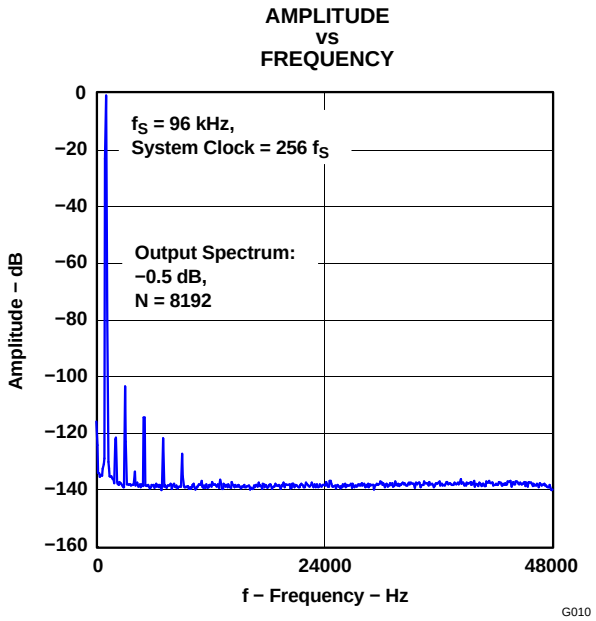


Figure 10.

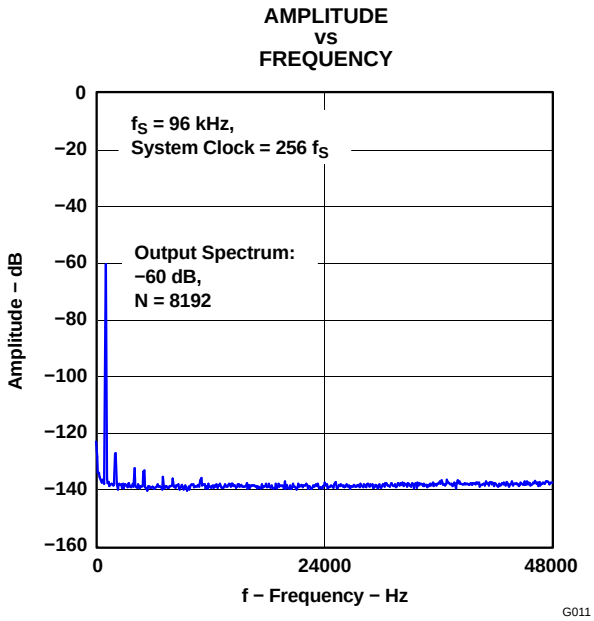


Figure 11.

TYPICAL PERFORMANCE CURVES (continued)

QUAD RATE

All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, 24-bit data, unless otherwise noted.

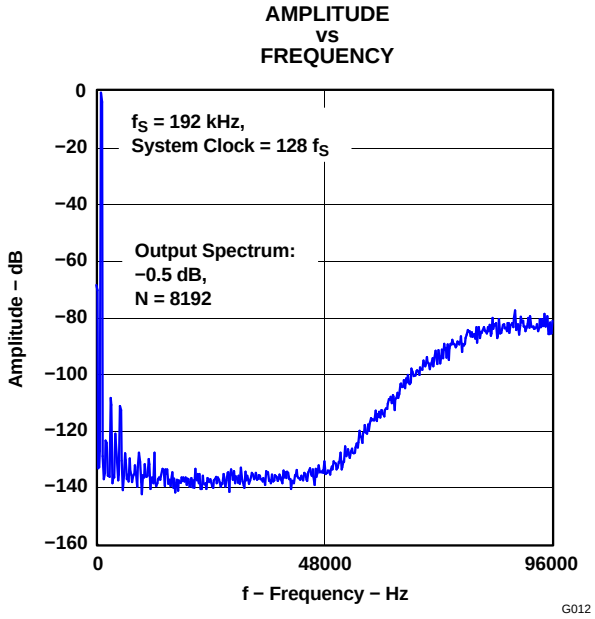


Figure 12.

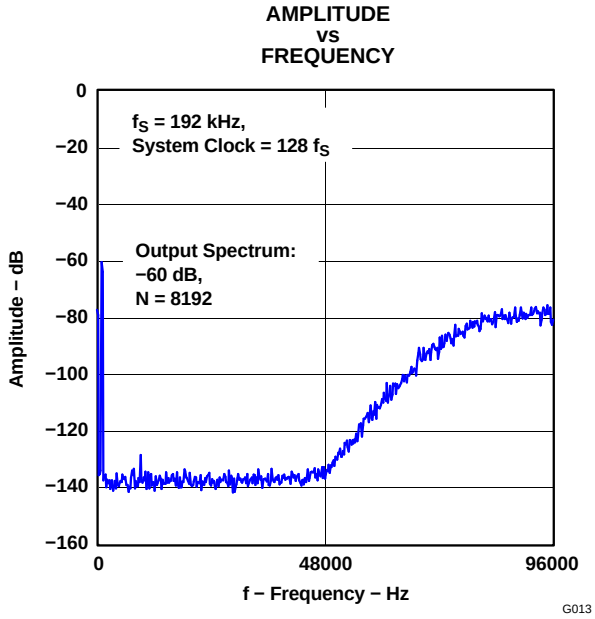


Figure 13.

DSD MODE

All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, f_S = 44.1 kHz, system clock = 16.9344 MHz, unless otherwise noted.

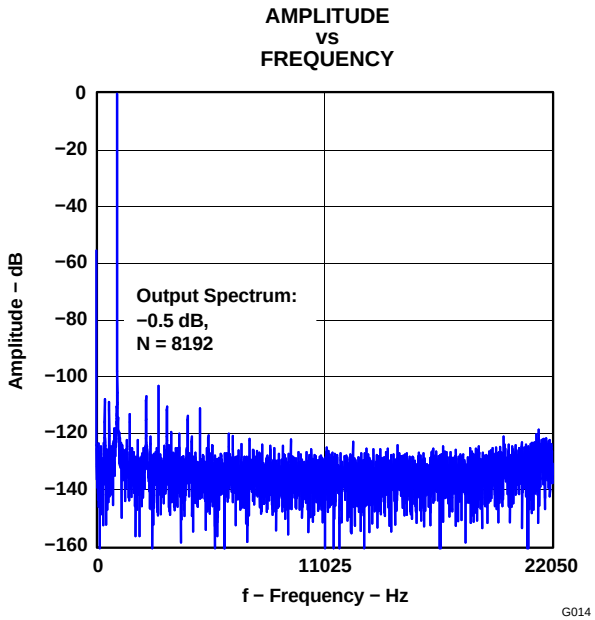


Figure 14.

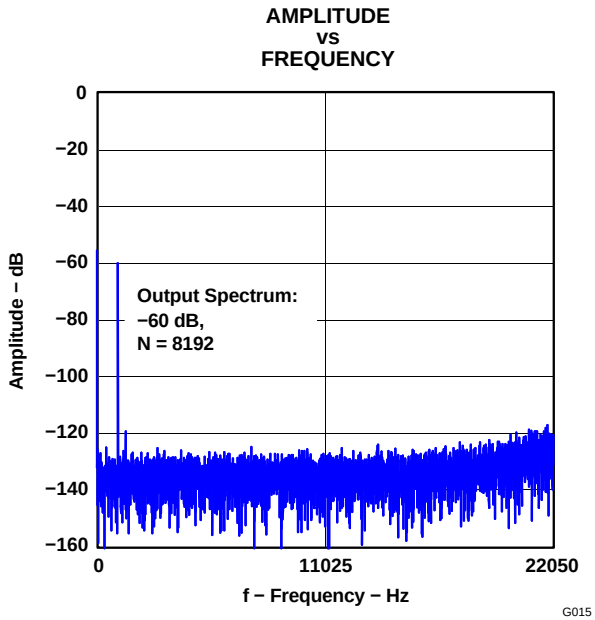


Figure 15.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER

LINEAR PHASE ANTIALIAS DIGITAL FILTER FREQUENCY RESPONSE

OVERALL CHARACTERISTICS
FOR SINGLE-RATE FILTER

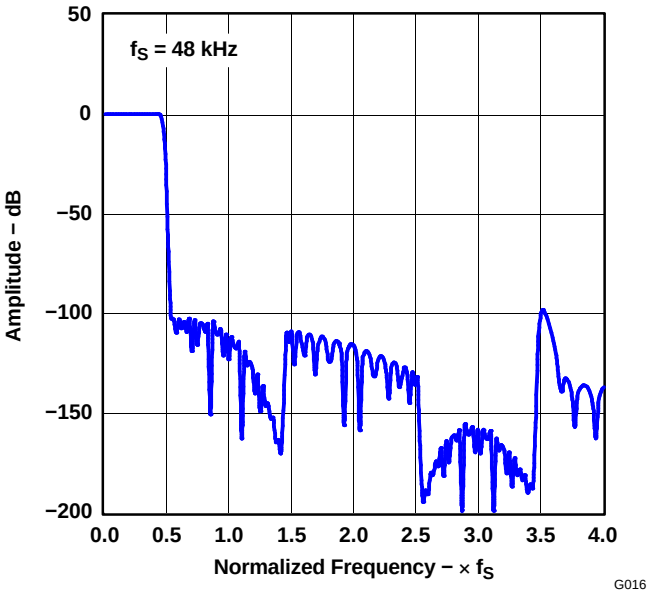


Figure 16.

STOP-BAND ATTENUATION CHARACTERISTICS
FOR SINGLE-RATE FILTER

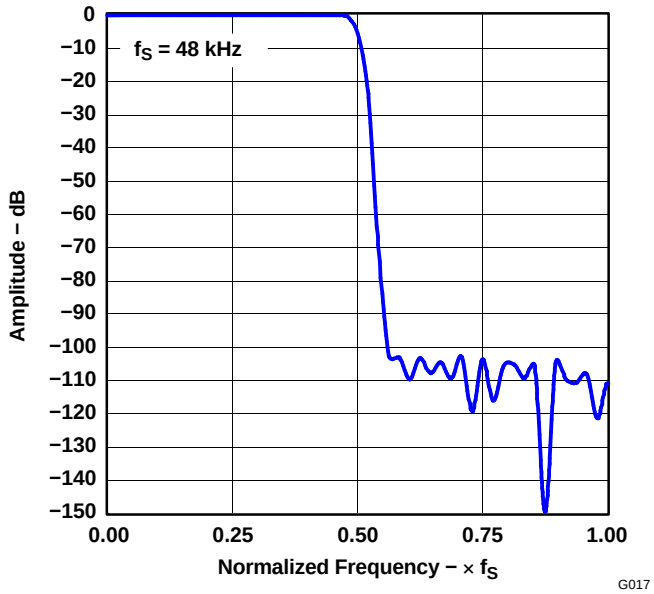


Figure 17.

PASS-BAND RIPPLE CHARACTERISTICS
FOR SINGLE-RATE FILTER

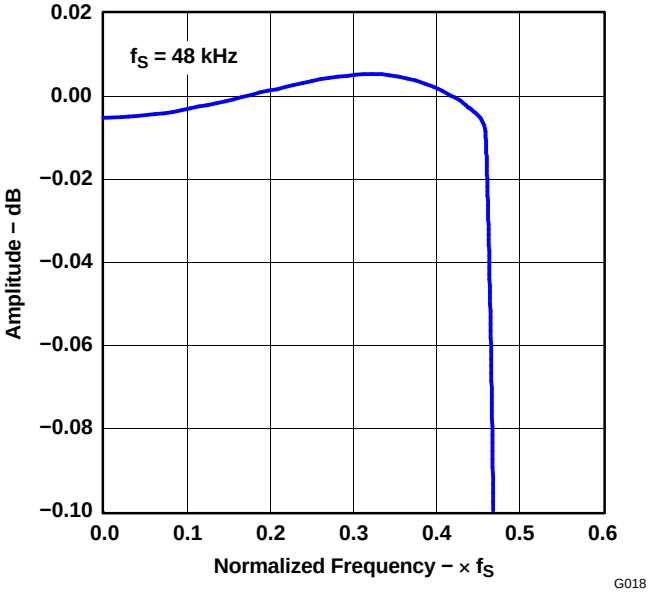


Figure 18.

TRANSIENT BAND CHARACTERISTICS
FOR SINGLE-RATE FILTER

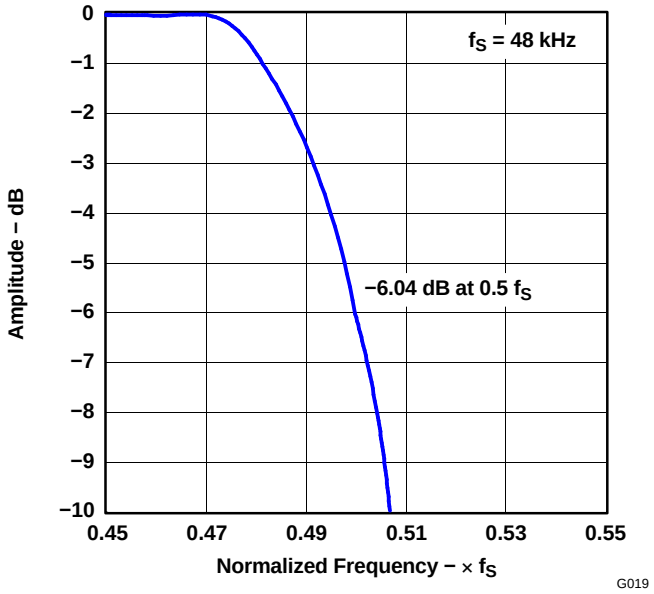


Figure 19.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (Continued)

LINEAR PHASE ANTIALIAS DIGITAL FILTER FREQUENCY RESPONSE (Continued)

OVERALL CHARACTERISTICS
FOR DUAL-RATE FILTER

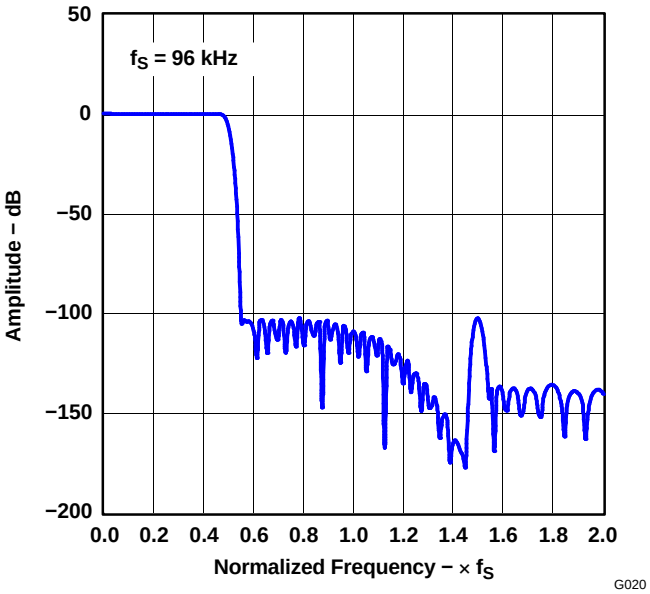


Figure 20.

STOP-BAND ATTENUATION CHARACTERISTICS
FOR DUAL-RATE FILTER

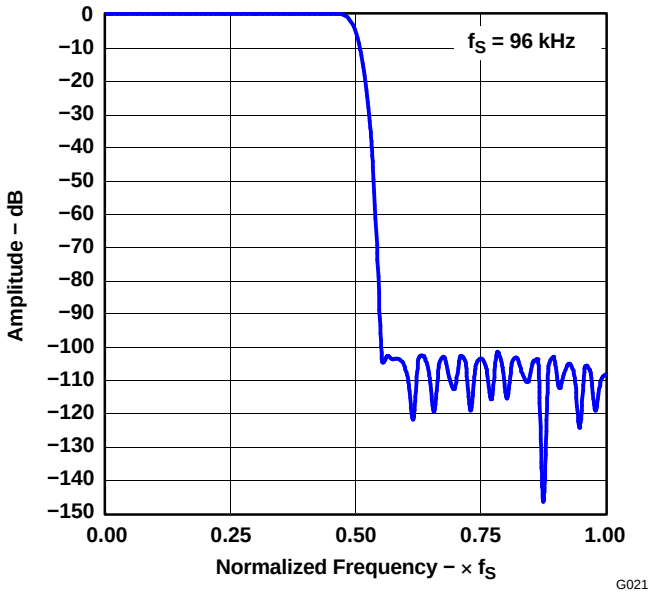


Figure 21.

PASS-BAND RIPPLE CHARACTERISTICS
FOR DUAL-RATE FILTER

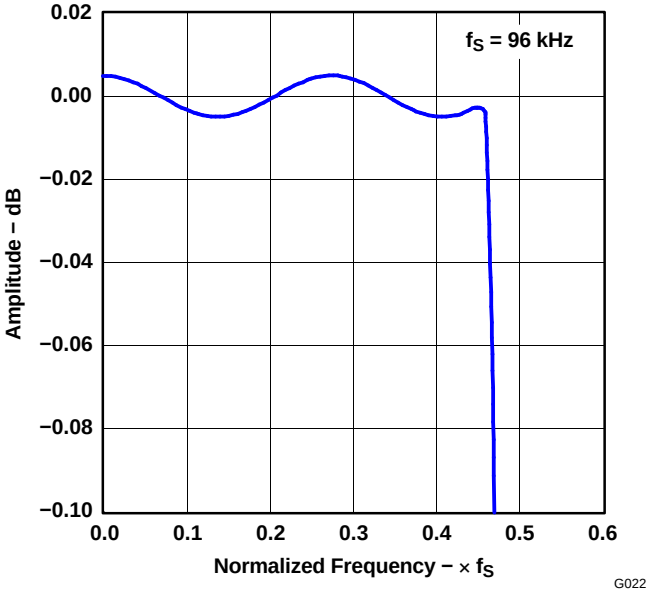


Figure 22.

TRANSIENT BAND CHARACTERISTICS
FOR DUAL-RATE FILTER

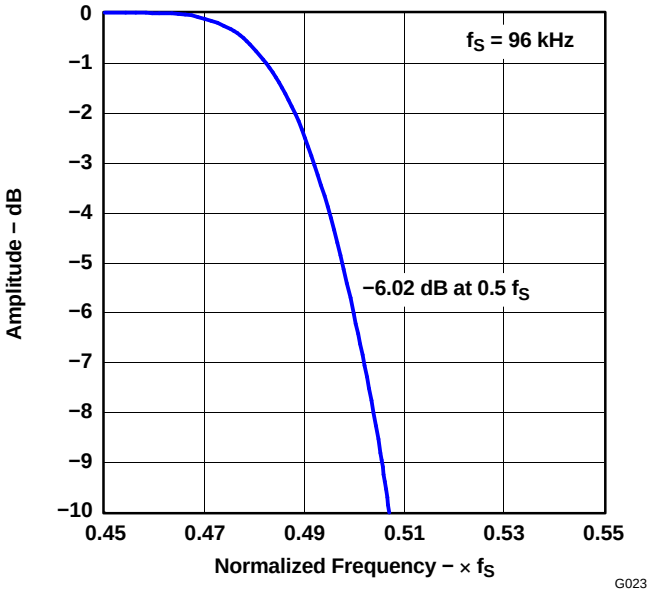


Figure 23.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (Continued)

LINEAR PHASE ANTIALIAS DIGITAL FILTER FREQUENCY RESPONSE (Continued)

OVERALL CHARACTERISTICS FOR QUAD-RATE FILTER

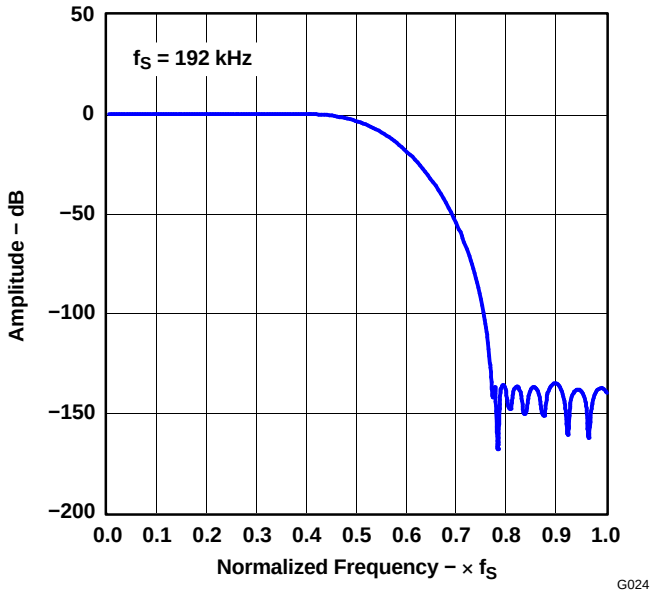


Figure 24.

STOP-BAND ATTENUATION CHARACTERISTICS FOR QUAD-RATE FILTER

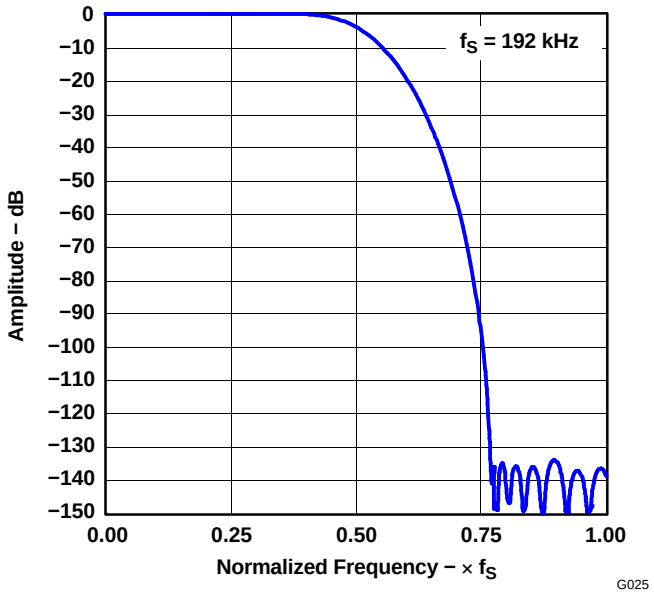


Figure 25.

PASS-BAND RIPPLE CHARACTERISTICS FOR QUAD-RATE FILTER

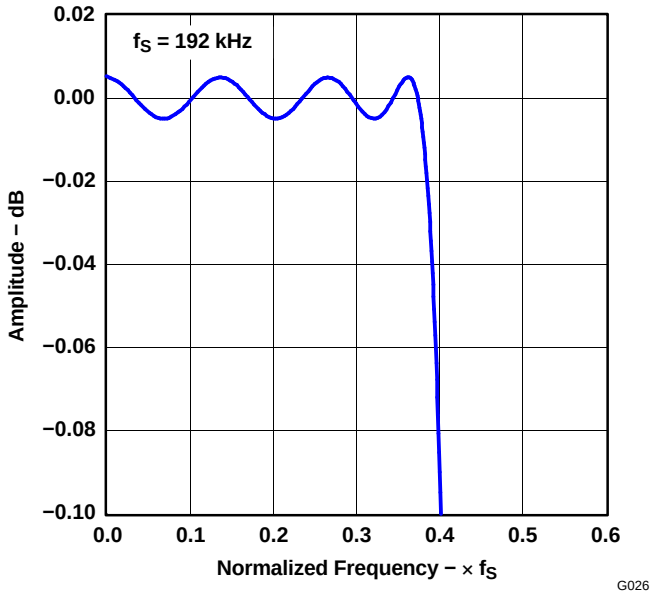


Figure 26.

TRANSIENT BAND CHARACTERISTICS FOR QUAD-RATE FILTER

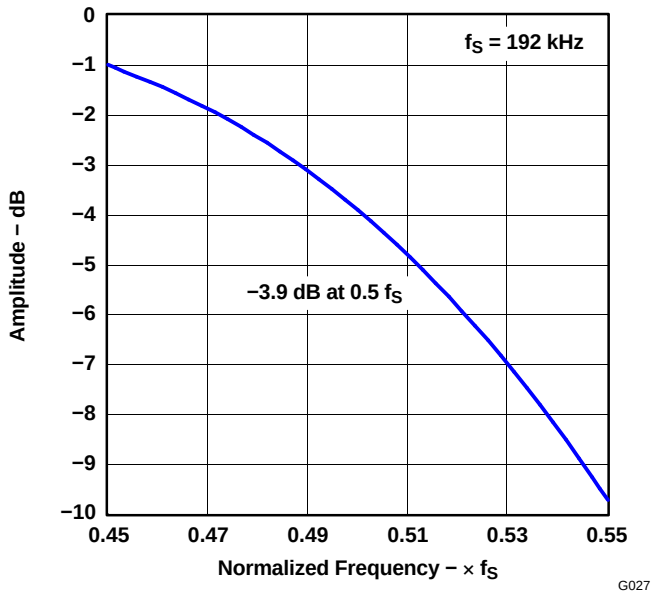


Figure 27.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (Continued)

HIGH-PASS FILTER (HPF) FREQUENCY RESPONSE

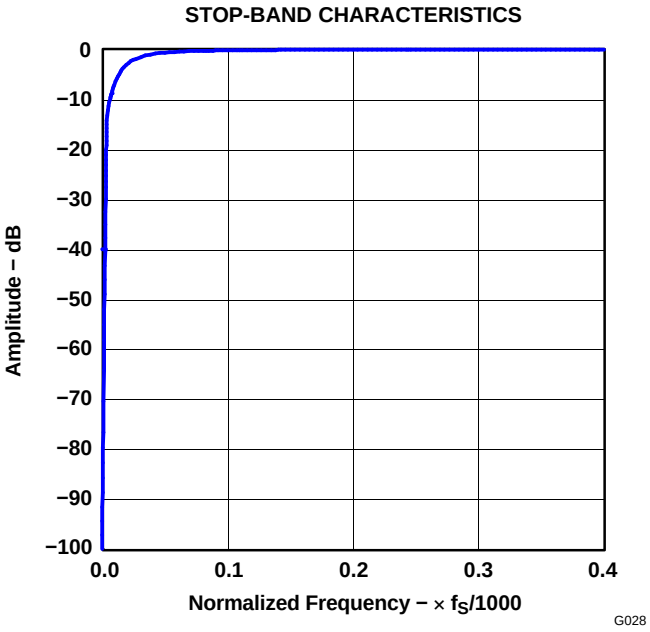


Figure 28.

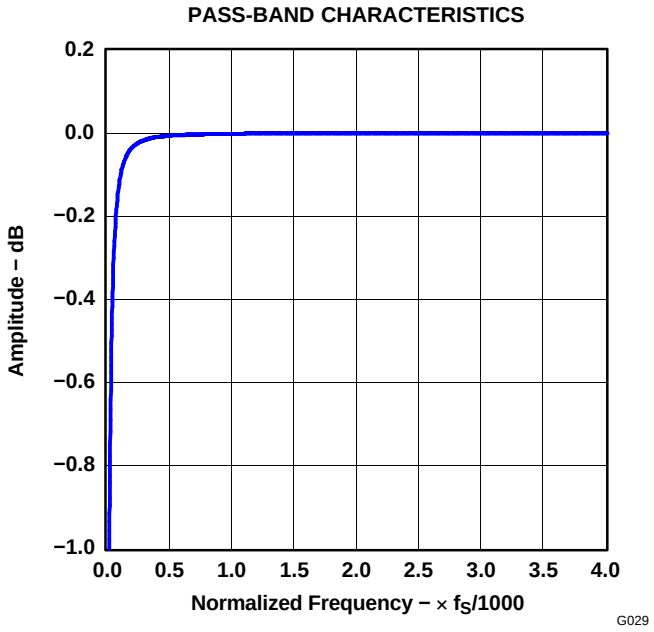


Figure 29.

PRINCIPLES OF OPERATION

THEORY OF OPERATION

The PCM1804 consists of a band-gap reference, a delta-sigma modulator with full-differential architecture for L-channel and R-channel, a decimation filter with a high-pass filter, and a serial interface circuit. Figure 30 illustrates the total architecture of the PCM1804. An on-chip, high-precision reference with 10-μF external capacitor(s) provides all the reference voltage needed in the PCM1804, and it defines the full-scale voltage range of both channels. Full-differential architecture provides a wide dynamic range and excellent power-supply rejection performance. The input signal is sampled at ×128, ×64, and ×32 oversampling rates according to the overasmpling ratio control, OSR[0:2]. The single rate, dual rate, and quad rate eliminate the external sample-hold amplifier. Figure 31 illustrates how for each oversampling ratio the PCM1804 decimates the modulator output down to PCM data when the modulator is running at 6.144 MHz. The delta-sigma modulation randomizes the modulator outputs and reduces the idle tone level. The oversampled data stream from the delta-sigma modulator is converted to a 1-f_S, 24-bit digital signal, while removing high-frequency noise components using a decimation filter. The dc components of the signal are removed by the HPF, and the HPF output is converted to a time-multiplexed serial signal through the serial interface, which provides flexible serial formats and master/slave modes. The PCM1804 also has a DSD output mode. The PCM1804 can output the signal directly from the modulators to DSDL (pin 16) and DSDR (pin 15).

PRINCIPLES OF OPERATION (continued)

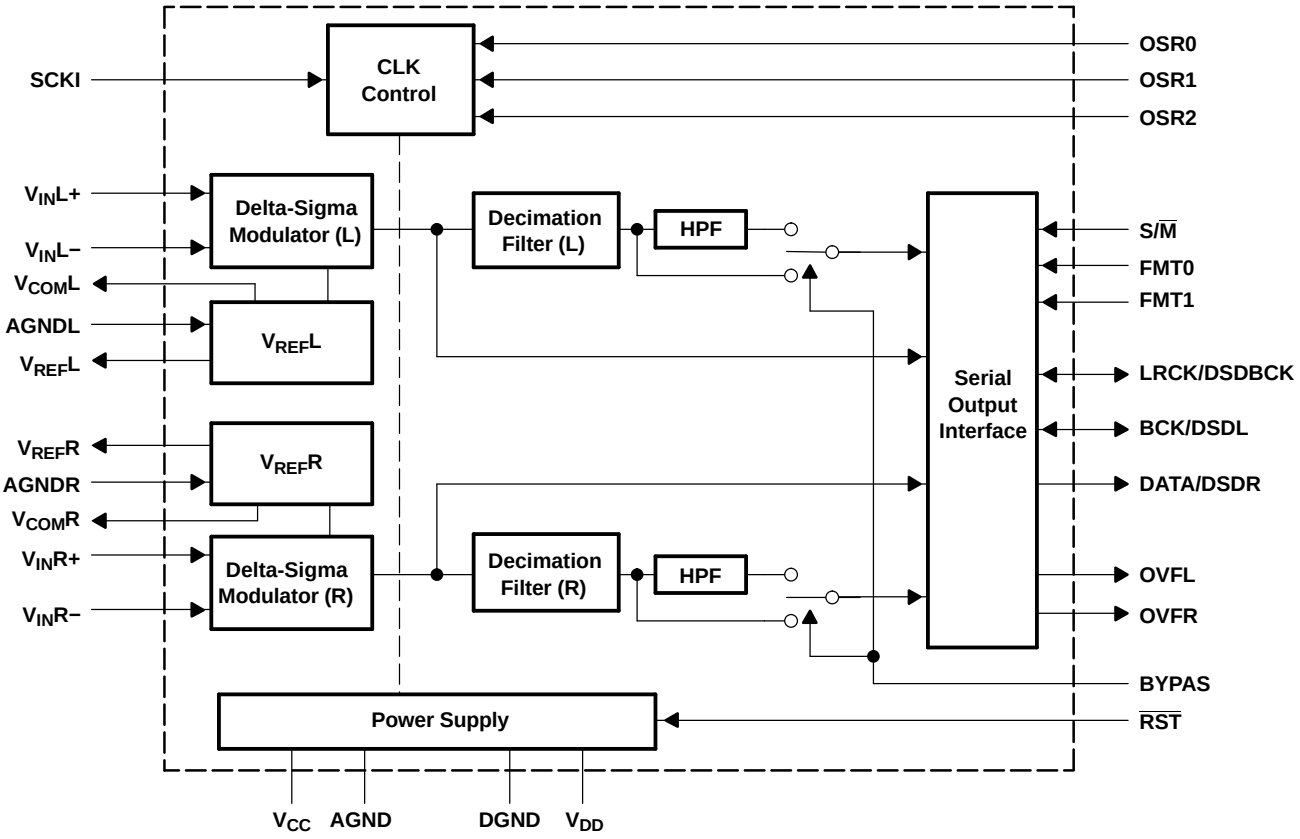


Figure 30. Total Block Diagram of PCM1804

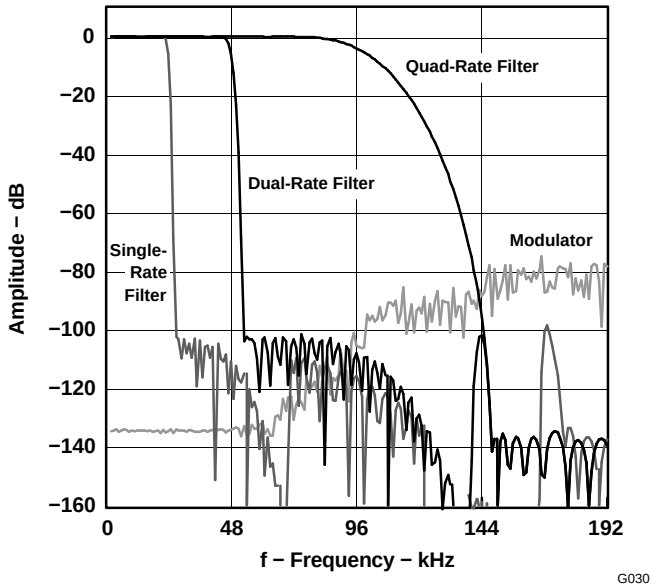
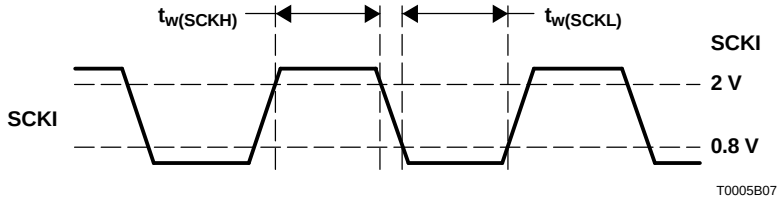


Figure 31. Spectrum of Modulator Output and Decimation Filter

PRINCIPLES OF OPERATION (continued)

SYSTEM CLOCK INPUT

The PCM1804 supports 128 f_S, 192 f_S (only in master mode at quad rate), 256 f_S, 384 f_S, 512 f_S, and 768 f_S as a system clock, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI (pin 18). Table 3 shows the relationship of typical sampling frequency and the system clock frequency, and Figure 32 shows system clock timing. In master mode, the system clock rate is selected by OSR2 (pin 11), OSR1 (pin 10), and OSR0 (pin 9) as shown in Table 1. In slave mode, the system clock rate is automatically detected. In DSD mode, OSR2 (pin 11), OSR1 (pin 10), OSR0 (pin 9), and the system clock frequency are fixed as shown in Table 1 and Table 3.



PARAMETER		MIN	UNIT
$t_{w(SCKH)}$	System clock pulse duration, HIGH	11	ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	11	ns

Figure 32. System Clock Input Timing

POWER-ON AND RESET FUNCTIONS

The PCM1804 has both an internal power-on-reset circuit and $\overline{RST}$ (pin 19). For internal power-on reset, initialization (reset) is performed automatically at the time when the power supply V_{DD} exceeds 2 V (typical) and V_{CC} exceeds 4 V (typical). $\overline{RST}$ accepts external forced reset, and a low level on $\overline{RST}$ initiates the reset sequence. Because an internal pulldown resistor terminates $\overline{RST}$, no connection of $\overline{RST}$ is equivalent to a low-level input. Because the system clock is used as a clock signal for the reset circuit, the system clock must be supplied as soon as power is supplied; more specifically, at least three system clocks are required prior to V_{DD} > 2 V, V_{CC} > 4 V, and $\overline{RST}$ = high. While V_{DD} < 2 V (typical), V_{CC} < 4 V (typical), or $\overline{RST}$ = low, and $1/f_S$ (maximum) count after V_{DD} > 2 V (typical),V_{CC} > 4 V (typical) and $\overline{RST}$ = high, the PCM1804 stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of $1116/f_S$ has passed. Figure 33 and Figure 34 illustrate the internal power-on-reset and external-reset timing, respectively. Figure 35 illustrates the digital output for power-on reset and $\overline{RST}$ control. The PCM1804 needs $\overline{RST}$ = low when control pins are changed or in slave mode when SCKI, LRCK, and BCK are changed.

POWER-DOWN FUNCTION

The PCM1804 has a power-down feature that is controlled by $\overline{RST}$ (pin 19). Entering the power-down mode is done by keeping the $\overline{RST}$ input level low for more than $65536/f_S$. In the master mode, the SCKI (pin 18) is used as the clock signal for the power-down counter. While in the slave mode, SCKI (pin 18) and LRCK (pin 17) are used as the clock signal. The clock(s) must be supplied until the power-down sequence completes. As soon as $\overline{RST}$ goes high, the PCM1804 starts the reset-release sequence described in the *Power-On and Reset Functions* section.

OVERSAMPLING RATIO

The oversampling ratio is selected by OSR2 (pin 11), OSR1 (pin 10), and OSR0 (pin 9) as shown in Table 1 and Table 2. The PCM1804 needs $\overline{RST}$ = low when logic levels on the OSR2, OSR1, and OSR0 pins are changed.

Table 1. Oversampling Ratio in Master Mode

OSR2	OSR1	OSR0	OVERSAMPLING RATIO	SYSTEM CLOCK RATE
Low	Low	Low	Single rate (× 128 f_S)	768 f_S
Low	Low	High	Single rate (× 128 f_S)	512 f_S
Low	High	Low	Single rate (× 128 f_S)	384 f_S
Low	High	High	Single rate (× 128 f_S)	256 f_S
High	Low	Low	Dual rate (× 64 f_S)	384 f_S
High	Low	High	Dual rate (× 64 f_S)	256 f_S
High	High	Low	Quad rate (× 32 f_S)	192 f_S
High	High	High	Quad rate (× 32 f_S)	128 f_S
High	Low	Low	DSD mode (× 64 f_S)	384 f_S
High	Low	High	DSD mode (× 64 f_S)	256 f_S

Table 2. Oversampling Ratio in Slave Mode

OSR2	OSR1	OSR0	OVERSAMPLING RATIO	SYSTEM CLOCK RATE
Low	Low	Low	Single rate (× 128 f_S)	Automatically detected
Low	Low	High	Dual rate (× 64 f_S)	Automatically detected
Low	High	Low	Quad rate (× 32 f_S)(1)	Automatically detected
Low	High	High	Reserved	–
High	Low	Low	Reserved	–
High	Low	High	Reserved	–
High	High	Low	Reserved	–
High	High	High	Reserved	–

(1) Only at the 128-f_S system clock rate

Table 3. Sampling Frequency and System Clock Frequency

OVERSAMPLING RATIO	SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)					
		128 f_S	192 f_S(1)	256 f_S	384 f_S	512 f_S	768 f_S
Single rate(2)	32	–	–	8.192	12.288	16.384	24.576
	44.1	–	–	11.2896	16.9344	22.5792	33.8688
	48	–	–	12.288	18.432	24.576	36.864
Dual rate(3)	88.2	–	–	22.5792	33.8688	–	–
	96	–	–	24.576	36.864	–	–
Quad rate(4)	176.4	22.5792	33.8688	–	–	–	–
	192	24.576	36.864	–	–	–	–
DSD mode(3)	44.1	–	–	11. 2896	16.9344	–	–

(1) Only available in master mode at the quad rate
(2) Modulator is running at 128 f_S.
(3) Modulator is running at 64 f_S.
(4) Modulator is running at 32 f_S.

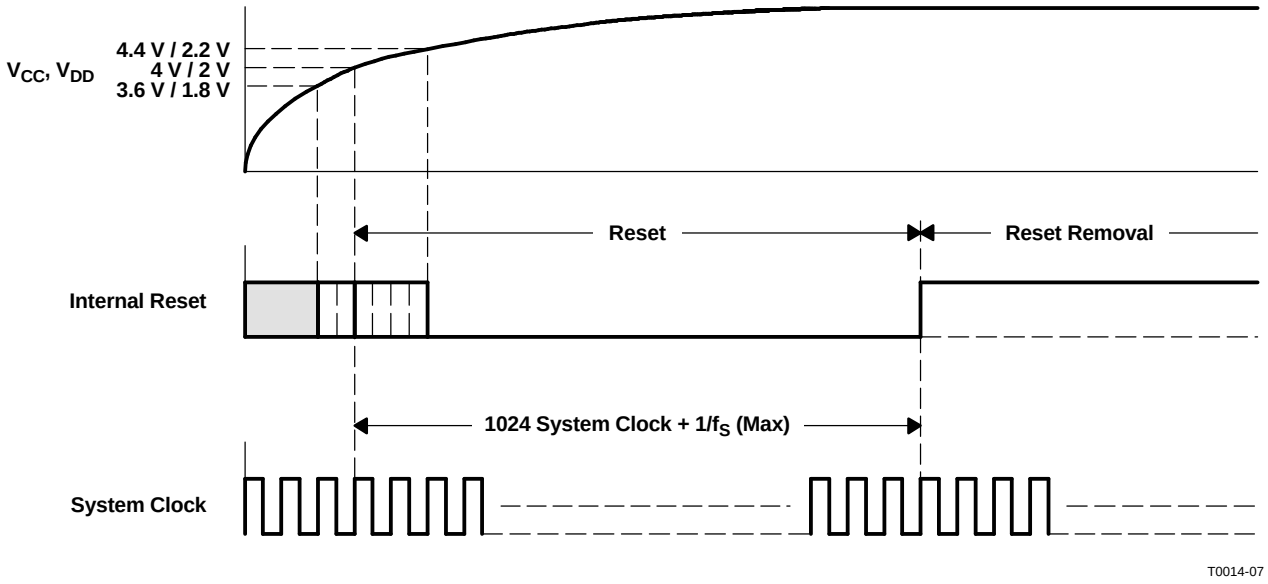


Figure 33. Internal Power-On-Reset Timing

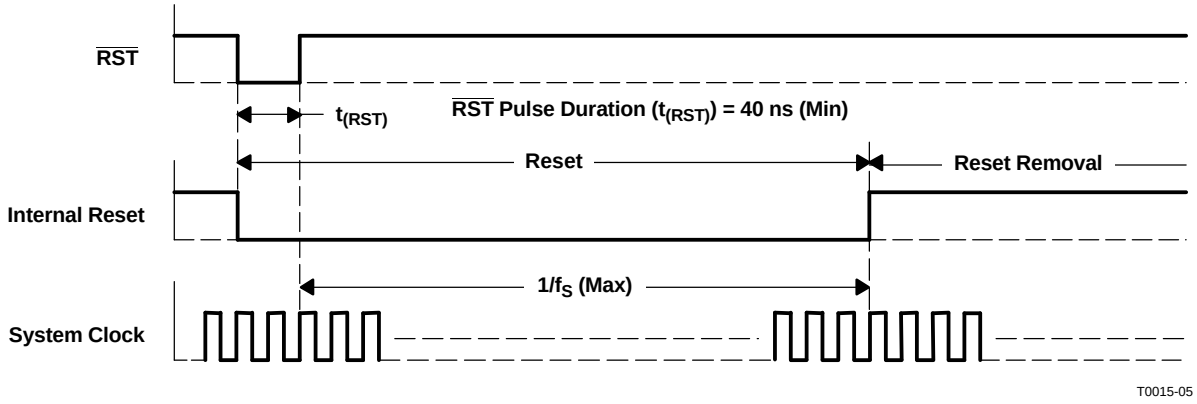
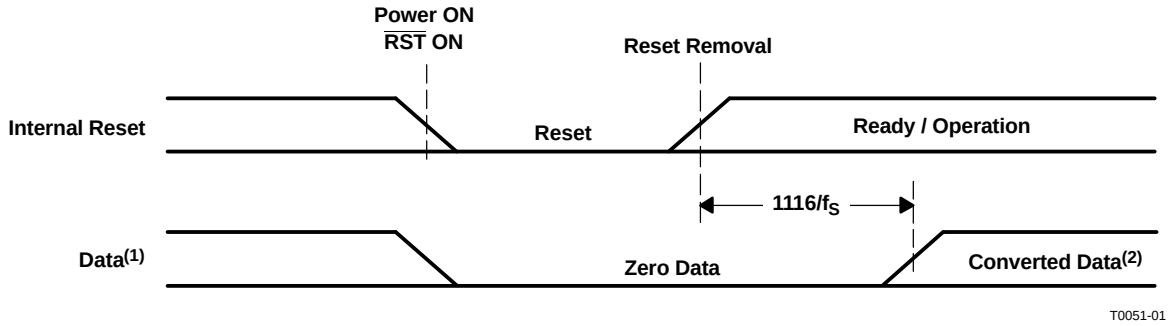


Figure 34. External Reset Timing



(1) In the DSD mode, DSDL is also controlled like DSDR.

(2) The HPF transient response appears initially.

Figure 35. ADC Digital Output for Power-On Reset and $\overline{RST}$ Control

AUDIO DATA INTERFACE

The PCM1804 interfaces the audio system through BCK/DSDL (pin 16), LRCK/DSDBCK (pin 17), and DATA/DSDR (pin 15). The PCM1804 needs $\overline{RST}$ = low when in the interface mode and/or the data format are changed.

INTERFACE MODE

The PCM1804 supports master mode and slave mode as interface modes, which are selected by S/$\overline{M}$ (pin 8) as shown in Table 4. In master mode, the PCM1804 provides the timing of the serial audio data communications between the PCM1804 and the digital audio processor or external circuit. While in slave mode, the PCM1804 receives the timing for data transfer from an external controller. Slave mode is not available for DSD.

Table 4. Interface Mode

S/$\overline{M}$	MODE
Low	Master mode
High	Slave mode

DATA FORMAT

The PCM1804 supports four audio data formats in both master and slave modes, and these data formats are selected by FMT0 (pin 6) and FMT1 (pin 7) as shown in Table 5.

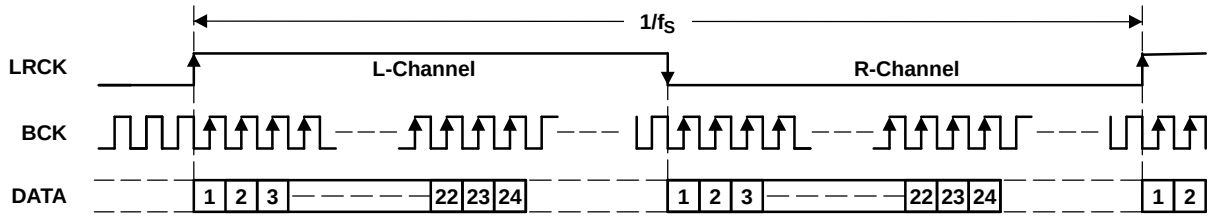
Table 5. Data Format

FMT1	FMT0	FORMAT	MASTER	SLAVE
Low	Low	PCM, left-justified, 24-bit	Yes	Yes
Low	High	PCM, I^2S, 24-bit	Yes	Yes
High	Low	PCM, standard, 24-bit	Yes	Yes
High	High	DSD	Yes	–

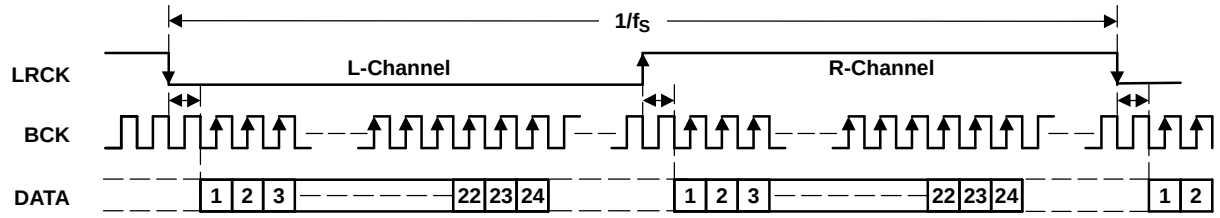
INTERFACE TIMING FOR PCM

Figure 36 through Figure 38 illustrate the interface timing for PCM.

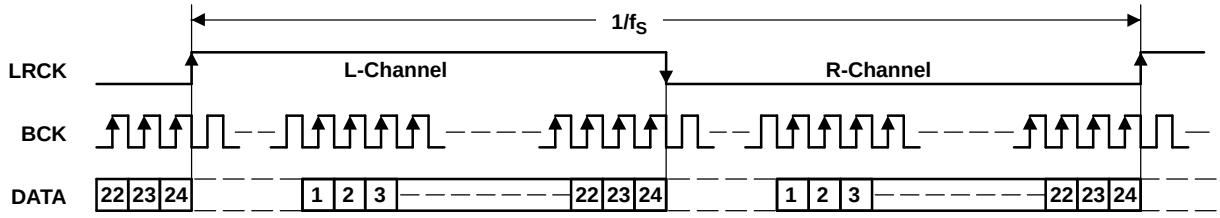
(1) Left-Justified Data Format; L-Channel = High, R-Channel = Low



(2) I²S Data Format; L-Channel = Low, R-Channel = High



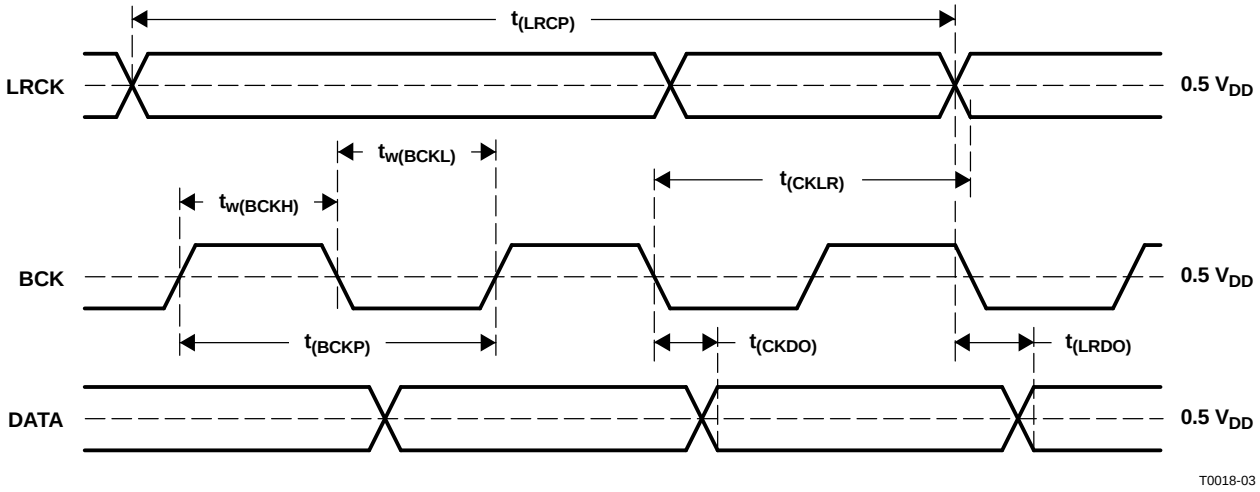
(3) Standard Data Format; L-Channel = High, R-Channel = Low



T0009-03

NOTE: LRCK and BCK work as outputs in master mode and as inputs in slave mode.

Figure 36. Audio Data Format for PCM



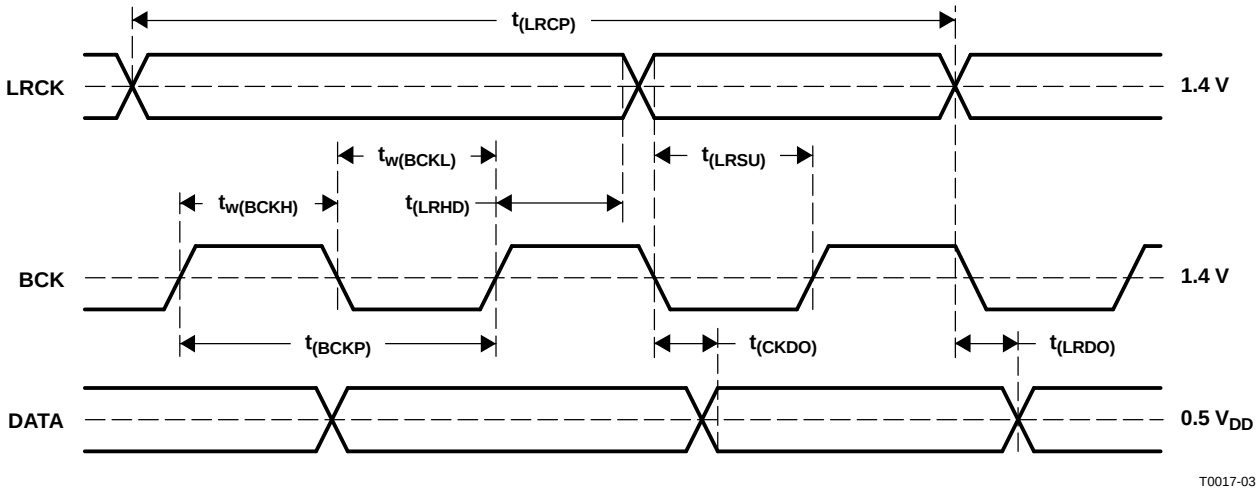
PARAMETERS		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period		1/(64 f_S)(3)		
$t_{W(BCKH)}$	BCK pulse duration, HIGH	32			ns
$t_{W(BCKL)}$	BCK pulse duration, LOW	32			ns
$t_{(CKLR)}$	Delay time, BCK falling edge to LRCK valid	–5		15	ns
$t_{(LRCP)}$	LRCK period		1/f_S		
$t_{(CKDO)}$	Delay time, BCK falling edge to DATA valid	–5		15	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DATA valid	–5		15	ns
t_r	Rising time of all signals(1)(2)			10	ns
t_f	Falling time of all signals(1)(2)			10	ns

(1) Rising and falling times are measured from 10% to 90% of IN/OUT signal swing.

(2) Load capacitance of all signals is 10 pF.

(3) $t_{(BCKP)}$ is fixed at 1/(64 f_S) in case of master mode.

Figure 37. Audio Data Interface Timing for PCM (Master Mode: LRCK and BCK Work as Outputs)



PARAMETERS		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	1/(64 f_S)		1/(48 f_S)	
$t_{w(BCKH)}$	BCK pulse duration, HIGH	32			ns
$t_{w(BCKL)}$	BCK pulse duration, LOW	32			ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	12			ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	12			ns
$t_{(LRCP)}$	LRCK period		1/f_S		
$t_{(CKDO)}$	Delay time, BCK falling edge to DATA valid	5		25	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DATA valid	5		25	ns
t_r	Rising time of all signals(1)(2)			10	ns
t_f	Falling time of all signals(1)(2)			10	ns

(1) Rising and falling times are measured from 10% to 90% of IN/OUT signals swing.

(2) Load capacitance of DATA/DSDR signal is 10 pF.

Figure 38. Audio Data Interface Timing for PCM (Slave Mode: LRCK and BCK Work as Inputs)

INTERFACE TIMING FOR DSD

Figure 39 and Figure 40 illustrate the interface timing for DSD.

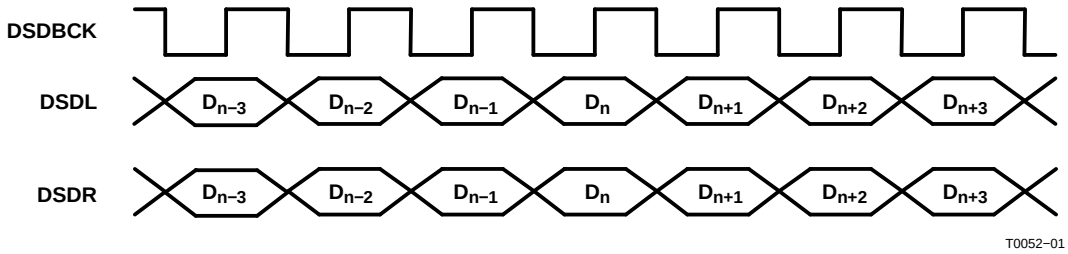
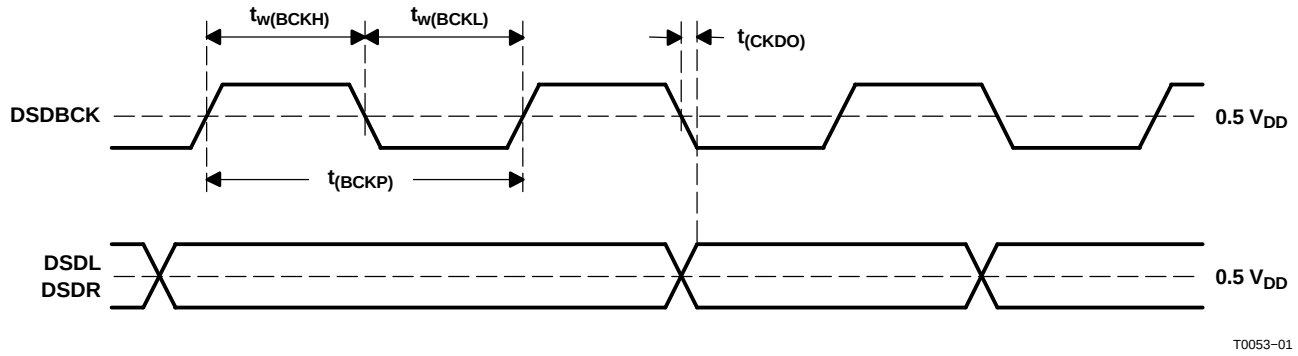


Figure 39. Audio Data Format



PARAMETERS		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	DSDBCK period		354		ns
$t_{W(BCKH)}$	DSDBCK pulse duration, HIGH		177		ns
$t_{W(BCKL)}$	DSDBCK pulse duration, LOW		177		ns
$t_{(CKDO)}$	Delay time DSDBCK falling edge to DSDL, DSDR valid	–5		15	ns
t_r	Rising time of all signals(1)(2)			10	ns
t_f	Falling time of all signals(1)(2)			10	ns

(1) Rising and falling times are measured from 10% to 90% of IN/OUT signal swing.

(2) Load capacitance of DSDBCK/DSDL/DSDR signal is 10 pF.

Figure 40. Audio Data Interface Timing for DSD (Master Mode Only)

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM FOR PCM

In slave mode, the PCM1804 operates under LRCK synchronized with the system clock SCKI. The PCM1804 does not need a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCK during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_S$ and digital output is forced into BPZ code until resynchronization between LRCK and SCKI is completed.

In case of changes less than ±5 BCK, resynchronization does not occur and the previously described digital output control and discontinuity do not occur.

Figure 41 illustrates ADC digital output for loss of synchronization and resynchronization. During undefined data, the PCM1804 may generate some noise in the audio signal. Also, the transitions of normal to undefined data and undefined or zero data to normal cause a discontinuity of data on the digital output. This can generate noise in the audio signal. In master mode, synchronization loss never occurs.

HIGH-PASS FILTER (HPF) BYPASS CONTROL FOR PCM

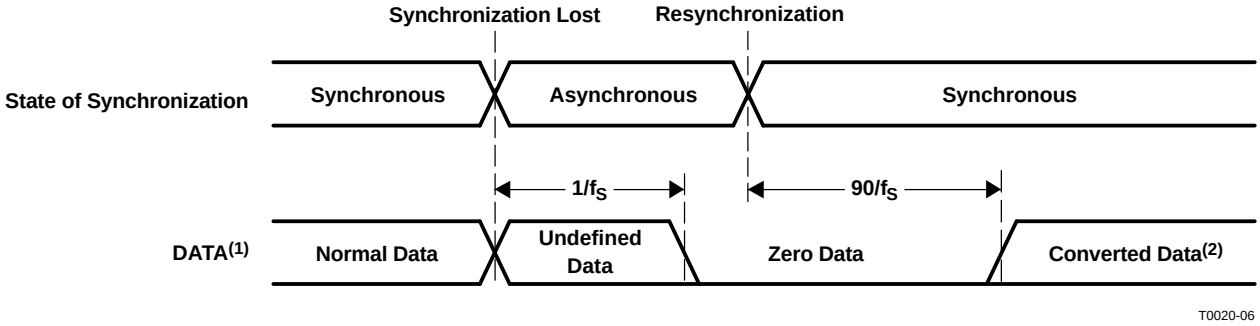
The built-in function for dc component rejection can be bypassed by BYPAS (pin 12) control. In bypass mode, the dc component of the input analog signal and the internal dc offset are also converted and output in the digital output data.

HPF Bypass Control

BYPAS PIN	HPF MODE
Low	Normal (high-pass) mode
High	Bypass (through) mode

OVERFLOW FLAG FOR PCM

The PCM1804 has two overflow flag pins, OVFR (pin 20) and OVFL (pin 21). The pins go to high as soon as the analog input goes across the full-scale range. The high level is held for 1.016 s at maximum, and returns to low if the analog input does not go across the full-scale range for the period.



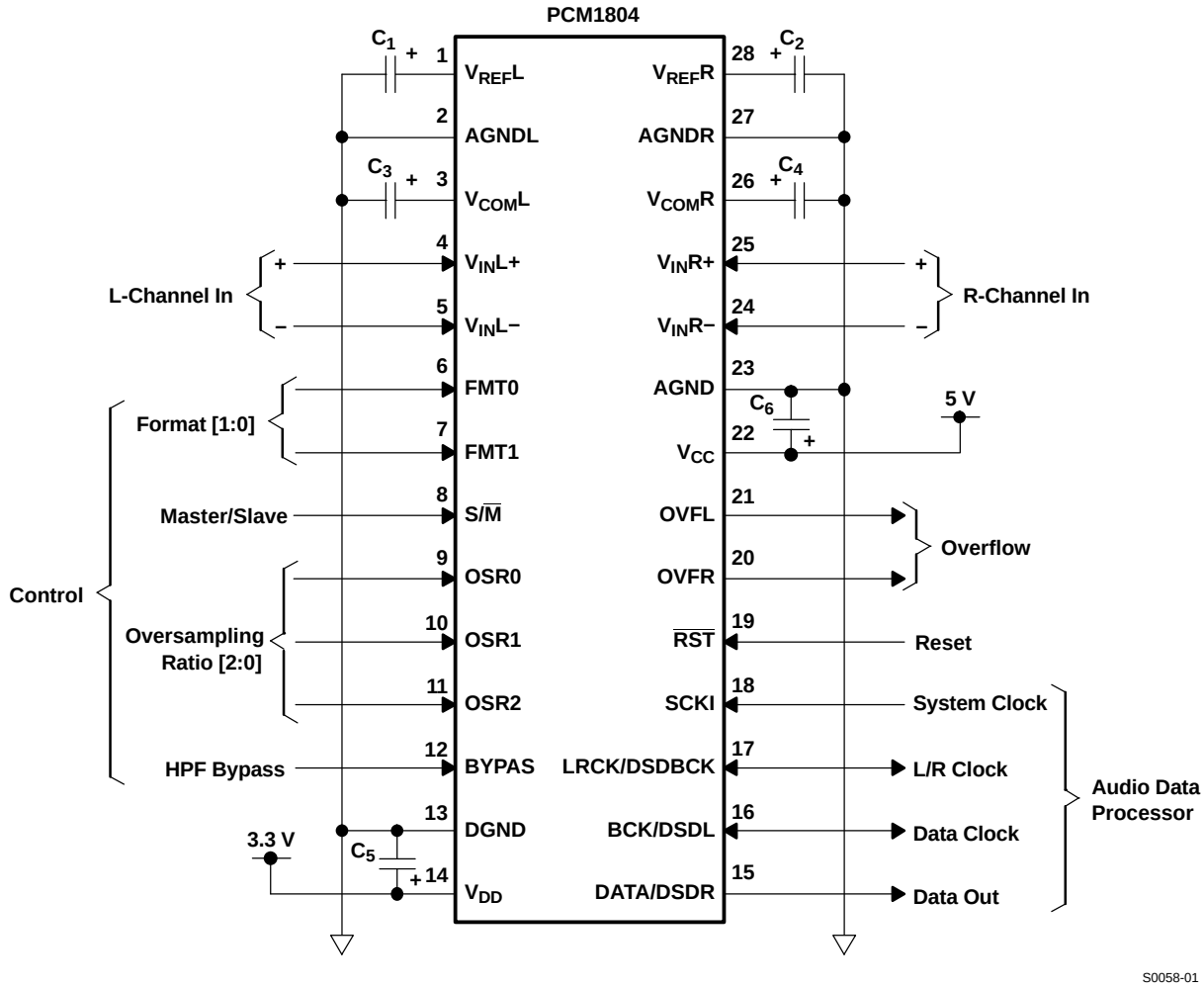
(1) Applies only for slave mode; the loss of synchronization never occurs in master mode.

(2) The HPF transient response appears initially.

Figure 41. ADC Digital Output for Loss of Synchronization and Resynchronization

TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 42 illustrates a typical circuit connection diagram in the PCM data format operation.

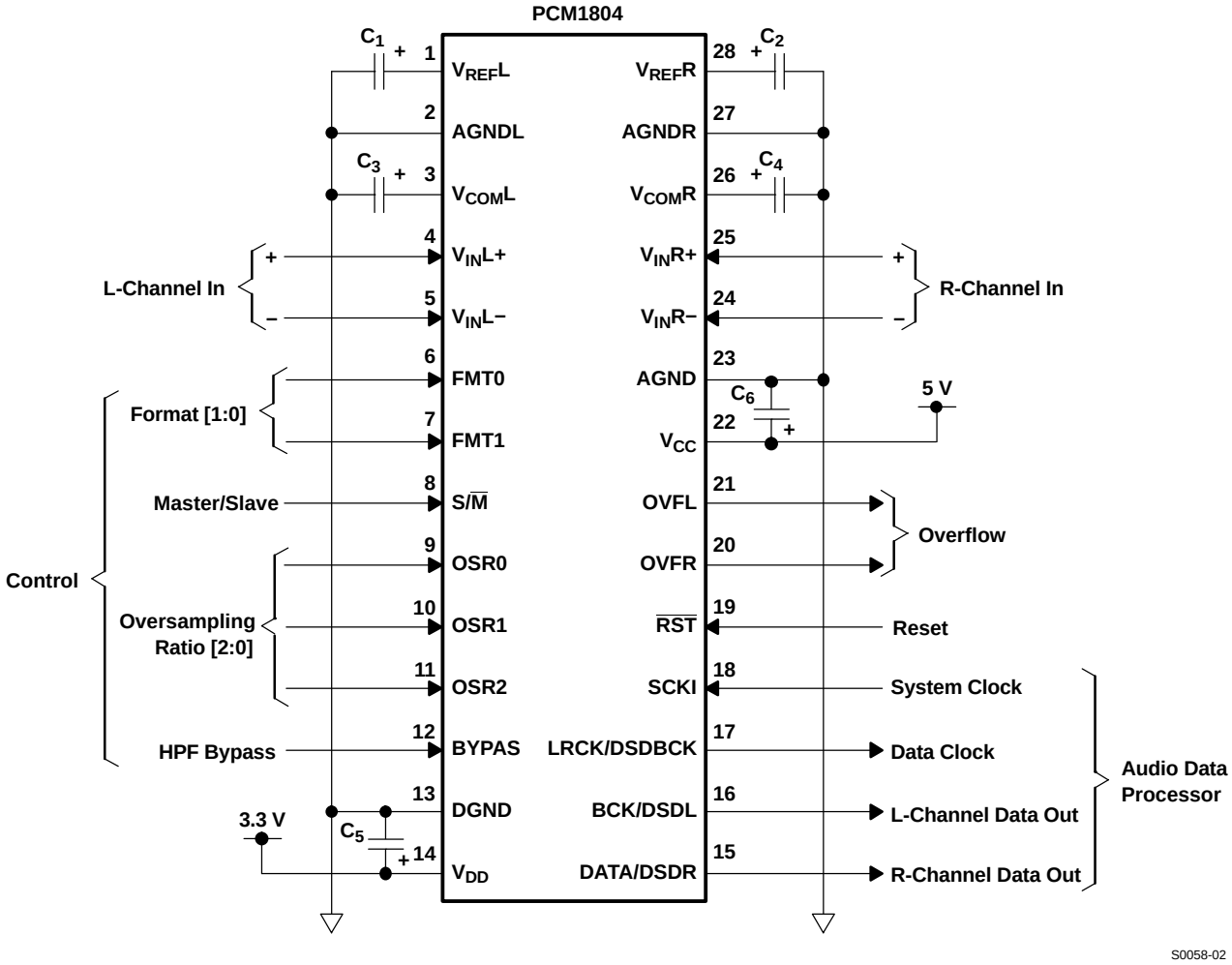


A. C1, C2, C5, and C6: Bypass capacitors, 0.1-µF ceramic and 10-µF tantalum, depending on layout and power supply

B. C3, C4: Bypass capacitor, 0.1-µF tantalum, depending on layout and power supply

Figure 42. Typical Circuit Connection Diagram for PCM

Figure 43 illustrates a typical circuit connection diagram in the DSD data format operation.



A. C1, C2, C5, and C6: Bypass capacitors, 0.1-µF ceramic and 10-µF tantalum, depending on layout and power supply

B. C3 and C4: Bypass capacitors, 0.1-µF tantalum, depending on layout and power supply

Figure 43. Typical Circuit Connection Diagram for DSD

APPLICATION INFORMATION

BOARD DESIGN AND LAYOUT CONSIDERATIONS

V_{CC}, V_{DD} Pins

The digital and analog power supply lines to the PCM1804 should be bypassed to the corresponding ground pins with 0.1-μF ceramic and 10-μF tantalum capacitors placed as close to the pins as possible to maximize the dynamic performance of the ADC. Although the PCM1804 has two power lines to maximize the potential of dynamic performance, using one common power supply is recommended to avoid unexpected power-supply trouble like latch-up or power-supply sequence.

V_{IN} Pins

Use of 0.01-μF film capacitors between $V_{IN}L+$ and $V_{IN}L-$ and between $V_{IN}R+$ and $V_{IN}R-$ is strongly recommended to remove higher-frequency noise from the delta-sigma input section.

$V_{REF}X$, $V_{COM}X$ Inputs

Use 0.1-μF ceramic and 10-μF tantalum capacitors between $V_{REF}L$, $V_{REF}R$, and corresponding AGNDx, to ensure low-source impedance at ADC references. Use 0.1-μF tantalum capacitors between $V_{COM}L$, $V_{COM}R$ and corresponding AGNDx to ensure low source impedance of common voltage. These capacitors should be located as close as possible to the $V_{REF}L$, $V_{REF}R$, $V_{COM}L$, and $V_{COM}R$ pins to reduce dynamic errors on references and common voltage. The dc voltage level of these pins is 2.5 V.

DATA/DSDR, BCK/DSDL, and LRCK/DSDBCK Pins

The DATA/DSDR, BCK/DSDL, and LRCK/DSDBCK pins in master mode have large load drive capability. Locating the buffer near the PCM1804 and minimizing the load capacitance, minimizes the digital-analog crosstalk and maximizes the dynamic performance of the ADC.

System Clock

The quality of the system clock can influence dynamic performance, as the PCM1804 operates based on a system clock. Therefore, it might be necessary to consider the system clock duty, jitter, and the time difference between system clock transition and BCK/DSDL or LRCK/DSDBCK transition in slave mode.

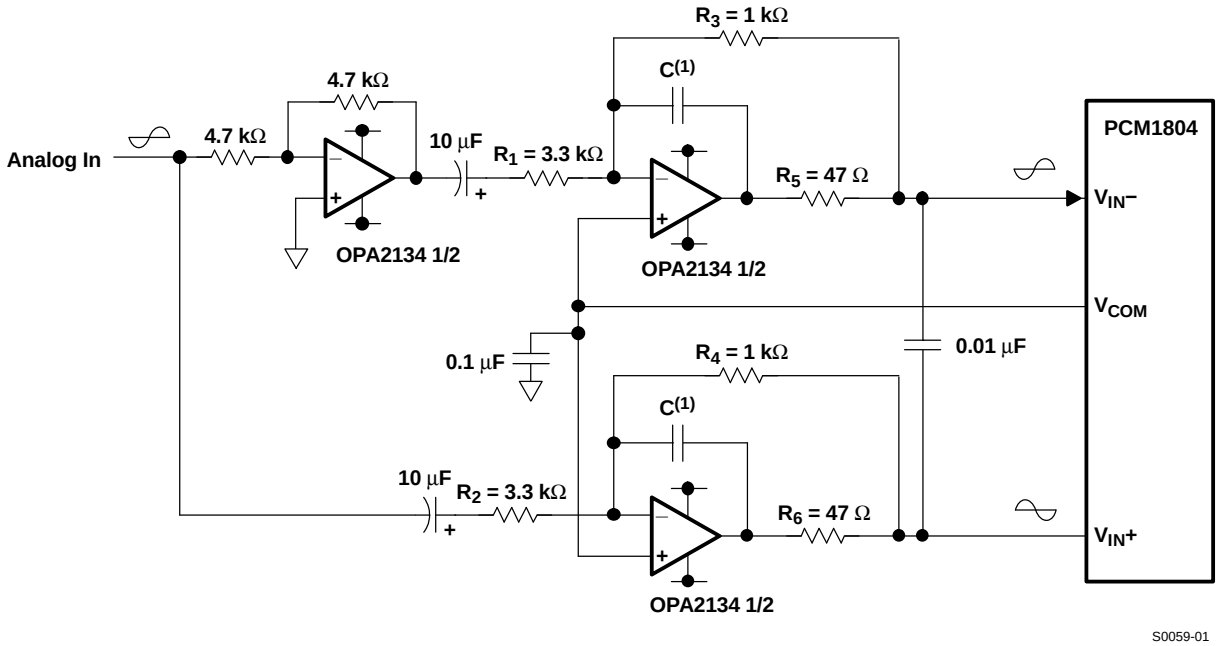
Reset Control

If capacitors larger than 10 μF are used on $V_{REF}L$ and $V_{REF}R$, an external reset control with a delay time corresponding to the $V_{REF}L$ and $V_{REF}R$ response is required. Also, it works as a power-down control.

APPLICATION CIRCUIT FOR SINGLE-ENDED INPUT

An application diagram for a single-ended input circuit is shown in Figure 44. The maximum signal input voltage and differential gain of this circuit is designed as Vinmax = 8.28 Vpp, Ad = 0.3. Differential gain (Ad) is given by R3/R1(R4/R2) in a circuit configured as a normal inverted-gain amplifier. Resistor R5(R6) in the feedback loop gives low-impedance drive operation and noise filtering for the analog input of the PCM1804. The circuit technique using R5(R6) is recommended.

APPLICATION INFORMATION (continued)



(1) A capacitor value of 1800 pF is recommended, unless an input signal greater than –6 dBFS at 100 kHz or higher is applied in the DSD mode. In that case, 3300 pF is recommended.

Figure 44. Application Circuit for Single-Ended Input Circuit (PCM)

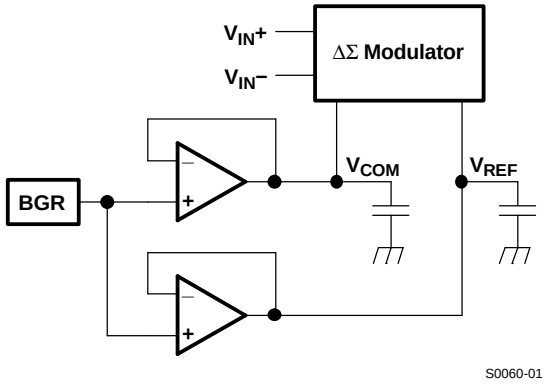


Figure 45. Equivalent Circuit of Internal Reference (V_{COM}, V_{REF})

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCM1804DB	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1804DBG4	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1804DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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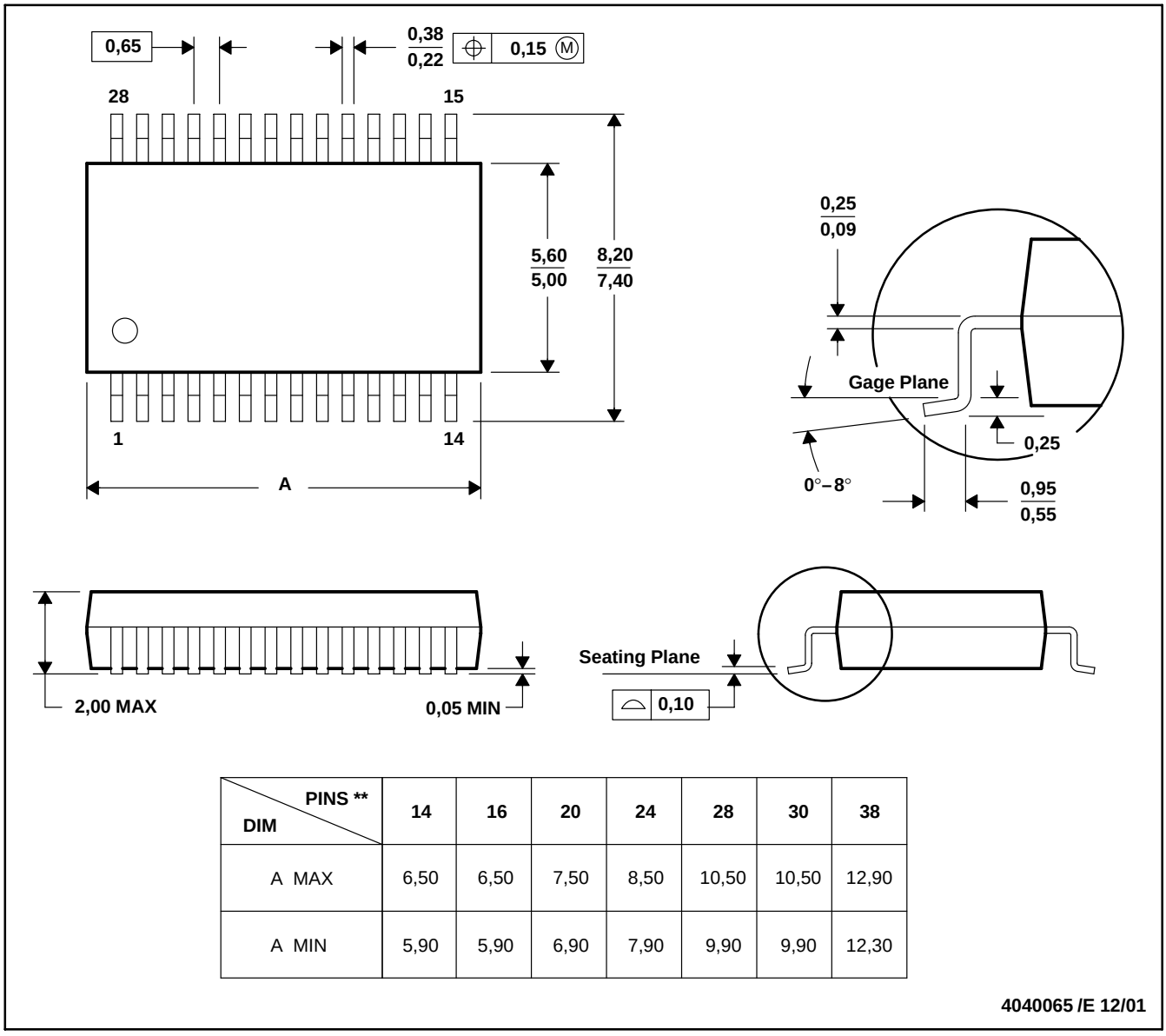
MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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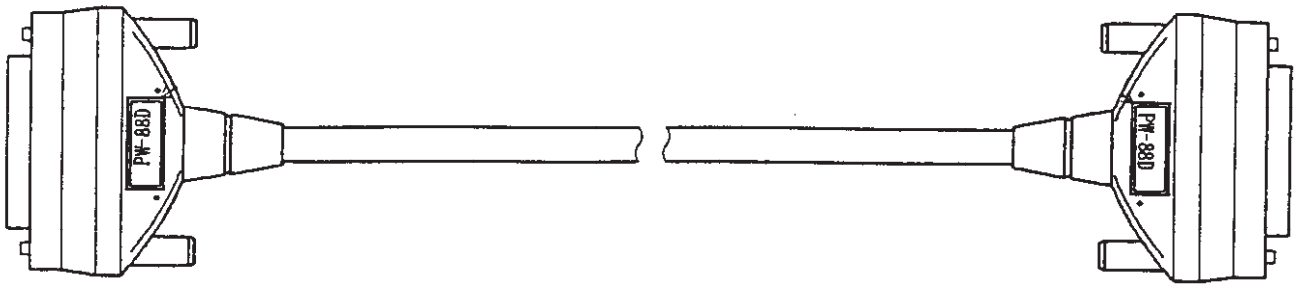
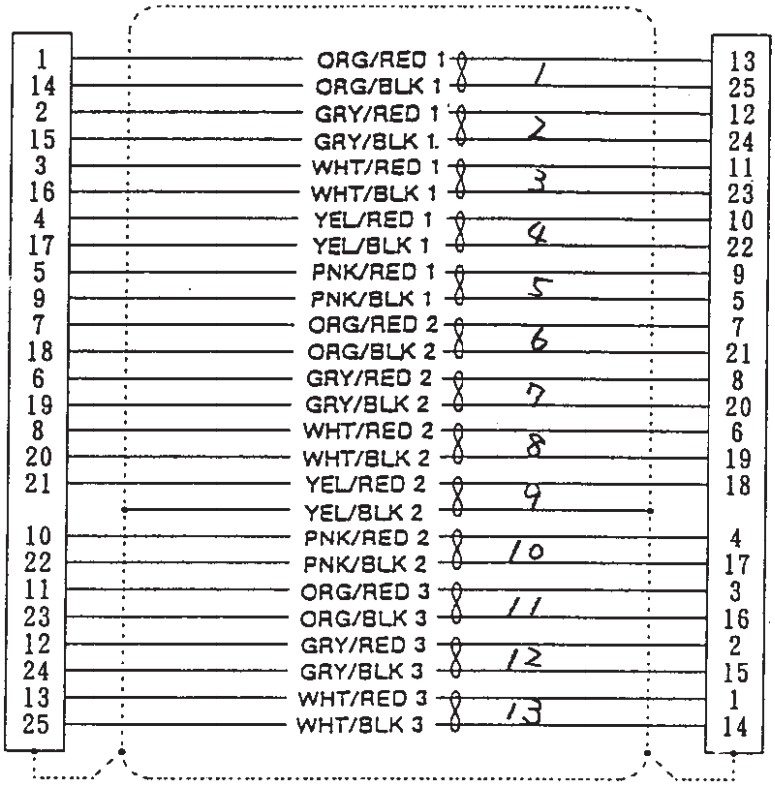
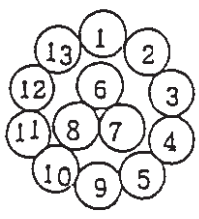
THE CABLES FOR TDIF



Male Male

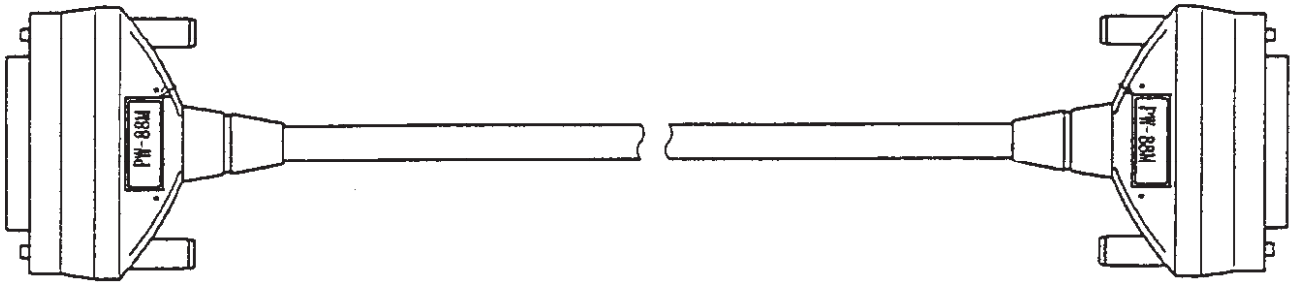


means Twisted wire

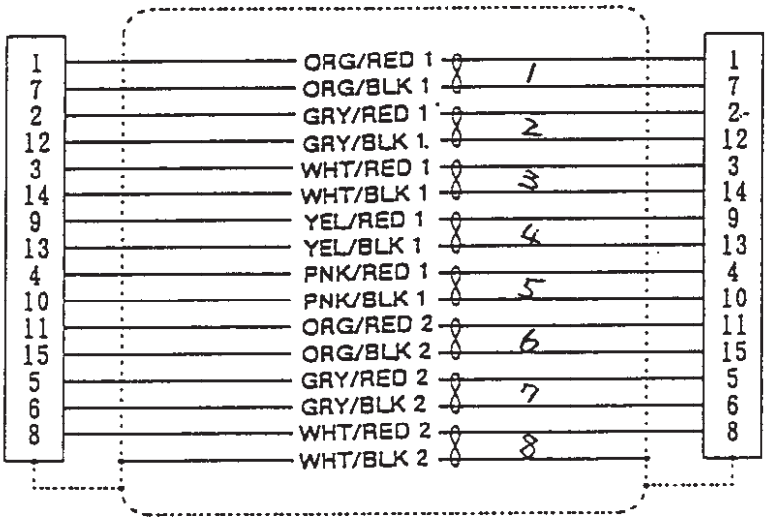


2 pcs.	1315 2908-	Connector Plug, 25 pin D-Sub (Male)
2 pcs.	5336 3581-00	Case Assy, 25 pin D-Sub

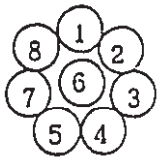
THE CABLES FOR METER



Female Male

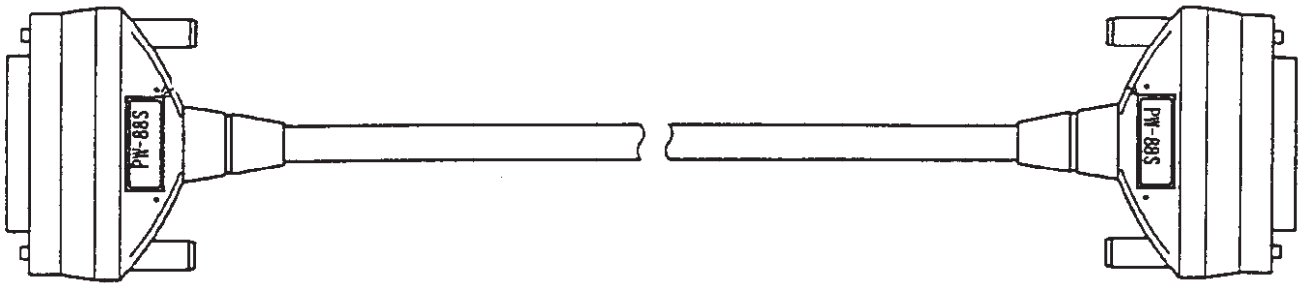


means Twisted wire

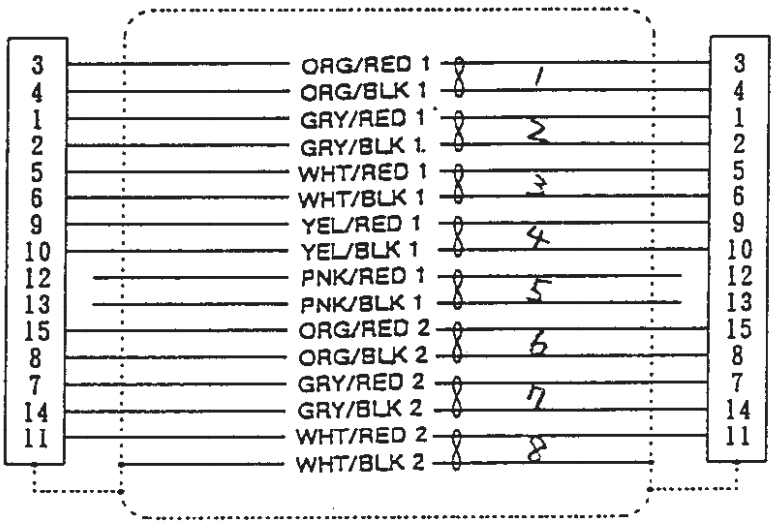


1 pce.	5336 3570-00	Connector Plug, 15 pin D-Sub (Male)
1 pce.	1315 2907-	Connector Socket, 15 pin D-Sub (Female)
2 pcs.	5336 3580-00	Case Assy, 15 pin D-Sub

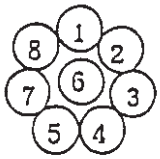
THE CABLES FOR SYNC



Male Male

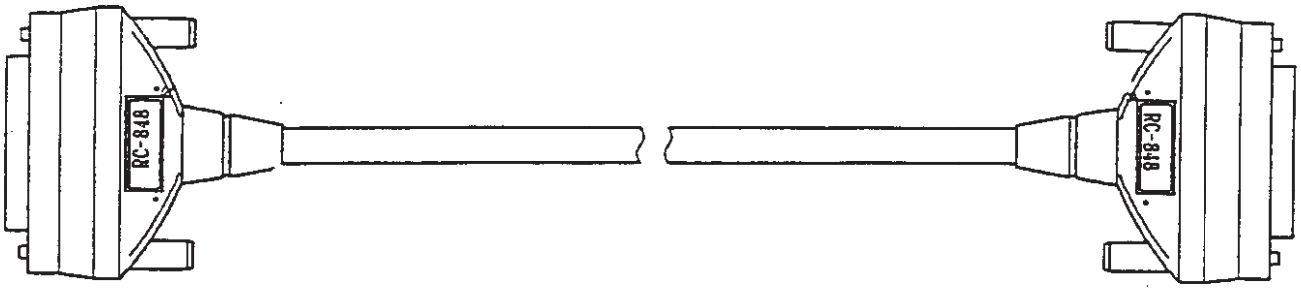


means Twisted wire



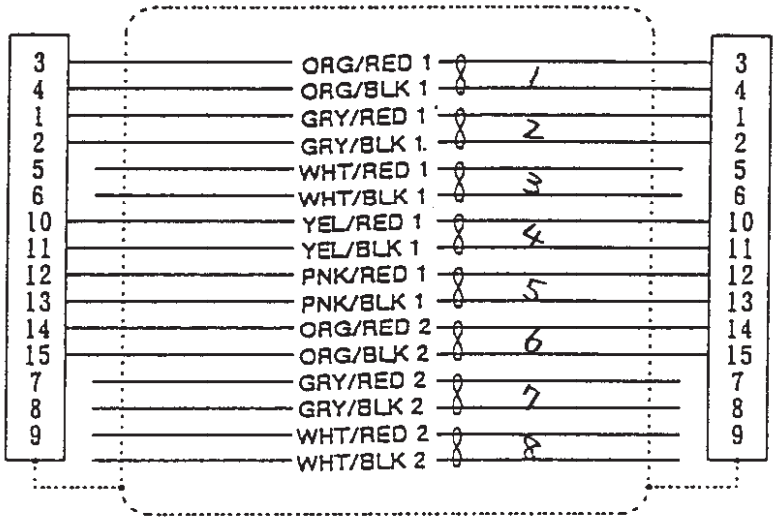
2 pcs.	5336 3570-00	Connector Plug, 15 pin D-Sub (Male)
2 pcs.	5336 3580-00	Case Assy, 15 pin D-Sub

THE CABLES FOR REMOTE

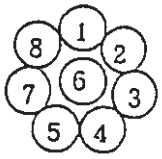


Female

Male



means Twisted wire



1 pce.	5336 3570-00	Connector Plug, 15 pin D-Sub (Male)
1 pce.	1315 2907-	Connector Socket, 15 pin D-Sub (Female)
2 pcs.	5336 3580-00	Case Assy, 15 pin D-Sub

NIPPON PRECISION CIRCUITS INC.

SM5843A×1

Audio Multi-function Digital Filter

OVERVIEW

The SM5843A×1 is a multi-function digital filter IC, fabricated using NPC's Molybdenum-gate CMOS process, for digital audio reproduction equipment. It features 8-times oversampling (interpolation), digital deemphasis and soft muting functions. It accepts 16, 18, or 20-bit input data, and outputs data in 18 or 20-bit format. It operates using either a 384fs or 256fs system clock.

FEATURES

- Filter configuration (2-channel processing)
  - 8-times oversampling (interpolation)
    - 3-stage FIR configuration
  - Deemphasis filter
    - IIR filter configuration for correct gain and phase characteristics
    - 2-channel independent ON/OFF control
    - 32/44.1/48 kHz sampling frequency (fs)
  - 21 × 22-bit parallel multiplier/25-bit accumulator for high precision
  - Overflow limiter
- 2 oversampling filter characteristics
  - Sharp roll-off characteristic (response 1)
    - ≤ ±0.00005 dB passband ripple (0 to 0.4535fs)
    - ≥ 110 dB stopband attenuation (0.5465fs to 7.4535fs)
  - Slow roll-off characteristic (response 2)
    - ≤ ±0.00003 dB passband ripple (0 to 0.235fs)
    - ≥ 77 dB stopband attenuation (0.745fs to 7.255fs)
- Soft muting
- Digital attenuator
- Input data format
  - 2s complement, MSB first
    - LR alternating, 16/18/20-bit serial, trailing data
    - LR alternating, 20-bit serial, leading data
    - LR simultaneous, 20-bit serial, leading data
- Output data format
  - 2s complement, MSB first, LR simultaneous
  - 18/20-bit serial
  - BCKO burst (NPC format)
- Dither processing ON/OFF control
- Jitter-free/Sync mode selectable
- 256fs/384fs system clock selectable
  - 21.2/14.2MHz maximum frequency (384fs/256fs)
- 5 V supply
- Crystal oscillator circuit built-in
- TTL-compatible input/outputs
- 28-pin plastic DIP and SOP
- Molybdenum-gate CMOS

APPLICATIONS

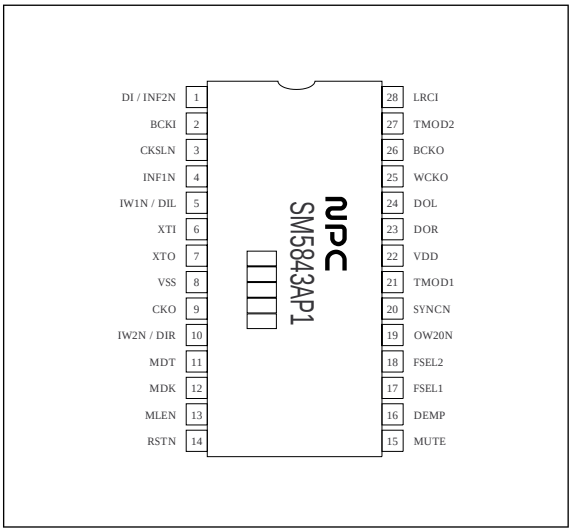
- CD players
- DAT players
- PCM systems

ORDERING INFOMATION

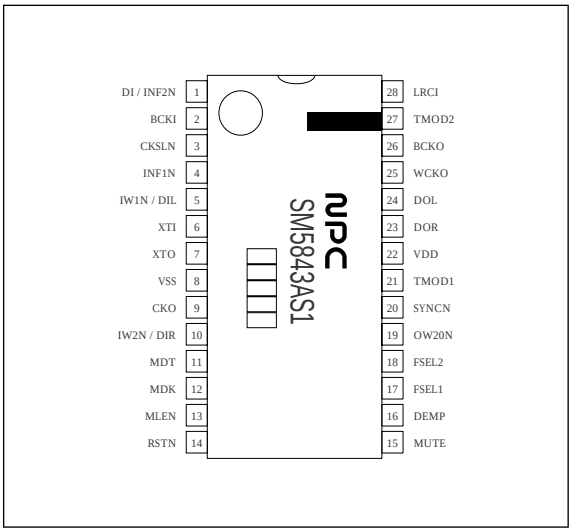
Device	Package
SM5843AP1	28pin DIP
SM5843AS1	28pin SOP

PINOUT(TOP VIEW)

28-pin DIP

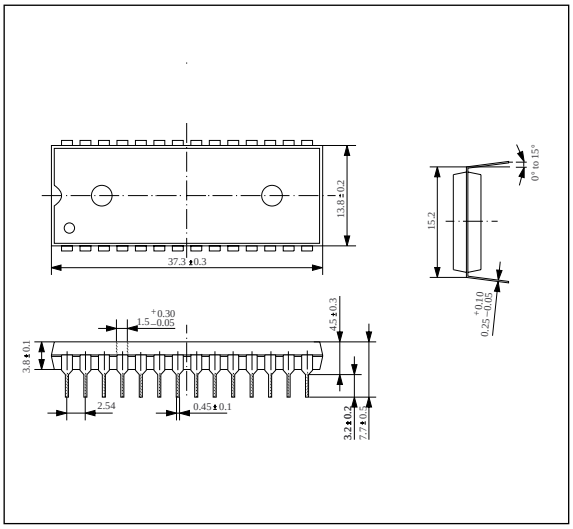


28-pin SOP

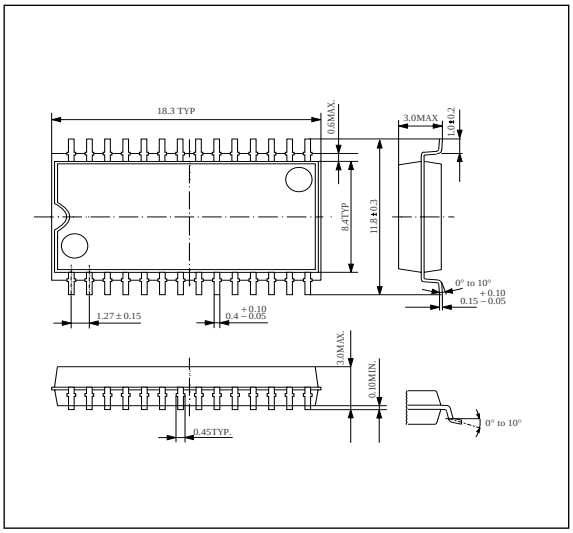


PACKAGE DIMENSIONS(Unit: mm)

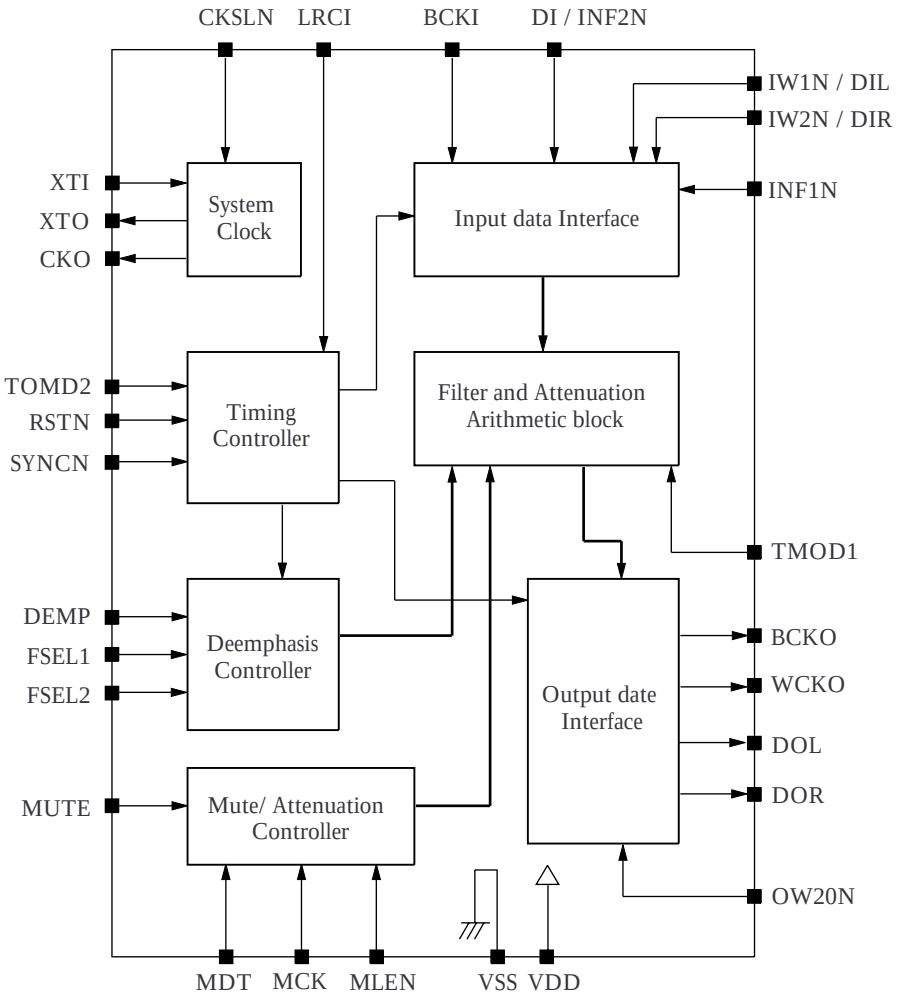
28-pin DIP



28-pin SOP



BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Number</th><th>Name</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>1</td><td>DI/INF2N</td><td>Ip</td><td>Data input when INF1N is LOW, and input format select pin when INF1N is HIGH.</td></tr>
<tr><td>2</td><td>BCKI</td><td>Ip</td><td>Input bit clock</td></tr>
<tr><td>3</td><td>CKSLN</td><td>Ip</td><td>Oscillator and system clock select input. 384fs when HIGH, and 256fs when LOW.</td></tr>
<tr><td>4</td><td>INF1N</td><td>Ip</td><td>Input format select pin. INF1N and INF2N select the pin functions below.
<table>
<tr><th rowspan="2">INF1N</th><th rowspan="2">DI/INF2N</th><th rowspan="2">Input format</th><th colspan="3">Pin function selection</th></tr>
<tr><th>DI/INF2N</th><th>IW1N/DIL</th><th>IW2N/DIR</th></tr>
<tr><td>LOW</td><td>LOW</td><td rowspan="2">LR alternating, trailing data</td><td rowspan="2">DI</td><td rowspan="2">IW1N</td><td rowspan="2">IW2N</td></tr>
<tr><td>LOW</td><td>HIGH</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>LR alternating, leading data</td><td rowspan="2">INF2N</td><td rowspan="2">DIL</td><td rowspan="2">DIR</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>LR simultaneous, leading data</td></tr>
</table></td></tr>
<tr><td>5</td><td>IW1N/DIL</td><td>Ip</td><td>Input bit length select pin when INF1N is LOW, and left-channel data input when INF1N is HIGH. IW1N and IW2N select the input data length.
<table>
<tr><th>INF1N</th><th>IW2N/DIL</th><th>IW1N/DIR</th><th>Input bit length</th></tr>
<tr><td rowspan="4">LOW</td><td>LOW</td><td>LOW</td><td>20 bits</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>20 bits</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>18 bits</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>16 bits</td></tr>
<tr><td>HIGH</td><td>×</td><td>×</td><td>20 bits</td></tr>
</table></td></tr>
<tr><td>6</td><td>XTI</td><td>I</td><td>Oscillator input connection</td></tr>
<tr><td>7</td><td>XTO</td><td>O</td><td>Oscillator output connection</td></tr>
<tr><td>8</td><td>VSS</td><td>–</td><td>Ground</td></tr>
<tr><td>9</td><td>CKO</td><td>O</td><td>Oscillator output clock. Same frequency as XTI.</td></tr>
<tr><td>10</td><td>IW2N/DIR</td><td>Ip</td><td>Input bit length select pin when INF2N is LOW, and right-channel data input when INF2N is HIGH. IW1N and IW2N select the input data length as shown in the table for pin 5.</td></tr>
<tr><td>11</td><td>MDT</td><td>Ip</td><td>Attenuator serial data input</td></tr>
<tr><td>12</td><td>MCK</td><td>Ip</td><td>Attenuator bit clock input</td></tr>
<tr><td>13</td><td>MLEN</td><td>Ip</td><td>Attenuator latch enable input</td></tr>
<tr><td>14</td><td>RSTN</td><td>Ip</td><td>System reset. Reset operation when LOW, and normal operation when HIGH.</td></tr>
<tr><td>15</td><td>MUTE</td><td>Ip</td><td>Mute control signal. Muting when HIGH, and normal operation when LOW.</td></tr>
<tr><td>16</td><td>DEMP</td><td>Ip</td><td>Deemphasis control signal. OFF when LOW, and ON when HIGH.</td></tr>
<tr><td>17</td><td>FSEL1</td><td>Ip</td><td rowspan="2">Deemphasis filter select inputs
<table>
<tr><th>FSEL1</th><th>FSEL2</th><th>Sampling frequency (fs)</th></tr>
<tr><td>LOW</td><td>LOW</td><td>44.1 kHz</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>48 kHz</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>Test mode</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>32 kHz</td></tr>
</table></td></tr>
<tr><td>18</td><td>FSEL2</td><td>Ip</td></tr>
<tr><td>19</td><td>OW20N</td><td>Ip</td><td>Output bit length select pin. 20-bit output when LOW, and 18-bit output when HIGH.</td></tr>
<tr><td>20</td><td>SYNCN</td><td>Ip</td><td>Sync mode select pin. Normal sync mode when LOW, and jitter-free mode when HIGH.</td></tr>
<tr><td>21</td><td>TMOD1</td><td>Ip</td><td>Dither processing control. ON when LOW, and OFF when HIGH.</td></tr>
<tr><td>22</td><td>VDD</td><td>–</td><td>5 V supply</td></tr>
</table>

Number	Name	I/O[1]	Description
23	DOR	O	Right-channel data output
24	DOL	O	Left-channel data output
25	WCKO	O	Output word clock
26	BCKO	O	Output bit clock
27	TMOD2	Ip	Filter characteristic select pin. Sharp roll-off (response 1) when HIGH, and slow roll-off (response 2) when LOW.
28	LRCI	Ip	Input data sample rate (fs) clock

1. I = input, Ip = Input with pull-up resistor, O = output

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	550 (DIP)	mW
		390 (SOP)	
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

fs = 384fs (CKSLN = HIGH): V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.5 to 5.5	V
Operating temperature range	T_{opr}	–20 to 80	°C

fs = 256fs (CKSLN = LOW): V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.75 to 5.25	V
Operating temperature range	T_{opr}	–20 to 70	°C

DC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 5.0 V[1]	–	50	65	mA
XTI HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
XTI AC-coupled input voltage	V_{INAC}		0.3V_{DD}	–	–	V_{p-p}
HIGH-level input voltage[2]	V_{IH2}		2.4	–	–	V
LOW-level input voltage[2]	V_{IL2}		–	–	0.5	V
HIGH-level output voltage[3]	V_{OH}	I_{OH} = –0.4 mA	2.5	–	–	V
LOW-level output voltage[3]	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH}	V_{IN} = V_{DD}	–	10	20	µA
XTI LOW-level input current	I_{IL1}	V_{IN} = 0 V	–	10	20	µA
LOW-level input current[2]	I_{IL2}	V_{IN} = 0 V	–	10	20	µA
Input leakage current[2]	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA

1. f_{SYS} = 256fs = 14.2 MHz (CKSLN = LOW), no output load
2. Pins DI/INF2N, BCKI, CKSLN, INF1N, IW1N/DIL, IW2N/DIR, MDT, MCK, MLEN, RSTN, MUTE, DEMP, FSEL1, FSEL2, OW20N, SYNCN, LRCI, TMOD1, TMOD2
3. Pins CKO, DOL, DOR, BCKO, WCKO

AC Electrical Characteristics

Input Clock (XTI)

Crystal oscillator

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	2.0	–	21.2	MHz

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	1.0	–	14.2	MHz

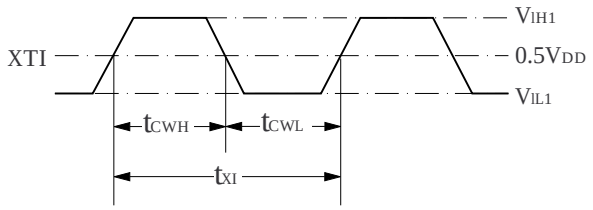
External clock input

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	20	–	250	ns
Clock LOW-level pulsewidth	t_{CWL}	20	–	250	ns
Clock pulse cycle time	t_{XI}	47	–	500	ns

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 70 °C

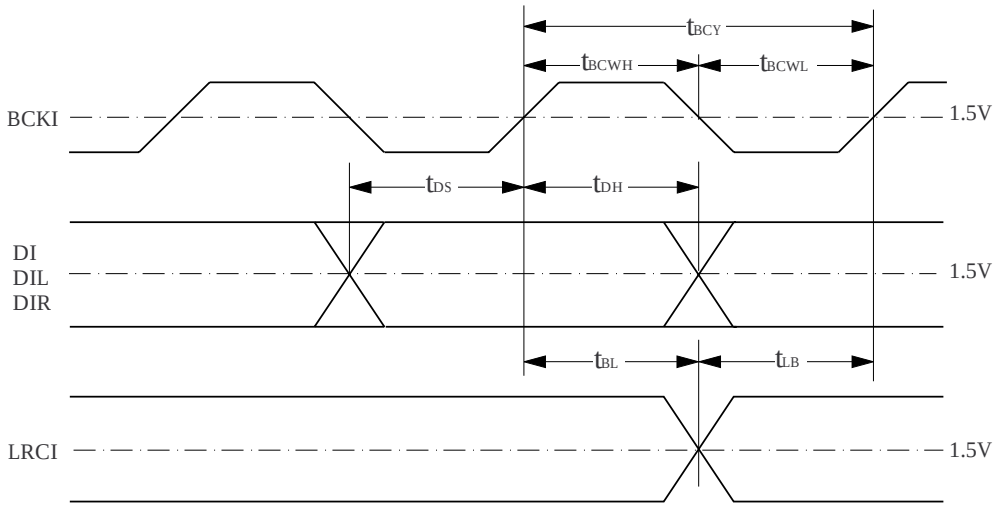
Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	30	–	500	ns
Clock LOW-level pulsewidth	t_{CWL}	30	–	500	ns
Clock pulse cycle time	t_{XI}	70	–	1000	ns



Serial input timing (BCKI, DI, DIL, DIR, LRCI)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI pulse cycle	t_{BCY}	100	–	–	ns
DIN setup time	t_{DS}	50	–	–	ns
DIN hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns



Reset timing (RSTN)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

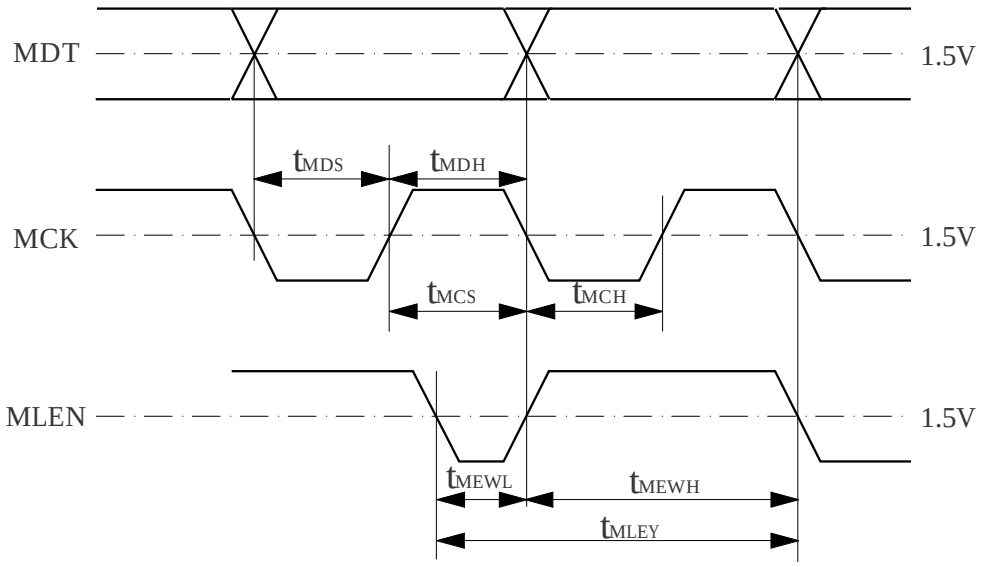
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{RST}$ LOW-level reset pulsewidth	t_{RST}	At power-ON	1	–	–	µs
		At all other times	50	–	–	ns

Attenuator timing (MDT, MCK, MLEN)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
MDT setup time	t_{MDS}	20	–	–	ns
MDT hold time	t_{MDH}	20	–	–	ns
MLEN setup time	t_{MCS}	40	–	–	ns
MLEN hold time	t_{MCH}	20	–	–	ns
MLEN LOW-level pulsewidth	t_{MEWL}	20	–	–	ns
MLEN HIGH-level pulsewidth	t_{MEWH}	20	–	–	ns
MLEN pulse cycle time	t_{MLEY}	6	–	–	t_{SYS}[1]

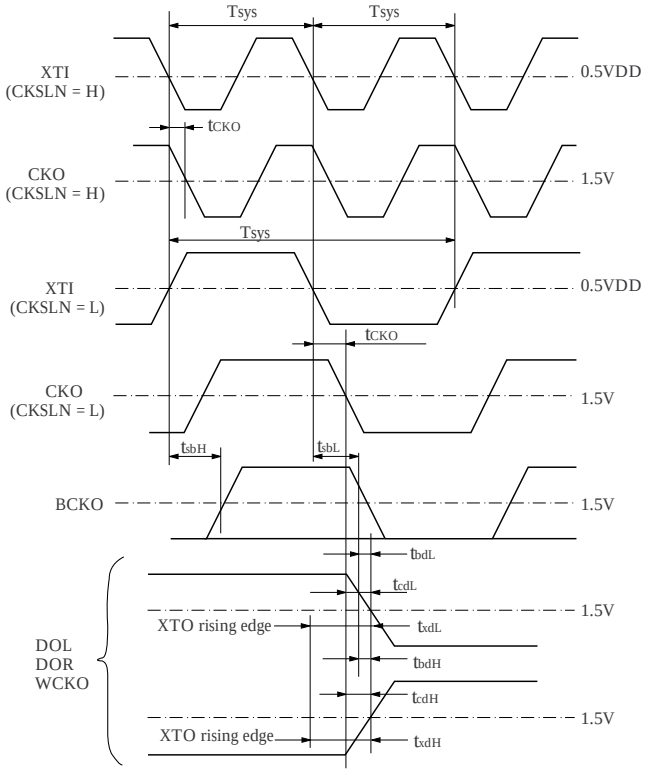
1. t_{SYS} = 1/384fs when CKSLN is HIGH, and 1/256fs when CKSLN is LOW.



Output timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C, C_L = 15 pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI to XTO delay	t_{XTO}	XTI fall to XTO rise	3	–	15	ns
XTI to CKO delay	t_{CKO}	XTI fall to CKO fall	10	–	35	ns
XTI to BCKO delay (CKSLN = HIGH)	t_{sbH}	XTI fall to BCKO rise	20	–	60	ns
	t_{sbL}	XTI fall to BCKO fall	20	–	60	
XTI to BCKO delay (CKSLN = LOW)	t_{sbH}	XTI fall to BCKO rise	20	–	60	ns
	t_{sbL}	XTI fall to BCKO fall	20	–	60	
BCKO to DOL, DOR, WCKO delay	t_{bdH}	BCKO fall to output rise	–5	–	10	ns
	t_{bdL}	BCKO fall to output fall	–5	–	10	
CKO TODOL, DOR, WCKO delay	t_{cdH}	CKO fall to output rise	5	–	25	ns
	t_{cdL}	CKO fall to output fall	5	–	25	
XTO TODOL, DOR, WCKO delay	t_{xdH}	XTO rise to output rise	15	–	50	ns
	t_{xdL}	XTO rise to output fall	15	–	50	



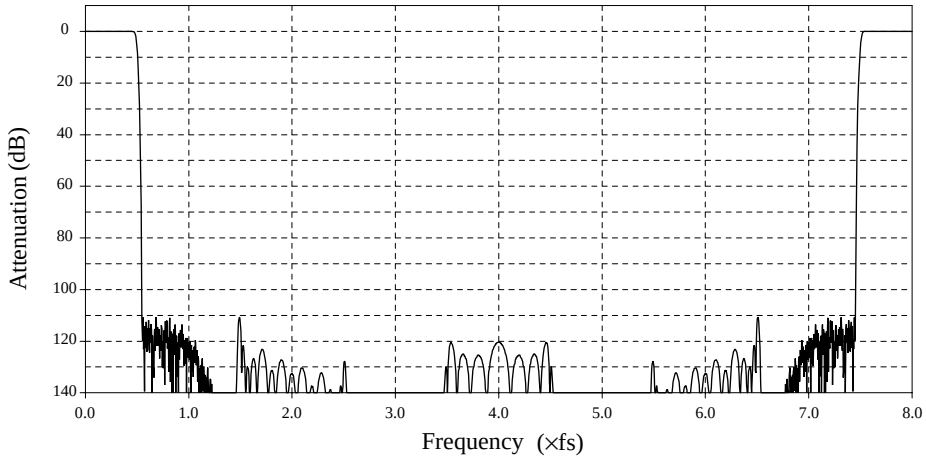
Filter Characteristics

8-times interpolation filter (sharp roll-off: response 1)

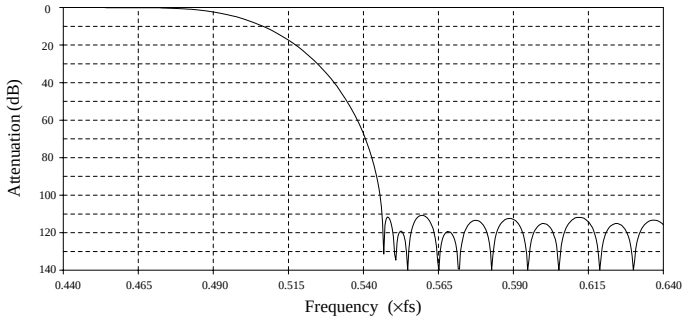
Parameter	Condition	Rating @ 256fs
Passband		0 to 0.4535fs
Stopband		0.5465fs to 7.4535fs
Passband ripple		≤ ±0.00005 dB
Stopband attenuation		≥ 110 dB
Group delay[1]	SYNCN = LOW	44.625/fs
	SYNCN = HIGH	44.25/fs to 45.0/fs

1. The digital filter arithmetic computation time from when the completion of data input at rate fs to the start of data output at rate 8fs.

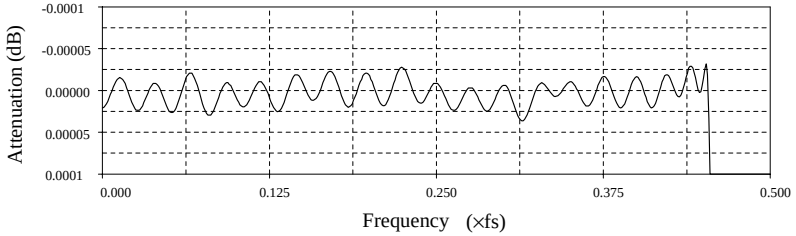
8fs filter response with deemphasis OFF



8fs filter band transition response with deemphasis OFF



8fs filter passband response with deemphasis OFF

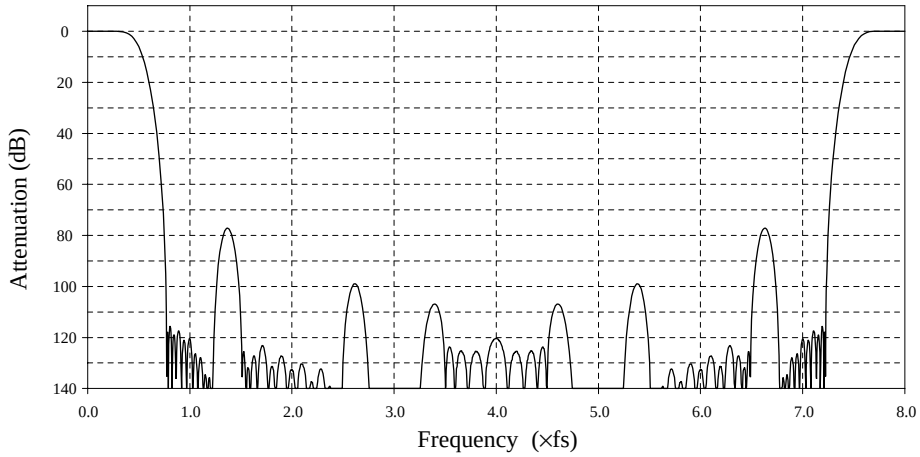


8-times interpolation filter (slow roll-off: response 2)

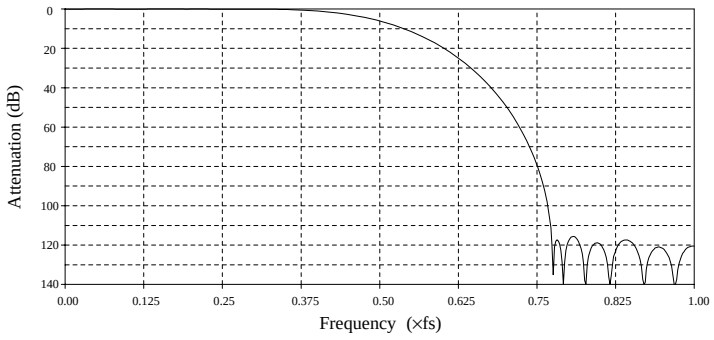
Parameter	Condition	Rating @ 256fs
Passband	< 3 dB attenuation	0 to 0.455fs
Stopband	> 77 dB attenuation	0.745fs to 7.255fs
Passband ripple	0 to 0.235fs	≤ ±0.00003 dB
Stopband attenuation		≥ 77 dB
Group delay[1]	SYNCN = LOW	25.625/fs
	SYNCN = HIGH	25.25/fs to 26.0/fs

1. The digital filter arithmetic computation time from when the completion of data input at rate fs to the start of data output at rate 8fs.

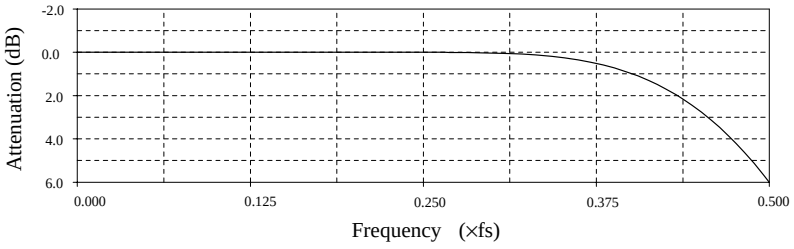
8fs filter response with deemphasis OFF



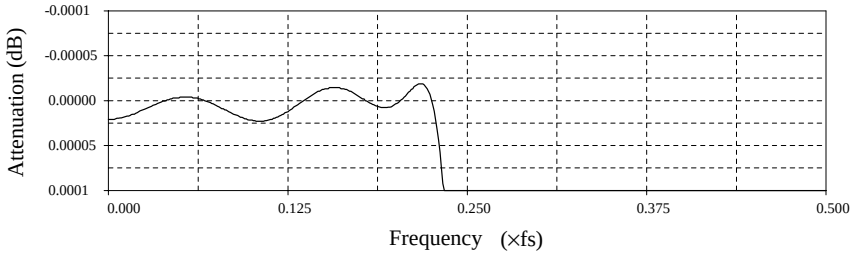
8fs filter band transition response with deemphasis OFF



8fs filter passband response with deemphasis OFF



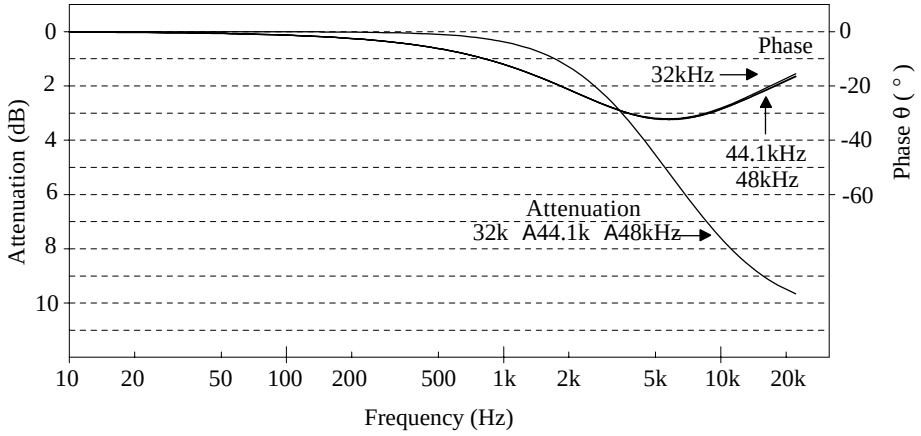
8fs filter passband response [amplitude gain enlarged]



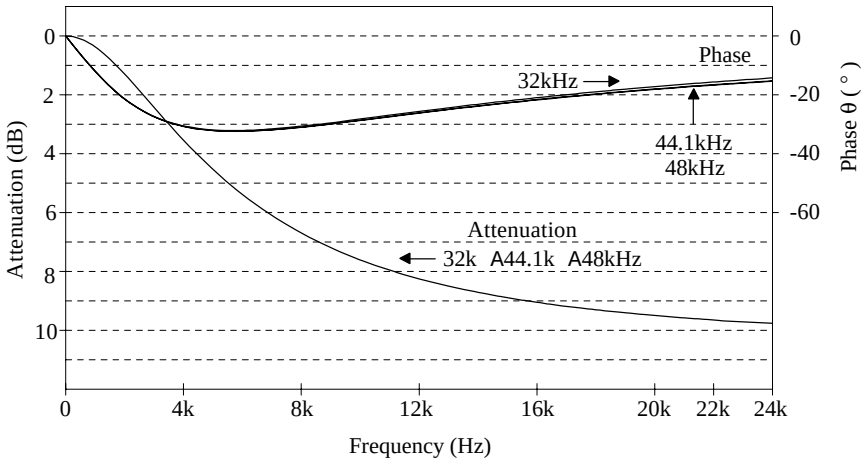
Deemphasis filter

Parameter		Sampling frequency (fs)		
		32 kHz	44.1 kHz	48 kHz
Passband bandwidth (kHz)		0 to 14.5	0 to 20.0	0 to 21.7
Deviation from ideal characteristic	Attenuation	≤ ±0.001 dB		
	Phase, θ	0 to 1.5°		

Passband response with deemphasis ON (logarithmic frequency axis)



Passband response with deemphasis ON (linear frequency axis)



FUNCTIONAL DESCRIPTION

The basic arithmetic block is shown in figure 1, and the function of each block is described in the following sections.

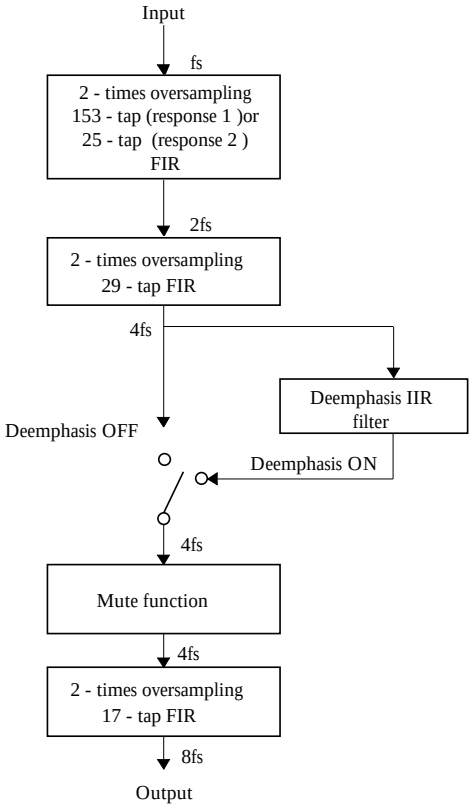


Figure 1. Arithmetic block diagram

8-times Oversampling (Interpolation)

The interpolation arithmetic block is comprised of 3 cascaded, 2-times FIR interpolation filters, as shown in figure 1.

The input signal is sampled at rate fs, and then 8-times oversampling data is output. Sampling noise in the 0.5465fs to 7.4535fs stopband for the sharp roll-off (response 1) characteristic, 0.745fs to 7.255fs for the slow roll-off (response 2) characteristic, is removed by the interpolation filter.

Digital Deemphasis

The digital deemphasis filter has the same construction as analog filters. It is implemented as an IIR filter to faithfully reproduce the gain and phase characteristics of standard analog deemphasis filters. The three sets of filter coefficients for the three fs = 32.0/44.1/48.0 kHz sampling frequencies are selected by FSEL1 and FSEL2 when the sampling frequency is specified, as shown in the following table. Deemphasis is ON when DEMP is HIGH, and OFF when DEMP is LOW.

FSEL1	FSEL2	Sampling frequency (fs)
LOW	LOW	44.1 kHz
LOW	HIGH	48 kHz
HIGH	LOW	Test mode
HIGH	HIGH	32 kHz

Note that test mode is not available for operation.

Soft Muting

The muting function controls the muting of both left and right channels simultaneously. Muting is ON when MUTE is HIGH, muting is OFF when MUTE is LOW.

When MUTE goes HIGH, the attenuation changes smoothly from 0 to −∞ dB in 512/fs, or approximately 11.6 ms when fs = 44.1 kHz. When MUTE goes LOW, muting is released and the attenuation changes smoothly from −∞ to 0 dB, again taking approximately 11.6 ms.

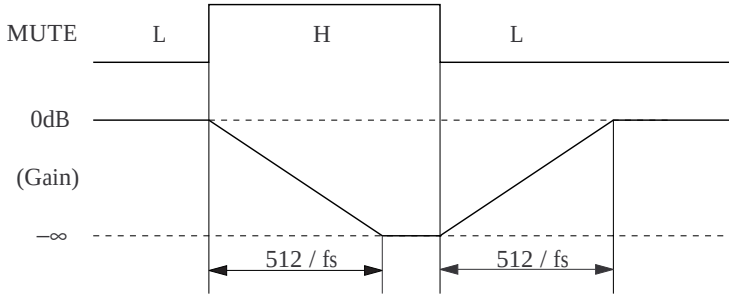


Figure 2. Mute timing

When RSTN goes LOW, the DOL and DOR outputs go LOW, immediately muting the output signal. Muting is released and timing is synchronized immediately after RSTN goes HIGH.

Digital Attenuator (MDT, MCK, MLEN)

The attenuation function is controlled by MDT, MCK and MLEN. MDT data, in 11-bit serial MSB first format, is shifted into an internal shift register on the rising edge of the serial data clock MCK. The contents of the shift register are transferred to the internal processing circuits on the rising edge of the MLEN gate pulse. The attenuation data format is shown in figure 3.

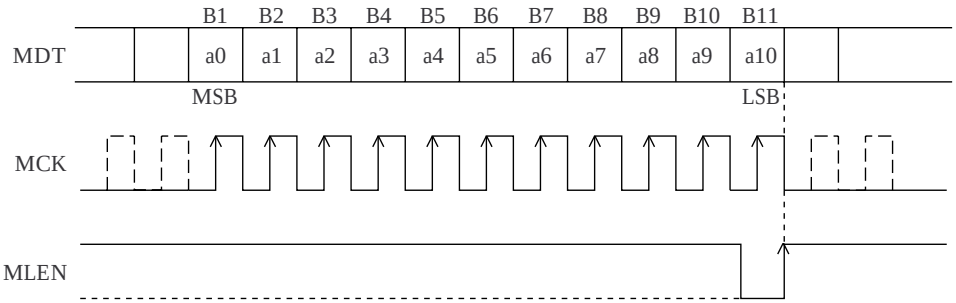


Figure 3. Attenuation data format

The attenuation register data DATT can take on any value between 0 and 1024 (400_H). The attenuation is given by the following equation for both left and right channels simultaneously.

Attenuation = $20 \times \log_{10}(DATT/1024)$ [dB]

Thus, the attenuation level is −∞ when DATT is 0, and attenuation is 0 dB when DATT is 1024. DATT is set to 1024 (400_H) after system reset initialization. The attenuation data and attenuation level for sample DATT values are shown in the following table.

Attenuation data DATT	Attenuation level (dB)
000_H	−∞
001_H to $3FF_H$	−60.206 to −0.0085
400_H	0

Attenuation operation

When an attenuation value DATT is set, the attenuation changes smoothly from the current attenuation level to the new level. The new attenuation data is stored in the attenuation register while the current attenuation data is stored in a temporary register. The attenuation then changes smoothly by ramping between the two register values, updating the temporary register with each step. If a new attenuation value for DATT is set before the previous target attenuation level is reached, the attenuation then ramps toward the new attenuation level.

When MUTE is HIGH, the attenuation level is −∞. When MUTE goes LOW (muting OFF), the attenuation level returns to that of the original value of DATT.

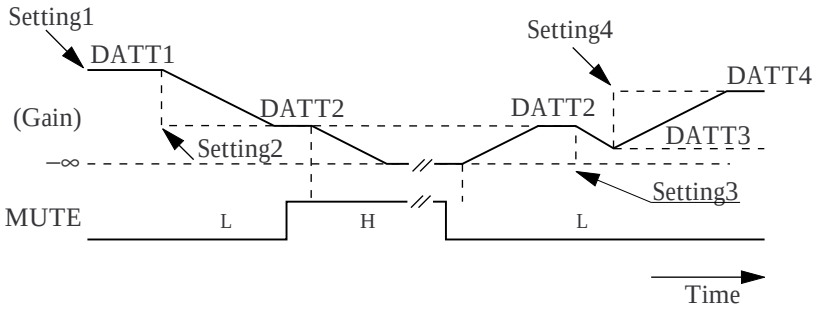


Figure 4. Attenuation and mute timing

System Clock (XTI, XTO, CKO, CKSLN)

Two system clock frequencies, 384fs and 256fs, can be used. An external clock source can be input on XTI, or a crystal oscillator can be constructed by connecting a crystal between XTI and XTO. The system clock is also buffered and then output on CKO. The system clock frequency selection and the internal clock frequency are shown in the following table.

Parameter	CKSL	
	HIGH	LOW
XTI input clock frequency ($f_{XI} = 1/t_{XI}$)	384fs	256fs
CKO clock frequency	384fs	256fs
Internal clock frequency (t_{SYS})	$2 \times t_{XI}$	t_{XI}

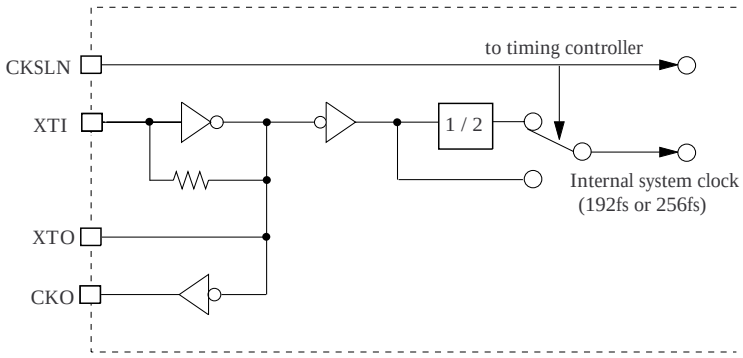


Figure 5. Clock generator circuit

Audio Data Input (INF1N, INF2N, IW1N, IW2N, DI, DIL, DIR, BCKI, LRCI)

The input data format and several input pin functions are selected by the state of INF1N and INF2N.

INF1N	DI/INF2N	Input format	Pin function selection		
			DI/INF2N	IW1N/DIL	IW2N/DIR
LOW	LOW	LR alternating[1], trailing data	DI	IW1N	IW2N
LOW	HIGH				
HIGH	LOW	LR alternating, leading data	INF2N	DIL	DIR
HIGH	HIGH	LR simultaneous[2], leading data			

1. Alternating left-channel and right-channel data input on a single input DI.
2. Simultaneous left-channel and right-channel data input on two inputs, DIL and DIR, respectively.

The input data word length is selected by the state of IW1N and IW2N when INF1N is LOW. 20-bit is selected when INF1N is HIGH.

INF1N	IW2N/DIL	IW1N/DIR	Input bit length
LOW	LOW	LOW	20 bits
	LOW	HIGH	20 bits
	HIGH	LOW	18 bits
	HIGH	HIGH	16 bits
HIGH	×	×	20 bits

Jitter-free Function (SYNCN)

The arithmetic circuit and output control timing is derived from the system clock, and is therefore independent of the input LRCI and BCKI clocks. Accordingly, any jitter in the data input clock (LRCI and BCKI) does not cause jitter in the output.

Generally, the internal timing is synchronized to the LRCI input timing after a system reset release, when RSTN goes from LOW to HIGH, on the first LRCI clock start edge. If the input timing and LRCI start edge timing subsequently drift, the input timing is automatically resynchronized when the timing error exceeds a certain value. There are 2 timing error values at which resynchronization occurs, selected by the state of SYNCN.

Jitter-free mode (SYNCN = HIGH)

When SYNCN is HIGH, the timing error value is ±3/8 × (LRCI clock period). When the difference between the input timing and LRCI start edge position do not exceed this value, internal timing is not resynchronized and all functions continue to operate normally.

Sync mode (SYNCN = LOW)

When SYNCN is LOW, the timing error value is ±1 × (system clock period), which is a much smaller timing error tolerance than in jitter-free mode. In this mode, the internal timing is guaranteed to follow the LRCI clock timing within this tolerance, making this mode useful for systems constructed from a multiple number of SM5843A×1 devices.

Note that resynchronization affects the internal operation and can generate a momentary click noise output.

Audio Data Output (DOL, DOR, BCKO, WCKO, OW20N)

The output data is in serial, simultaneous left and right-channel, 2s complement, MSB first, BCKO burst (NPC format) format. The output data word length is selected by the state of OW20N. 18-bit output is selected when OW20N is HIGH, and 20-bit output when OW20N is LOW.

8fs serial data is output in sync with the falling edge of the internal system clock and BCKO clock. The number of BCKO bit clock pulses per word changes depending on the output bit length selected (18/20 bits). Consequently, output data is latched into the internal output register on the falling of the edge of an output word clock WCKO, which has timing independent of the number of output bits as specified in the following table.

Parameter	Symbol	CKSLN = HIGH	CKSLN = LOW
Bit clock rate	T_B	1/192fs	1/256fs
Data word length	T_{DW}	$24t_{SYS}$	$32t_{SYS}$

System Reset (RSTN)

The SM5843A×1 must be reset under the following conditions.

- At power-ON.
- When the LRCI clock and internal operation timing need to be resynchronized.
- When switching the CKSLN clock select input.
- When switching between filter characteristics using TMOD2.
- When either or both of the LRCI and XTI clocks stop or are interrupted.

The system is reset by applying a LOW-level pulse on RSTN.

The arithmetic and output timing counters are reset on the first LRCI start edge after reset is released, as long as the XTI clock has already stabilized. The LRCI start edge is determined by the state of INF1N and INF2N. When INF1N is LOW or when both INF1N and INF2N are HIGH, the start edge is the rising edge. When INF1N is HIGH and INF2N is LOW, the start edge is the falling edge.

When RSTN is LOW, the DOL and DOR outputs are LOW, muting the output signal to an attenuation level of −∞.

The power-ON reset pulse can be applied by a microcontroller or, for systems where XTI and LRCI are stable at power-ON, by connecting a capacitor of several hundred pF between RSTN and VSS. For systems that do not use a microcontroller, the capacitor must be chosen such that the XTI and LRCI clocks fully stabilize before RSTN goes from LOW to HIGH.

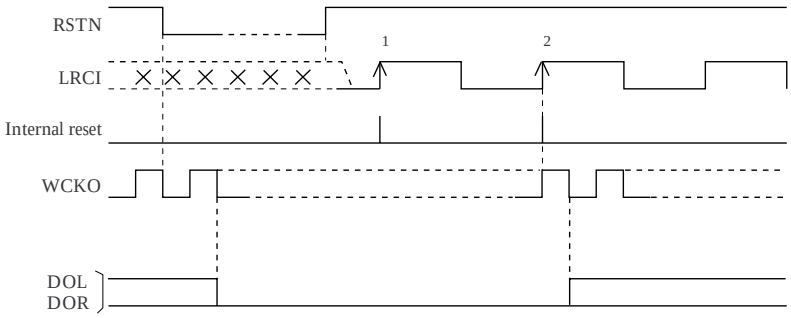


Figure 6. System reset timing and output muting

Filter Characteristic Selection (TMOD2)

There are 2 digital filter frequency response characteristics incorporated into the SM5843A×1, selected by the state of TMOD2. A sharp roll-off characteristic (response 1) is selected when TMOD2 is HIGH, and a slow roll-off characteristic (response 2) when TMOD2 is LOW. The response is modified by changing the number of taps in the 1st FIR filter stage, as shown in figure 1.

- Filter response 1
  - 153-tap 1st FIR
  - 29-tap 2nd FIR
  - 17-tap 3rd FIR
- Filter response 2
  - 25-tap 1st FIR
  - 29-tap 2nd FIR
  - 17-tap 3rd FIR

Note that the device should be reset when changing TMOD2 during normal operation.

Dither Rounding-off Processing (TMOD1)

Dither rounding-off processing of output data is ON when TMOD1 is LOW. Dither is OFF and normal processing mode is selected when TMOD1 is HIGH.

TIMING DIAGRAMS

Input Timing Examples (DIN, BCKI, LRCI)

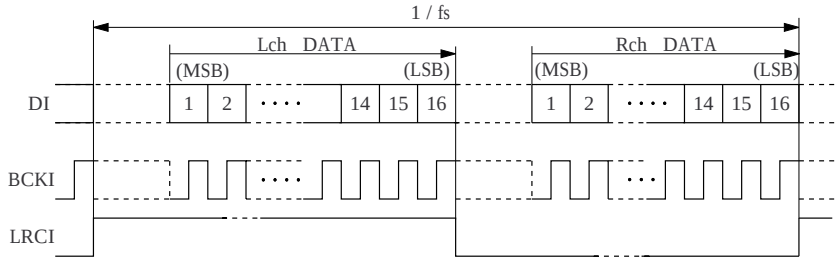
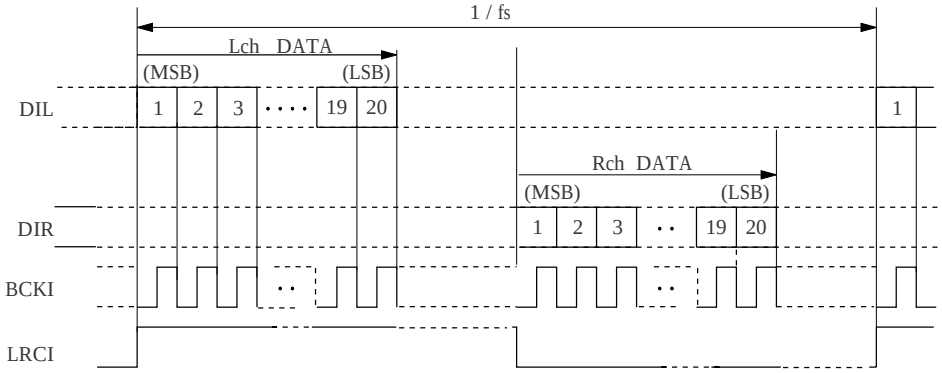
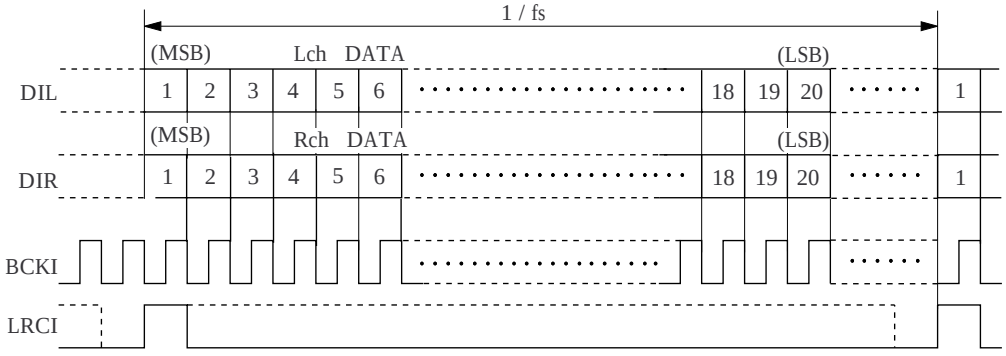


Figure 7. LR alternating, trailing data, 16-bit input



Data after lsb (bit 20) is ignored. After bit 20, BCKI clock input is not needed.

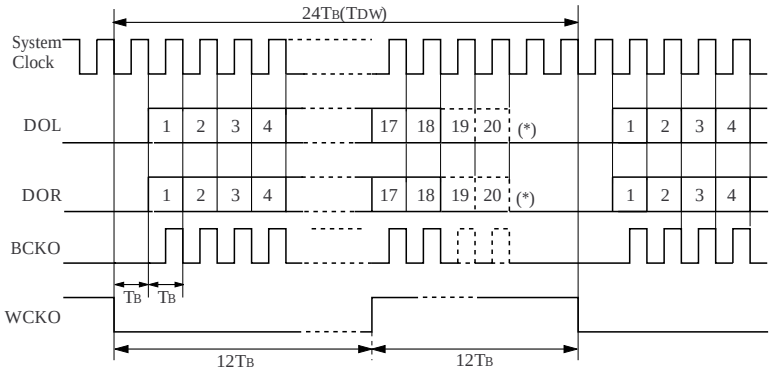
Figure 8. LR alternating, leading data, 20-bit input



Data after lsb (bit20) is ignored. After bit 20, BCKI clock input is not needed.

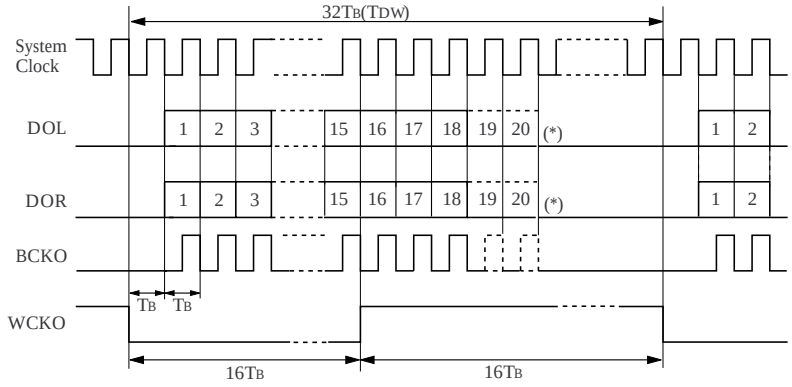
Figure 9. LR simultaneous, leading data, 20-bit input

Output Timing Examples (DOL, DOR, BCKO, WCKO)



The number of output bits is determined by the output bit length selected.

Figure 10. 18/20-bit output ($\overline{CKSL}$ = HIGH)



The number of output bits is determined by the output bit length selected.

Figure 11. 18/20-bit output ($\overline{CKSL}$ = LOW)

Data Input to Output Delay Timing

This is the digital filter arithmetic computation time from the completion of data input at rate fs (t_{INPUT}) on the rising edge of LRCI to the start of data output at rate 8fs (t_{OUTPUT}) on the falling edge of WCKO.

Filter response	CKSLN	SYNCN	Mode	$t_{OUTPUT} - t_{INPUT}$
Filter response 1	LOW (256fs)	LOW	After reset + sync mode	44.625/fs
		HIGH	Jitter-free mode	44.25/fs – 45.0/fs
	HIGH (384fs)	LOW	After reset + sync mode	44.75/fs
		HIGH	Jitter-free mode	44.375/fs – 45.125/fs
Filter response 2	LOW (256fs)	LOW	After reset + sync mode	25.625/fs
		HIGH	Jitter-free mode	25.25/fs – 26.0/fs
	HIGH (384fs)	LOW	After reset + sync mode	25.75/fs
		HIGH	Jitter-free mode	25.375/fs – 26.125/fs

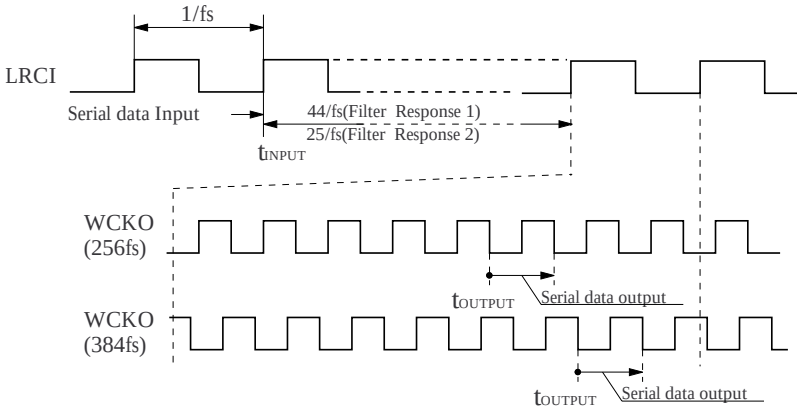


Figure 12. Delay timing (SYNCN = LOW)

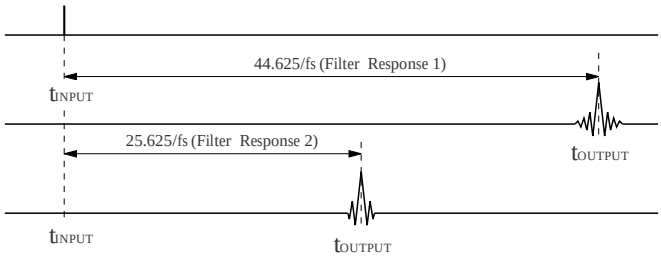
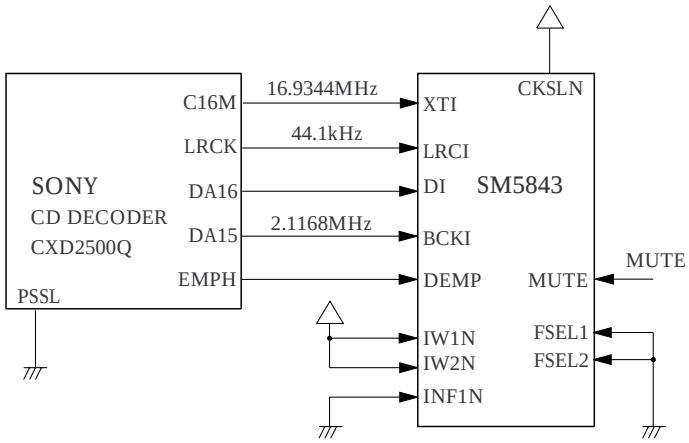


Figure 13. Delay timing (SYNCN = CKSLN = LOW)

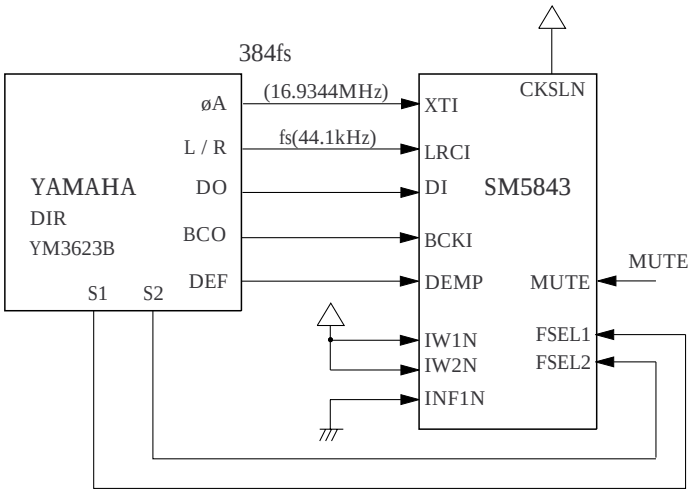
APPLICATION CIRCUITS

Input Interface Circuits

CD decoder (CXD2500Q) connection

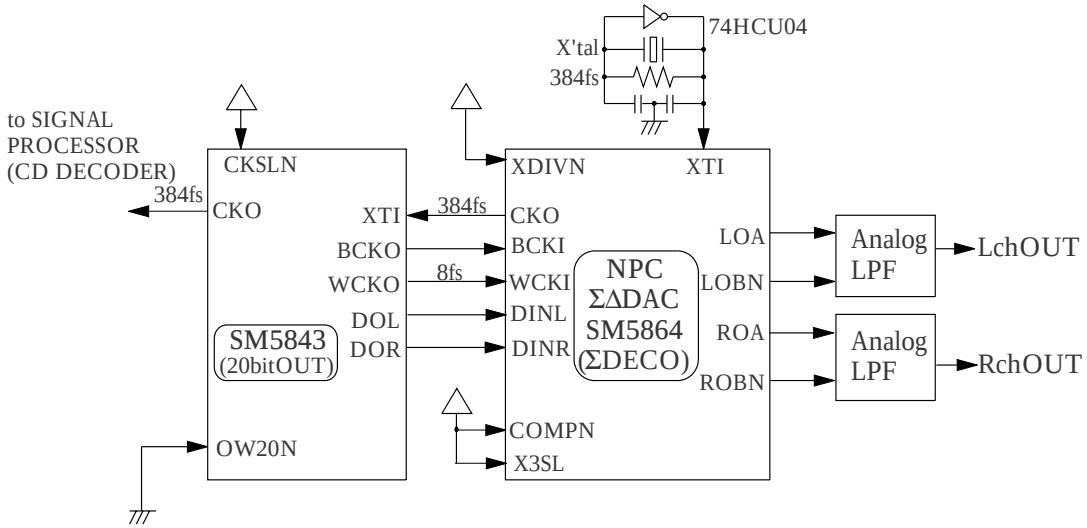


Digital audio interface receiver (YM3623B) connection



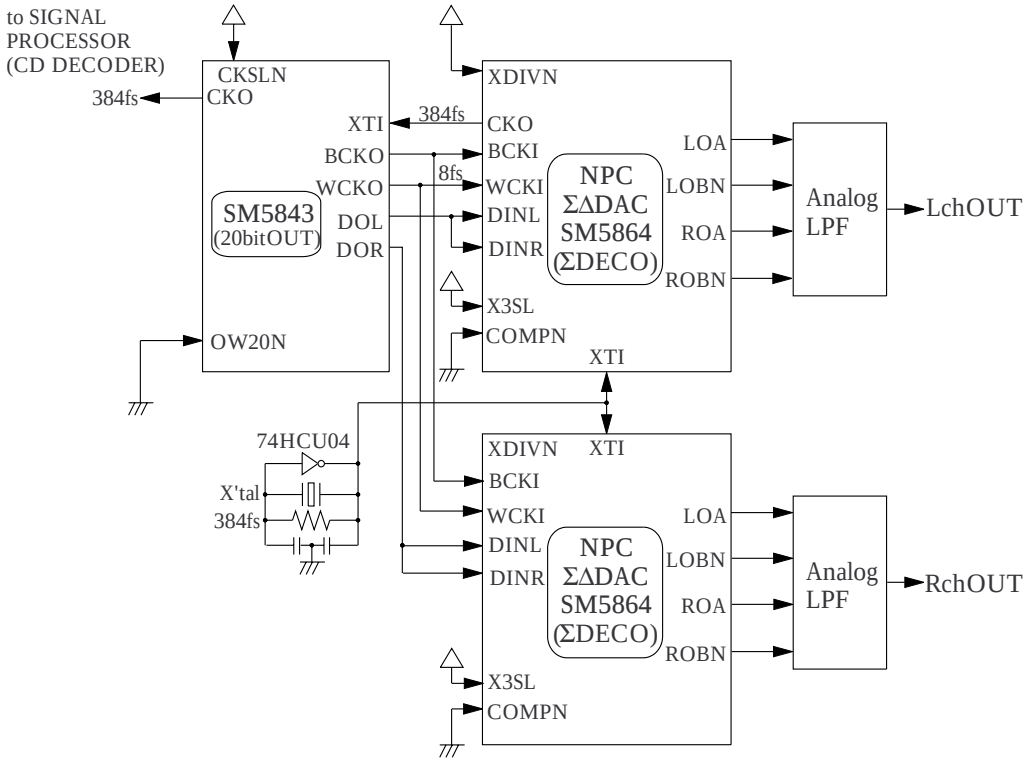
Output Interface Circuits

20-bit input ΣΔ DAC (SM5864AP) connection 1



20-bit input ΣΔ DAC (SM5864AP) connection 2

L/R-channel independent complementary PWM output



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NC9626AE 1997.03

To allow the use of the advanced features provided by the HR series of TASCAM DTRS recorders, the DA-98HR and DA-78HR, the RC-898 remote control unit has been updated.

In addition, some other features have been made to reflect changes in the DTRS product line.

Note that when using this version of the RC-898 (2.0), units in the HR series should be at least system version 1.12 (DA-78HR) and system version 1.01 (DA-98HR). It is strongly recommended that it is not used with HR series units with earlier system versions.

The changes are restricted to menus and menu items. In other respects, the operation of the RC-898 is as described in the existing manual.

Track Delay Time (menu group 0)

DA-98HR – Note that although the operation of this function has not changed significantly, when it is used in conjunction with the DA-98HR's higher sampling frequencies (dual-frequency and quad-frequency), the number of samples now accurately reflects the time selected on the DA-98HR (that is, a higher sampling frequency is expressed as a larger number of samples for a given time).

Also note that when fewer than eight tracks are available for recording as the result of selecting a dual or quad sampling frequency, the unavailable tracks are not shown for selection.

For example, if the first DTRS unit in the chain is a DA-98HR which has been set to record at a sampling frequency of 192k (quad-frequency), only tracks 1 and 2 of this unit are available for recording and are shown for selection on the RC-898 screen, and instead of tracks 1 through 8 being available for grouped selection (usually, 1–8 appears in the display), only tracks 1 through 2 are available (1–2).

Track Copy (menu group 0)

DA-98 & DA-38 – Note that this menu item applies only to DA-38 and DA-98 DTRS units.

When it is required to change the input assignment of DA-98HR and DA-78HR units, the new Input Patchbay menu item (see immediately below) should be used.

Input Patchbay (menu group 0)

DA-78HR & DA-98HR – This new menu item allows the assignment of different signal sources to the inputs of the appropriate DTRS machine.

Input Patch						Mon 1		
Trk	1	2	3	4	5	6	7	8
Src	T	M	S	S	D	M	S	S
ch	1	–	3	4	5	–	7	8

There are four different sources that may be selected: T (tape), D (the currently-selected digital source on the DA-98HR), S (the slot source on the DA-98HR) and M (mute—this is not really a source).

Note that when this menu is used to select the input sources of a DA-78HR, the S option can refer only to the analog inputs. The D option refers to the SPDIF input, if this has been selected, otherwise to the TDIF-1 inputs.

If all tracks have been selected for recording at base frequency (DA-98HR), all tracks are shown, otherwise only those tracks available for recording are shown.

1 **Select the machine for editing (SHIFT + ▲ or ▼ keys).**

2 **Use the ◄ and ► cursor keys to move to the appropriate track.**

3 **Use the ▲ or ▼ keys to change the input source.**

4 **To select the source channel, use the ◄ cursor key to move to the extreme left of the screen, (Src) and then move the cursor down to the ch row.**

5 **Use the ► cursor key to select the channel (as defined in the ch row) number.**

To return to the source row, once again move the cursor to the extreme left, and then move up.

Rec Mute (menu group 1)

DA-98, DA-78HR & DA-98HR – The rec mute function can be enabled on a track-by-track basis, as described in the RC-898 manual.

However, note that if a DA-98HR unit is used and the sampling frequency is set to dual- or quad-frequency so that there are fewer than eight tracks available, only those tracks that are available will be shown in this screen.

Analog Reference Level (menu group 2)

DA-98 & DA-98HR – When this screen is selected with a DA-98HR fitted with AD and DA boards such as the optional IF-AN98HR boards, the input and output reference levels can be viewed (the changes are made using jumpers on the IF-AN98HR boards).

```
Analog Ref Level
      Machine  1
   Input    Output
  -16 dB    -16 dB
```

When this screen is selected with a DA-98 unit, the input and output reference levels can be set together to –16 dB, –18 dB or –20 dB.

```
Analog Ref Level
      Machine  1
      In/Out
      -16 dB
```

Video Reference (menu group 3)

DA-98HR – On the DA-98HR, the incoming video reference can be detected automatically (Auto) and this setting will typically work satisfactorily.

However, to improve synchronization in the case of a less-than-perfect video sync source, the rate can be manually set to any of the following: 30F, 29.97F, 25F, or 24F. See the DA-98HR manual for full details of this function.

```
Video Reference
      Machine  1


          Auto
```

1 **Select the machine whose video reference is to be edited.**

2 **Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the value.**

TC Accuracy (menu group 4)

DA-78HR & DA-98HR – When using the RC-898 with the DA-78HR and the DA-98HR, it is possible to change the timecode accuracy on a per-machine basis.

This means that slightly nonstandard timecode input can be accepted and used by the units which have the `Wider` option selected. Typically, all units will use the `Normal` setting, however:

```
TC Accuracy
Wider
Normal
Machine 1 2 3 4 5 6
```

1 Use the ◄ and ► cursor keys to move to the appropriate machine column.

2 Use the ▲ or ▼ keys to move the cursor to the appropriate line for that machine (either the `Wider` or the `Normal` line).

Consult the DTRS unit's manual for full details of this facility.

TC Timing (menu group 5)

DA-98HR, DA-78HR & DA-98 – When using the AD conversion facilities in the optional slot boards for the DA-98HR, and when using the DA-78HR, it is now possible to select either an analog or a digital timing reference for the timecode inputs and outputs independently. With the DA-98, this option is available for timecode output only.

The screen title and display have now changed (the screen shown below refers to a DA-98HR or DA-78HR unit).

```
TC Timing
     Machine  1
  Input   Output
  Analog  Analog
```

1 Select the machine whose timing reference is to be edited.

2 Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the timecode timing value for the input and output of that machine.

Clock (menu group 9)

All units – Although this screen appears the same as in previous versions of the RC-898, the available options have been changed to reflect the new models.

As before, the options for the DA-88 and DA-98 models (as well as for the DA-78HR and DA-98HR) are `Int` (internal), `Word` (word clock) and `Video` (video input).

For the DA-78HR and DA-98HR, the `Dig in` option has been added (digital inputs).

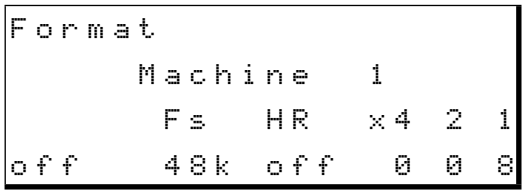
For the DA-98HR only, the `slot` option has been added, allowing certain optional slot boards to be used as the clock master. Note that the same restrictions apply as on the DA-98HR (for example, the IF-AN98HR slot boards cannot act as the master clock source).

Format (menu group 9)

DA-78HR & DA-98HR – This menu has been expanded to recognize the high-resolution and high sampling frequency capacities of the newer models.

In the case of both the DA-78HR and the DA-98HR, a HR (high-resolution) field allows the setting of this parameter to be on (24-bit) or off (16-bit).

In the case of the DA-98HR, the sampling frequency selected acts as the base frequency for the unit. The available track combinations are then displayed on the bottom right of the screen.



When the cursor is moved to this field, use the ▲ and ▼ keys to switch between the following options:

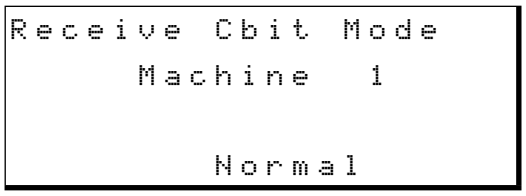
0 0 8	(eight base-frequency tracks)
0 2 4	2 x dual-frequency tracks, 4 base-frequency tracks
0 3 2	3 x dual-frequency tracks, 2 x base-frequency tracks
0 4 0	4 x dual-frequency tracks
2 0 0	2 x quad-frequency tracks

The process of selecting machines for the formatting process, and actually carrying out the format is as described in the RC-898 manual (move the cursor to off, change the message to ready, change the message to on, and then use the **RECORD** and **PLAY** key combination to start the format process).

Consult the DA-98HR manual for full details of the available track functions.

Receive Cbit Mode (menu group A)

DA-98HR – When using the DA-98HR, any mismatches between the received audio data and the data specified by the Cbits in the audio data stream will usually be shown on the DA-98HR display. However, it is possible to turn this off, using the screen here:



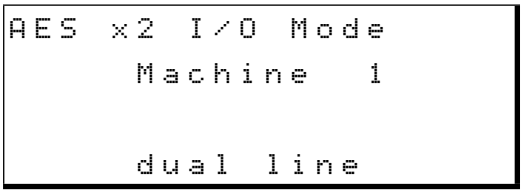
1 **Select the machine to be edited.**

2 **Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the parameter to either** Normal **or** No Warning.

AES x 2IO (menu group A)

DA-98HR – When using a DA-98HR unit when four dual-frequency tracks have been selected as the available tracks, there is a choice of how the signals should be output: either as dual-line or high-frequency signals, as explained more fully in the DA-98HR manual.

The settings are made using the following screen:

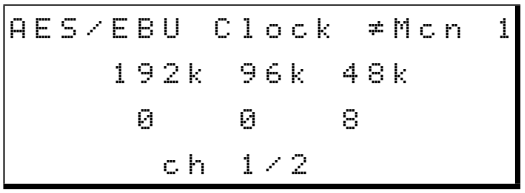


1 **Select the machine to be edited.**

2 **Move the cursor to the bottom line and use the the ▲ or ▼ keys to set the parameter to either** dual line **or** high speed.

AES/EBU Clock (menu group A)

DA-98HR – When recording on the DA-98HR with AES/EBU inputs, you may wish to select one of the options described here as a clock source.

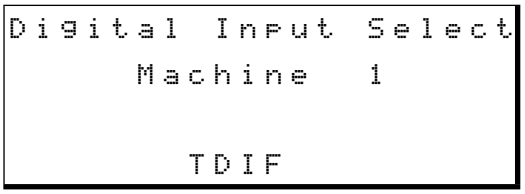


When this screen is shown, the current available track setting for the selected machine is also displayed. This available track setting also affects the choice of clock source, as does the dual AES/EBU mode described above.

Setting	Available clock source channels
Base x 8	1/2, 3/4, 5/6, 7/8
Dual-frequency x 4 (dual channel)	1, 2, 3, 4
Dual-frequency x 4 (high-speed)	1/2, 3/4
Dual-frequency x 2, base x 4	1, 2, 3/4, 5/6
Dual-frequency x 3, base x 2	1, 2, 3, 4/5
Quad-frequency x 2	1, 2

Digital Input Selection (menu group A)

DA-78HR & DA-98HR – This menu item allows the selection of digital sources for these two units in addition to the TDIF-1 input source.

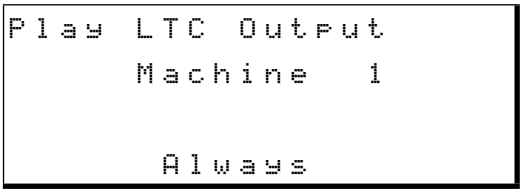


For the DA-98HR, the choice is either `TDIF` or `AES/EBU`.

For the DA-78HR, the choice is either `TDIF` or `SPDIF`.

Play TC Out (menu group A)

DA-78HR & DA-98HR – This menu item allows you to choose whether the selected unit will always output linear timecode (LTC) or will only output such timecode when the unit clock is locked (that is, it outputs LTC only when audio data is output).



The two options here are `Always` and `Locked Only`.

Output Patchbay (menu group B)

DA-78HR & DA-98HR – This screen allows the assignment of a track's audio to any output, simulating a digital patchbay. Only the numerals in the bottom row of the screen can be changed here (that is, the audio track number).

```
Output Patch
      Machine  1
  ch  1 2 3 4 5 6 7 8
 Trk  1 2 3 4 5 6 7 8
```

Mix Input Selection (menu group B)

DA-78HR & DA-98HR – This screen allows the selection of the sources for the internal mixer of DA-98HR and DA-78HR units.

```
Mix Input        Mcn 1
 Trk  1 2 3 4 5 6 7 8
 Src  T M S S D M S S
  ch  1 - 3 4 5 - 7 8
```

1 Select the machine for editing.

NOTE

If the machine selected is not capable of being controlled using this menu (that is, it is neither a DA-98HR nor a DA-78HR) an appropriate message is shown.

2 Use the ◄ and ► cursor keys to move to the appropriate track.

3 Use the ▲ or ▼ keys to change the input source.

4 To select the source channel, use the ◄ cursor key to move to the extreme left of the screen, (`Src`) and then move the cursor down to the `ch` row.

5 Use the ► cursor key to select the channel (as defined in the `ch` row) number.

To return to the source row, once again move the cursor to the extreme left, and then move up.

Output Word Length (menu group B)

DA-78HR & DA-98HR – This menu allows either 16-bit or 24-bit to be selected as the word length of the output audio data.

```
Output Word Length
 16 bit
 24 bit
Machine 1 2 3 4 5 6
```

The rows on this screen represent the bit resolution of the output audio, and the columns represent the machines in the chain.

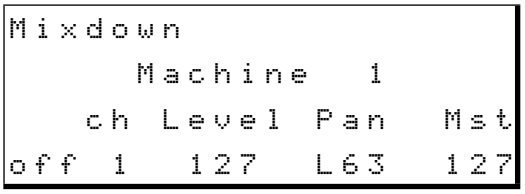
1 Use the ◄ and ► cursor keys to move to the appropriate machine column.

2 Use the ▲ or ▼ keys to move the cursor to the appropriate line for that machine (either the `16 bit` or the `24 bit` line).

Mixdown (menu group B)

DA-78HR & DA-98HR – This screen allows the sources selected for mixdown in the screen described above to be mixed into a stereo pair, with individual level and pan for each channel of the mix, as well as a master level for the whole stereo mix.

Select the machine on which the mixdown is to take place.



The bottom left parameter controls whether the mixdown is on or off for the machine. If this is set to off, no other settings made on this screen will have any effect.

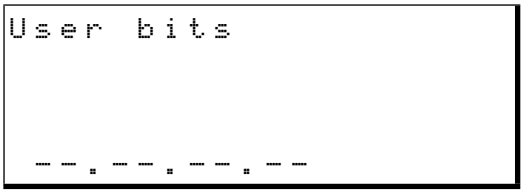
The channel may be selected, and the level adjusted from 0 to 127.

Pan settings are from hard left L- through L63 through C (center) to -R (hard right).

The master mix volume may be adjusted from 0 to 127.

User bits (menu group D)

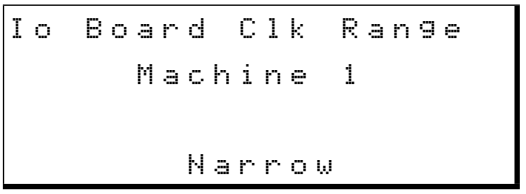
DA-78HR & DA-98HR – There are no parameters to be set in this screen, which simply displays any user bits recorded within the timecode source.



IO Clock range (menu group D)

DA-98HR – When using the DA-98HR with the optional IF-AN98HR slot boards, it may be necessary to adjust the clock width setting.

The Narrow setting enables a crystal oscillator, and suppresses jitter, providing high-quality audio. However, if the clock master accuracy is low, the precision is affected, and the audio quality may suffer. The Wide setting enables an LC oscillator. The jitter level is increased a little compared with the Narrow setting and the audio quality may be slightly diminished, but this setting can be used even with poor-quality input clocks.



For details of the limitations imposed on this setting, consult the appropriate section of the DA-98HR manual.

Tape Load/Save (menu group F)

DA-78HR & DA-98HR – This allows the saving and loading of the RC-898's settings to and from tape. The settings that are saved are:

- Locate Points (Master only)
- Locate Pre-roll
- GPI Setup
- Event
- 9pin Control Mode
- 9pin Rec Acceptable
- Key Mode
- Frame Display
- Display Time

These parameters are stored on tape. They do not affect any audio data on the tape. Only one set of parameters can be stored on one tape.

NOTE

This operation only applies to the tape recorded on the first machine in the chain (ID=1).

1 With a tape loaded in the unit, use the ▲ and ▼ keys to select either `Load` or `Save`. Press SELECT.

2 The display shows `Are you sure ?`. Press SELECT to confirm the operation. To cancel the operation, press either ESCAPE or STOP so the display shows `Cancel`. Press the ESCAPE key to dismiss this message.

While the operation is taking place (either loading or saving the data), the display shows `Executing...`. Any REC FUNCTION indicators will go out.

3 If the operation is successful, the display shows `Complete`. Press the ESCAPE key to dismiss this message.

If an error occurs, one of the following messages may appear. Press the **ESCAPE** key to dismiss these messages:

`Can't start`	A suitable tape is not loaded, etc.
`Data not found`	No data has been recorded on the tape (when loading)
`Read error`	An error occurred when reading the data from tape (when loading)
`Verify error`	An error occurred when certifying the data after writing (when saving)

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