TASCAM

X-48MKⅡ

SCHEMATIC DIAGRAM

回路図

CONTENTS 目次

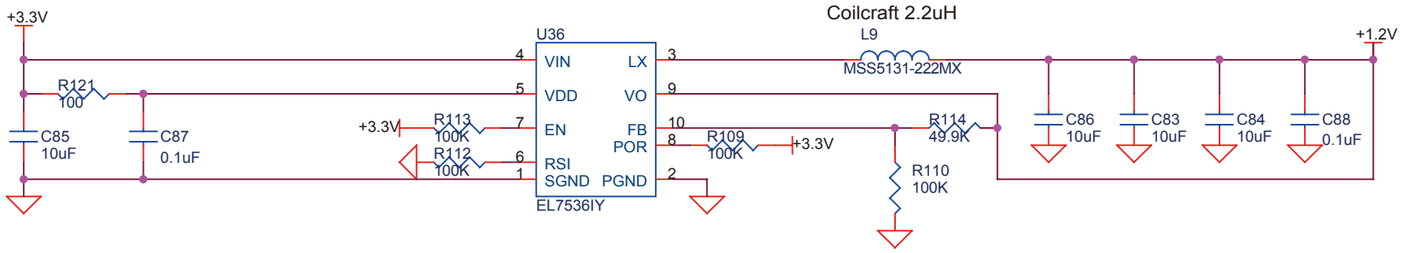
Place jumper between 3-2 when configuring via Xilinx cable.
Place jumper between 2-1 when performing full JTAG scan

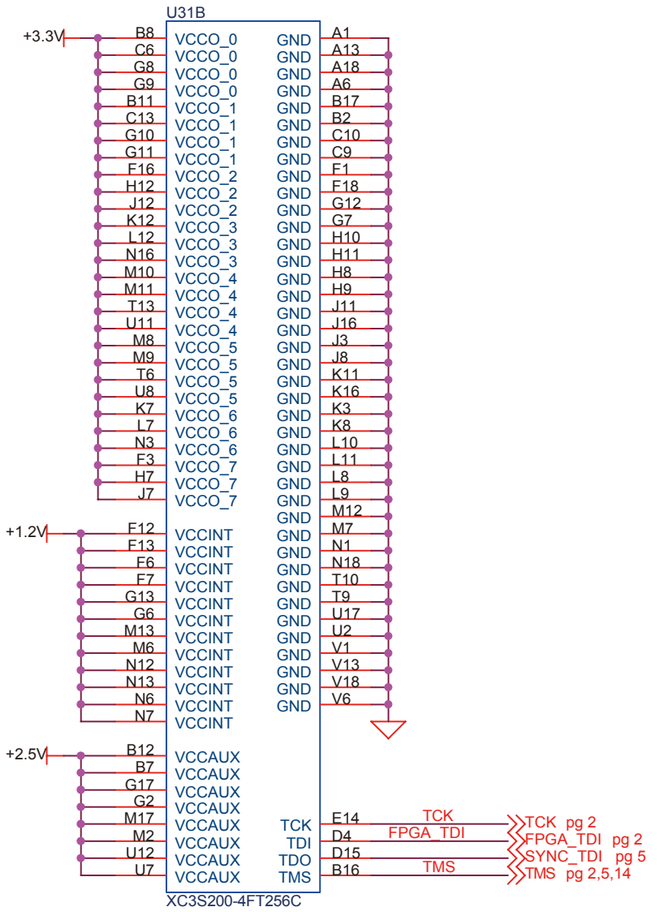
All clock should be same length +/- 0.25"

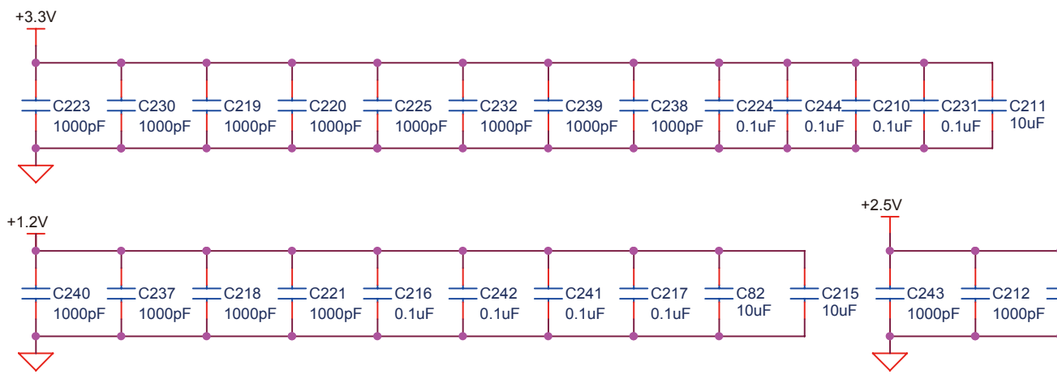
Slave Serial: M0=1, M1=1, M2=1

Xilinx JTAG Header

PCI (2/14) FPGA Power and Bypass







pg 2,14 CLK_66MHZ[4:0]

pg 2,14 PLX_LA[31:2]

pg 2 FPGA_A[15:0]

pg 2 BUS_EXCHANGE

pg 2 SRAM_BE#[3:0]

pg 2 SRAM_CS#

pg 2 SRAM_OE#

pg 2 FPGA_SRAM_WE#

pg 2 FPGA_SRAM_CS#

pg 2 FPGA_SRAM_OE#

Ping

U22A — CY7C1329G-133AC

CLK_66MHZ2

PING_CS#, PING_CE2, PING_OE#, PING_BE#0, PING_BE#1, PING_BE#2, PING_BE#3, PING_ADSP#, PING_GW#, PING_ADV#

PING_A[31:0] — PING_D[31:0]

Pong

U16A — CY7C1329G-133AC

CLK_66MHZ3

PONG_CS#, PONG_CE2, PONG_OE#, PONG_BE#0, PONG_BE#1, PONG_BE#2, PONG_BE#3, PONG_ADSP#, PONG_GW#, PONG_ADV#

PONG_A[31:0] — PONG_D[31:0]

U23, U27 — SN74CBTLV16212VR

+3.3V — C187, C197, C168, C147, C124 — 0.1uF

R175 4.7K

R180, R182, R183, R181, R179, R178, R177, R176 — 4.7K

R184, R185 — 4.7K

R79, R82, R78, R81 — 1K

TP PAD17, TP PAD19, TP PAD16, TP PAD18

RP6 — 746X101103J

SRAM_CS#, SRAM_OE#, FPGA_SRAM_CS#, FPGA_SRAM_OE#, FPGA_SRAM_WE#

PAD21 TP, PAD20 TP, PAD22 TP

RP15 — 746X101103J

PING_ADSP#, PING_GW#, PING_ADV#, PING_CE2

U16B, U22B — CY7C1329G-133AC

SRAM ByPass

C160–C179 1000pF / 0.01uF / 0.1uF, C173 10uF

C130–C143 1000pF / 0.01uF / 0.1uF, C134 10uF

DIFFERENTIAL INPUT IS MORE ROBUST TO HANDLE DIRTY CLOCKS

Word Clock Input

Frequence Range:
32kHz - 101kHz

SOURCE_SEL [2:0] :
0 = Word In
1 = 48K
2 = 96K
3 = 44.1K
4 = 88.2K
5 = S/PDIF
6 = D FA_WCLK_IN or DIFB_WCLK_IN
7 = DDS_XWC

Frequency Range:
Fs*256 => Up to
27MHz

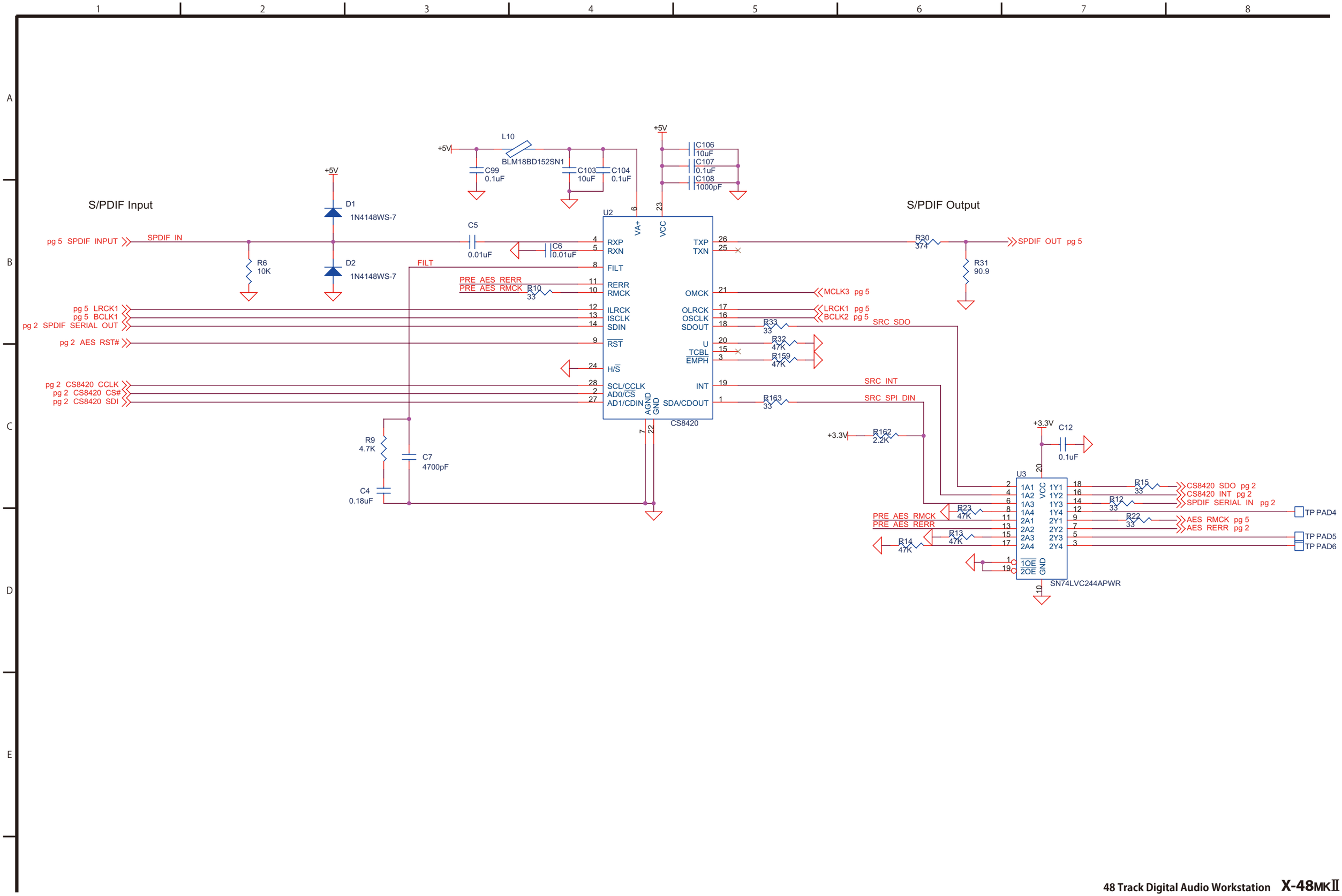
Word Clock Output

Frequency Range:
32kHz - 101kHz

Time Base Header

Power Supply Sync

PCI (5/14) SPDIF I/O



1 2 3 4 5 6 7 8

A B C D E

L1 P1330 105K 1000uH +12V +12V LTCIN
C1 4 7uF 35V
C89 0 1uF

L3 P1330 105K 1000uH 12V 12V LTCIN
C3 4 7uF 35V
C93 0 1uF

GAP WITH BRIDGE

DIFFERENTIAL INPUT IS USED BECAUSE SINGLE ENDED REQUIRES POWER ON OTHER BOARD.

SMPTE LTC Input

SMPTE LTC RX
C10 4 7uF 35V
R156 100K
D10 1N4148WS 7
D11 1N4148WS 7
R160 10K

SMPTE LTC RX+
C8 4 7uF 35V
R155 100K
D9 1N4148WS 7
D8 1N4148WS 7
R158 10K
C94 100pF
R157 10K

SMPTE LTC Receive

C100 100pF
R161 10K
U55A NJM4565M
D4 1N4148WS 7
D3 1N4148WS 7
R19 12K
U55B NJM4565M
R161 3 3K
C16 1uF X5R 25V
R36 10K
+3 3V C21 0 1uF
R41 33K
U10A TC74VHCU04FT
R42 10K
R46 33K
U10B TC74VHCU04FT
U10C TC74VHCU04FT
R47 47
LTC RX pg 2

L2 P1330 105K +12V +12V LTCOUT
C2 4 7uF 35V
C90 0 1uF

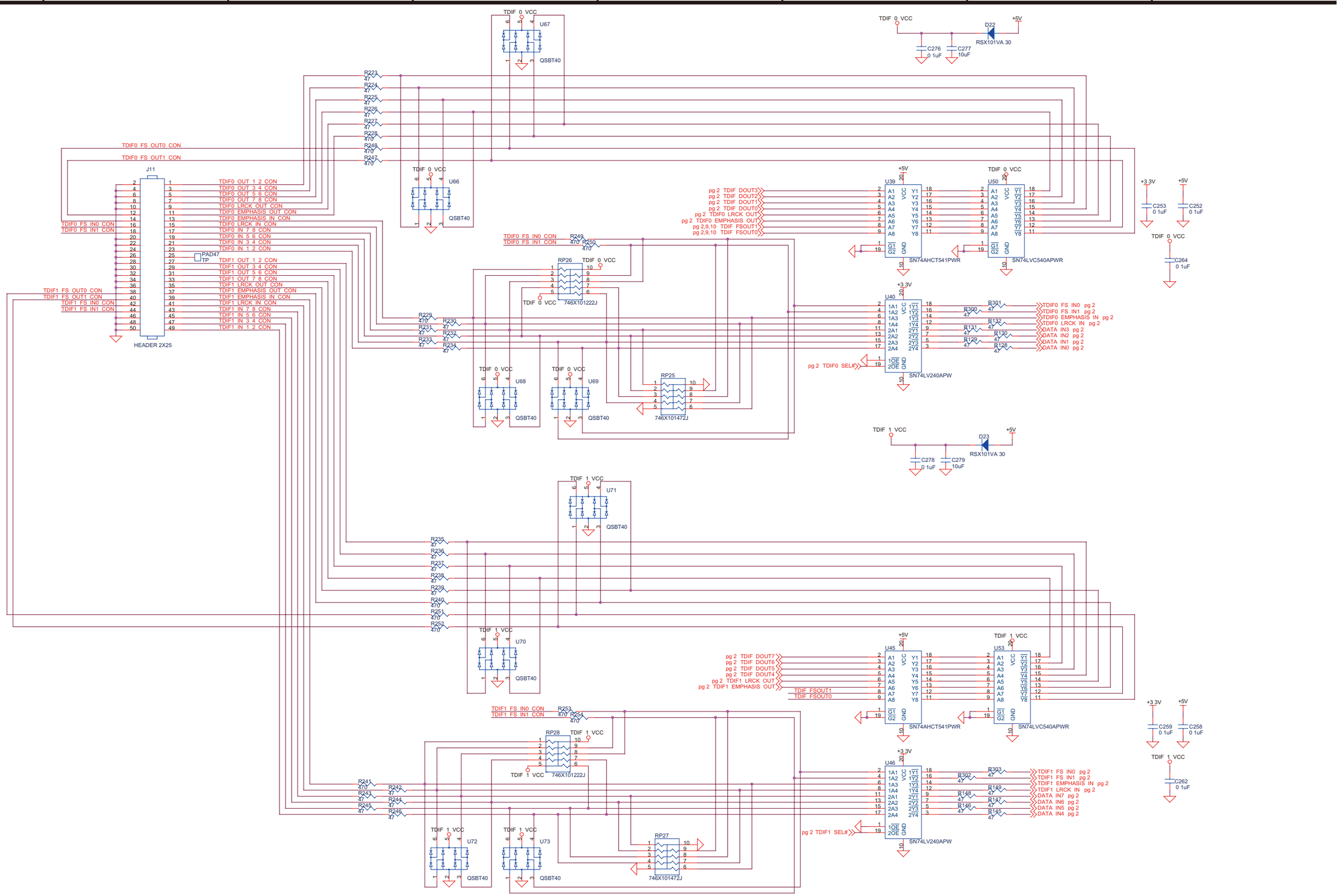
L4 P1330 105K 12V 12V LTCOUT
C9 4 7uF 35V
C97 0 1uF

C109 100pF
R169 10K
C29 220pF
U10D TC74VHCU04FT
pg 2 SMPTE LTC TX
R40 5 1K
R45 3 9K
R50 1K
R168 10K
U56A NJM4565M
C18 47U/35V
LTC OUT+
R166 100K
R167 100K
U56B NJM4565M
C14 47U/35V
LTC OUT
R165 22K
C105 100pF

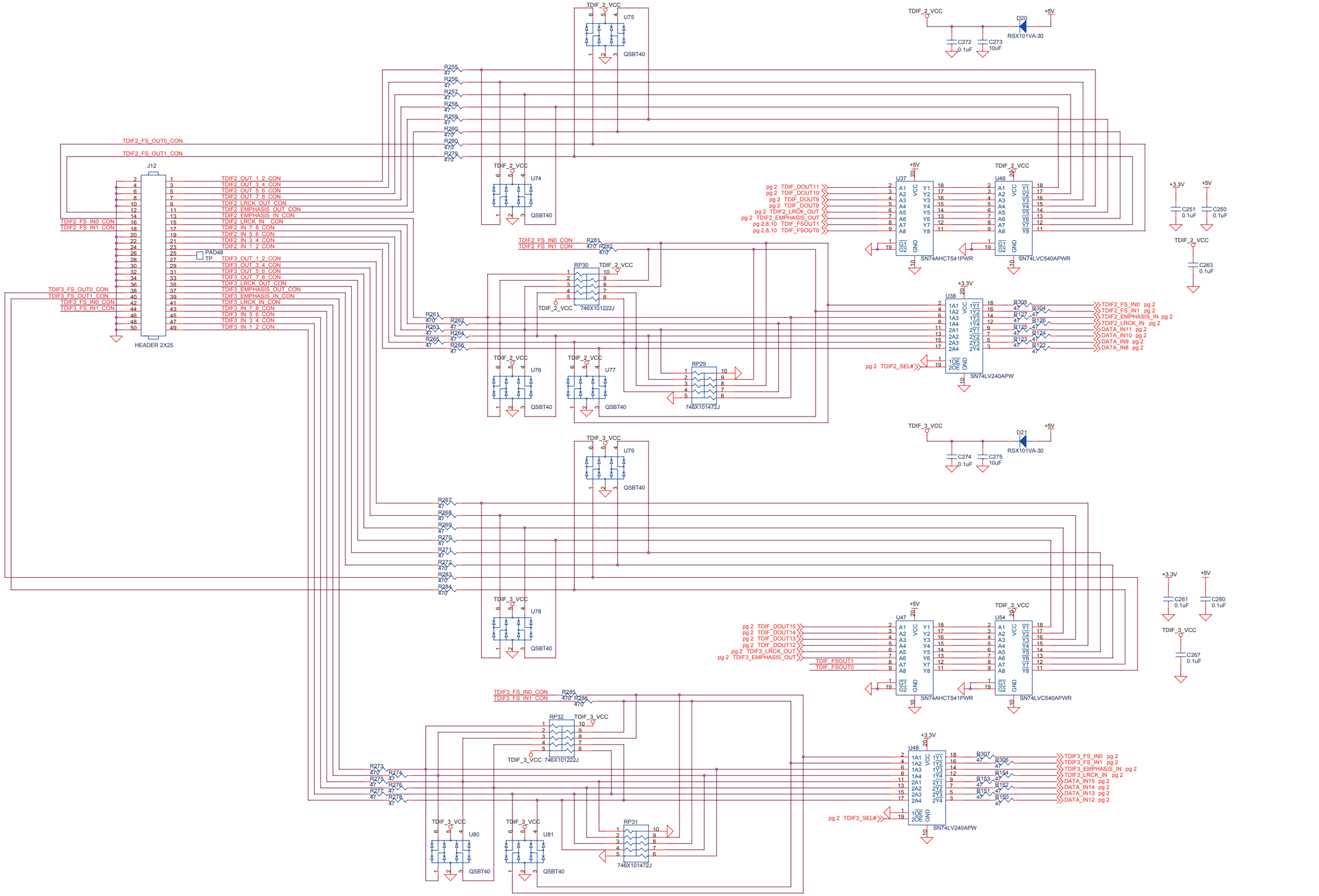
J1 HEADER 2X5
SMPTE LTC RX+
LTC OUT+
SMPTE LTC RX
LTC OUT

R187 2 7
C191 10uF
C196 0 1uF
C190 10uF
C195 0 1uF
D6 1N4148WS 7
D7 1N4148WS 7
pg 5 VIDEO IN
U24 EL4511CU
VERTIN HIN SYNCIN SCL SDA SDENB PDWN XTAL XTALN
SYNCOUT HOUT VERTOUT ODD/EVEN BACKPORCH SYNCLOCK VBLANK LEVEL
pg 2 EL4511 SCL
pg 2 EL4511 SDA
pg 2 EL4511 SDENB
VSYNC pg 2
FIELD pg 2
SYNCLOCK pg 2
Y3 ECS 327 12 5 17 32.768KHZ Crystal

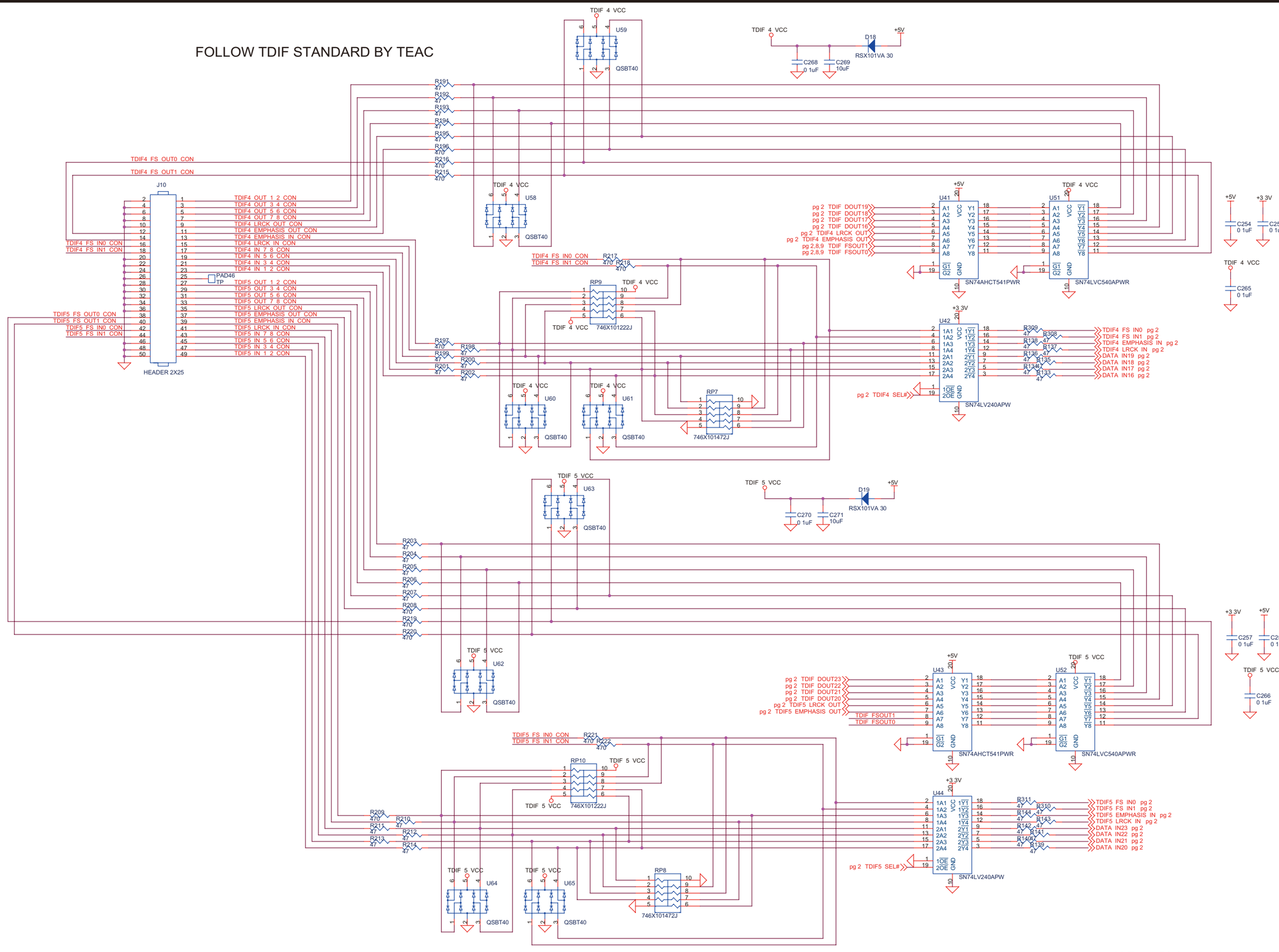
U10E TC74VHCU04FT
U10F TC74VHCU04FT

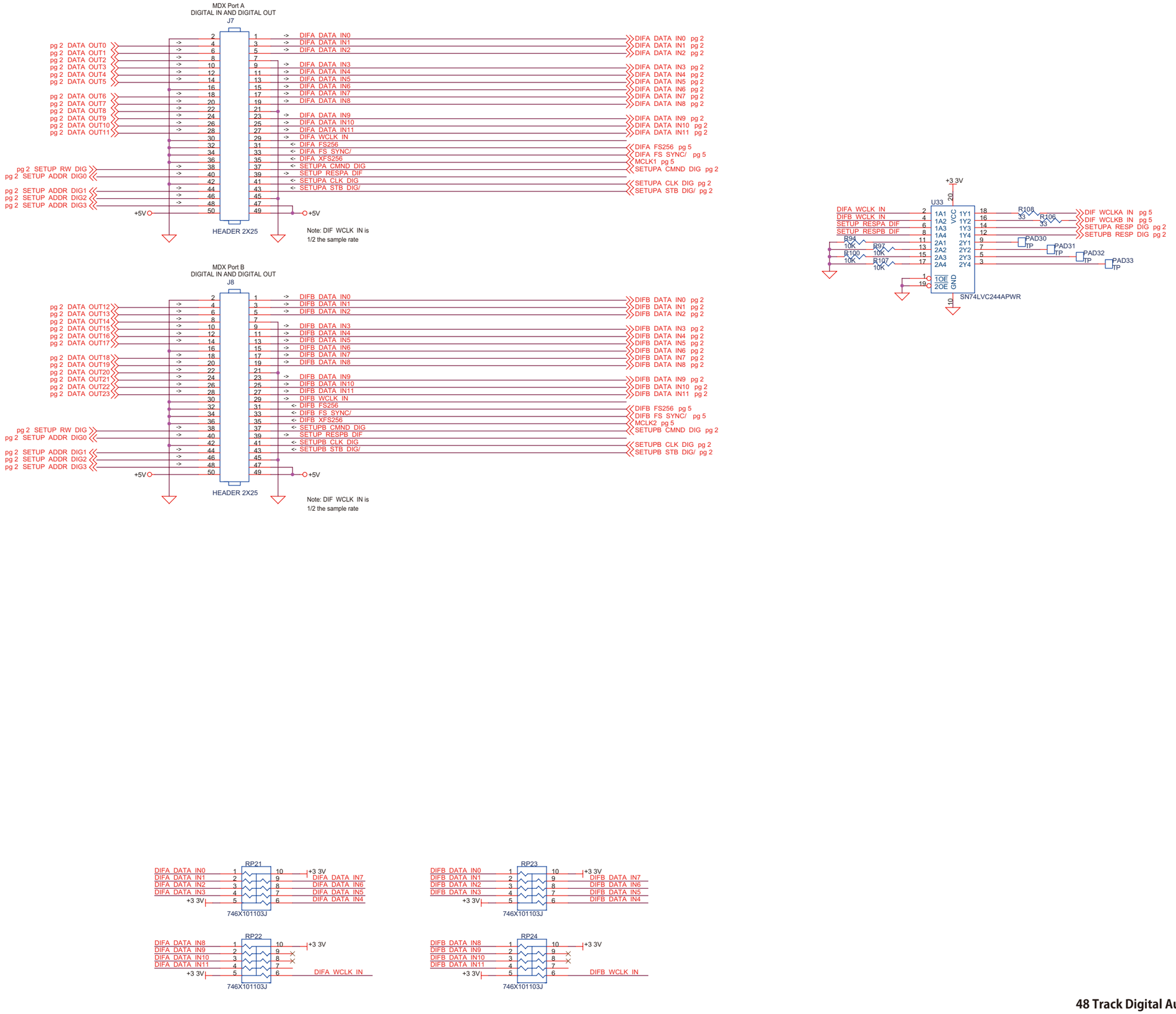

J11
HEADER 2X25
TDIF0_FS_OUT0_CON
TDIF0_FS_OUT1_CON
TDIF0_FS_IN0_CON
TDIF0_FS_IN1_CON
TDIF0_OUT_1_2_CON
TDIF0_OUT_3_4_CON
TDIF0_OUT_5_6_CON
TDIF0_OUT_7_8_CON
TDIF0_LRCK_OUT_CON
TDIF0_EMPHASIS_OUT_CON
TDIF0_EMPHASIS_IN_CON
TDIF0_LRCK_IN_CON
TDIF0_IN_7_8_CON
TDIF0_IN_5_6_CON
TDIF0_IN_3_4_CON
TDIF0_IN_1_2_CON
TDIF1_FS_OUT0_CON
TDIF1_FS_OUT1_CON
TDIF1_FS_IN0_CON
TDIF1_FS_IN1_CON
TDIF1_OUT_1_2_CON
TDIF1_OUT_3_4_CON
TDIF1_OUT_5_6_CON
TDIF1_OUT_7_8_CON
TDIF1_LRCK_OUT_CON
TDIF1_EMPHASIS_OUT_CON
TDIF1_EMPHASIS_IN_CON
TDIF1_LRCK_IN_CON
TDIF1_IN_7_8_CON
TDIF1_IN_5_6_CON
TDIF1_IN_3_4_CON
TDIF1_IN_1_2_CON
PAD47
TP
TDIF 0 VCC
TDIF 1 VCC
U66
U67
U68
U69
U70
U71
U72
U73
QSBT40
RP25
RP26
RP27
RP28
746X101472J
746X101222J
R223 47
R224 47
R225 47
R226 47
R227 47
R228 470
R246 470
R247 470
R229 470
R230 47
R231 47
R232 47
R233 47
R234 47
R235 47
R236 47
R237 47
R238 47
R239 47
R240 470
R251 470
R252 470
R249 470
R250 470
R253 470
R254 470
R241 470
R242 47
R243 47
R244 47
R245 47
R246 47
C276 0 1uF
C277 10uF
C278 0 1uF
C279 10uF
D22 RSX101VA 30
D23 RSX101VA 30
+5V
+3.3V
C253 0 1uF
C252 0 1uF
C264 0 1uF
C259 0 1uF
C258 0 1uF
C262 0 1uF
U39
U50
U45
U53
U40
U46
SN74AHCT541PWR
SN74LVC540APWR
SN74LV240APW
SN74AHCT541PWR
SN74LVC540APWR
SN74LV240APW
pg 2 TDIF DOUT3
pg 2 TDIF DOUT2
pg 2 TDIF DOUT1
pg 2 TDIF DOUT0
pg 2 TDIF0 LRCK OUT
pg 2 TDIF0 EMPHASIS OUT
pg 2,9,10 TDIF FSOUT1
pg 2,9,10 TDIF FSOUT0
pg 2 TDIF DOUT7
pg 2 TDIF DOUT6
pg 2 TDIF DOUT5
pg 2 TDIF DOUT4
pg 2 TDIF1 LRCK OUT
pg 2 TDIF1 EMPHASIS OUT
TDIF_FSOUT1
TDIF_FSOUT0
pg 2 TDIF0 SEL#
pg 2 TDIF1 SEL#
TDIF0 FS IN0 pg 2
TDIF0 FS IN1 pg 2
TDIF0 EMPHASIS IN pg 2
TDIF0 LRCK IN pg 2
DATA IN3 pg 2
DATA IN2 pg 2
DATA IN1 pg 2
DATA IN0 pg 2
TDIF1 FS IN0 pg 2
TDIF1 FS IN1 pg 2
TDIF1 EMPHASIS IN pg 2
TDIF1 LRCK IN pg 2
DATA IN7 pg 2
DATA IN6 pg 2
DATA IN5 pg 2
DATA IN4 pg 2

PCI (8/14) TDIF 3-2 Interface

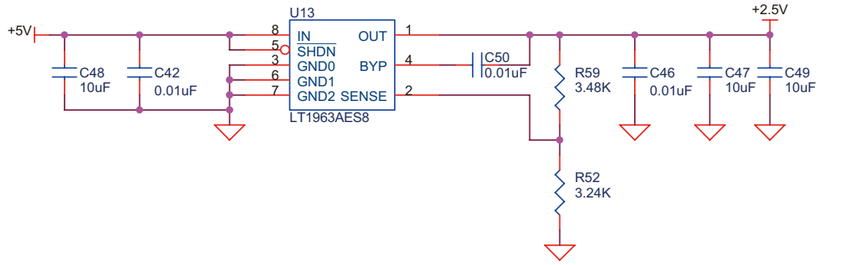


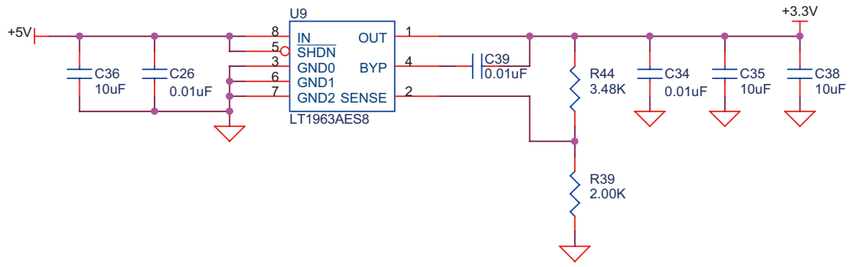
FOLLOW TDIF STANDARD BY TEAC



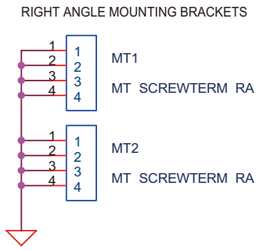

MDX Port A
DIGITAL IN AND DIGITAL OUT
J7
HEADER 2X25
Note: DIF WCLK IN is 1/2 the sample rate
MDX Port B
DIGITAL IN AND DIGITAL OUT
J8
HEADER 2X25
Note: DIF WCLK IN is 1/2 the sample rate
+3.3V
U33
SN74LVC244APWR
R94
R97
R100
R107
R108
R106
PAD30
PAD31
PAD32
PAD33
RP21
RP22
RP23
RP24
746X101103J

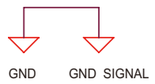
PCI (11/14) Power Supplies





RIGHT ANGLE MOUNTING BRACKETS



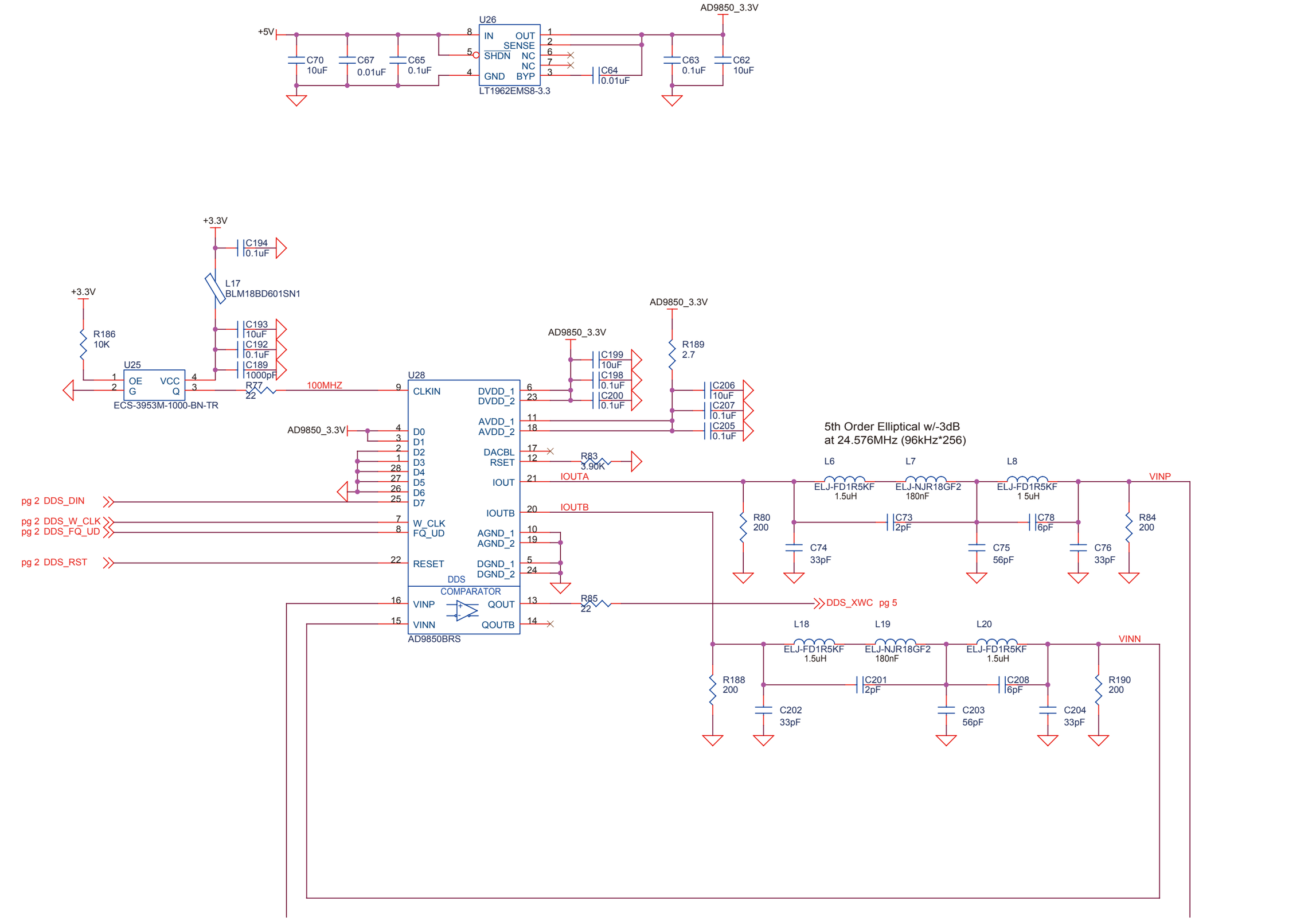


Reference for SMT

REF1 TEAC REF
REF49 TEAC REF
REF2 TEAC REF
REF50 TEAC REF
REF51 TEAC REF
REF52 TEAC REF
REF54 TEAC REF
REF53 TEAC REF

Reference for QFP components

REF12 TEAC REF SMALL
REF14 TEAC REF SMALL
REF17 TEAC REF SMALL
REF20 TEAC REF SMALL
REF5 TEAC REF SMALL
REF8 TEAC REF SMALL
REF9 TEAC REF SMALL
REF10 TEAC REF SMALL
REF3 TEAC REF SMALL
REF6 TEAC REF SMALL
REF7 TEAC REF SMALL
REF4 TEAC REF SMALL
REF15 TEAC REF SMALL
REF19 TEAC REF SMALL
REF27 TEAC REF SMALL
REF33 TEAC REF SMALL
REF31 TEAC REF SMALL
REF18 TEAC REF SMALL
REF13 TEAC REF SMALL
REF11 TEAC REF SMALL
REF16 TEAC REF SMALL
REF21 TEAC REF SMALL
REF24 TEAC REF SMALL
REF22 TEAC REF SMALL
REF25 TEAC REF SMALL
REF28 TEAC REF SMALL
REF43 TEAC REF SMALL
REF44 TEAC REF SMALL
REF45 TEAC REF SMALL
REF46 TEAC REF SMALL
REF47 TEAC REF SMALL
REF48 TEAC REF SMALL
REF42 TEAC REF SMALL
REF41 TEAC REF SMALL
REF40 TEAC REF SMALL
REF39 TEAC REF SMALL
REF38 TEAC REF SMALL
REF37 TEAC REF SMALL
REF32 TEAC REF SMALL
REF35 TEAC REF SMALL
REF29 TEAC REF SMALL
REF34 TEAC REF SMALL
REF30 TEAC REF SMALL
REF36 TEAC REF SMALL
REF23 TEAC REF SMALL
REF26 TEAC REF SMALL


AD9850_3.3V
U26
+5V
IN
OUT
SENSE
SHDN
NC
NC
GND
BYP
LT1962EMS8-3.3
C70 10uF
C67 0.01uF
C65 0.1uF
C64 0.01uF
C63 0.1uF
C62 10uF
+3.3V
C194 0.1uF
L17 BLM18BD601SN1
C193 10uF
C192 0.1uF
C189 1000pF
R186 10K
U25
OE
VCC
G
Q
ECS-3953M-1000-BN-TR
R77 22
100MHZ
U28
CLKIN
DVDD_1
DVDD_2
AVDD_1
AVDD_2
DACBL
RSET
IOUT
IOUTB
AGND_1
AGND_2
DGND_1
DGND_2
DDS
COMPARATOR
VINP
VINN
QOUT
QOUTB
AD9850BRS
C199 10uF
C198 0.1uF
C200 0.1uF
R189 2.7
C206 10uF
C207 0.1uF
C205 0.1uF
R83 3.90K
IOUTA
IOUTB
R85 22
DDS_XWC pg 5
pg 2 DDS_DIN
pg 2 DDS_W_CLK
pg 2 DDS_FQ_UD
pg 2 DDS_RST
D0
D1
D2
D3
D4
D5
D6
D7
W_CLK
FQ_UD
RESET
5th Order Elliptical w/-3dB
at 24.576MHz (96kHz*256)
L6
L7
L8
ELJ-FD1R5KF 1.5uH
ELJ-NJR18GF2 180nF
ELJ-FD1R5KF 1 5uH
VINP
R80 200
C74 33pF
C73 2pF
C75 56pF
C78 6pF
C76 33pF
R84 200
L18
L19
L20
ELJ-FD1R5KF 1.5uH
ELJ-NJR18GF2 180nF
ELJ-FD1R5KF 1.5uH
VINN
R188 200
C202 33pF
C201 2pF
C203 56pF
C208 6pF
C204 33pF
R190 200

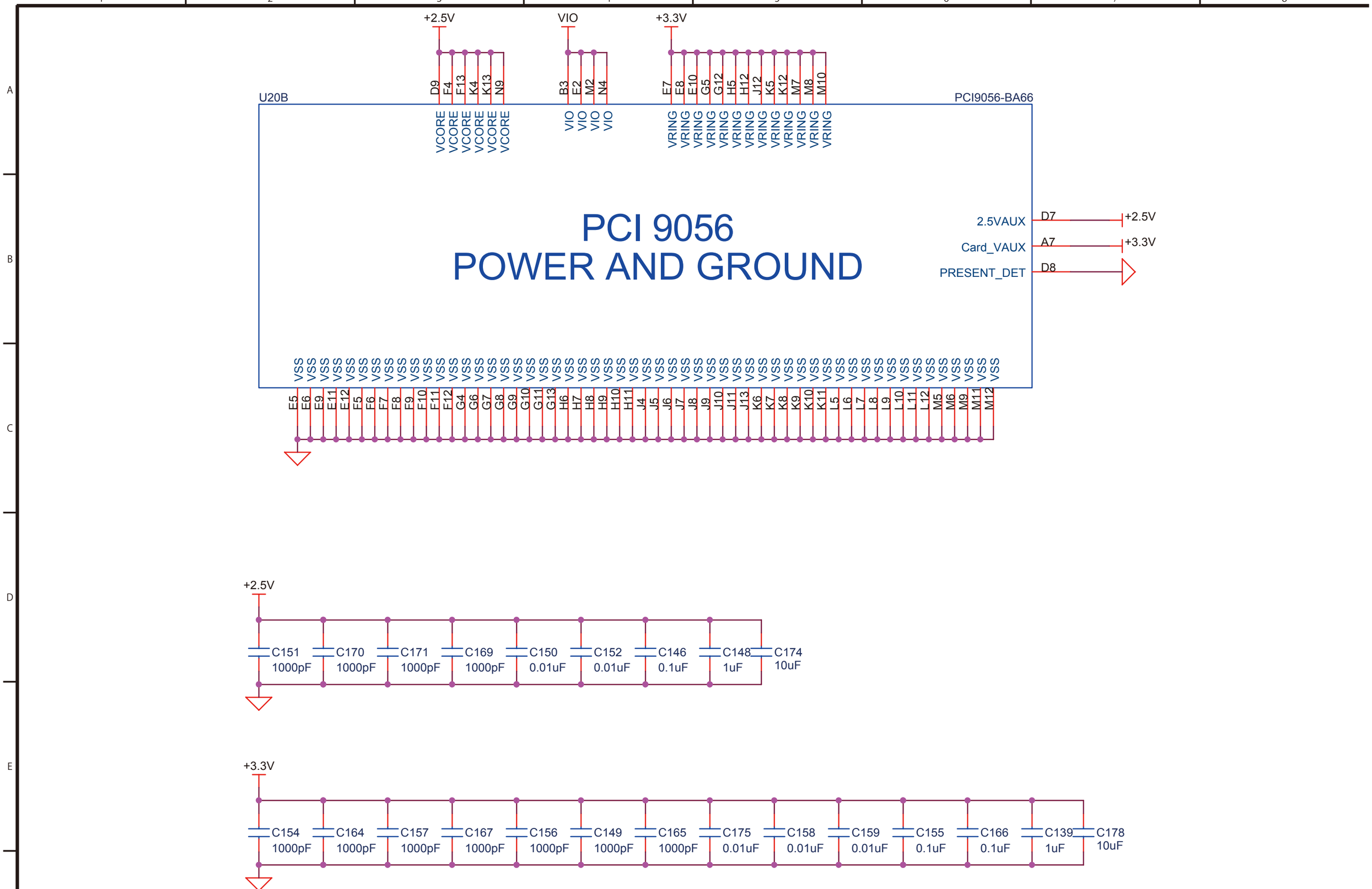
PLX PCI 9056
C MODE
PBGA-256

PCICLK net must be exactly 2.5".

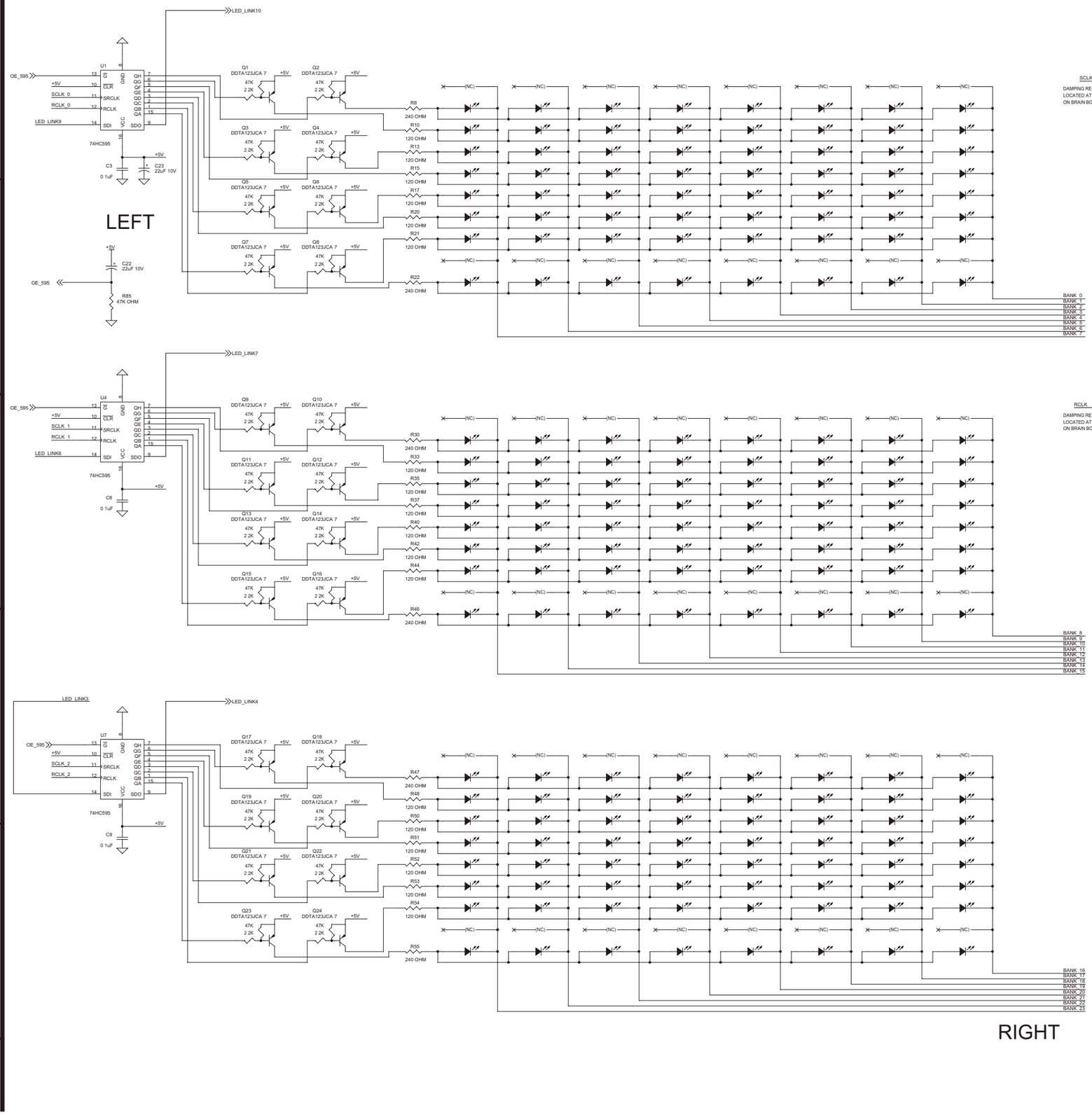
No PCI net can be longer than 1.5". All PCI nets shall be 65-75 ohms.

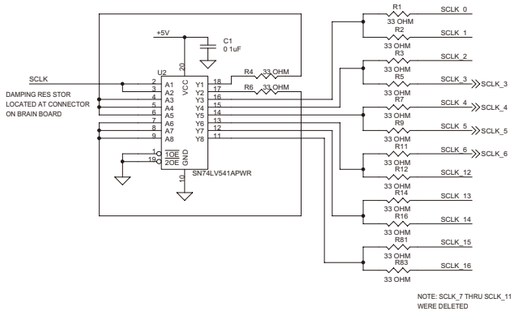
Pull up/down

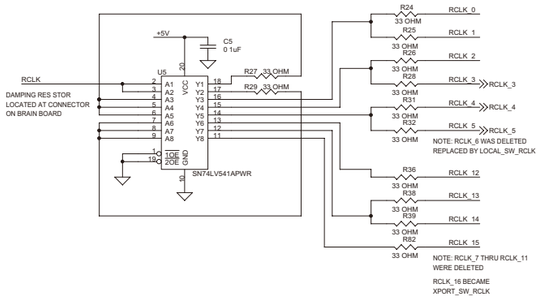
Place within 0.25" of the PCI Fingers. Use 0.02" wide traces to the plane.

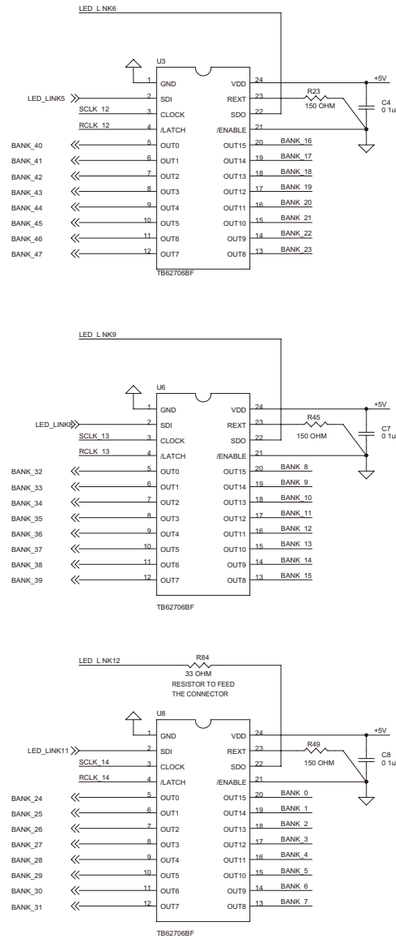

+2.5V
VIO
+3.3V
U20B
PCI9056-BA66
PCI 9056
POWER AND GROUND
2.5VAUX
D7
+2.5V
Card_VAUX
A7
+3.3V
PRESENT_DET
D8
+2.5V
C151 1000pF
C170 1000pF
C171 1000pF
C169 1000pF
C150 0.01uF
C152 0.01uF
C146 0.1uF
C148 1uF
C174 10uF
+3.3V
C154 1000pF
C164 1000pF
C157 1000pF
C167 1000pF
C156 1000pF
C149 1000pF
C165 1000pF
C175 0.01uF
C158 0.01uF
C159 0.01uF
C155 0.1uF
C166 0.1uF
C139 1uF
C178 10uF

Front Panel (1/3) Bargraph LEDs Bottom Row









REVISION HISTORY

07 JUNE 2004 - FROM DESIGN REVIEW IN TOKYO

1. REVISED CLOCK DRIVER CIRCUIT
2. INCORPORATED DRIVER TRANSISTORS WITH BUILT-IN RESISTORS
3. CONVERTED THE 33.2 OHM TO 33 OHM 5% 0603
4. CONVERTED LED CURRENT-SET RESISTORS TO 120 OHM 5%

09 JUNE 2004 - FROM XLS TRACKING FILE

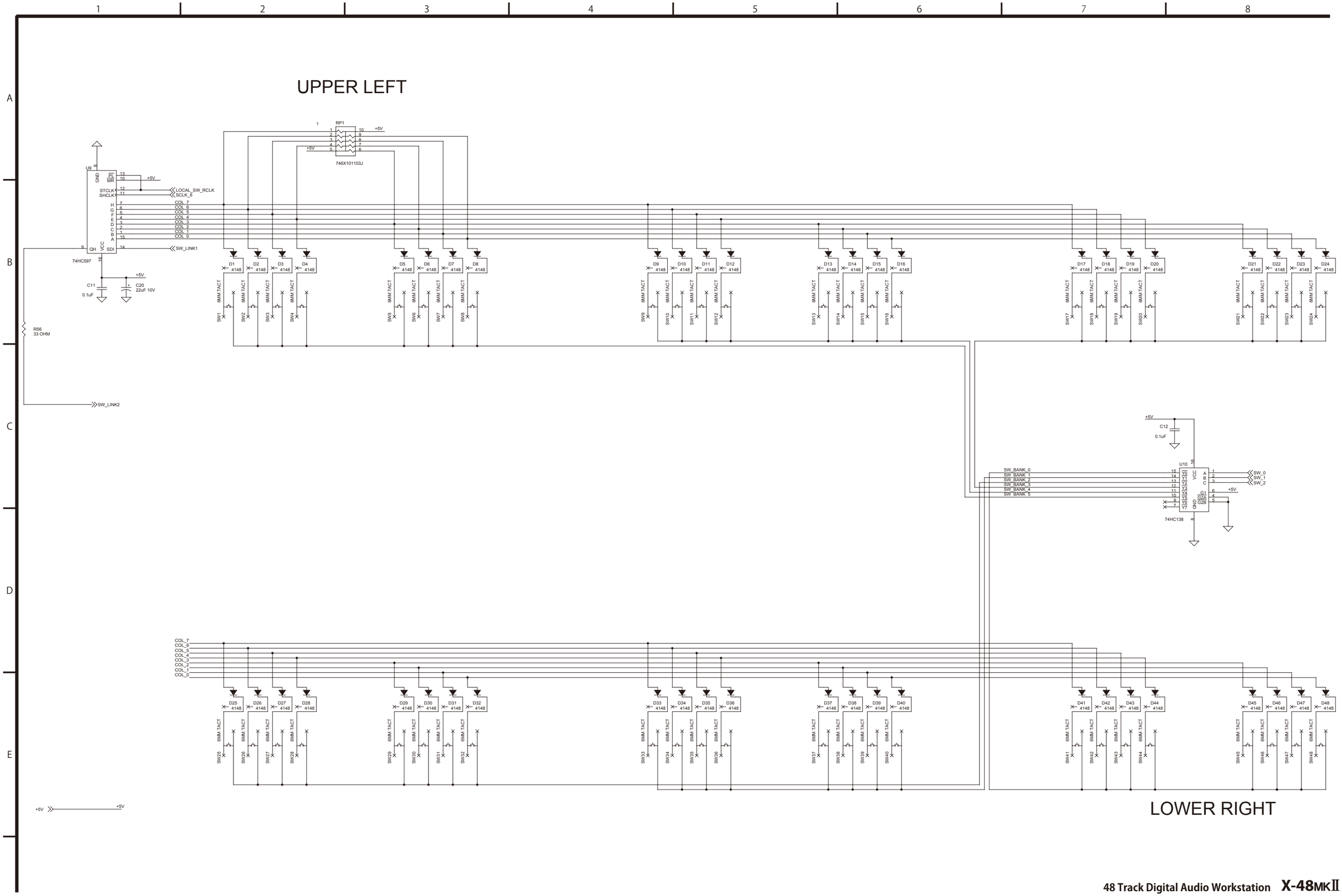
1. CHANGED CLOCK BUFFERS FROM AHC244 TO LV541
2. IMPLEMENTED A MATRIX DESIGN FOR SWITCH SCANNING

10 JUNE 2004

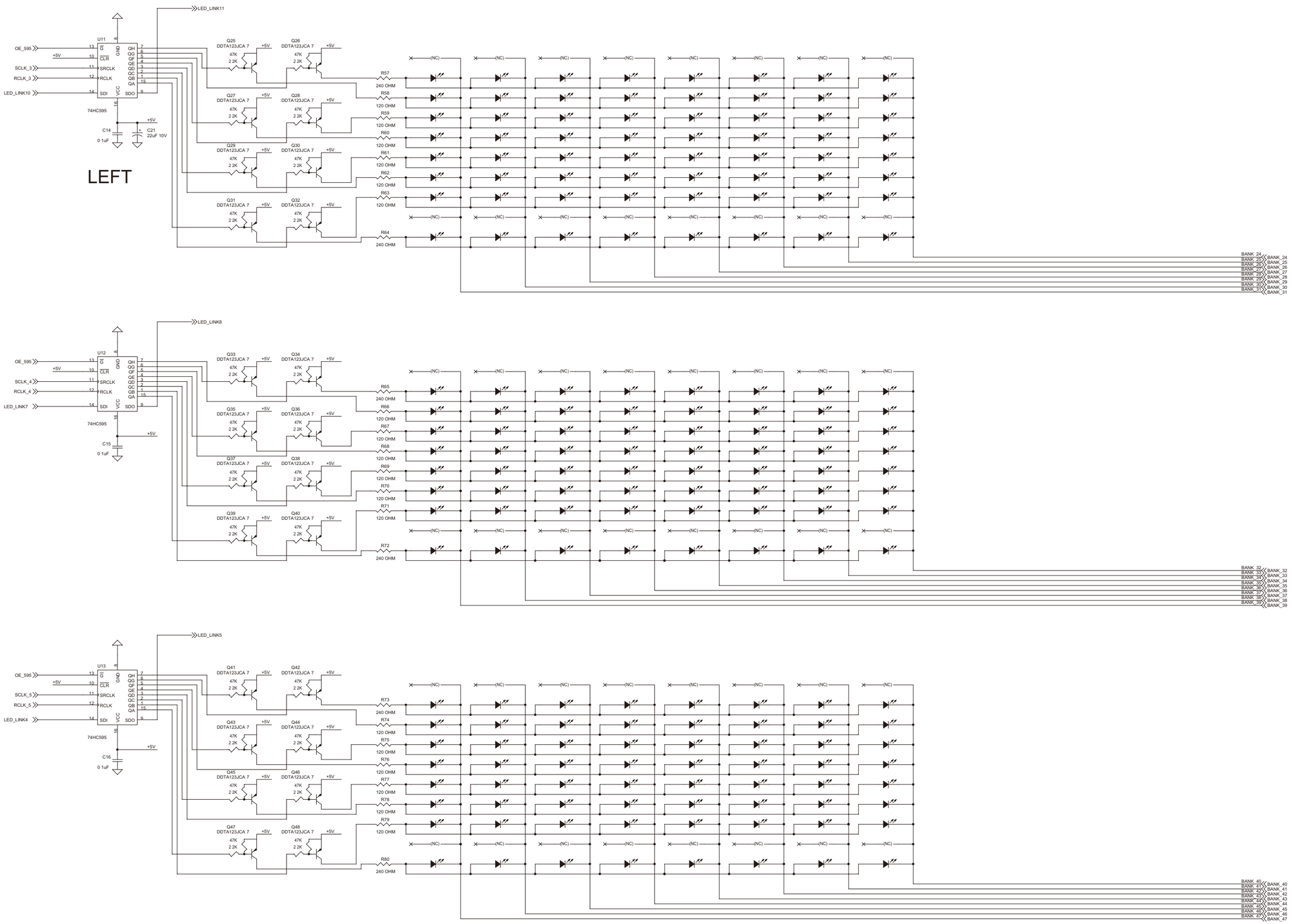
1. REDUCED CLOCK CHIPS COUNT FROM 6 TO 3
2. REVISED SWITCH BANK SELECT FOR FASTER TIMING, ELIMINATE LATENCY ISSUES

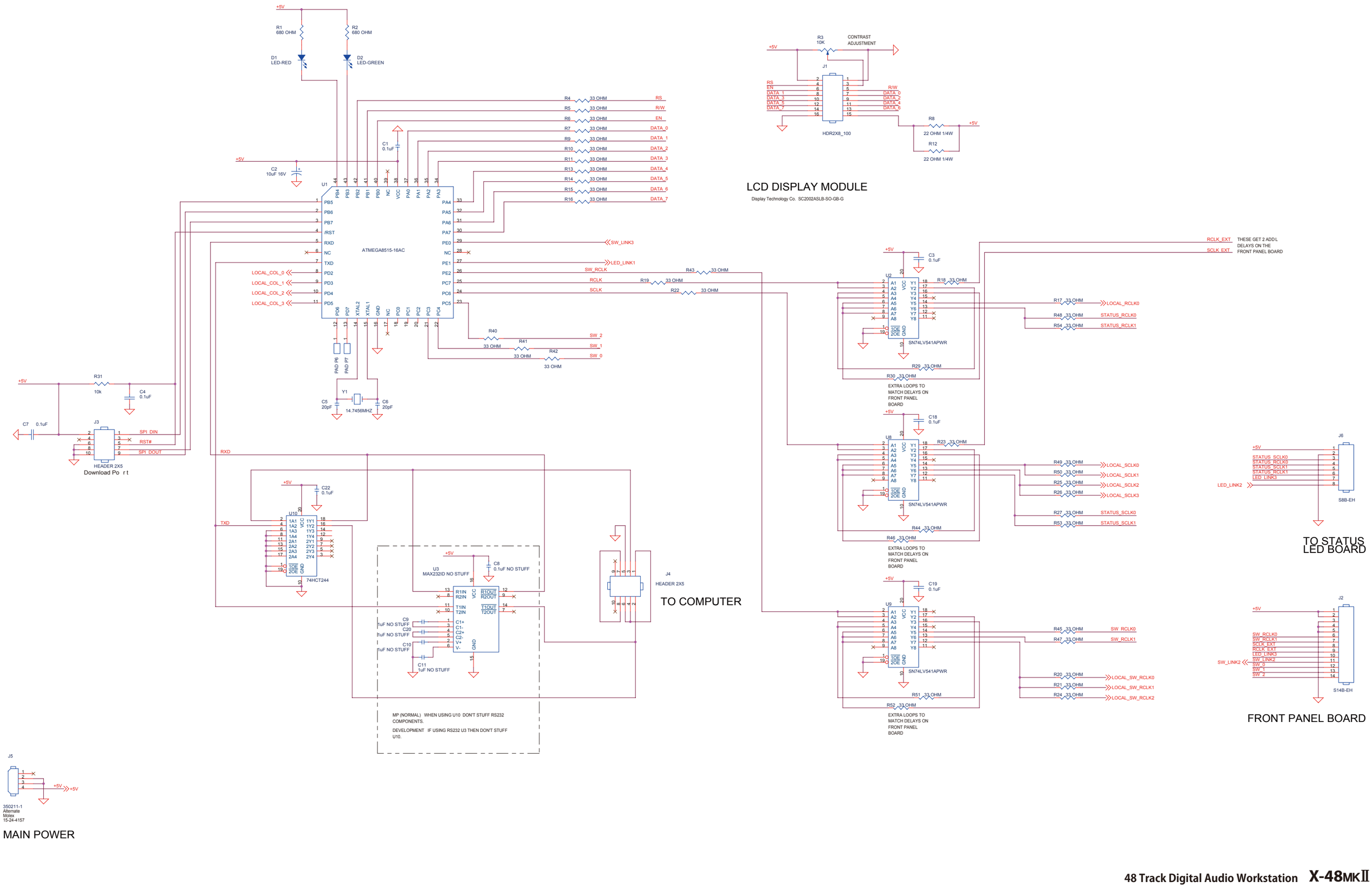
22 JUNE 2004

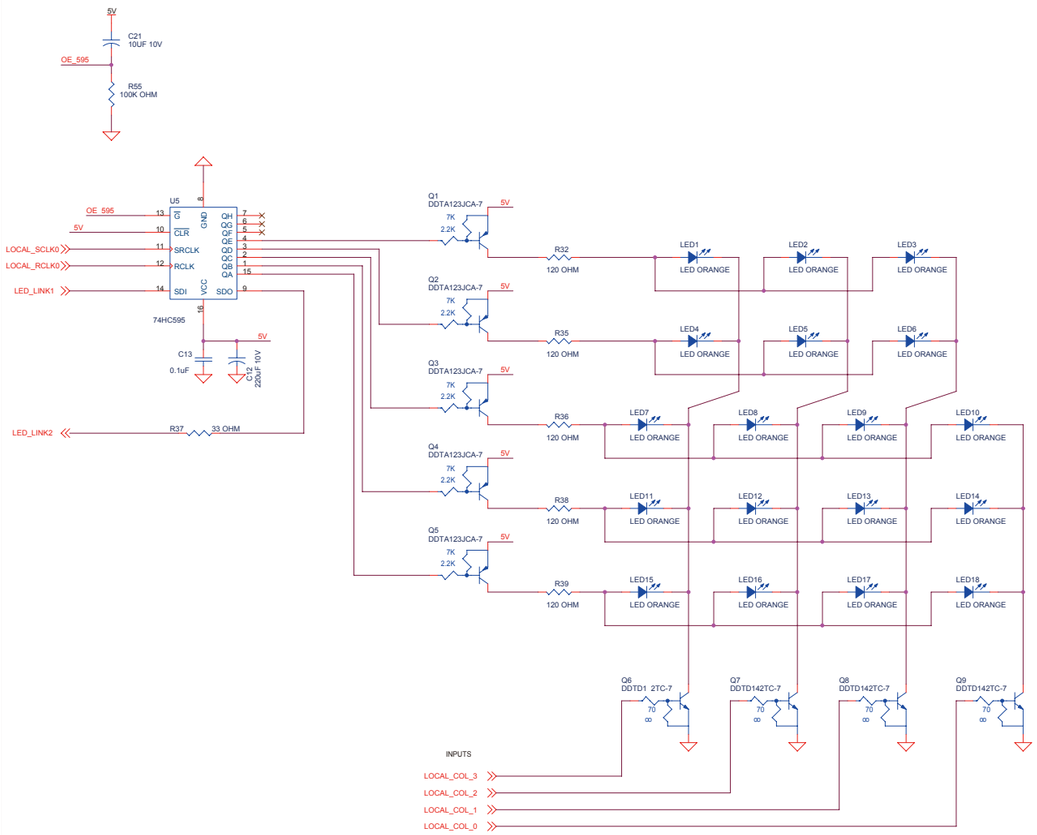
1. REVISED SERIAL AND MUX ORDER FOR OPTIMAL LAYOUT

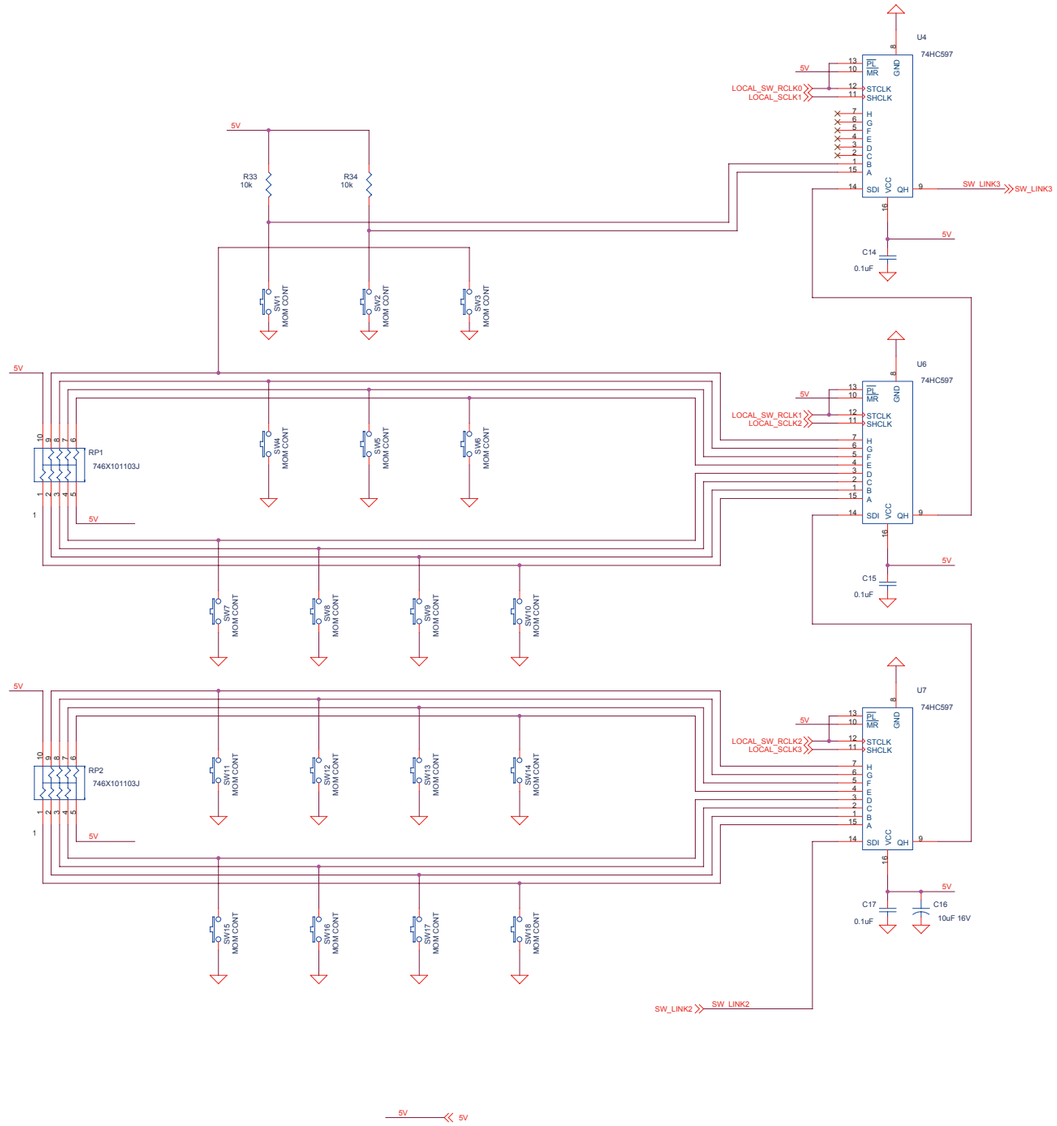

UPPER LEFT
RP1
746X101103J
+5V
U9
74HC597
GND
VCC
PL
MR
STCLK
SHCLK
SDI
QH
LOCAL_SW_RCLK
SCLK_6
SW_LINK1
SW_LINK2
COL_7
COL_6
COL_5
COL_4
COL_3
COL_2
COL_1
COL_0
C11
0.1uF
C20
22uF 10V
R56
33 OHM
D1 4148
D2 4148
D3 4148
D4 4148
D5 4148
D6 4148
D7 4148
D8 4148
D9 4148
D10 4148
D11 4148
D12 4148
D13 4148
D14 4148
D15 4148
D16 4148
D17 4148
D18 4148
D19 4148
D20 4148
D21 4148
D22 4148
D23 4148
D24 4148
6MM TACT
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
SW16
SW17
SW18
SW19
SW20
SW21
SW22
SW23
SW24
C12
0.1uF
U10
74HC138
SW_BANK_0
SW_BANK_1
SW_BANK_2
SW_BANK_3
SW_BANK_4
SW_BANK_5
SW_0
SW_1
SW_2
D25 4148
D26 4148
D27 4148
D28 4148
D29 4148
D30 4148
D31 4148
D32 4148
D33 4148
D34 4148
D35 4148
D36 4148
D37 4148
D38 4148
D39 4148
D40 4148
D41 4148
D42 4148
D43 4148
D44 4148
D45 4148
D46 4148
D47 4148
D48 4148
SW25
SW26
SW27
SW28
SW29
SW30
SW31
SW32
SW33
SW34
SW35
SW36
SW37
SW38
SW39
SW40
SW41
SW42
SW43
SW44
SW45
SW46
SW47
SW48
LOWER RIGHT

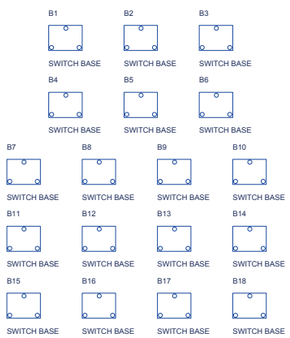
Front Panel (3/3) Bargraph LEDs Top Row



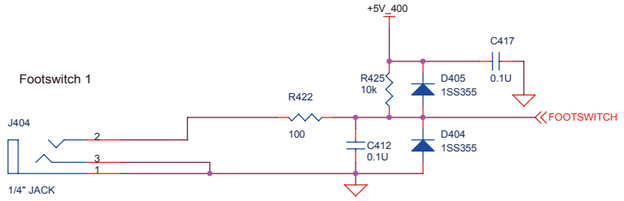

+5V
R1 680 OHM
R2 680 OHM
D1 LED-RED
D2 LED-GREEN
C1 0.1uF
C2 10uF 16V
U1
ATMEGA8515-16AC
PB4 PB3 PB2 PB1 PB0 NC VCC PA0 PA1 PA2 PA3
PB5 PB6 PB7 /RST RXD NC TXD PD2 PD3 PD4 PD5
PA4 PA5 PA6 PA7 PE0 NC PE1 PE2 PC7 PC6 PC5
PD6 PD7 XTAL2 XTAL1 GND NC PC0 PC1 PC2 PC3 PC4
R4 33 OHM RS
R5 33 OHM R/W
R6 33 OHM EN
R7 33 OHM DATA_0
R9 33 OHM DATA_1
R10 33 OHM DATA_2
R11 33 OHM DATA_3
R13 33 OHM DATA_4
R14 33 OHM DATA_5
R15 33 OHM DATA_6
R16 33 OHM DATA_7
SW_LINK3
LED_LINK1
SW_RCLK
RCLK
SCLK
R43 33 OHM
R19 33 OHM
R22 33 OHM
LOCAL_COL_0
LOCAL_COL_1
LOCAL_COL_2
LOCAL_COL_3
R40 SW_2
R41 33 OHM SW_1
R42 33 OHM SW_0
PAD P6
PAD P7
Y1
14.7456MHZ
C5 20pF
C6 20pF
R3 10K CONTRAST ADJUSTMENT
J1
HDR2X8_100
RS EN DATA_1 DATA_3 DATA_5 DATA_7
R/W DATA_0 DATA_2 DATA_4 DATA_6
R8 22 OHM 1/4W
R12 22 OHM 1/4W
LCD DISPLAY MODULE
Display Technology Co. SC2002ASLB-SO-GB-G
C3 0.1uF
U2
SN74LV541APWR
R18 33 OHM
R17 33 OHM LOCAL_RCLK0
R48 33 OHM STATUS_RCLK0
R54 33 OHM STATUS_RCLK1
R29 33 OHM
R30 33 OHM
EXTRA LOOPS TO MATCH DELAYS ON FRONT PANEL BOARD
RCLK_EXT
SCLK_EXT
THESE GET 2 ADD L DELAYS ON THE FRONT PANEL BOARD
C18 0.1uF
U8
SN74LV541APWR
R23 33 OHM
R49 33 OHM LOCAL_SCLK0
R50 33 OHM LOCAL_SCLK1
R25 33 OHM LOCAL_SCLK2
R26 33 OHM LOCAL_SCLK3
R27 33 OHM STATUS_SCLK0
R53 33 OHM STATUS_SCLK1
R44 33 OHM
R46 33 OHM
EXTRA LOOPS TO MATCH DELAYS ON FRONT PANEL BOARD
C19 0.1uF
U9
SN74LV541APWR
R45 33 OHM SW_RCLK0
R47 33 OHM SW_RCLK1
R20 33 OHM LOCAL_SW_RCLK0
R21 33 OHM LOCAL_SW_RCLK1
R24 33 OHM LOCAL_SW_RCLK2
R51 33 OHM
R52 33 OHM
EXTRA LOOPS TO MATCH DELAYS ON FRONT PANEL BOARD
J6
S8B-EH
STATUS_SCLK0 STATUS_RCLK0 STATUS_SCLK1 STATUS_RCLK1 LED_LINK3 LED_LINK2
TO STATUS LED BOARD
J2
S14B-EH
SW_RCLK0 SW_RCLK1 SCLK_EXT RCLK_EXT LED_LINK3 SW_LINK2 SW_0 SW_1 SW_2 SW_LINK2
FRONT PANEL BOARD
R31 10k
C4 0.1uF
C7 0.1uF
J3
HEADER 2X5
Download Port
SPI_DIN RST# SPI_DOUT
RXD
TXD
C22 0.1uF
U10
74HCT244
U3 MAX232ID NO STUFF
C8 0.1uF NO STUFF
R1IN R2IN T1IN T2IN R1OUT R2OUT T1OUT T2OUT C1+ C1- C2+ C2- V+ V-
C9 1uF NO STUFF
C20 1uF NO STUFF
C10 1uF NO STUFF
C11 1uF NO STUFF
MP (NORMAL) WHEN USING U10 DON'T STUFF RS232 COMPONENTS.
DEVELOPMENT IF USING RS232 U3 THEN DON'T STUFF U10.
J4
HEADER 2X5
TO COMPUTER
J5
350211-1
Alternate
Molex
15-24-4157
MAIN POWER


5V
C21
10UF 10V
OE_595
R55
100K OHM
U5
74HC595
OE_595
LOCAL_SCLK0
LOCAL_RCLK0
LED_LINK1
LED_LINK2
SRCLK
RCLK
SDI
SDO
C13
0.1uF
C12
220uF 10V
R37
33 OHM
Q1
DDTA123JCA-7
Q2
DDTA123JCA-7
Q3
DDTA123JCA-7
Q4
DDTA123JCA-7
Q5
DDTA123JCA-7
7K
2.2K
R32
R35
R36
R38
R39
120 OHM
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
LED9
LED10
LED11
LED12
LED13
LED14
LED15
LED16
LED17
LED18
LED ORANGE
Q6
DDTD1 2TC-7
Q7
DDTD142TC-7
Q8
DDTD142TC-7
Q9
DDTD142TC-7
INPUTS
LOCAL_COL_3
LOCAL_COL_2
LOCAL_COL_1
LOCAL_COL_0

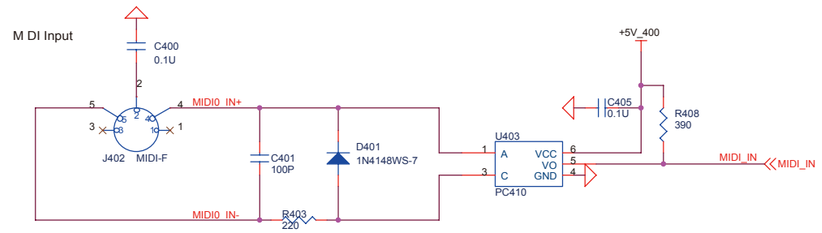

U4
74HC597
U6
74HC597
U7
74HC597
LOCAL_SW_RCLK0
LOCAL_SW_RCLK1
LOCAL_SW_RCLK2
LOCAL_SCLK1
LOCAL_SCLK2
LOCAL_SCLK3
STCLK
SHCLK
SW_LINK3
SW_LINK2
C14
C15
C16
10uF 16V
C17
0.1uF
R33
10k
R34
10k
RP1
746X101103J
RP2
746X101103J
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
SW16
SW17
SW18
MOM CONT


B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
B16
B17
B18
SWITCH BASE

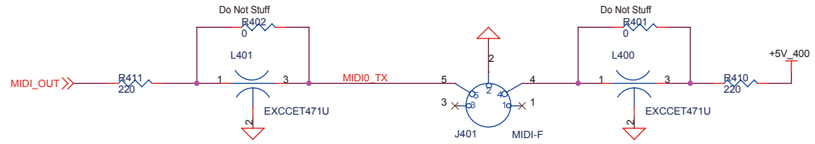
Footswitch 1



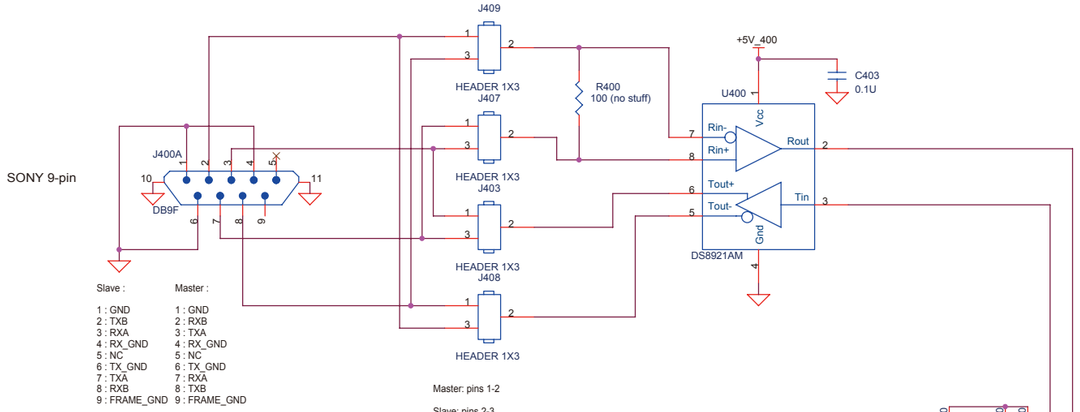
M DI Input

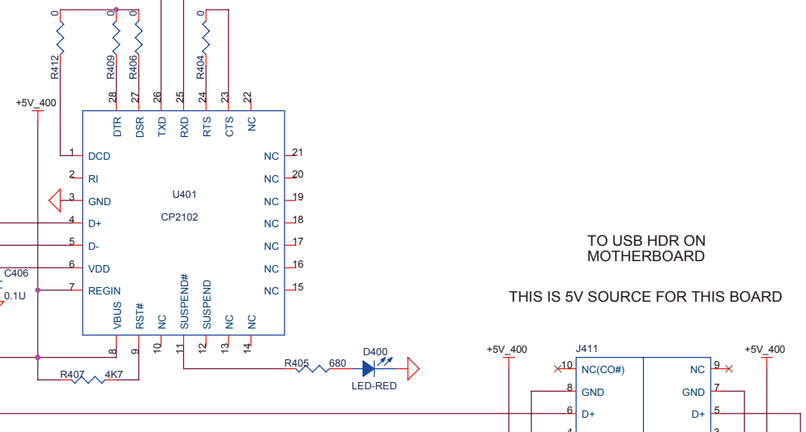


MIDI Output



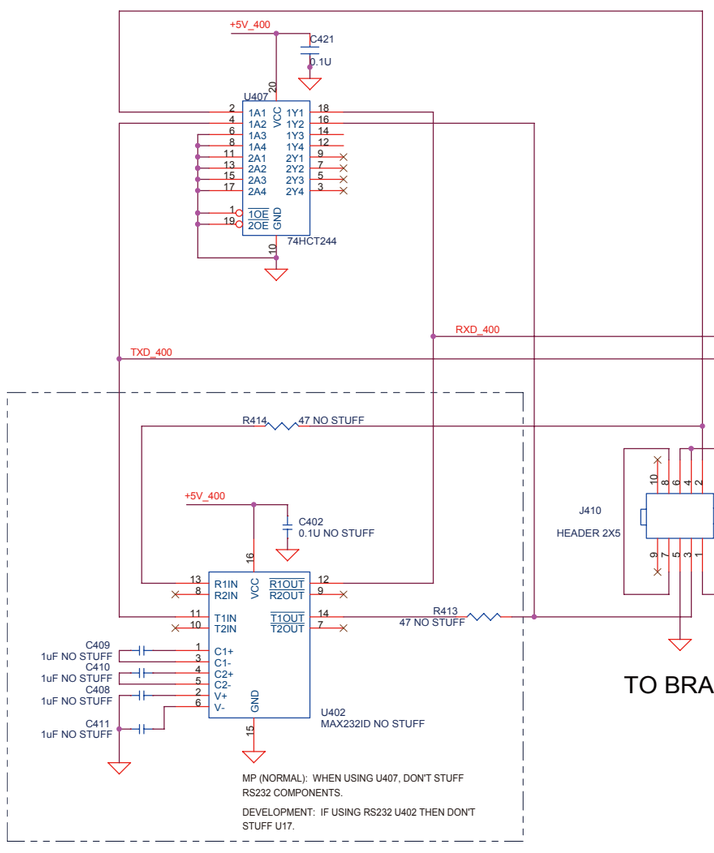
SONY 9-pin

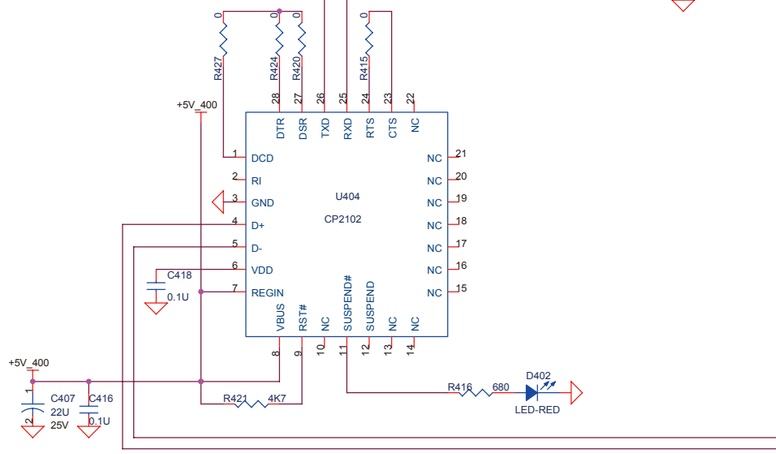


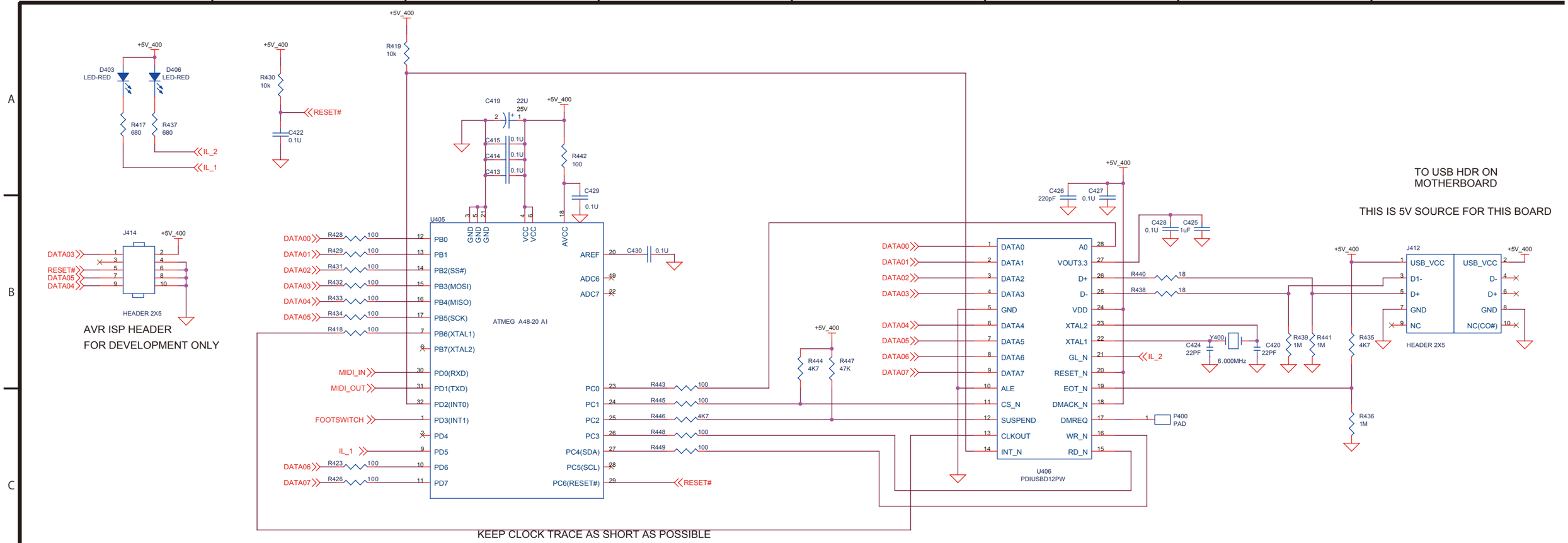


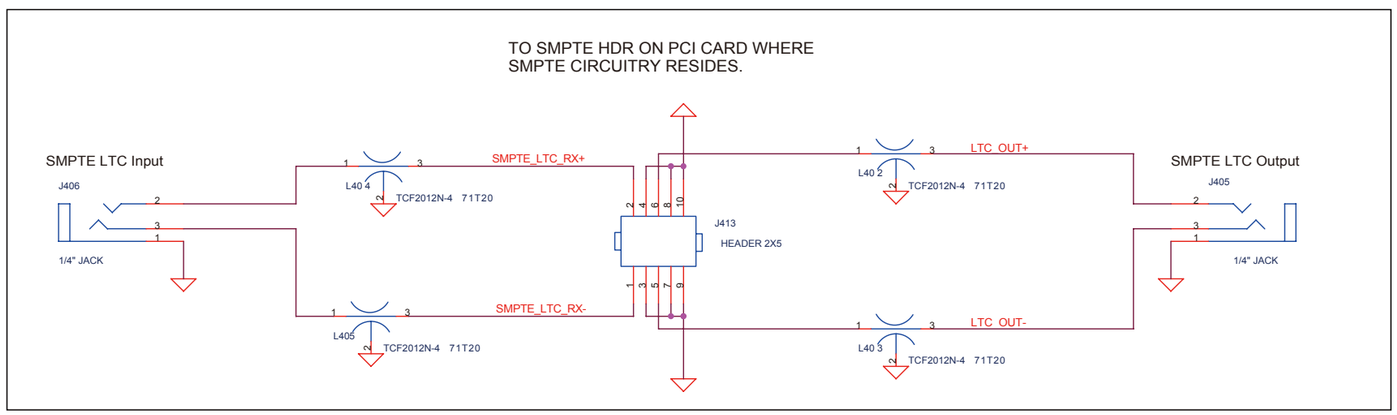
TO USB HDR ON MOTHERBOARD

THIS IS 5V SOURCE FOR THIS BOARD

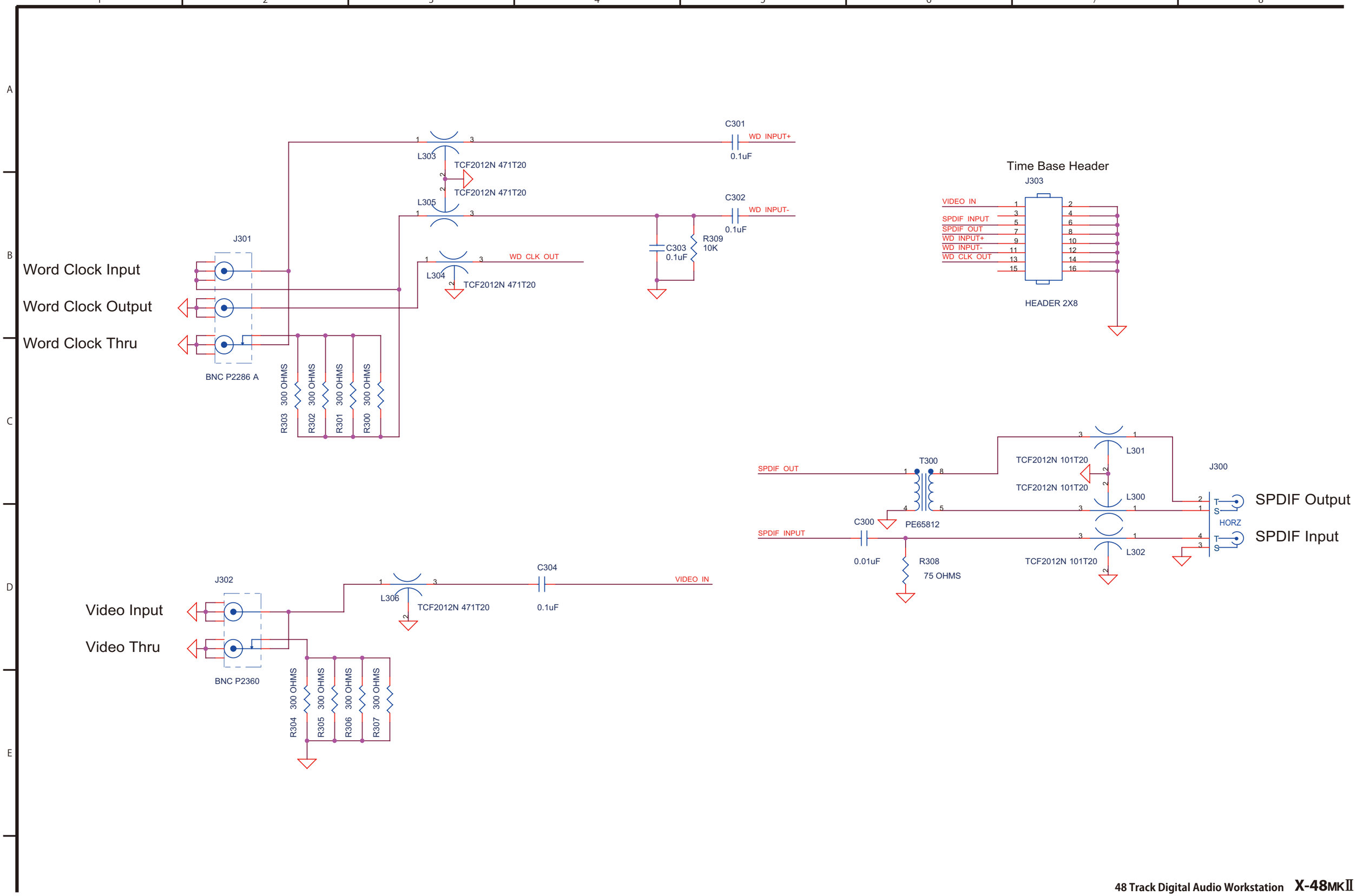




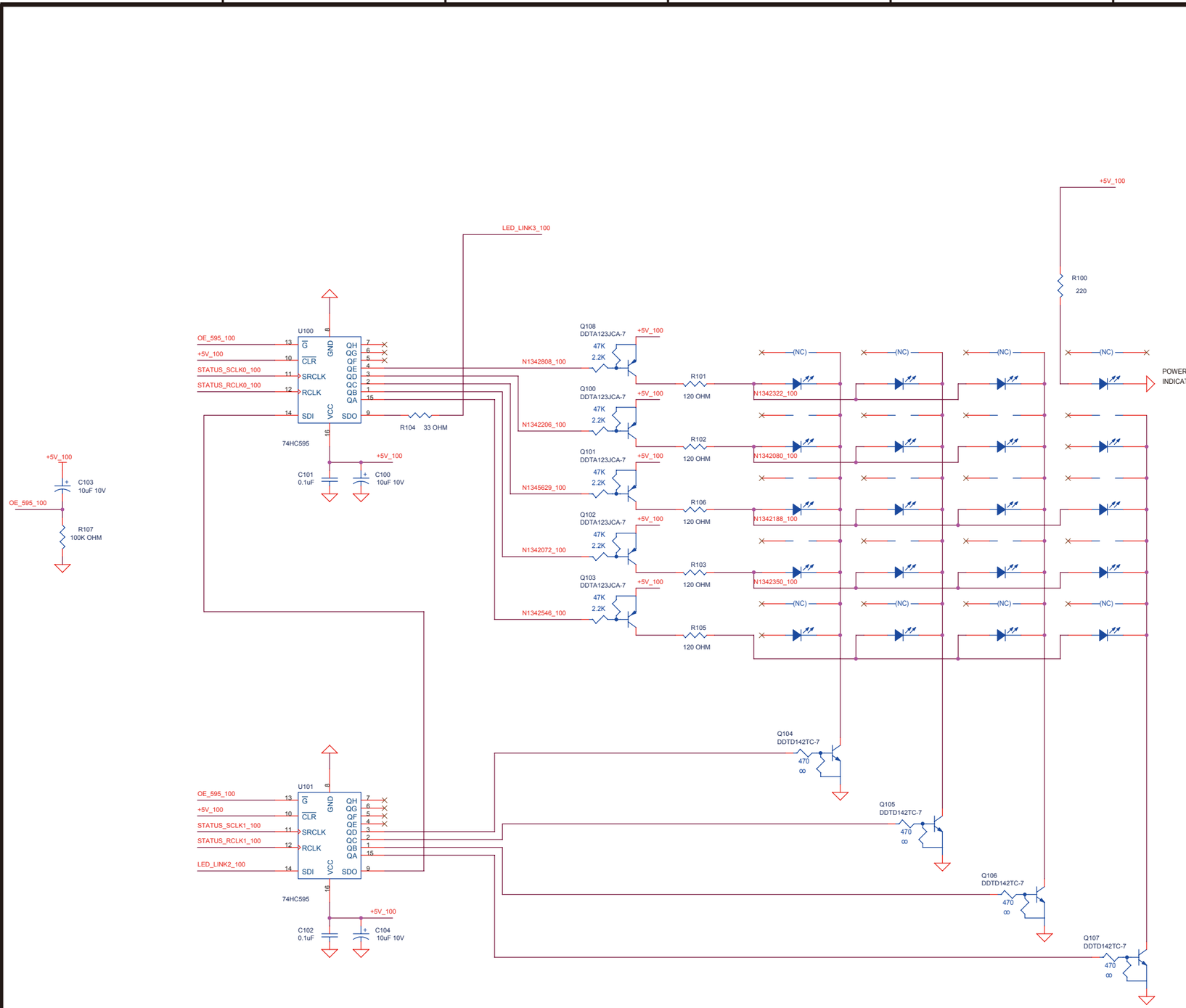

+5V_400
D403 LED-RED
D406 LED-RED
R417 680
R437 680
IL_2
IL_1
R430 10k
RESET#
C422 0.1U
R419 10k
C419 22U 25V
C415 0.1U
C414 0.1U
C413 0.1U
R442 100
C429 0.1U
U405
GND GND GND VCC VCC AVCC
ATMEG A48-20 AI
AREF
C430 0.1U
ADC6
ADC7
PB0
PB1
PB2(SS#)
PB3(MOSI)
PB4(MISO)
PB5(SCK)
PB6(XTAL1)
PB7(XTAL2)
PD0(RXD)
PD1(TXD)
PD2(INT0)
PD3(INT1)
PD4
PD5
PD6
PD7
PC0
PC1
PC2
PC3
PC4(SDA)
PC5(SCL)
PC6(RESET#)
DATA00
DATA01
DATA02
DATA03
DATA04
DATA05
DATA06
DATA07
MIDI_IN
MIDI_OUT
FOOTSWITCH
R428 100
R429 100
R431 100
R432 100
R433 100
R434 100
R418 100
R423 100
R426 100
R443 100
R445 100
R446 4K7
R448 100
R449 100
R444 4K7
R447 47K
J414
HEADER 2X5
AVR ISP HEADER
FOR DEVELOPMENT ONLY
KEEP CLOCK TRACE AS SHORT AS POSSIBLE
C426 220pF
C427 0.1U
C428 0.1U
C425 1uF
U406
PDIUSBD12PW
A0
VOUT3.3
D+
D-
VDD
XTAL2
XTAL1
GL_N
RESET_N
EOT_N
DMACK_N
DMREQ
WR_N
RD_N
R440 18
R438 18
Y400
6.000MHz
C424 22PF
C420 22PF
R439 1M
R441 1M
R435 4K7
R436 1M
P400 PAD
TO USB HDR ON MOTHERBOARD
THIS IS 5V SOURCE FOR THIS BOARD
J412
USB_VCC
D1-
D+
GND
NC
NC(CO#)
HEADER 2X5

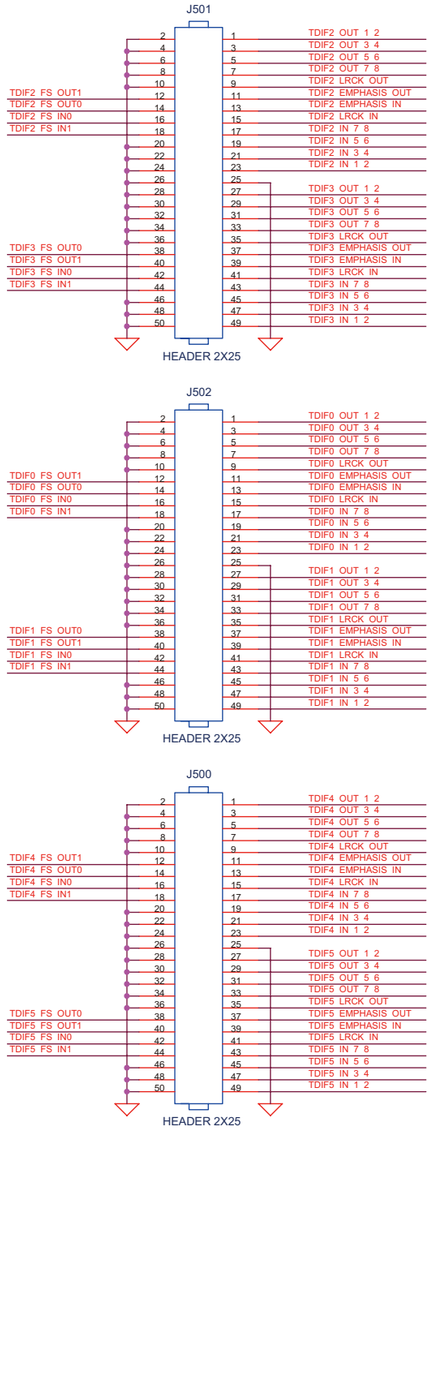

TO SMPTE HDR ON PCI CARD WHERE
SMPTE CIRCUITRY RESIDES.
SMPTE LTC Input
J406
1/4" JACK
L404 TCF2012N-4 71T20
L405 TCF2012N-4 71T20
SMPTE_LTC_RX+
SMPTE_LTC_RX-
J413
HEADER 2X5
L402 TCF2012N-4 71T20
L403 TCF2012N-4 71T20
LTC_OUT+
LTC_OUT-
SMPTE LTC Output
J405
1/4" JACK

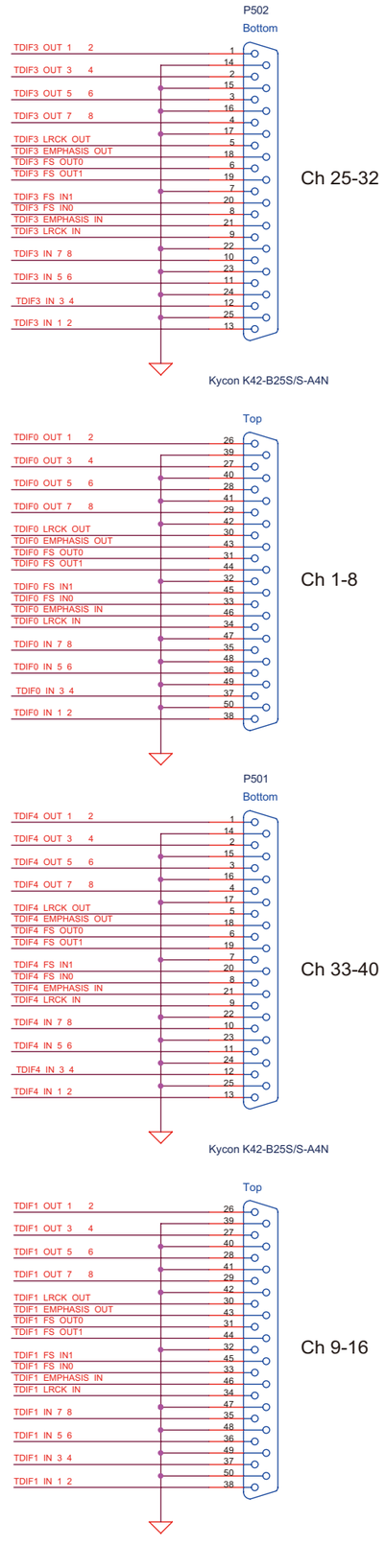
Clock


1
2
3
4
5
6
7
8
A
B
C
D
E
Word Clock Input
Word Clock Output
Word Clock Thru
J301
BNC P2286 A
R303 300 OHMS
R302 300 OHMS
R301 300 OHMS
R300 300 OHMS
L303
TCF2012N 471T20
L305
TCF2012N 471T20
L304
TCF2012N 471T20
WD CLK OUT
C301
0.1uF
WD INPUT+
C302
0.1uF
WD INPUT-
C303
0.1uF
R309
10K
Time Base Header
J303
VIDEO IN
SPDIF INPUT
SPDIF OUT
WD INPUT+
WD INPUT-
WD CLK OUT
HEADER 2X8
Video Input
Video Thru
J302
BNC P2360
R304 300 OHMS
R305 300 OHMS
R306 300 OHMS
R307 300 OHMS
L306
TCF2012N 471T20
C304
0.1uF
VIDEO IN
SPDIF OUT
SPDIF INPUT
T300
PE65812
C300
0.01uF
R308
75 OHMS
L301
TCF2012N 101T20
L300
TCF2012N 101T20
L302
TCF2012N 101T20
J300
HORZ
SPDIF Output
SPDIF Input

Status LED


+5V_100
C103
10uF 10V
OE_595_100
R107
100K OHM
LED_LINK3_100
U100
OE_595_100
+5V_100
STATUS_SCLK0_100
STATUS_RCLK0_100
LED_LINK2_100
G
CLR
SRCLK
RCLK
SDI
VCC
GND
SDO
QH
QG
QF
QE
QD
QC
QB
QA
74HC595
R104 33 OHM
C101
0.1uF
C100
10uF 10V
U101
C102
0.1uF
C104
10uF 10V
N1342808_100
N1342206_100
N1345629_100
N1342072_100
N1342546_100
Q108
DDTA123JCA-7
Q100
Q101
Q102
Q103
47K
2.2K
R101
120 OHM
R102
R106
R103
R105
N1342322_100
N1342080_100
N1342188_100
N1342350_100
(NC)
R100
220
POWER ON
INDICATOR
Q104
DDTD142TC-7
Q105
Q106
Q107
470
∞
J100
POWER SWITCH
6MM TACT
SW100
S2B-EH
J101
STATUS_SCLK0_100
STATUS_RCLK0_100
STATUS_SCLK1_100
STATUS_RCLK1_100
LED_LINK3_100
LED_LINK2_100
S8B-EH
FROM BRAIN BOARD



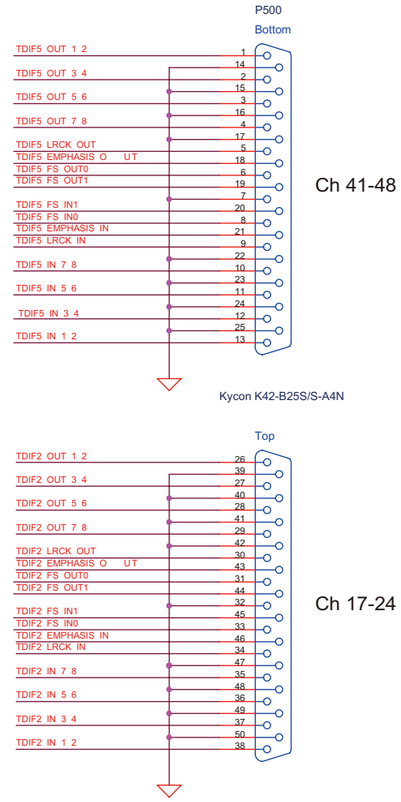


Ch 25-32

Ch 1-8

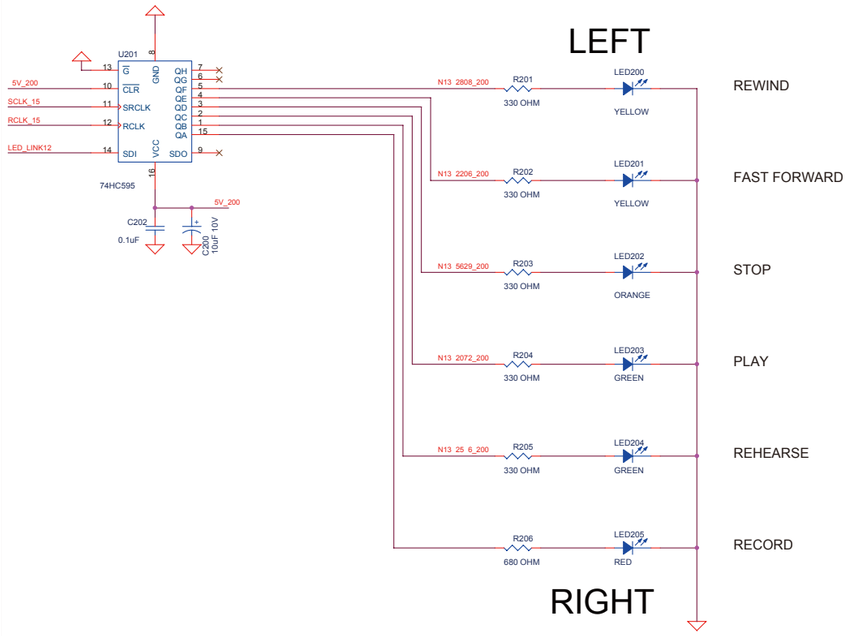
Ch 33-40

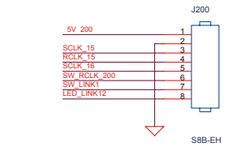
Ch 9-16



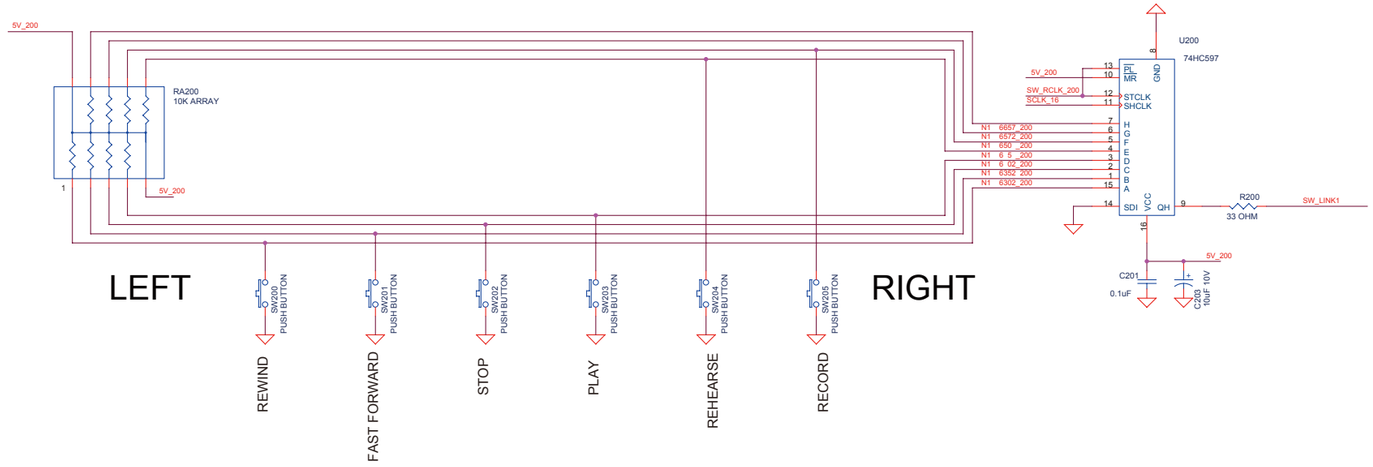
Ch 41-48

Ch 17-24

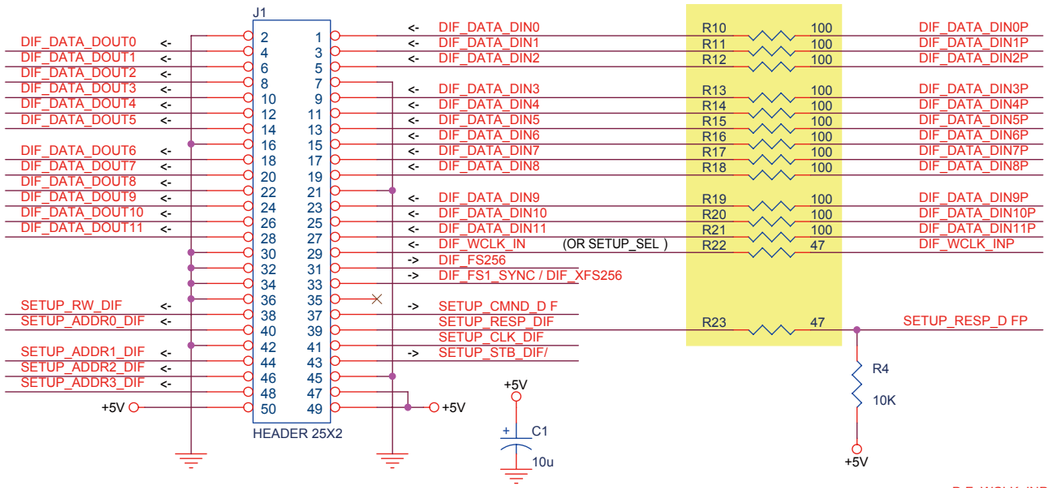


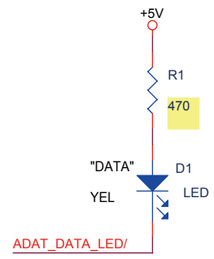


FROM FRONT PANEL BOARD

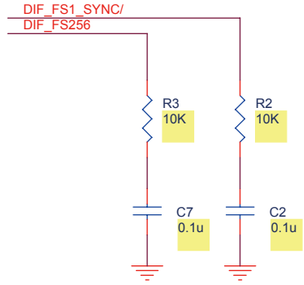


MDX MAIN

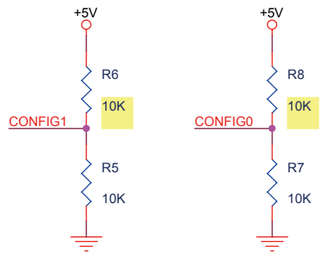




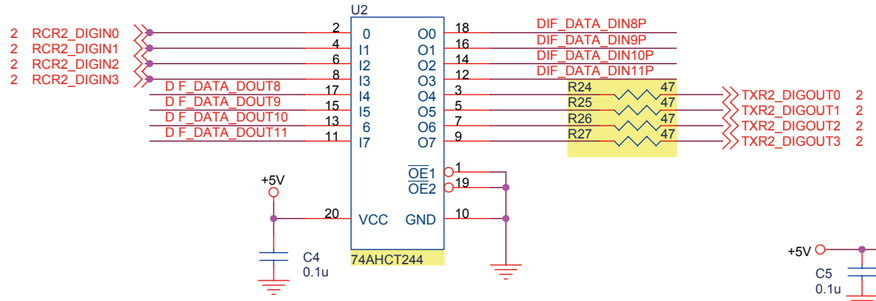
R2,R3 : Don't stuff

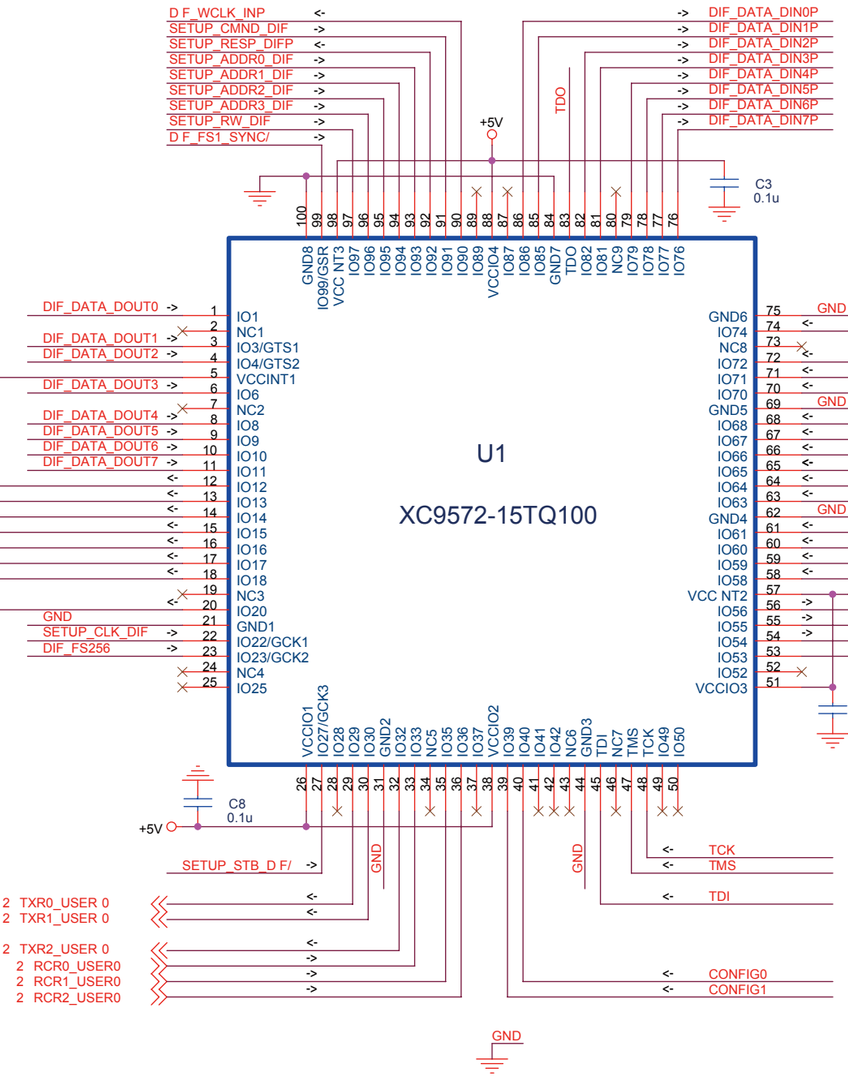


R6,R8 : Don't stuff

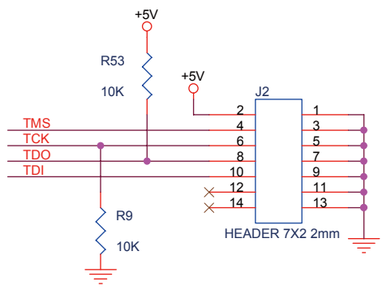


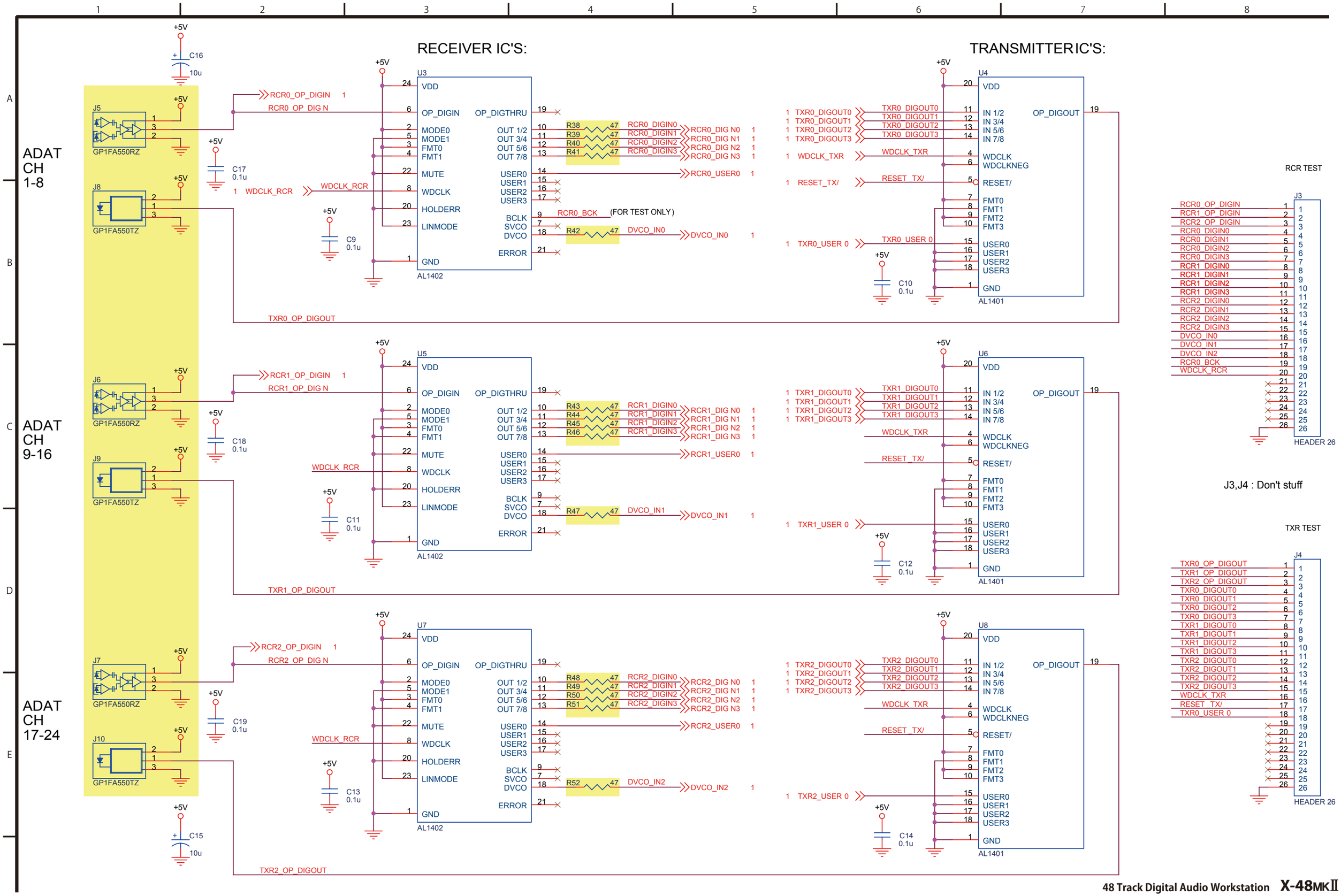
C2,C7 : Don't stuff



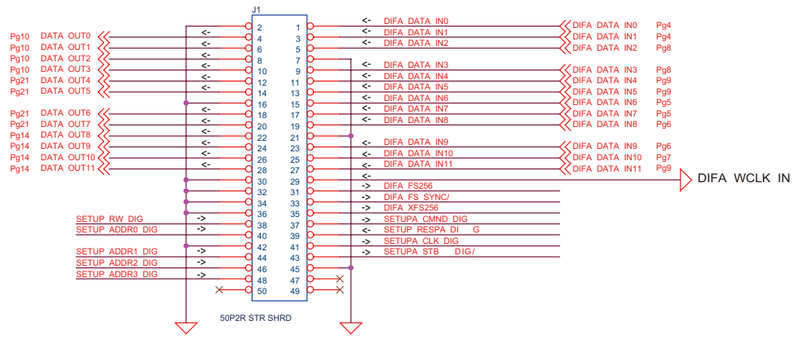


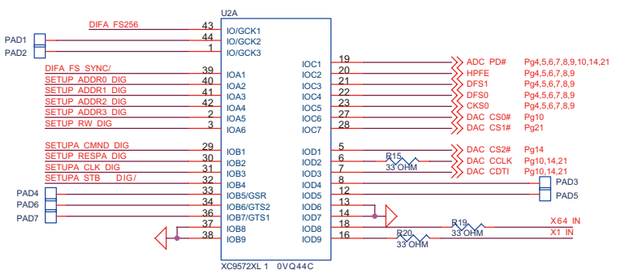
Parallel cable IV connector for CPLD

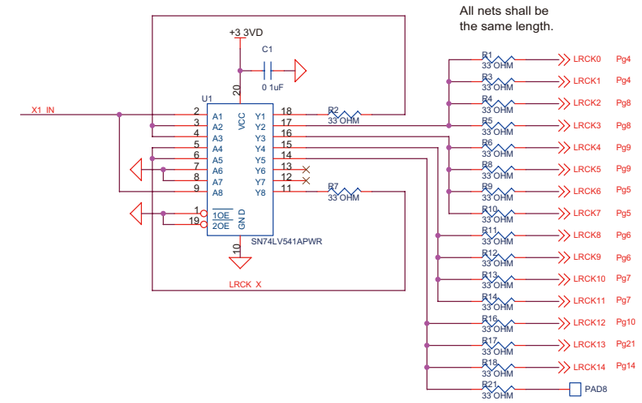


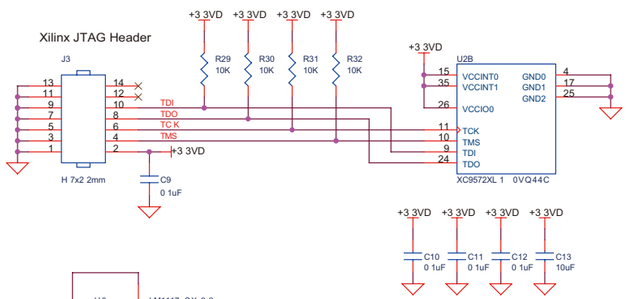

RECEIVER IC'S:
TRANSMITTER IC'S:
ADAT CH 1-8
ADAT CH 9-16
ADAT CH 17-24
U3
U4
U5
U6
U7
U8
AL1402
AL1401
GP1FA550RZ
GP1FA550TZ
RCR0_OP_DIGIN
RCR0_OP_DIG N
WDCLK_RCR
TXR0_OP_DIGOUT
RCR1_OP_DIGIN
RCR1_OP_DIG N
TXR1_OP_DIGOUT
RCR2_OP_DIGIN
RCR2_OP_DIG N
TXR2_OP_DIGOUT
RCR0_BCK (FOR TEST ONLY)
DVCO_IN0
DVCO_IN1
DVCO_IN2
RCR0_USER0
RCR1_USER0
RCR2_USER0
TXR0_USER 0
TXR1_USER 0
TXR2_USER 0
RESET_TX/
WDCLK_TXR
RCR TEST
HEADER 26
J3,J4 : Don't stuff
TXR TEST

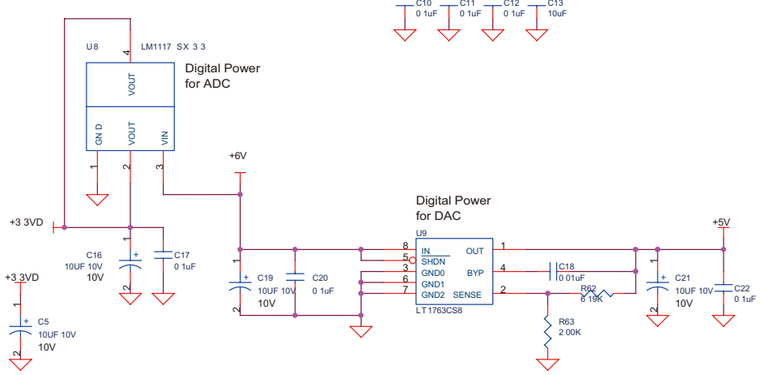
DIGITAL IN AND DIGITAL OUT

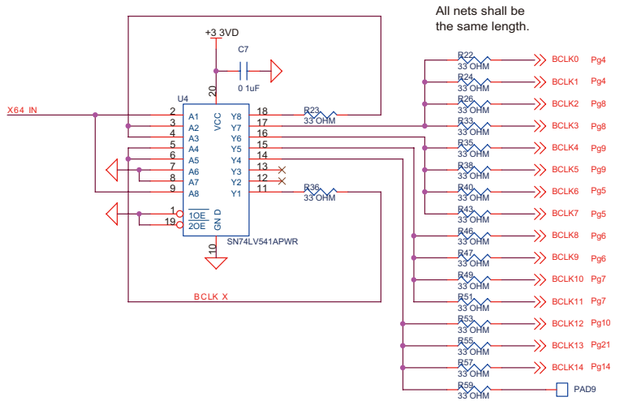


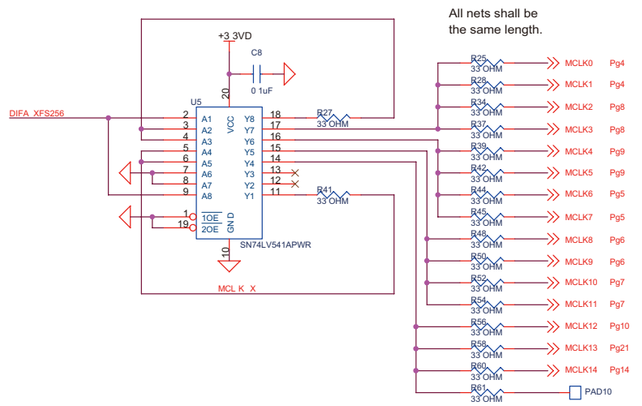




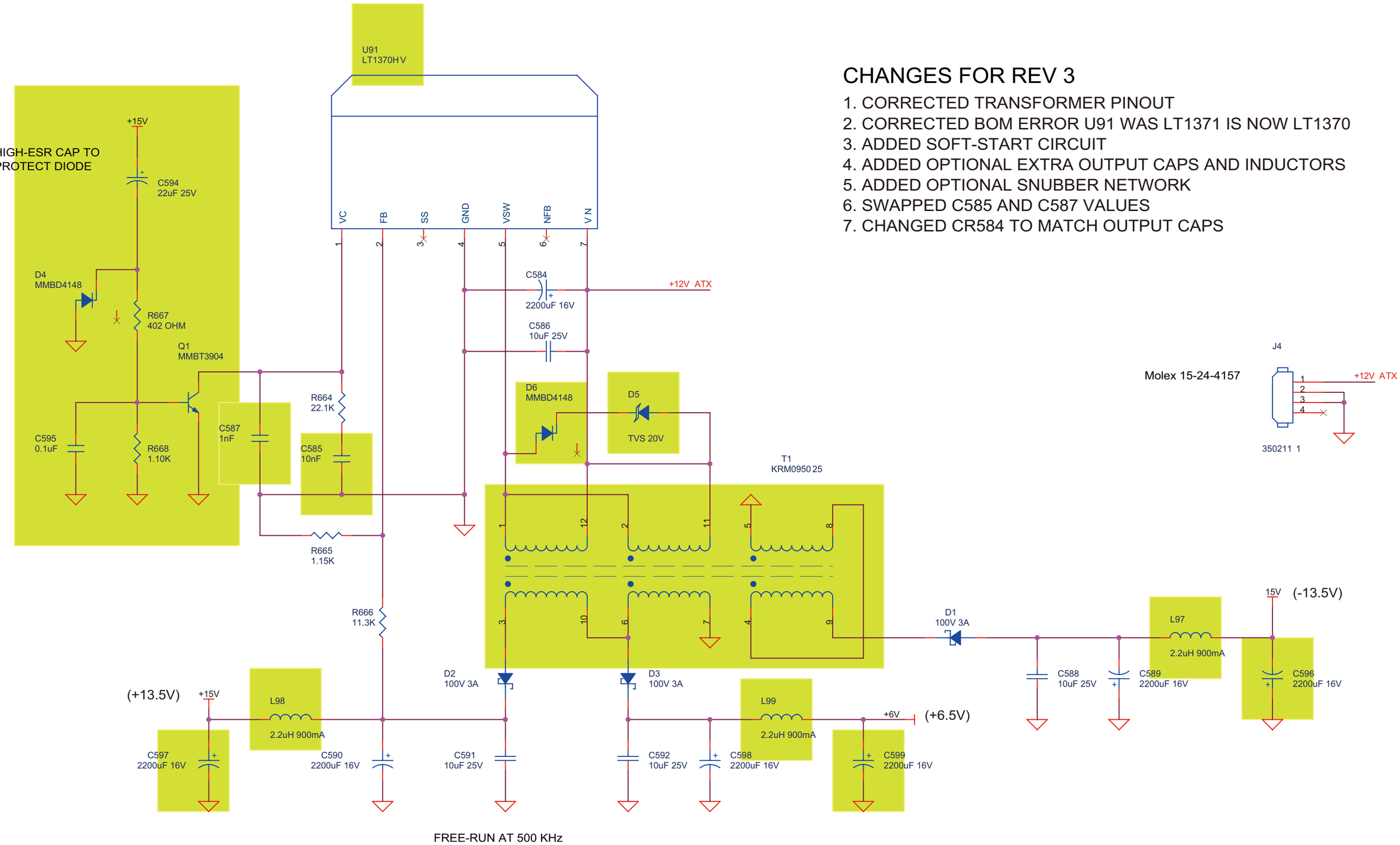








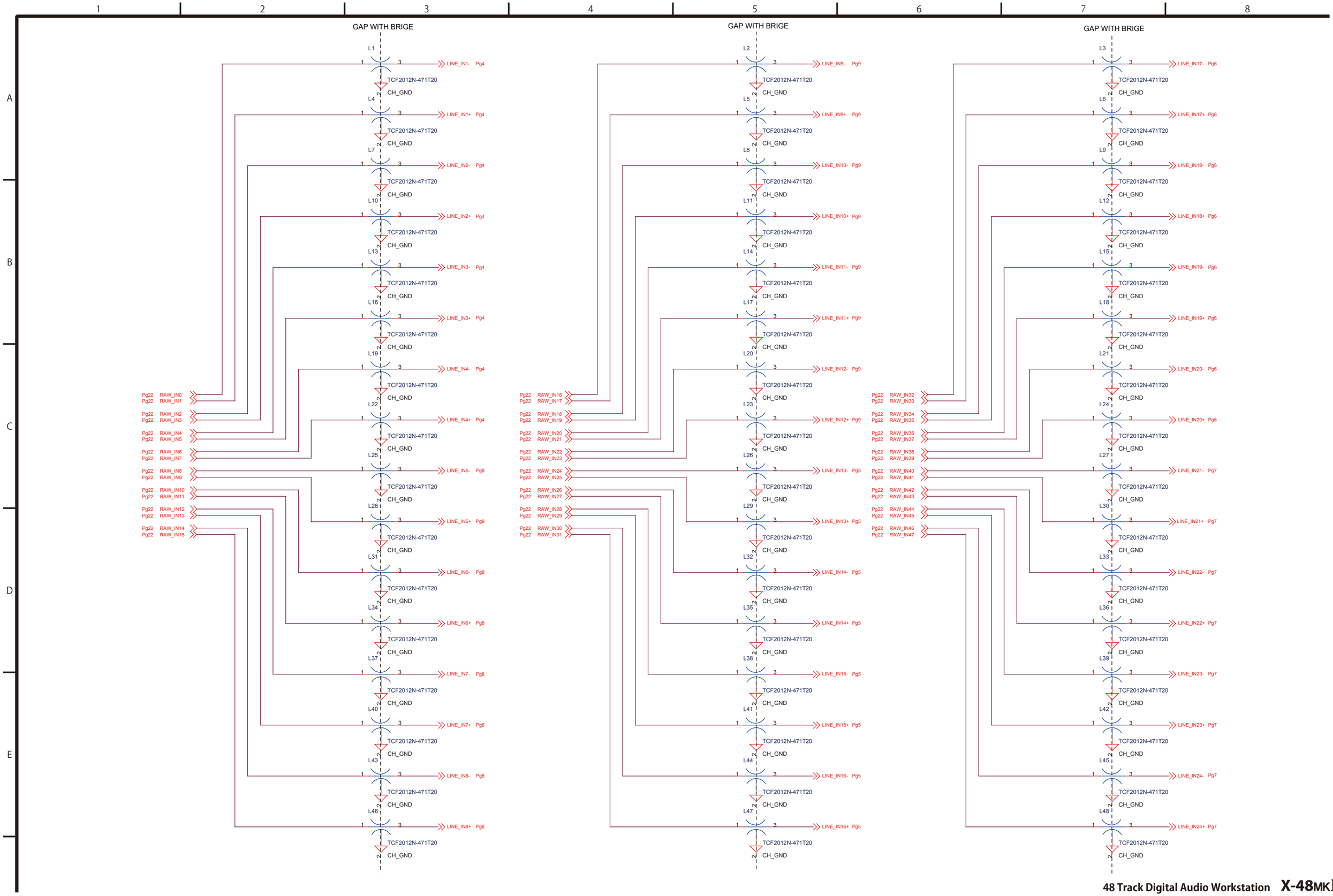
CH GND AGND



CHANGES FOR REV 3

1. CORRECTED TRANSFORMER PINOUT
2. CORRECTED BOM ERROR U91 WAS LT1371 IS NOW LT1370
3. ADDED SOFT-START CIRCUIT
4. ADDED OPTIONAL EXTRA OUTPUT CAPS AND INDUCTORS
5. ADDED OPTIONAL SNUBBER NETWORK
6. SWAPPED C585 AND C587 VALUES
7. CHANGED CR584 TO MATCH OUTPUT CAPS

IF-AN24X (3/22) Line In Filters



IF-AN24X (4/22) Line In 1-4

-3dB @ 40KHZ

Z_IN = 10K

-3dB @ 0.67 HZ

TAU = 400nS

2.9Vpp

Pg3 LINE_IN1-
Pg3 LINE_IN1+
Pg3 LINE_IN2-
Pg3 LINE_IN2+
Pg3 LINE_IN3-
Pg3 LINE_IN3+
Pg3 LINE_IN4-
Pg3 LINE_IN4+

C30 C40 C45 C51 C61 C66 C76 C80 22uf 25V
R67 R73 R78 R84 R90 R95 R99 R103 10.7K
R69 R75 R80 R88 R93 R97 R101 R105 154K
R64 R72 R77 R82 R89 R94 R98 R102 1.58K
C29 C37 C43 C48 C57 C64 C75 C79 1000pF
U11A U11B U14A U14B U16A U16B U18A U18B NE5532DR
-15V +15V AGND
VBIAS1
C36 C47 C63 C78 0.01uF
R68 R74 R79 R85 R92 R96 R100 R104 91 OHM
C35 C46 C62 C77 1000pF

U12 QSBT40
U17 QSBT40
+5VA1 AGND

R81 22.1K
R83 22.1K
C49 0.1uF
C50 10UF 10V 10V
VBIAS1

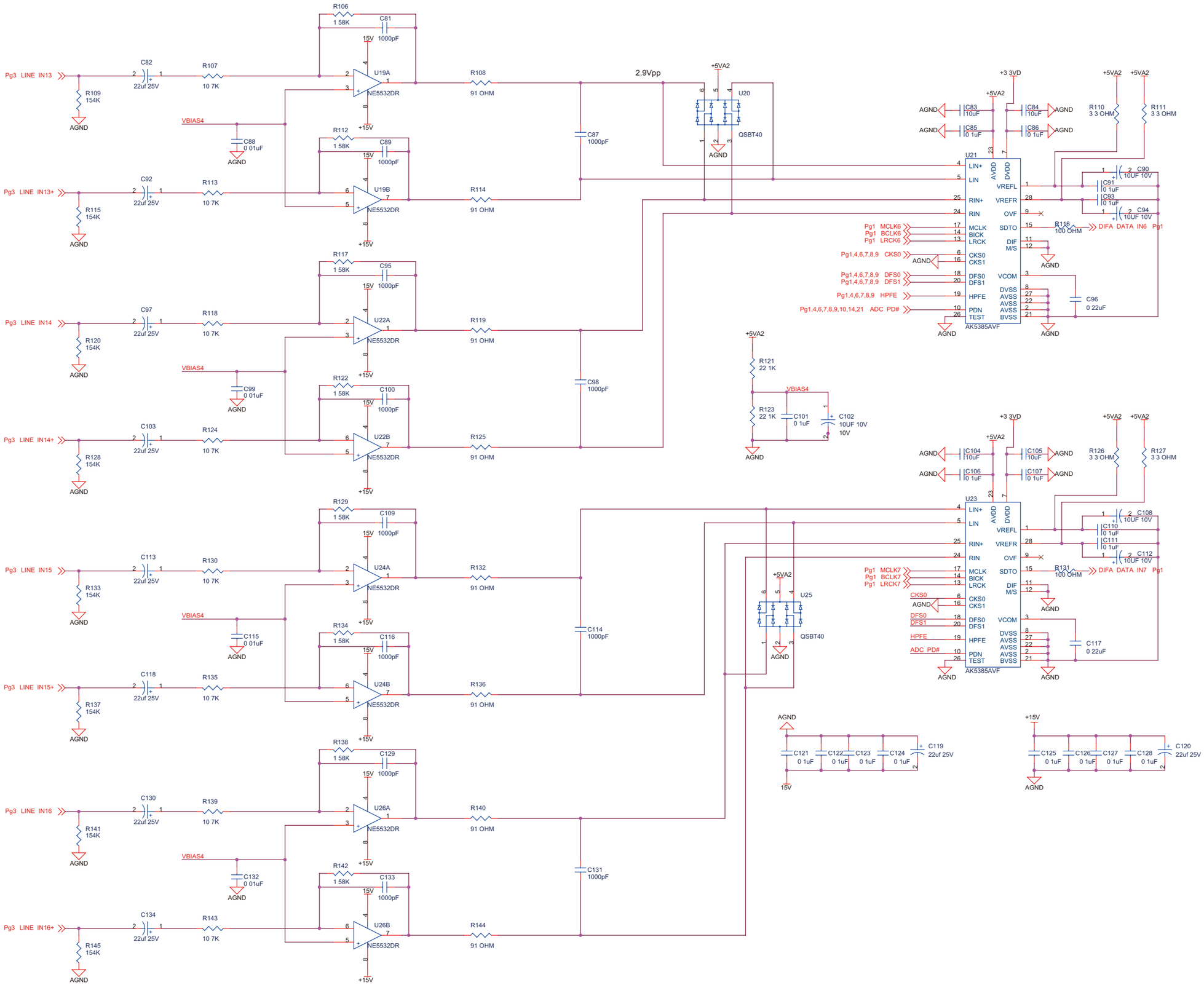
U10 LT1763CS8
IN OUT SHDN BYP GND0 GND1 GND2 SENSE
+6V
C25 10UF 10V
C26 0.1uF
C23 0.01uF
R65 6.19K
R66 2.00K
C27 0.1uF
C28 10uF
C24 10UF 10V 10V

+3.3VD +5VA1
C31 10uF
C32 10uF
C33 0.1uF
C34 0.1uF
R70 3.3 OHM
R71 3.3 OHM

U13 AK5385AVF
LIN+ LIN- RIN+ RIN- MCLK BICK LRCK CKS0 CKS1 DFS0 DFS1 HPFE PDN TEST
AVDD DVDD VREFL VREFR OVF SDTO DIF M/S VCOM DVSS AVSS BVSS
Pg1 MCLK0
Pg1 BCLK0
Pg1 LRCK0
Pg1,5,6,7,8,9 CKS0
Pg1,5,6,7,8,9 DFS0
Pg1,5,6,7,8,9 DFS1
Pg1,5,6,7,8,9 HPFE
Pg1,5,6,7,8,9,10,14,21 ADC_PD#
C38 C42 10UF 10V
C39 C41 0.1uF
R76 100 OHM
DIFA_DATA_IN0 Pg1
C44 0.22uF

U15 AK5385AVF
C52 C54 C53 C55 10uF 0.1uF
R86 R87 3.3 OHM
C56 C60 10UF 10V
C58 C59 0.1uF
R91 100 OHM
DIFA_DATA_IN1 Pg1
C65 0.22uF

C67 C68 C69 C70 C71 C72 C73 C74 0.1uF
-15V


Pg3 LINE IN13
Pg3 LINE IN13+
Pg3 LINE IN14
Pg3 LINE IN14+
Pg3 LINE IN15
Pg3 LINE IN15+
Pg3 LINE IN16
Pg3 LINE IN16+
R106 1 58K
C81 1000pF
R107 10 7K
C82 22uf 25V
R108 91 OHM
R109 154K
U19A NE5532DR
R112 1 58K
C89 1000pF
R113 10 7K
C92 22uf 25V
R114 91 OHM
R115 154K
U19B NE5532DR
R117 1 58K
C95 1000pF
R118 10 7K
C97 22uf 25V
R119 91 OHM
R120 154K
U22A NE5532DR
R122 1 58K
C100 1000pF
R124 10 7K
C103 22uf 25V
R125 91 OHM
R128 154K
U22B NE5532DR
R129 1 58K
C109 1000pF
R130 10 7K
C113 22uf 25V
R132 91 OHM
R133 154K
U24A NE5532DR
R134 1 58K
C116 1000pF
R135 10 7K
C118 22uf 25V
R136 91 OHM
R137 154K
U24B NE5532DR
R138 1 58K
C129 1000pF
R139 10 7K
C130 22uf 25V
R140 91 OHM
R141 154K
U26A NE5532DR
R142 1 58K
C133 1000pF
R143 10 7K
C134 22uf 25V
R144 91 OHM
R145 154K
U26B NE5532DR
VBIAS4
C88 0 01uF
C99 0 01uF
C115 0 01uF
C132 0 01uF
AGND
+15V
15V
2.9Vpp
C87 1000pF
C98 1000pF
C114 1000pF
C131 1000pF
+5VA2
U20
QSBT40
U25
R121 22 1K
R123 22 1K
C101 0 1uF
C102 10UF 10V
10V
U21
U23
AK5385AVF
LIN+
LIN
RIN+
RIN
MCLK
BICK
LRCK
CKS0
CKS1
DFS0
DFS1
HPFE
PDN
TEST
AVDD
DVDD
VREFL
VREFR
OVF
SDTO
DIF
M/S
VCOM
DVSS
AVSS
BVSS
+3 3VD
C83 10uF
C84 10uF
C85 0 1uF
C86 0 1uF
C90 10UF 10V
C91 0 1uF
C93 0 1uF
C94 10UF 10V
R110 3 3 OHM
R111 3 3 OHM
R116 100 OHM
DIFA DATA IN6 Pg1
Pg1 MCLK6
Pg1 BCLK6
Pg1 LRCK6
Pg1,4,6,7,8,9 CKS0
Pg1,4,6,7,8,9 DFS0
Pg1,4,6,7,8,9 DFS1
Pg1,4,6,7,8,9 HPFE
Pg1,4,6,7,8,9,10,14,21 ADC PD#
C96 0 22uF
C104 10uF
C105 10uF
C106 0 1uF
C107 0 1uF
C108 10UF 10V
C110 0 1uF
C111 0 1uF
C112 10UF 10V
R126 3 3 OHM
R127 3 3 OHM
R131 100 OHM
DIFA DATA IN7 Pg1
Pg1 MCLK7
Pg1 BCLK7
Pg1 LRCK7
CKS0
DFS0
DFS1
HPFE
ADC PD#
C117 0 22uF
C121 0 1uF
C122 0 1uF
C123 0 1uF
C124 0 1uF
C119 22uf 25V
C125 0 1uF
C126 0 1uF
C127 0 1uF
C128 0 1uF
C120 22uf 25V

IF-AN24X (6/22) Line In 17-20

Pg3 LINE_IN17- / LINE_IN17+ / LINE_IN18- / LINE_IN18+ / LINE_IN19- / LINE_IN19+ / LINE_IN20- / LINE_IN20+

C142 / C152 / C157 / C163 / C173 / C178 / C188 / C192 22uf 25V

R149 / R155 / R160 / R166 / R172 / R177 / R181 / R185 10.7K

R151 / R157 / R162 / R170 / R175 / R179 / R183 / R187 154K

AGND

VBIAS5

C148 / C159 / C175 / C190 0.01uF

R146 / R154 / R159 / R164 / R171 / R176 / R180 / R184 1.58K

C141 / C149 / C155 / C160 / C169 / C176 / C187 / C191 1000pF

-15V / +15V

U28A / U28B / U31A / U31B / U33A / U33B / U35A / U35B NE5532DR

R150 / R156 / R161 / R167 / R174 / R178 / R182 / R186 91 OHM

C147 / C158 / C174 / C189 1000pF

2 9Vpp

U29 QSBT40

+5VA3

U34 QSBT40

+6V

C4 10UF 10V 10V

U27 LT1763CS8 (IN, SHDN, GND0, GND1, GND2, OUT, BYP, SENSE)

C137 10UF 10V / C138 0.1uF

C135 0.01uF / R147 6.19K / R148 2.00K

C139 0.1uF / C140 10uF / C136 10UF 10V 10V

+3.3VD

C143 / C144 / C145 / C146 10uF / 0.1uF

R152 / R153 3.3 OHM

U30 / U32 AK5385AVF

LIN+ / LIN- / RIN+ / RIN- / MCLK / BICK / LRCK / CKS0 / CKS1 / DFS0 / DFS1 / HPFE / PDN / TEST / AVDD / DVDD / VREFL / VREFR / OVF / SDTO / DIF / M/S / VCOM / DVSS / AVSS / BVSS

Pg1 MCLK8 / BCLK8 / LRCK8

Pg1,4,5,7,8,9 CKS0 / DFS0 / DFS1 / HPFE / ADC_PD#

C150 / C154 / C168 / C172 10UF 10V

C151 / C153 / C170 / C171 0.1uF

R158 / R173 100 OHM

DIFA_DATA_IN8 Pg1 / DIFA_DATA_IN9 Pg1

C156 / C177 0.22uF

R163 22.1K / R165 22.1K

C161 0.1uF / C162 10UF 10V 10V

C164 / C165 / C166 / C167 10uF / 0.1uF

R168 / R169 3.3 OHM

C179 / C180 / C181 / C182 0.1uF

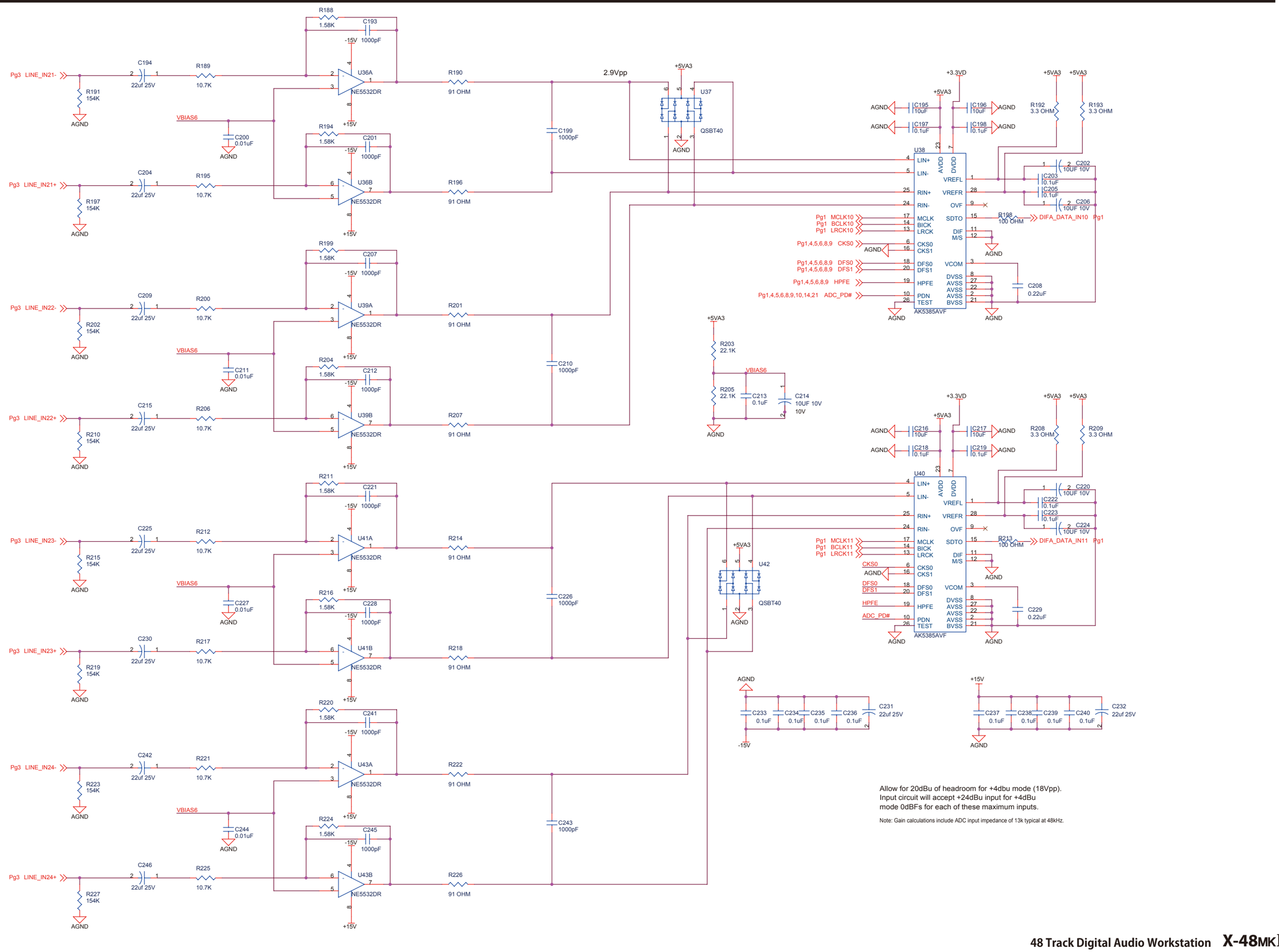
C183 / C184 / C185 / C186 0.1uF

-15V

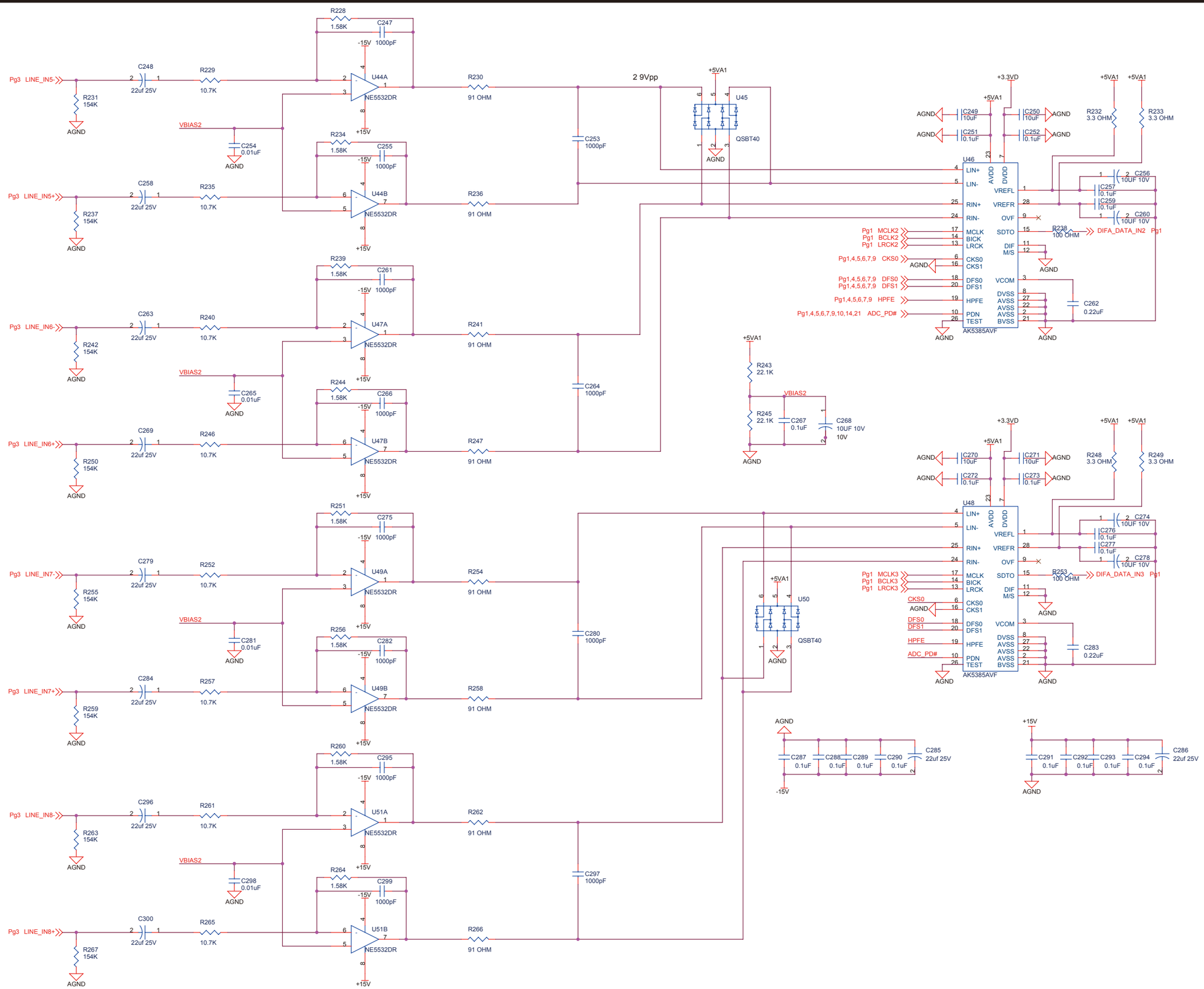
Allow for 20dBu of headroom for +4dbu mode (18Vpp).
Input circuit will accept +24dBu input for +4dBu mode 0dBFs for each of these maximum inputs.

Note: Gain calculations include ADC input impedance of 13k typical at 48kHz.

IF-AN24X (7/22) Line In 21-24



IF-AN24X (8/22) Line In 5-8



IF-AN24X (9/22) Line In 9-12

1 2 3 4 5 6 7 8

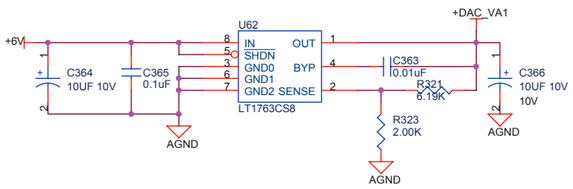
A B C D E

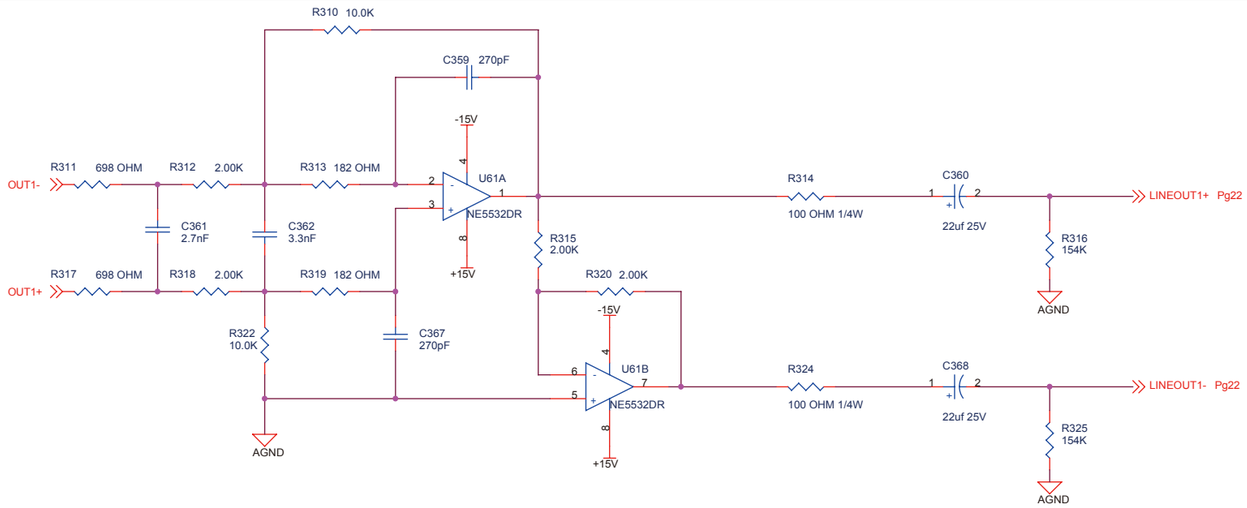
Pg3 LINE_IN9- / LINE_IN10- / LINE_IN11- / LINE_IN12-
Pg3 LINE_IN9+ / LINE_IN10+ / LINE_IN11+ / LINE_IN12+
C308 C318 C323 C329 C339 C344 C354 C358 22uf 25V
R271 R277 R282 R288 R294 R299 R303 R307 10.7K
R273 R279 R284 R292 R297 R301 R305 R309 154K
AGND
VBIAS3
C314 C325 C341 C356 0.01uF
R268 R276 R281 R286 R293 R298 R302 R306 1.58K
C307 C315 C321 C326 C335 C342 C353 C357 1000pF
-15V +15V
U53A U53B U56A U56B U58A U58B U60A U60B NE5532DR
R272 R278 R283 R289 R296 R300 R304 R308 91 OHM
C313 C324 C340 C355 1000pF
2 9Vpp
U54 QSBT40
+6V
U52 LT1763CS8
IN SHDN GND0 GND1 GND2 OUT BYP SENSE
C303 10UF 10V
C304 0.1uF
C301 0.01uF
R269 6.19K
R270 2.00K
C305 0.1uF
C306 10uF
C302 10UF 10V 10V
+5VA2 +3.3VD
C309 C310 C311 C312 10uF 0.1uF
R274 R290 3.3 OHM
R275 R291 3.3 OHM
U55 U57 AK5385AVF
LIN+ LIN- RIN+ RIN- MCLK BICK LRCK CKS0 CKS1 DFS0 DFS1 HPFE PDN TEST
AVDD DVDD VREFL VREFR OVF SDTO DIF M/S VCOM DVSS AVSS BVSS
C316 C320 C334 C338 10UF 10V
C317 C319 C336 C337 0.1uF
R280 R295 100 OHM
DIFA_DATA_IN4 Pg1
DIFA_DATA_IN5 Pg1
Pg1 MCLK4 Pg1 BCLK4 Pg1 LRCK4
Pg1 MCLK5 Pg1 BCLK5 Pg1 LRCK5
Pg1,4,5,6,7,8 CKS0
Pg1,4,5,6,7,8 DFS0 Pg1,4,5,6,7,8 DFS1
Pg1,4,5,6,7,8 HPFE
Pg1,4,5,6,7,8,10,14,21 ADC_PD#
C322 C343 0.22uF
R285 22.1K
R287 22.1K
C327 0.1uF
C328 10UF 10V 10V
C330 C331 C332 C333 10uF 0.1uF
C345 C346 C347 C348 C349 C350 C351 C352 0.1uF

Allow for 20dBu of headroom for +4dbu mode (18Vpp).
Input circuit will accept +24dBu input for +4dBu
mode 0dBFs for each of these maximum inputs.

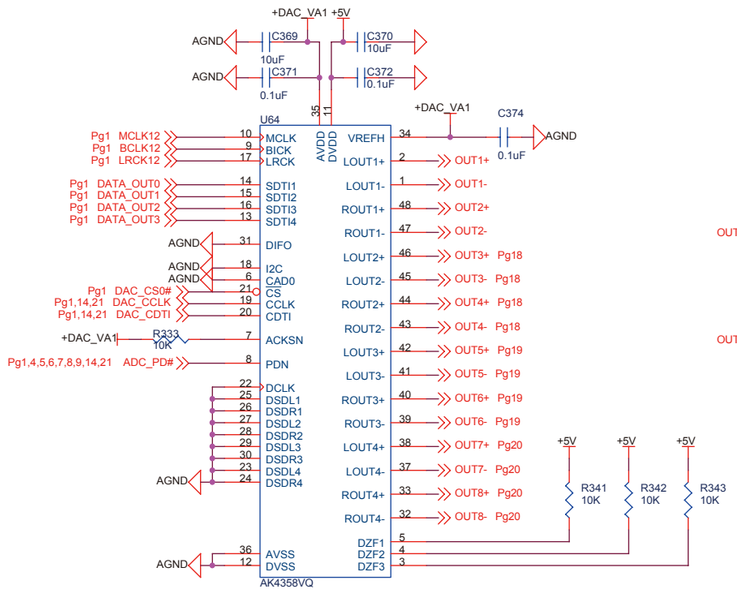
Note: Gain calculations include ADC input impedance of 13k typical at 48kHz.

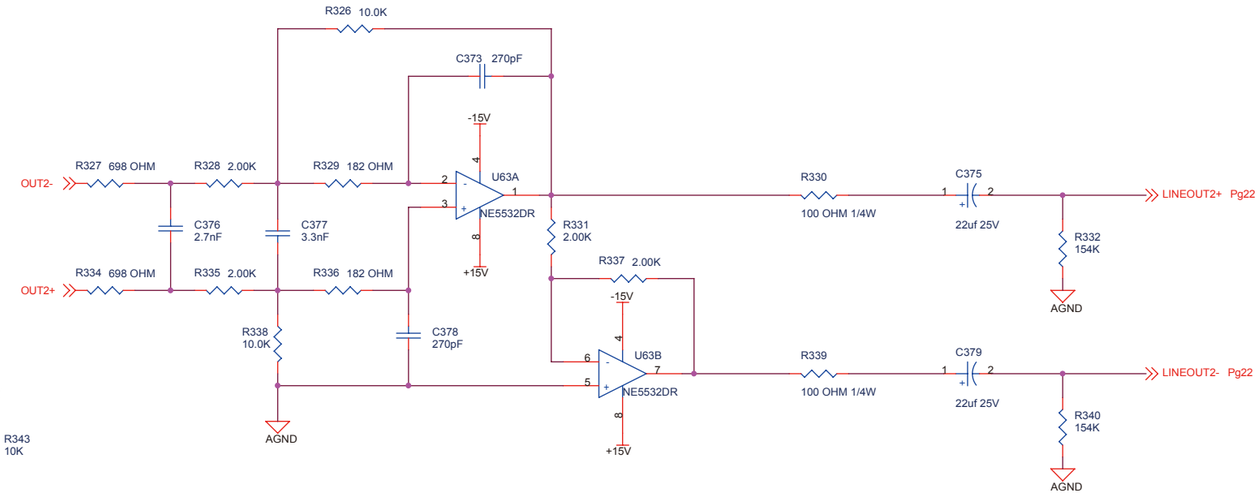
IF-AN24X (10/22) Line Out 1-2



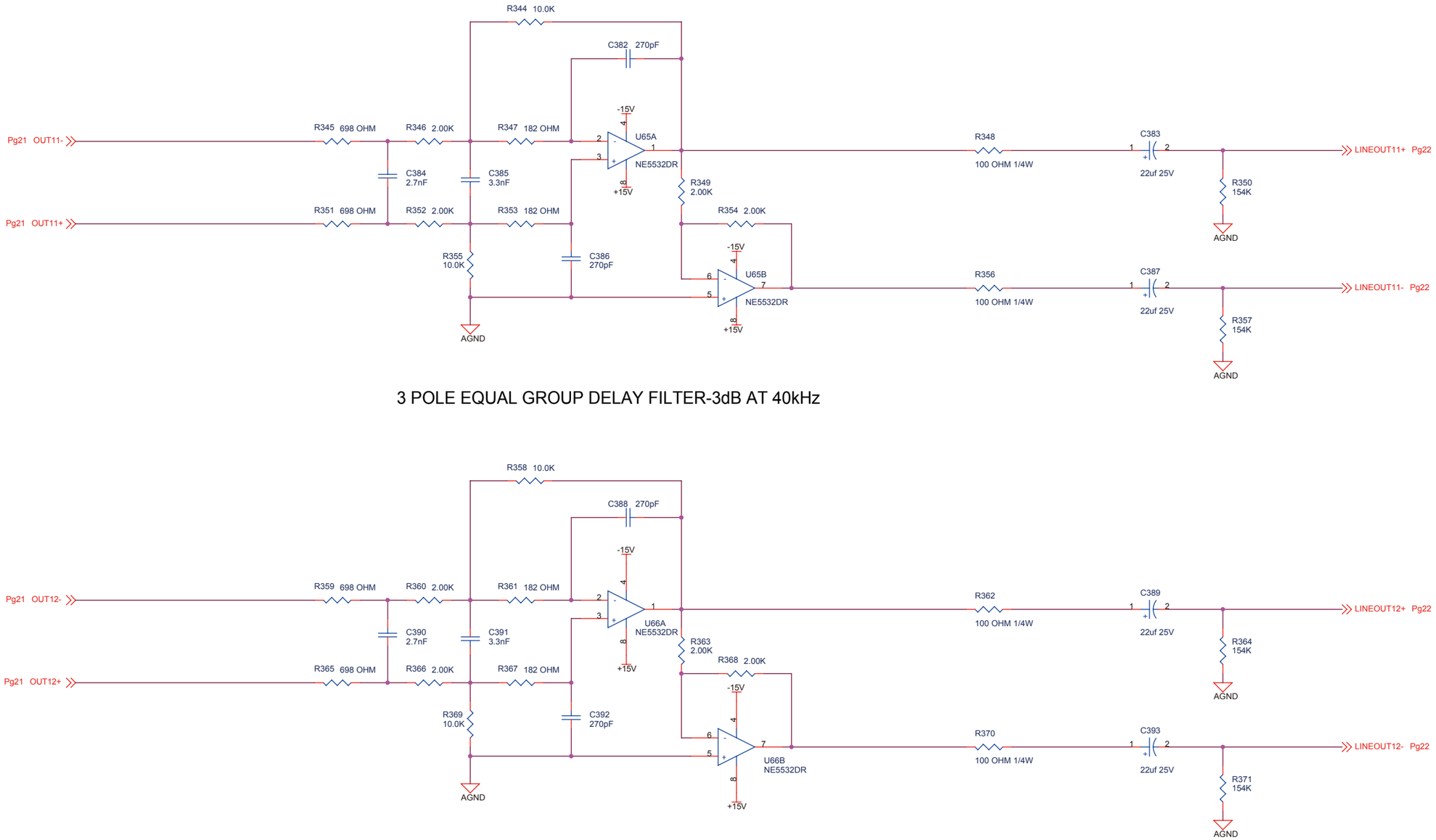


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

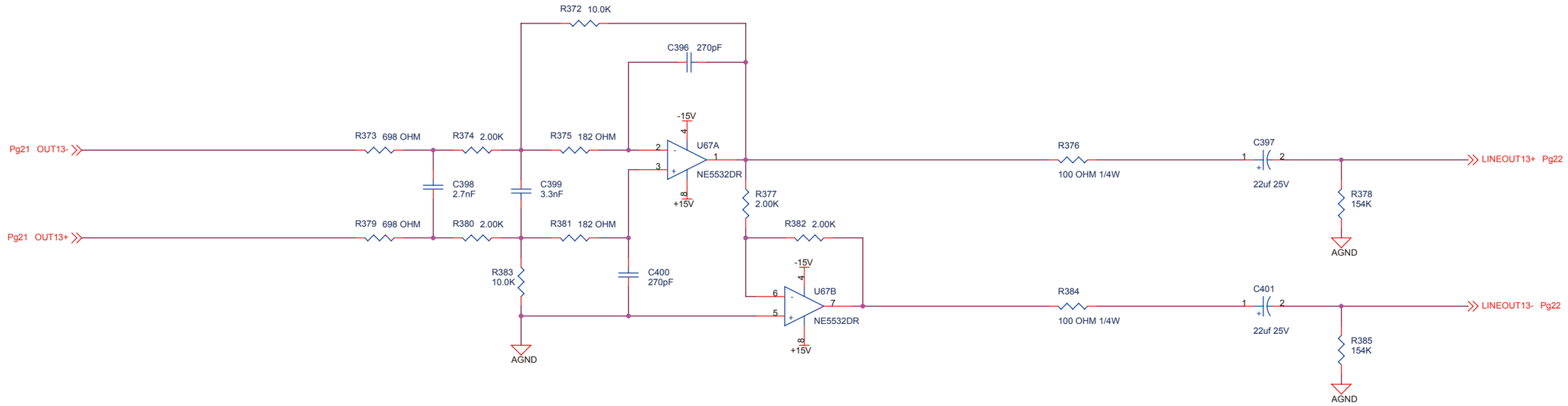




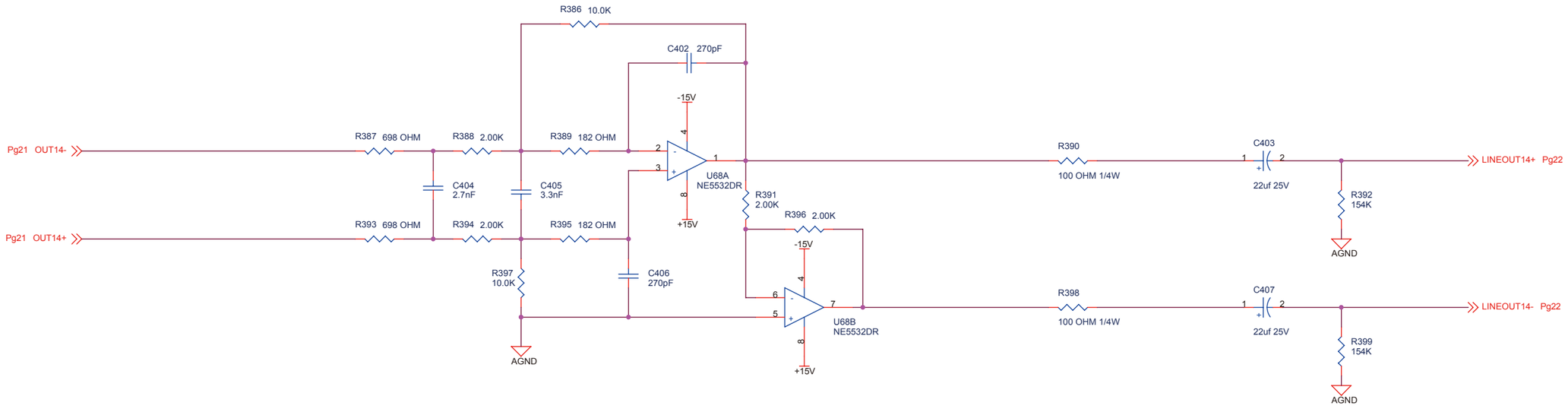
IF-AN24X (11/22) Line Out 11-12

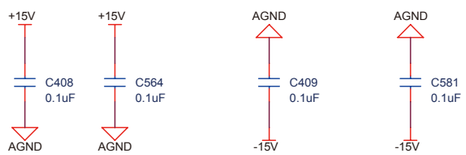


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

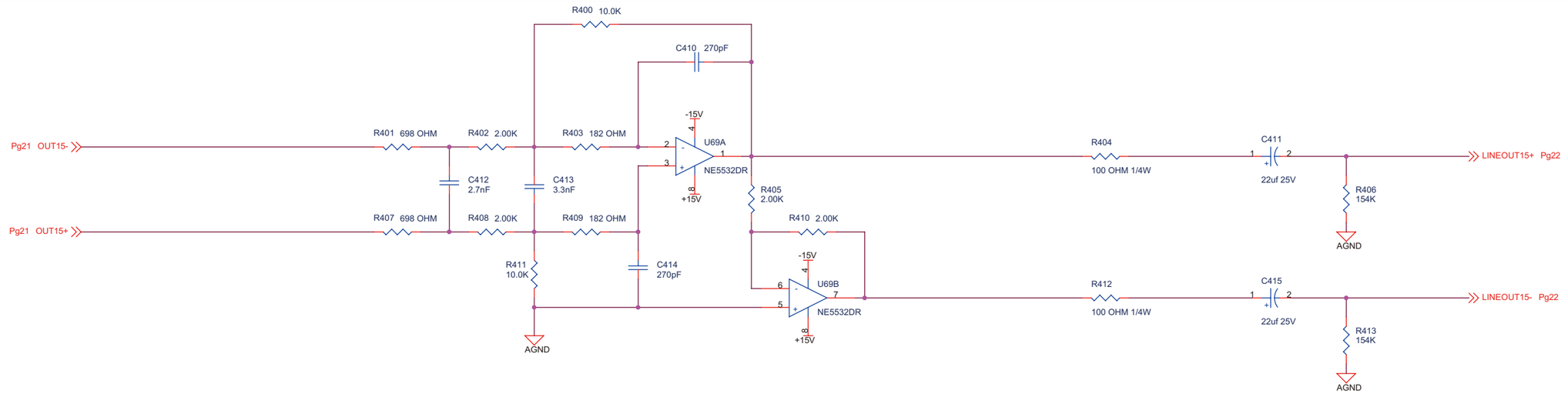


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

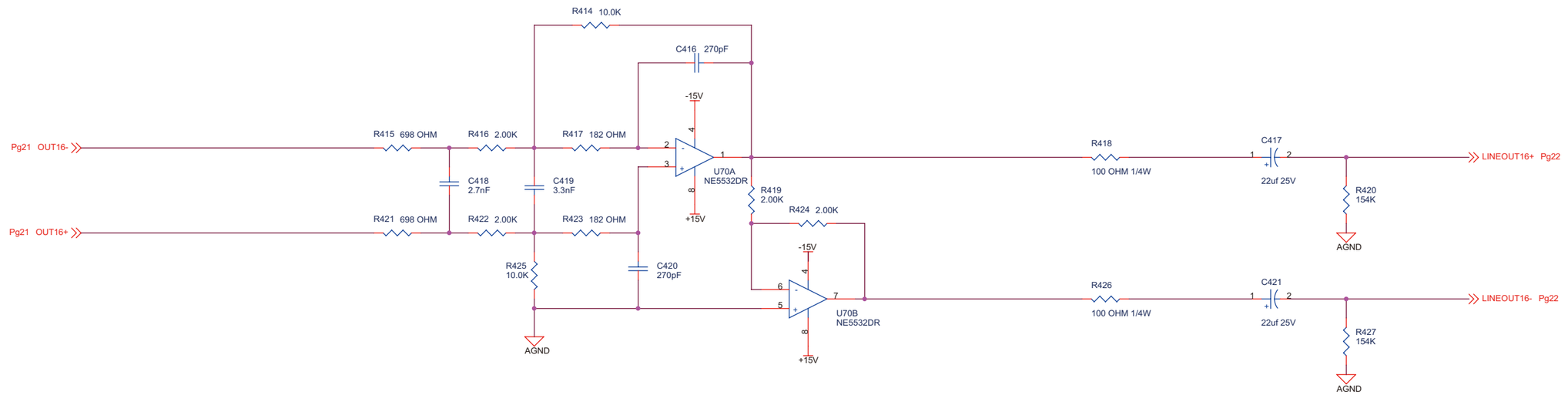


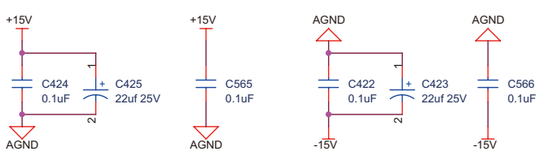


IF-AN24X (13/22) Line Out 15-16

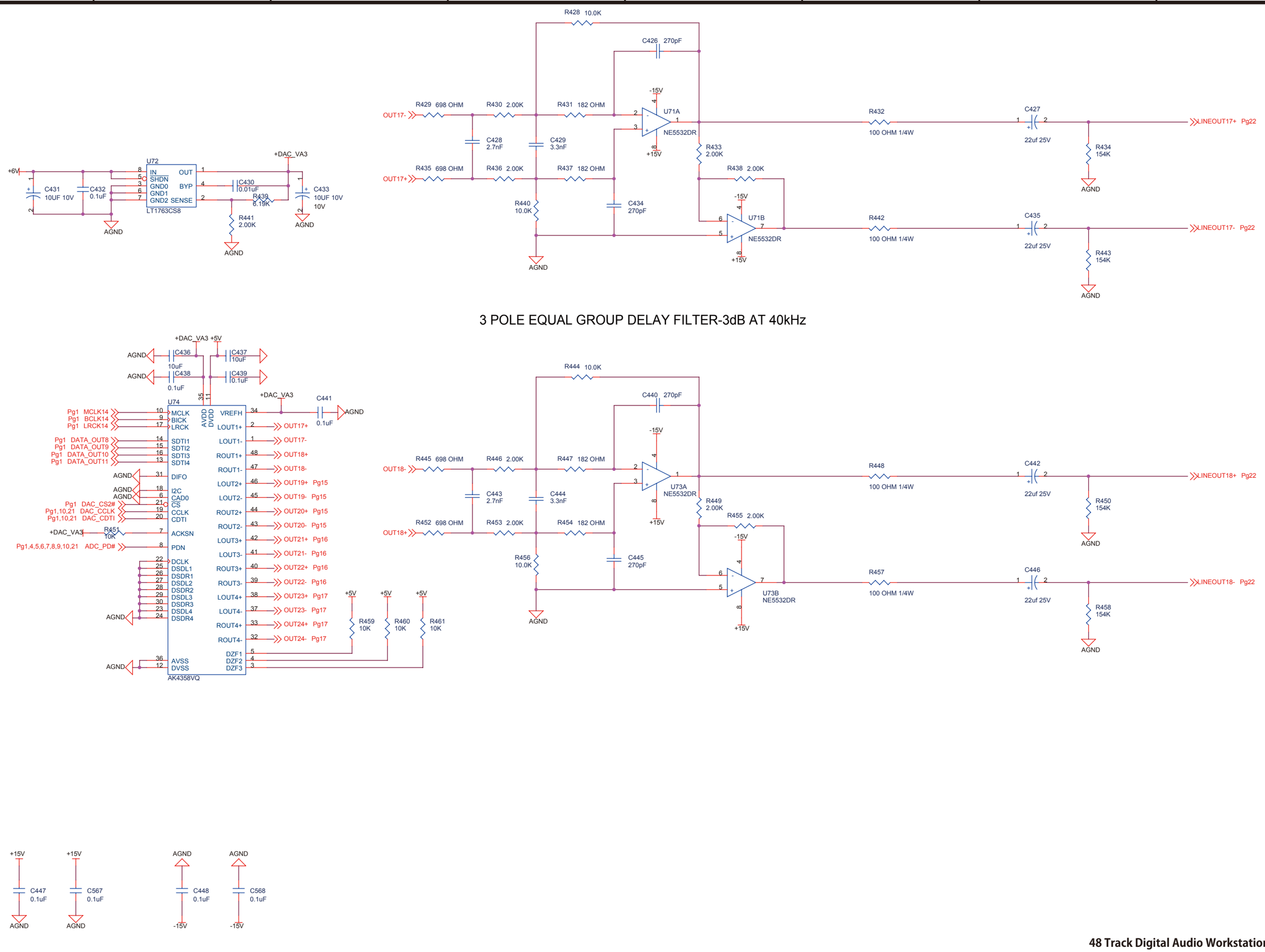


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

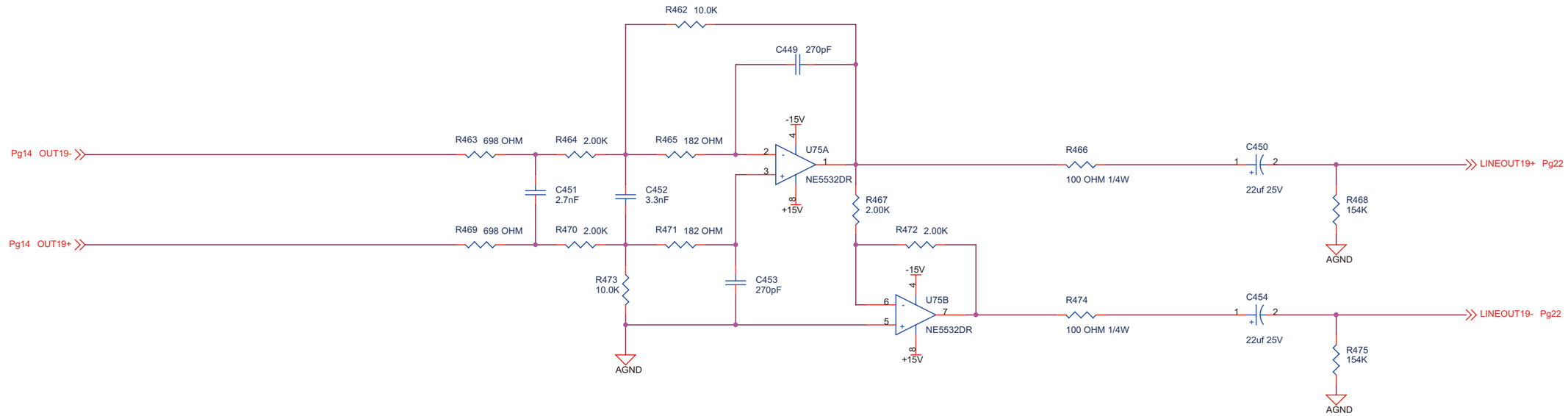




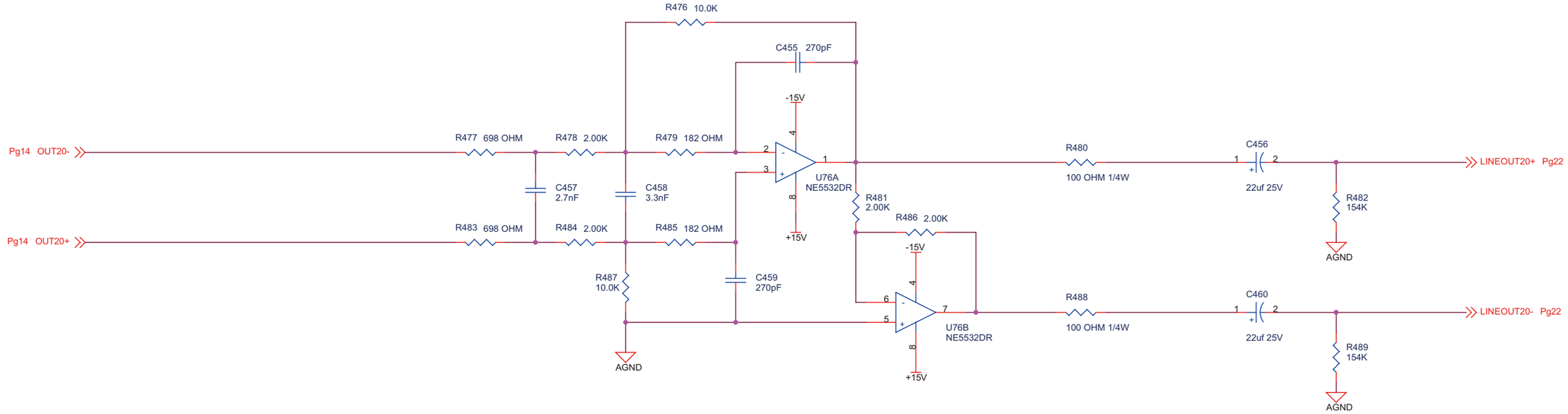
IF-AN24X (14/22) Line Out 17-18

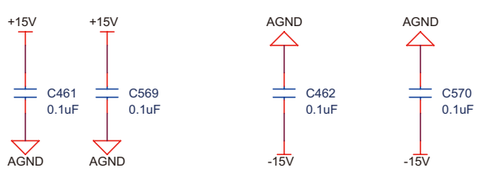


IF-AN24X (15/22) Line Out 19-20

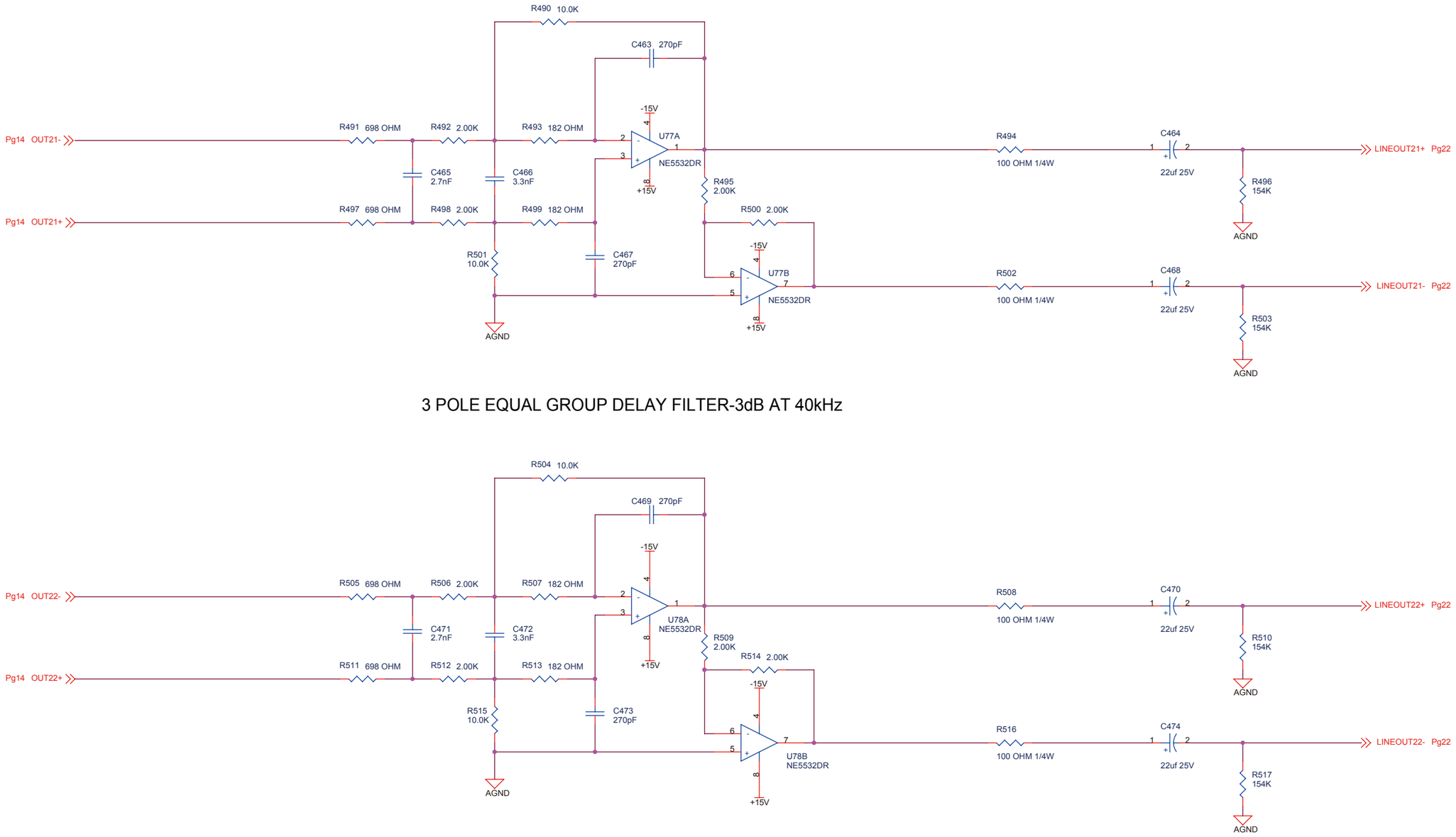


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

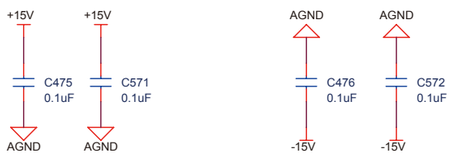




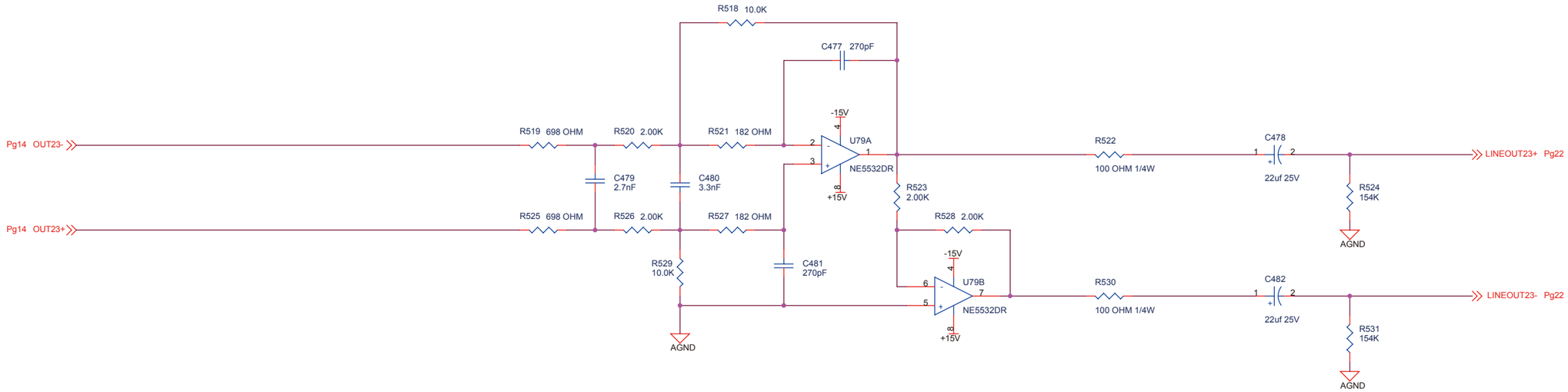
IF-AN24X (16/22) Line Out 21-22



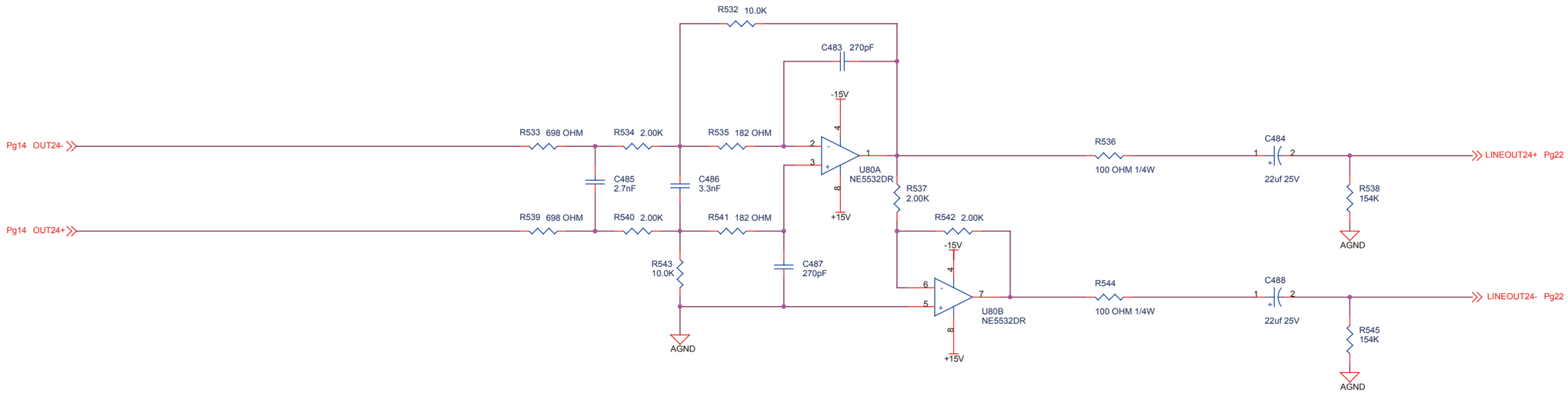
3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

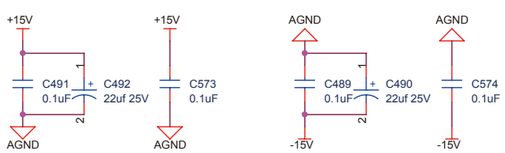


IF-AN24X (17/22) Line Out 23-24

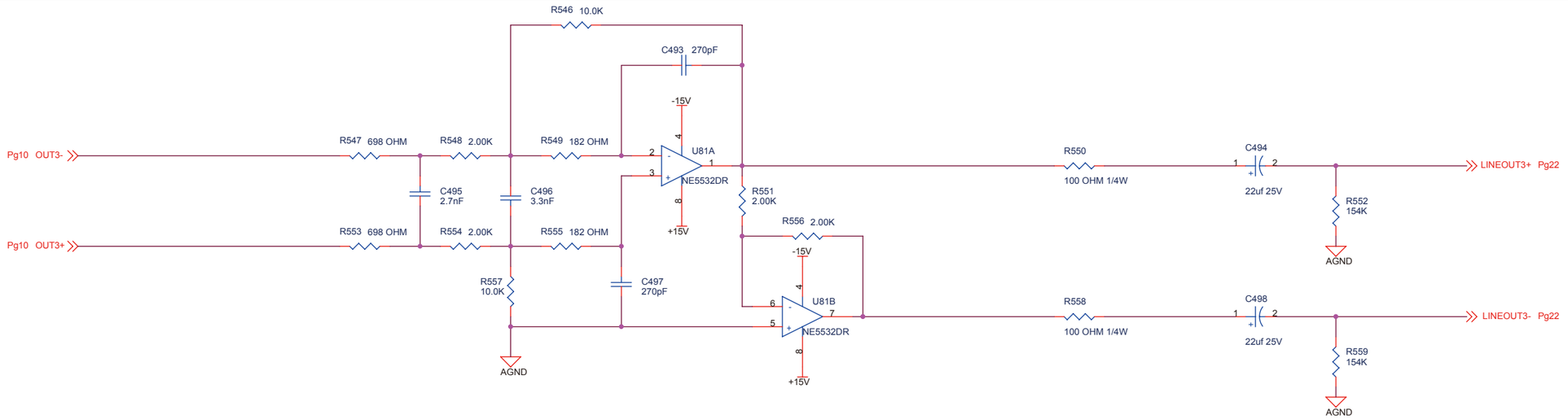


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

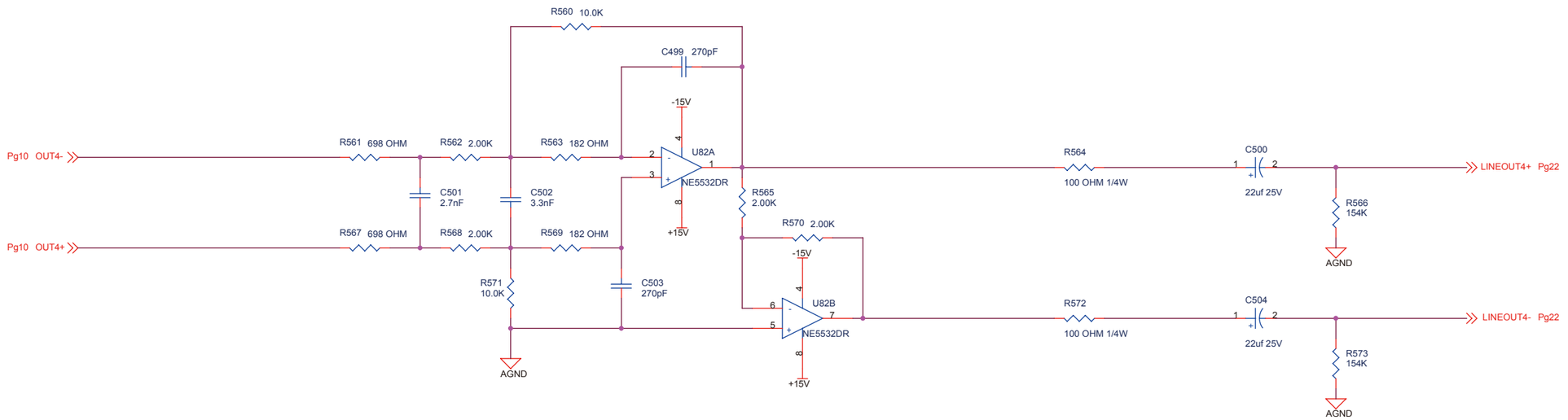


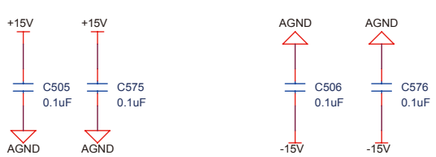


IF-AN24X (18/22) Line Out 3-4

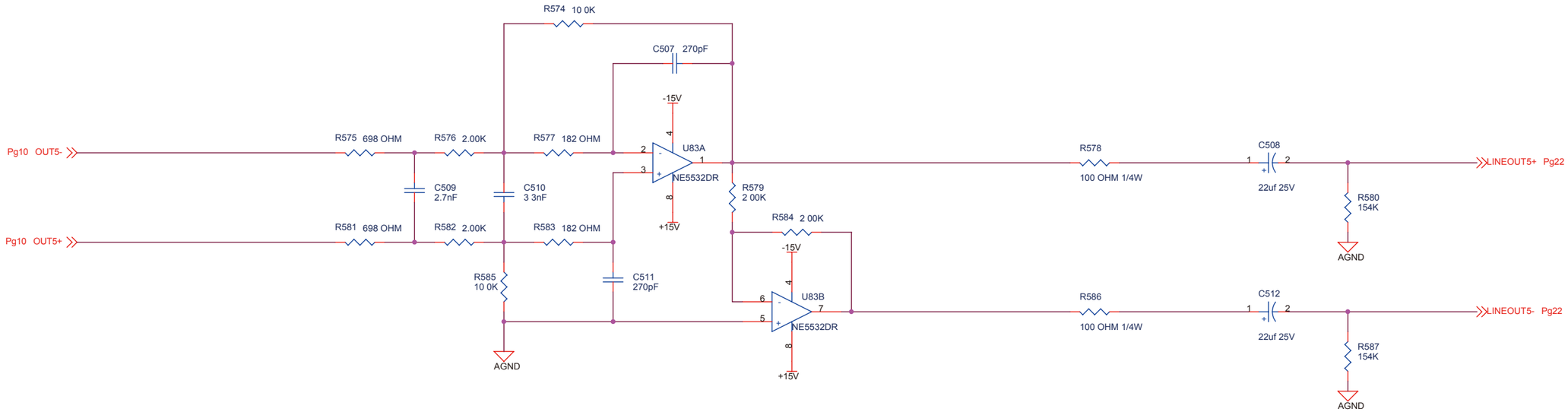


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

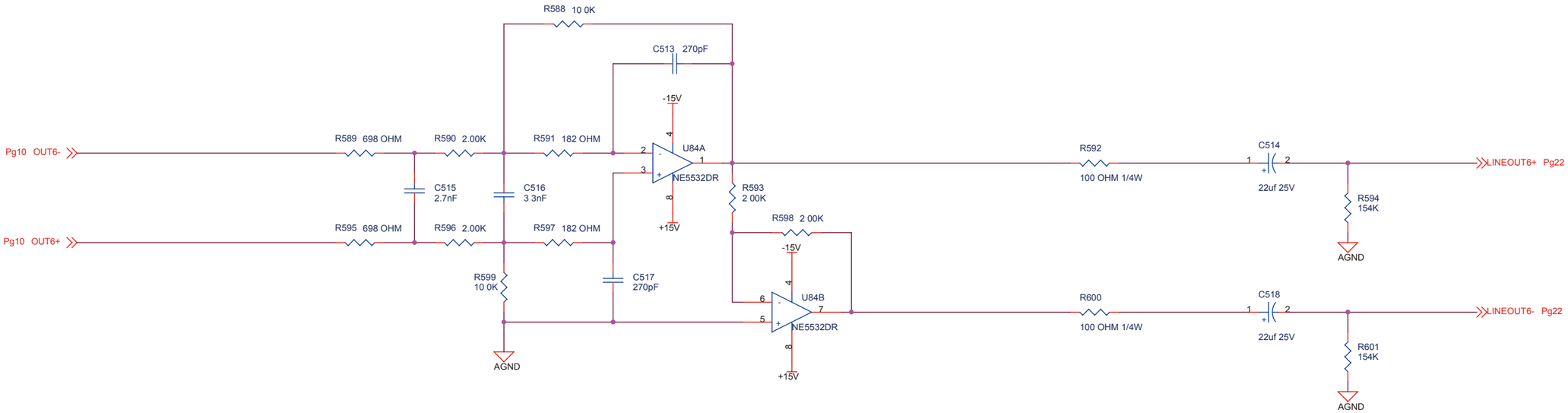


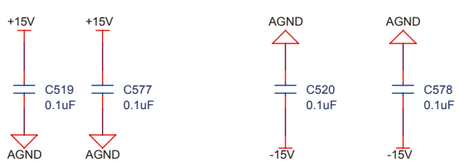


IF-AN24X (19/22) Line Out 5-6

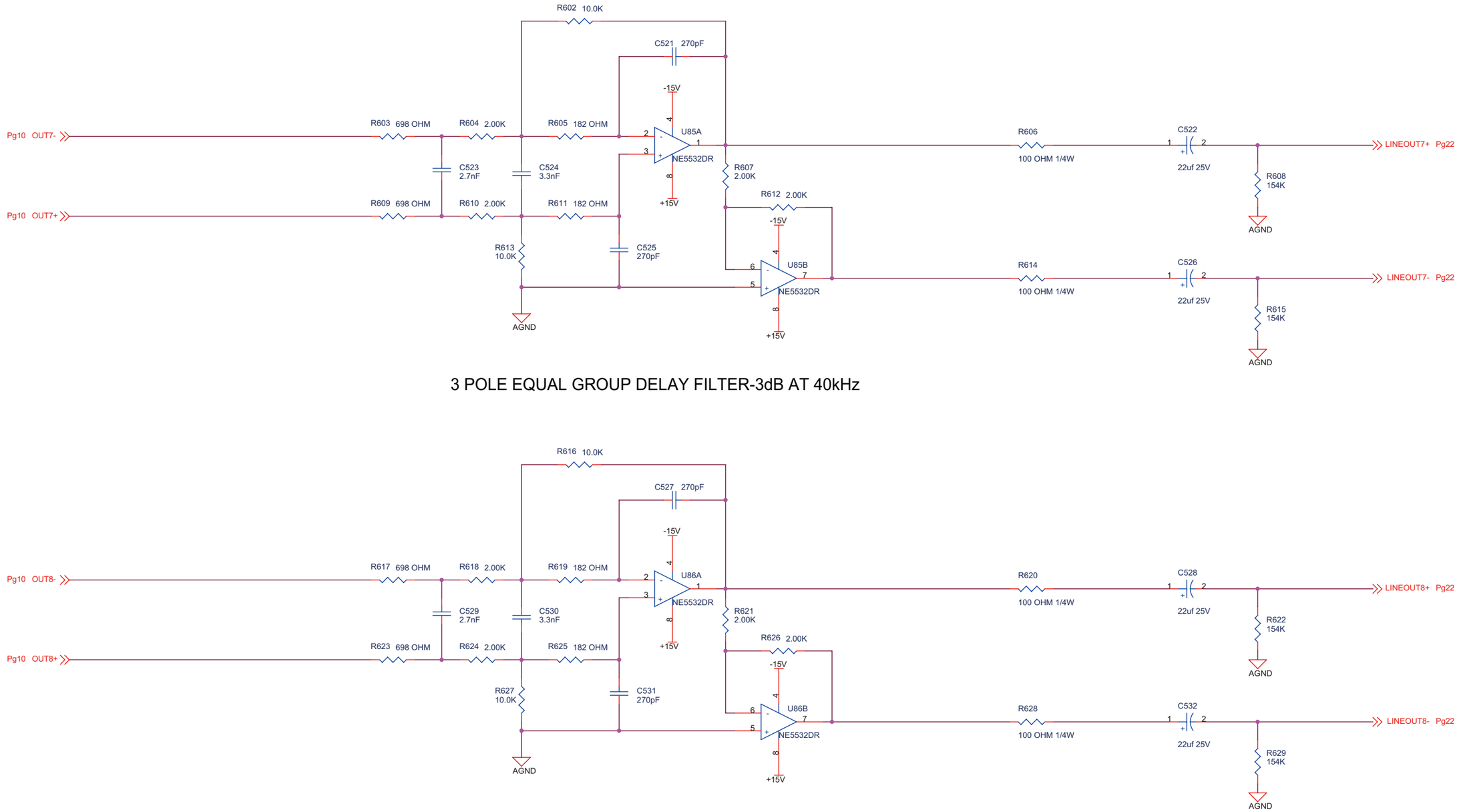


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

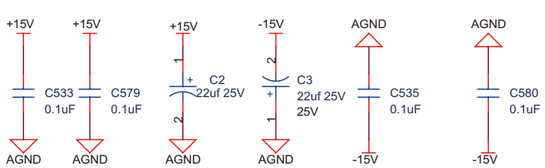




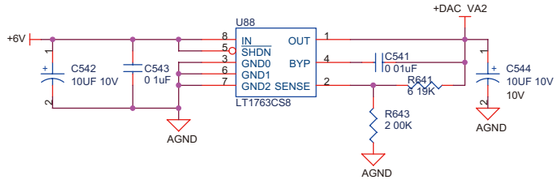
IF-AN24X (20/22) Line Out 7-8

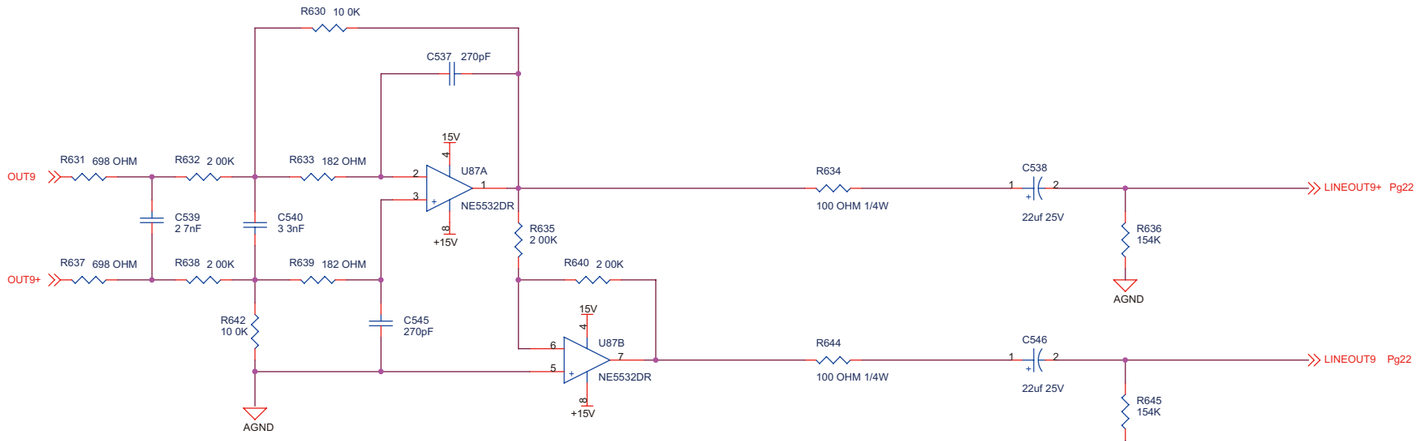


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz

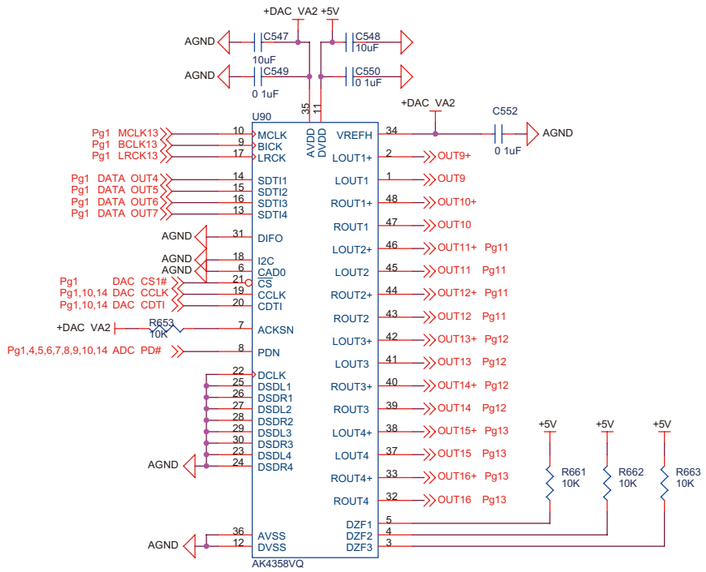


IF-AN24X (21/22) Line Out 9-10

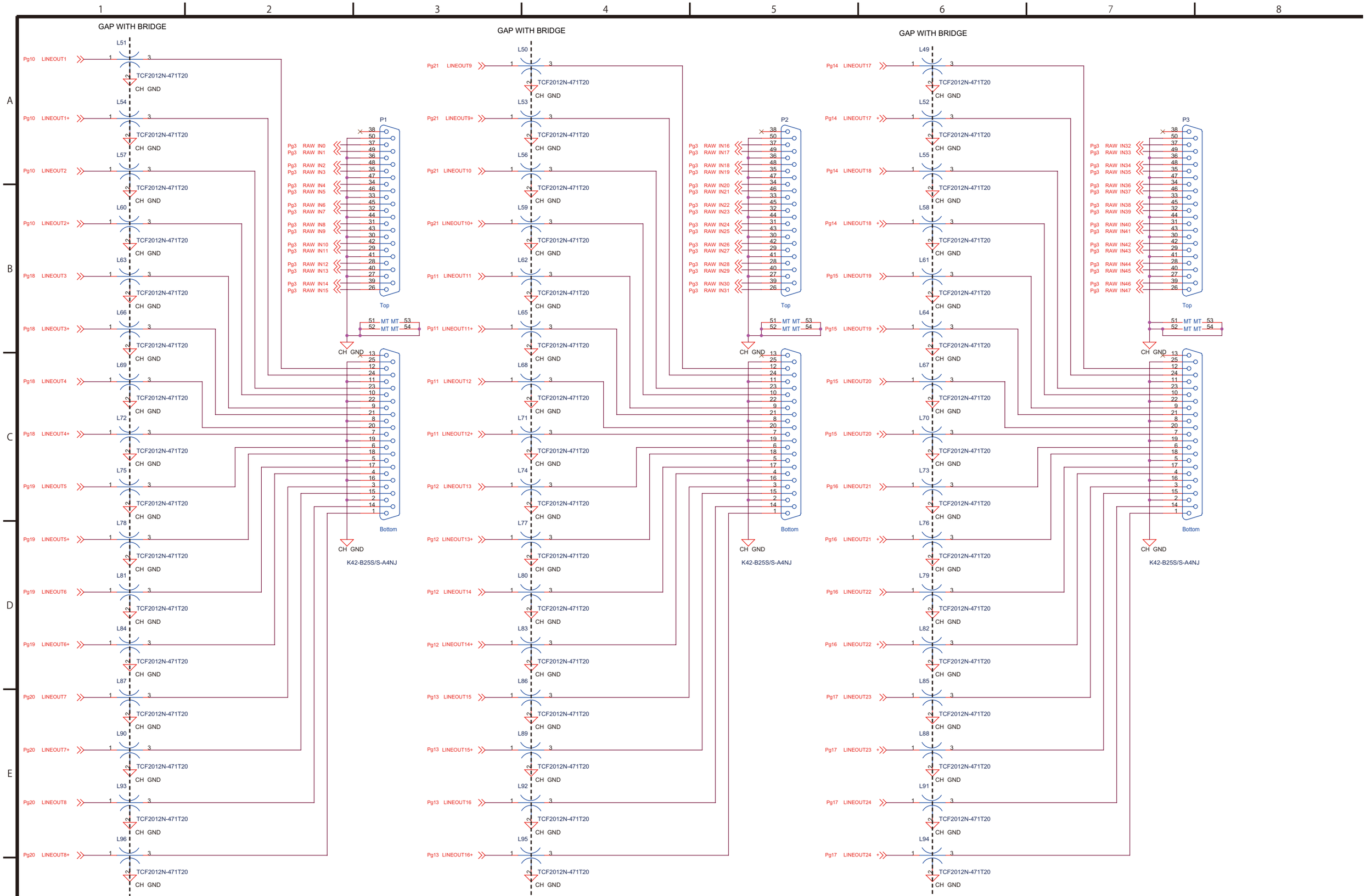


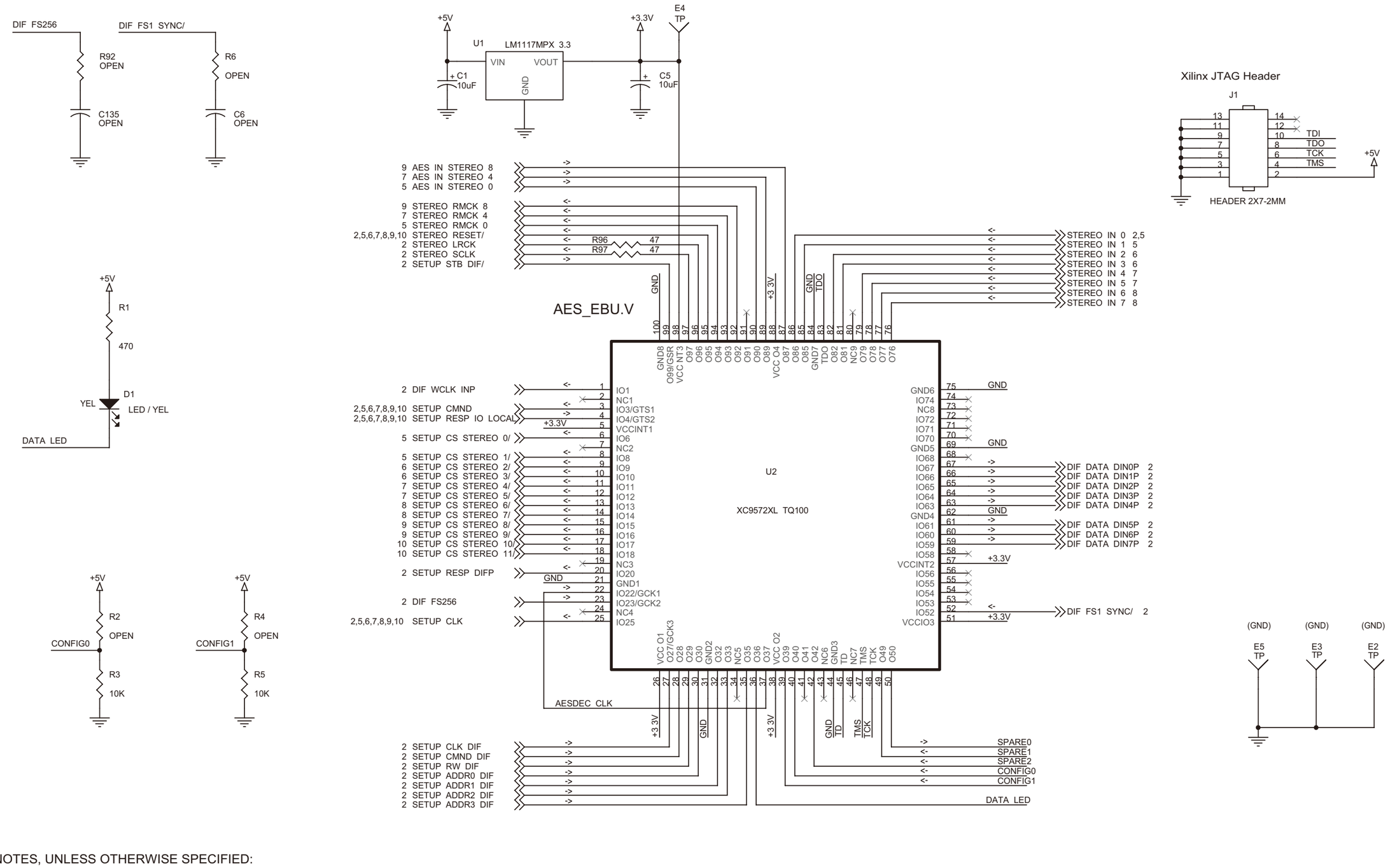


3 POLE EQUAL GROUP DELAY FILTER-3dB AT 40kHz



IF-AN24X (22/22) Line In/Out Connectors





NOTES, UNLESS OTHERWISE SPECIFIED:

1. CAPS ARE 50V MIN, +/- 10%. RESISTORS ARE 1/10W, +/15%.

MDX MA N

J2

HEADER 25X2

J3

TEST

HEADER 26

U3

74AHCT244APW

U4

74AHCT244APW

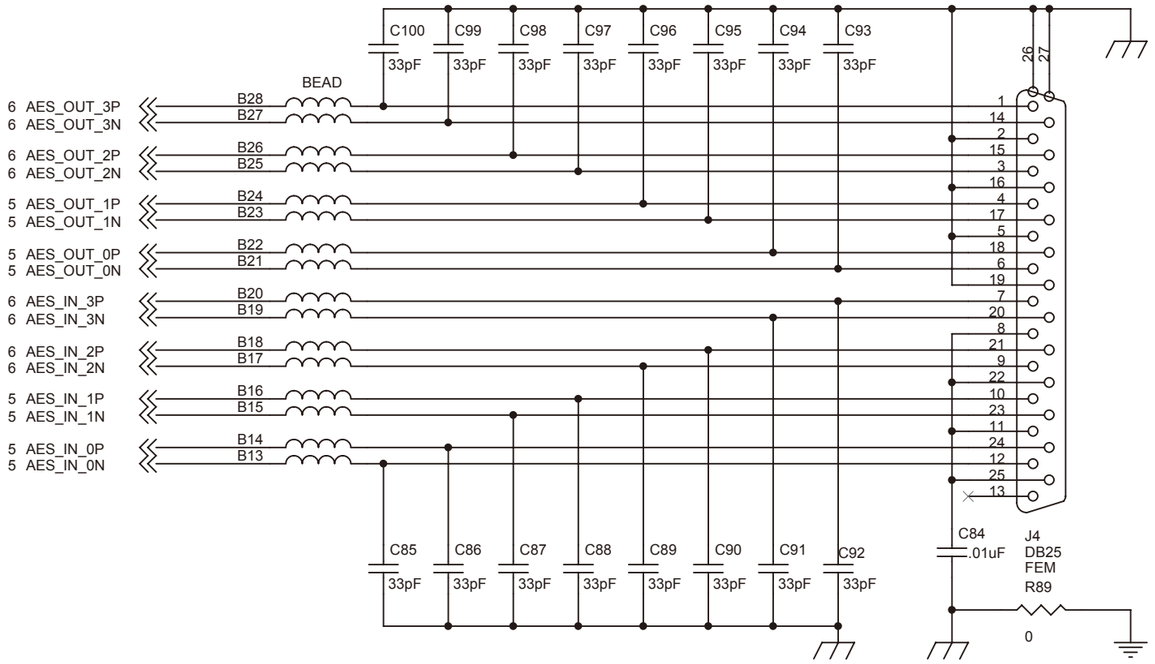
U5

74AHCT244APW

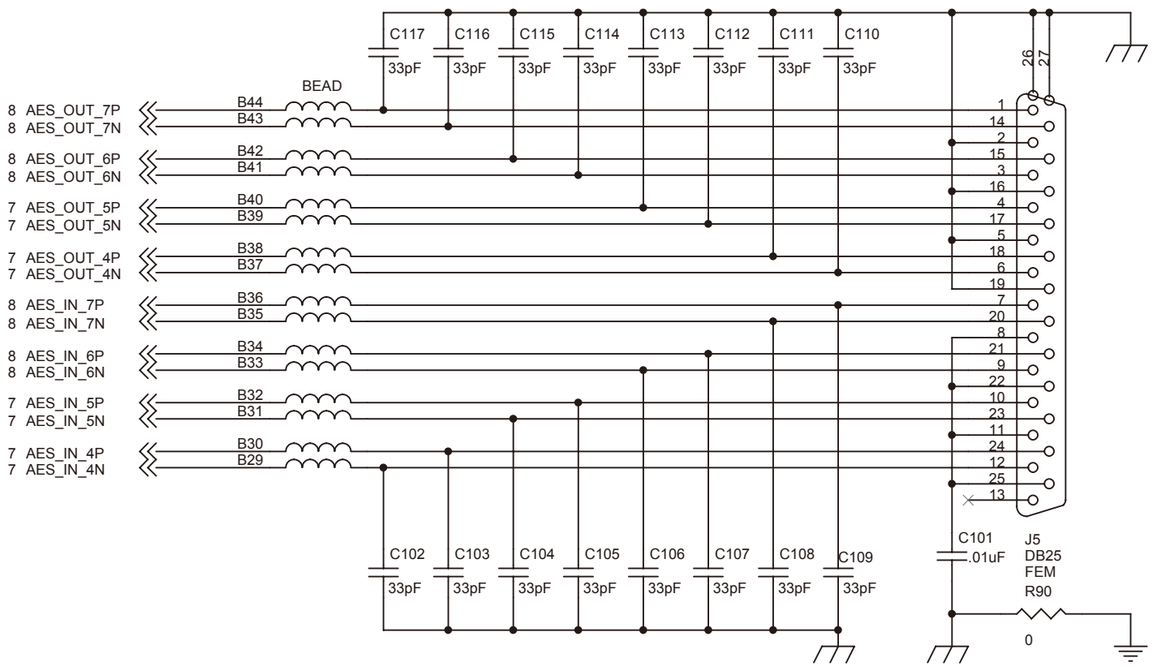
U21

74AHCT244APW

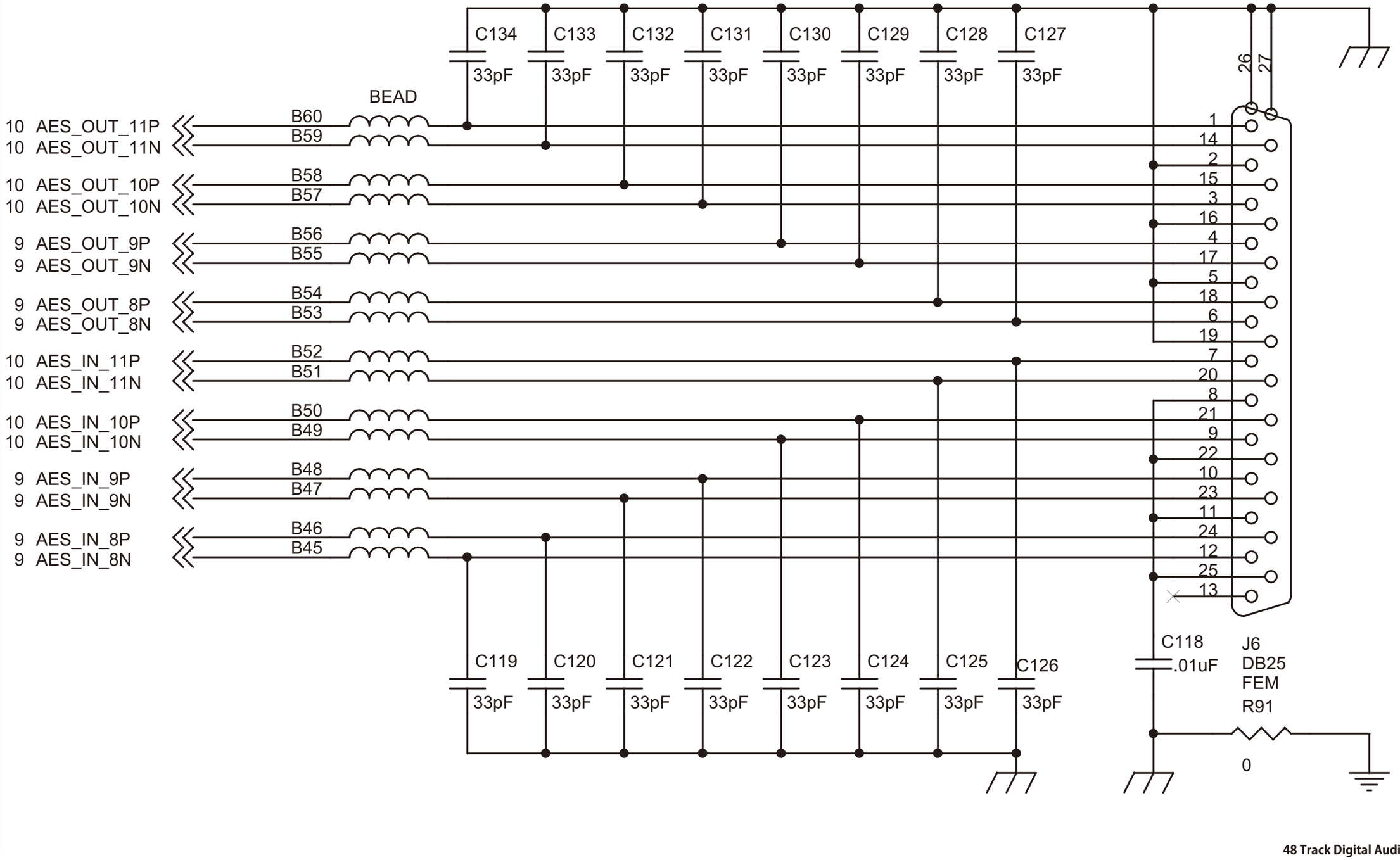
AES_EBU CONN 1 OF 3, DIG IN/OUT DB25

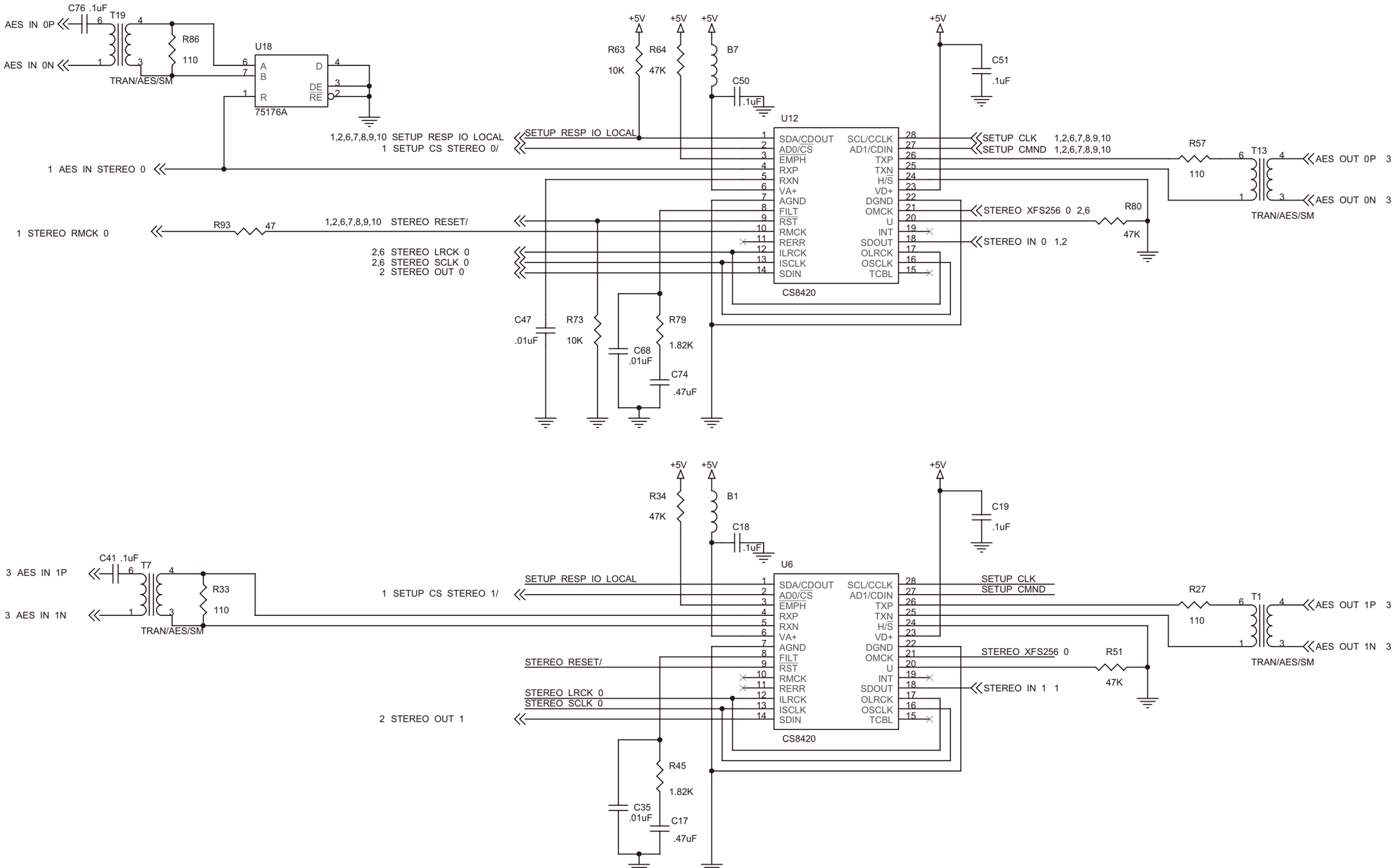


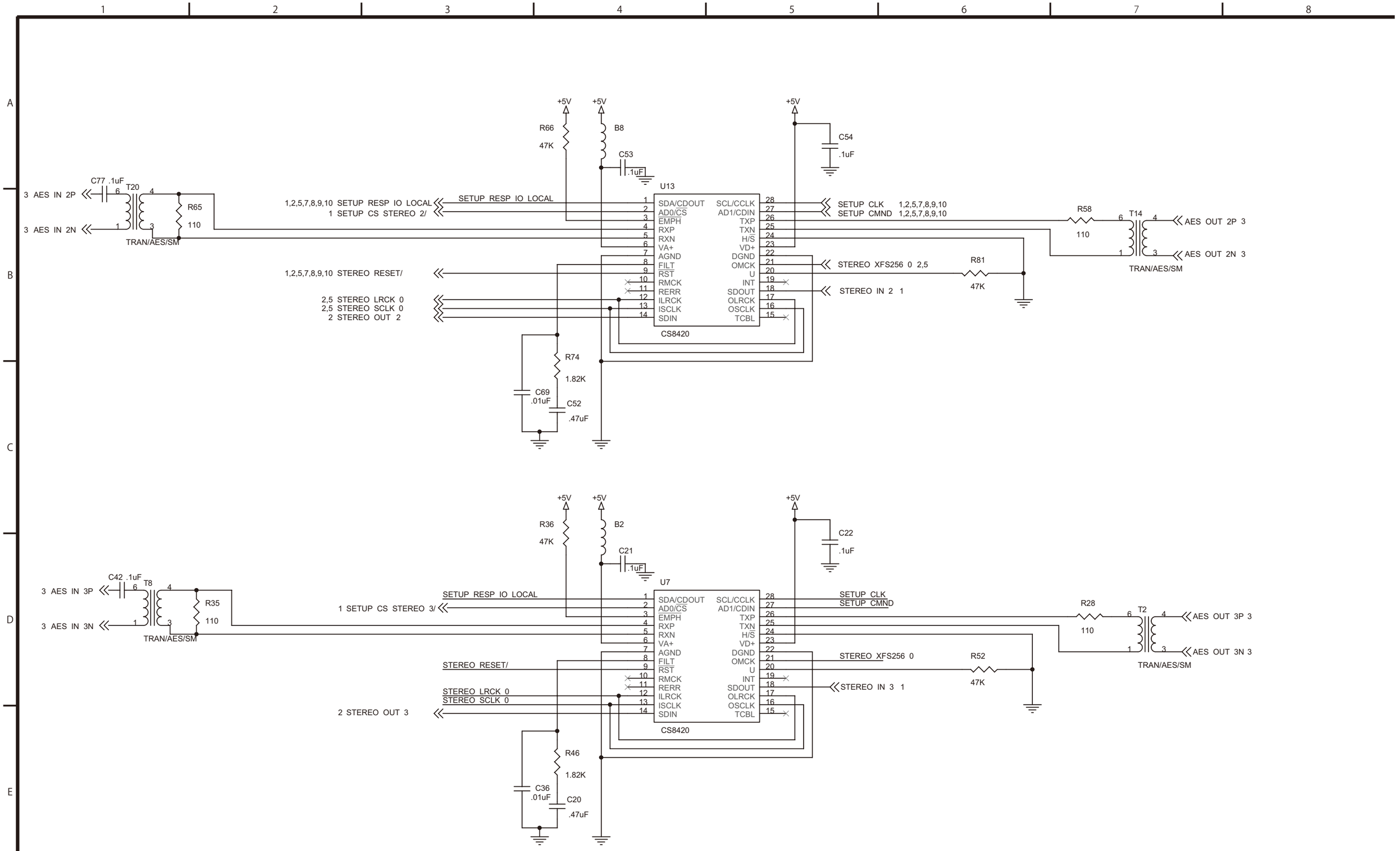
AES_EBU CONN 2 OF 3, DIG IN/OUT DB25

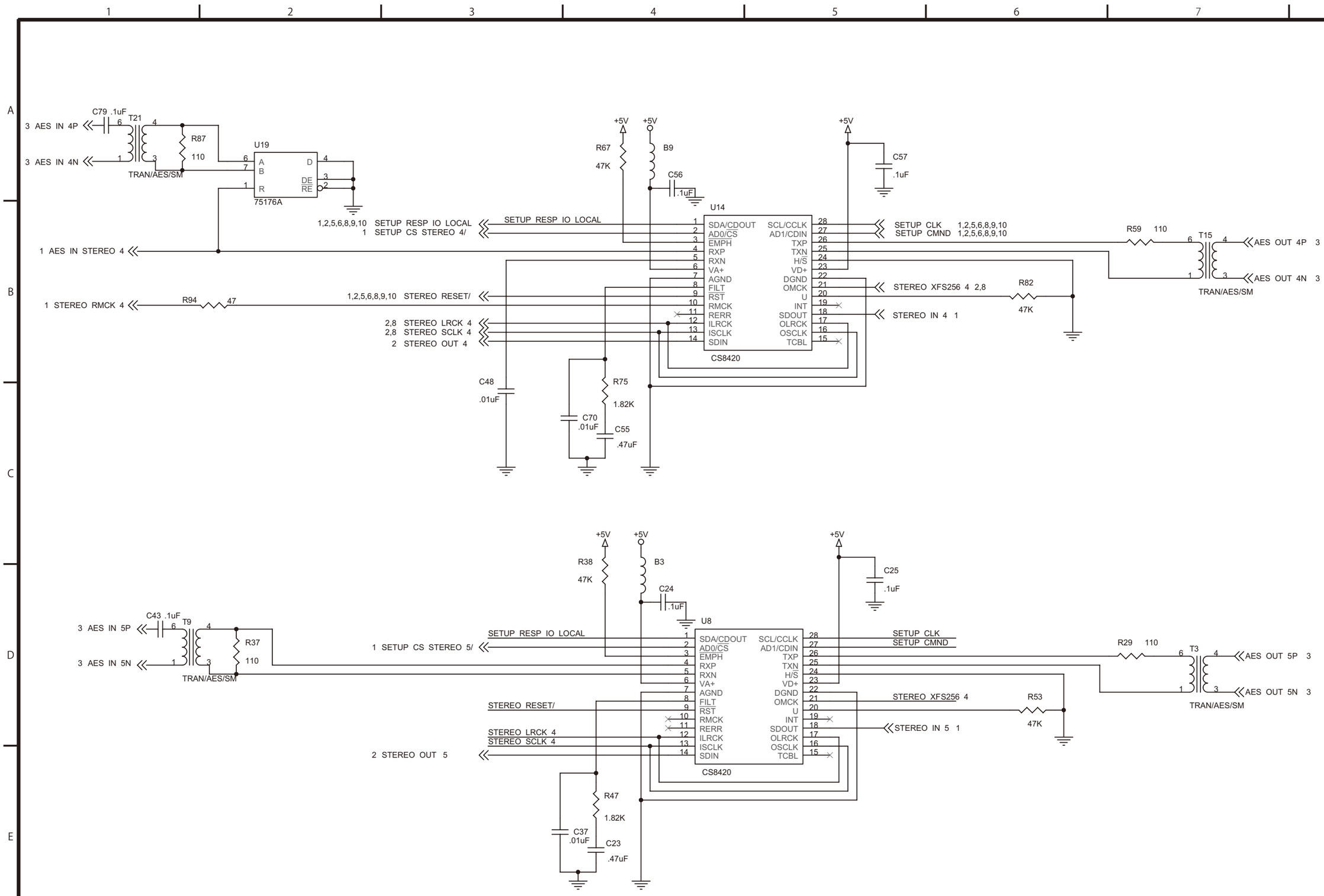


AES_EBU CONN 3 OF 3, DIG IN/OUT DB25

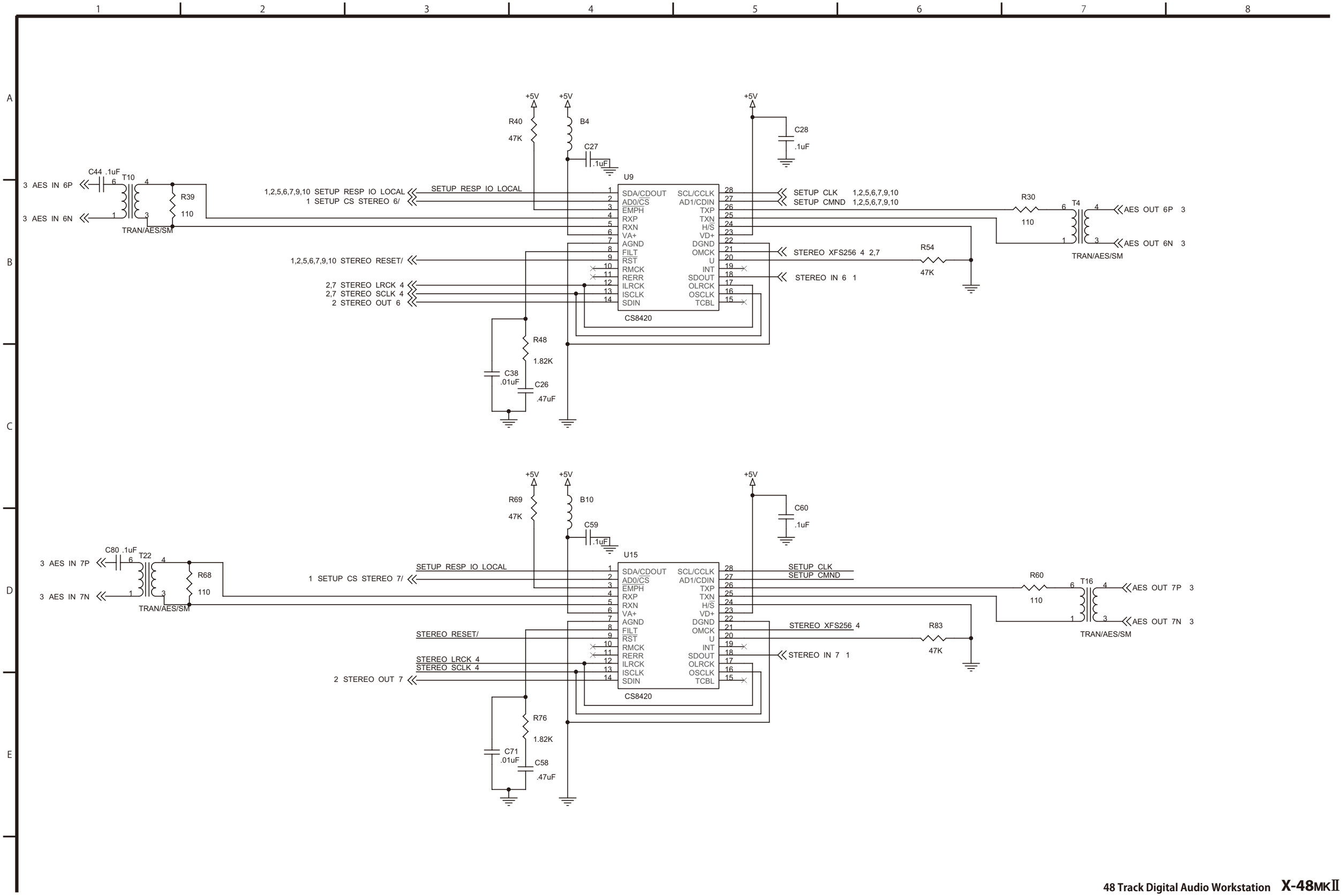


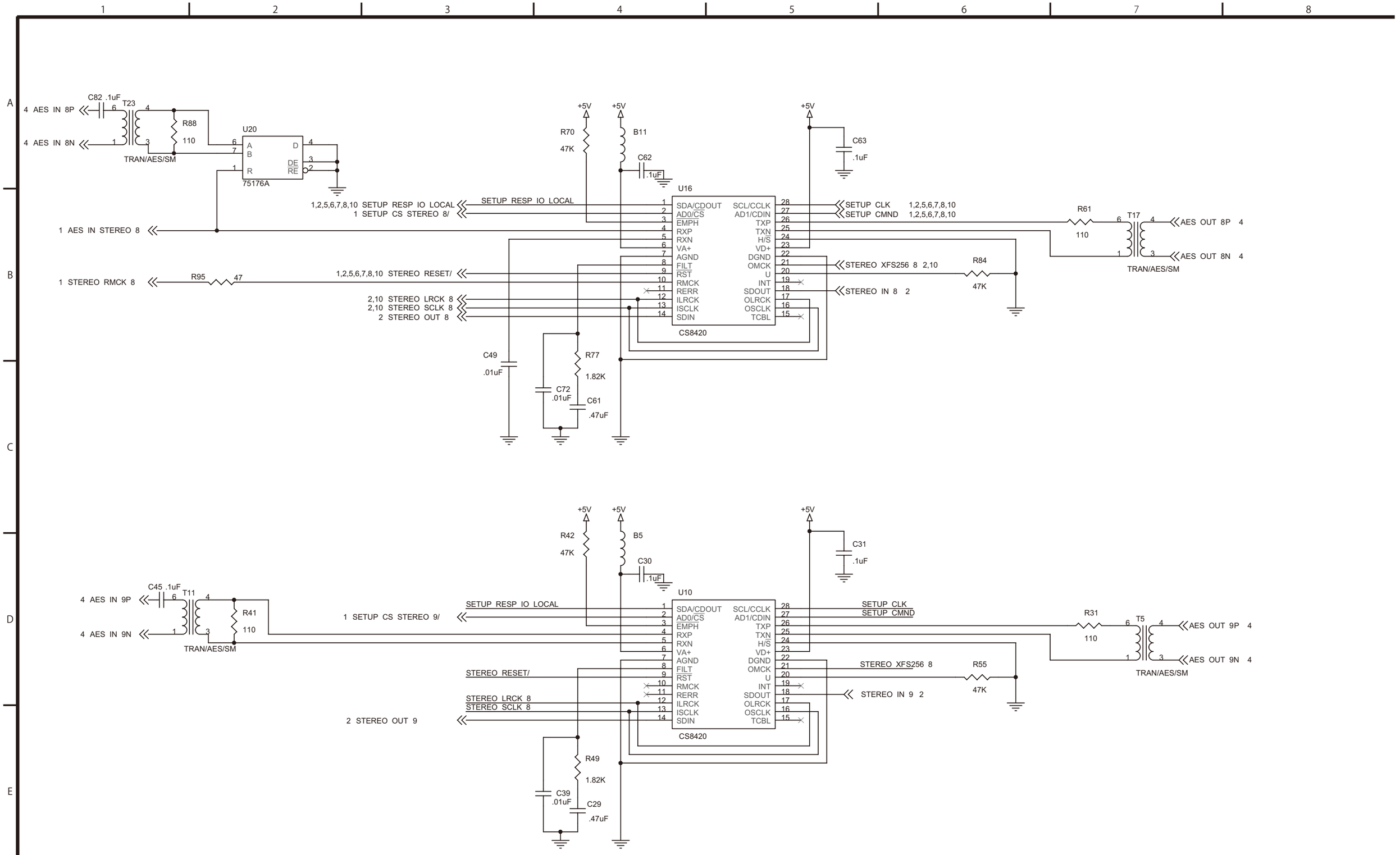

C76 .1uF
T19
3 AES IN 0P
3 AES IN 0N
R86
110
TRAN/AES/SM
U18
A
B
R
D
DE
RE
75176A
R63
10K
R64
47K
B7
C50
.1uF
+5V
C51
.1uF
1,2,6,7,8,9,10 SETUP RESP IO LOCAL
1 SETUP CS STEREO 0/
SETUP RESP IO LOCAL
U12
SDA/CDOUT
AD0/CS
EMPH
RXP
RXN
VA+
AGND
FILT
RST
RMCK
RERR
ILRCK
ISCLK
SDIN
SCL/CCLK
AD1/CDIN
TXP
TXN
H/S
VD+
DGND
OMCK
U
INT
SDOUT
OLRCK
OSCLK
TCBL
CS8420
SETUP CLK 1,2,6,7,8,9,10
SETUP CMND 1,2,6,7,8,9,10
R57
110
T13
AES OUT 0P 3
AES OUT 0N 3
TRAN/AES/SM
1 AES IN STEREO 0
1 STEREO RMCK 0
R93
47
1,2,6,7,8,9,10 STEREO RESET/
2,6 STEREO LRCK 0
2,6 STEREO SCLK 0
2 STEREO OUT 0
STEREO XFS256 0 2,6
R80
47K
STEREO IN 0 1,2
C47
.01uF
R73
10K
C68
.01uF
R79
1.82K
C74
.47uF
R34
47K
B1
C18
.1uF
C19
.1uF
C41 .1uF
T7
3 AES IN 1P
3 AES IN 1N
R33
110
TRAN/AES/SM
1 SETUP CS STEREO 1/
SETUP RESP IO LOCAL
STEREO RESET/
STEREO LRCK 0
STEREO SCLK 0
2 STEREO OUT 1
U6
SETUP CLK
SETUP CMND
STEREO XFS256 0
STEREO IN 1 1
R51
47K
R27
110
T1
AES OUT 1P 3
AES OUT 1N 3
TRAN/AES/SM
R45
1.82K
C35
.01uF
C17
.47uF


1
2
3
4
5
6
7
8
A
B
C
D
E
+5V
+5V
+5V
R66
47K
B8
C53
.1uF
C54
.1uF
U13
C77 .1uF
T20
3 AES IN 2P
3 AES IN 2N
R65
110
TRAN/AES/SM
1,2,5,7,8,9,10 SETUP RESP IO LOCAL
SETUP RESP IO LOCAL
1 SETUP CS STEREO 2/
SDA/CDOUT
AD0/CS
EMPH
RXP
RXN
VA+
AGND
FILT
RST
RMCK
RERR
ILRCK
ISCLK
SDIN
SCL/CCLK
AD1/CDIN
TXP
TXN
H/S
VD+
DGND
OMCK
U
INT
SDOUT
OLRCK
OSCLK
TCBL
CS8420
SETUP CLK 1,2,5,7,8,9,10
SETUP CMND 1,2,5,7,8,9,10
R58
110
T14
AES OUT 2P 3
AES OUT 2N 3
TRAN/AES/SM
1,2,5,7,8,9,10 STEREO RESET/
STEREO XFS256 0 2,5
R81
47K
STEREO IN 2 1
2,5 STEREO LRCK 0
2,5 STEREO SCLK 0
2 STEREO OUT 2
R74
1.82K
C69
.01uF
C52
.47uF
+5V
+5V
+5V
R36
47K
B2
C21
.1uF
C22
.1uF
U7
C42 .1uF
T8
3 AES IN 3P
3 AES IN 3N
R35
110
TRAN/AES/SM
SETUP RESP IO LOCAL
1 SETUP CS STEREO 3/
SDA/CDOUT
AD0/CS
EMPH
RXP
RXN
VA+
AGND
FILT
RST
RMCK
RERR
ILRCK
ISCLK
SDIN
SCL/CCLK
AD1/CDIN
TXP
TXN
H/S
VD+
DGND
OMCK
U
INT
SDOUT
OLRCK
OSCLK
TCBL
CS8420
SETUP CLK
SETUP CMND
R28
110
T2
AES OUT 3P 3
AES OUT 3N 3
TRAN/AES/SM
STEREO RESET/
STEREO XFS256 0
R52
47K
STEREO IN 3 1
STEREO LRCK 0
STEREO SCLK 0
2 STEREO OUT 3
R46
1.82K
C36
.01uF
C20
.47uF

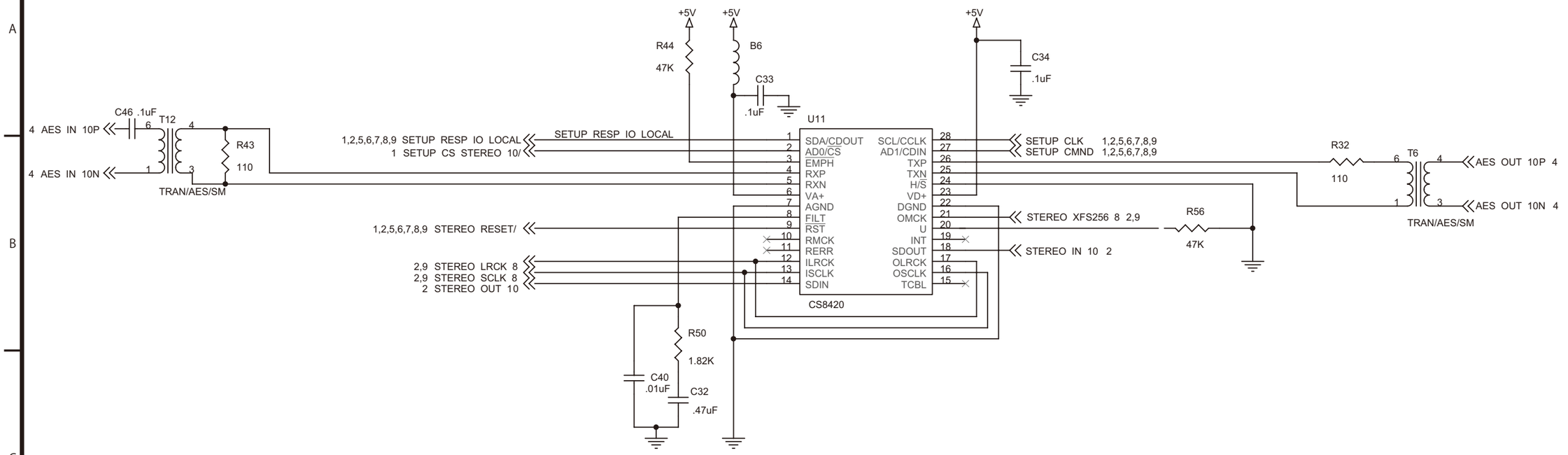

3 AES IN 4P
3 AES IN 4N
C79 .1uF
T21
R87
110
TRAN/AES/SM
U19
75176A
1 AES IN STEREO 4
1 STEREO RMCK 4
R94
47
+5V
R67
47K
B9
C56
.1uF
C57
.1uF
U14
CS8420
SDA/CDOUT
AD0/CS
EMPH
RXP
RXN
VA+
AGND
FILT
RST
RMCK
RERR
ILRCK
ISCLK
SDIN
SCL/CCLK
AD1/CDIN
TXP
TXN
H/S
VD+
DGND
OMCK
U
INT
SDOUT
OLRCK
OSCLK
TCBL
1,2,5,6,8,9,10 SETUP RESP IO LOCAL
1 SETUP CS STEREO 4/
SETUP RESP IO LOCAL
SETUP CLK 1,2,5,6,8,9,10
SETUP CMND 1,2,5,6,8,9,10
1,2,5,6,8,9,10 STEREO RESET/
2,8 STEREO LRCK 4
2,8 STEREO SCLK 4
2 STEREO OUT 4
STEREO XFS256 4 2,8
STEREO IN 4 1
R82
47K
R59 110
T15
AES OUT 4P 3
AES OUT 4N 3
TRAN/AES/SM
C48
.01uF
R75
1.82K
C70
.01uF
C55
.47uF
3 AES IN 5P
3 AES IN 5N
C43 .1uF
T9
R37
110
TRAN/AES/SM
R38
47K
B3
C24
.1uF
C25
.1uF
U8
CS8420
SETUP RESP IO LOCAL
1 SETUP CS STEREO 5/
STEREO RESET/
STEREO LRCK 4
STEREO SCLK 4
2 STEREO OUT 5
SETUP CLK
SETUP CMND
STEREO XFS256 4
STEREO IN 5 1
R53
47K
R29 110
T3
AES OUT 5P 3
AES OUT 5N 3
TRAN/AES/SM
R47
1.82K
C37
.01uF
C23
.47uF

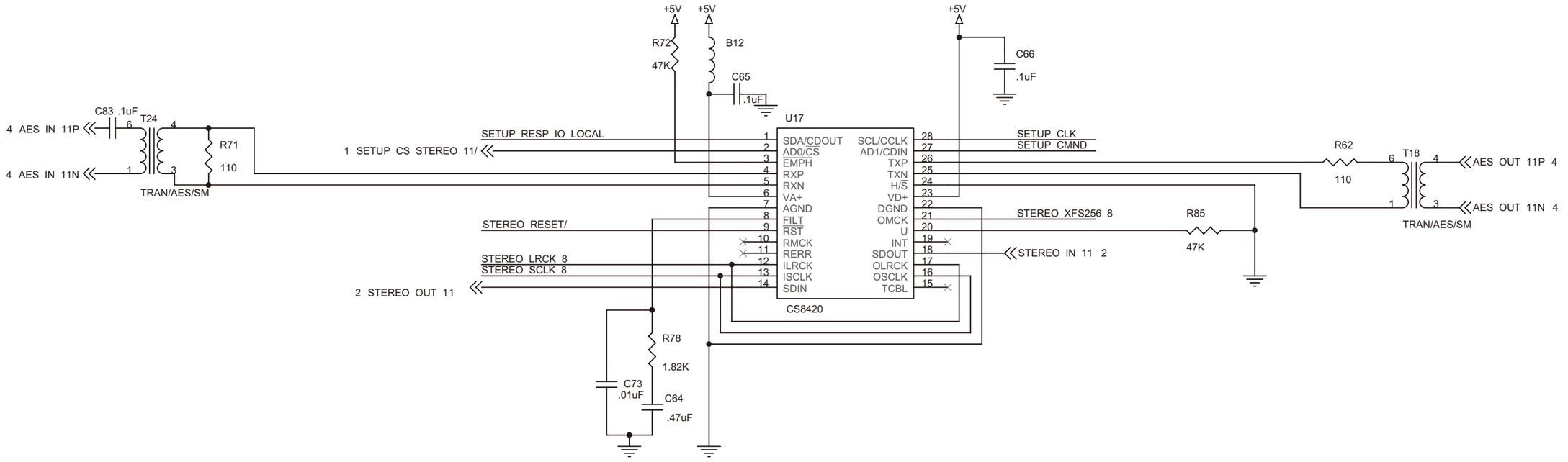
IF-AE24X (8/10) AES Interface 13-16



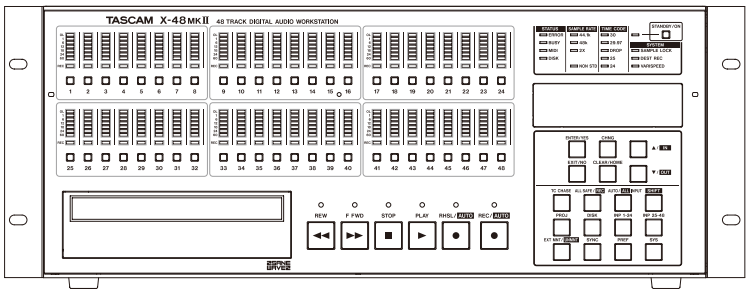

4 AES IN 8P
4 AES IN 8N
C82 .1uF
T23
R88
110
TRAN/AES/SM
U20
75176A
+5V
R70
47K
B11
C62
.1uF
C63
.1uF
U16
CS8420
SDA/CDOUT
AD0/CS
EMPH
RXP
RXN
VA+
AGND
FILT
RST
RMCK
RERR
ILRCK
ISCLK
SDIN
SCL/CCLK
AD1/CDIN
TXP
TXN
H/S
VD+
DGND
OMCK
U
INT
SDOUT
OLRCK
OSCLK
TCBL
1,2,5,6,7,8,10 SETUP RESP IO LOCAL
1 SETUP CS STEREO 8/
SETUP RESP IO LOCAL
SETUP CLK 1,2,5,6,7,8,10
SETUP CMND 1,2,5,6,7,8,10
1 AES IN STEREO 8
1 STEREO RMCK 8
R95
47
1,2,5,6,7,8,10 STEREO RESET/
2,10 STEREO LRCK 8
2,10 STEREO SCLK 8
2 STEREO OUT 8
STEREO XFS256 8 2,10
STEREO IN 8 2
R84
47K
R61
110
T17
AES OUT 8P 4
AES OUT 8N 4
TRAN/AES/SM
C49
.01uF
R77
1.82K
C72
.01uF
C61
.47uF
4 AES IN 9P
4 AES IN 9N
C45 .1uF
T11
R41
110
TRAN/AES/SM
U10
CS8420
R42
47K
B5
C30
.1uF
C31
.1uF
1 SETUP CS STEREO 9/
SETUP RESP IO LOCAL
STEREO RESET/
STEREO LRCK 8
STEREO SCLK 8
2 STEREO OUT 9
SETUP CLK
SETUP CMND
STEREO XFS256 8
STEREO IN 9 2
R55
47K
R31
110
T5
AES OUT 9P 4
AES OUT 9N 4
TRAN/AES/SM
R49
1.82K
C39
.01uF
C29
.47uF

IF-AE24X (10/10) AES Interface 21-24





TASCAM



SERVICE MANUAL

X-48MKII

48 Track Digital Audio Workstation

CONTENTS

目次

INSTRUCTIONS FOR SERVICE PERSONNEL

BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

Effective : July, 2011

S-0226

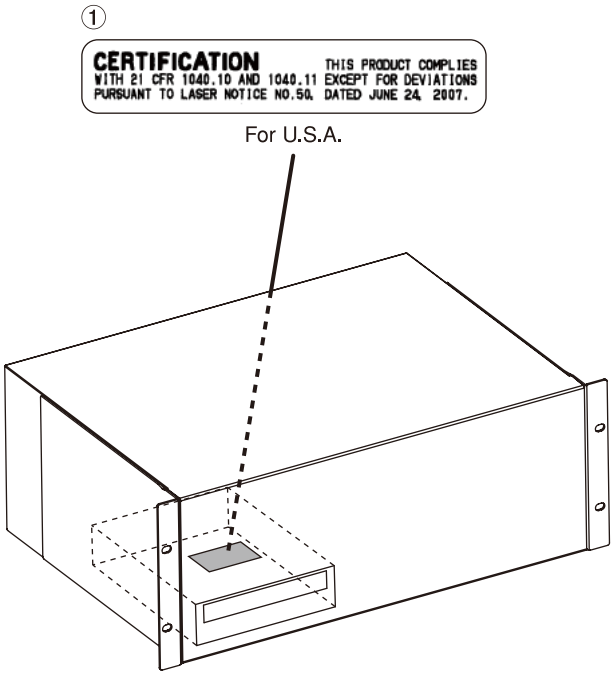
1. SAFETY INFORMATION

安全規格

This product has been designed and manufactured according to FDA regulations "title 21, CFR, chapter 1, subchapter J, based on the Radiation Control for Health and Safety Act of 1968", and is classified as a class 1 laser product. There is no hazardous invisible laser radiation during operation because invisible laser radiation emitted inside of this product is completely confined in the protective housings.
The label required in this regulation is shown.

● **CAUTION**

USE OF CONTROLS OR ADJUSTMENT OR PERFORMANCE OF PROCEDURES OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.



Optical pickup :	Type	: OWY 8/35, OWY 8/36, OWY8/44, OWY8/45
	Manufacturer	: Pioneer CORP.
	Laser output (CD)	: Less than 1.3mW (Play) and 104.7mW (Record) on the objective lens
	(DVD)	: Less than 1.08mW (Play) and 102mW (Record) on the objective lens
	Wavelength	: 777-787 nm(CD), 656-663 nm(DVD)

● **CAUTION**

Danger of explosion if battery is incorrectly replaced.
Replace only with the same or equivalent type.

2. Specifications

仕様

Audio I/O

TDIF	6 x 25-pin (female) -sub connectors Conform to TDIF-1 standard
S/PDIF IN/OUT	2 x RCA pin jacks (input/output impedance 75ohm) IEC60958 data format

Miscellaneous I/O connections

WORD SYNC IN	BNC connector Switchable 75ohm termination TTL level
WORD SYNC OUT/THRU	2 x BNC connector TTL level
VIDEO IN/THRU	2 x BNC connector Tri-level signal supported
MIDI IN/OUT	2 x 5-pin DIN connectors Conform to MIDI specifications
TIME CODE IN/OUT	2 x 1/4" TRS jacks Conform to SMPTE specifications
FOOT SWITCH	1/4" TS jack
REMOTE (for only 9-pin)	9-pin female D-sub connector Wired to RS-422 standards
USB	4 x USB 2.0 'A' type connectors
10/100/1000	RJ45 LAN connector 10BASE-T/100BASE-TX/1000BASE-TX Ethernet
10/100	RJ45 LAN connector 10BASE-T/100BASE-TX Ethernet
VGA	15-pin female Dsub VGA connector
MOUSE	PS/2 Mouse port
KEYBOARD	PS/2 Keyboard port
eSATA	eSATA connector

オーディオ入出力

TDIF コネクター（× 6）:
コネクター　　: 25 ピンD サブ（メス）コネクター
データフォーマット : TDIF-1 規格準拠
ワード長　　: 24 ビット

S/PDIF IN、S/PDIF OUT 端子 :
コネクター　　: RCA ピンジャック
データフォーマット : IEC60958（S/PDIF）

各種入出力

WORD SYNC IN 入力端子 :
コネクター　: BNC（アンバランス）
TTL レベル、75 Ω終端ON/OFF 切替

WORD SYNC THRU、WORD SYNC OUT 出力端子 :
コネクター　: BNC（アンバランス）
TTL レベル、75 Ω

MIDI IN、MIDI OUT 端子 :
コネクター　: 5 ピンDIN コネクター
MIDI 規格準拠

TIME CODE IN、TIME CODE OUT 端子 :
コネクター　: TRS ホンジャック
SMPTE 規格準拠

FOOT SW 端子 :
コネクター　: 6 φ、2 極ホンジャック

REMOTE 端子 :
コネクター　: 9 ピンD サブ（メス）
RS-422 準拠、ソニー 9 ピンシリアルプロトコル（P2）

USB ポート（× 4）:
コネクター　: USB2.0A タイプコネクター

10/100/1000 ポート :
コネクター　: RJ45 LAN コネクター
10BASE-T/100BASE-TX/
1000BASE-TX イーサネット

10/100 ポート :
コネクター　: RJ45 LAN コネクター
10BASE-T/100BASE-TX イーサネット

VGA ポート :
コネクター　: 15 ピンD サブ（メス）VGA コネクター

MOUSE ポート :
コネクター　: PS/2 マウスポート

KEYBOARD ポート :
コネクター　: PS/2 キーボードポート

eSATAポート :
コネクター　: eSATAコネクター

Physical characteristics

Maximum overall dimensions (W x D x H) :
483 x 439 x 184 (mm)
9 x 17.3 x 7.3 (in)

Weight : 13.7kg (30.2lbs)

Voltage requirements : 120VAC, 0Hz
230VAC, 0Hz
240VAC, 0Hz

Power consumption : 49W

Supplied accessories : Power cord
Owner's manual
Quick reference guide
System restore CD
Documentation CD
Two white plastic spacers and screws
for installation of digital cards (IFAE24/IF-AD24)

物理的仕様

外形寸法 : 483（幅）x 439（幅）x 184（高さ）mm

質量 : 3.7kg

電源 : 100V、50 / 60Hz AC

消費電力 : 49W

付属品 : 電源コード × 1
取扱説明書 × 1
クイックリファレンスガイド × 1
システムリストアCD × 1
ドキュメンテーションCD × 1
プラスチックスペーサ / ビス (デジタルカード取り付け用) × 1
保証書 × 1

● 仕様・外観などは、改善のため予告なく変更することがあります。

3. Hardware Test

ハードウェアーのテスト

Summary

This document describes required test program which is to test the hardware of X-48MK II at the production line. Since a whole hardware including PCBs and wires have to be tested at the production line easily after X-48MK II is fabricated, a unique hardware test program is necessary in the X-48MK II main programs. This test program should be executed without display, mouse, keyboard and other external devices except "loopback cable" which is used for I/O loop back test.

Flow of hardware test at the production line

Overall flow of production test process is shown in Fig1

1. How to enter the test mode
   After turning on the power, press and hold down the following key combination to enter the test mode:
   "**ENTER/YES**" key + "**EXIT/NO**" key : Enter the test mode
2. How to exit the test mode
   Press "CLEAR/HOME" key when in the test mode.
   "**CLEAR/HOME**" key : Exit the test mode

概要

本書では、生産ラインでのX-48MK II ハードウェア試験に使用するプログラムについて説明します。PCB、配線を含むハードウェアはすべて、X-48MK II の製作終了後生産ラインにて試験する必要があるため、X-48MK II のメインプログラム内に専用のハードウェア試験プログラムが必要です。この試験プログラムは、画面モニター、マウス、キーボード、その他の外部装置を使用せずに実行します。
ただし、I/O ループバック試験では「ループバックケーブル」を使用します。

生産ラインでのハードウェア試験の流れ

図 1 は生産試験工程の全体の流れ図を示しています。

1. 試験モードへ入る
   電源を入れ、以下のキーの組み合わせで長押しすると試験モードに入ります。
   "ENTER/YES"キー＋**"EXIT/NO"** キー : 試験モードに入ります。
2. 試験モードを終了する
   試験モード中に**"CLEAR/HOME"**キーを押します。
   "CLEAR/HOME" キー : 試験モードを終了します。

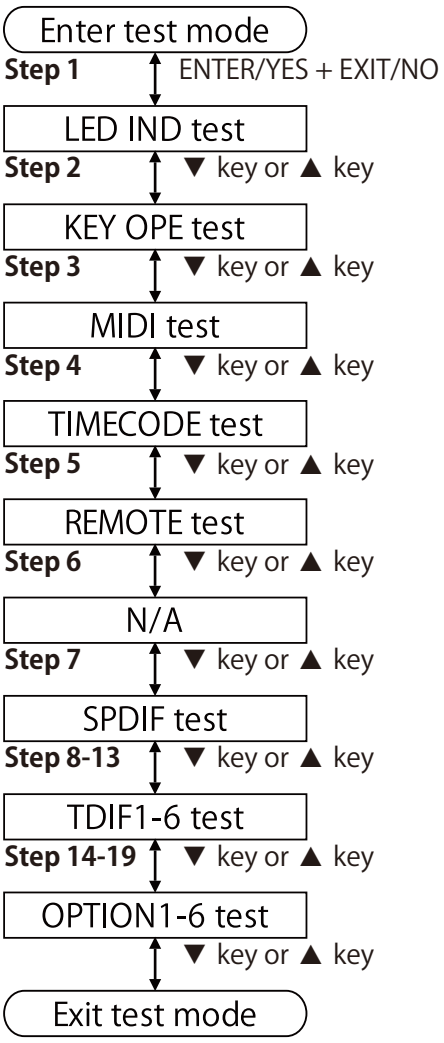


Fig.1 図1

3. Test step details

The hardware test at the production line will usually proceed to the next step in accordance with the figure 1 by pressing "Down arrow" key. However, each test can be freely selected by pressing "Up arrow" key and "Down arrow" key.

The current test step, test name and result of the test are displayed on the LCD screen as shown in Fig.2.

3. 試験ステップの詳細

生産ラインでのハードウェア試験は図1 のように、下矢印キーを押すごとに次のステップに順に進んでいきますが、上矢印 / 下矢印キーを押して任意の試験を選ぶこともできます。

現在の試験ステップ、試験名、試験結果が図2 のようにLCD画面に表示されます

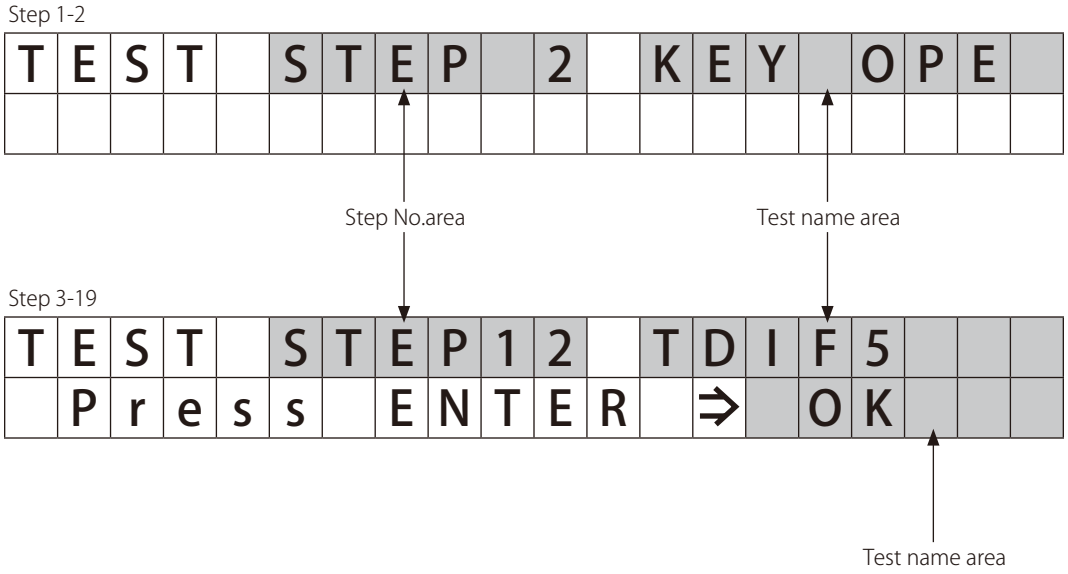


Fig.2 図2

3.1 Step 1: LED indicate test (LED IND)

This step tests all LEDs and circuits around LED drivers.

[Default status]

All LEDs on the front panel turn on in this step.

[Testing]

Visual check is made with default status. No display of result is needed.

3.1 ステップ1: LED 表示試験(LED IND)

全LED とLED ドライバ周辺の回路を試験します。

[初期状態]

フロントパネルの全LED がこのステップで点灯します。

[試験方法]

初期状態で視認検査。結果表示は不要。

3.2 Step 2 : Key operation test (KEY OPE)

This step tests all keys on the front panel and their scan circuits, except EXIT/NO key and UP/DOWN arrow keys.

[Default status]

All LEDs on the front panel are turned off.

[Testing]

If a certain key is pressed, then the LED status of the key is turned over (on -> off or off -> on).
Since visual check is made, no display of result is needed.

From Step3 to Step19, inputs and outputs on the rear panel are tested with cables or unique loopback connectors which are specially made for the test. Each step test a connector or a set of I/O connectors by comparing output data and "loopbacked input data". If output data is same with input data, it means the hardware for the interface has no problem and "OK" is displayed in the result area on the LCD screen. If not, "NG" is displayed.

3.3 Step 3 : MIDI test (MIDI)

This step tests MIDI input and output.

[External connection]

A normal MIDI cable is necessary and MIDI input and MIDI output are connected with the cable.

[Testing]

Compare random MIDI output data with loopbacked data, and display the result.

3.4 Step 4 : Timecode test (TIMECODE)

This step tests TIMECODE input and output.

[External connection]

A normal 1/4 inch balance cable is necessary and TiMECODE input and TIMECODE output are connected with the cable.

[Testing]

Compare timecode data output with loopbacked data, and display the result.

3.2 ステップ2 : キー動作試験(KEY OPE)

EXIT/NO キーおよび上下矢印キー以外の、フロントパネルの全キーとそのスキャン回路を試験します。

[初期状態]

フロントパネルの全インジケータが消灯します。

[試験方法]

任意のキーを押すと、そのキーのインジケータの状態が逆になります（オン->オフ、またはオフ->オン）。
視認検査のため結果表示は不要。

ステップ3 ～ 19 では、試験用のケーブルまたは専用のループバックコネクタを使用して、リアパネルの入出力を試験します。各ステップでは、出力データと「ループバックされた入力データ」とを比較することで、個々のコネクタまたはI/O コネクタを試験します。出力データが入力データと同じであれば、インターフェース用のハードウェアに異常はなく、LCD 画面の結果表示領域には"OK"と表示されます。異常があると"NG"と表示されます。

3.3 ステップ3 : MIDI 試験(MIDI)

MIDI 入出力を試験します。

[外部接続]

標準のMIDI ケーブルで、MIDI IN とMIDI OUT を接続します。

[試験方法]

適当なMIDI 出力データとループバックデータを比較し、結果を表示します。

3.4 ステップ4 : タイムコード試験(TIMECODE)

TIMECODE 入出力を試験します。

[外部接続]

標準の1/4 インチバランス型ケーブルを使用し、TIMECODE入出力端子を接続します。

[試験方法]

タイムコードデータの出力をループバックデータと比較し、その結果を表示します。

3.5 Step 5 : REMOTE test

This step tests REMOTE(RS-422) input and output.

[External connection]

A unique connector with cable which connects TxD and RxD each other, is necessary.

[Testing]

Compare random output data with loopbacked input data, and display the result.

3.6 Step 6 : N/A

This step is not available.
Display "N/A" as the test name.

3.7 Step 7 : SPDIF test (SPDIF)

This step tests SPDIF input and output.

[External connection]

A normal RCA pin cable is necessary, and SPDIF input and SPDIF output are connected with the cable.

[Testing]

Compare random audio output data with loopbacked data, and display the result.

3.8 Step 8-13 : TDIF1-6 test (TDIFx)

Each step tests TDIF inputs and outputs in a TDIF connector.

[External connection]

A unique connector with cable which connects each input and output signal each other, is necessary.

[Testing]

Compare random audio output data with loopbacked data, and display the result.

3.9 Step 14-19 : Option 1-6 test (OPTIONx)

Each step tests inputs and outputs for a option slot interface with a IF-AE24.

[External connection]

A unique connector with cable which connects each input and output signal each other, is necessary.

[Testing]

Compare random audio output data with loopbacked data, and display the result.

3.5 ステップ5 : REMOTE 試験

このステップではREMOTE(RS-422)入出力を試験します。

[外部接続]

TxD およびRxD を接続する専用のコネクタケーブルが必要です。

[試験方法]

適当な出力データとループバックされた入力データを比較し、結果を表示します。

3.6 ステップ6 : N/A

このステップは利用できません。
試験名として"N/A"と表示されます。

3.7 ステップ7 : SPDIF 試験 (SPDIF)

このステップはSPDIF 入出力を試験します。

[外部接続]

標準のRCA ピンケーブルを使用し、SPDIF 入出力端子を接続します。

[試験方法]

適当なオーディオ出力データとループバックされたデータを比較し、結果を表示します。

3.8 ステップ8 ～ 13 : TDIF1 ～ 6 試験 (TDIFx)

各ステップで、TDIF コネクタ内のTDIF 入出力を試験します。

[外部接続]

入出力信号を互いに接続する専用のコネクタケーブルが必要です。

[試験方法]

適当なオーディオ出力データとループバックされたデータを比較し、結果を表示します。

3.9 ステップ14 ～ 19 : オプション1 ～試験 (OPTIONx)

各ステップでIF-AE24 を使用してスロットインターフェースの入出力を試験します。

[外部接続]

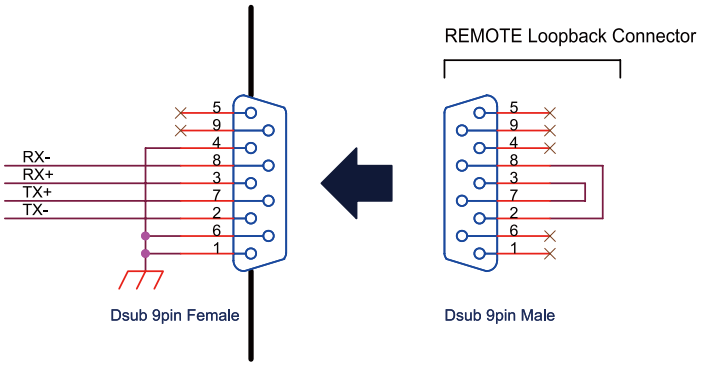
入出力信号を相互に接続する特殊なコネクタケーブルが必要です。

[試験方法]

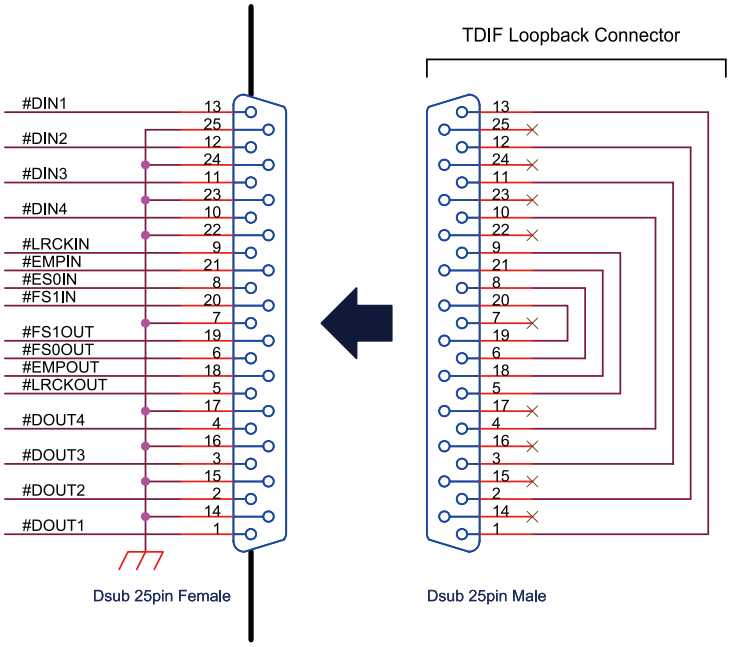
適当なオーディオ出力データとループバックされたデータを比較し、結果を表示します。

Loopback connectors for X-48MK II hardware testing

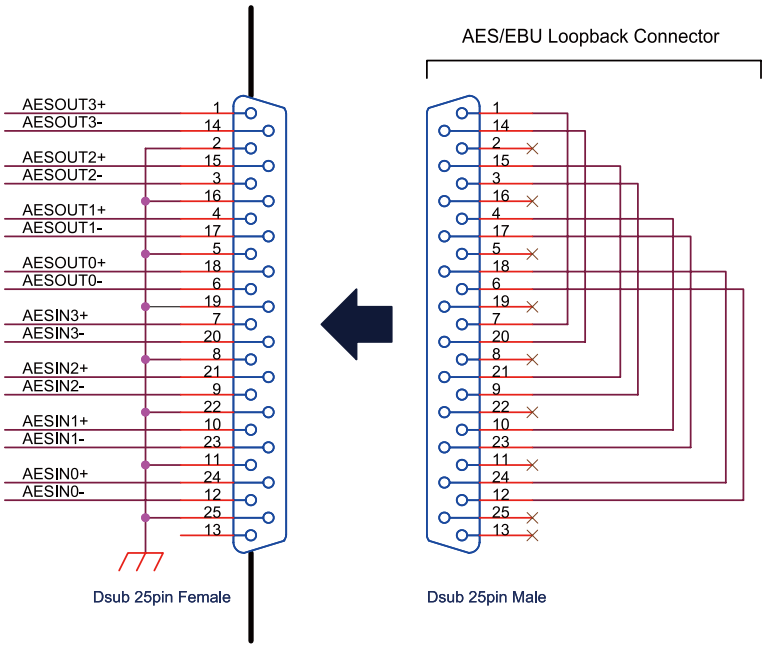
(1) REMOTE (Step5)



(2) TDIF (Step8-13)



(3) AES/EBU (Step14-19)



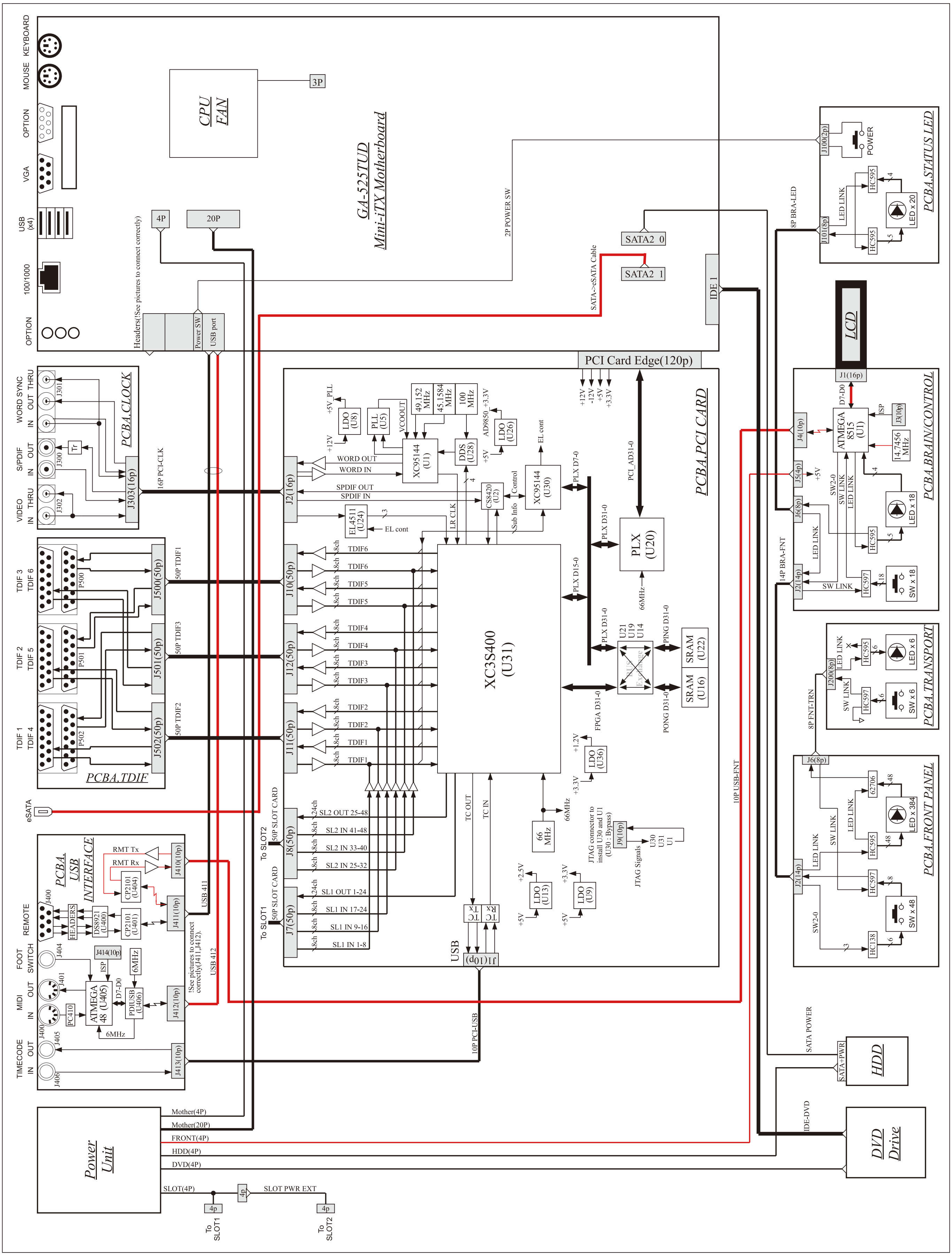
X-48MK II hardware bugs and related hardware

Category	Symptoms of bugs	Referenced hardware(*1)
Overall Front panel	No LED turns on. Perfectly Non-operative. LCD displays nothing.	X-48MK II _hw_FrontPanel (Refer to page 11)
Sample lock	X-48MK II unlocks when clock source = "Internal". X-48MK II unlocks with a proper external clock."	X-48MK II _hw_clock (Refer to page 12)
Foot Switch test	Foot switch doesn't work.	X-48MK II _hw_FootSwitch (Refer to page 13)
HW test Step1	Test result = ND.	X-48MK II _hw_Step1 (Refer to page 14)
HW test Step2	Test result = ND.	X-48MK II _hw_Step2 (Refer to page 15)
HW test Step3	Test result = ND.	X-48MK II _hw_Step3 (Refer to page 16)
HW test Step4	Test result = ND.	X-48MK II _hw_Step4 (Refer to page 17)
HW test Step5	Test result = ND.	X-48MK II _hw_Step5 (Refer to page 18)
HW test Step7	Test result = ND.	X-48MK II _hw_Step7 (Refer to page 19)
HW test Step8-13	Test result = ND.	X-48MK II _hw_Step8-13 (Refer to page 20)
HW test Step14-16	Test result = ND.	X-48MK II _hw_Step14-16 (Refer to page 21)
HW test Step17-19	Test result = ND.	X-48MK II _hw_Step17-19 (Refer to page 22)

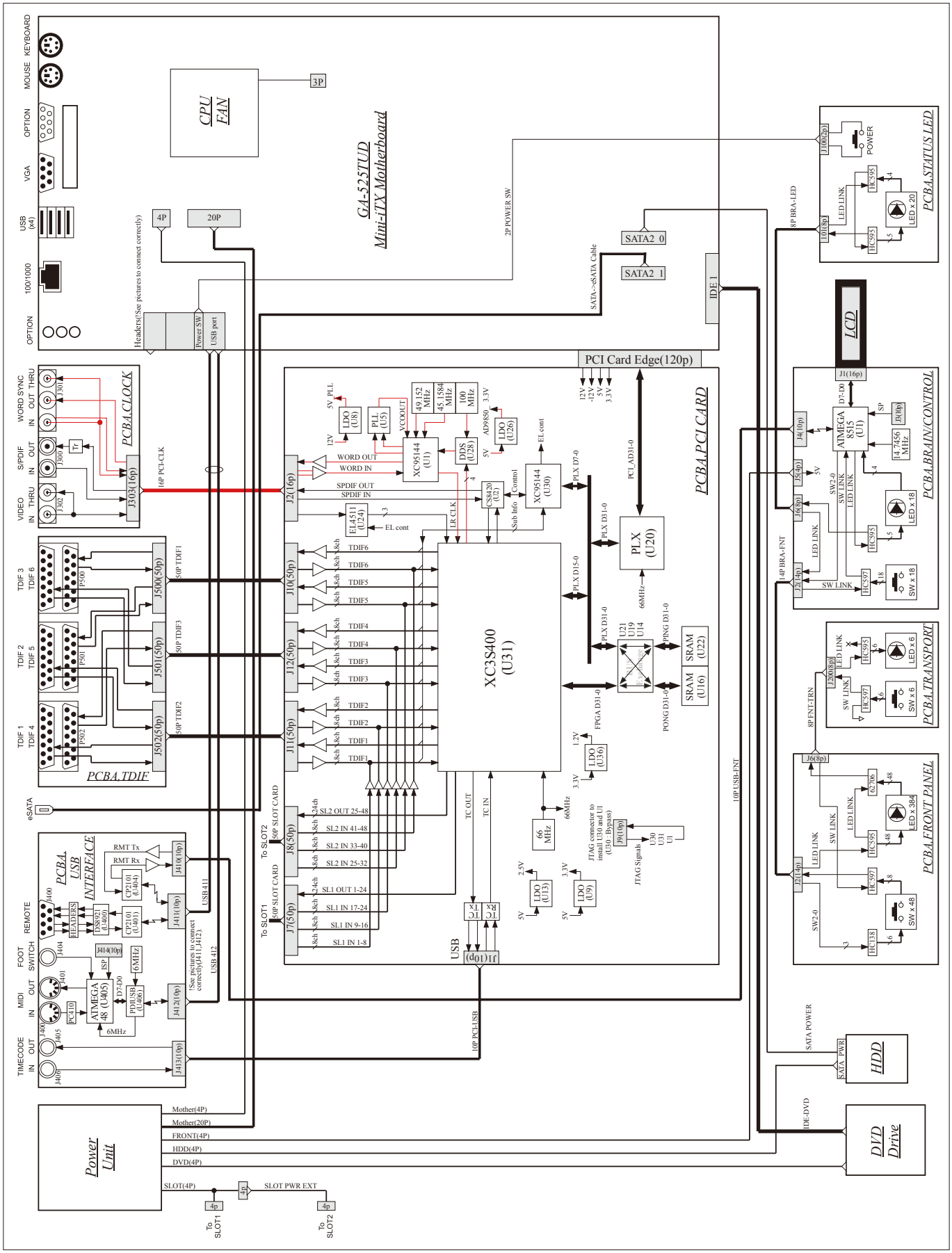
(*1) In each of the pdf files, hardware related to the bug is highlighted in red.
To find out the cause, you should check all parts (including cables and solderings) connected to the red signals."

(*1) 各PDF ファイル内で、バグに関連したハードウェアは赤で表示されています。
原因究明には、赤い信号に接続されているすべてのパーツ（ケーブルおよびハンダ部を含む）を点検してください。

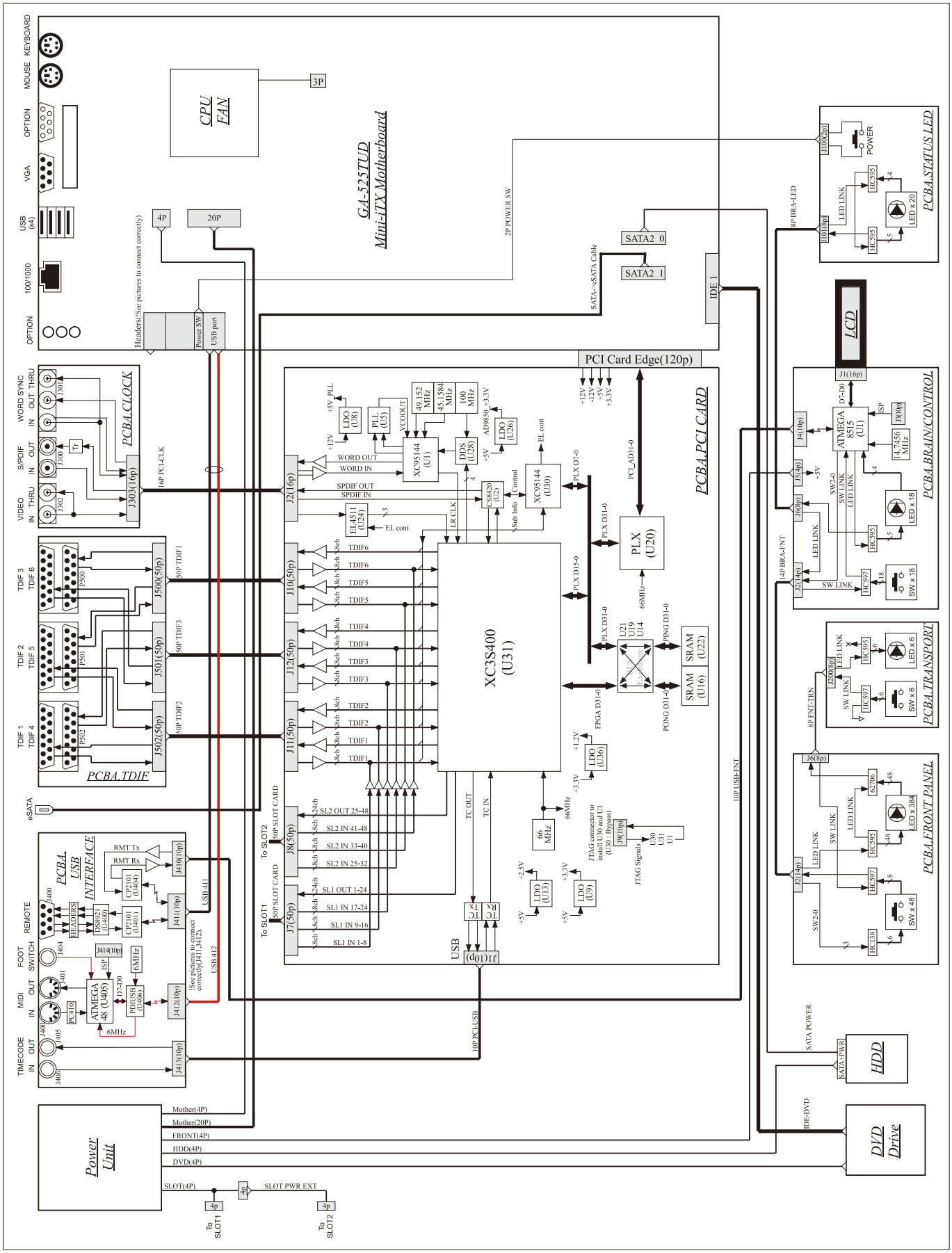
X-48MK II _hw_FrontPanel



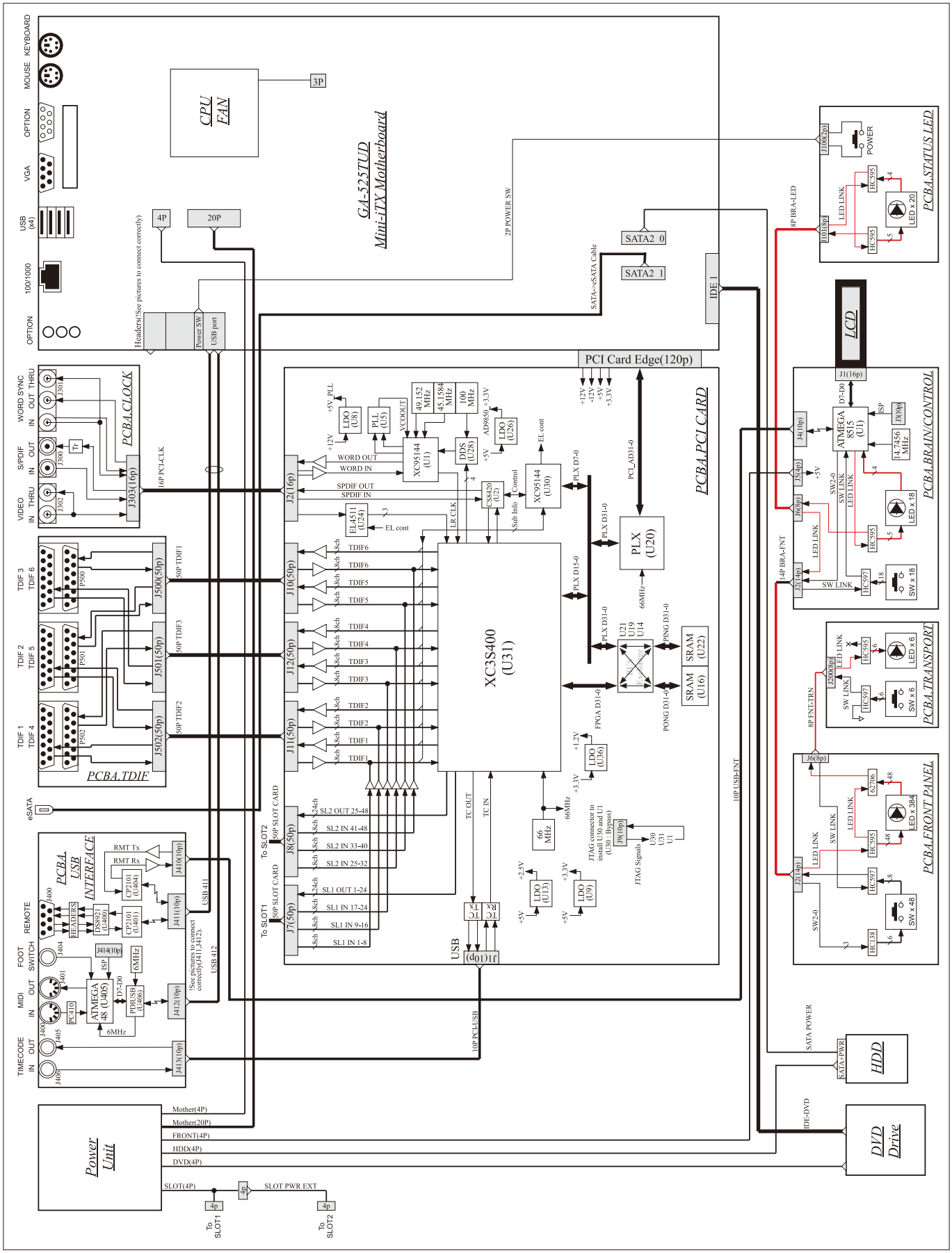
X-48MK II _hw_clock



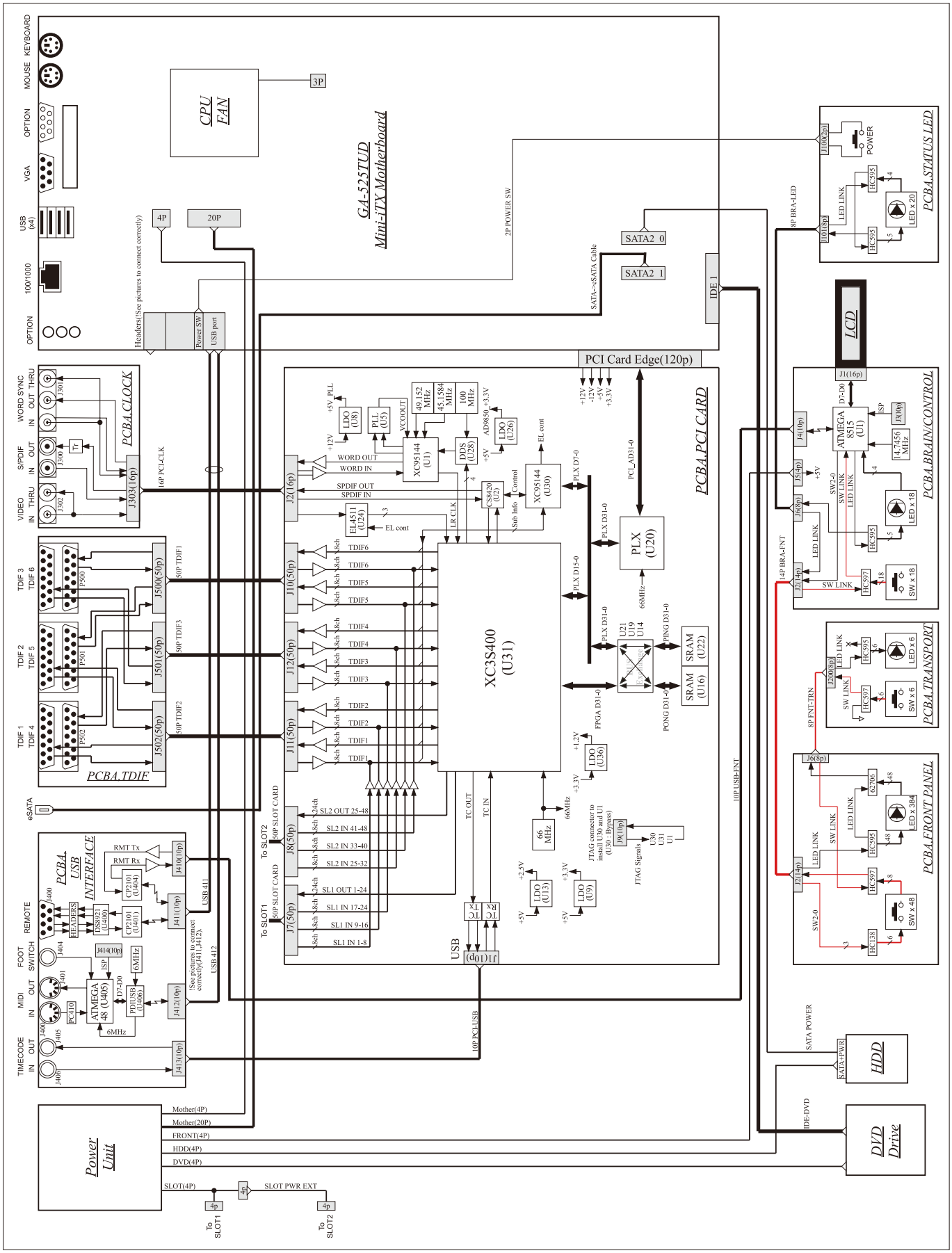
X-48MK II _hw_FootSwitch



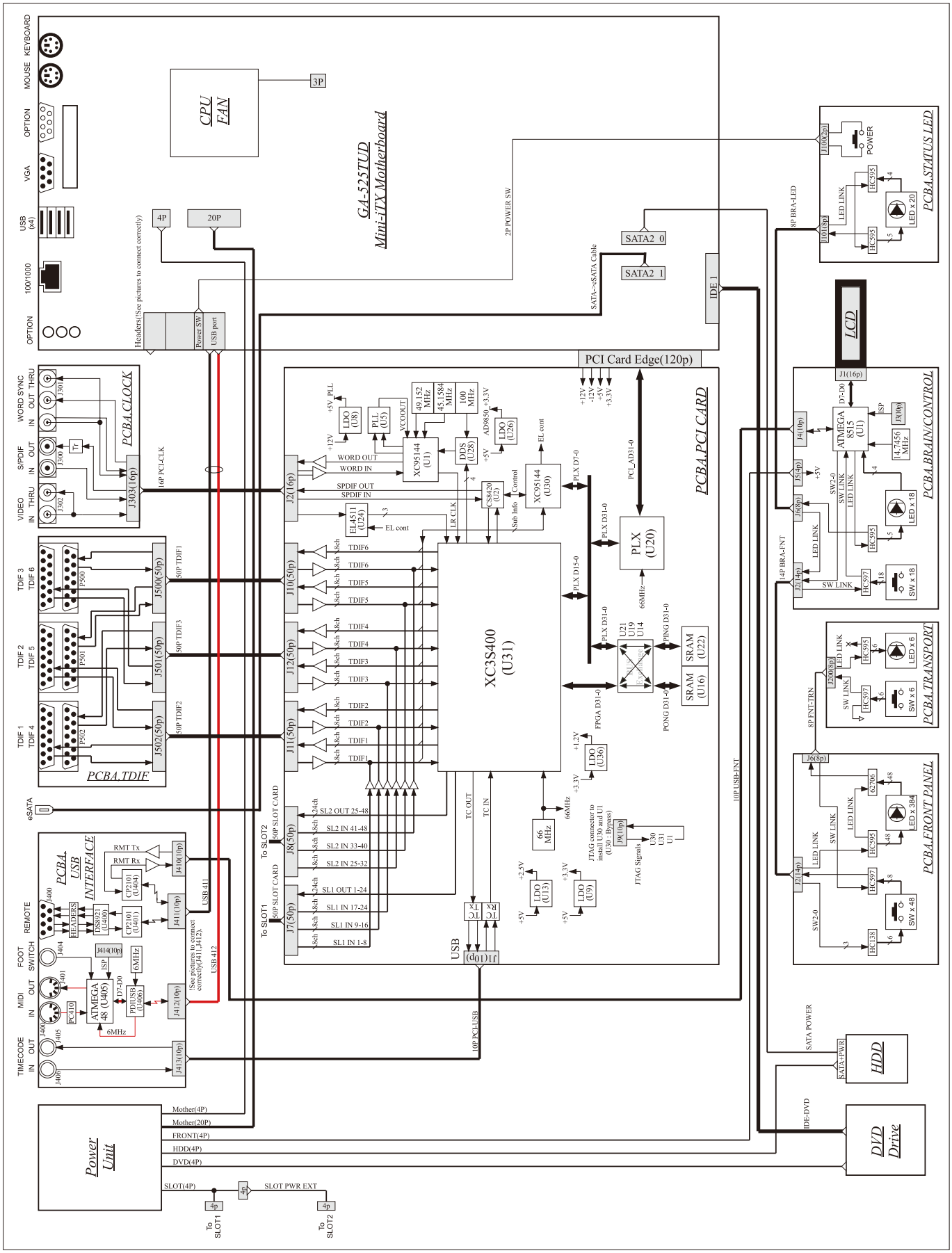
X-48MK II _hw_Step1



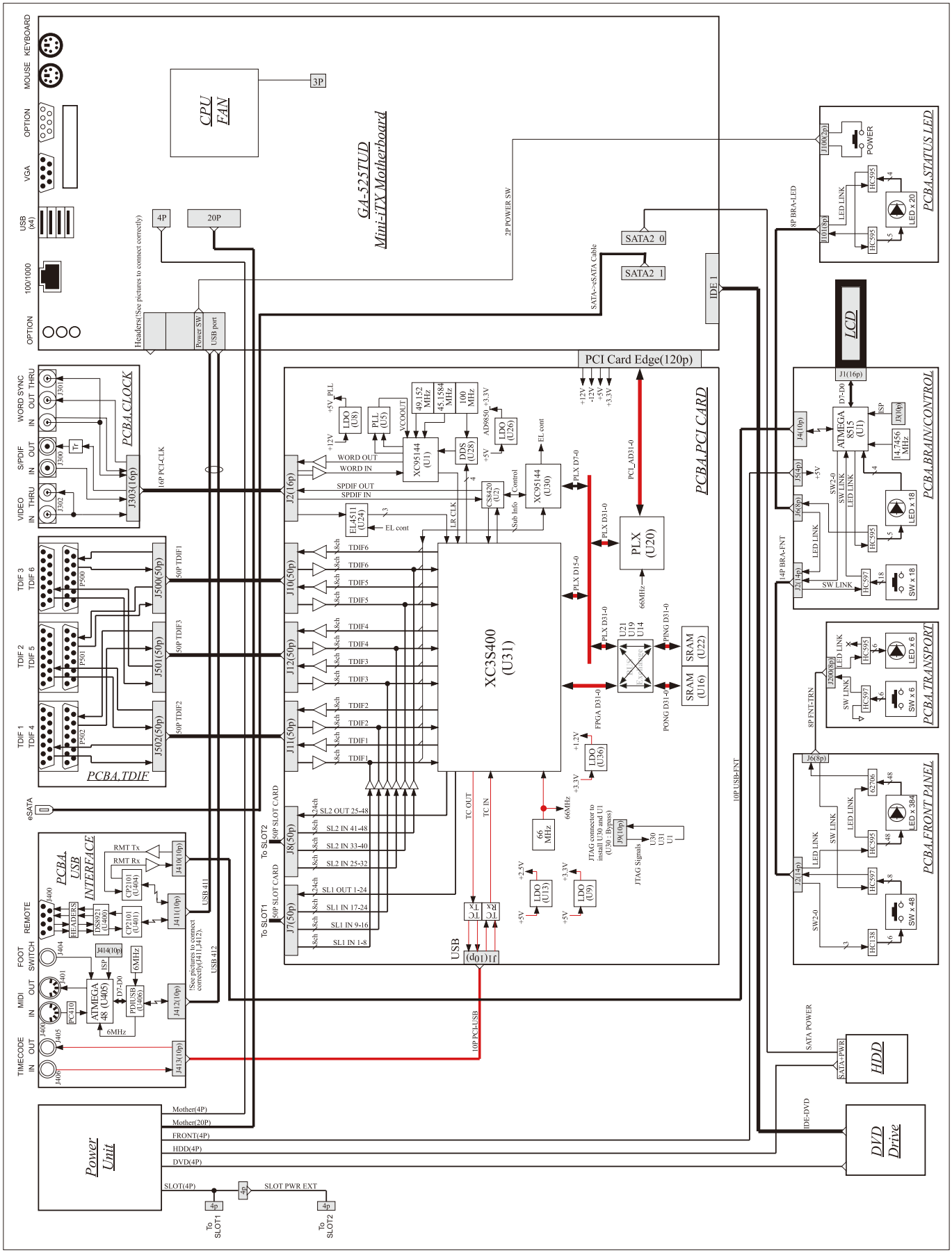
X-48MK II _hw_Step2



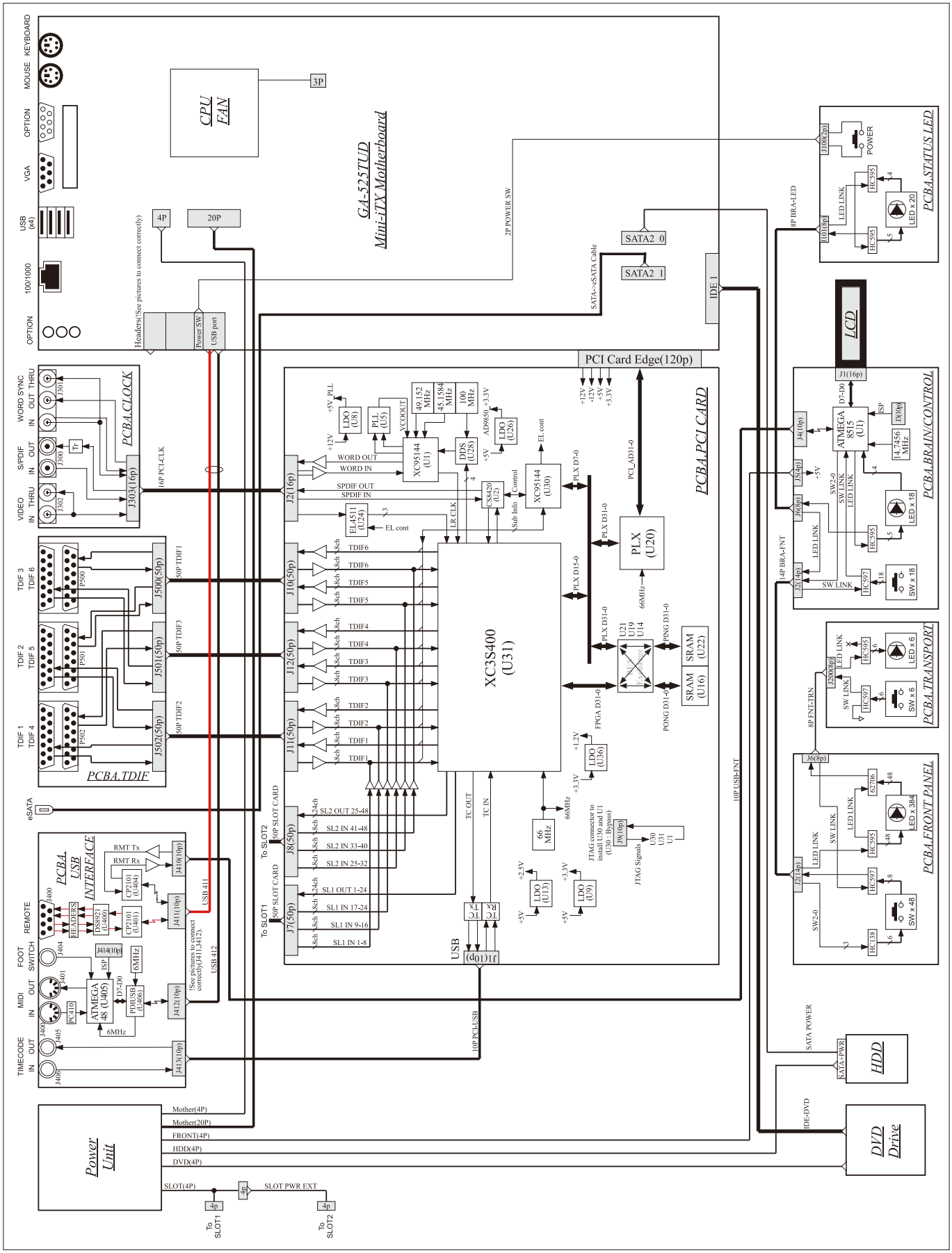
X-48MK II _hw_Step3



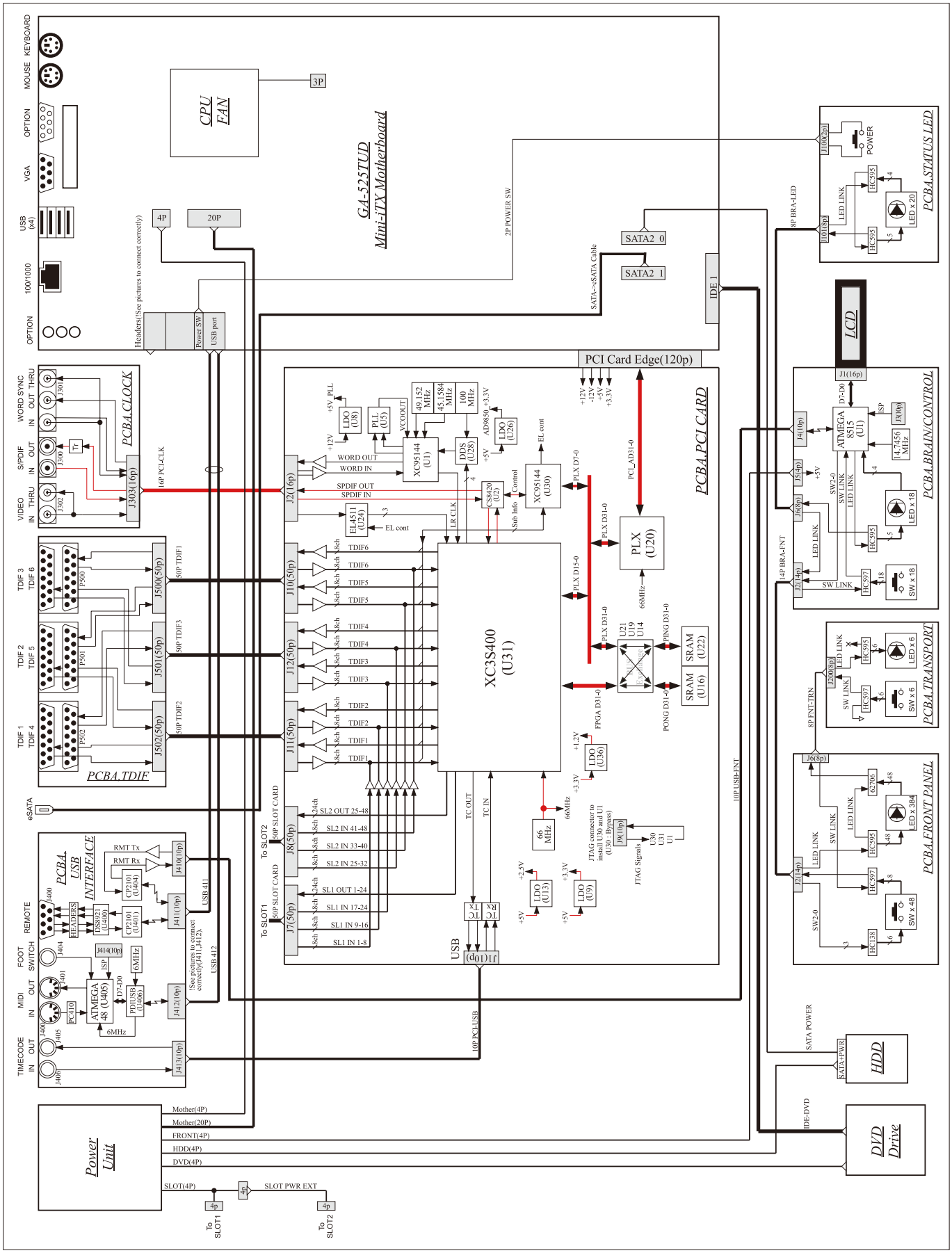
X-48MK II _hw_Step4



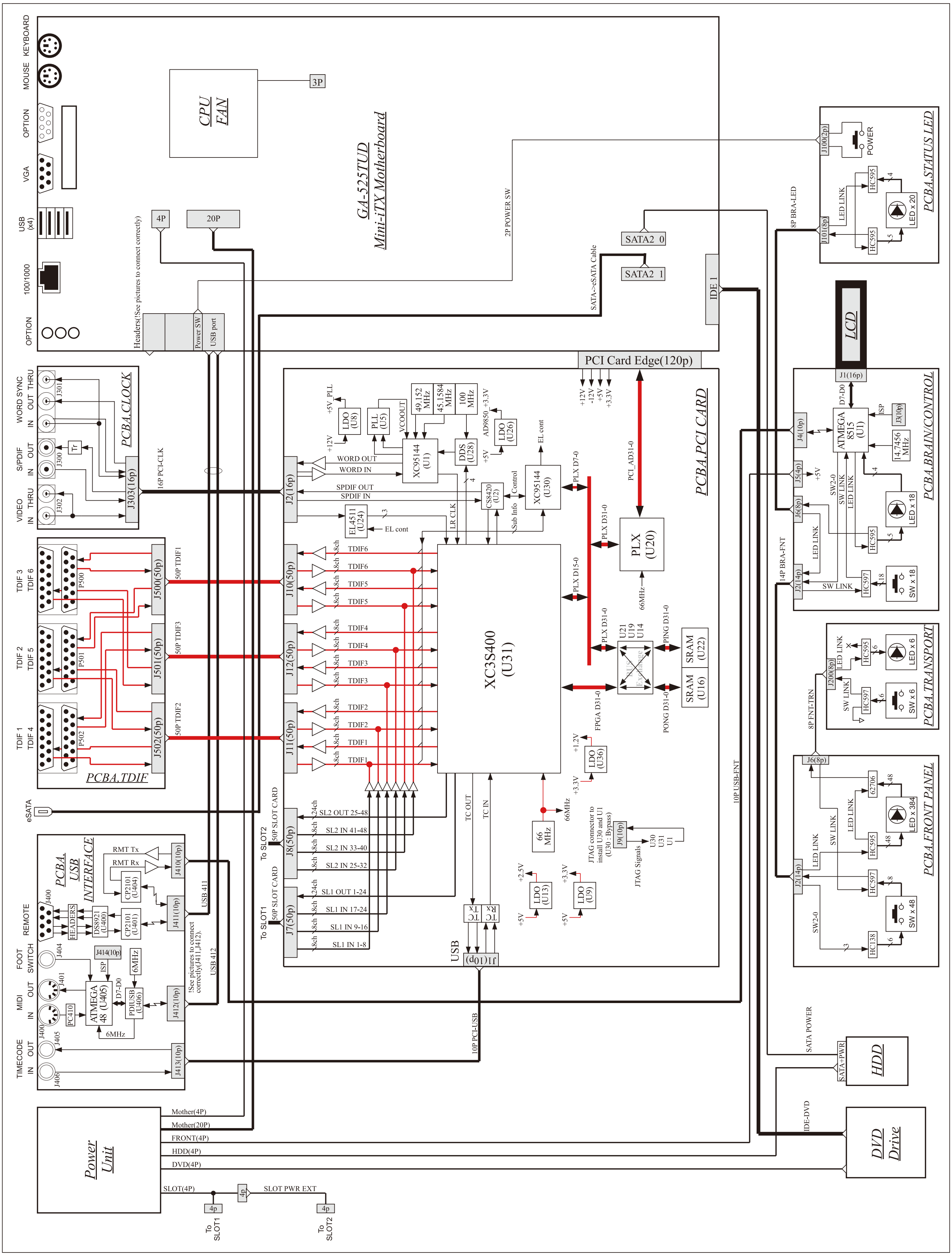
X-48MK II _hw_Step5



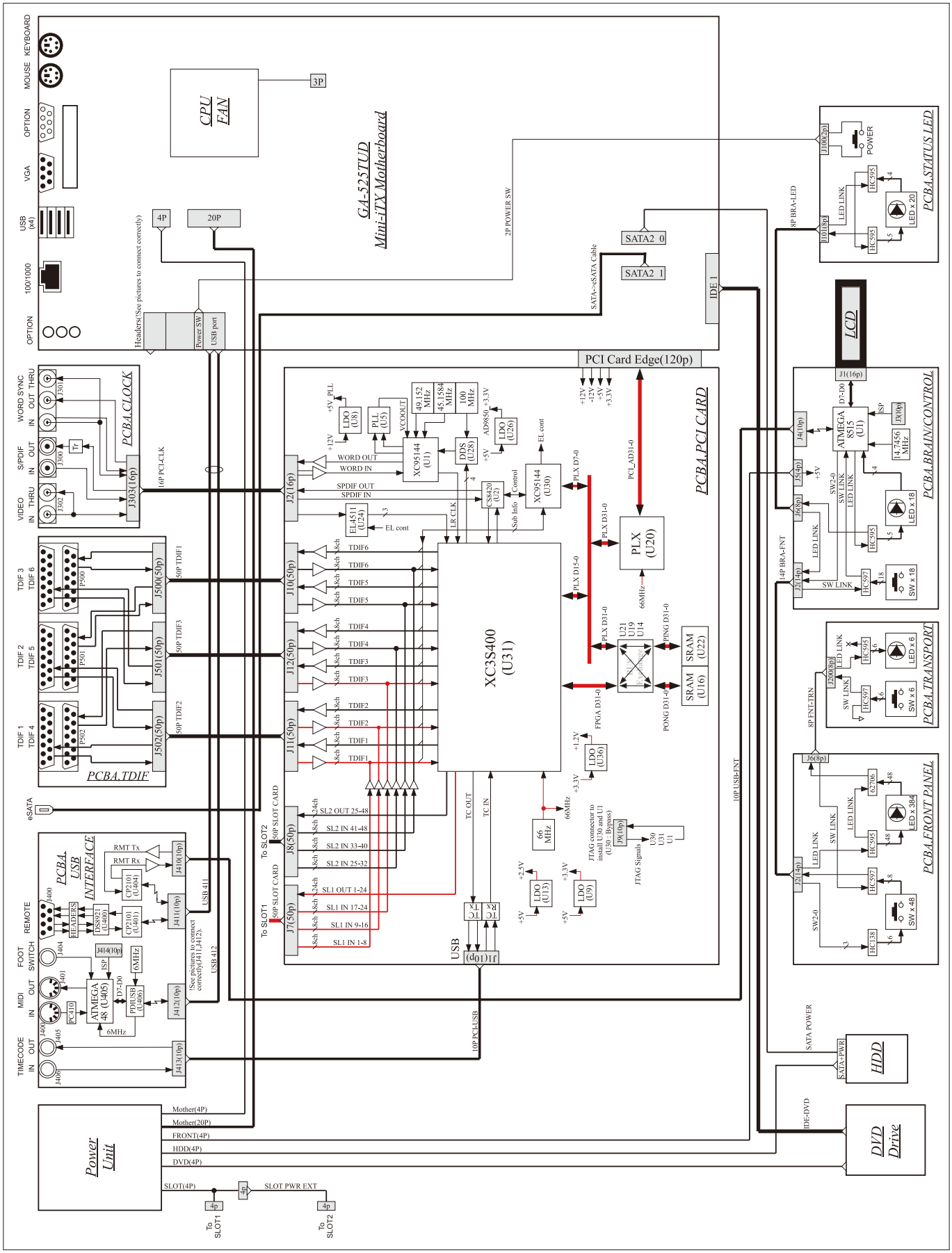
X-48MK II _hw_Step7



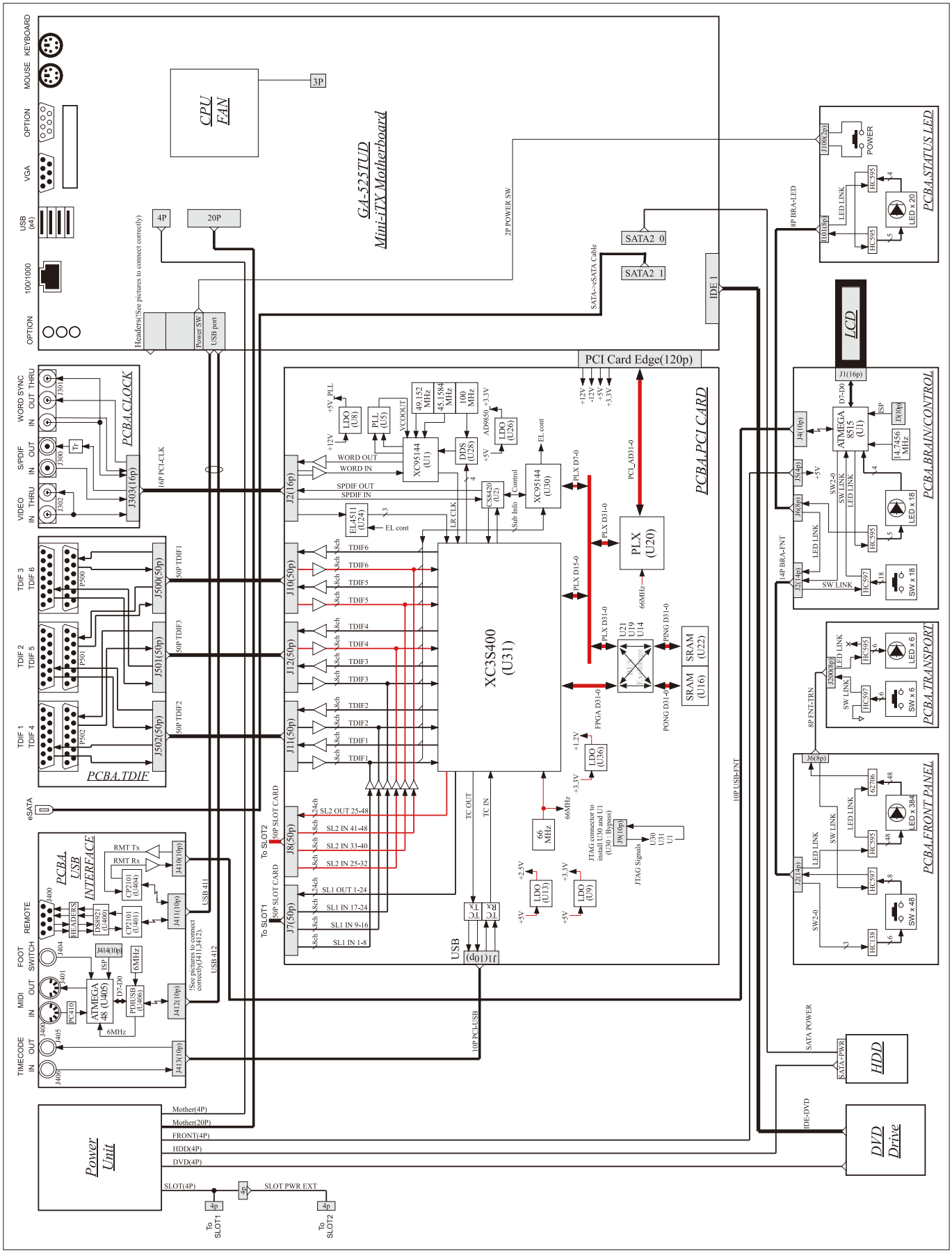
X-48MK II _hw_Step8-13



X-48MK II _hw_Step14-16



X-48MK II _hw_Step17-19



4. Installation
インストール

Programming the X-48MK II PCI Card

Gather Tools :

The first step in programming the devices used in the X-48MK II is to acquire all the tools necessary.

Programming Methods :

A dedicated test PC can be used to power the PCI card and run the software to program it. An open PCI slot and DB25 parallel port is required.

X-48MK II PCI カードのプログラミング

ツールの準備 :

X-48MK II で使用されているデバイスをプログラミングする最初の手順として、必要なツールをすべて準備します。

プログラミングの方法 :

試験用PC でPCI カードに電源を送り、ソフトウェアを使用してプログラミングします。空いているPCI スロット1基とDB25パラレル端子が必要です。

Xilinx Tools :

Parallel Cable IV Description

The new Xilinx Parallel Cable IV (PC4) (Figure 1) is a high-speed download cable that configures or programs all Xilinx FPGA, CPLD, ISP PROM, and System ACE MPM devices. The cable takes advantage of the IEEE 1284 ECP protocol and Xilinx iMPACT software to increase download speeds over eight times faster than existing solutions. The cable automatically senses and adapts to target I/O voltages and is able to accommodate a wide range of I/O standards from 1.5V to 5V. PC4 is designed for use in a desktop environment.

PC4 supports the widely used industry standard IEEE 1149.1 Boundary Scan (JTAG) specification using a four-wire interface. It also supports the Xilinx Slave Serial mode for Xilinx FPGA devices. It interfaces to target systems using a ribbon cable that features integral alternating ground leads to reduce crosstalk and improve signal integrity.

The cable is externally powered from either a power “brick” or by interfacing to a standard PC mouse or keyboard connection. A bi-color status LED indicates the presence of operating and target reference voltages.

Figure 1: **Xilinx Parallel Cable IV**

Programming Xilinx Chips (Step1) :

1. Place a jumper on **'J5'** between pins 2-3 to configure via Xilinx cable.
2. Plug the '**Xilinx Parallel Cable IV**' into the dedicated test PC's parallel port. Plug the mini-din into the mouse or keyboard port as well. Connect the IDC header of the **'parallel cable 4'** to **'J9'** labeled '**JTAG**' on the PCI card. The red stripe on the cable should line up with pin 1.
3. Plug the PCI card into an open slot in the dedicated test PC.
4. Power on the PC.

   Note : The LED on the programmer should be green indicating **'ready to program'**.

   Note : If the card is plugged into a new or different slot for the first time, the '**Found New Hardware Wizard**' window will pop up. Select **'Programming_Tools / PLX_Monitor / PciSdk.inf'**. If the wizard requires a driver, select **'Programming_Tools / PLX_Monitor / Bin / PlxApi.dll'**.
5. Run iMPACT
   [Start menu -> Program -> Xilinx ISE 7.1i -> Accessary -> iMPACT]

   On a pop-up window, select **'Create new project'** if this is the first time. From the second time, select **'load most recent project'**.
6. The **'Operation Mode Selection'** window will pop up. Select **'Configure Devices'** and click **'Next'**.

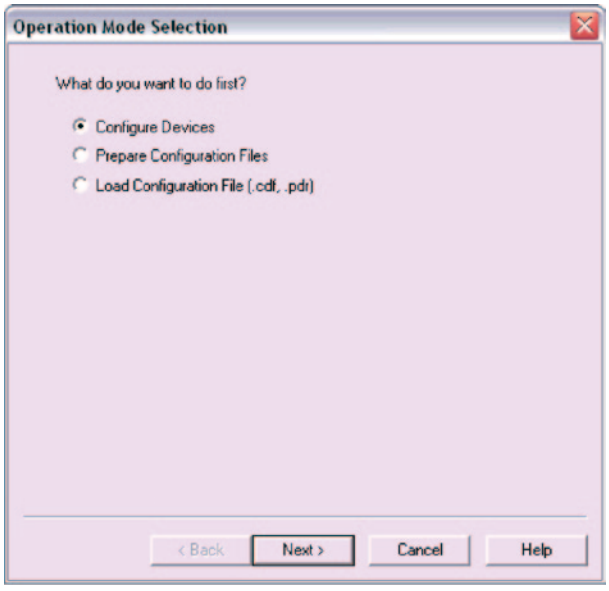
Xilinx チップのプログラミング（ステップ1）:

1. Xilinx ケーブル接続の設定として、**'J5'** のピン2 とピン3 にジャンパーを取り付けます。
2. 試験用PC のパラレル端子に'**Xilinx Parallel Cable IV**' を接続します。マウスまたはキーボードにもミニDIN を差し込みます。**"パラレルケーブル4"**のIDC ヘッダを、PCI カードの**'JTAG'** ラベルのついた**'J9'** に接続します。ケーブルの赤い線がピン1 側にくるようにします。
3. カードを試験用PC の空いたスロットに差し込みます。
4. PC の電源を入れます。

   注 : プログラマのインジケータが、**"プログラムできる状態"**を示す緑に点灯していることを確認してください。

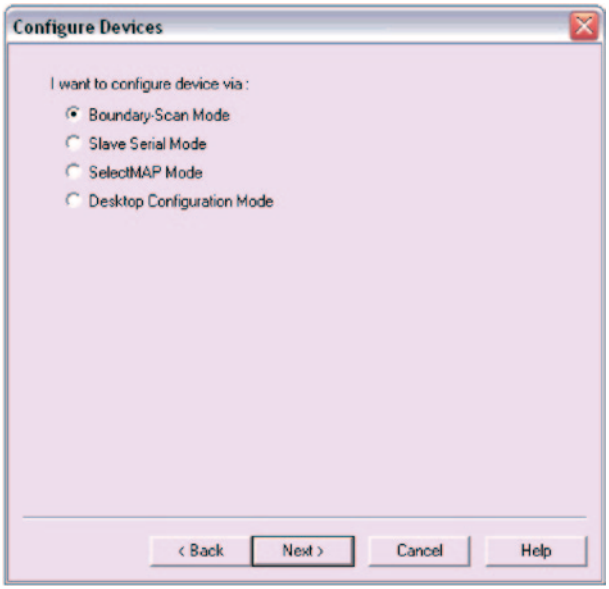
   注 : カードを新しいスロットまたは別のスロットに今回初めて接続した場合は、**Found New Hardware** ウイザード画面が表示されるので、**'Programming_Tools / PLX_Monitor / PciSdk.inf'**を選択します。ドライバが必要な場合は**'Programming_Tools / PLX_Monitor / Bin / PlxApi.dll'**を選択します。
5. IMPACT を起動します。
   [スタートメニュー -> プログラム -> Xilinx ISE 7.1i -> アクセサリ -> iMPACT]

   今回が初めての場合は、ポップアップウインドウから**'Create new project'**を選択します。次回からは**'load most recent project'**を選択します。
6. **'Operation Mode Selection'** 画面が表示されます。**'Configure Devices'**を選択し、**'Next'**をクリックします。



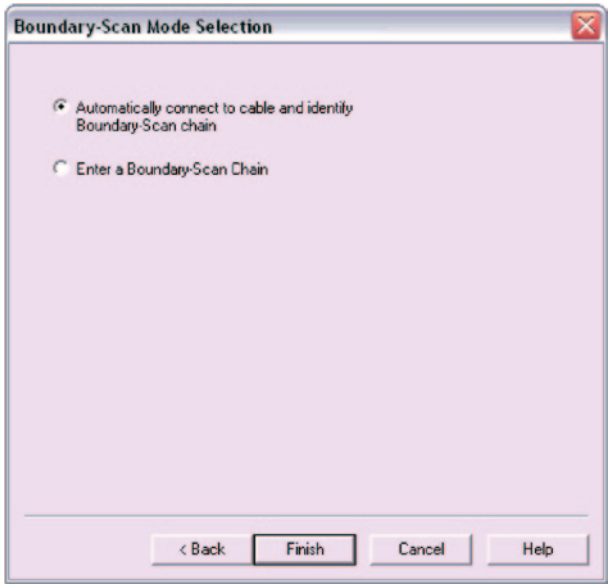
7. The **'Configure Devices'** window will pop up.
Select **'Boundary-Scan Mode'** and click **'Next'**.

7. **'Configure Devices'** 画面が表示されます。
'Boundary-Scan Mode' を選択し、**'Next'** をクリックします。



8. The **'Boundary-Scan Mode Selection'** window will pop up.
Select **'Automatically connect to cable and identify Boundary-Scan chain'** and click **'Finish'**.

8. **'Boundary-Scan Mode Selection'** 画面が表示されます。
'Automatically connect to cable and identify Boundary-Scan chain' を選択し、**'Finish'** をクリックします。



9. Click **'OK'** after the **Boundary-Scan mode** detects a device.

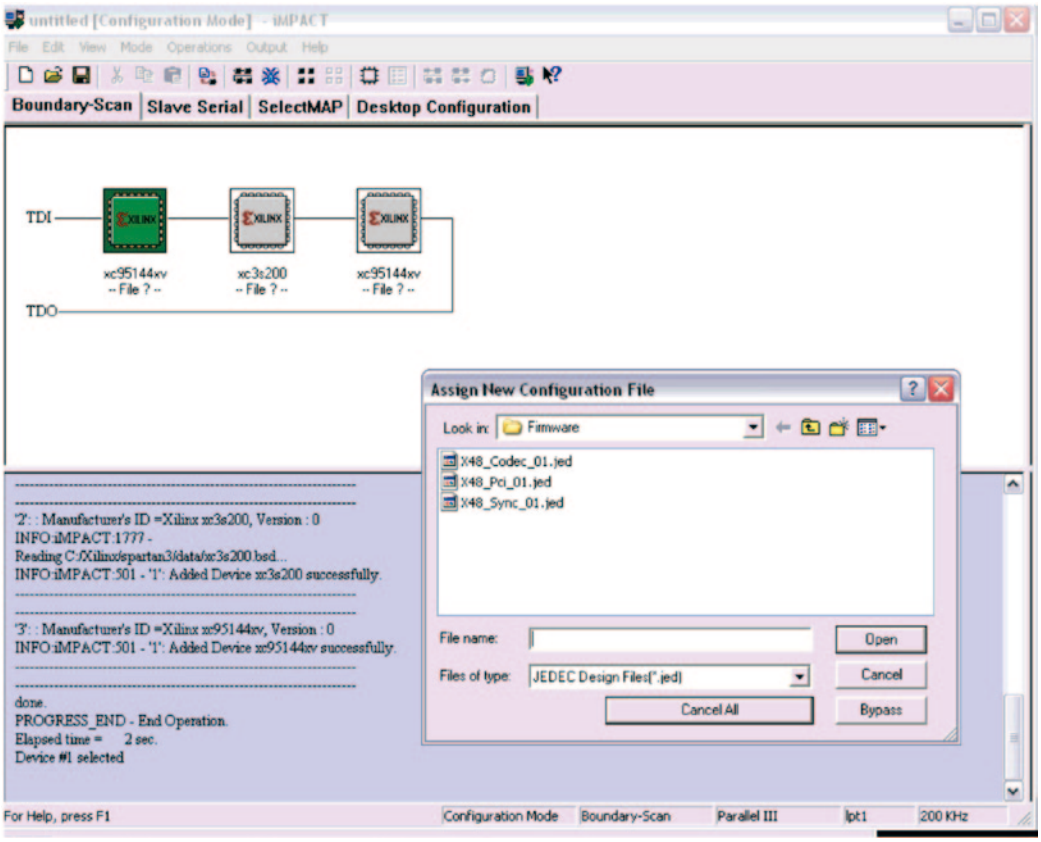
9. **Boundary-Scan モード**でデバイスが検知されたら、**'OK'**をクリックします。

10. Window will pop up called **'Assign New Configuration File'**.

Note : If this window does not pop up, right click on the device and select **'Assign New Configuration File'**.

10. **'Assign New Configuration File'** 画面が表示されます。

注 : この画面が表示されない場合は、デバイスを右クリックして **'Assign New Configuration File'** を選択してください。



11. Browse to the proper file and click **'Open'** (listed in table 1 below).

Ref	Device	JTAG order	File Name
U30	XC95144XV-7TQ144C	1st in JTAG chain	X-48MK II _PCI_ CPLD_A_REV_09.jed
U31	XC3S400-4FT256C	2nd in JTAG chain	(not programmed. Select'**Bypass**')
U1	XC95144XV-7TQ100C	3rd in JTAG chain	X-48MK II _PCI_ CPLD_B_REV_82.jed

Table 1 : Xilinx programming information

12. The **'Assign New Configuration File'** will automatically open for the next device in the chain.

Once all devices have the appropriate file assigned, right click on the first device (U30) and select **'Program...'**.

11. 適切なファイル（以下の表1 参照）を選択し、**'Open'** をクリックします。

部番	デバイス	JTAGの順序	ファイル名
U30	XC95144XV-7TQ144C	JTAG チェーンの1 番目	X-48MK II _PCI_ CPLD_A_REV_09.jed
U31	XC3S400-4FT256C	JTAG チェーンの2 番目	(プログラミングなし。**'Bypass'**を選択)
U1	XC95144XV-7TQ100C	JTAG チェーンの3 番目	X-48MK II _PCI_ CPLD_B_REV_82.jed

Table 1: Xilinx プログラミングデータ

12. チェーン内の次のデバイスに対する**'Assign New Configuration File'** 画面が自動表示されます。

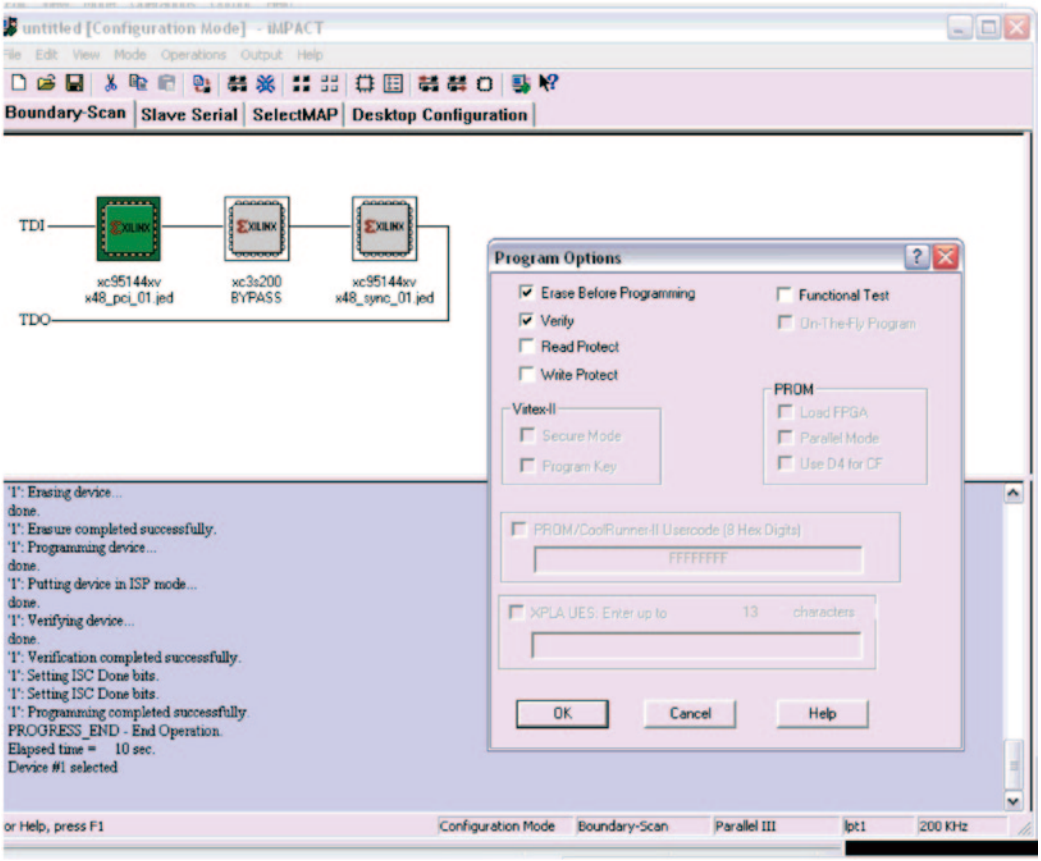
すべてのデバイスに適切なファイルを指定したら、最初のデバイス（U30）で右クリックし、**'Program...'** を選択します。

13. Make sure the following items are checked.
(Clear all the other check boxes.)

- Erase Before Programming
- Verify

13. 以下の項目にチェックが入っているか確認します。
（他の項目はすべて、チェックを外します。）

- Erase Before Programming
- Verify



14. Click **'OK'** to start programming.
Verify that programming succeeded.
Repeat programming for U1.
Close iMPACT (The end of Step1)'.

14. **'OK'** をクリックしてプログラミングを開始します。
プログラミングが問題なく完了したかを確認してください。
U1 についてもプログラミング手順をくり返します。
IMPACT を終了します。(ステップ1 終了)。

Programming PLX Chip (Step2) :

1. Run **'Programming_Tools / PLX_Monitor / Bin / PlxMon.exe'**.
2. If the program prompts that there is **'no 9056 device listing'**, do the following.
   - Click **'OK'**
   - The **'Properties'** window will open
   - Click **'Cancel'**
3. Go to the **'Command -> Serial Eeprom'**.
   The **'9056 EEPROM Values'** window will pop up.
4. Click **'Load File'** and browse to the **'Step1_2 / Step2 / X-48MK II _PCI_Rev4.eep'**.
5. Click the **'Write'** button.
6. Click the **'Refresh'** button and verify that the loaded data did not changed.
7. Click the **'Close'** button.

Verifying the PCI Card:

1. After programming is complete, go to **'Command -> Reset Device'.**
2. Go to **'Command -> Memory'**.
3. Click **'Memory Fill'**.
4. Check **'Fill with random values'**.
5. Type **'FFFF'** into the **'Fill size (in bytes) field'**.
6. Click **'Fill Memory'**.
7. Click **'Read Memory'**.
8. Verify that there are random values in the memory locations listed.
9. Close programs and shut down the dedicated test computer.
10. Remove the PCI card from the computer.
11. Disconnect the IDC header of the parallel cable 4 from **'J9',** and remove the jumper from **'J5'**.

Installation of the PCI card is complete. (The end of Step2).
This PCI card can be assembled into PCI slot in X-48MK II .

PLX チップのプログラミング（ステップ2）:

1. **'Programming_Tools / PLX_Monitor / Bin / PlxMon.exe'**を実行します。
2. **'9056 デバイスリストがない'**というメッセージが表示されたら、以下の手順に従ってください。
   - **'OK'** をクリックします。
   - **'Properties'** 画面が開きます。
   - **'Cancel'** をクリックします。
3. **'Command -> Serial Eeprom'** を選択します。
   '9056 EEPROM Values' 画面が開きます。
4. **'Load File'** をクリックし、**'Step1_2 / Step2 / X-48MK II _PCI_Rev4.eep'** を選択します。
5. **'Write'** ボタンをクリックします。
6. **'Refresh'** ボタンをクリックし、ロードされたデータが変わっていないことを確認します。
7. **'Close'** ボタンをクリックします。

PCI カードの検証：

1. プログラミング終了後、**'Command -> Reset Device'** を選択します。
2. **'Command -> Memory'** を選択します。
3. **'Memory Fill'** をクリックします。
4. **'Fill with random values'** をチェックします。
5. **'Fill size（in bytes）'**フィールドに**'FFFF'**をタイプします。
6. **'Fill Memory'** をクリックします。
7. **'Read Memory'** をクリックします。
8. リストされているメモリロケーションにランダム値があることを確認します。
9. プログラムを終了し、試験用コンピュータの電源を切ります。
10. コンピュータからPIC カードを取り外します。
11. **'J9'** からパラレルケーブル4 のIDC ヘッダを外し、**'J5'** からジャンパーを取り外します。

PCI カードのインストールが完了しました。（ステップ2 終了）
これで、X-48MK II のPCI スロットに、このPCI カードを取り付けることができます。

Programming X-48MK II Interface Card

The first step in programming the devices used in the X-48MK II is to acquire all the tools necessary.

Atmel Tools :

AVR ISP In-System Programmer

Description:

AVR In-System Programmer is used for field upgrades of existing products using the Atmel AVR® Architecture AVR In-System Programmer based on the STK500 Hardware and Software. Supports all In-System Programmable AVR devices.

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2726

X-48MK II インターフェースカードのプログラミング

X-48MK II で使用しているデバイスのプログラミングをするには、まず必要なツールをすべて揃えます。

Atmel ツール :

AVR ISP In-System Programmer

内容：

AVR In-System Programmer（ISP）は、Atmel AVR® シリーズのCPU が搭載されている製品において、そのCPU のプログラムを、CPU が実装されている状態で、現場でアップデートするために使用されます。すべてのIn-System プログラマブルAVR デバイスをサポートします。

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2726

AVR Studio® 4

Description:

AVR Studio® 4 is the new professional Integrated Development Environment (IDE) for writing and debugging AVR applications in Windows 95 / Windows 98 / Windows NT / Windows 2000 / Windows XP environments.

AVR Studio® 4 includes an assembler and a simulator. The following AVR development tools are also supported:

ICE50, ICE40, JTAGICE mkII, JTAGICE, ICE200, STK500 / 501 / 502 / 503 / 504 and AVRISP.

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2725

AVR Studio® 4

内容：

AVR Studio® 4は、Windows 95 / Windows 98 / Windows NT / Windows 2000 / Windows XP 用書き込み／デバッグAVRアプリケーションのための新しいプロ向けIDE (Integrated Development Environment)です。

AVR Studio® 4 にはアセンブラとシミュレータが含まれています。

以下のAVR 開発ツールもサポートされています。

ICE50、ICE40、JTAGICE mkII、JTAGICE、ICE200、STK500 / 501 / 502 / 503 / 504、AVRISP

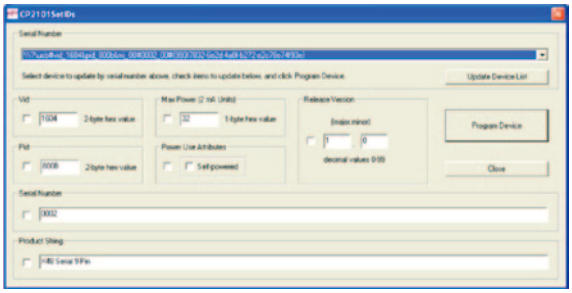
http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2725

CP2101 Tools :
CP2101 Set IDs
Description:

The CP2101 Set IDs program is a small window that can run on Windows NT / Windows 2000 / Windows XP and allows users to reprogram the USB VID and PID (as well as some other useful information) of a CP2101 USB serial port chip attached to the computer.

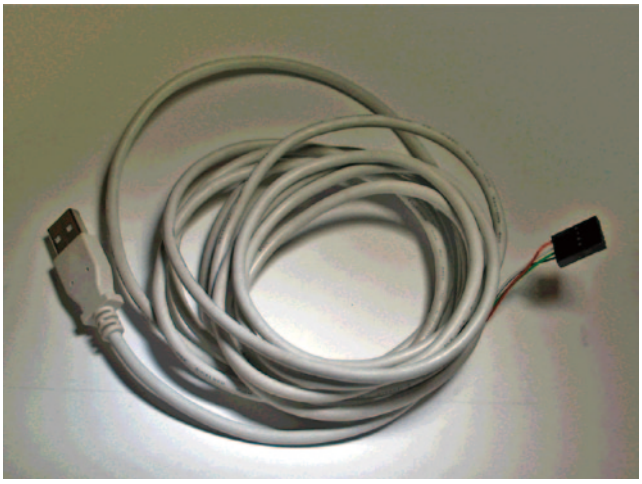
CP2101 ツール :
CP2101Set IDs
内容 :

CP2101 Set IDs プログラムは、Windows NT / Windows 2000 / Windows XP 用の実行可能な小ウインドウで、コンピュータに搭載されるCP2101USBシリアルポートのUSB VIDおよびPID（その他の便利な情報も含む）をユーザーが再プログラムできるようにするものです。
この実行可能なプログラムのコピーは本書に添付されています。



The CP2101 programming cable is provided by SaneWave.
This is a dedicated cable which SaneWave specially made. In most cases, TASCAM doesn't need to install CP2101. If needed, please contact to service section at TCJ.

CP2101 プログラミングケーブルはSaneWaveから入手したものです。
これはSaneWaveが特別に作製した専用ケーブルです。ほとんどの場合、TASCAMはCP2101をインストールする必要はありません。必要に応じて、TCJ のサービス部門にお問い合わせください。



Programming the Atmel Microprocessor (Step3) :

1. Plug the AVR ISP's DB9 cable into the dedicated test PC's COM port and plug the IDC header of the AVR ISP into the programming header for the Atmel, **'J414'**. The red stripe on the cable should line up with pin 1. The device and reference designator.

Programming Header	Atmel Device
J414	ATMega48

2. Plug the CP2101 programming cable to the right line in **'J412'** (See pic).
3. Plug the CP2101 programming cable into USB connector of the dedicated test PC.

Note : Do not do 'action **3.** ' before **1.** and **2.** to protect AVR ISP from electrical destruction.

Note : The LED on the AVR ISP should be green lighted indicating **'ready to program'** after just a few seconds.

Atmel マイクロプロセッサのプログラミング（ステップ3）:

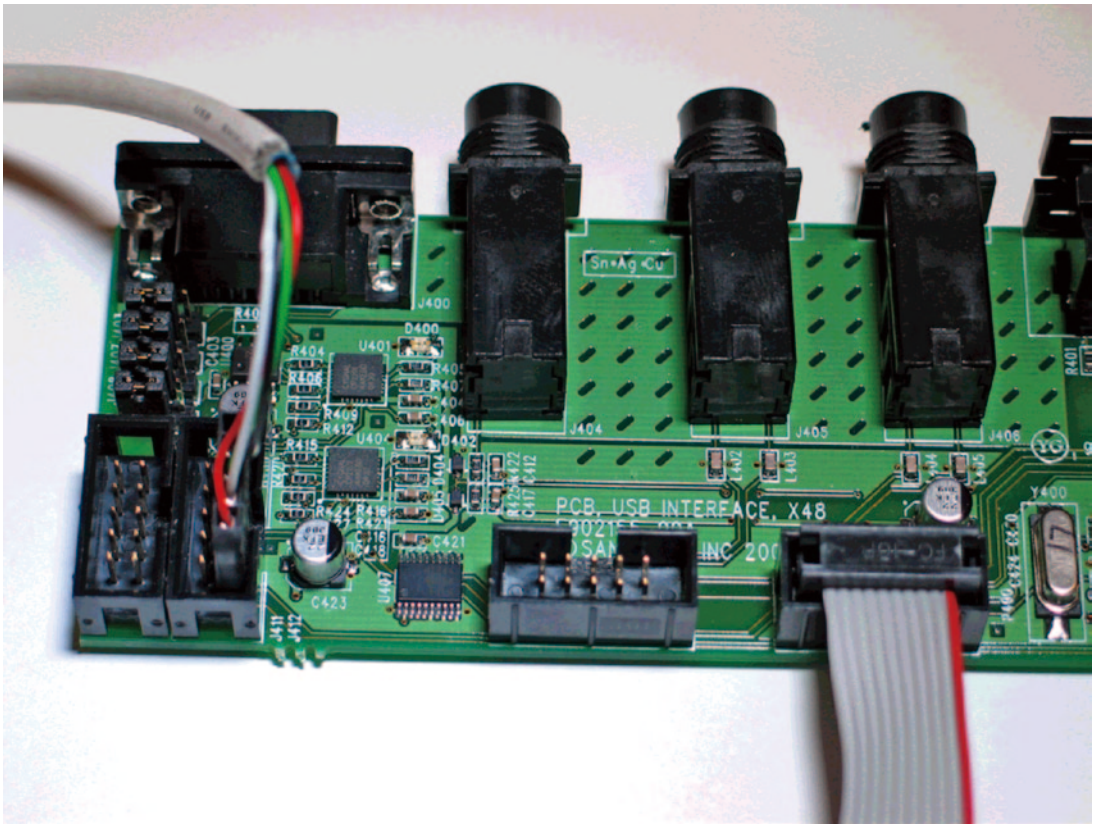
1. AVR ISP のDB9 ケーブルを試験用PC のCOM ポートに接続し、AVR ISP のIDC ヘッダをAtmel 用プログラミングヘッダ**'J414'**に接続します。ケーブルの赤い線がピン1側になるようにしてください。デバイスおよびプログラミングヘッダの参照番号は以下の表のとおりです。

プログラミングヘッダ	Atmel デバイス
J414	J414 ATMega48

2. CP2101 プログラミングケーブルを、**'J412'** の右のラインに接続します。（図参照）
3. CP2101 プログラミングケーブルを、専用の試験用PC のUSB 端子に接続します。

注 : AVR SIP が損傷しないよう、上記の手順**1.**や**2.**の前に手順**3.** を実施しないでください。

注 : 数秒後にAVR SIP のインジケータが、**"プログラムできる状態"**を示す緑に点灯していることを確認してください。



4. Run AVR Studio® 4.
[Start Menu -> Program -> Atmel AVR Tools -> AVR Studio 4]

If **'Welcome...'** window open, click **'cancel'** button on the window to close it.
Go to **'Tools -> Program AVR -> Auto Connect'**.

Note : If the firmware for the programmer is out of date you will be prompted to upgrade, press **'OK'** to upgrade.

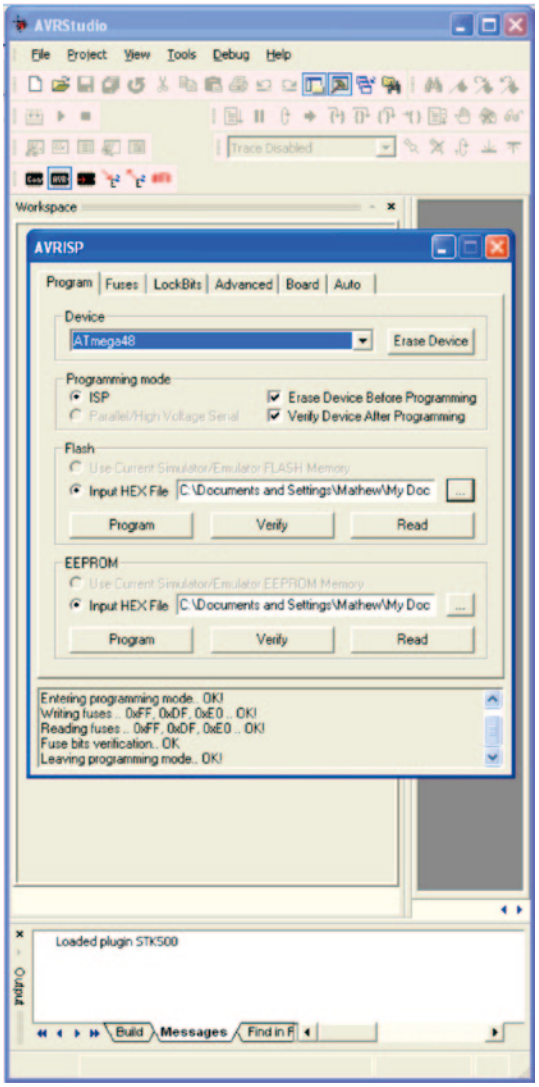
The **'AVRISP'** window will open.

4. AVR Studio® 4 を起動します。
[スタートメニュー -> プログラム -> Atmel AVR Tools -> AVR Studio 4]

"Welcome...（ようこそ）"の画面が表示されたら、**'cancel'** ボタンをクリックして画面を閉じます。
'Tools -> Program AVR -> Auto Connect'を選択します。

注 : プログラマのファームウエアが最新でない場合は、アップグレードするようメッセージが表示されるので、**'OK'**をクリックしてアップグレードしてください。

'AVRISP' 画面が開きます。



5. Go to the **'Program'** tab of the AVRISP window, and select **'ATmega48'** from pull-down menu of **'Device'** section.

6. Go to the **'Fuses'** tab and click **'Read'**.

Note : It should say **'OK'** after everything in the window below the buttons.

7. Set Fuse Bits for the ATMega48 by 'checking' following two items (all other items must be 'unchecked').

- Brown-out detection level at VCC=2.7 V
- Ext. Clock; Start-Up time PWRDWN / RESET : 6 CK/14 CK + 65 ms; [CKSEL = 0000 SUT = 10]

5. AVRISP 画面の**'Program'** タブをクリックし、**'Device'** セクションのプルダウンメニューから**'ATmega48'**を選択します。

6. **'Fuses'** タブを選択し、**'Read'**をクリックします。

注 : ボタンの下の領域の各行に**'OK'**が表示されます。

7. 以下の2 つの項目にチェックを入れてATMega48のFuse Bitsを設定します。（他の項目は必ずチェックを外してください。）

- Brown-out detection level at VCC = 2.7 V
- Ext. Clock; Start-Up time PWRDWN / RESET : 6 CK/14 CK + 65 ms; [CKSEL = 0000 SUT = 10]

8. Click the 'Program' button

Note : It should say **'OK'** after everything in the window below the buttons.

9. Go back to the **'Program'** tab of the AVRISP window.
In the Programming Mode section, verify that the following items are selected or checked :
- ISP
- Erase Device Before Programming
- Verify Device After Programming

10. In the Flash section, browse and select **'Step3_4 / Step3 / X48Interface_MP2_1.a90'** as a Input HEX File.

11. Click **'Program'** button in the flash section to program the ATMega48 (U405).
Make sure there was no error during the programming.

12. Close AVR Studio® 4.

13. Remove the CP2101 Programming cable from the dedicated test PC.

14. Remove the CP2101 Programming cable from **'J412'** on USB interface board.

15. After a few seconds from **14.**, remove the IDC header of the AVR ISP from **'J414**'. (The end of **Step3**).

8. 'Program' ボタンをクリックします。

注 : ボタンの下にある欄内の各行に**'OK'** が表示されます。

9. AVRISP 画面の**'Program'** タブを選択します。
Programming Mode セクションで、以下の項目が選択またはチ ェックされていることを確認します。
- ISP
- Erase Device Before Programming
- Verify Device After Programming

10. Flash セクションでInput HEXファイルとして以下を選択します。**'Step3_4/Step3 / X48Interface_MP2_1.a90'**

11. Flash セクションの**'Program**' ボタンをクリックしてATMega48 (U405)をプログラミングします。
プログラミング中にエラーが生じなかったことを確認します。

12. AVR Studio® 4 を終了します。

13. 専用の試験用PC からCP2101 プログラミングケーブルを外します。

14. USB インターフェースカードの**'J412'**からCP2101プログラミングケーブルを外します。

15. 上記手順**14.** を実施して数秒後に、**'J414'**からAVR ISPのIDC ヘッダを外します。（**ステップ3**の終了）

Programming the CP2101 Chips (Step4) :

Background knowledge :

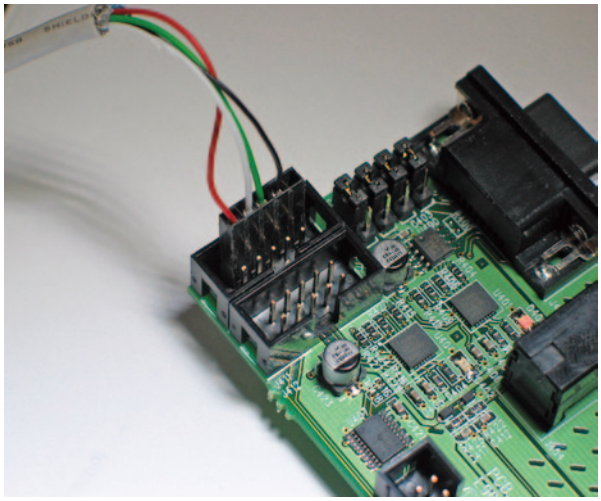
Before the CP2101 Chip is programmed, all CP2101s appear to the computer as identical USB devices because all CP2101 have same default 'product ID' inside of them. This makes the computer confused, if both chips are plugged in at the same time.

To avoid this problem, we must program each of the chips separately, one at a time.

Before you may program the CP2101, you must first install its default settings to your computer, and then after that, you can reprogram it to the correct settings for the X-48MK II , and then reinstall it.

Programming the first CP2101 - the Serial 9 Pin (U401) :

1. Unplug All cables from the board.
   Plug the USB CP2101 programming cable to outer line (pins 2,4,6,8 and 10) in **'J411'** as shown in the picture.



2. Plug the CP2101 programming cable into a USB port of the dedicated test PC.
3. After a few seconds, **Windows** should put up a **'Found New Hardware'** wizard.

   Note : This hardware wizard appears if the USB port of the dedicated test PC is connected to CP2101 for the first time. So **3.**-**8.** aren't necessary from the second time.
4. Click the radio button that says **'No Not This time'** and click the **'Nex'** Button.
5. Pick the **'Install From a specific Location'** option and click the **'Nex'** button.
6. Click the browse button and browse to **'Step3_4 / Step4 / CP2101 Default Install'.**
   Click 'Next'.
7. **Windows** will warn against installing a driver that is unsigned.
   Ignore this warning and continue.
8. Windows should inform you that your installation was complete, then it will pop up ANOTHER **'Found New Hardware'** window. Repeat steps **4.**-**7.** exactly as before.

CP2101 チップのプログラミング（ステップ4）:

手順開始前にお読みください :

CP2101チップをプログラミングする前は、すべてのCP2101が同一のUSBデバイスとしてコンピュータに認識されています。これは、どれもが同じデフォルトの「製品ID番号」を持っているからです。

二つのチップを同時に搭載すると、この状態ではコンピュータが混乱してしまいます。これを避けるには、個々のチップを別々にプログラミングすることが必要です。

手順としては、CP2101にX-48MK II 用のプログラムをインストール前に、PCが認識できる様にPCの初期設定を行い、その後にX-48MK II 用のプログラムのインストールを行います。

1つ目のCP2101のプログラミング - シリアル9ピン (U401) :

1. カードからすべての配線を外します。
   写真のように、**'J411'**のUSB CP2101プログラミングケーブルを外側のライン（ピン2、4、6、8、10）に接続します。

2. CP2101プログラミングケーブルを試験用PCのUSB 端子に接続します。
3. 数秒で、**Windows** の**'Found New Hardware'**ウイザードが表示されます。

   注 : 試験用PCのUSB 端子に初めてCP2101を接続した場合だけ、このウイザードが表示されるます。次回から、手順**3.** ～ **8.**は不要です。
4. **'No Not This time'** ラジオボタンをクリックし、**'Nex'** ボタンをクリックします。
5. **'Install From a specific Location'**を選択し、**'Nex'** ボタンをクリックします。
6. **"Browse'** ボタンをクリックして**'Step3_4 / Step4 / CP2101Default Install'**を選択し、**'Nex'** ボタンをクリックします。
7. 「署名のないドライバ(unsigned driver)をインストールしようとしている」という **Windows** の警告メッセージが表示されます。
   このメッセージを無視して続行します。
8. インストールが完了するとその旨メッセージが表示され、今度は別の**'Found New Hardware'** 画面が表示されるので、手順**4.** ～ **7.** をくり返します。

9. Now we must reprogram the CP2101 so that X-48MK II motherboard can recognize the CP2101.
Double-click **'Step3_4 / Step4 / CP2101 Set IDs / CP-2101SetIDs.exe'**.
Set all of the boxes with the data in the image below. Copy the data exactly. Make sure each box is checked, and be POSITIVE that **'Vid'** and **'Pid'** are correct.

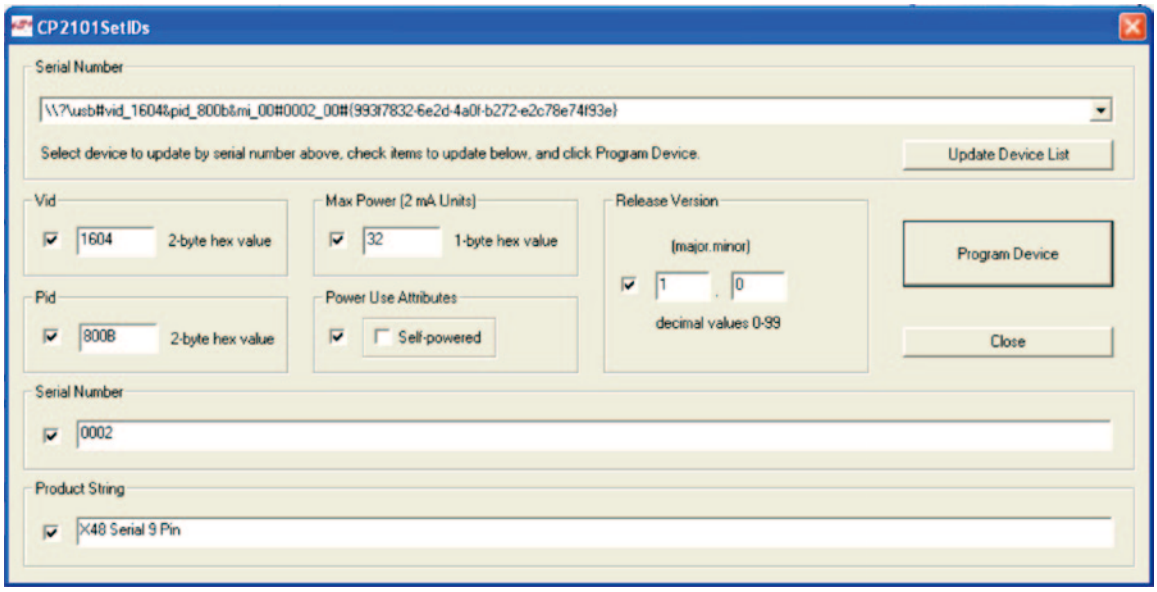
Note : Do not type the following parameters to avoid any typo. Do copy the following texts and paste them into the CP2101 window. If at least either of **'Vid'** or **'Pid'** is mistaken, the USB interface won't be able to be used forever.
(This bad method will be improved on next step.)

Vid = 1604
Pid = 800B
Max Power = 32
Release Version = 1.0
Serial Number = 0002
Product String = X48 Serial 9 Pin

9. X-48MK II のマザーボードがCP2101を認識するよう、CP2101を再プログラミングします。
'Step3_4 / Step4 / CP2101 Set IDs / CP2101SetIDs.exe' をダブルクリックします。
以下の画面に従って、すべてのフィールドに値を入力します。必ず同じように数値をコピー入力してください。各チェックボックスにチェックが入っていることを確認し、**'Vid'**と**'Pid'**を必ず正しく入力してください。

注： タイプミスがないよう、次のパラメータは値をコピー / ペーストしてください。**'Vid'**または**'Pid'**のいずれかにタイプミスがあると、USBインターフェースは永久に使用できなくなります。
（この手順は、次回改善予定です。）

Vid = 1604
Pid = 800B
Max Power = 32
Release Version = 1.0
Serial Number = 0002
Product String = X48 Serial 9 Pin



When all boxes are checked hit the **'Program Device'** button.

10. If the programming finish, unplug the CP2101 programming cable from the test PC.

11. Unplug the cable from the USB interface board and close the SetIDs program.

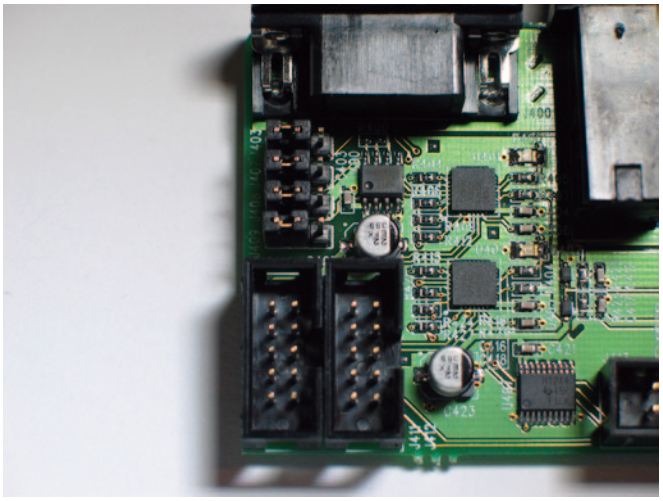
各ボックスをすべてチェックしたら、**'Program Device'** ボタンをクリックします。

10. プログラミグが終了したら、試験用PC からCP2101 プログラミングケーブルを外します。

11. USB インターフェースカードからケーブルを取り外し、Set IDs プログラムを終了します。

12. Place the four jumpers for the serial 9 pin as shown in the photo.

12. 以下の写真のように、シリアル9 ピンに4 つのジャンパーを取り付けます。



Done

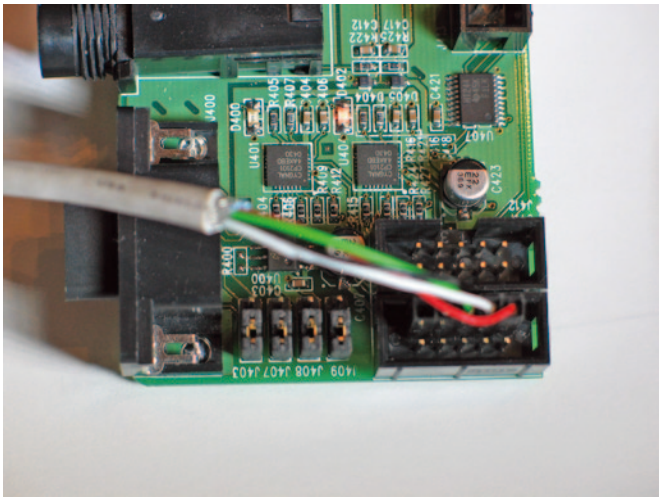
これで完了です。

Programming the second CP2101 - the Front Panel Serial Port (U404) :

2 つ目のCP2101 のプログラミング-フロントパネルのシリアルポート(U404) :

13. Plug in the CP2101 programming cable to inner line (pins 1, 3, 5, 7 and 9) in the **'J411'** as shown in the picture.

13. CP2101プログラミングケーブルを下の写真のように **'J411'**の内側のライン（ピン1/3/5/7/9）に接続します。



14. Plug in the CP2101 programming cable to the dedicated test PC.

15. This time, **Windows** will recognize the CP2101 device, since we have already installed the other CP2101 default. Now we must reprogram the CP2101.
Double-click **'Step3_4 / Step4 / CP2101 Set IDs / CP2101SetIDs. exe'**
Set all of the boxes with the data in the image below. Copy the data exactly. Make sure each box is checked, and be POSITIVE that **'Vid'** and **'Pid'** are correct.

Note : Do not type the following parameters to avoid any typo. Do copy the following texts and paste them into the CP2101 window. If at least either of **'Vid'** or **'Pid'** is mistaken, the USB interface won't be able to be used forever.
(This bad method will be improved on next step.)

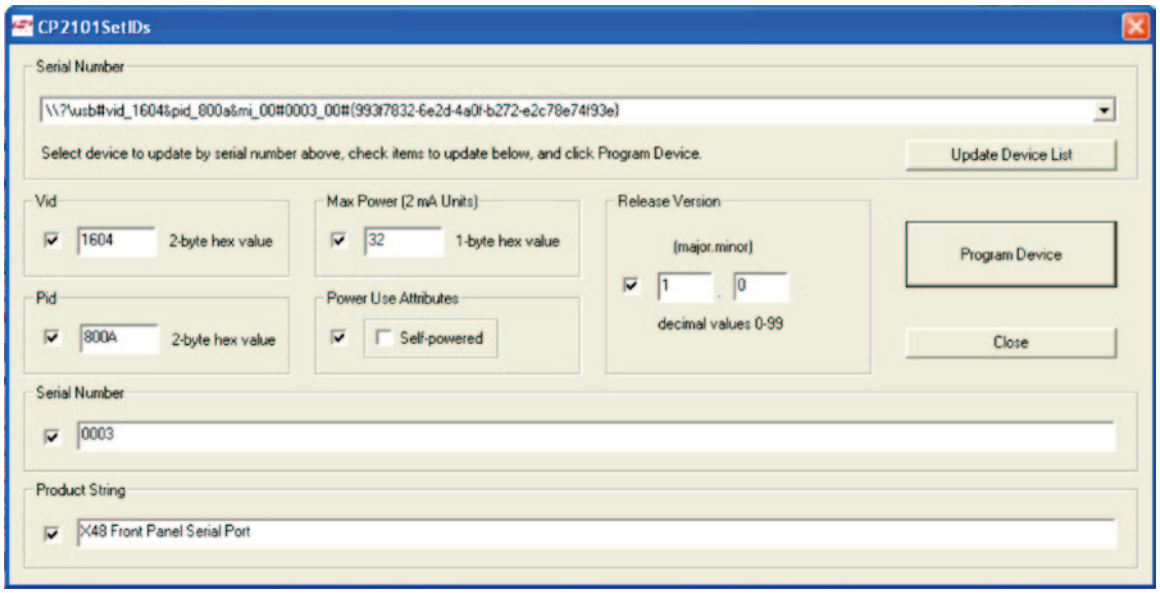
Vid = 1604
Pid = 800A
Max Power = 32
Release Version = 1.0
Serial Number = 0003
Product String = X48 Front Panel Serial Port

14. CP2101プログラミングケーブルを試験用PC に接続します。

15. すでに別のCP2101のデフォルトをインストールしてあるので、今度は **Windows** でCP2101デバイスが認識されます。このCP2101を再プログラミングすることが必要です。
'Step3_4 / Step4 / CP2101 Set IDs / CP2101SetIDs.exe' をダブルクリックします。
以下の画面にあるようにフィールドにデータを設定します。値を間違わないようにコピー入力してください。各チェックボックスにチェックが入っていることを確認し、**'Vid'**と**'Pid'**を必ず正しく入力してください。

注 : タイプミスがないよう、次のパラメータは値をコピー / ペーストしてください。**'Vid'**または**'Pid'**のいずれかにタイプミスがあると、USBインターフェースは永久に使用できなくなります。
（この手順は、次回改善予定です。）

Vid = 1604
Pid = 800A
Max Power = 32
Release Version = 1.0
Serial Number = 0003
Product String = X48 Front Panel Serial Port



When all boxes are checked hit the **'Program Device'** button.

16. If the programming finish, unplug the CP2101 programming cable from the test PC.

17. Unplug the cable from the USB interface board and close the Set IDs program.
Now the installation of the USB interface board is complete. (The end of **Step4**)
This USB interface board can be assembled into X-48MK II.

各ボックスをすべてチェックしたら、**'Program Device'** ボタンをクリックします。

16. プログラミグが終了したら、試験用PCからCP2101プログラミングケーブルを外します。

17. USB インターフェースカードからケーブルを取り外し、Set IDs プログラムを終了します。
USBインターフェースカードのインストールが完了しました。（**ステップ4**の終了）
これで、このUSBインターフェースカードをX-48MK II に取り付けることができます。

Programming X-48MK II Front Panel

The first step in programming the devices used in the X-48MK II is to acquire all the tools necessary.

Atmel Tools :

AVR ISP In-System Programmer

Description:

AVR In-System Programmer is used for field upgrades of existing products using the Atmel AVR® Architecture AVR In-System Programmer based on the STK500 Hardware and Software. Supports all In-System Programmable AVR devices.

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2726

X-48MK II フロントパネルのプログラミング

X-48MK II で使用しているデバイスのプログラミングをするには、まず必要なツールをすべて揃えます。

Atmel ツール :

AVR ISP In-System Programmer

内容：

AVR In-System Programmer（ISP）は、Atmel AVR® シリーズのCPU が搭載されている製品において、そのCPU のプログラムを、CPU が実装されている状態で、現場でアップデートするために使用されます。すべてのIn-System プログラマブルAVR デバイスをサポートします。

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2726

AVR Studio® 4

Description:

AVR Studio® 4 is the new professional Integrated Development Environment (IDE) for writing and debugging AVR applications in Windows 95 / Windows 98 / Windows NT / Windows 2000 / Windows XP environments.

AVR Studio® 4 includes an assembler and a simulator.

The following AVR development tools are also supported:

ICE50, ICE40, JTAGICE mkII, JTAGICE, ICE200, STK500 / 501 / 502 / 503 / 504 and AVRISP.

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2725

AVR Studio® 4

内容：

AVR Studio® 4は、Windows 95 / Windows 98 / Windows NT / Windows 2000 / Windows XP 用書き込み／デバッグAVRアプリケーションのための新しいプロ向けIDE (Integrated Development Environment)です。

AVR Studio® 4 にはアセンブラとシミュレータが含まれています。

以下のAVR 開発ツールもサポートされています。

ICE50、ICE40、JTAGICE mkII、JTAGICE、ICE200、STK500 / 501 / 502 / 503 / 504、AVRISP

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2725

Programming the Atmel Microprocessor (Step5) :

1. Plug the AVR ISP's DB9 cable into the dedicated test PC's COM port, and Plug the IDC header of the AVR ISP into the programming header for the Atmel, **'J3'**.
   (The header is on the back of the BRAIN board.)
   The red stripe on the cable should line up with pin 1.
   The device and reference designator for the programming header are listed in the following table.

Programming Header	Atmel Device
J3	ATMega8515

2. Make sure the dedicated ATX power unit for installation use is turned off, and plug a 4P connector of the ATX power unit to **'J5'** on the BRAIN board.
   Turn on the ATX power unit.

   Note : The LED on the programmer should be green lighted indicating **'ready to program'** after just a few seconds.

3. Run AVR Studio® 4.
   [Start Menu -> Program -> Atmel AVR Tools -> AVR Studio 4]

   If **'Welcome...'** window open, click **'cancel'** button on the window to close it.

   Go to **'Tools -> Program AVR -> Auto Connect'**

   Note : If the firmware for the programmer is out of date you will be prompted to upgrade, press **'OK'** to upgrade.

   The **'AVRISP'** window will open.

Atmelマイクロプロセッサのプログラミング（ステップ5）:

BRAIN ボードの電源がオフである事を確認して下さい。

1. AVR ISPのDB9ケーブルを試験用PCのCOMポートに接続し、AVR ISPのIDCヘッダをAtmel 用プログラミングヘッダ **'J3'**に接続します。
   (ヘッダはBRAINボードの背面にあります。)
   ケーブルの赤い線がピン1 側になるようにしてください。デバイスおよびプログラミングヘッダの参照番号は以下の表のとおりです。

プログラミングヘッダ	Atmel デバイス
J3	ATMega8515

2. インストール専用ATX電源ユニットを使っている場合は、専用の電源ユニットがオフになっていることを確認してから、ATX電源ユニットの4PコネクタをBRAINカードの**'J5'** に接続します。
   ATX 電源ユニットをオンにします。
   また、X-48MK II に組み込んだ状態でプログラミングする場合は、ここでX-48MK II の電源をオンにします。

   注 : 数秒後にプログラマのインジケータが、**"プログラムできる状態"**を示す緑に点灯していることを確認してください。

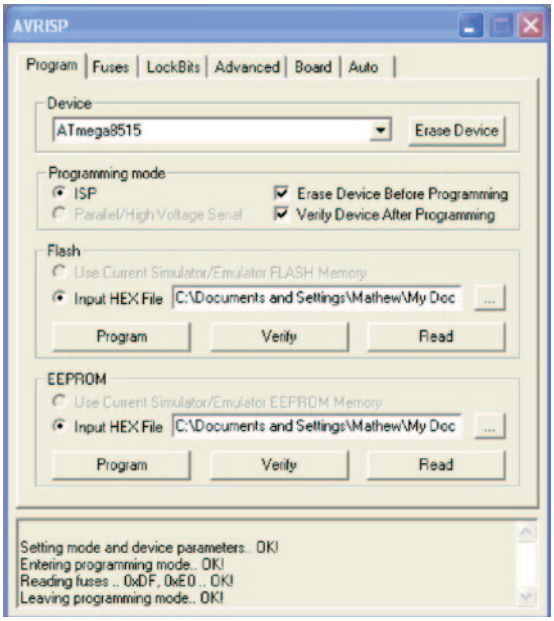
3. AVR Studio® 4を起動します。
   [スタートメニュー -> プログラム -> Atmel AVR Tools -> AVR Studio 4]

   "Welcome...（ようこそ）"の画面が表示されたら、**'cancel'** ボタンをクリックして画面を閉じます。

   'Tools -> Program AVR -> Auto Connect'を選択します。

   注 : プログラマのファームウエアが最新でない場合は、アップグレードするようメッセージが表示されるので、**'OK'**をクリックしてアップグレードしてください。

   'AVRISP'画面が開きます。



5. Go to the **'Program'** tab of the AVRISP window, and select **'ATmega8515**' from pull-down menu of **'Device'** section.

6. Go to the **'Fuses'** tab and click **'Read'**.
Note : It should say **'OK'** after everything in the window below the buttons.

7. Set **Fuse Bits** for the ATMega8515 by checking following three items. (All the other check boxes must be cleared).
- Boot Flash Section Size = 1024 words
- Brown-out detection level at VCC = 2.7 V
- Ext. Crystal / Resonator High Freq; Start-up time: 16K Ck + 64 ms; [CKSEL=1111 SUT=11]
(this is the very bottom choice)

8. Click the **'Program**' button.

Note : It should say **'OK'** after everything in the window below the buttons.

9. Go back to the **'Program'** tab of the AVRISP window
In the Programming Mode section, verify that the following items are selected / checked:
- ISP
- Erase Device Before Programming
- Verify Device After Programming

10. In the Flash section, browse and select **'Step5 / X48_ front_panel_MP2_1.a90'** as a Input HEX File.

11. Click **'Program'** Button in the flash section to program the **ATmega8515(U1)**.
Make sure there was no error during the programming.

12. Close AVR Studio® 4 .

13. Turn off the ATX power unit.

14. After a five seconds from **13.**, remove the IDC header of the AVR ISP from **'J3'**. (The end of **Step3**)
Now the installation of the BRAIN board is complete. (The end of **Step5**)
This BRAIN board can be assembled into X-48MK II .

5. AVRISP 画面の**'Program'** タブをクリックし、**'Device'** セクションのプルダウンメニューから**'ATmega8515'**を選択します。

6. **'Fuses'**タブを選択し、**'Read'**をクリックします。
注 : ボタンの下にある欄内の各行に**'OK'**が表示されます。

7. 以下の3 つの項目にチェックを入れて**ATMega8515**の**Fuse Bits**を設定します。（他の項目は必ずチェックを外してください。）
- Boot Flash Section Size = 1024 words
- Brown-out detection level at VCC = 2.7V
- Ext. Crystal / Resonator High Freq; Start-up time : 16K Ck + 64 ms; [CKSEL=1111 SUT=11]
(this is the very bottom choice)

8. **'Program'** ボタンをクリックします。
注 : ボタンの下にある欄内の各行に**'OK'**が表示されます。

9. AVRISP 画面の**'Program'** タブに戻ります。
Programming Mode セクションで、以下の項目が選択 / チェックされていることを確認します。
- ISP
- Erase Device Before Programming
- Verify Device After Programming

10. Flash セクションでInput HEXファイルとして以下を選択します。**'Step5 / X48_front_panel_MP2_1.a90'**

11. Flash セクションの**'Program'** ボタンをクリックして**ATmega8515(U1**)をプログラミングします。
プログラミング中にエラーが生じなかったことを確認します。

12. AVR Studio® 4 を終了します。

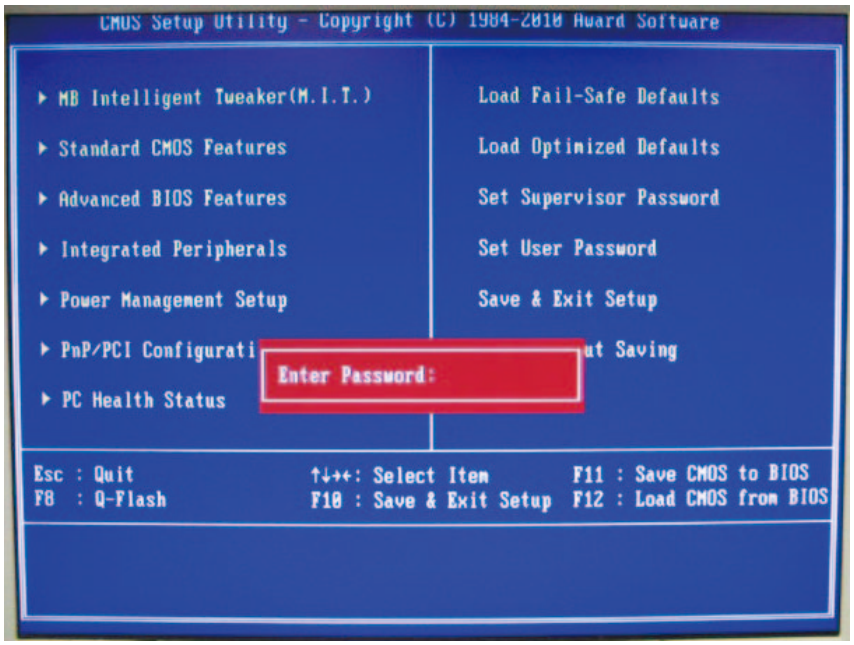
13. ATX 電源ユニットまたはX-48MK II の電源をオフにします。

14. 上記の手順**13.**を実施して5秒後に、**'J3'** からAVR ISP の IDC ヘッダを外します。（**ステップ3**の終了）
BRAIN ボードのインストールが完了しました。
（**ステップ5**の終了）
これでBRAIN ボードをX-48MK II に使用することができます。

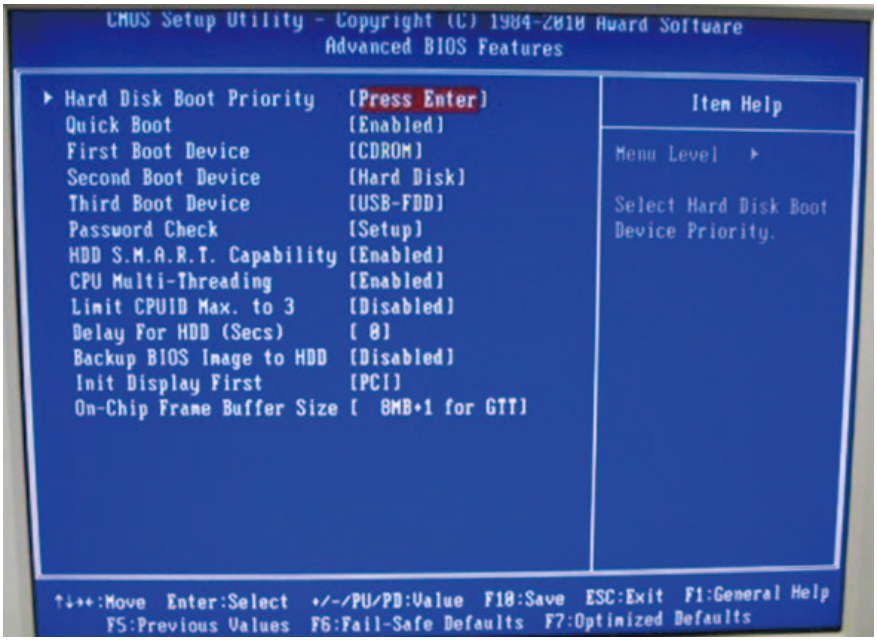
Embedded XP Installation for MP

Installation

1. While pressing and holding **'DEL'** key on the keyboard, turn on X-48MK II . The BIOS setup screen appears.
2. The message **'Enter Password'** appears on the **CMOS Setup Utility** screen. Type **'mitaka'**, and then press **'Enter'** key.



3. Select **'Advanced BIOS Features'** menu in the **CMOS Setup Utility** screen, and then set parameters as shown below.



Return to the **CMOS Setup Utility** screen by pressing **'ESC'** key on the keyboard.

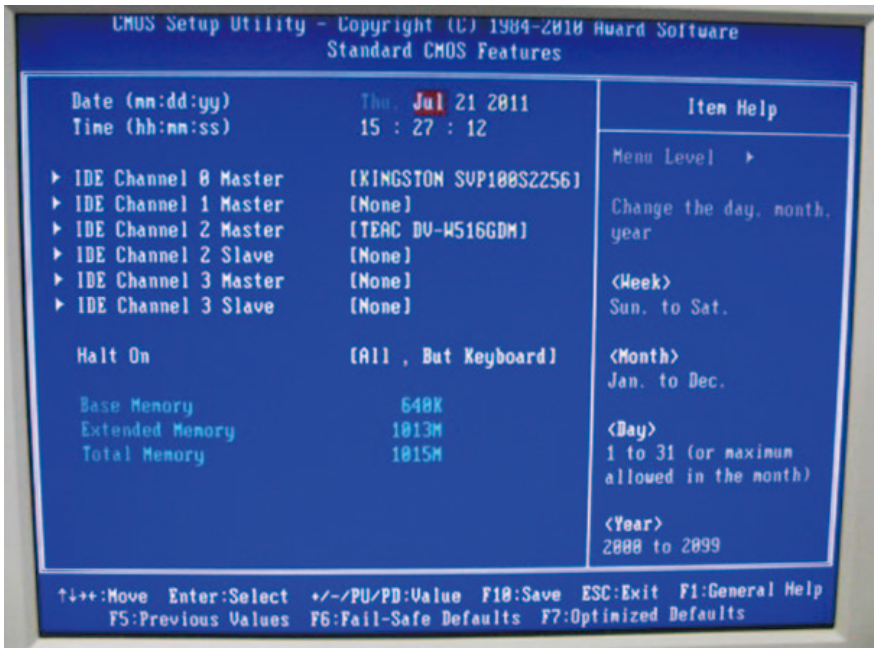
MP 用Embedded XP のインストール

インストール

1. キーボード上の**'DEL'** キーを長押ししながら、X-48MK II の電源を入れます。
2. **CMOS Setup Utility** 画面に**'Enter Password'**と表示されますので、**'mitaka'**と入力し、**'Enter'** キーを押します。
3. **CMOS Setup Utility** 画面から**'Advanced BIOS Features'** メニューを選択し、以下のようにパラメータを設定します。

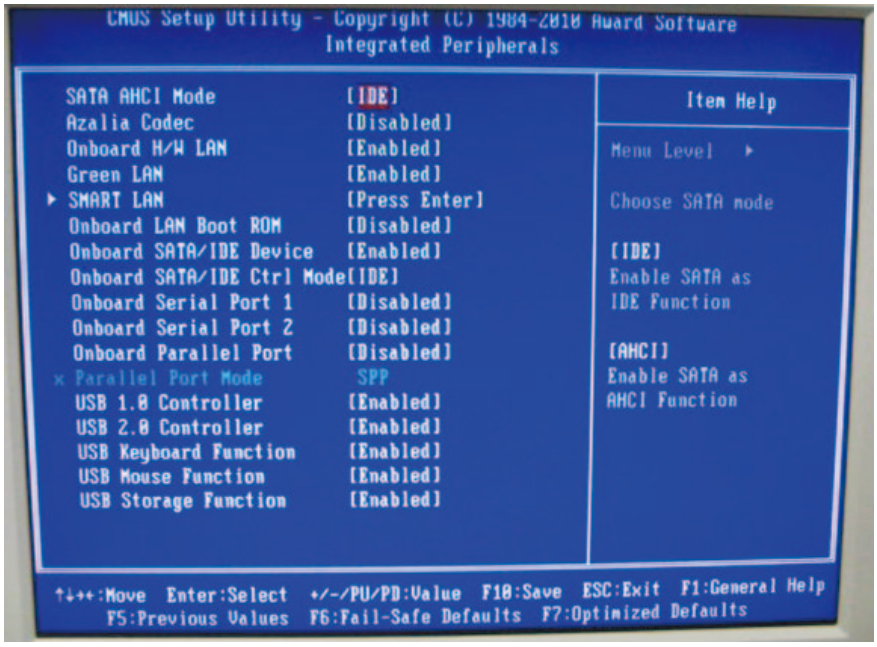
キーボードの**'ESC'** キーを押して**CMOS Setup Utility** 画面に戻ります。

4. Select **'Standard CMOS Features'** menu, and then set parameters as shown below.
   Make sure **'Extended Memory'** is **'1013M'**.



Return to the **CMOS Setup Utility** screen by pressing **'ESC'** key on the keyboard.

5. Select **'Integrated Peripherals'** menu, and then set parameters as shown below.



Return to the **CMOS Setup Utility** screen by pressing **'ESC'** key on the keyboard.

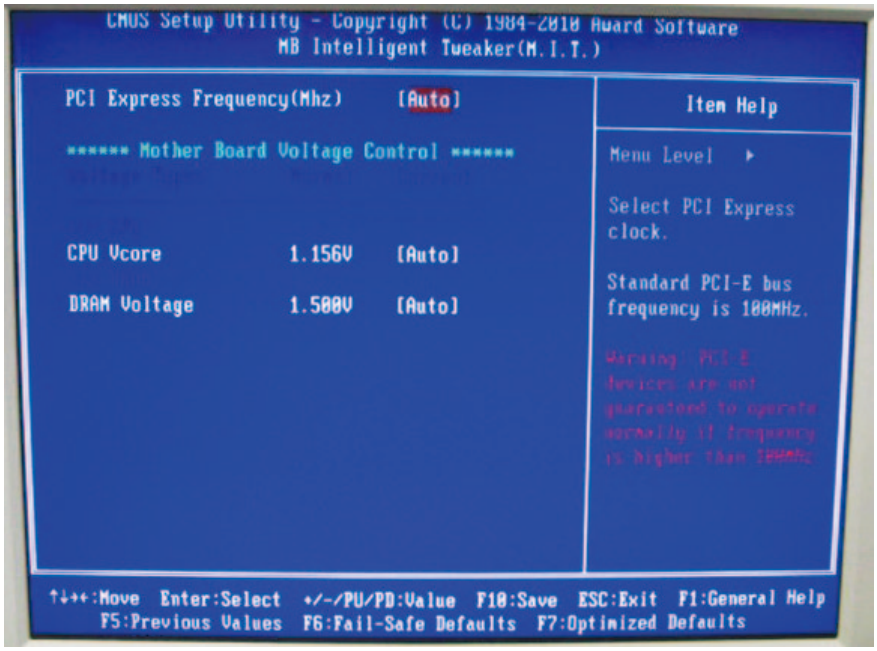
4. **'Standard CMOS Features'**メニューを選択し、以下のようにパラメータを設定します。
   'Extended Memory'が**'1013M'**であることを確認します。

キーボードの**'ESC'** キーを押して**CMOS Setup Utility** 画面に戻ります。

5. **'Integrated Peripherals'** メニューを選択し、以下のようにパラメータを設定します。

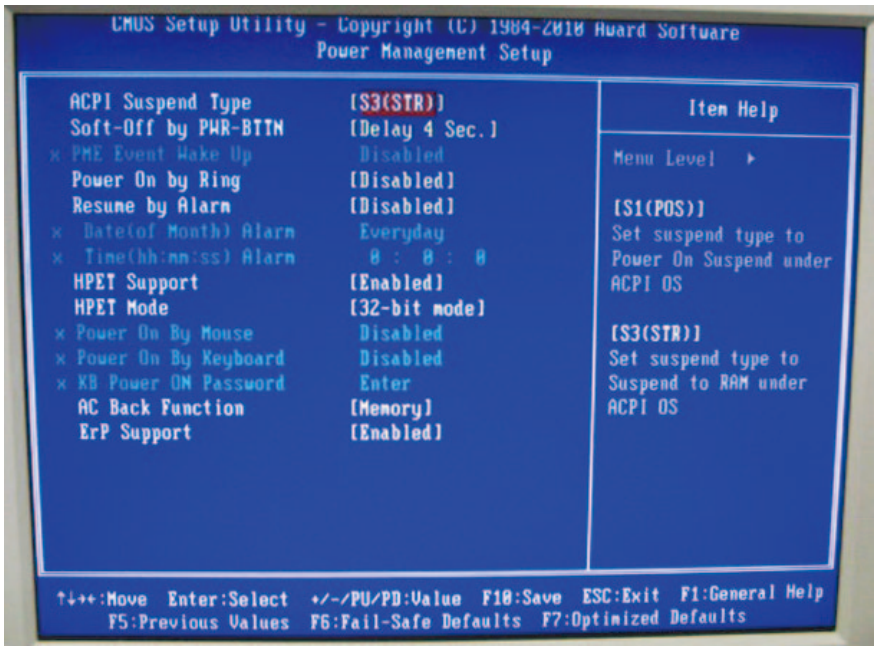
キーボードの**'ESC'** キーを押して**CMOS Setup Utility** 画面に戻ります。

6. Select **'MB Intelligent Tweaker (M.I.T.)'** menu, and then set parameter as shown below.



Return to the **CMOS Setup Utility** screen by pressing **'ESC'** key on the keyboard.

7. Select **'Power Management Setup'** menu, and then set parameters as shown below.



Return to the **CMOS Setup Utility** screen by pressing **'ESC'** key on the keyboard.

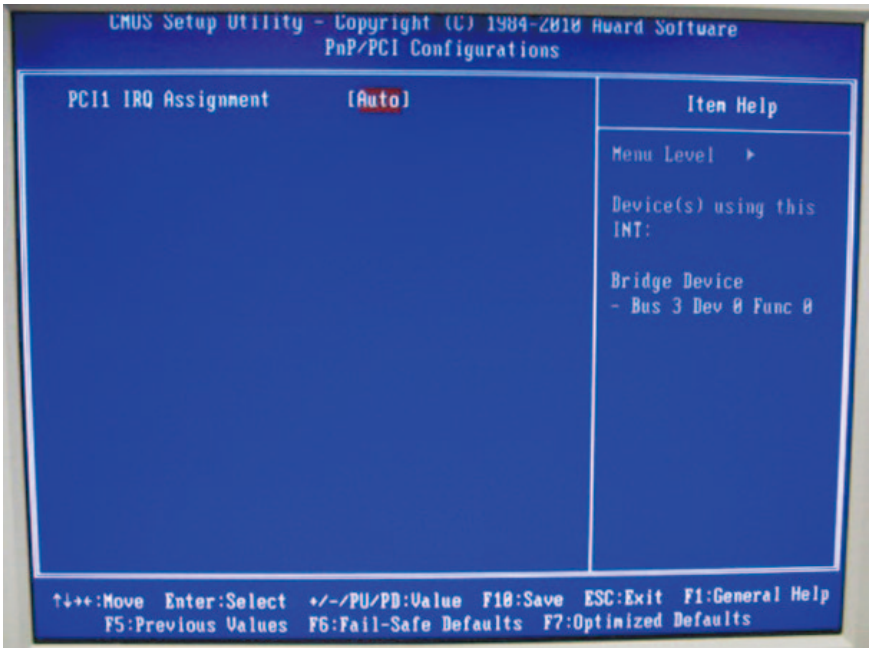
6. **'MB Intelligent Tweaker (M.I.T.)'** メニューを選択し、以下のようにパラメータを設定します。

キーボードの**'ESC'** キーを押して**CMOS Setup Utility** 画面に戻ります。

7. **'Power Management Setup'**メニューを選択し、以下のようにパラメータを設定します。

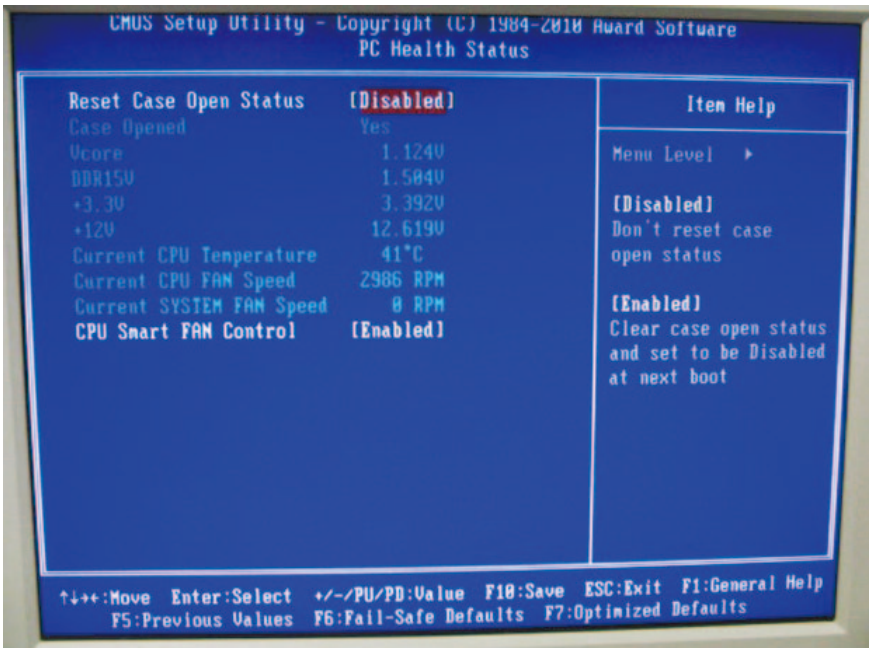
キーボードの**'ESC'** キーを押して**CMOS Setup Utility** 画面に戻ります。

8. Select **'PnP/PCI Configurations'** menu, and then set parameters as shown below.



Return to the **CMOS Setup Utility** screen by pressing **'ESC'** key on the keyboard.

9. Select **'PC Health Status'** menu, and then set parameters as shown below.



Return to the **CMOS Setup Utility** screen by pressing **'ESC'** key on the keyboard.

10. Insert the **'X-48MK II Restore CD'** CD-ROM into the built-in DVD drive.

11. Return to the **CMOS Setup Utility** screen by pressing **'ESC'** key, and then press **'F10'** key to save changes and exit the screen. Now you can boot X-48MK II from the CD-ROM by pressing any key while the following message is displayed.

"Press any key for CD-ROM boot".

8. **'PnP/PCI Configurations'** メニューを選択し、以下のようにパラメータを設定します。

キーボードの**'ESC'** キーを押して**CMOS Setup Utility** 画面に戻ります。

9. **'PC Health Status'**メニューを選択し、以下のようにパラメータを設定します。

キーボードの**'ESC'** キーを押して**CMOS Setup Utility** 画面に戻ります。

10. **'X-48MK II Restore CD'** CD-ROMを内蔵DVD ドライブに挿入します。

11. **CMOS Setup Utility** 画面からキーボードの**'F10'** キーを押し、設定した内容を保存して終了します。
これで、以下のメッセージが画面表示されている間に任意のキーを押すと、CD-ROMからX-48MK II を立ち上げることができます。

"Press any key for CD-ROM boot".

12. Once the OS Installer is fully booted, you will see the '**X48 OS Installer'** window on the display.

13. Choose **'No, rebuild the data drive as well as the X48 OS drive'**, and then click **'Install'** button.

14. Wait for several minutes until the installation process is completed.

15. After the installation is completed, press **'Restart X48'** button.

16. When the restart started, press **'DEL'** key to enter the BIOS setup screen again.

17. After the BIOS screen appears, take out the CD-ROM from the DVD drive.

18. Press **'ESC'** key. Then, press **'Y'**, and then **'Enter'** key to exit without saving.
Then, X-48MK II boots from the hard disk and a track screen of X-48MK II recorder is shown on the display.

19. After the restart process has finished, the OS displays a restart popup window to recognize new hardware and new software. Press **'OK'**. Then, X-48MK II starts restarting again.

The entire installation process is completed.

12. OSインストーラが完全に立ち上がると、**'X48 OS Installer'** 画面が表示されます。

13. **'No, rebuild the data drive as well as the X48 OS drive'** を選択し、**'Install'** ボタンをクリックします。

14. インストールが完了するまで数分お待ちください。

15. インストール後、**'Restart X48'**ボタンを押します。

16. 再起動が始まったら、**'DEL'** キーを押してBIOS 設定画面をもう一度表示させます。

17. BIOS 画面が表示されたら、DVDドライブからCD-ROMを取り出します。

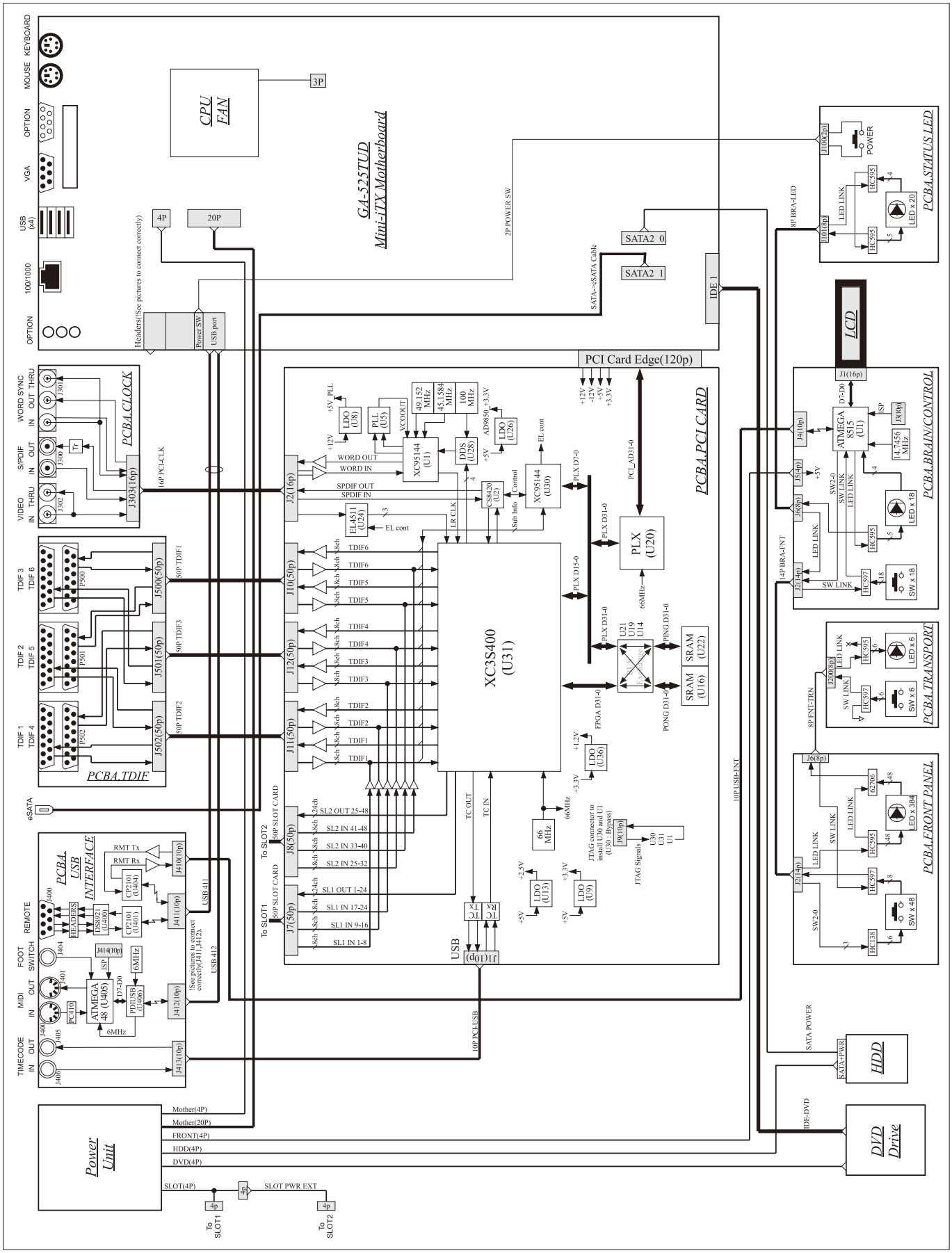
18. **'ESC'** キーを押し、**'Y'** キーを押してから**'Enter'** キーを押して、保存せずに終了します。
これで、X-48MK II はハードディスクから立ち上がり、X-48MK II レコーダーのトラック画面が表示されます。

19. 再起動が完了すると、新しいハードウェア / ソフトウェアを認識するための再起動画面が表示されます。**'OK'** を押すとX-48MK II が再起動します。

これで全てのインストールが完了しました。

5. Block Diagram

ブロックダイアグラム



6. Error Messages list

エラーメッセージリスト

Action	Message	原因(Cause)	対策(Solution)
Edit->Repeat Paste	Please enter a number between x and x.	ユーザーが無効なリピート回数を入力しました。	有効な数値を入力してください。
		user entered invalid number of repeats.	enter valid number.
New Project	You have entered an invalid name for the new project.	名前の長さが長過ぎる可能性があります。	新規プロジェクトを作成しなおしてください。
		possibly invalid name length.	repeat new project creation.
New Project	An internal error occurred creating your new project -- no default document exists!	不明	再起動が必要の場合があります。
		unknown	possible re-boot required.
New Project	The project 'project name' already exists.	入力した名前が現存のプロジェクトと同じです。	固有のプロジェクト名を再入力してください。
		the name entered is the same as existing project.	re-enter a unique project name.
New Project	An error occurred creating the new project.	不明- ハードドライブエラーの可能性があります。	ドライブをチェックしてください。
		unknown - possible hard drive error.	check drive
Open Project	The document is an unsupported version and cannot be opened.	無効なファイル	
		Invalid file	
Open Project	An error occurred while loading the document.	ファイルが壊れている可能性があります。	
		possible file corruption.	
Import Project	Invalid project file.	プロジェクトファイルが無効です。	
		Invalid project file.	
Import Project	An error was encountered while trying to import the project.	ファイルが壊れている可能性があります。	
		possible file corruption.	
Import Project	The imported project contains x clips on the timeline that are missing their underlying audio file. You can use the Audio Pool window to relink or remove the regions that are missing.	オリジナルのプロジェクトをエキスポートしたとき、オーディオファイルがありませんでした。	Audio Pool 画面でリンクしなおすか、ファイルのないリージョンを削除してください。
		the original project was missing audio files when it was exported.	use the Audio Pool window to relink or remove the regions that are missing.
Export Project	The folder 'export project name' is not empty. Please choose an unused folder.	エキスポートしたプロジェクトに入力した名前が現存のフォルダの名前と同じです。	固有の名前を再入力してください。
		name entered for exported project is name of existing folder.	re-enter a unique name.

Action	Message	原因(Cause)	対策(Solution)
Export Project	Invalid project file.	エキスポートしたファイルの拡張子が無効です。	拡張子は自動的に適用されます-拡張子を除いたプロジェクト名を再入力してください。
		exported file has invalid extension.	extensions are automatically applied - re-enter project name without extension.
Export Project	An error was encountered while trying to export the project.	不明	
		unknown	
Export Project	The specified export drive doesn't have enough free space to complete the export operation. The project will need approximately 'x' MB, but you have only 'x' MB available.	ターゲットのドライブに十分な空き容量がありません。	十分なスペースのあるドライブを使用してください。
		target drive doesn't have enough free space on it.	choose a drive that has enough free space on it.
Export Project	The exported file will exceed the maximum file size allowed. Try a non-embedded AAF export.	Audio 内蔵(embedded)のAAFエキスポートファイルは最大サイズ2GB です。	Audio が別ファイルの（nonembeddedの）AAF エキスポートファイルを使用してください。
		an AAF export file with embedded audio has a maximum size of 2GB.	use the non-embedded AAF export.
Save Project	An error occurred while saving the document.	不明-ハードドライブエラーの可能性があります。	ドライブをチェックしてください
		unknown - possible hard drive error.	check drive.
Import Audio	A file with the desired name ('file name') already exists in the project...	インポートされたオーディオファイルは固有の名前をつけることが必要です。	インポートするファイルの名前をもう一度付けてください。
		imported audio files must have unique names.	rename the file to be imported.
Import Audio	Unable to copy the file: 'file name' The project directory may be full.		
Import Audio	Unable to import the file: 'file name' The audio file format may not be supported.	そのAudio ファイルタイプに対応していません。	他社のユーティリティを使用してファイルを対応ファイルに変換してください。
		the file type is not supported.	use a 3rd party utility to convert the file to a known type.
Import Audio	The current project's audio folder is invalid.	プロジェクト・オーディオ・フォルダが見つかりませんでした。	プロジェクトファイルおよびオーディオファイルへのパスを再確認してください。
		the project audio folder was not found.	check path of project files and audio files.
Import Audio	There are no tracks to import the audio file(s) to...	内蔵トラックエラー	再起動してください。
		internal track error.	re-boot
Import Audio	An unknown error occurred while trying to import audio file(s).	不明	別のファイルおよび / または別のプロジェクトを試してみてください。
		unknown	try a different file and/or a different project.

Action	Message	原因(Cause)	対策(Solution)
Import Audio	An unknown error occurred while importing the audio file(s).	不明	別のファイルおよび / または別のプロジェクトを試してみてください。
		unknown	try a different file and / or a different project.
Installer	The installer application was not found on an optical disk or external memory device. Insert a disk or device containing the installer application and try again.	インストーラアプリケーションファイルがありません。	インストーラファイルを入れるか、完全インストールを行ってください。
		the installer application file is missing.	provide the installer file or do a full install.
Store settings	You must specify a valid filename to save the system settings to.	ユーザーが無効な長さまたは文字の名前を入力しました。	有効な名前を使って、システム設 定を保存してみてください。
		user entered name with invalid length or invalid characters.	try saving system settings again with a valid name.
Drive Sharing	You can't share a drive while the X48 is playing or recording...	再生または録音中にX48 データドライブをシェアしようとしました。	再生または録音中のシェアをしないでください。
		attempt to share the X48 data drive while playing or recording.	don't attempt this.
Drive Sharing	An error occurred trying to share the X48's 'Data' drive.	不明	
		unknown	
Set X48 Name	Unable to set X48 name.	不詳のシステムエラー	
		unknown system error.	
Project Backup	An error occurred while burning the backup media.	DVD+RW ドライブまたはメディアにエラーが生じました。	別のディスクで試してください。
		an error occurred with the burner or the media.	try another disc.
Drive Benchmarking	An error occurred while trying to benchmark the specified drive. Check to ensure there is sufficient free space on the drive to perform the tests.	スペースが不十分またはドライブエラー。	ドライブ上に空きスペースを作ってください。
		insufficient space or drive error.	create more drive space.
File Manager - delete	Could not delete selected files.	ファイルを使用中、またはドライブエラー。	
		a file is in use or there is a drive error.	
File Manager - delete	A file you have chosen to delete is currently in use by the system.	選択したファイルの1 つまたは複数を使用中。	まず別のプロジェクトを開き、次にもう一度削除操作を行ってください。
		one or more of the selected files is in use.	open a different project first, then try the delete operation again.
File Manager - New Folder	A folder with the name 'folder name' already exists. Please enter a different name.		固有の名前を入力してください。
			enter a unique name.

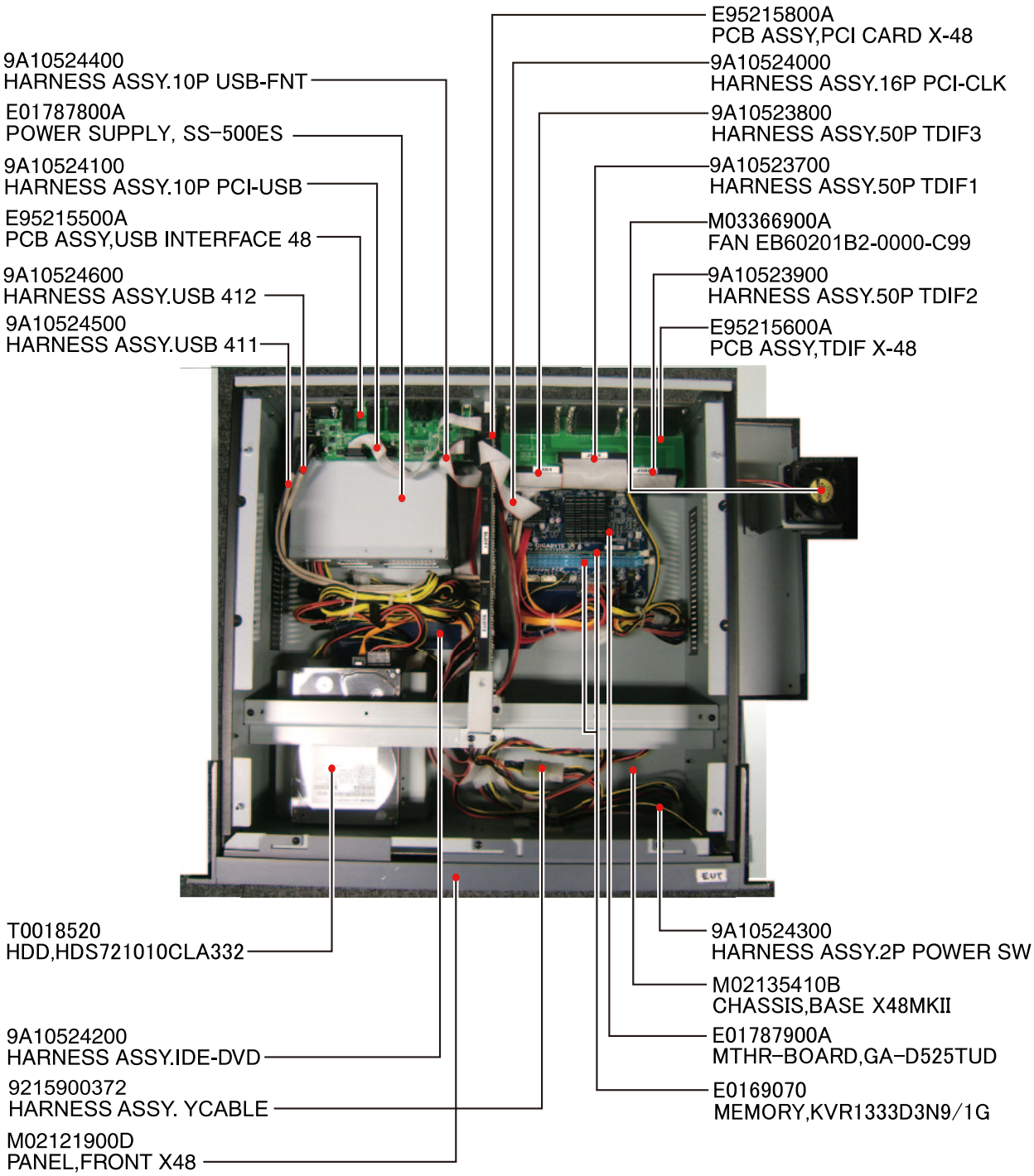
Action	Message	原因(Cause)	対策(Solution)
File Manager - New Folder	Cannot create directory. Please try again.	システムエラーまたはドライブエラー	
		system or drive error.	
File Manager - Copy	Cannot copy these items because the folder 'folder name' being copied has the same name as an existing file.		フォルダの名前を付けなおしてください。
			rename folder.
File Manager - Copy	Cannot copy these items because an unknown error occurred.		
File Manager - Copy	An unknown error occurred during the file transfer.		
File Manager - Rename	The filename cannot be blank. Please enter a valid filename.		
File Manager - Rename	A file named 'file name' already exists. Please enter a different name.		固有の名前を入力してください。
			enter a unique name.
File Manager - Rename	A folder named 'folder name' already exists. Please enter a different name.		固有の名前を入力してください。
			enter a unique name.
File Manager - Rename	Could not rename this item.	システムエラーまたはドライブエラーの可能性があります。	
		possible system or drive error.	
File Manager - Rename	A folder name cannot be longer than 255 characters. Please enter a shorter filename.		有効な名前を入力してください。
			enter a valid name.
File Manager - Rename	A folder name cannot contain any of the following characters: Ä / : * ? "" < > | Please enter a valid filename.	アクティブなプロジェクトが、アンマウントしようとしているボリューム上にある可能性があります。	
		possibly the active project is on the volume to unmount.	
File Manager - Unmount	An error occurred trying to unmount the volume. Ensure the drive is not in use, then try again.	システムがそのボリュームを使用中の可能性があります。	あとでまたやり直すか、X-48MK II の電源を落としてください。
		the system may still be using the volume.	try again later or shut down the X-48MK II .
File Manager - Restore	An error occurred reading the restore data.	システムエラーまたはドライブエラーの可能性があります。	
		possible system or drive error.	
File Manager - File Backup	There are no burnable CD or DVD drives in the system.	DVD+RW ドライブが見つかりませんでした。	
		did not find burner.	

Action	Message	原因(Cause)	対策(Solution)
File Manager - File Backup	You didn't select any files or folders to burn.	選択されていません。	1 つまたは複数のファイル / フォルダを選択してください。
		no selection.	select one or more files / folders.
File Manager - File Backup	An error occurred assembling the list of files to burn.	システムエラーまたはドライブエラーの可能性があります。	
		possible system or drive error.	
File Manager - File Backup	There are no files to burn...	バックアップのサイズが 0 バイトです。	
		size of backup is 0 bytes.	
File Manager - File Backup	One or more files exceed the maximum media capacity. Please use a larger disk type.		サイズの大きいディスクタイプを使用してください。
			use a larger disk type.
File Manager - File Backup	An error occurred building the disk images to burn.	システムエラーまたはドライブエラーの可能性があります。	
		possible system or drive error.	

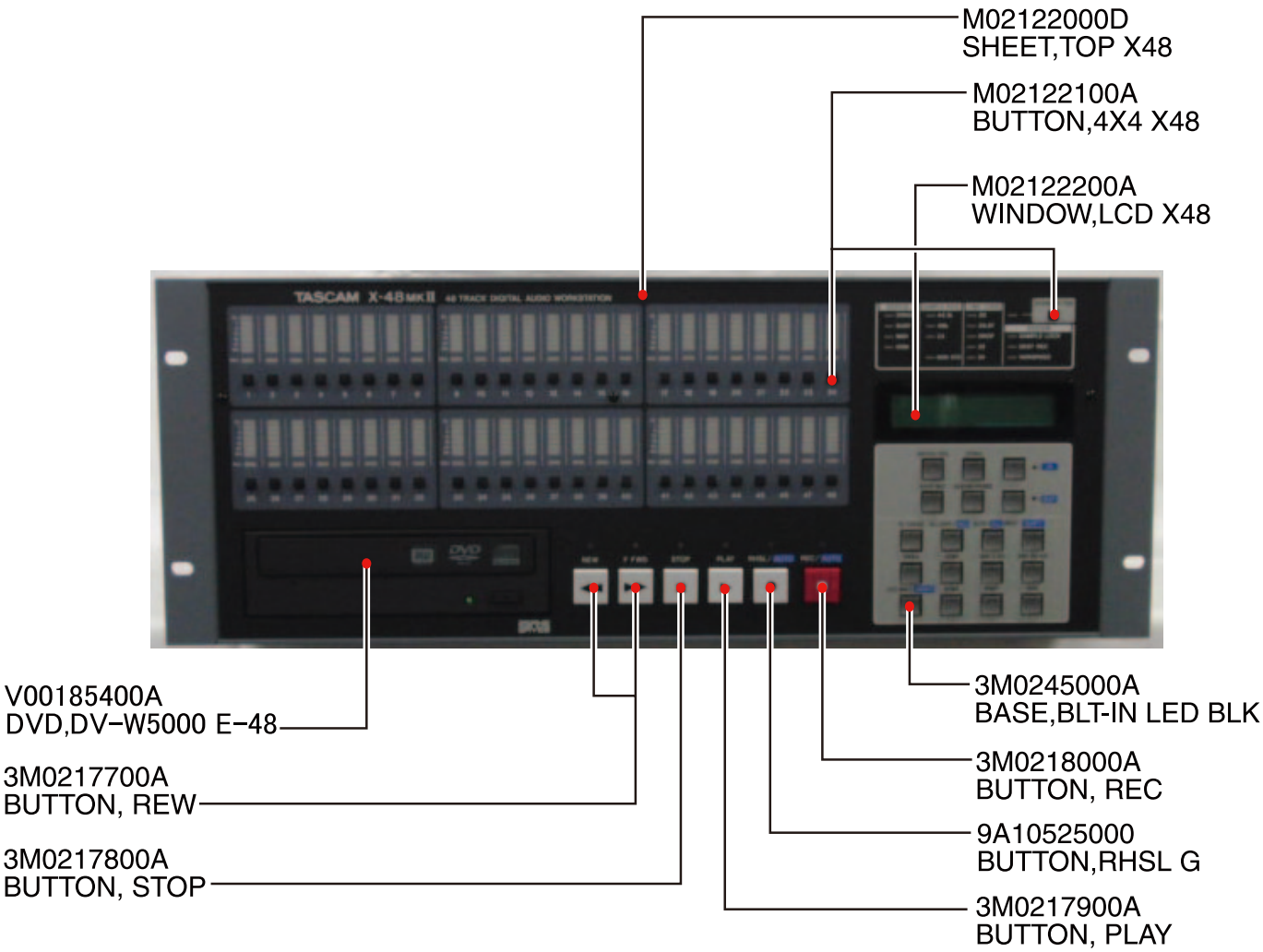
7. Exploded Views and Parts List

分解図とパーツリスト

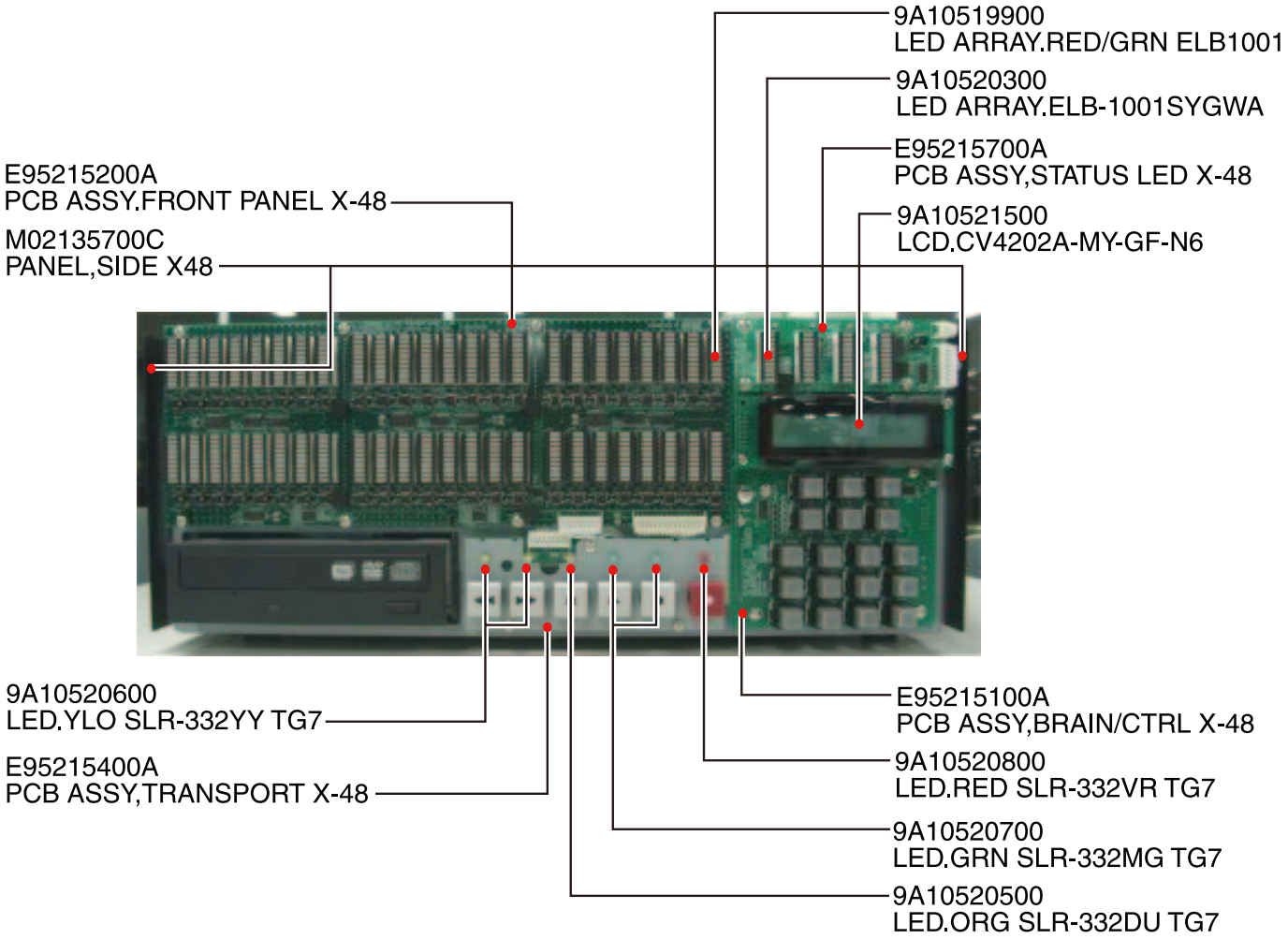
Top View



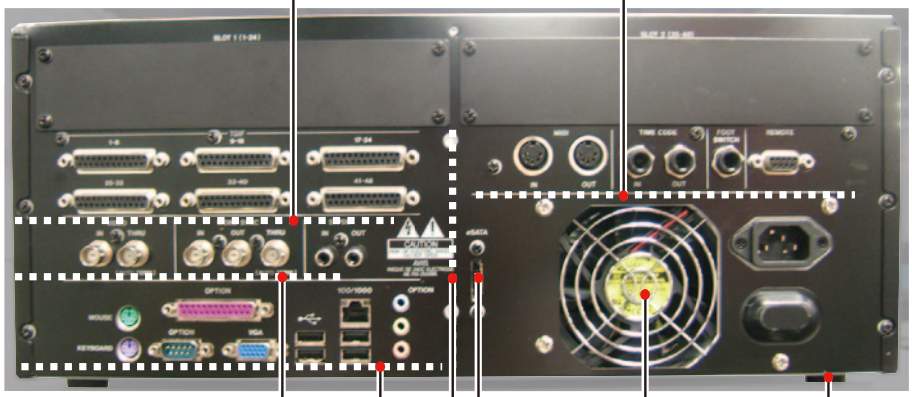
Front Panel

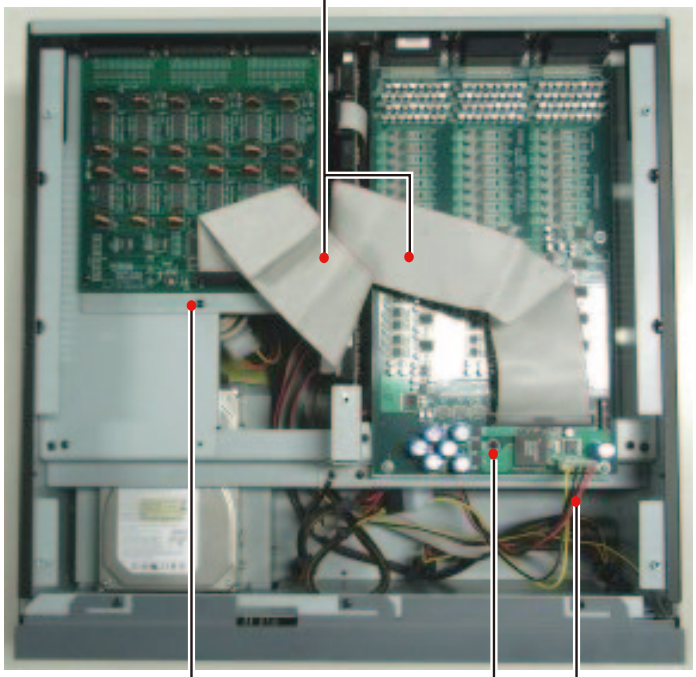

M02122000D
SHEET,TOP X48
M02122100A
BUTTON,4X4 X48
M02122200A
WINDOW,LCD X48
V00185400A
DVD,DV-W5000 E-48
3M0217700A
BUTTON, REW
3M0217800A
BUTTON, STOP
3M0245000A
BASE,BLT-IN LED BLK
3M0218000A
BUTTON, REC
9A10525000
BUTTON,RHSL G
3M0217900A
BUTTON, PLAY

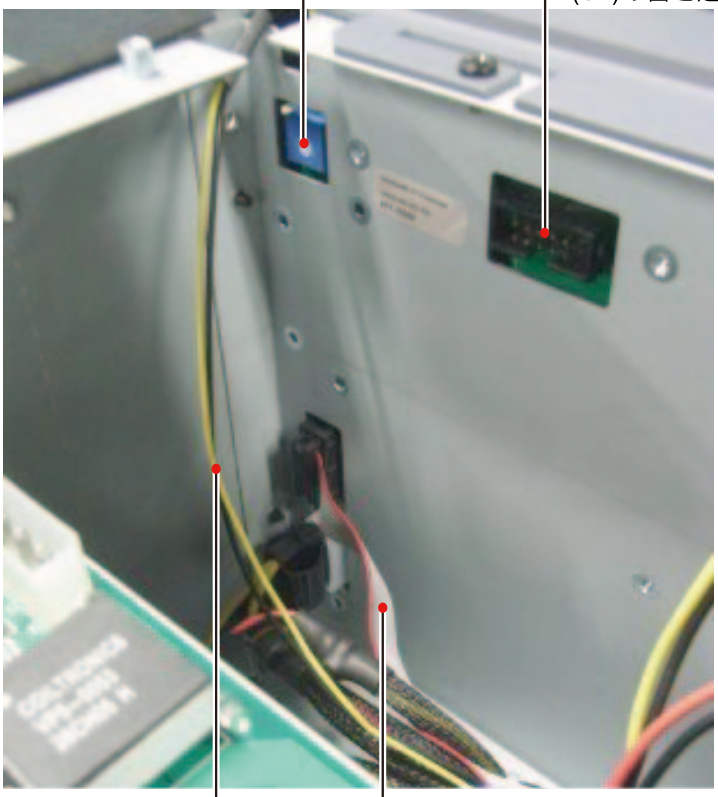
Front Raw


9A10519900
LED ARRAY.RED/GRN ELB1001
9A10520300
LED ARRAY.ELB-1001SYGWA
E95215700A
PCB ASSY,STATUS LED X-48
9A10521500
LCD.CV4202A-MY-GF-N6
E95215200A
PCB ASSY.FRONT PANEL X-48
M02135700C
PANEL,SIDE X48
9A10520600
LED.YLO SLR-332YY TG7
E95215400A
PCB ASSY,TRANSPORT X-48
E95215100A
PCB ASSY,BRAIN/CTRL X-48
9A10520800
LED.RED SLR-332VR TG7
9A10520700
LED.GRN SLR-332MG TG7
9A10520500
LED.ORG SLR-332DU TG7

Rear Panel


E95215600A
PCB ASSY,TDIF X-48
E95215500A
PCB ASSY,USB INTERFACE 48
E95215900A
PCB ASSY,CLOCK X-48
E01787900A
MTHR-BOARD,GA-D525TUD
E95215800A
PCB ASSY,PCI CARD X-48
9A10524900
FOOT,ABS BLK X-48
E01787800A
POWER SUPPLY, SS-500ES
E01788000A
HARNESS ASSY,SATA-eSATA


9A10526400
HARNESS ASSY,50P SLOT CARD
9A10527100
SCREW,BPB 3*8 FZB
9A10524700
HARNESS ASSY.SLOT PWR EXT

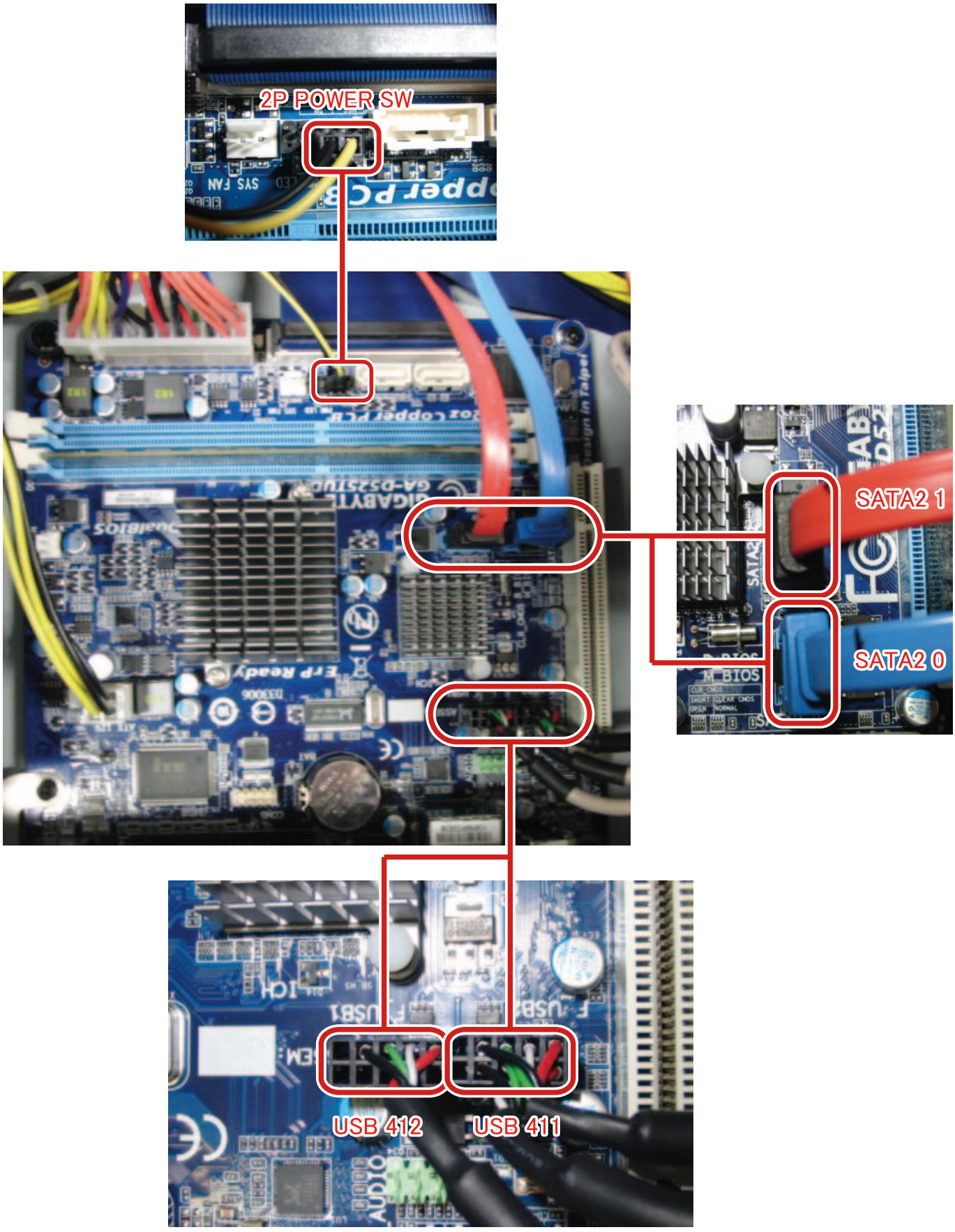

Adjust LCD contrast.
LCDのコントラスト調整
Used only to install ATMEGA8515 (U1) on the BRAIN/CONTROL board.
BRAIN/CONTROL基板上のATMEGA8515 (U1)の書き込みに使用します。
9A10524300
HARNESS ASSY.2P POWER SW
9A10524400
HARNESS ASSY.10P USB-FNT

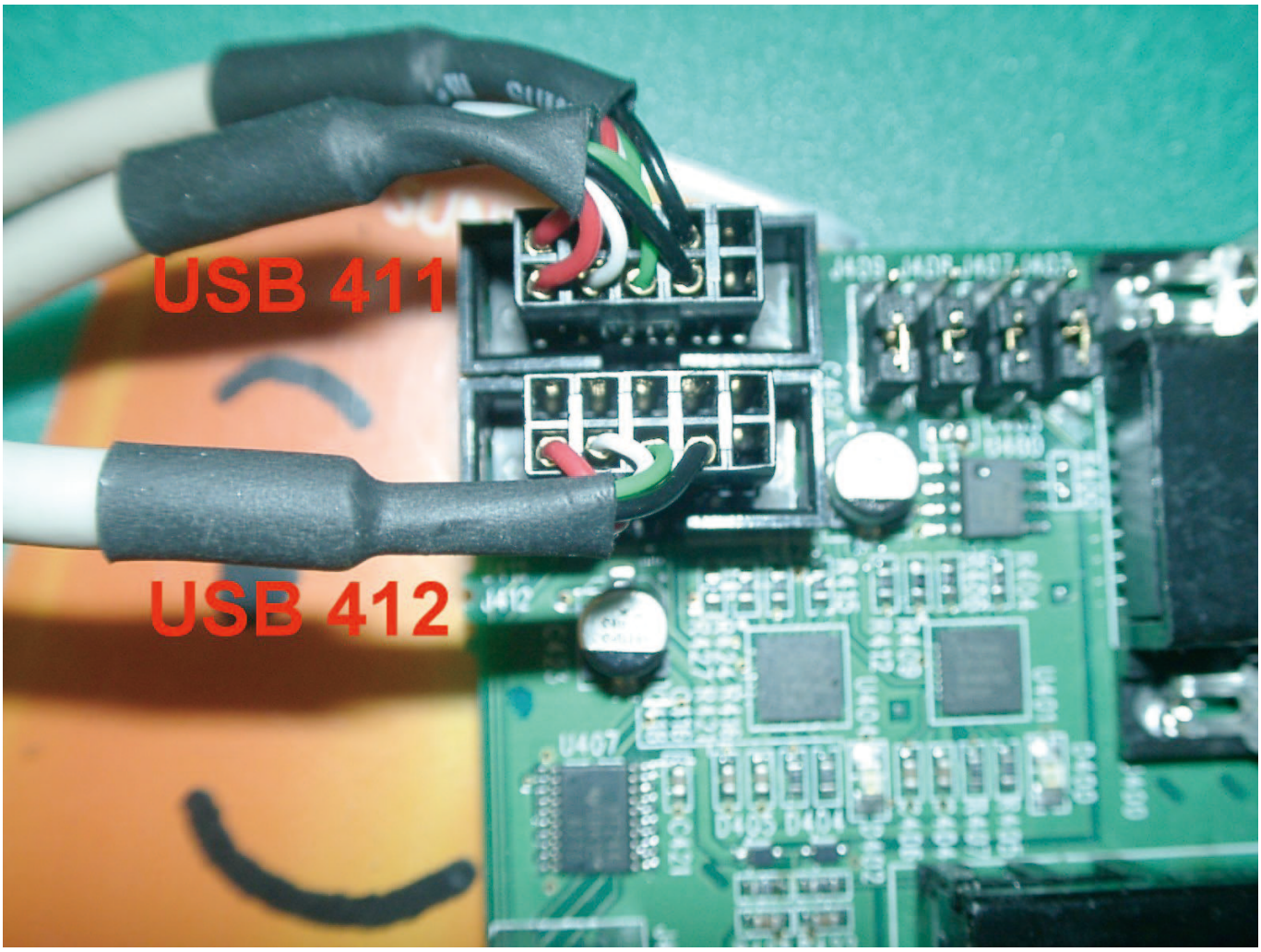
Exploded View

REF.NO.	PARTS NO.	DESCRIPTION .	KCR PARTS NO
	E01787800A	POWER SUPPLY, SS-500ES	H089006124
	T0018520	HDD,HDS721010CLA332	8089006135
	E0169070	MEMORY,KVR1333D3N9/1G	8089006146
	V00185400A	DVD,DV-W5000 E-48	H089005483
	M03366900A	EB60201B2-0000-C99	8028000682
	E01787900A	MTHR-BOARD,GA-D525TUD4	8089006157
	E01788000A	HARNESS ASSY,SATA-eSATA	8025070113
	9A10523400	HARNESS ASSY. 8P BRA-LED	9215900076
	9A10523500	HARNESS ASSY. 8P FNT-TRN	9215900087
	9A10523600	HARNESS ASSY. 14P BRA-FNT	9215900098
	9A10523700	HARNESS ASSY. 50P TDIF1	9215900101
	9A10523800	HARNESS ASSY. 50P TDIF3	9215900112
	9A10523900	HARNESS ASSY. 50P TDIF2	9215900123
	9A10524000	HARNESS ASSY. 16P PCI-CLK	9215900134
	9A10524100	HARNESS ASSY. 10P PCI-USB	9215900167
	9A10524200	HARNESS ASSY. IDE-DVD	8026800013
	9A10524300	HARNESS ASSY. 2P POWER SW	9215900178
	9A10524400	HARNESS ASSY. 10P USB-FNT	9215900189
	9A10524500	HARNESS ASSY. USB 411	9215900190
	9A10524600	HARNESS ASSY. USB 412	9215900203
	M02122100A	BUTTON, 4X4 X48	0228900071
	M02121900D	PANEL, FRONT X48	4500260577
	M02122300B	ANGLE, RACR X48	4520260059
	9A10524800	SCREW, BPA 4*10 FZB	4300420348
	M02122010A	SHEET, TOP X48 MK2	5110400340
	M02122200A	WINDOW, LCD X48	5240400065
	M02135700C	PANEL, SIDE X48	4500620015
	M02135600D	COVER, TOP X48	4500660271
	M02135410B	CHASSIS, BASE X48 MK2	4500660384
	9A10524900	FOOT, ABS BLK X-48	5131002700
	3M0217700A	BUTTON REW	5191000487
	3M0217800A	BUTTON STOP	5191000488
	3M0217900A	BUTTON PLAY	5191000499
	3M0218000A	BUTTON REC	5191000502
	3M0245000A	BASE, BLT-IN LED BLK	5191000513
	M01830400A	B0TTON, BLT-IN LED	5191000524
	9A10525000	BUTTON, RHSL G	5191000535
	9A10525100	POLTHN BAG, 80*90	6030000685
	9A10525200	SHEET, PE 900*1500	6030080074
		HARNESS ASSY. YCABLE	9215900372
	M03321400A	PLATE (EARTH M/B)	4520908043
	M03321300A	PLATE (EARTH USB)	4521000197
	M03320900A	BRACKET (FAN)	4520602039
	M02135900B	PLATE (ANALOG R)	4520602028
	M03321000A	BRACKET (PS)	4520602040

8. Cable Connection

ケーブル接続図

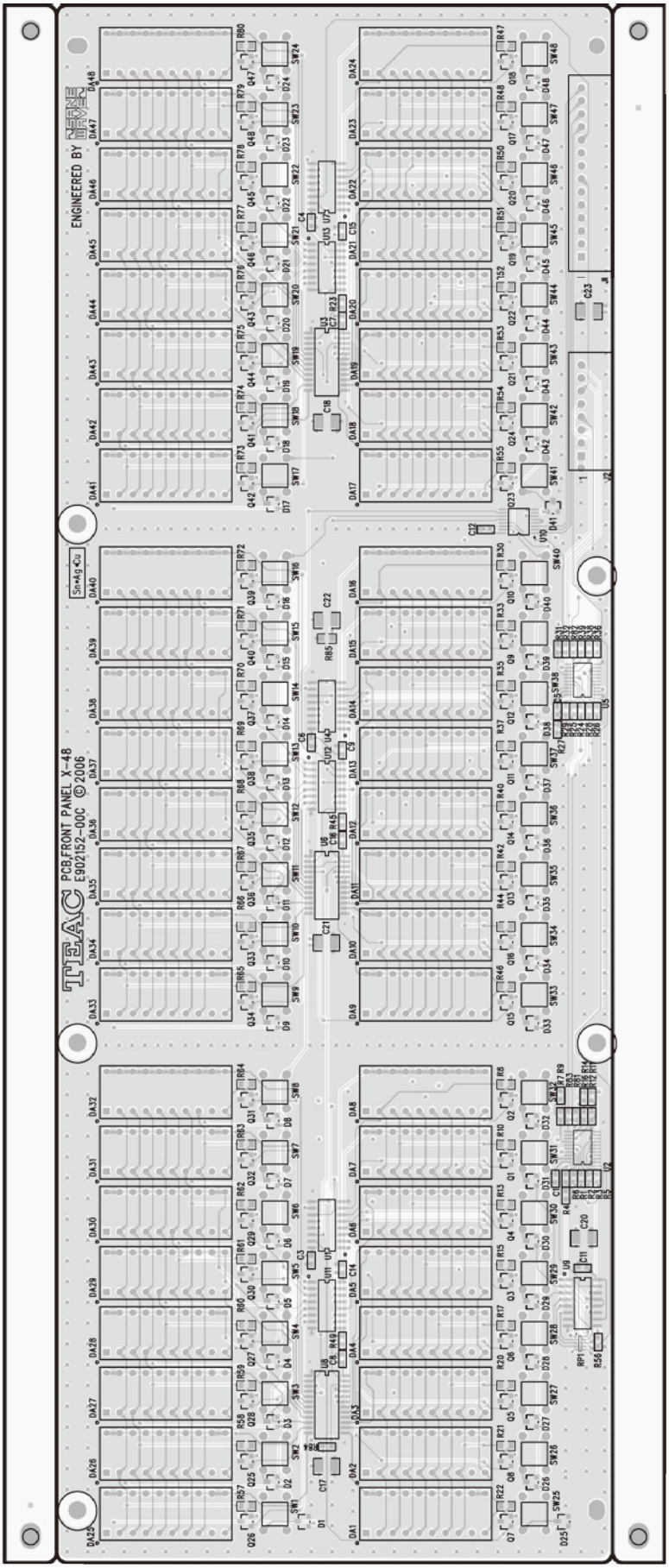



USB 411
USB 412

9. PC Boards and Parts List

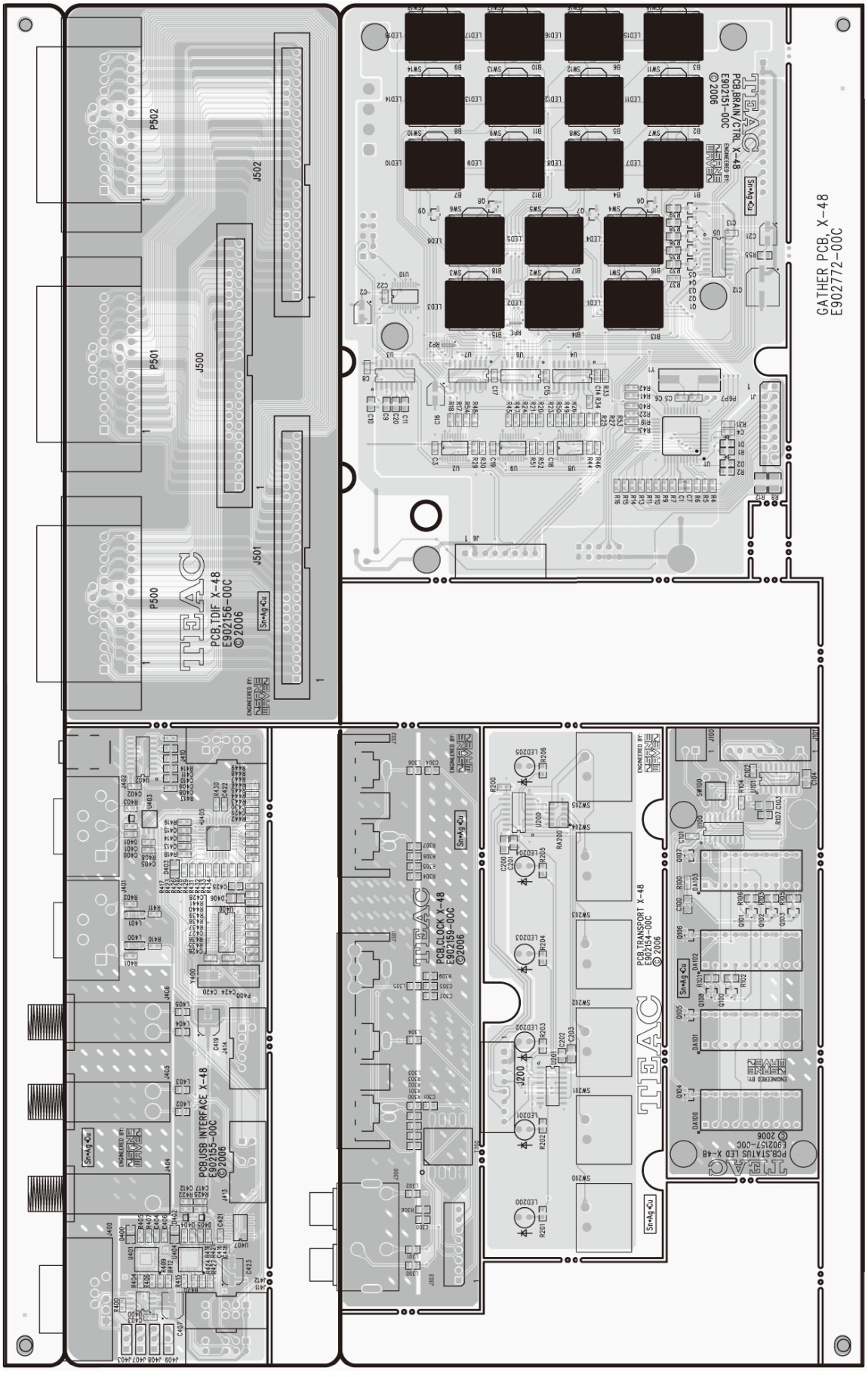
基板図とパーツリスト

FRONT PANEL PCB ASSY

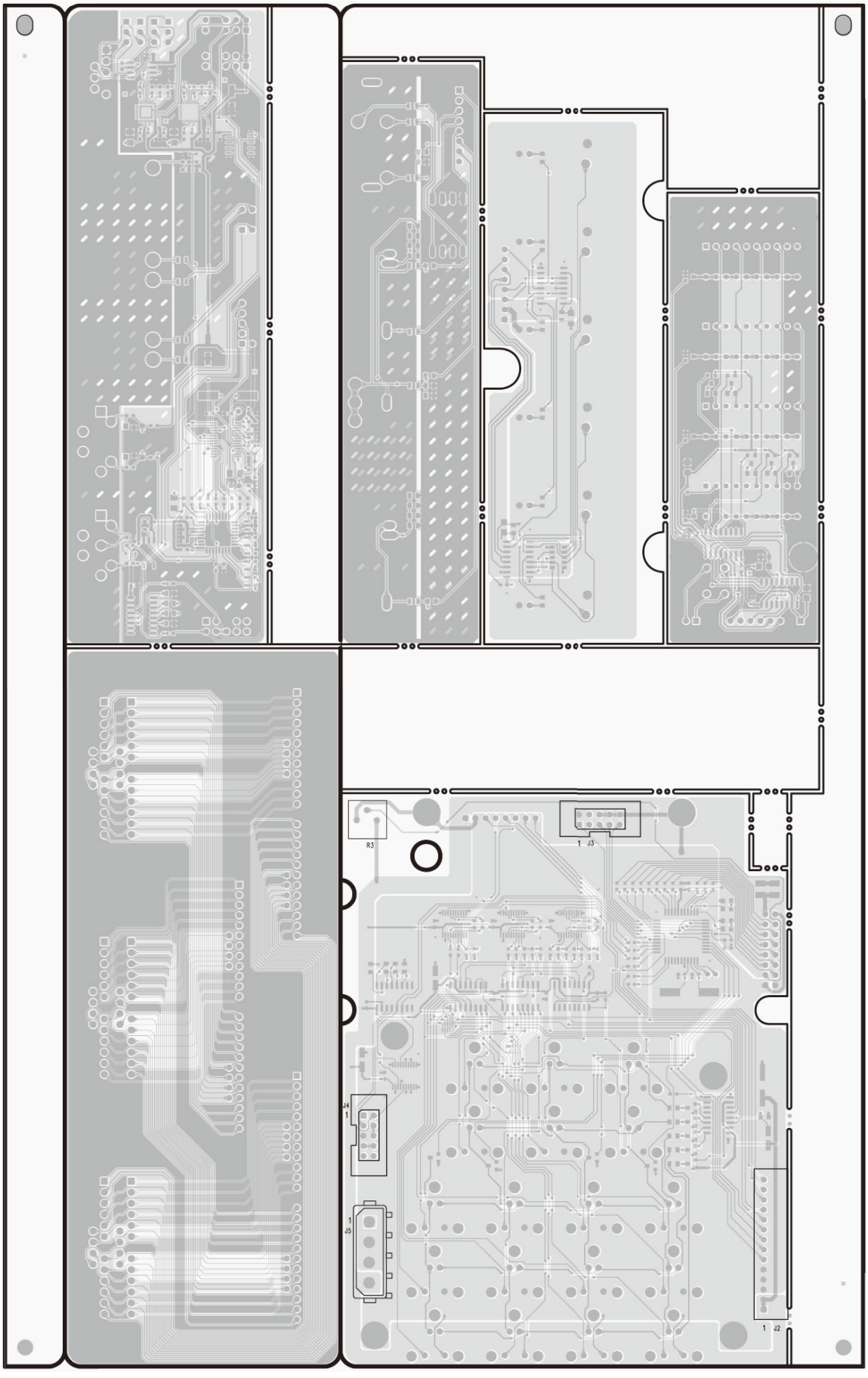


GATHER PCB ASSY (STATUS LED, TRANSPORT, BRAIN/CTRL, TDIF, CLOCK, USB INTERFACE) (SIDE A)

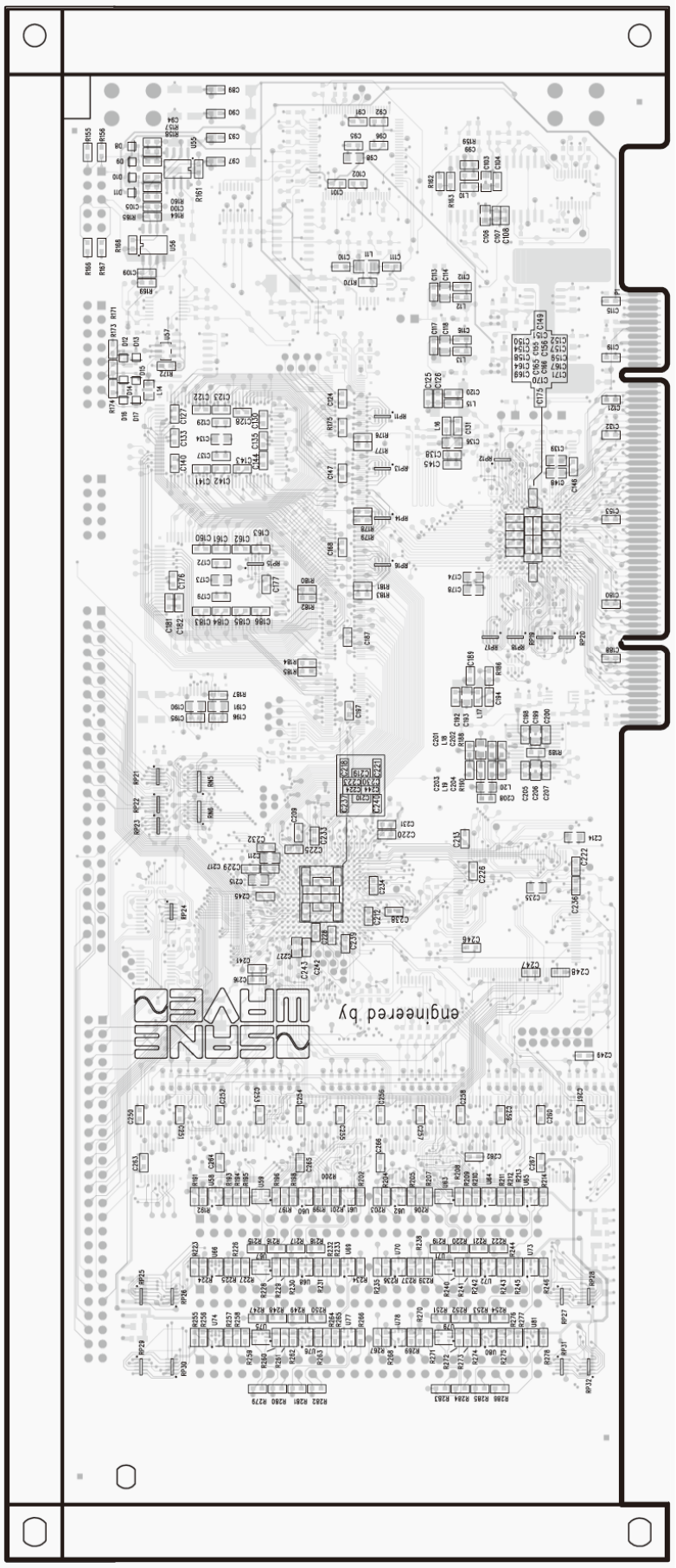
SIDE A



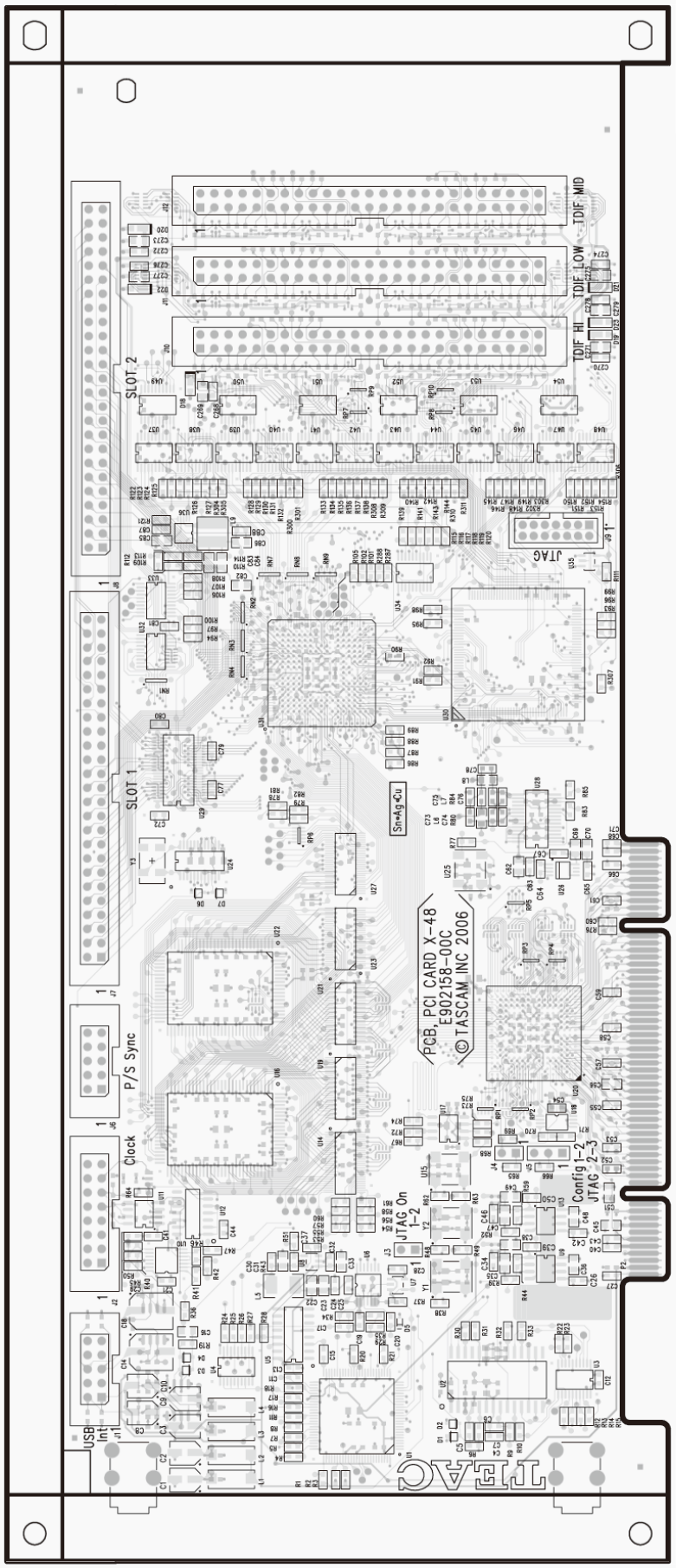
GATHER PCB ASSY (STATUS LED, TRANSPORT, BRAIN/CTRL, TDIF, CLOCK, USB INTERFACE)
SIDE B



PCI PCB ASSY
SIDE A



PCI PCB ASSY
SIDE B



PCB Assy FRONT PANEL

REF.NO.	PARTS NO.	DESCRIPTION .	KCR PARTS NO
	E95215200A	PCB ASSY. FRONT PANEL X-48	 9211900083
		PCB, FRONT PANEL X-48	
DA1 - 48	9A10519900	LED ARRAY. RED/GRN ELB1001	 7005040043
J1	9A10520000	CONNECTOR. JST-E-250-14RT	 8004140392
J2	9A10520100	CONNECTOR. JST-E-250-08RT	 8004080779
SW1 - SW48	9A10520200	SW. TACT B3F-1050	 8012100180
		.....	 8012100191

GATHER PCB Assy

REF.NO.	PARTS NO.	DESCRIPTION .	KCR PARTS NO
	E95215200A	GATHER PCB ASSY, X-48	9211900129
		GATHER PCB, X-48	
		PCB ASSY, STATUS LED X-48	
DA100-103	9A10520300	LED ARRAY. ELB-1001SYGWA	7005020589
J100	9A10520400	CONNECTOR. JST-E-250-02RT	8004021609
J101	9A10520100	CONNECTOR. JST-E-250-08RT	8004080779
SW100	9A10520200	SW. TACT B3F-1050	8012100180
			8012100191
		PCB ASSY,TRANSPORT X-48	
J200	9A10520100	CONNECTOR.JST-E-250-08RT	8004080779
LED202	9A10520500	LED.ORG SLR-332DU TG7	7005060029
LED200, 201	9A10520600	LED.YLO SLR-332YY TG7	7005010187
LED203, 204	9A10520700	LED.GRN SLR-332MG TG7	7005020512
LED205	9A10520800	LED.RED SLR-332VR TG7	7005000741
LED200-LED205	9A10520900	HOLDER. LED LED-7	5130000719
SW200-SW205	9A10521000	SW. PUSH SKBMFA000A-TK	8012050589
		PCB ASSY, BRAIN/CTRL X-48	
J1	9A10521100	CONNECTOR.16P B03-2X8AG1	8004160334
J2	9A10520000	CONNECTOR.JST-E-250-14RT	8004140392
J3, J4	9A10519500	CONNECTOR.10P GBH1-103	8004100567
J5	9A10521200	CONNECTOR.4P GAX-B-508	8004041516
J6	9A10520100	CONNECTOR.JST-E-250-08RT	8004080779
LED1-18	9A10520500	LED.ORG SLR-332DU TG7	7005060029
R3	9A10521300	VR.TRIM 10 KOHM	7001830932
SW1-18	9A10521400	SW. TAFCT EVQ11L05R	8012050590
	9A10521500	LCD. CV4202A-MY-GF-N6	7010000942
LCD	9A10521600	CONNECTOR. 16P GPD11-165	8004160345
		PCB ASSY, TDIF X-48	
J500-502	9A10519700	CONNECTOR. 50P GBH1-503	8004500103
P500-502	9A10521700	CONNECTOR. D-SUB 50P 2PCS	8004500114
			8004500147
		PCB ASSY, CLOCK X-48	
J300	9A10521800	JACK. 2P RCA RJ-1078	8013090003
J301	9A10521900	JACK. 3P BNC P2286-A	8013090014
J302	9A10522000	JACK. 2P BNC P2360	8013090025
J303	9A10519600	CONNECTOR. 16P GBH1-163-1	8004160323
T300	9A10522100	TRANS. PULSE PE-65812NLT	7008040067
		PCB ASSY, USB INTERFACE 48	
J400	9A10522200	CONNECTOR. 9P GDB0-09FR	8004090579
J401, 402	9A10522300	CONNECTOR. MIDI 2P HDC-052	8004140416
J403, 407-409	9A10522400	CONNECTOR. 3P GPS11-035-1	8004031250
J404-406	9A10522500	JACK. TRS LJB0660-3RT	8014990902
			8014990913
J410-414	9A10519500	CONNECTOR. 10P GBH1-103	8004100567

PCB Assy, PCICARD

REF.NO.	PARTS NO.	DESCRIPTION .	KCR PARTS NO
	E95215800A	PCB ASSY, PCI CARD X-48 PCB, PCI CARD X-48	9211900107
J1, J6	9A10519500	CONNECTOR.10P GBH1-103	8004100567
J2	9A10519600	CONNECTOR.16P GBH1-163	8004160323
J7, J8, J10-J12	9A10519700	CONNECTOR.50P GBH1-503	8004500103
J9	9A10519800	CONNECTOR.14P GBH2-142	8004140405

10. Included Accessories

付属品

Included Accessories

REF.NO.	PARTS NO.	DESCRIPTION .	KCR PARTS NO
	M02117200B	CORR CDBD CS,X-48	6000006784
	9A10525300	CORR CDBD CS,OUTER X-48	
	9A10525400	CUSHION,L X48	6130001426
	9A10525500	CUSHION,R X48	6130001437
	3E014150	POWER CORD,UL-G [J,US/C]	
	3E014160	POWER CORD,EUR-G [E]	
	3E014170	POWER CORD,UK [UK]	
	3E014180G	POWER CORD,AUS [A]	
	3E039940	POWER CORD,TM G [T]	
	E0178290	POWER CORD,KOR C13 1.8M G [K]	
	E0147010	POWER CORD,UE-96S-239 G [CH]	
	E0168660	AC PLUG,WS-037-A PSE G	
	9A10525600	POLTHN BAG,230*300	6030000323
	D01152205A	OWNERS MNL,(J) X48mk2 G [JEX]	
	D01152220A	OWNERS MNL,(E) X48mk2 G [US/C]	
	D01152281A	OWNERS MNL,(F) X48mk2 G [E]	
	D01152280A	OWNERS MNL,(G) X48mk2 G [E]	
	D01152282A	OWNERS MNL,(I) X48mk2 G [E]	
	D01152283A	OWNERS MNL,(S) X48mk2 G [E]	
		OWNERS MNL,(C) X48mk2 G [CH]	
	T00183800A	SYSTEM RESTORE,X-48MK2 G	
	D01152800A	DOCUMENTATION,X-48MK2 G	
	D00729600E	WARRANTY CARD(JPN)	
	D01059900A	CARD,REGISTRATION T/C G	
	D00822001B	WARR CARD,ENG/FRE C A G	
	3M0013300A	ENVELOPE,(WARR CARD) G	
	D00819901B	DISTRIBUTOR LIST,WLD CA G	
	D00712700E	SHEET,REGIST WEB JPN G	
	D00712800D	SHEET,REGIST FAX JPN G	
	3M0028300A	ASSY,RACK MOUNT SCREW KIT	
	3B0005812A	SCREW,BPA M5X12 (NI)	
	3M0028100A	WASHER-FIBER(BLK)	
	M02676400A	POLTHN BAG,60*100*0.03 G	
	3M0003000B	POLTHN BAG,(MANUAL) G	

NOTES

- PC boards shown are viewed from parts side.
- Parts marked with * require longer delivery time.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in this manual.
- ⚠ Parts marked with this sign are safety critical components. They must be replaced with identical components - refer to the appropriate parts list and ensure exact replacement.
- Parts of [ ] mark can be used only with the version designated.
  [J] : JAPAN [US/C] : U.S.A./CANADA [E] : EUROPE
  [UK] : U.K. [A] : AUSTRALIA [JEX] : JAPAN & ASIA
  [T] : TAIWAN [K] : KOREA [CH] : CHINA
  [ETC] : U.S.A./CANADA/South America

注 意

- プリント基板図は部品面を示しています。
- * 印の部品は納期が若干かかります。
  あらかじめご了承ください。
- 分解図に部番のない部品および品番のない部品は供給できません。
- 標準の抵抗、コンデンサーは省略してあります。
  回路図を参照してください。
- ⚠ 印は安全重要部品です。

- 仕向先
  [J] : JAPAN [US/C] : U.S.A./CANADA [E] : EUROPE
  [UK] : U.K. [A] : AUSTRALIA [JEX] : JAPAN & ASIA
  [T] : TAIWAN [K] : KOREA [CH] : CHINA
  [ETC] : U.S.A./CANADA/South America

11. IF-AN24X

IF-AN24X

Programming the CPLD on IF-AN24X

Tools :

A dedicated test PC, Xilinx parallel cable IV and ISE7.1(or later) are necessary as well as the X-48MK II .

Programming Xilinx Chips :

1. Install IF-AN24X board to X-48MK II and connect the power cable and the 50pin cable.
2. Plug the **'Xilinx Parallel Cable IV'** into the dedicated test PC's parallel port. Plug the mini-din into the mouse or keyboard port as well. Connect the IDC header of the **'parallel cable 4'** to **'J3'**(14pin) connector on the IF-AN24X board. The red stripe on the cable should line up with pin 1.
3. Power on the X-48MK II .
4. On the PC, run iMPACT.
   [Start menu -> Program -> Xilinx ISE 7.1i -> Accessary -> iMPACT]

   On a pop-up window, select **'Create new project'** if this is the first time. From the second time, select **'load most recent project'**.
5. The **'Operation Mode Selection'** window will pop up. Select **'Configure Devices'** and click **'Next'**.

IF-AN24XのCPLDのプログラミング

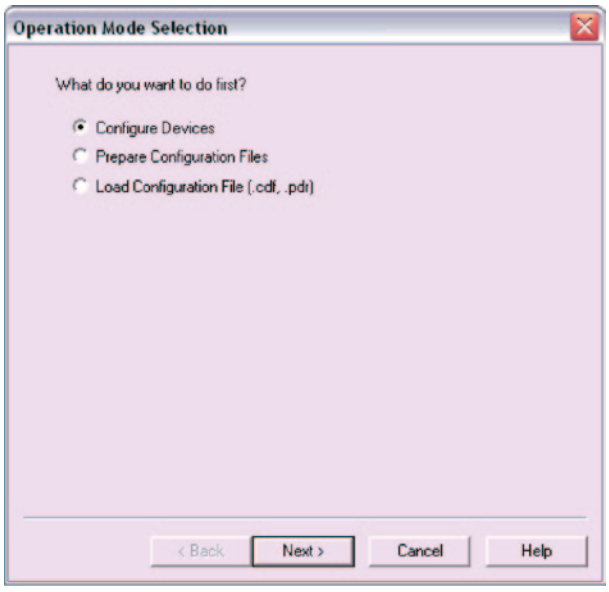
ツール :

X-48MK II 本体の時と同じ様に、試験用PC、Xilinxパラレルケーブル IV、ISE7.1（またはそれ以降）が必要です。

Xilinx チップのプログラミング :

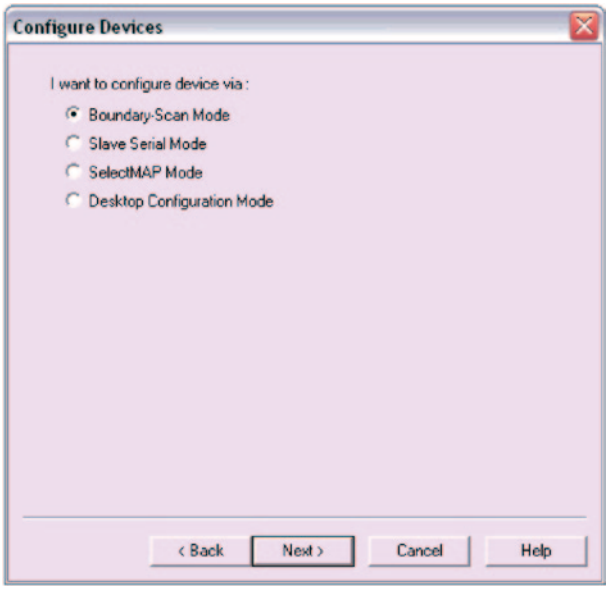
1. IF-AN24XカードをX-48MK II に取り付け、電源コードと50ピンケーブルを接続します。
2. **'Xilinx Parallel Cable（パラレルケーブル）IV'**を試験用PCのパラレル端子に接続し、ミニDIN はマウスまたはキーボード端子に接続します。**'パラレルケーブル4'**のIDC ヘッダをIF-AN24Xカードの**'J3'**（14 ピン）コネクタに接続します。ケーブルの赤い線がピン1 側にくるようにします。
3. X-48MK II の電源を入れます。
4. PC上でiMPACTを起動します。
   [スタートメニュー -> プログラム -> Xilinx ISE 7.1i -> アクセサリ -> iMPACT]

   今回が初めての場合は、ポップアップウインドウから**'Create new project'**を選択します。次回からは**'load most recent project'**を選択します。
5. **'Operation Mode Selection'** 画面が表示されます。**'Configure Devices'**を選択し、**'Next'**をクリックします。



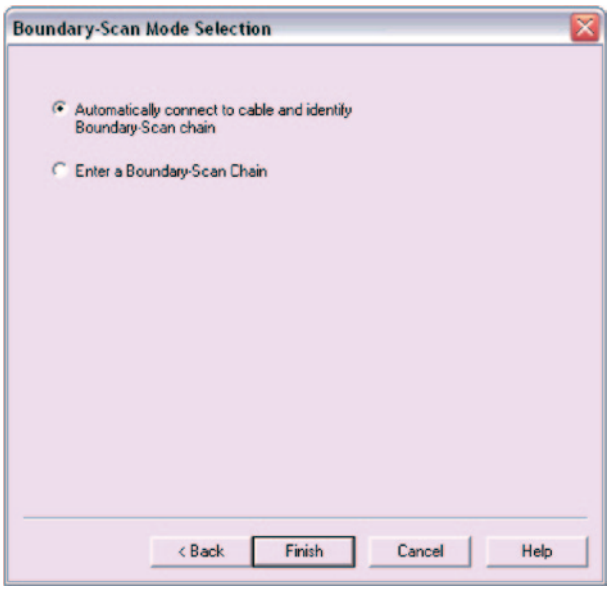
6. The **'Configure Devices'** window will pop up.
Select **'Boundary-Scan Mode'** and click **'Next'**.

6. **'Configure Devices'** 画面が表示されます。
'Boundary-Scan Mode'を選択し、**'Next'**をクリックします。



7. The **'Boundary-Scan Mode Selection'** window will pop up.
Select **'Automatically connect to cable and identify Boundary-Scan chain'** and click **'Finish'**.

7. **'Boundary-Scan Mode Selection'** 画面が表示されます。
'Automatically connect to cable and identify Boundary-Scan chain'を選択し、**'Finish'**をクリックします。

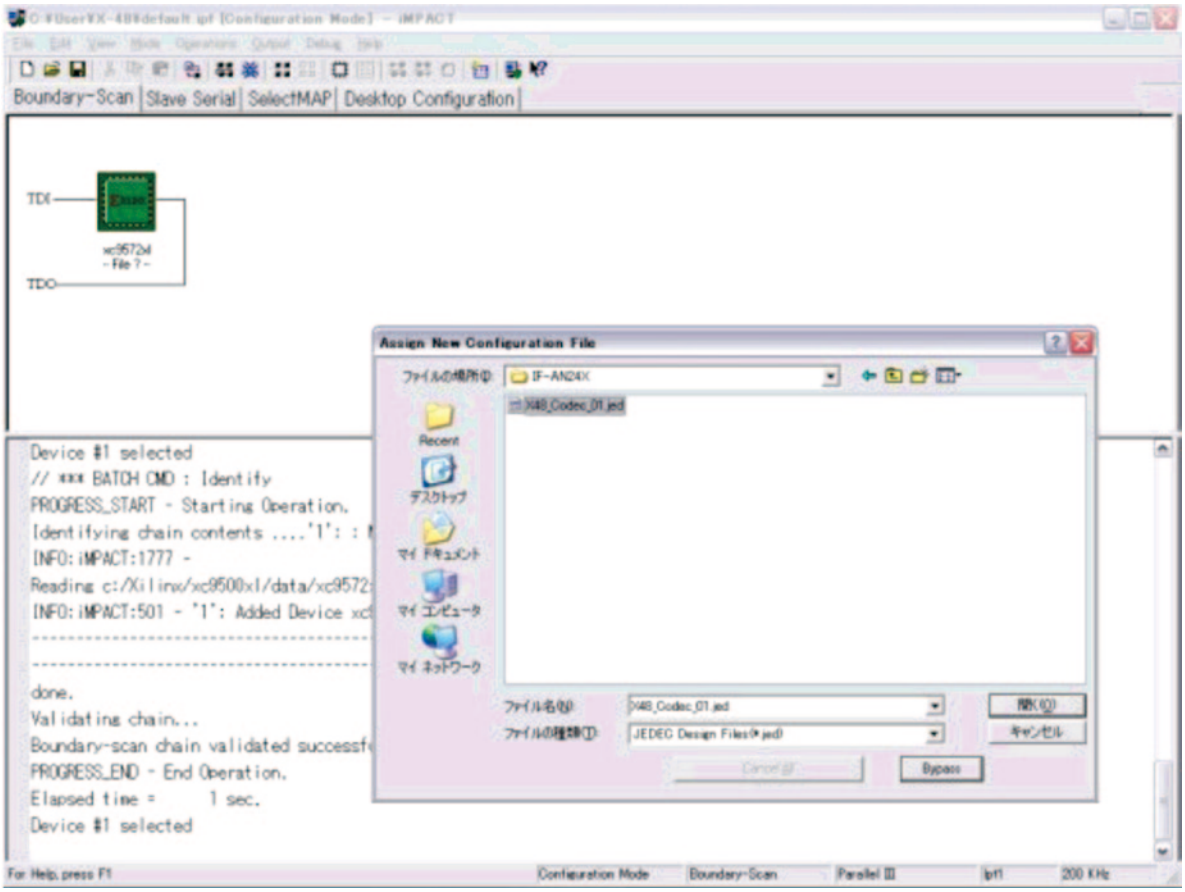


8. Click **'OK'** after the Boundary-Scan mode detects a device.

8. Boundary-Scan モードでデバイスが検知されたら、**'OK'**をクリックします。

9. A window will pop up called **'Assign New Configuration File'**.
Note : If this window does not pop up, right click on the device and select **'Assign New Configuration File'**.

9. **'Assign New Configuration File'** 画面が表示されます。
注 : この画面が表示されない場合は、デバイスを右クリックして **'Assign New Configuration File'** を選択してください。



10. Browse to the proper file and click **'Open'**.
(listed in table 1 below).

Ref	Device	File Name
U2	XC9572XL-10VQ44C	X48_AN24_CPLD_4.jed

Table 1 : Xilinx programming information

11. Once the device have the appropriate file assigned, right click on the first device (U2) and select **'Program...'**
Make sure the following items are checked (all others are unchecked) :

- Erase Before Programming
- Verify

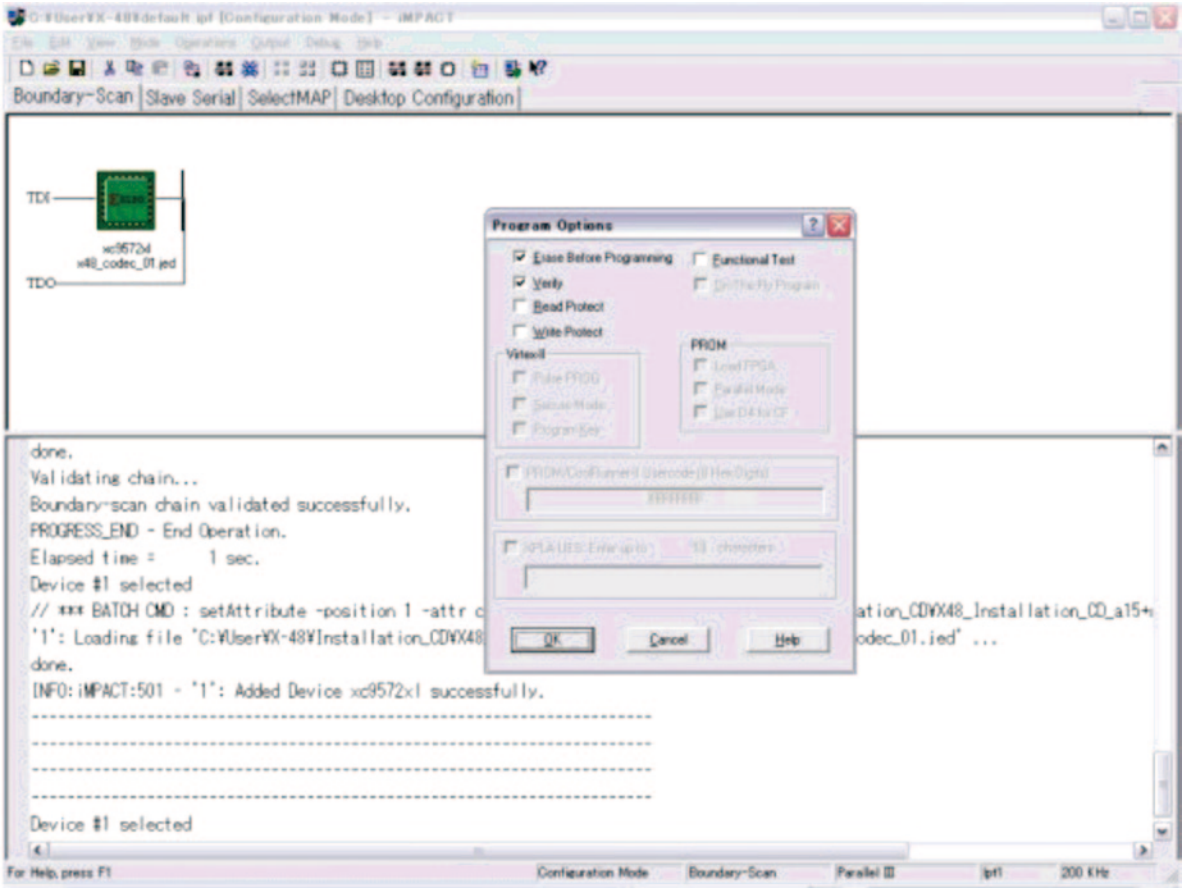
10. 適切なファイル（以下の表1 参照）を選択し、**'Open'** をクリックします。

部番	デバイス	ファイル名
U2	XC9572XL-10VQ44C	X48_AN24_CPLD_4.jed

Table 1: Xilinx プログラミングデータ

11. デバイスに適切なファイルを指定したら、デバイス（U2）を右クリックし、**'Program...'** を選択します。
以下の項目にチェックが入っているか確認します。
（他の項目はすべて、チェックを外します。）

- Erase Before Programming
- Verify



12. Click **'OK'** to start programming.
Verify that programming succeeded.

13. Close iMPACT.
Recycling power is needed to have the new CPLD code be available.

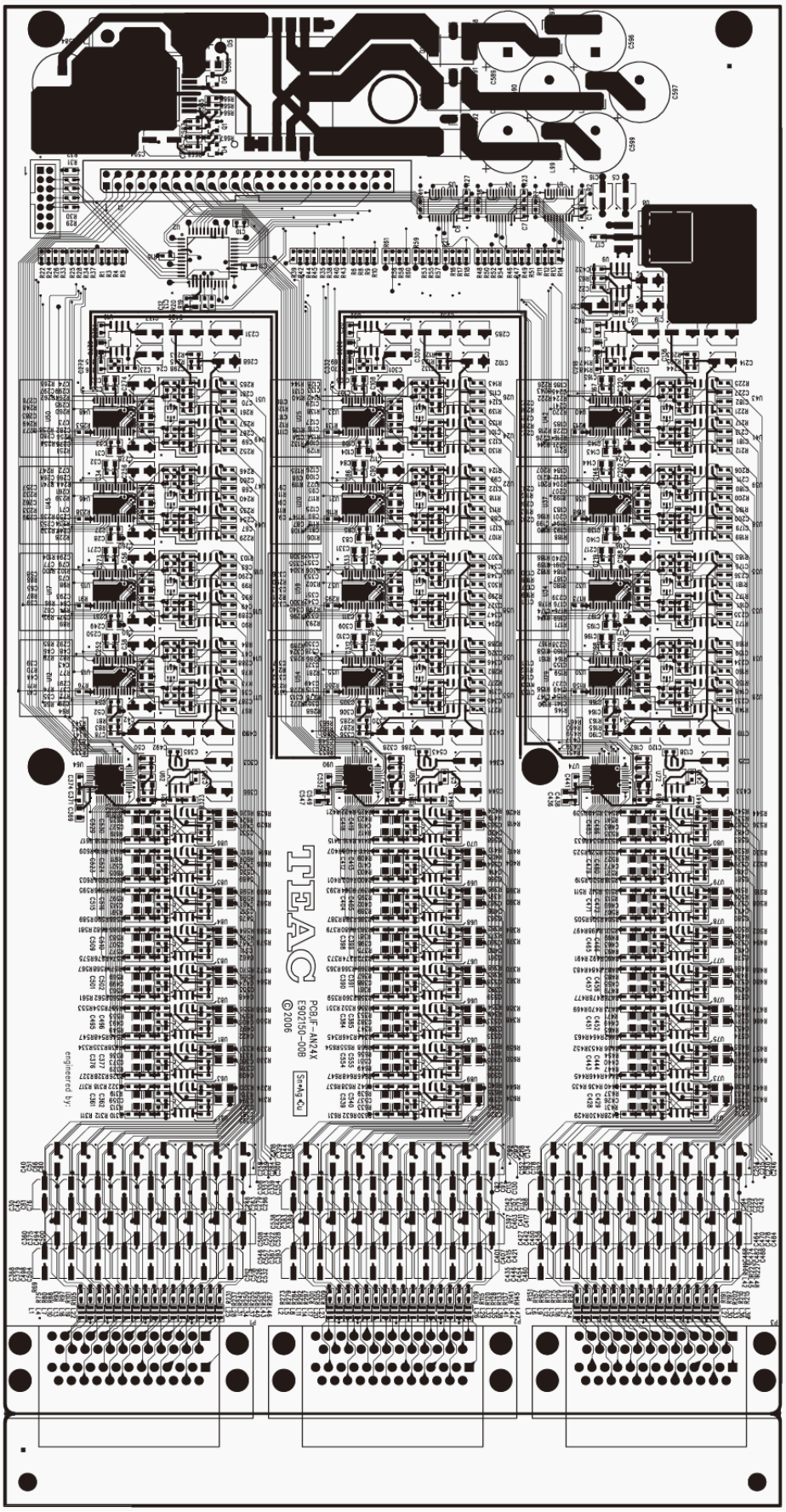
12. **'OK'** をクリックしてプログラミングを開始します。
プログラミングが問題なく完了したかを確認してください。

13. iMPACT を終了します。
新しいCPLDコードを使用するには、電源をオフ->オンしてください。

PC Boards and Parts List (基板図とパーツリスト)

For service use, this PCB assembly have to be delivered with all firmware and jumper headers installed.

サービスで使用する場合は、この基板はすべてのファームウェアーのインストールとジャンパーヘッダーの取り付けが完了している事が必要です。



IF-AN24X

REF.NO.	PARTS NO.	DESCRIPTION .	KCR PARTS NO
	E95215000B	PCB ASSY,IF-AN24X	
	E90215000B	PCB, IF-AN24X	8005005698
C584, 589-599	9A10525900	CE. 2200UF 16V REA222M1CSA	7000032501
J1	9A10519700	CONNECTOR.50P GBH1-503	8004500103
J3	9A10519800	CONNECTOR.14P GBH2-142	8004140405
J4	9A10521200	CONNECTOR.4P GAX-B-508	8004041516
P1-3	9A10521700	CONNECTOR.D-SUB 50P 2PCS	8004500114
			8004500147
T1	9A10526000	TRANS, KRM-095025 KCR	9221600814
U13-57	9A10526100	IC, AK5385AVFP	7003300620
U64, 74, 90	9A10526200	IC, AK4358VQP	7003300631
	M02136000C	BRACKET, IF-AN24X	9216900221
PACKING	M02512200A	CORR CDBD, SHEET IF-AN24X	6000106096
PACKING	3M0121800A	CONDUCT POLY BAG	6030100464
PACKING	M02167200B	CORR CDBD CS, IF-AN24X	6000006808
PACKING	9A10526300	CORR CDBD CS, OUTER IF-AN24X	6000006897
ACC	9A10526400	HARNESS ASSY, 50P SLOT CARD	9215900145
ACC	9A10526500	POLTHN BAG, 170*260	6030000185

12. IF-AE24X

IF-AE24X

Programming the CPLD on IF-AE24X

Tools :

A dedicated test PC, Xilinx parallel cable IV and ISE7.1(or later) are necessary as well as the X-48MK II .

Programming Xilinx Chips :

1. Install IF-AE24X board to X-48MK II and connect the 50pin cable.
2. Plug the **'Xilinx Parallel Cable IV'** into the dedicated test PC's parallel port. Plug the mini-din into the mouse or keyboard port as well. Connect the IDC header of the **'parallel cable 4'** to **'J1'**(14pin) connector on the IF-AE24X board. The red stripe on the cable should line up with pin 1.
3. Power on the X-48MK II .
4. On the PC, run iMPACT
   [Start menu -> Program -> Xilinx ISE 7.1i -> Accessary -> iMPACT]

   On a pop-up window, select **'Create new project'** if this is the first time. From the second time, select **'load most recent project'**.
5. The **'Operation Mode Selection'** window will pop up. Select **'Configure Devices'** and click **'Next'**

IF-AE24XのCPLDのプログラミング

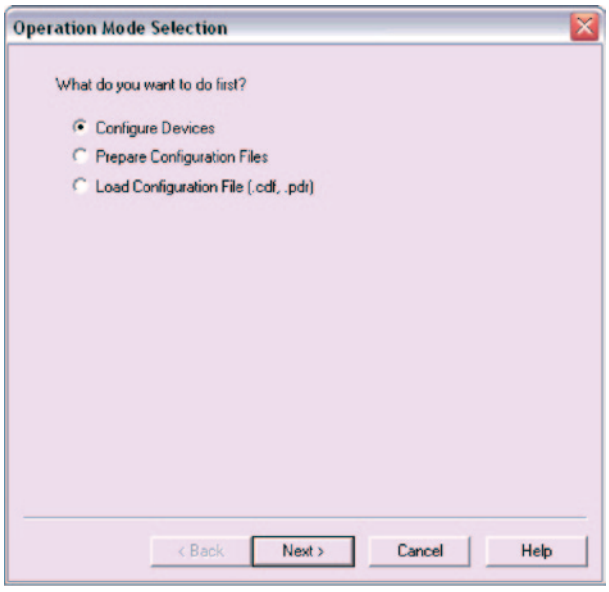
ツール :

X-48MK II 本体の時と同じ様に、試験用PC、Xilinxパラレルケーブル IV、ISE7.1（またはそれ以降）が必要です。

Xilinx チップのプログラミング :

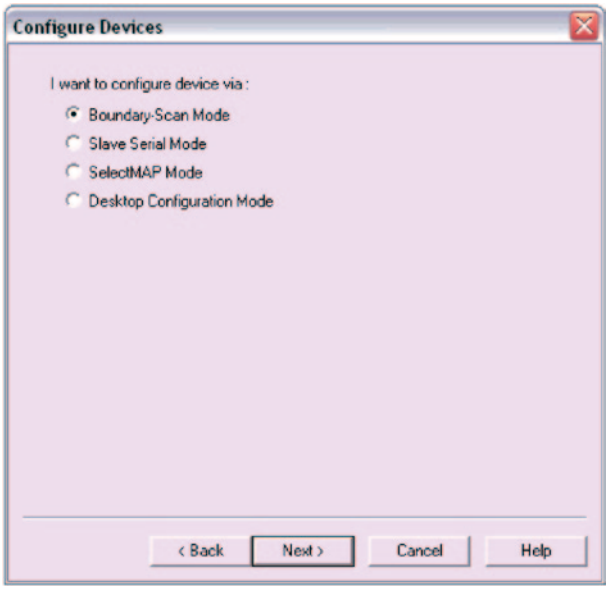
1. IF-AE24XカードをX-48MK II に取り付け、電源コードと50ピンケーブルを接続します。
2. **'Xilinx Parallel Cable（パラレルケーブル）IV'**を試験用PCのパラレル端子に接続し、ミニDIN はマウスまたはキーボード端子に接続します。**'パラレルケーブル4'**のIDC ヘッダをIF-AE24Xカードの**'J1'**（14 ピン）コネクタに接続します。ケーブルの赤い線がピン1 側にくるようにします。
3. X-48MK II の電源を入れます。
4. PC上でiMPACTを起動します。
   [スタートメニュー -> プログラム -> Xilinx ISE 7.1i -> アクセサリ -> iMPACT]

   今回が初めての場合は、ポップアップウインドウから**'Create new project'**を選択します。次回からは**'load most recent project'**を選択します。
5. **'Operation Mode Selection'** 画面が表示されます。**'Configure Devices'**を選択し、**'Next'**をクリックします。



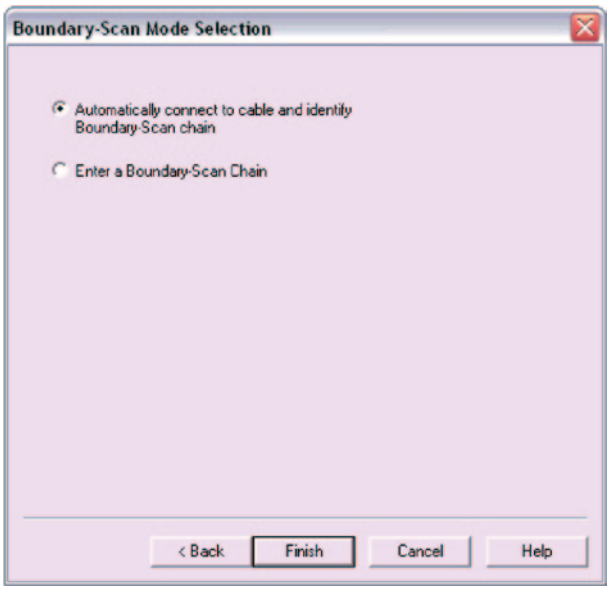
6. The **'Configure Devices'** window will pop up.
Select **'Boundary-Scan Mode'** and click **'Next'**.

6. **'Configure Devices'** 画面が表示されます。
'Boundary-Scan Mode'を選択し、**'Next'**をクリックします。



7. The **'Boundary-Scan Mode Selection'** window will pop up.
Select **'Automatically connect to cable and identify Boundary-Scan chain'** and click **'Finish'**.

7. **'Boundary-Scan Mode Selection'** 画面が表示されます。
'Automatically connect to cable and identify Boundary-Scan chain'を選択し、**'Finish'**をクリックします。



8. Click **'OK'** after the Boundary-Scan mode detects a device.

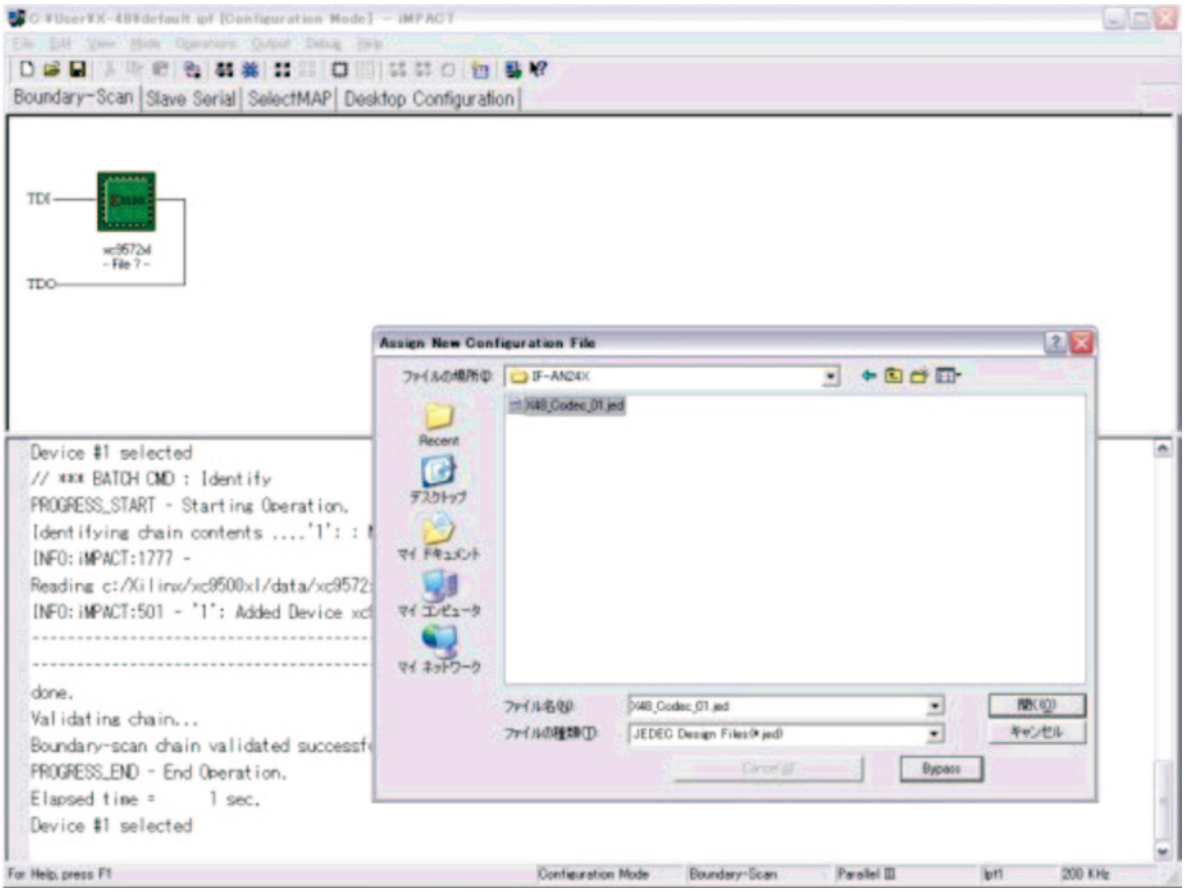
8. Boundary-Scan モードでデバイスが検知されたら、**'OK'**をクリックします。

9. A window will pop up called **'Assign New Configuration File'**

Note : If this window does not pop up, right click on the device and select **'Assign New Configuration File'**

9. **'Assign New Configuration File'** 画面が表示されます。

注 : この画面が表示されない場合は、デバイスを右クリックして **'Assign New Configuration File'** を選択してください。



10. Browse to the proper file and click **'Open'**. **(listed in table 1 below).**

Ref	Device	File Name
U2	XC9572XL-10TQG100C	AES_EBU.jed

Table 1 : Xilinx programming information

10. 適切なファイル（以下の表1 参照）を選択し、**'Open'** をクリックします。

部番	デバイス	ファイル名
U2	XC9572XL-10TQG100C	AES_EBU.jed

Table 1: Xilinx プログラミングデータ

11. Once the device have the appropriate file assigned, right click on the first device (U2) and select **'Program...'**

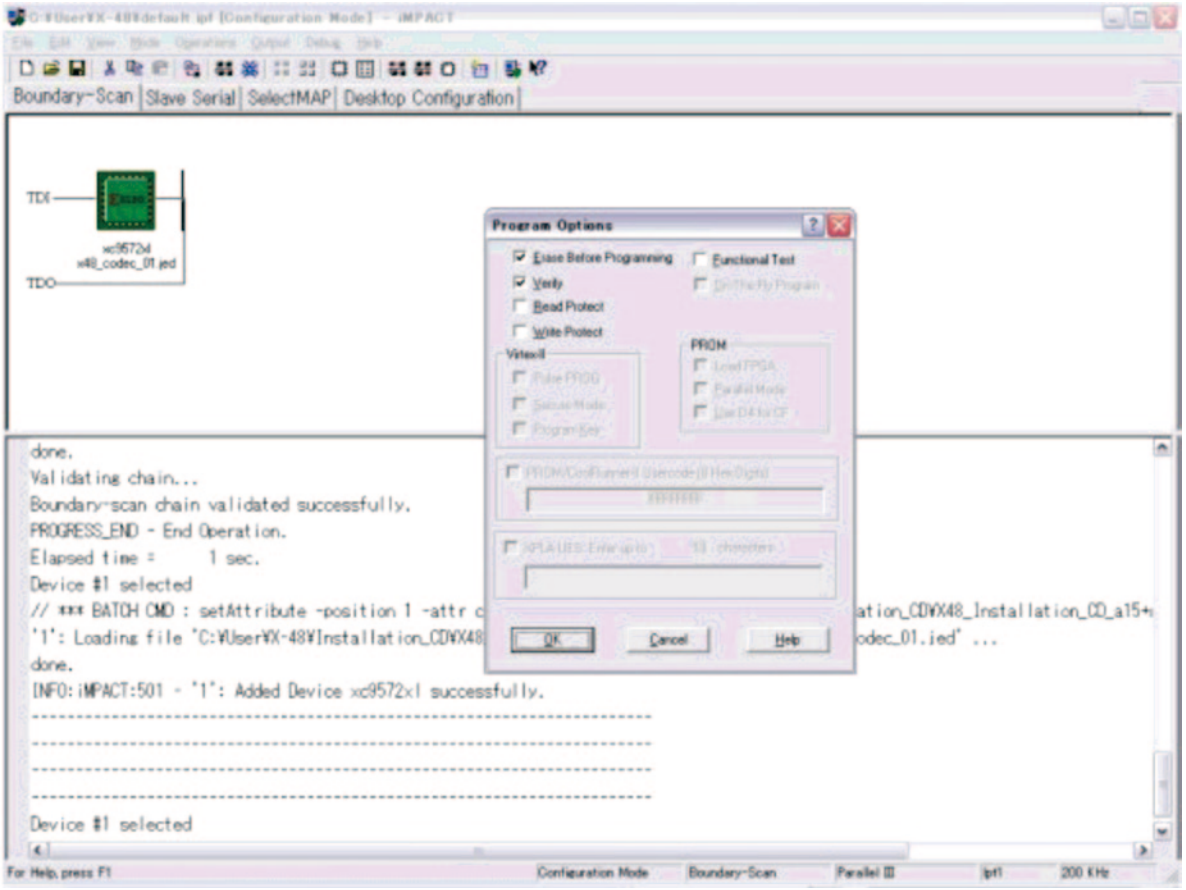
Make sure the following items are checked (all others are unchecked) :

- Erase Before Programming
- Verify

11. デバイスに適切なファイルを指定したら、デバイス（U2）を右クリックし、**'Program...'** を選択します。

以下の項目にチェックが入っているか確認します。（他の項目はすべて、チェックを外します。）

- Erase Before Programming
- Verify



12. Click **'OK'** to start programming.
Verify that programming succeeded.

13. Close iMPACT.
Recycling power is needed to have the new CPLD code be available.

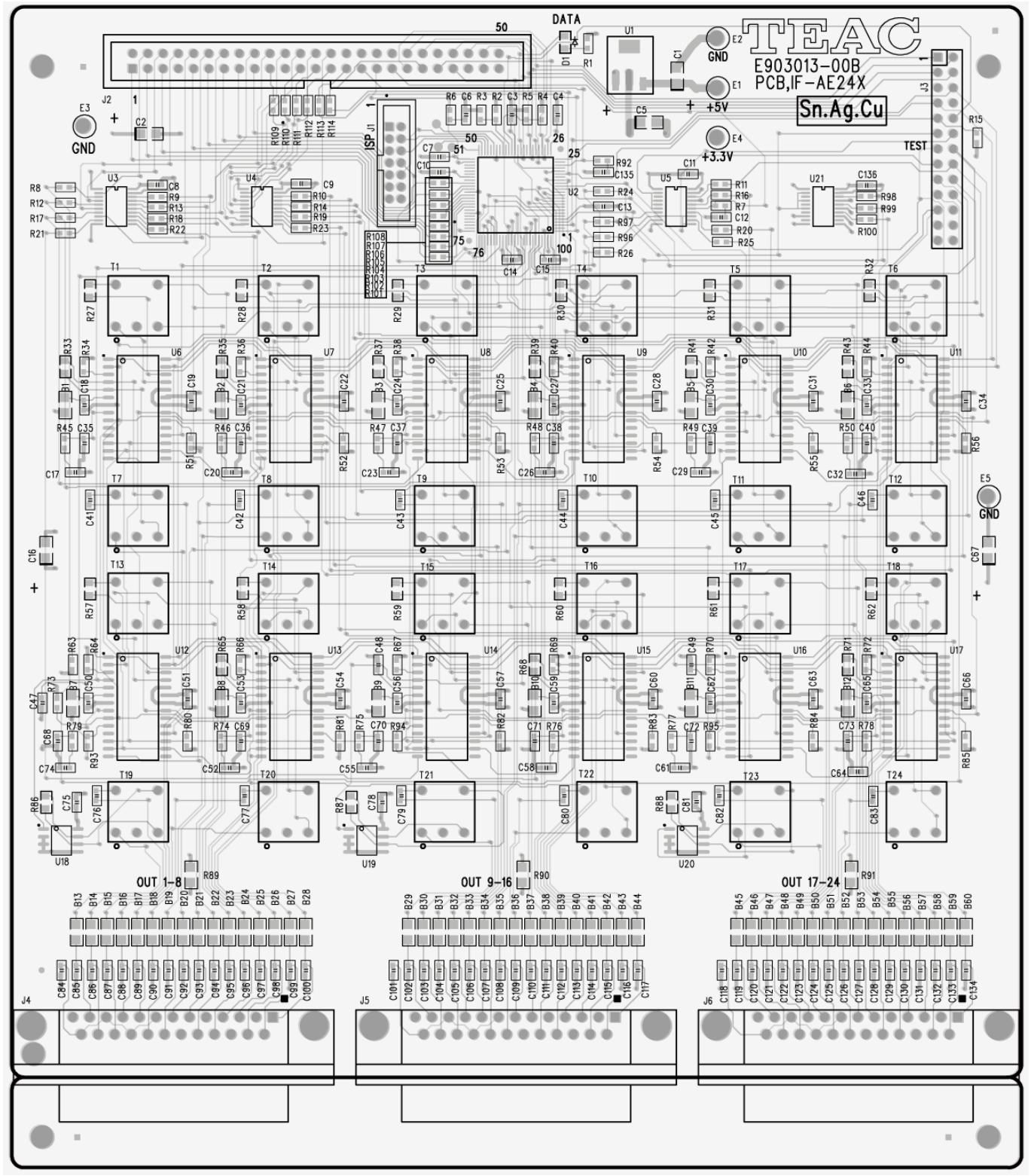
12. **'OK'** をクリックしてプログラミングを開始します。
プログラミングが問題なく完了したかを確認してください。

13. iMPACT を終了します。
新しいCPLDコードを使用するには、電源をオフ->オンしてください。

PC Boards and Parts List (基板図とパーツリスト)

For service use, this PCB assembly have to be delivered with all firmware and jumper headers installed.

サービスで使用する場合は、この基板はすべてのファームウェアーのインストールとジャンパーヘッダーの取り付けが完了している事が必要です。



IF-AE24X

REF.NO.	PARTS NO.	DESCRIPTION .	KCR PARTS NO
	E90301300A	PCB, IF-AE24X	8005006000
J1	9A10519800	CONNECTOR. 14P GBH2-142	8004140405
J2	9A10519700	CONNECTOR. 50P GBH1-503	8004500103
J4. 5. 6	9A10526600	CONNECTOR, D-SUB 50P	8004250153
T1-24	3E026430G	TRANS, PULSE400UH GZ0	7008030956
U6-17	9A10526700	IC, CS8420-CSZRZ	7003320617
60350-C	M02586900C	BRACKET, IF-AE24X	9216504392
PCB	9A10526800	FOOT, RUBBER PCB	5131300221
PACKING	3M0121800A	CONDUCT POLY BAG	6030100464
PACKING	9A10526900	CORR CDBD CS,INR IF-AE24X	6000007287
PACKING	9A10527000	CORR CDBD CS,OTR IF-AE24X	6000007298
ACC	9A10527100	SCREW, BPB 3*8 FZB	4300220495
ACC	9A10525100	POLTHN BAG, 80*90	6030000685
ACC	9A10526400	HARNESS ASSY, 50P SLOT CARD	9215900145
ACC	9A10526500	POLTHN BAG, 170*260	6030000185

13. IF-AD24X

IF-AD24X

Programming the CPLD on IF-AD24X

Tools :

A dedicated test PC, Xilinx parallel cable IV and ISE7.1(or later) are necessary as well as the X-48MK II .

Programming Xilinx Chips :

1. Install IF-AD24X board to X-48MK II and connect the 50pin cable.
2. Plug the **'Xilinx Parallel Cable IV'** into the dedicated test PC's parallel port. Plug the mini-din into the mouse or keyboard port as well. Connect the IDC header of the **'parallel cable 4'** to **'J2'**(14pin) connector on the IF-AD24X board. The red stripe on the cable should line up with pin 1.
3. Power on the X-48MK II .
4. On the PC, run iMPACT
   [Start menu -> Program -> Xilinx ISE 7.1i -> Accessary -> iMPACT]

   On a pop-up window, select **'Create new project'** if this is the first time. From the second time, select **'load most recent project'**.
5. The **'Operation Mode Selection'** window will pop up. Select **'Configure Devices'** and click **'Next'**.

IF-AD24XのCPLDのプログラミング

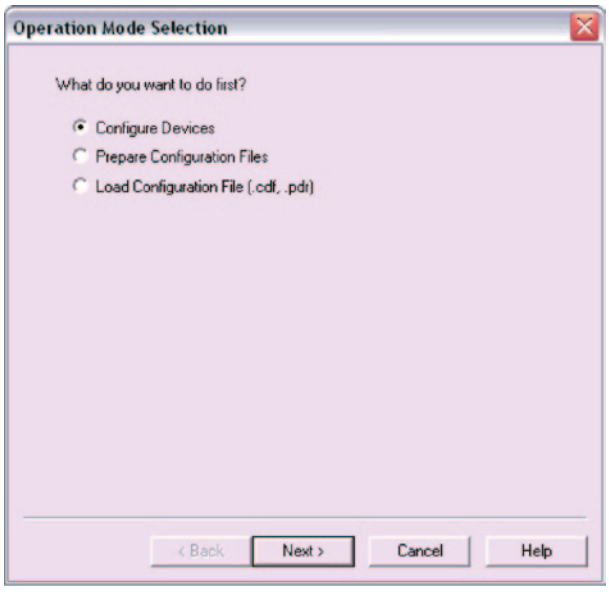
ツール :

X-48MK II 本体の時と同じ様に、試験用PC、Xilinxパラレルケーブル IV、ISE7.1（またはそれ以降）が必要です。

Xilinx チップのプログラミング :

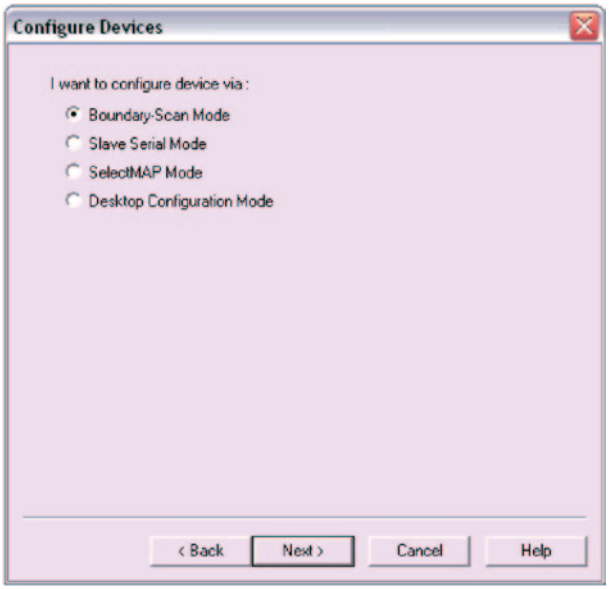
1. IF-AD24XカードをX-48MK II に取り付け、電源コードと50ピンケーブルを接続します。
2. **'Xilinx Parallel Cable（パラレルケーブル）IV'**を試験用PCのパラレル端子に接続し、ミニDIN はマウスまたはキーボード端子に接続します。**'パラレルケーブル4'**のIDC ヘッダをIF-AD24Xカードの**'J2'**（14 ピン）コネクタに接続します。ケーブルの赤い線がピン1 側にくるようにします。
3. X-48MK II の電源を入れます。
4. PC上でiMPACTを起動します。
   [スタートメニュー -> プログラム -> Xilinx ISE 7.1i -> アクセサリ -> iMPACT]

   今回が初めての場合は、ポップアップウインドウから**'Create new project'**を選択します。次回からは**'load most recent project'**を選択します。
5. **'Operation Mode Selection'** 画面が表示されます。**'Configure Devices'**を選択し、**'Next'**をクリックします。



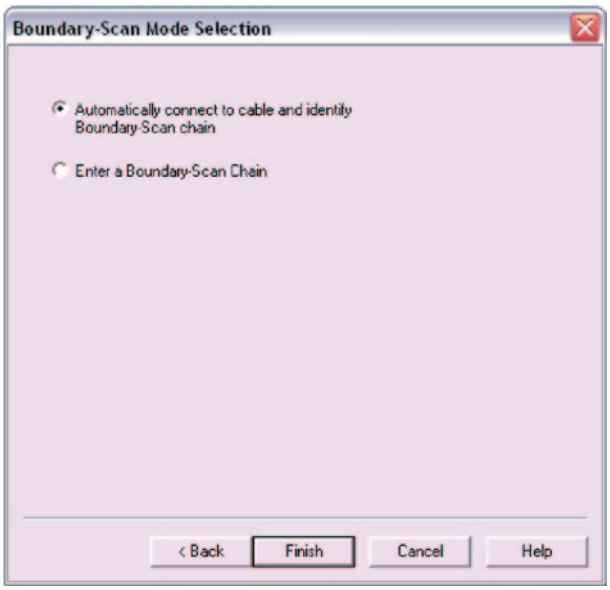
6. The **'Configure Devices'** window will pop up.
Select **'Boundary-Scan Mode'** and click **'Next'**.

6. **'Configure Devices'** 画面が表示されます。
'Boundary-Scan Mode'を選択し、**'Next'**をクリックします。



7. The **'Boundary-Scan Mode Selection'** window will pop up.
Select **'Automatically connect to cable and identify Boundary-Scan chain'** and click **'Finish'**.

7. **'Boundary-Scan Mode Selection'** 画面が表示されます。
'Automatically connect to cable and identify Boundary-Scan chain'を選択し、**'Finish'**をクリックします。

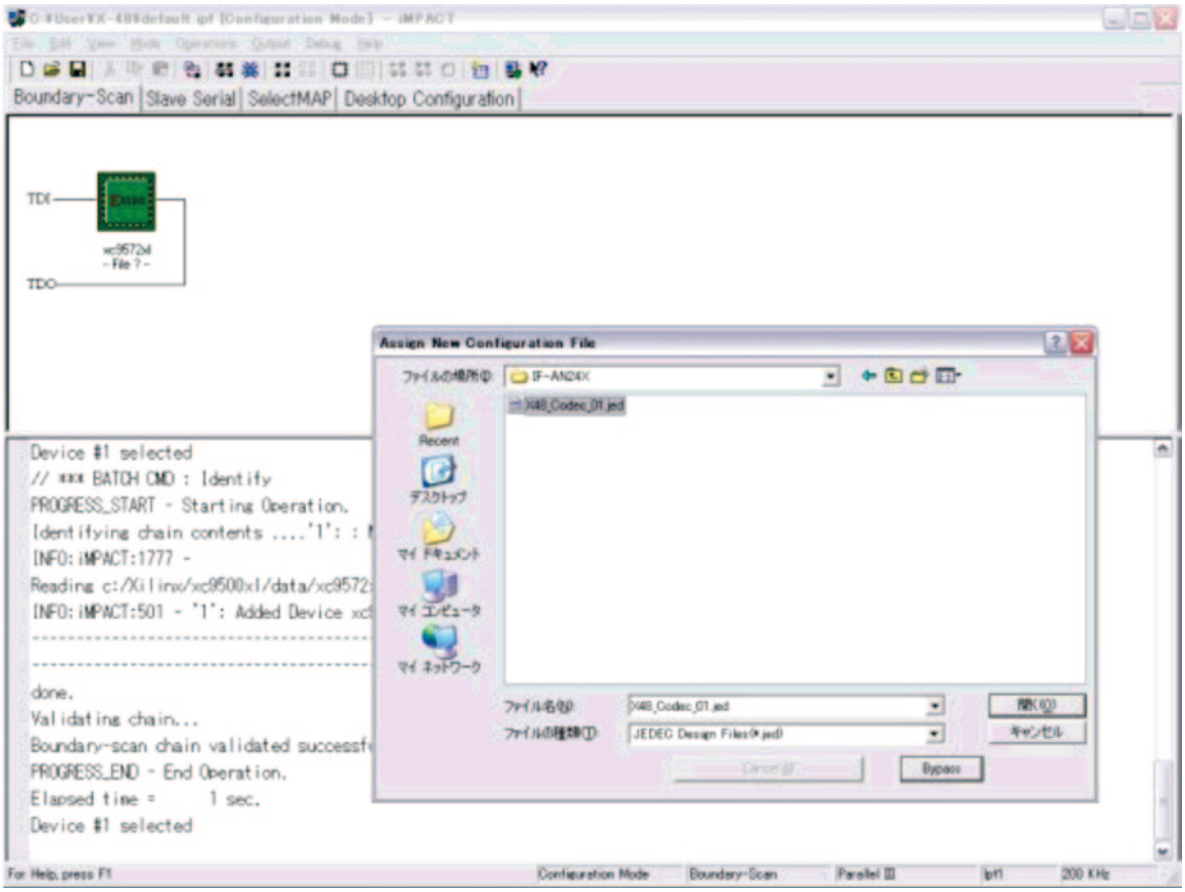


8. Click **'OK'** after the Boundary-Scan mode detects a device.

8. Boundary-Scan モードでデバイスが検知されたら、**'OK'**をクリックします。

9. A window will pop up called **'Assign New Configuration File'**.
Note : If this window does not pop up, right click on the device and select **'Assign New Configuration File'**.

9. **'Assign New Configuration File'** 画面が表示されます。
注 : この画面が表示されない場合は、デバイスを右クリックして **'Assign New Configuration File'** を選択してください。



10. Browse to the proper file and click **'Open'**.
(listed in table 1 below).

Ref	Device	File Name
U1	XC9572-15TQG100C	Topadatv3.jed

Table 1 : Xilinx programming information

10. 適切なファイル（以下の表1 参照）を選択し、**'Open'** をクリックします。

部番	デバイス	ファイル名
U1	XC9572-15TQG100C	Topadatv3.jed

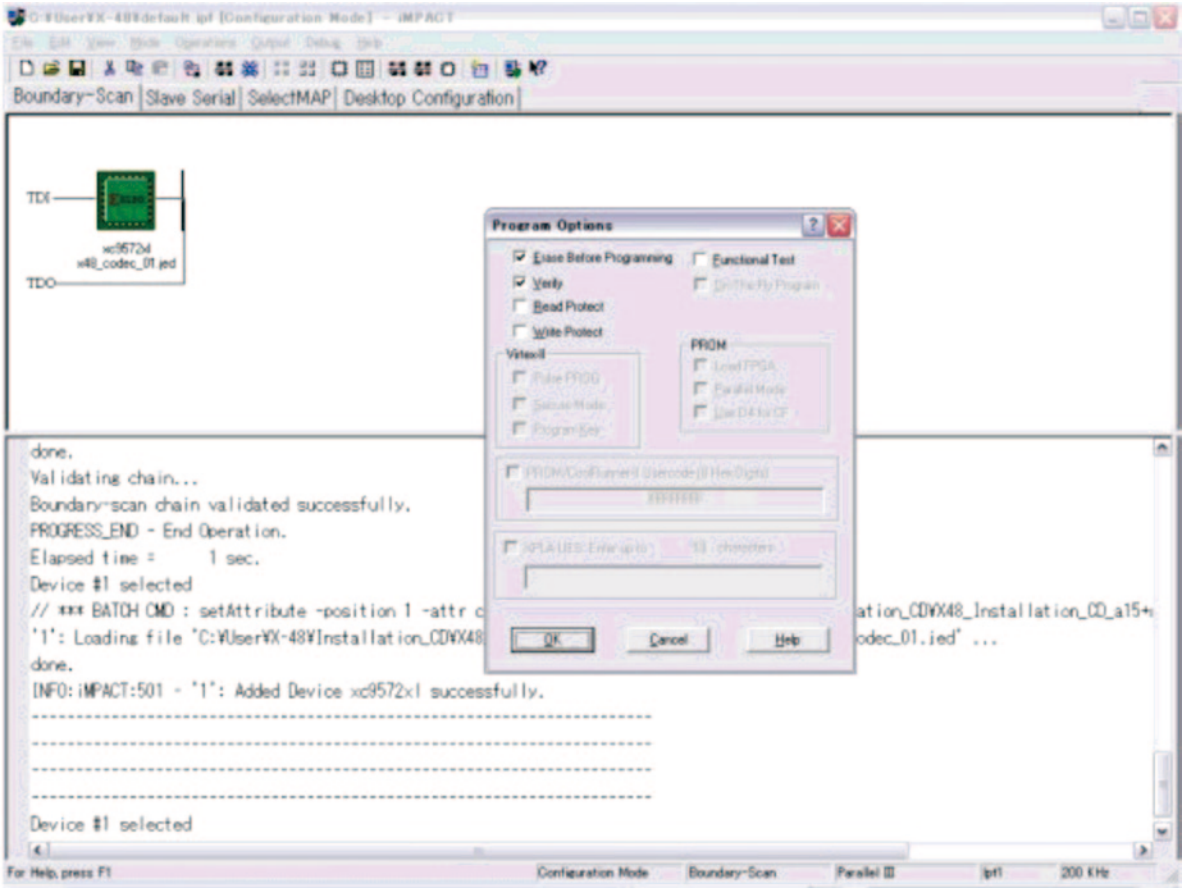
Table 1: Xilinx プログラミングデータ

11. Once the device have the appropriate file assigned, right click on the first device (U1) and select **'Program...'**
Make sure the following items are checked (all others are unchecked) :

- Erase Before Programming
- Verify

11. デバイスに適切なファイルを指定したら、デバイス（U1）を右クリックし、**'Program...'** を選択します。
以下の項目にチェックが入っているか確認します。
（他の項目はすべて、チェックを外します。）

- Erase Before Programming
- Verify



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PC Boards and Parts List (基板図とパーツリスト)

For service use, this PCB assembly have to be delivered with all firmware and jumper headers installed.

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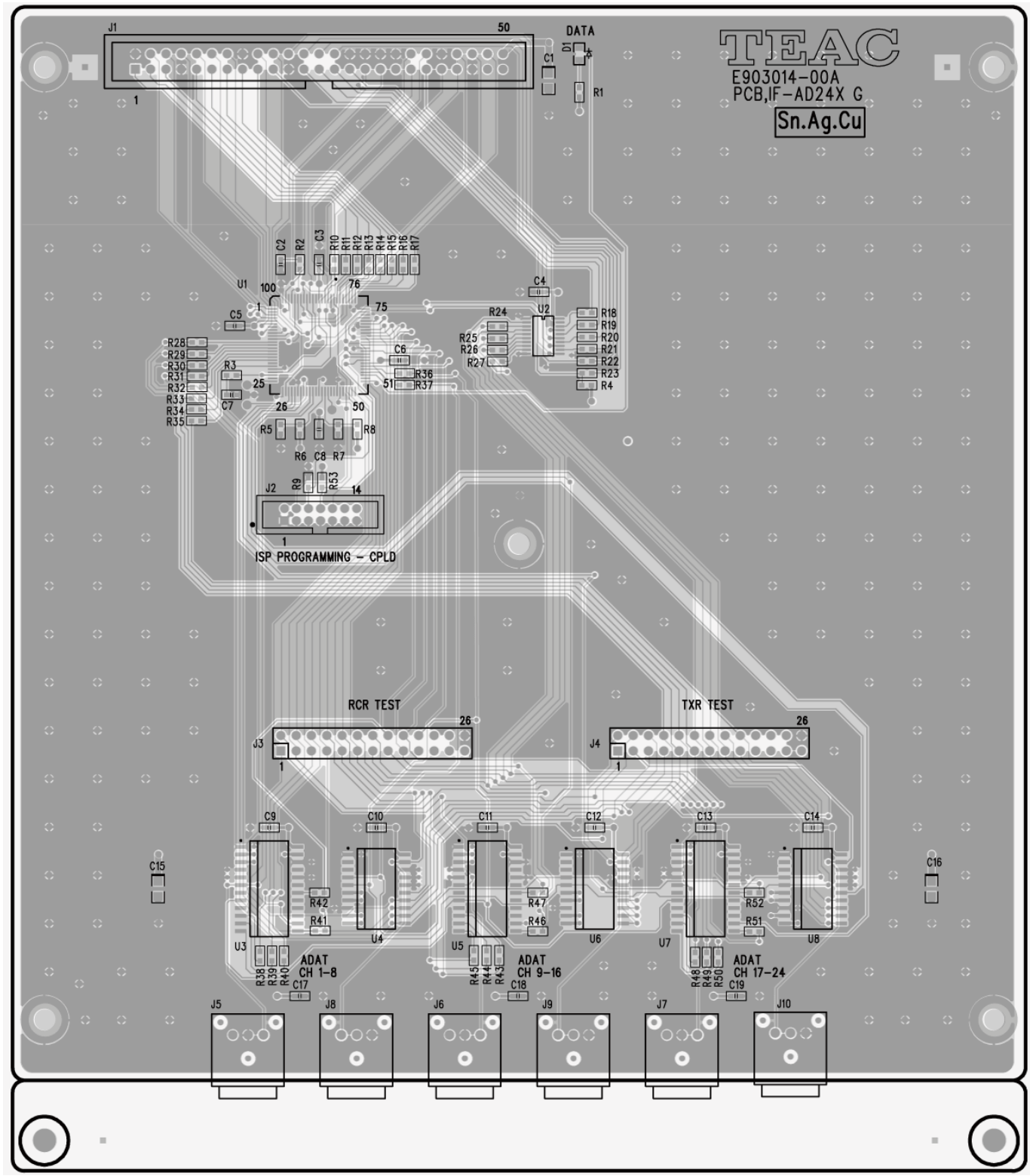

IF-AD24X

REF.NO.	PARTS NO.	DESCRIPTION .	KCR PARTS NO
	E95301400A	PCB ASSY, IF-AD24X	
	E90301400A	PCB, IF-AD24X	8005005994
J1	9A10519700	CONNECTOR. 50P GBH1-503	8004500103
J2	9A10519800	CONNECTOR. 14P GBH2-142	8004140405
J5, 6, 7	9A10527200	OPT CONN, GP1FAV50RK0F	8004061241
J8, 9, 10	9A10527300	OPT CONN, GP1FAV50TK0F	8004061252
U3, 5, 7	9A10527400	IC, AL1402GT	7003300722
U4, 6, 8	9A10527500	IC, AL1401AGT	7003300733
	M02587000C	BRACKET	9216504529
PACKING	3M0121800A	CONDUCT POLY BAG	6030100464
PACKING	9A10526900	CORR CDBD CS, INR IF-AE24X	6000007287
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ACC	9A10527100	SCREW, BPB 3*8 FZB	4300220495
ACC	9A10525100	POLTHN BAG, 80*90	6030000685
ACC	9A10526400	HARNESS ASSY, 50P SLOT CARD	9215900145
ACC	9A10526500	POLTHN BAG, 170*260	6030000185

Updates

Always use the most recent firmware for this unit.

Please visit the TASCAM website (http://tascam.com/) to check for the latest firmware.

Important precautions (MUST READ)

Recommendations related to external hard disk drives

Only use external hard disk drives with rotation speeds of at least 7200 rpm and built-in caches of at least 8 MB. Hard drives with specifications lower than this might not be able to transmit data for 48 tracks.

In addition, we strongly recommend that you check external drives daily using the "Drive Benchmarking" command in the "File" menu.

Maintaining hard disk drives in good condition

Since large amounts of data for 48 tracks are read from and written to the hard drive by the X-48MKII, it is important to maintain a sufficient data transmission rate by always keeping the hard drive in good condition. This is especially important when using double sampling rates of 88.2 kHz and 96 kHz with an external hard drive.

In order to prevent errors from occurring due to insufficient data transmission rates, please do the following whenever necessary.

- If more than 3 projects have been created on the same partition of a hard drive, before creating another new project on that partition, back up all the existing projects on that partition. Then, delete them and format the partition.
- Before beginning any long recording, format the hard drive and create a new project.

Maintenance items

V2.02 fix

Importing and exporting 32-bit floating-point audio files was not possible. This has been fixed.

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Maintenance items

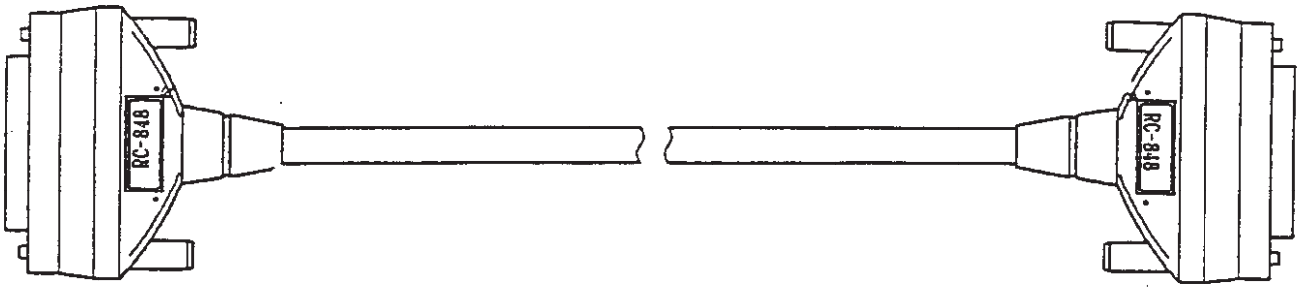
V2.03 fix

During recording and in recording standby when sending or receiving an AES signal using an IF-AE24X, if the IF-AE24X had an unconnected terminal, the meters for the tracks corresponding to that open terminal would move and noise would occur. This has been fixed.

V2.02 fix

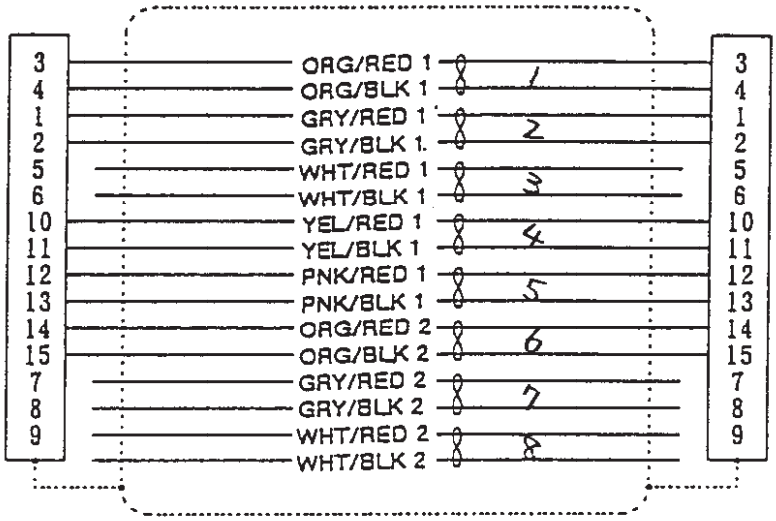
Importing and exporting 32-bit floating-point audio files was not possible. This has been fixed.

THE CABLES FOR REMOTE

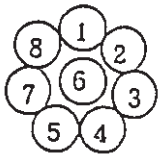


Female

Male



means Twisted wire

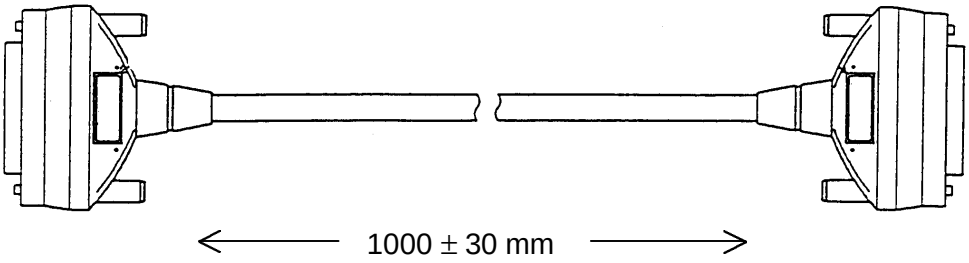


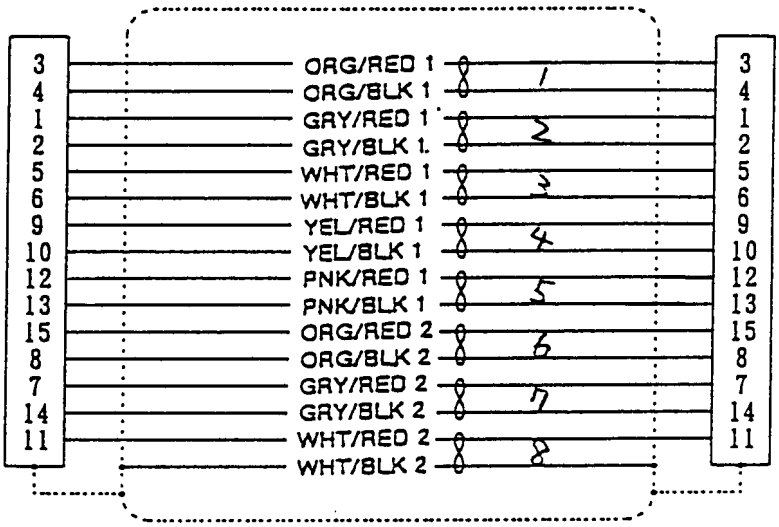
1 pce.	5336 3570-00	Connector Plug, 15 pin D-Sub (Male)
1 pce.	1315 2907-	Connector Socket, 15 pin D-Sub (Female)
2 pcs.	5336 3580-00	Case Assy, 15 pin D-Sub

Cable Assy, MMC-38

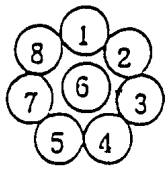
Male
DA-38 SYNC IN

Female
MMC-38 REMOTE OUT



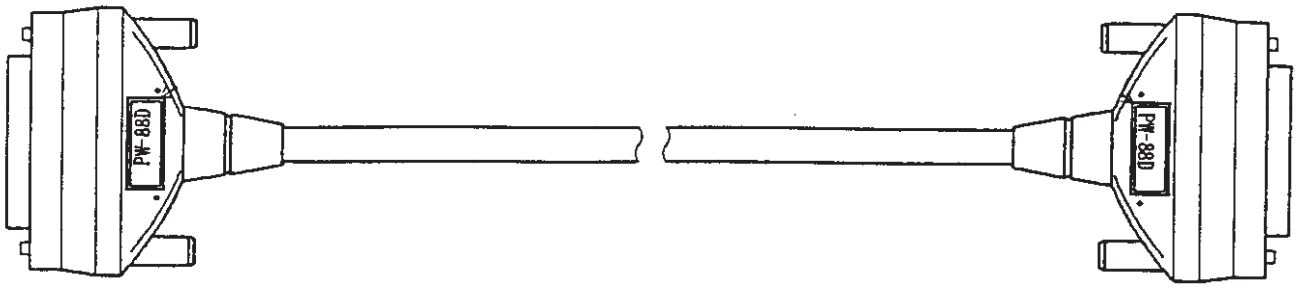


means Twisted wire

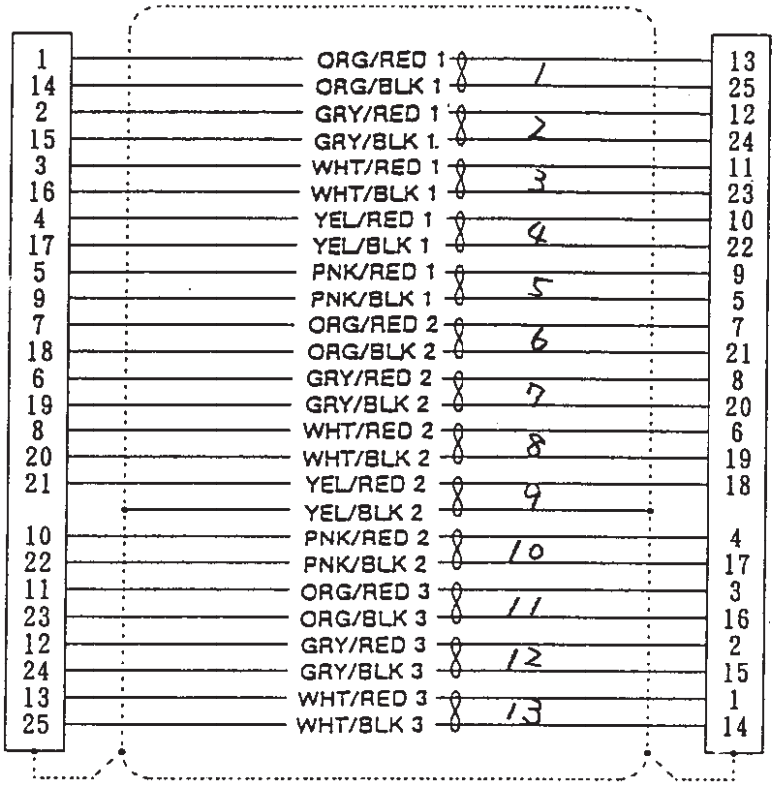


1 pce	53363570-00	Connector Plug, 15 pin D-Sub(Male)
1 pce	13152907	Connector Socket, 15 pin D-Sub(Female)
2 pcs	53363580-00	Case Assy, 15 pin D-Sub

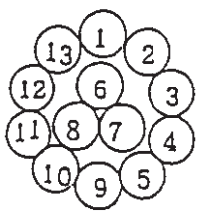
THE CABLES FOR TDIF



Male Male

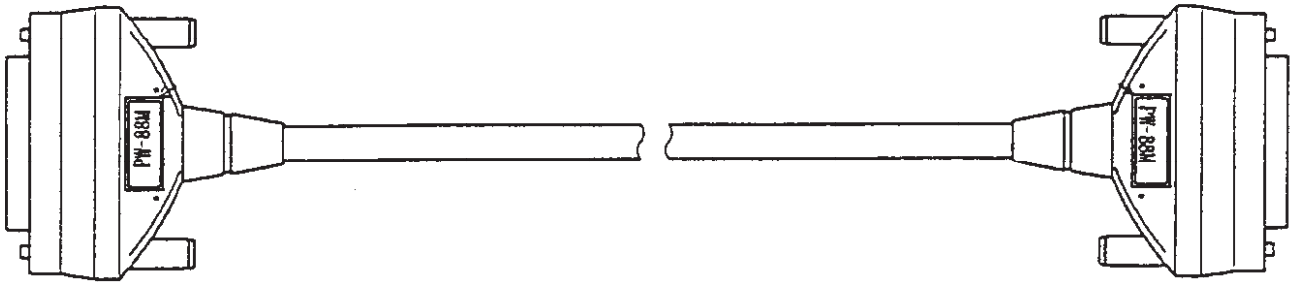


means Twisted wire

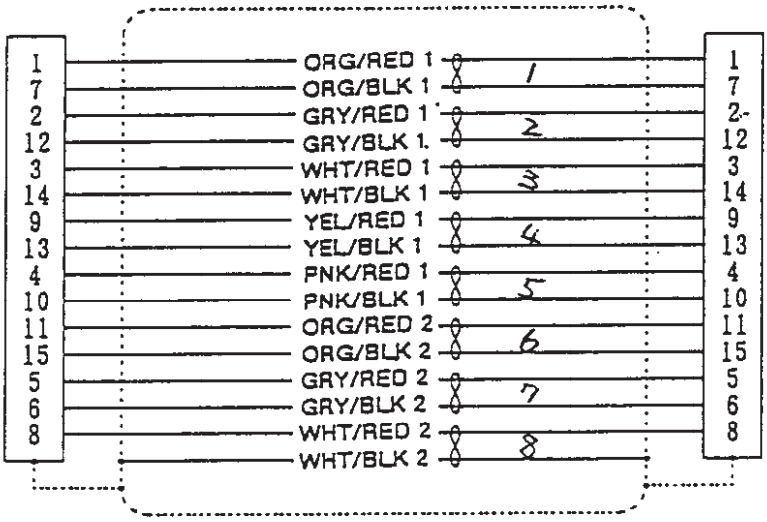


2 pcs.	1315 2908-	Connector Plug, 25 pin D-Sub (Male)
2 pcs.	5336 3581-00	Case Assy, 25 pin D-Sub

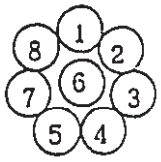
THE CABLES FOR METER



Female Male

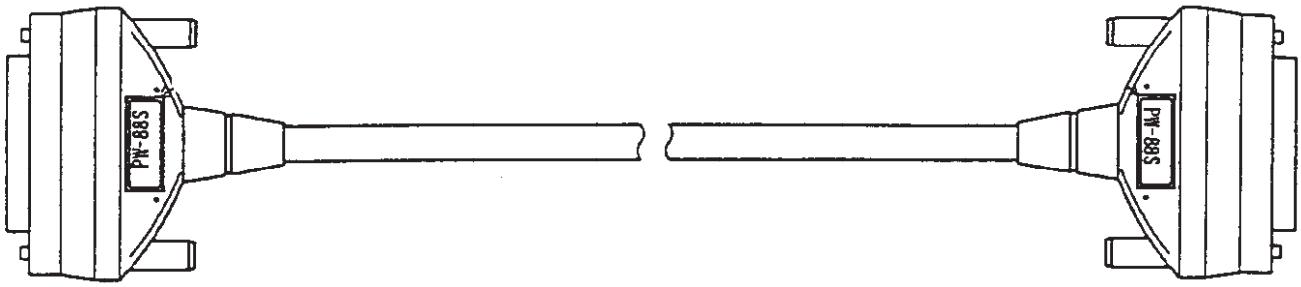


means Twisted wire

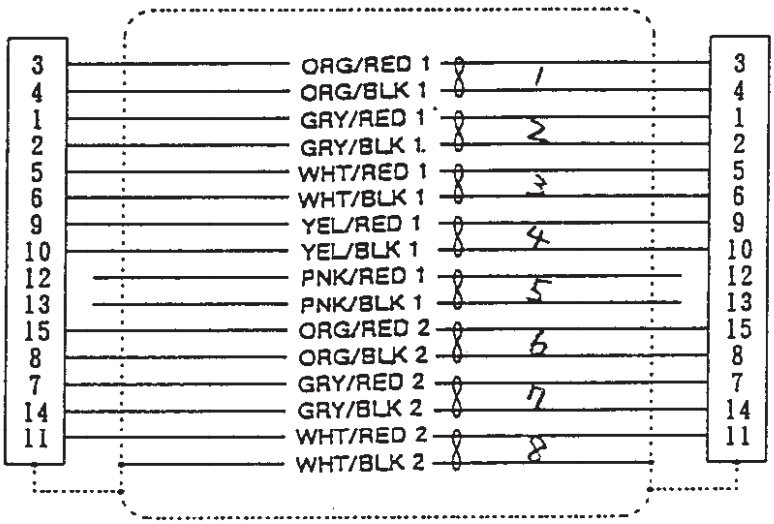


1 pce.	5336 3570-00	Connector Plug, 15 pin D-Sub (Male)
1 pce.	1315 2907-	Connector Socket, 15 pin D-Sub (Female)
2 pcs.	5336 3580-00	Case Assy, 15 pin D-Sub

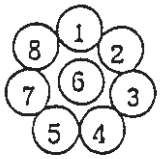
THE CABLES FOR SYNC



Male Male



means Twisted wire



2 pcs.	5336 3570-00	Connector Plug, 15 pin D-Sub (Male)
2 pcs.	5336 3580-00	Case Assy, 15 pin D-Sub

SONY NINE-PIN ATR DIALECT

HISTORY OF REVISION

hist.	date	revision	sign
1	8/26/88	P.17 x1 , P22 x1 , P35 x1	K. Nomoto
2			
3			
4			
5			
6			
7			

TO: K. Nomoto for distribution at ATP to all interested and involved parties.

FROM: T. STAROS FTL SPPC

SONY NINE-PIN ATR DIALECT

DRAFT 3.13a
(A document in process)

ALL CHANGES ARE HIGHLIGHTED IN BOLDFACE TYPE
UNRESOLVED ISSUES ARE ALSO HIGHLIGHTED IN BOLDFACE TYPE
PLEASE REVIEW CAREFULLY!

==========

THIS DOCUMENT REPRESENTS A RECONCILIATION IN REGARD TO THE ISSUES ADDRESSED IN THE PREVIOUS DIALOG WITH J. TAKAYAMA. FOLLOWING THE DISRIBUTION OF DRAFT 3.11.

Subsequently, there have been a few minor edits to improve clarity of the original intent. The only change in substance has been an addition to the text of 4x/3A, allowing IN and OUT point delays to be distinguished from each other.

BEST REGARDS

SYSTEM CONTROL COMMANDS

00/0C LOCAL DISABLE
This command disables the CONTROLLED DEVICE from all Local control actuations, with the "LOCAL" key being the sole execption.

00/0E ATTENTION DISABLE
This command disables the ability of the CONTROLLED DEVICE to issue an ATTENTION INTERUPT command. The Power On Default of the CONTROLLED DEVICE is ATTENTION DISSABLE true.

00/11 DEVICE TYPE REQUEST
This command causes a SYSTEM TALLY responce containing the apropriate 2 byte DEVICE TYPE model code.

00/1D LOCAL ENABLE
This command enables the CONTROLLED DEVICE to all Local control actuations.

00/1F ATTENTION ENABLE
This command enables the ability of the CONTROLLED DEVICE to issue an ATTENTION INTERUPT command. The Power On Default of the CONTROLLED DEVICE is ATTENTION ENABLE false.

SYSTEM TALLY HEADERS

10/01 ACK

On receipt of a command that does not request data from a CONTROLLING DEVICE the CONTROLLED DEVICE will respond with this code as an acknowlegment tally.

12/11 DEVICE TYPE

On reciept of a DEVICE TYPE REQUEST (00/11) the CONTROLLED DEVICE will respond with this tally header followed a two byte code unique to the model of the CONTROLLED DEVICE.

THESE CODES ARE ONLY PARTIALLY DEFINED AT THIS TIME

DATA-1

Bit 7	Bit 6	Bit 5	Bit 4	
0	1	0	1	Open reel Stationary head Analog ATR
0	1	1	0	Open reel Stationary head Digital ATR
0	1	1	1	Cassette Rotary head Digital ATR

11/12 NAK

On reciept of the following errors, the CONTROLLED DEVICE will respond with this tally header as a negative acknowlegment, followed by a single DATA-1 byte, coded as follows.

DATA-1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIME OUT	FRAME ERROR	OVERUN ERROR	PARITY ERROR		CHKSUM ERROR		UNDEFD COMMAND

11/20 ATTENTION INTERUPT

This command is issued by the CONTROLLED DEVICE without provocation from the controlling entity. This command is used to provide an interrupt request capabilitiy to the CONTROLLED DEVICE. DATA-1 provides for a more detaild accounting of the nature of the issue requireing attention.

DATA-1 coding:

00h PREROLL Process Completed
01h Passed OUT POINT in process of TMP
02h Network De-activated

80h PREROLL Process PROHIBITED
81h reserved
82h Network Activated
83h Hard Error
84h Lock Margin Failure - Function Abort
In any SYNC PLAY ENABLE process (includingany Macro Tape Motion Processs such as AUTO EDIT, PREVIEW, REVIEW) should Lock be lost:

1) less than 6 frames before the IN POINT
or
2) less than the a Device Dependent Minimum Lock margin before the IN POINT.

85h Lost Lock
An abnormal loss of lock has has occuredduring maintained synchronous operation involving PLAY, SYNC-PLAY ENABLE, CHASE, REVIEW, PREVIEW, or AUTO EDIT operations.

TRANSPORT / AUDIO COMMANDS

20/00 STOP TMC

Causes the controlled ATR to stop as soon as possible. All recording tracks are automatically exited from record operation prior to exicution.

20/01 PLAY TMC

Causes the Device to play and Resolve to the most expediently available reference boundry. The CONTROLLED DEVICE will Resolve to the source as specified by DATA-1 and DATA-2 of the SERVO REFERENCE SELECT Command.

If either the selected SERVO REFERENCE or the it complementary Internal Tape Reference are not available, the CONTROLLED DEVICE shall default to Internal Xtal reference.

This Command may be used in conjuntion with the VAR FWD Command as a means to slew with another Device. After the slewing operation is performed, a PLAY Command may provide a "resolving" function.

"Resolve" is by definition, a Lock independent of a specific Offset to the Time Data that may be contained within either the selected SERVO REFERENCE or it complementary Internal Tape reference. In this regard a Resolve is always performed in a Data Independent manner, regardless of any Data Dependent atributes specified by the SERVO REFERENCE DATA-2 Selection.

20/02 RECORD-PLAY TMC

Causes the CONTROLLED DEVICE to immediately PLAY (as defined above) and initiate the recording process on the channel(s) that have been previously RECORD READY enabled via the EDIT PRESET Command. This recording operation may be cancelled by any of the other Transport Motion Commands (TMCs).

On the PCM-3402 this Command shall force activation of the "Advance Record" function.

21/08 TAPE LIFTER DEFEAT

Defeats the tape lifter mechanism of the controlled ATR, thus allowing full tape contact with the heads at all times.

DATA-1 coding:

00h	off
01h	on

20/10 FAST FORWARD TMC
Causes the controlled ATR to go foward at it's maximum speed without necessarily reproducing sound. All recording tracks are automatically exited from record operation prior to exicution.

22/11 VAR FWD TMC
Causes the controlled ATR to enter capstan controlled variable foward playback mode, relative to the selected FIXED SPEED.

coding:

If V = nominal play velocity from fixed speed select, then:

VAR FWD Velocity = V X VF (Velocity Factor)

VF= 10 ((DATA1/32)-2).
+[10 (((DATA1+1)/32)-2) - 10 (((DATA1)/32)-2)]* DATA2/256

2x/11(21) JOG FWD (REV) TMC
2x/13(23) SHUTTLE FWD (REV) TMC
Causes the controlled ATR to travel forward (reverse) at the specified speed without necessarily reproducing sound. Audio monitoring will be muted unless the LIFTER DEFEAT Status is true. All recording tracks are automatically exited from record operation prior to exicution.
coding:

If V = nominal play velocity from fixed speed select or da sys fs select, then:

Terminal Velocity = V X VF (Velocity Factor)

VF= 10 ((DATA1/32)-2).
+[10 (((DATA1+1)/32)-2) - 10 (((DATA1)/32)-2)]* DATA2/256

20/20 FAST REWIND TMC
Causes the controlled ATR to rewind at it's maximum speed without necessarily reproducing sound. All recording tracks are automatically exited from record operation prior to exicution.

2x/23 SHUTTLE REV TMC
See Text for SHUTTLE FWD 21/13

20/30 PREROLL TMP
Causes the controlled ATR to move to a tape position derived from the PREROLL DURATION PRESET, (minus any Device specific acceleration allowance) in advance of the IN POINT. LTC FROM TAPE defines tape position. All recording tracks are automatically exited from record operation prior to exicution.

24/31 CUE WITH DATA TMP

Causes the controlled ATR to move to the specified tape position as defined by LTC on Tape. All recording tracks are automatically exited from record operation prior to exicution.

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

20/34 SYNC PLAY ENABLE STMP

This Command is a Synchronous Tape Motion Process which causes the CONTROLLED DEVICE to be enabled to start and lock relative to SYNC offset in anticipation of the in point.

This Command will cause the CONTROLLED DEVICE to automatically Cue to the appropriate PREROLL position.

The CONTROLLED DEVICE will then monitor the selected ascending Timecode Reference (see SERVO REFERENCE SELECT DATA-3). Reaching the "Lock Actuation Time", will trigger the CONTROLLED DEVICE to accelerate and synchronize it's LTC from Tape, with the TIMECODE Reference.

This Lock Actuation Time may be defined:

Lock Actuation Time =

IN POINT - (PREROLL DURATION + SYNC OFFSET)

At the in point Synchronization must be assured. During the PREROLL DURATION the synchronization is established as specified by the term in the DATA-3 byte of servo reference select.

After the in point, synchronization is maintained as specified by the terms in the DATA-1 and DATA-2 bytes of servo reference select. In all cases, it is assumed that the selected Timecode Reference is presented to the CONTROLLED DEVICE in a reasonably real time manner during the actual PREROLL DURATION .

The Sync Active Status bit is True thoughout the Process of this command's operation.

The LTC timecode output of the device shall be a transparent re-transmision of the recieved LTC timecode during this STMP operation.

26/35 TRIG VARI STMP

This Command is a Synchronous Tape Motion Process which initially causes the CONTROLLED DEVICE to automatically Cue to the appropriate PREROLL position.

This command will then cause the Controlled device to monitor the ascending Timecode reference as selected by DATA-3 of the SERVO REFERENCE SELECT.

The CONTROLLED DEVICE will wait until the PREROLL DURATION prior to the Trigger Point specified in DATA-1 through DATA-4. At that time the CONTROLLED DEVICE will accelerate to the Vari Speed specified by DATA-5 and DATA-6, reaching the IN POINT at the Specified Trigger Time.

This Process does not truely PLAY in a manner synchronous to an incomming reference. Regardes, it is catagorized as Synchronous Tape Motion Process because it must establish a specific Vari Speed at a specified Trigger Time. The Sync Active Status bit is True thoughout the Process of this command's operation.

TRIGGER POINT

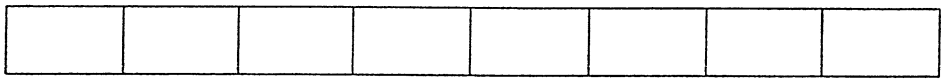
DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

DATA-5

00h = greater that nominal FIXED SPEED
80h = less than nominal FIXED SPEED

DATA-6

8 Bits Data: 00h hrough FFh (0 to 255 Decimal)



Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

Deviation from nominal FIXED SPEED in Percent are defined as follows:

Deviation (%) = .1 x DATA-6

Considering DATA-5 and DATA-6, the Argument Range is therefore 25.5%

29/36 TRIG TIMEFIT STMP

This Command is a Synchronous Tape Motion Process which initially causes the CONTROLLED DEVICE to automatically Cue to the appropriate PREROLL position.

This command will then cause the Controlled device to monitor the ascending Timecode reference as selected by DATA-3 of the SERVO REFERENCE SELECT.

The CONTROLLED DEVICE will wait until the PREROLL DURATION prior to the Trigger Point specified in DATA-1 through DATA-4. At that time the CONTROLLED DEVICE will accelerate to a Vari Speed internally determined by the the previously preset IN and OUT POINTS, and DATA-1 through DATA-8.

The CONTROLLED DEVICE will continue past the OUT point by the POSTROLL DURATION and STOP. DATA-9 specifies the Audio muting during the PREROLL and POSTROLL DURATIONS.

This Process does not truely PLAY in a manner synchronous to an incomming reference. Regardes, it is catagorized as Synchronous Tape Motion Process because it must establish a specifically calculated Vari Speed at a specified Trigger Time. The Sync Active Status bit is True thoughout the Process of this command's operation.

The internally determined Vari Speed may be calculated by the following:

Speed Deviation (%)=(TRIGGER DURATION - IN DURATION) x 100

Where:

TRIGGER DURATION = END TRIGGER POINT - TRIGGER POINT
and
IN DURATION = OUT POINT - IN POINT

TRIGGER POINT

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

END TRIGGER POINT

DATA-5		DATA-6		DATA-7		DATA-8	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

DATA-9
- 00h = no muting
- 01h = PREROLL DURATION muted
- 02h = POSTROLL DURATION muted
- 03h = PREROLL and POSTROLL DURATIONs muted

2x/37 CHASE STMP

This Command is a Synchronous Tape Motion Process which causes the controlled Device to Follow and Synchronize the LTC Tapecode with the selected Timecode Reference. This Synchronization is performed in full respect to the SYNC offset.

The LTC timecode output of the device shall be a transparent re-transmision of the recieved LTC timecode during CHASE operation.

The selected Timecode Reference (LTC or VITC or INTERNAL TCG) to which chase is to be performed is selected by the DATA-3 byte of servo reference select.
<<< unresolved>>>

This Command may utilize an optional DATA-1.

DATA-1

00h = Standard operation (as above)
01h = Capstan engagement prohibited

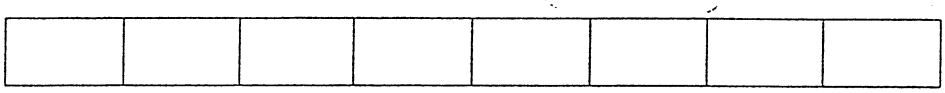
02h = Lock is maintained to External Digital Audio Reference. as locally selected (AES/EBU or SDIF Word Sync)

21/38(39) PROG SPEED +(-) TMC

These Commands cause an internal Xtal referenced play back of the CONTROLLED DEVICE within the Argument Range of of 25.5% relative to the selected FIXED SPEED.

DATA-1

8 Bits Data: 00h hrough FFh (0 to 255 Decimal)



Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

Deviation from nominal FIXED SPEED in Percent are defined as follows:

Deviation (%) = .1 x DATA-6

20/40 PREVIEW MTMP

This command is a Macro Tape Motion Process consisting of sequences of other TMPs and TMCs. This function also provides for specific Audio monitoring behaviors. This command causes the Device to perform the sync play ENABLE (an STMP) , and stop past the out point by the POSTROLL DURATION.

The Sync Active Status bit is True only thoughout the sync play ENABLE Process of this Macro command's operation.

Monitor Switching

Audio channels that are Record Readied by the edit preset command

During the PREROLL DURATION, all channels will monitor the Sync Head.

At the in point these channels will monitor Input

At the out point these channels will return to monitoring the Sync Head

Audio channels that are not Record Readied by the edit preset command

These channels will monitor the Sync Head throughout the preview operation.

20/41 REVIEW MTMP

This command is a Macro Tape Motion Process consisting of sequences of other TMPs and TMCs. This function also provides for specific Audio monitoring behaviors. This command causes the Device to perform the sync play ENABLE, and stop past the out point by the POSTROLL DURATION. All Audio channels will be set to Repro throughout the review operation. The Device will then locate to the out point..

The Sync Active Status bit is True only thoughout the sync play ENABLE Process of this Macro command's operation.

20/42 AUTO EDIT MTMP

This command is a Macro Tape Motion Process consisting of sequences of other TMPs and TMCs. This function also provides for specific Audio monitoring and record behaviors. This command causes the Device to perform the sync play ENABLE, and stop past the out point by the POSTROLL DURATION. The Device will then locate to the out point.

The Sync Active Status bit is True only thoughout the sync play ENABLE Process of this Macro command's operation.

Monitor Switching

Audio channels that are Record Readied by the edit preset command

During the PREROLL DURATION, these channels will monitor the Sync Head. At the in point these channels will have entered recording mode.

At the out point these channels will have exited recording mode. Following the out point these channels will return to monitoring the Sync Head

Audio channels that are not in Record Readied by the edit preset command

These channels will monitor the Sync Head throughout the preview operation.

20/43 OUT POINT PREVIEW MTMP

This command is a Macro Tape Motion Process consisting of sequences of other TMPs and TMCs. This function also provides for specific Audio monitoring behaviors. This command causes the Device to PLAY from a point twice the PREROLL DURATAION prior to the out point and stop past the out point by the POSTROLL DURATION.

The Sync Active Status bit is false thoughout the Process of this Macro command's operation.

Monitor Switching

Audio channels that are Record Readied by the edit preset command

During the play period these channels will monitor Input

At the out point these channels will monitor the Sync Head

Audio channels that are not Record Readied by the edit preset command

These channels will monitor the Sync Head throughout the out point preview operation.

20/60 FULL EE OFF

Cancels full ee on. (see below)

20/61 FULL EE ON
Forces all channels to monitor Input regardless of requirements of preview, review, auto edit or any other macro command which requests a Monitor selection proceedure.

The LTC Timecode output will be a transparent re-transmision of the recieved LTC timecode, however internally, the timecode track will continue to be read by the device.

20/63 SELECT EE ON
Forces all channels that have been Record Readied by the edit preset command, to monitor Input regardless of requirements of preview, review, auto edit or any other macro command which requests a monitor selection proceedure. This Command is cancelled by EDIT OFF.

20/64(65) EDIT OFF (ON)
When the CONTROLLED DEVICE is in PLAY, this command causes an immediate Record exit (entry) on the channels that have been previously Record Readied by the edit preset command.

When the CONTROLLED DEVICE is in STOP, the EDIT ON command shall cause an immediate PLAY actuation, with an immediate Record entry on the channels that have been previously Record Readied by the edit preset command.

PRESET AND SELECT COMMANDS

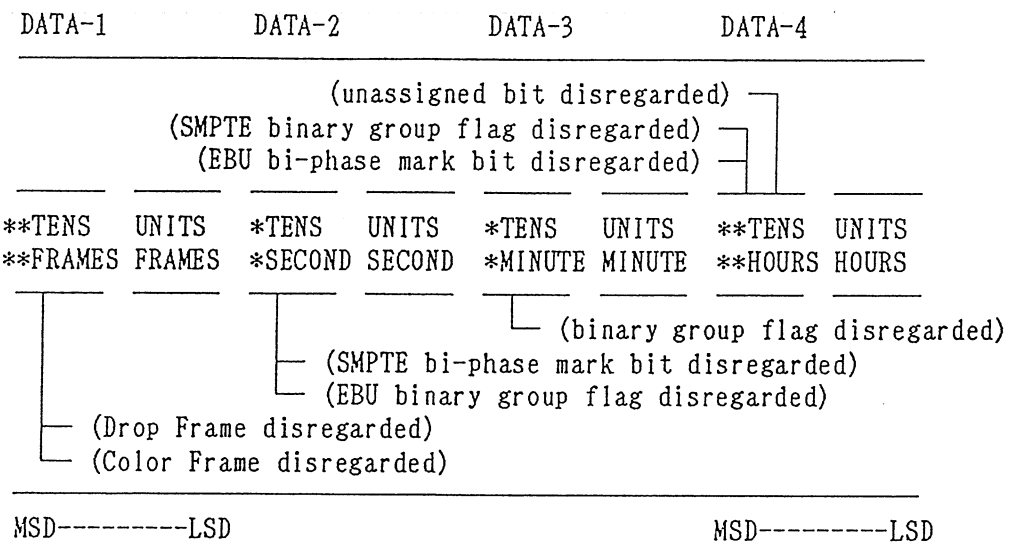
44/00 TIMER-1 PRESET

This command loads data into the counter roller tape timer. DATA-1 through DATA-4 are formatted as BCD; illustrated below. TIMER-1 must count in Modulo 24Hr form.

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

44/04 TCG PRESET

This command loads time code data into TCG (time code generator) of the CONTROLLED DEVICE. DATA-1 through DATA-4 are formatted as BCD; illustrated below.



SMPTE drop/non-drop, EBU, and Film code selections are locally selected

44/05 TCG UB PRESET
This command loads User Bit data into TCG (time code generator) of the CONTROLLED DEVICE. DATA-1 through DATA-4 are formatted as illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
2nd BINARY GROUP	1st BINARY GROUP	4th BINARY GROUP	3rd BINARY GROUP	6th BINARY GROUP	5th BINARY GROUP	8th BINARY GROUP	7th BINARY GROUP
MSD---------LSD						MSD---------LSD	

40/08 TIMER-1 RESET
This command resets TIMER-1 to zero.

40/10 IN ENTRY
This command loads the present time information from the SELECTED TAPE CODE of the CONTROLLED DEVICE into the IN DATA memory.

40/11 OUT ENTRY
This command loads the present time information from the SELECTED TAPE CODE of the CONTROLLED DEVICE into the OUT DATA memory.

44/14 IN DATA PRESET
This command loads the CONTROLLED DEVICE with the IN DATA time, DATA-1 through DATA-4 are formatted as BCD; illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

/15 OUT DATA PRESET
This command loads the CONTROLLED DEVICE with the OUT DATA time, DATA-1 through DATA-4 are formatted as BCD; illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

40/18 IN + SHIFT
This command increments the IN DATA time memory by one frame.

40/19 IN - SHIFT
This command decrements the IN DATA time memory by one frame.

40/1A OUT + SHIFT
This command increments the OUT DATA time memory by one frame.

40/1B OUT - SHIFT
This command decrements the OUT DATA time memory by one frame.

40/20 in flag reset
Resets the IN FLAG Status Bit

40/21 out flag reset
Resets the OUT FLAG Status Bit

40/24 in recall
Re-enables pending in point.

40/25 out recall
Re-enables pending out point.

40/2D LOST LOCK RESET
This Command resets DATA8 Bit6: LOST LOCK of the 7x/20:STATUS DATA.

The LOST LOCK status is set when maintained synchronous operation is compromised by a loss of lock during PLAY, SYNC-PLAY, CHASE, REVIEW, PREVIEW, or AUTO EDIT operations

4X/30 edit preset
This Command selects channels to be Record Ready for subsequently issued Edit Commands.

DATRs

DATA-1

	INSERT	ASMBLE		A4	TC A3	A2	A1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

DATA-2

resv'd	resv'd	resv'd	resv'd	DA4	DA3	DA2	DA1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Analog ATRs, (Four Tracks or less)

DATA-1

	resv'd	resv'd		A4	TC A3	A2	A1

Analog Multitrack ATRs, (More than Four tracks)
DATA-1, 2, 3, 4.

	resv'd	resv'd		resv'd	TC	resv'd	resv'd
A8	A7	A6	A5	A4	A3	A2	A1
A16	A15	A14	A13	A12	A11	A10	A9
A24	A23	A22	A21	A20	A19	A18	A17
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

For Analog ATR of four tracks or less,.only DATA-1 is required. In Multitrack use, the TC bit in DATA-1 will always control the locally assigned TC track regardless of it's assignment.

△1 ~~42/31~~ 44/31

PREROLL DURATION PRESET
Requests as specified a Real Time run up period to be performed in advance of the IN POINT. Requests for PREROLL DURATIONs less than the DEVICE SPECIFIC minimum for current operational parameters of the device shall cause the CONTROLLED DEVICE to default to it's minimum value. These minimum values may be confirmed by the editing entity through the tally of the PREROLL DURATION DATA. Minimum values are Device Specific, and may change as operational parameters of the machine change. Requests for PREROLL DURATIONs greater than the maximum shall cause the CONTROLLED DEVICE to default to it's greatest allowable value. DATA-1, through DATA-4 are formatted as BCD; illustrated below:

△1

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MIN.	UNITS MIN	TENS HOURS	UNITS HRS
MSD---------							-LSD

Maximum PREROLL Times are limited as follows:

59 Sec./29 Fr SMPTE Time code
59 Sec./24 Fr. EBU Time code
(59 sec./23 Fr. Film Time code)

41/32 TAPE/AUTO SELECT

This Command causes the Controlled device to select a specific monitor selection of Audio Channels during TMC states that do not normally provide for playback of the program material. ie STOP, FF, REW, PREROLL etc.

00= Input monitor on all channels when not in a Reproducing transport mode. The LTC Timecode output will be a transparent re-transmision of the recieved LTC timecode, however internally, the timecode track will continue to be read by the device.

01= Tape monitor on all channels when not in a Reproducing transport mode.

4x/33 SERVO REFERENCE SELECT

This Command provides the means to select the manner in which capstan controlled speed and synchronous transport operations are referenced.

Please refer to PLAY, RECORD PLAY, SYNC PLAY ENABLE, CHASE, PREVIEW, REVIEW, AUTO EDIT.

coding ==========

DATA-1

00h = Auto (Conditional DATR Recording) Reference

IF...

The CONTROLLED DEVICE is a DATR
and
Any Digital Audio Channel has been previously Record Readied by an Edit Preset selection
and
External Digital Audio Word Sync (AES/EBU or SDIF) is available (locally enabled and valid)

THEN...

The CONTROLLED DEVICE will utilize the reference specified by DATA-2, and switch to the External Digital Audio reference prior to the start of any recording operation. The CONTROLLED DEVICE will again utilize the reference specified by DATA-2apon the receipt of any subsequent TMC

ELSE...

The CONTROLLED DEVICE will utilize the reference specified by DATA-2.

01h = Specific Reference (specified in DATA-2)

02h = External Input Digital Audio Reference
The CONTROLLED DEVICE will utilize the External Digital Audio as capstan reference. AES/EBU or SDIF Word Sync as locally selected.

IF...
The CONTROLLED DEVICE is not a DATR
or
The External Digital Audio Reference is not available.
or
The External Digital Audio Reference is not valid.

THEN...
The CONTROLLED DEVICE will utilize the Internal Xtal as capstan reference

03h = Internal Xtal
The CONTROLLED DEVICE will utilize the Internal Xtal as capstan reference. If the CONTROLLED DEVICE is a DATR then the Internal Xtal source may be internally synchronized with an external Video reference. (as locally selected.)

04h = External Reference Signal
The CONTROLLED DEVICE will utilize an Externally supplied Capstan Reference Signal for capstan reference.

FFh = as locally selected

DATA-2
Selects the Tape Transport Servo reference for PLAY and RECORD PLAY TMCs, as well as selecting the Tape Transport Servo reference for the maintainence portions of the Synchronous transport operations such as SYNC PLAY ENABLE, CHASE, PREVIEW, REVIEW, and AUTO EDIT.

In PLAY and RECORD PLAY operations the the CONTROLLED DEVICE will Resolve the most expedient Tape Reference boundary to the reference specified below. PLAY and RECORD PLAY Resolve operations, by definition, disregard any Data Dependent specification specified in this selection. (See PLAY TMC).

In SYNC PLAY ENABLE, CHASE, PREVIEW, REVIEW, and AUTO EDIT, the CONTROLLED DEVICE will maintain Locked condition with the reference specified in this selection.

00h = External LTC Data Independent
01h = External LTC Data Dependent *
02h = External Video Data Independent
03h = External VITC Data Dependent *
04h = Internal TCG Data Dependent *
05h = External Digital Audio
(AES/EBU, SDIF)
FFh = as locally selected

*performs in Data Independent manner on PLAY and RECORD PLAY.

DATA-3

The CONTROLLED DEVICE will establish locked condition with the reference selected below.

00h = External LTC
01h = External VITC
03h = Internal TCG .
FFh = as locally selected

In Sync Play Enable, Chase, Preview, Review, and Auto Edit,

Select the Tape Transport Servo reference for Play and Record Play TMCs. In Play and Record Play operations, the control Device will Resolve (Data Independent) to the most expedient Tape Reference boundary to the reference specified above.

41/34 HEAD SELECT

Selects the current global tape head selection used for tape monitoring.

DATA-1:
00h = Sync Head (tape)
01h = PB Head (tape)

41/36 TIMER MODE SELECT

Selects the current Tape code Source selection used for all tape location specific operations.

DATA-1:
01h = LTC
02h = TIMER-1 <CAUTION-ACCURACY OF EDITS COMPROMISED>

4x/3A EDIT FIELD SELECT

This command provides for a delay of both the IN and OUT points by 40 Bits periods of LTC on tape. Alternativly, through the optional use of DATA-2 a full 0 to 79 Bit Sub-Frame accuracy may be supported.

DATA-1:
00h = per machine default
If command is received during an odd field then edit at bit 0
If command is received during an even field then edit at bit 40

>comment< <<< I still don't think I can support this capability>>>

01h = no delay, edit at bit 0
02h = Delay, edit at Bit 39

DATA-2: IN POINT DELAY
(optional, Causes DATA-1 to be disregarded)

TENS BITS	UNITS BITS
MSD---------LSD	

DATA-3: OUT POINT delay
(optional, if not sent, defaults to data in DATA-2)

TENS BITS	UNITS BITS	sets OUT POINT delay in Bits
MSD---------LSD		

~~42~~/3C 44 POSTROLL DURATION PRESET

Requests as specified a Real Time period to be rolled in excess of the OUT POINT. Requests for POSTROLL DURATIONs less than 2 seconds shall cause the CONTROLLED DEVICE to default to the 2 second minimum value. Requests for POSTROLL DURATIONs greater than the maximum shall cause the CONTROLLED DEVICE to default to it's greatest allowable value. DATA-1, through DATA-4 are formatted as BCD; illustrated below:

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MIN.	UNITS MIN.	TENS HRS.	UNITS HRS.
MSD---------LSD							

Maximum POSTROLL DURATIONS are limited as follows:

59 Sec./29 Fr	SMPTE Time code
59 Sec./24 Fr.	EBU Time code
(59 sec./23 Fr.	Film Time code)

42/50 DA INPUT SELECT

Selects either the digital or analog input for digital recording.

DATA-1

				DA4	DA3	DA2	DA1

DATA-2

				DA4	DA3	DA2	DA1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

coding: 00 = digital
01 = analog
10 = retains current condition
11 = as locally selected

42/51 DA SYS EMPH SELECT
Selects the systems's emphasis condition for analog input.

DATA-1

				DA4	DA3	DA2	DA1

DATA-2

				DA4	DA3	DA2	DA1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

coding: 00 = off
01 = on
10 = retains current condition
11 = as locally selected

41/58 DA SYS FS SELECT
Selects the DATR's Sample Rate.

coding: 00 = reserved
01 = 48 kHz
02 = 44.1 kHz
03 = 32 kHz
04 = reserved
05 = reserved
06 = 44.056 kHz
FF = as locally selected

41/73 FIXED SPEED SELECT
Selects the nominal tape play speed. A STOP may be exicuted prior to FIXED SPEED SELECT if the device is not in STOP. A CONTROLLED DEVICE may override this setting should the Timecode be prerecorded at a different fixed speed.

DATA-1:
00h = 30 IPS
01h = 15 IPS (or 13.78125 if Fs is 44.1 kHz)
02h = 7 1/2 IPS (or 6.890 if Fs is 44.1 kHz)
03h = 3 3/4 IPS
FFh = as locally selected

44(45)/78 SYNC OFFSET

This command loads synchronization Offset data into the CONTROLLED DEVICE. The Offset is the requested difference between the Internal LTC from tape and the External Timecode Reference in a locked and synchronous operation.

Offset = LTC - External Timecode Reference

ie. If the CONTROLLED DEVICE is to lead the External Timecode Reference by 1 minute, then:
Offset = 00:01:00:00

DATA-1 through DATA-4 provide for offset to frame resolution formatted as BCD; illustrated below. As Timecode is a modulo twenty four hour count, negative offsets are represented in 24h complement form.

ie. If the CONTROLLED DEVICE is to lag the External Timecode Reference by 1 minute, then:
Offset = (-)00:01:00:00 or 23:59:00:00

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

The optional DATA-5 provides a bit resolution extention to the SYNC OFFSET indicated above. DATA-5 is formatted as BCD; illustrated below. The argument range is 0 to 80.

DATA-5 (optional)	
TENS BITS	UNITS BITS
MSD---------LSD	

4x/72 SYNC GRADE SELECT (tentative)
(tentative, offered as a suggestion by J. Takayama, no arguments proposed at this time)

This command is used to specify a allowable Acuracy Window for all commands that provide Synchronous operation.

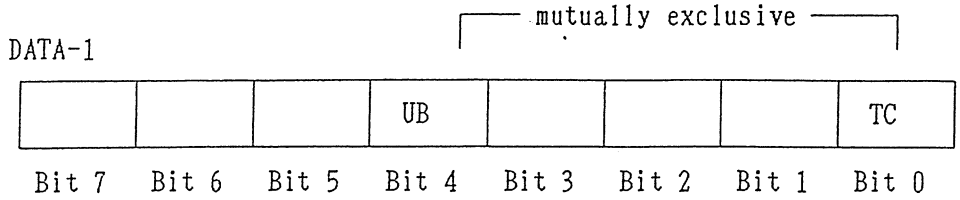
Synchronous operation grades:
Bit Accurate : +/- 1/40th frame (+/- 2 Timecode Bits
Frame Accurate : +/- 1 frame
Not Accrate : No Accuracy guaranteed; generally +/- a few frames.
Non-Synchronous operation grades:
Preroll&Play : No Accuracy guaranteed
Play : No Accuracy guaranteed
Manual : No Accuracy guaranteed

>>comment<< I have some question as to the utility of the need for this facility at all. In particular, I am not thrilled at all with the last three grades. The operation with most of the STMP's and MTMP's are really very ambigious. If we want these functions, why don't we just use the the primitive TMC's that are already provided!!. This is really an unclean oganization. I don't like this...Yech!

SENSE REQUEST COMMANDS (tally request)

61/0A TCG TIME DATA SENSE

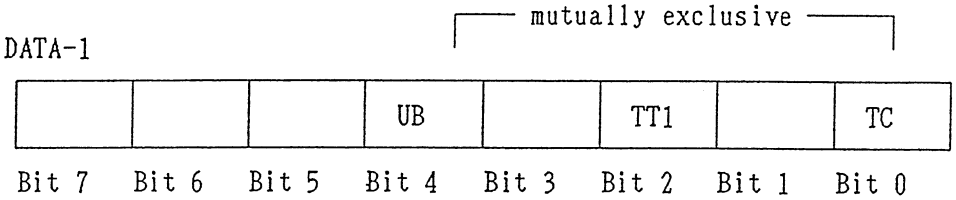
This command is used for requesting the current TCG TIME DATA. The CONTROLLED DEVICE will respond via the TCG TIME DATA SENSE RETURN HEADER in accordance with the contents of DATA-1.



REQUEST	RESPONCE
DATA-1 = 01 req for GEN TC	74/08 .. (GEN TIME DATA)
DATA-1 = 10 req for GEN TC	74/09 .. (GEN UB DATA)

61/0C CURRENT TIME DATA SENSE

This command is used for requesting the current LTC TIME DATA. The CONTROLLED DEVICE will respond via the LTC TIME DATA SENSE RETURN HEADER in accordance with the contents of DATA-1..



REQUEST	RESPONCE
DATA-1 = 01 req for LTC TC	74/04 .. (LTC TIME DATA)
	74/14 .. (LTC TIME DATA) (INTERPOLATED)
DATA-1 = 04 req for LTC TC	74/00 .. (T-TIMER-1-DATA)
DATA-1 = 10 req for LTC UB	74/05 .. (LTC UB DATA)

60/10 IN DATA SENSE

This command is used for requesting the current IN DATA. The CONTROLLED DEVICE will respond via the IN DATA SENSE RETURN HEADER.

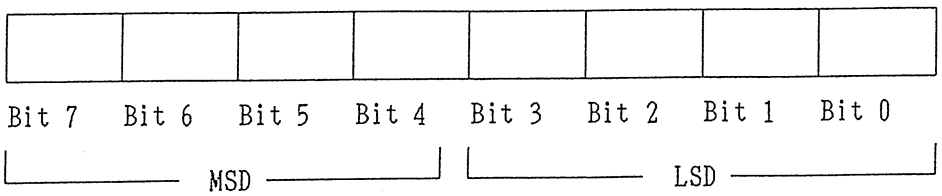
60/11 OUT DATA SENSE

This command is used for requesting the current OUT DATA. The CONTROLLED DEVICE will respond via the OUT DATA SENSE RETURN HEADER. Although the IN and OUT FLAGs may be reset, the Data is still available.

61/20 STATUS REQUEST

This command is used for requesting the STATUS DATA of the CONTROLLED DEVICE. The CONTROLLED DEVICE will return a responce in accordance with DATA-1 illustrated below.

DATA-1



MSD

Indicates the initial data number of the 7x/20 STATUS DATA to be tallied back

LSD

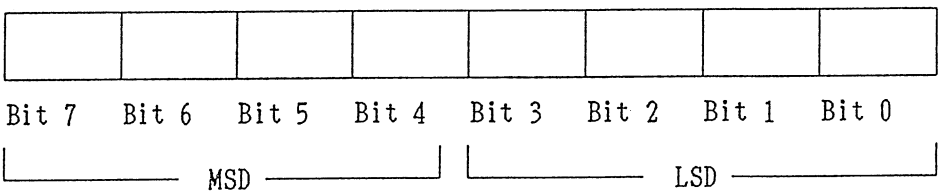
Indicates the number of data bytes in 7x/20 STATUS DATA to be tallied back

61/30 EDIT PRESET SENSE

Requests the return of the record ready map. The CONTROLLED DEVICE will respond via the EDIT PRESET DATA SENSE RETURN HEADER.

The CONTROLLED DEVICE will return a responce in accordance with DATA-1 illustrated below.

DATA-1



MSD

Indicates the initial data number of the 7x/30 EDIT PRESET DATA to be tallied back

LSD

Indicates the number of data bytes in 7x/30 EDIT PRESET DATA to be tallied back

60/31 PREROLL DATA SENSE

Requests the return of the PREROLL DURATION DATA. The CONTROLLED DEVICE will respond via the PREROLL DURATION DATA SENSE RETURN HEADER.

60/32 TAPE AUTO SEL SENSE

Requests the return of the TAPE/AUTO SEL DATA. The CONTROLLED DEVICE will respond via the TAPE/AUTO SEL STATUS SENSE RETURN HEADER.

60/33 SERVO REFERENCE SEL SENSE

Requests the return of the SERVO REFERENCE SEL DATA. The CONTROLLED DEVICE will respond via the SERVO REFERENCE SEL STATUS SENSE RETURN HEADER.

60/34 HEAD SEL SENSE
Requests the return of the HEAD SEL DATA. The CONTROLLED DEVICE will respond via the HEAD SEL STATUS SENSE RETURN HEADER.

60/36 TIMER MODE SENSE
This command requests the selection status of the TAPE TIME SELECT of the CONTROLLED DEVICE. The CONTROLLED DEVICE will respond via the TIMER MODE STATUS SENSE RETURN HEADER.

60/3C POSTROLL DATA SENSE
Requests the return of the POSTROLL DURATION DATA. The CONTROLLED DEVICE will respond via the POSTROLL DURATION DATA SENSE RETURN HEADER.

60/50 DA INPUT SENSE
This command requests the selection status of the DA INPUT of the CONTROLLED DEVICE. The CONTROLLED DEVICE will respond via the DA INPUT STATUS SENSE RETURN HEADER.

60/51 DA SYS EMPH SENSE
This command requests the selection status of the DA SYS EMPH of the CONTROLLED DEVICE. The CONTROLLED DEVICE will respond via the DA SYS EMPH STATUS SENSE RETURN HEADER.

60/52 DA INPUT EMPH SENSE
This command requests the selection status of the DA INPUT EMPH of the CONTROLLED DEVICE. The CONTROLLED DEVICE will respond via the DA INPUT EMPH STATUS SENSE RETURN HEADER.

60/53 PB EMPH SENSE
This command requests the selection status of the PB EMPH of the CONTROLLED DEVICE. The CONTROLLED DEVICE will respond via the PB EMPH STATUS SENSE RETURN HEADER.

60/58 DA SYS Fs SENSE
This command requests the selection status of the DA SYS Fs of the CONTROLLED DEVICE. The CONTROLLED DEVICE will respond via the DA SYS Fs STATUS SENSE RETURN HEADER.

60/73 FIXED SPEED SENSE
This command is used for requesting the current FIXED SPD DATA. The CONTROLLED DEVICE will respond via the FIXED SPD DATA SENSE RETURN HEADER.

61/78 SYNC OFFSET REQ
This command is used for requesting the current or Preset frame resolution, synchronization offset data from the CONTROLLED DEVICE. The CONTROLLED DEVICE will respond via the SYNC OFFSET DATA SENSE RETURN HEADER.

DATA-1:
00h = PRESET VALUE
01h = CURRENT VALUE
02h = reserved
¦ ¦
FFh = reserved

SENSE RETURN HEADERS (tally ret.)

74/00 TT1 DATA

When the CONTROLLED DEVICE recieves a CURRENT TIME SENSE REQUEST (data1 = 04) the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1 through DATA-4 are formatted as BCD; illustrated below.

74/04 LTC TIME DATA

When the CONTROLLED DEVICE recieves a CURRENT TIME SENSE REQUEST (data1 = 01) the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1 through DATA-4 are formatted as BCD; illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

74/05 LTC UB DATA

When the CONTROLLED DEVICE recieves a CURRENT TIME SENSE REQUEST (data1 = 10) the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1 through DATA-4 are formatted as illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
2nd BINARY GROUP	1st BINARY GROUP	4th BINARY GROUP	3rd BINARY GROUP	6th BINARY GROUP	5th BINARY GROUP	8th BINARY GROUP	7th BINARY GROUP
MSD---------LSD						MSD---------LSD	

74/08 TCG TIME DATA

When the CONTROLLED DEVICE recieves a TC GEN DATA SENSE REQUEST (data1 = 01) the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1 through DATA-4 are formatted as BCD; illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

74/09 TCG UB DATA

When the CONTROLLED DEVICE recieves a TC GEN DATA SENSE REQUEST (data1 = 10) the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1 through DATA-4 are formatted as illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
2nd BINARY GROUP	1st BINARY GROUP	4th BINARY GROUP	3rd BINARY GROUP	6th BINARY GROUP	5th BINARY GROUP	8th BINARY GROUP	7th BINARY GROUP
MSD---------LSD						MSD---------LSD	

74/10 IN DATA

When the CONTROLLED DEVICE recieves a IN DATA SENSE REQUEST the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1 through DATA-4 are formatted as BCD; illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

74/11 OUT DATA

When the CONTROLLED DEVICE recieves a OUT DATA SENSE REQUEST the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1 through DATA-4 are formatted as BCD; illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

74/14 LTC TIME DATA

If, when the CONTROLLED DEVICE recieves a CURRENT TIME SENSE REQUEST (data1 = 01) the CONTROLLED DEVICE cannot read valid LTC TIME DATA, the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following interpolated (extrapolated) LTC data. The interpolated LTC data is derived from the Timer roller, based on the last vaild LTC. DATA-1 through DATA-4 are formatted as BCD; illustrated below.

DATA-1		DATA-2		DATA-3		DATA-4	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

7x/20 STATUS DATA

When the CONTROLLED DEVICE recieves the STATUS SENSE REQUEST, the following data will be sent back as a responce:

7x/20 . i. STATUS DATA

BIT # / DATA	7	6	5	4	3	2	1	0
0			TAPE OUT	NO REF SERVO		HARD ERROR		LOCAL
1	STANDBY [1]	TENSION OFF	STOP		REW	FAST FWD	RECORD PLAY	PLAY
2	SERVO LOCK	PROG- SPD +/-	SHUTTLE	JOG	VARI- FWD	TAPEDIR (REV=1)	STILL	CUED or PREROLL
3	AUTO ON						OUT FLAG	IN FLAG
4	SEL EE (INPUT =1)	FULL EE		EDIT ON	REVIEW	AUTO EDIT	PREVIEW	PREROLL IN PROC
5		INSERT	ASMBL		A4	A3 (TC)	A2	A1
6								
7				SYNC ACTIVE	DISPLAY HLD [0]	SPOT ER [0]		IN/OUT STATUS
8		LOST LOCK	NEAR EOT	EOT		SERVO ALARM	SYSTEM ALARM	MASTER SAFE
9	FUNCT ABORT							
A								
B								
C					DA4	DA3	DA2	DA1
D								
E								
F								

SYNC PLAY ENABLE STATUS BIT IS NOT YET ASSIGNED

71-F/20 STATUS DATA (continued)

When the CONTROLLED DEVICE recieves a STATUS SENSE REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the the appropriatly configured data fields. See STATUS SENSE REQ. (61/20).

DATA #0/BIT 0

Bit 0 is set to "1" when the CONTROLLED DEVICE is not Network enabled.

DATA #0/BIT 2

Bit 2 is set to "1" when the CONTROLLED DEVICE senses any potentially disabling internal system errors.

DATA #0/BIT 4

Bit 4 is set to "1" when the CONTROLLED DEVICE senses that the requested servo reference is not available, not valid or that the CONTROLLED DEVICE does not support the requested SERVO REFERENCE

DATA #0/BIT 5

Bit 5 is set to "1" when the CONTROLLED DEVICE senses that tape is not threaded in a manner that permits normal operation.

DATA #1,/BITs 0, 1, 2, 3, 5

These data bytes indicate the identified TMC conditions.

DATA #1,/BIT 6

BIT 6 indicates that the CONTROLLED DEVICE is in a locally commanded Tension released TMC condition.

DATA #1,/BIT 7

BIT 7 will always indicates a positive true condition.

DATA #2,/BIT 0

BIT 0 indicates that the CONTROLLED DEVICE has successfully performed a CUE WITH DATA or PREROLL operation.

DATA #2,/BIT 1

BIT 1 indicates that the CONTROLLED DEVICE is not moving tape, This is independent of the current TMC condition.

DATA #2/BIT 2

BIT 2 indicates that current tape direction is negative. (undefined when tape is not moving)

DATA #2/BIT 3
BIT 3 This bit indicates that the CONTROLLED DEVICE is performing the VAR FWD TMC operation.

DATA #2/BIT 4
BIT 3 This bit indicates that the CONTROLLED DEVICE is performing the JOG TMC operation.

DATA #2/BIT 5
BIT 3 This bit indicates that the CONTROLLED DEVICE is performing the SHUTTLE TMC operation.

DATA #2/BIT 6
BIT 3 This bit indicates that the CONTROLLED DEVICE is performing the PROG SPEED + or PROG SPEED - TMC operations.

DATA #2/BIT 7
BITt 7 is set to "1" when the CONTROLLED DEVICE is in a locked, synchronized condition with it's Selected SERVO REFERENCE Source.

DATA #3/ BIT 0 (1) stored
BIT 0 indicates that ~~an~~ IN POINT ~~has been passed in a forward moving operation.??~~ is valid.

DATA #3/ BIT 1 (1) stored
BIT 1 indicates that ~~an~~ OUT POINT ~~has been passed in a forward moving operation.??~~ is valid.

DATA #3/ BIT 7
BIT 7 is always positive true, provided that the AUTO EDIT family of Macro Commands are supported.

DATA #4/Bit 0
BIT 0 indicates that a PREROLL is in Process

DATA #4/Bit 1
BIT 1 indicates that a PREVIEW is in Process

DATA #4/Bit 2
BIT 2 indicates that a AUTO EDIT is in Process

DATA #4/Bit 3
BIT 3 indicates that a REVIEW is in Process.

DATA #4/Bit 4
BIT 4 indicates that a Recording operation is in Process.

DATA #4/Bit 6
BIT 6 indicates that a FULL EE Monitor Selection is in effect.

DATA #4/Bit 7

BIT 7 indicates that a SELECT EE Monitor Selection is in effect.

DATA #5/Bit 0, 1, 2, 3

These Bits indicate Record Ready Status as selected by the EDIT PRESET Command

DATA #5/Bit 5, 6

These Bits indicate the INSERT and ASSEMBLE Status as selected by the EDIT PRESET Command

---

DATA #7/BIT 0

BIT 0 is set positive true when the CONTROLLED DEVICE in PREVIEW or AUTO EDIT and is running between the IN POINT and the OUT POINT.

DATA #7/BIT 2, 3

These Bits shall indicate positive false [0].

DATA #7/BIT 4

This Bit shall be positive true when there is currently a SYNCHRONOUS Tape Motion Process (STMP) in progress.

SYNC-PLAY, TRIG VARI, TRIG TIMFIT, and CHASE are STMPs.

PREVIEW, REVIEW and AUTO-EDIT are Macro Tape Motion Processes (MTMP) that may in turn cause the actuation of these STMPs.

>comment< <<< I hope this is better ??? >>>

DATA #8/BIT 0

BIT 0 shall indicate positive true should the CONTROLLED DEVICE be locally Record Inhibited.

DATA #8/BIT 1

BIT 1 is reserved for currently undefined hardware or systems errors. It shall, for now, indicate positive true always.

DATA #8/BIT 2

BIT 2 is reserved for currently undefined SERVO related hardware problems. It shall, for now, indicate positive true always.

DATA #8/BIT 4

BIT 4 shall indicate positive true when the CONTROLLED DEVICE detects less that 30 seconds of tape remaining. (at what velocity??, reverse also?)

DATA #8/BIT 5
BIT 5 shall indicate positive true when the CONTROLLED DEVICE detects less that 150 seconds of tape remaining. (at what velocity??, reverse also?)

DATA #8/BIT 6
BIT 6 shall indicate positive true when maintained synchronous operation is compromised by a loss of lock during the PLAY TMC, or the SYNC PLAY ENABLE, and CHASE STMP operations

DATA #9/BIT 7
BIT 7 shall indicate positive true when the CONTROLLED DEVICE is attempting a SYNC PLAY ENABLE STMP, and lock has been lost:
1) less than 6 frames before the IN POINT
or
2) less than the a Device Dependent Minimum Lock margin before the IN POINT.

DATA #C/Bit 0, 1, 2, 3
These Bits indicate Record Ready Status as selected by the EDIT PRESET Command

SYNC-PLAY ENABLE STATUS BIT IS NOT YET ASSIGNED

7x/30 EDIT PRESET DATA
When the CONTROLLED DEVICE recieves a EDIT PRESET DATA REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. The responce may differ in construction depending on the CONTROLLED DEVICE Type.

DATRs

DATA-1

	INSERT	ASMBLE		A4	TC A3	A2	A1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

DATA-2

resv'd	resv'd	resv'd	resv'd	DA4	DA3	DA2	DA1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Analog ATRs, (Four Tracks or less)

DATA-1

	resv'd	resv'd		A4	TC A3	A2	A1

Analog Multitrack ATRs, (More than Four tracks)
DATA-1, 2, 3, 4.

	resv'd	resv'd		resv'd	TC	resv'd	resv'd
A8	A7	A6	A5	A4	A3	A2	A1
A16	A15	A14	A13	A12	A11	A10	A9
A24	A23	A22	A21	A20	A19	A18	A17
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

For Analog ATR of four tracks or less,.only DATA-1 is required. In Multitrack use, the TC bit in DATA-1 will always control the locally assigned TC track regardless of it's assignment.

72/31 PREROLL DURATION DATA
When the CONTROLLED DEVICE recieves a PREROLL DURATION DATA REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1, through DATA-4 are formatted as BCD; illustrated below:

DATA-1		DATA-2	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS
MSD---------LSD			

Maximum PREROLL DURATIONs are limited as follows:

59 Sec./29 Fr SMPTE Time code
59 Sec./24 Fr. EBU Time code
(59 sec./23 Fr. Film Time code)

71/32 TAPE/AUTO SELECT STATUS
When the CONTROLLED DEVICE recieves a TAPE AUTO STATUS REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the data representing the condition of the current AUTO INPUT selection. ie:

00= Input monitor on all channels when not in a Reproducing transport mode

01= Tape monitor on all channels when not in a Reproducing transport mode

73/33 SERVO REF SEL STATUS

When the CONTROLLED DEVICE recieves a SERVO REF STATUS REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data.

DATA-1

00h = Auto (Conditional DATR Recording) Reference
01h = Specific Reference (specified in DATA-2)
02h = External Input Digital Audio Reference
03h = Internal Xtal
04h = External Reference Signal

DATA-2

00h = External LTC Data Independent
01h = External LTC Data Dependent
02h = External Video Data Independent
03h = External VITC Data Dependent
04h = Internal TCG Data Dependent
05h = External Digital Audio
(AES/EBU, SDIF

DATA-3

00h = External LTC
01h = External VITC
03h = Internal TCG

71/34 HEAD SELECT STATUS

When the CONTROLLED DEVICE recieves a HEAD SELECT STATUS REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data representing the current global tape head selection used for tape monitoring. ie:

00h = Sync Head (tape)
01h = PB Head (tape)

71/36 TIMER MODE STATUS

When the CONTROLLED DEVICE recieves a TIMER MODE STATUS REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data.

DATA-1:
01h = LTC
02h = TIMER-1

72/3C POSTROLL DURATION DATA

When the CONTROLLED DEVICE recieves a POSTROLL DURATION DATA REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1, through DATA-4 are formatted as BCD; illustrated below:

DATA-1		DATA-2	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS

MSD---------LSD

Maximum POSTROLL DURATIONs are limited as follows:

59 Sec./29 Fr	SMPTE Time code
59 Sec./24 Fr.	EBU Time code
(59 sec./23 Fr.	Film Time code)

71/50 DA INPUT STATUS

When the CONTROLLED DEVICE recieves a DA INPUT STATUS REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data.

DATA-1

				DA4	DA3	DA2	DA1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

coding: 0 = digital
1 = analog

71/51 DA SYS EMPH STATUS

When the CONTROLLED DEVICE recieves a DA SYS EMPH STATUS REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data.

DATA-1

				DA4	DA3	DA2	DA1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

coding: 0 = off
1 = on

71/52 DA INPUT EMPH STATUS
When the CONTROLLED DEVICE recieves a DA INPUT EMPH STATUS REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data.

DATA-1

				DA4	DA3	DA2	DA1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

coding: 0 = off
1 = on

71/53 DA PB EMPH STSTUS
When the CONTROLLED DEVICE recieves a DA PB EMPH STATUS REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data.

DATA-1

				DA4	DA3	DA2	DA1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

coding: 0 = off
1 = on

71/58 DA SYS Fs STATUS
When the CONTROLLED DEVICE recieves a DA SYS Fs STATUS REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data.

coding: 00 = reserved
01 = 48 kHz
02 = 44.1 kHz
03 = 32 kHz
04 = reserved
05 = reserved
06 = 44.056 kHz

71/73 FIXED SPEED DATA

When the CONTROLLED DEVICE recieves a FIXED SPEED DATA REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. DATA-1 contains the nominal tape play speed.

coding:

00hex = 30 IPS
01hex = 15 IPS (or 13.78125 if Fs is 44.1 kHz)
02hex = 7 1/2 IPS (or 6.890 if Fs is 44.1 kHz)
03hex = 3 3/4 IPS

75/78 SYNC OFFSET DATA

When the CONTROLLED DEVICE recieves a SYNC OFFSET REQ the CONTROLLED DEVICE will respond with this SENSE RETURN HEADER followed by the following data. This data represents either the PRESET Offset, or Current Offset of the Controlled device. DATA-1 through DATA-5 are formatted as BCD; illustrated below.

DATA-1:

00h = PRESET VALUE
01h = CURRENT VALUE
81h = CURRENT VALUE (interpolated)
other codes reserved

DATA-2		DATA-3		DATA-4		DATA-5	
TENS FRAMES	UNITS FRAMES	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS
MSD---------LSD						MSD---------LSD	

DATA-6	
TENS BITS	UNITS BITS
MSD---------LSD	

I have distinguished the different type of Processes by catagory.. I have integrated these catagories into the command definitions and into the SYNC ACTIVE Status description. A Summary below:

MTMP Macro Tape Motion Processes

PREVIEW
calls:

STMP	SYNC PLAY ENABLE	
TMC	STOP	(outpoint + POSTROLL DURATION)

REVIEW
calls:

STMP	SYNC PLAY ENABLE	
TMC	STOP	(@ OUT POINT + POSTROLL DURATION)
TMP	CUE WITH DATA	(@ OUT POINT)

AUTO EDIT
calls:

STMP	SYNC PLAY ENABLE	
TMC	STOP	(@ OUT POINT + POSTROLL DURATION)
TMP	CUE WITH DATA	(@ OUT POINT)

OUT POINT REVIEW
calls:

TMP	CUE WITH DATA	(@ OUT POINT - PRETROLL DURATION)
TMC	STOP	(@ OUT POINT + POSTROLL DURATION)

STMP Synchronous Tape Motion Processes

SYNC PLAY ENABLE

CHASE

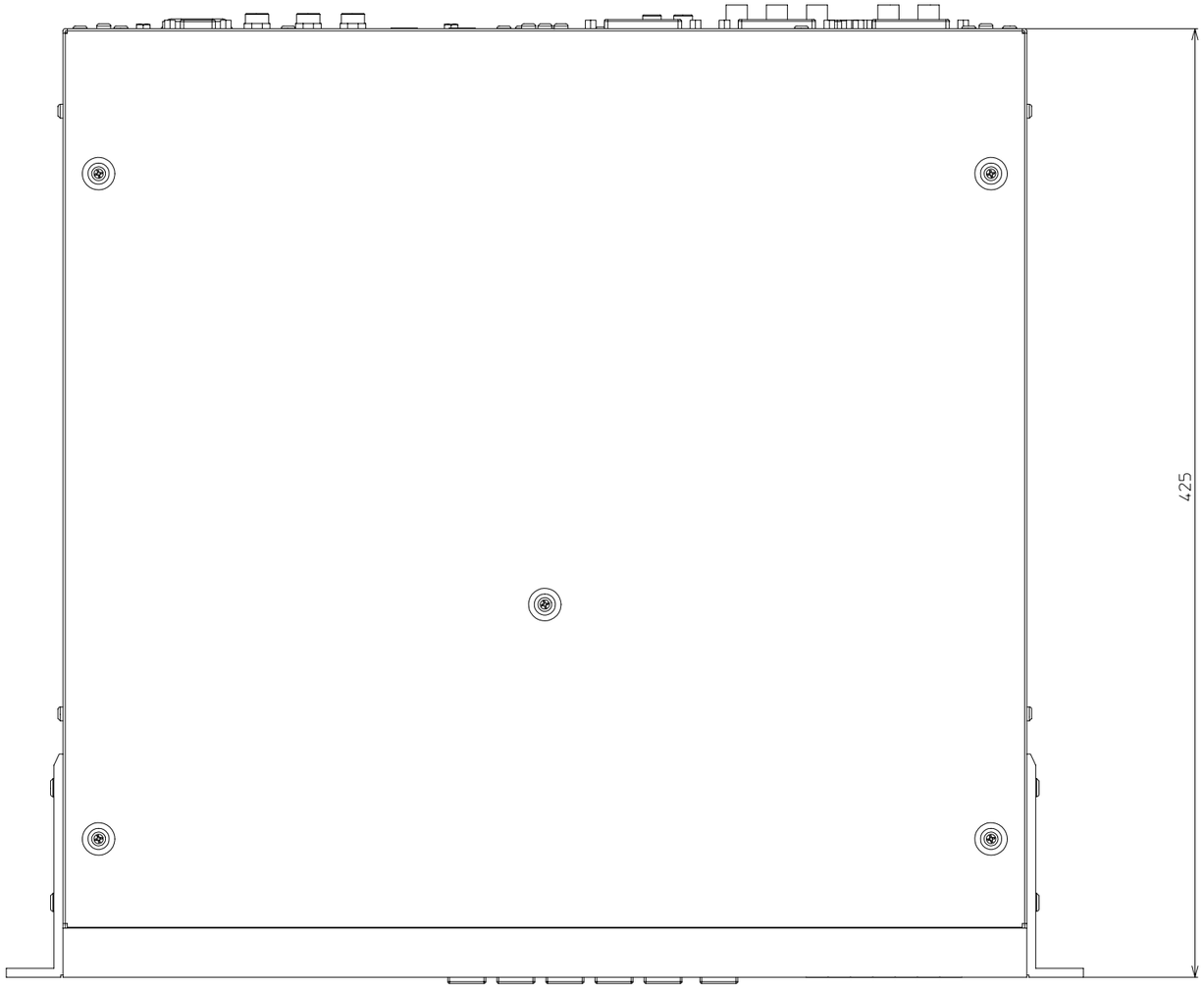
TRIG VARI

TRIG TIMEFIT

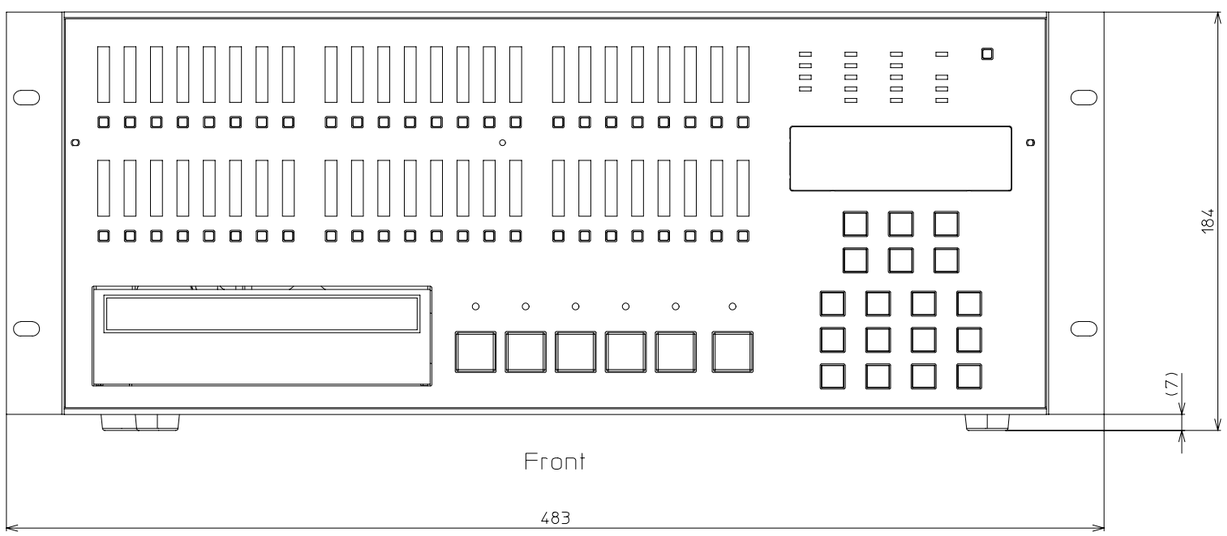
TMP Tape Motion Processes - (Non-Synchronous by definition)

PREROLL

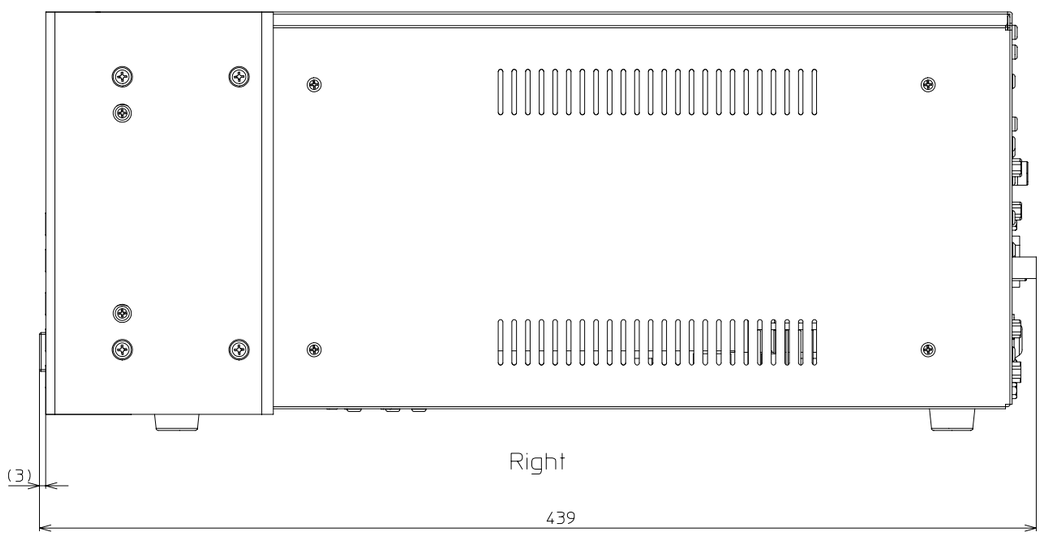
CUE WITH DATA



Top



Front



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