

DVD AUDIO/VIDEO SA-CD PLAYER

DVD-S1800

SERVICE MANUAL

DVD-S1800

IMPORTANT NOTICE

This manual has been provided for the use of authorized YAMAHA Retailers and their service personnel. It has been assumed that basic service procedures inherent to the industry, and more specifically YAMAHA Products, are already known and understood by the users, and have therefore not been restated.

WARNING: Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components, and failure of the product to perform as specified. For these reasons, we advise all YAMAHA product owners that any service required should be performed by an authorized YAMAHA Retailer or the appointed service representative.

IMPORTANT: The presentation or sale of this manual to any individual or firm does not constitute authorization, certification or recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of YAMAHA are continually striving to improve YAMAHA products. Modifications are, therefore, inevitable and specifications are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING: Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

IMPORTANT: Turn the unit OFF during disassembly and part replacement. Recheck all work before you apply power to the unit.

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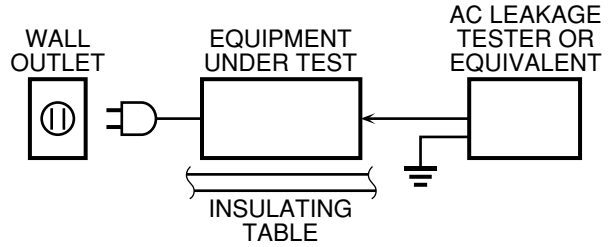
YAMAHA

YAMAHA CORPORATION
P.O.Box 1, Hamamatsu, Japan

'07.09

■ TO SERVICE PERSONNEL

1. Critical Components Information
Components having special characteristics are marked ⚠ and must be replaced with parts having specifications equal to those originally installed.
 2. Leakage Current Measurement (For 120V Models Only)
When service has been completed, it is imperative to verify that all exposed conductive surfaces are properly insulated from supply circuits.
- Meter impedance should be equivalent to 1500 ohms shunted by 0.15μF.



- Leakage current must not exceed 0.5mA.
- Be sure to test for leakage with the AC plug in both polarities.

WARNING: CHEMICAL CONTENT NOTICE!

This product contains chemicals known to the State of California to cause cancer, or birth defects or other reproductive harm.

DO NOT PLACE SOLDER, ELECTRICAL/ELECTRONIC OR PLASTIC COMPONENTS IN YOUR MOUTH FOR ANY REASON WHAT SO EVER!

Avoid prolonged, unprotected contact between solder and your skin! When soldering, do not inhale solder fumes or expose eyes to solder/flux vapor!

If you come in contact with solder or components located inside the enclosure of this product, wash your hands before handling food.

About lead free solder

All of the P.C.B.s installed in this unit and solder joints are soldered using the lead free solder.

Among some types of lead free solder currently available, it is recommended to use one of the following types for the repair work.

- Sn + Ag + Cu (tin + silver + copper)
- Sn + Cu (tin + copper)
- Sn + Zn + Bi (tin + zinc + bismuth)

Caution:

As the melting point temperature of the lead free solder is about 30°C to 40°C (50°F to 70°F) higher than that of the lead solder, be sure to use a soldering iron suitable to each solder.

WARNING: Laser Safety

This product contains a laser beam component. This component may emit invisible, as well as visible radiation, which may cause eye damage. To protect your eyes and skin from laser radiation, the following precautions must be used during servicing of the unit.

- 1) When testing and/or repairing any component within the product, keep your eyes and skin more than 30 cm away from the laser pick-up unit at all times. Do not stare at the laser beam at any time.
- 2) Do not attempt to readjust, disassemble or repair the laser pick-up, unless noted elsewhere in this manual.
- 3) CAUTION : Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Laser Emitting conditions:

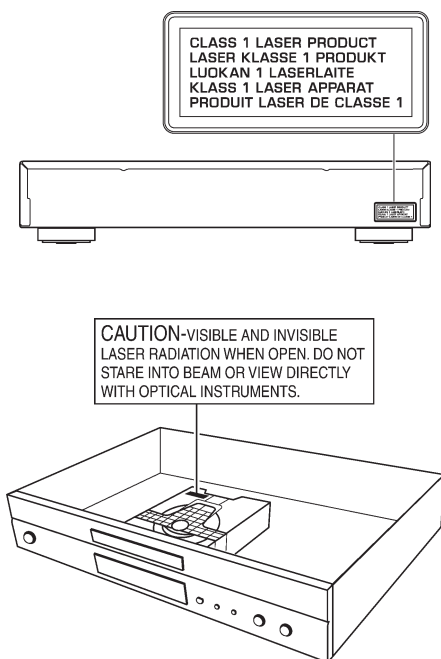
- 1) When the Top Cover is removed, and the STANDBY/ON SW is turned to the "ON" position, the laser component will emit a beam for several seconds to detect if a disc is present. During this time (5-10 sec.) the laser may radiate through the lens of the laser pick-up unit. Do not attempt any servicing during this period!
If no disc is detected, the laser will stop emitting the beam. When a disc is loaded, you will not be exposed to any laser emissions.
- 2) The laser power level can be adjusted with the VR on the pick-up PWB, however, this level has been set by the factory prior to shipping from the factory. Do not adjust this laser level control unless instruction is provided elsewhere in this manual. Adjustment of this control can increase the laser emission level from the device.

Laser Diode Properties

Type:	Semiconductor laser GaAlAs
Wave length:	650 nm (DVD) 790 nm (VCD/CD)
Output Power:	1.45 mW (DVD) 1.13 mW (VCD/CD)
Beam divergence:	60 degrees

VARO! : AVATTAESSA JA SUOJALUKITUS OHITETTAESSA OLET ALTTIINA NÄKYMÄTTÖMÄLLE LASER-SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN.

VARNING! : OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD OCH SPÄRREN ÄR URKOPPLAD. BETRakta EJ STRÅLEN.



CAUTION

VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN. AVOID EXPOSURE TO BEAM.

ADVARSEL

SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING. UNDGÅ UDSÆTTELSE FOR STRÅLING.

ADVARSEL

SYNLIG OG USYNLIG LASERSTRÅLING NÄR DEKSEL ÅPNES. UNNGÅ EKSPONERING FOR STRÅLEN.

VARNING

SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD. BETRakta EJ STRÅLEN.

VARO!

AVATTAESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄ TEILYLLE. ÄLÄ KATSO SÄTEESEEN.

VORSICHT

SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET. NICHT DEM STRAHL AUSSETZEN.

DANGER

VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN. AVOID DIRECT EXPOSURE TO BEAM.

ATTENTION

RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE. EXPOSITION DANGEREUSE AU FAISCEAU.

OSTRZEŻENIE

WIDZIALNE I NIEWIDZIALNE PROMIENIOWANIE LASEROWE PO OTWARCIU. UNIKAĆ NARAŻENIA NA WIĄZKĘ LASEROWĄ.

Warning for power supply

The primary side of the power supply carries live mains voltage when the player is connected to the mains even when the player is switched off !

This primary area is not shielded so it is possible to touch copper tracks and/or components when servicing the player. Service personnel have to take precautions to prevent touching this area or components in this area.

Note:

The screws on the DVD mechanism may never be touched, removed or re-adjusted.

Handle the DVD mechanism with care when the unit has to be exchanged!

The DVD mechanism is very sensitive for dropping or giving shocks.

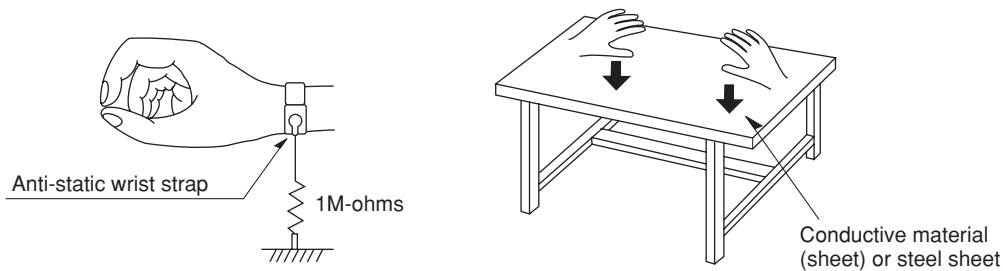
■ PREVENTION OF ELECTROSTATIC DISCHARGE

The laser diode in the DVD mechanism may be damaged due to static electricity from clothes or the human body. Use caution to prevent electrostatic damage when servicing or handling the DVD-mechanism.

1. Grounding for electrostatic damage prevention

Some devices, such as the DVD player, use an optical pickup (laser diode) that will be damaged by static electricity in the working environment. Only attempt service after ensuring that all grounding procedures have been completed.

1. Worktable grounding
Put a grounded conductive material (sheet) or iron sheet on the area where the optical pickup is placed.
2. Human body grounding
Use an anti-static wrist strap to discharge the static electricity from your body.



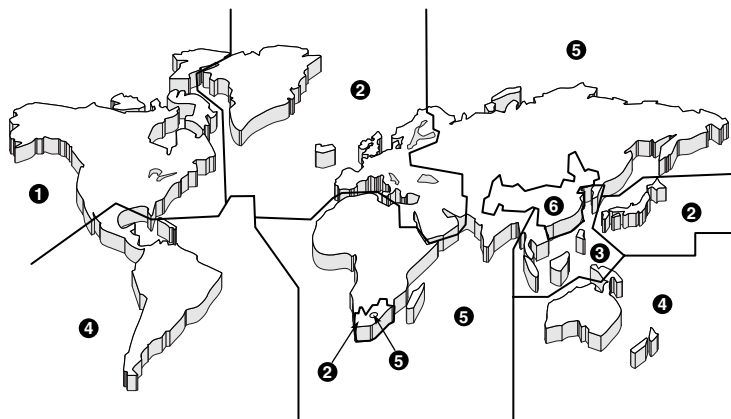
2. Handling Precautions for DVD mechanism

1. Handle the DVD mechanism gently, as it is an extremely high-precision assembly.
2. The flexible cable lines may break if an excessive force is applied to it. Use caution when handling the cable.
3. The semi-fixed resistor for laser power adjustment should not be adjusted. Do not turn the resistor.

■ LOCALE MANAGEMENT INFORMATION

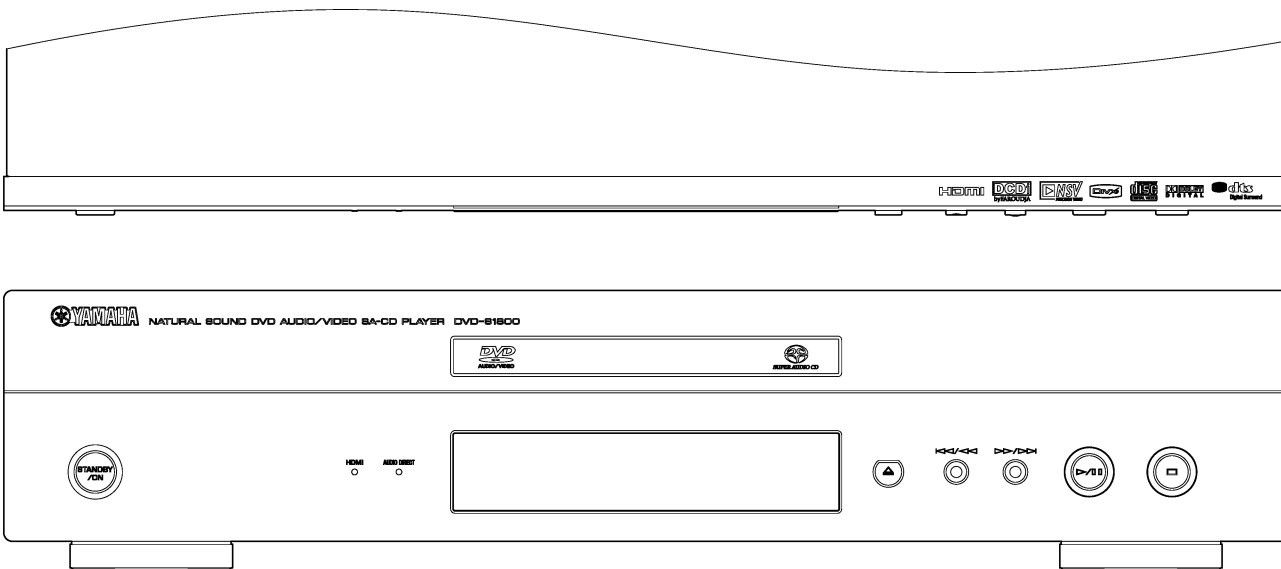
Locale Management Information : This DVD player is designed and manufactured to respond to the Locale Management Information that is recorded on a DVD disc. If the Locale number described on the DVD disc does not correspond to the Locale number of this DVD player, this DVD player cannot play this disc.

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FRONT PANEL

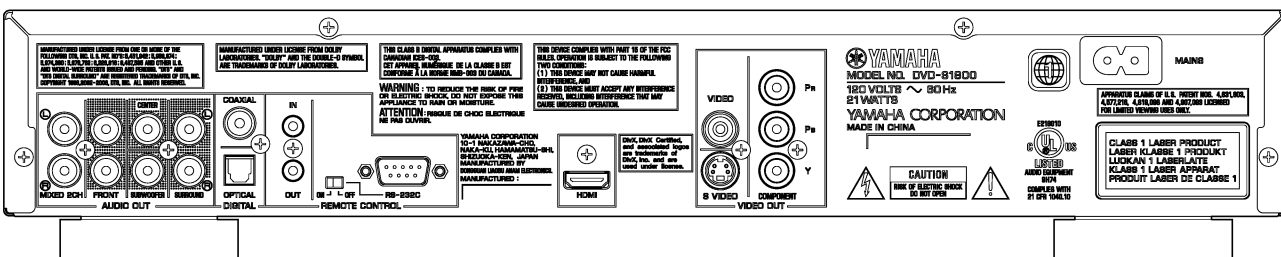
U, K, G, F, L models



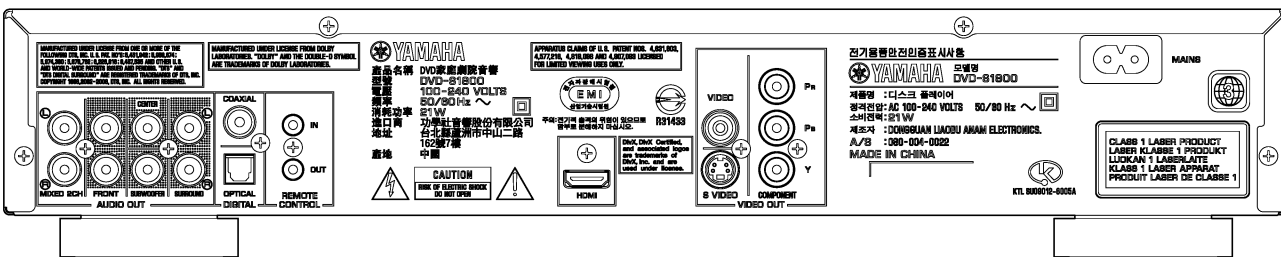
DVD-S1800

REAR PANELS

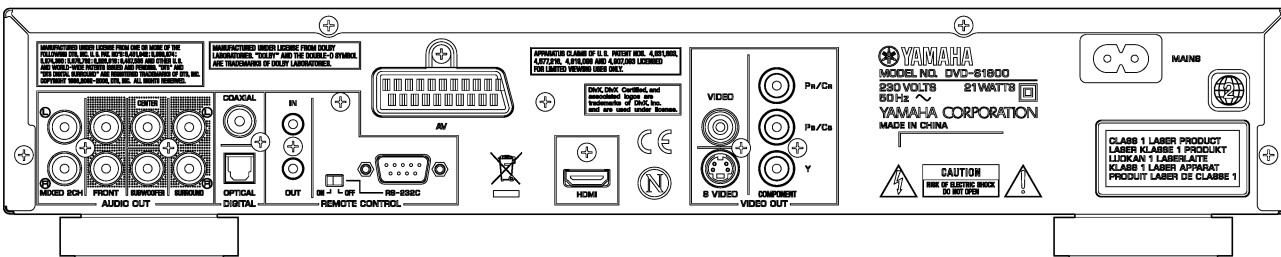
U model



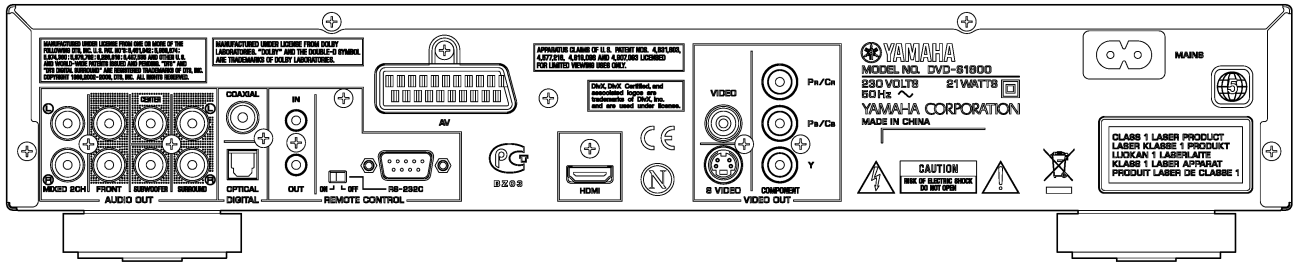
K model



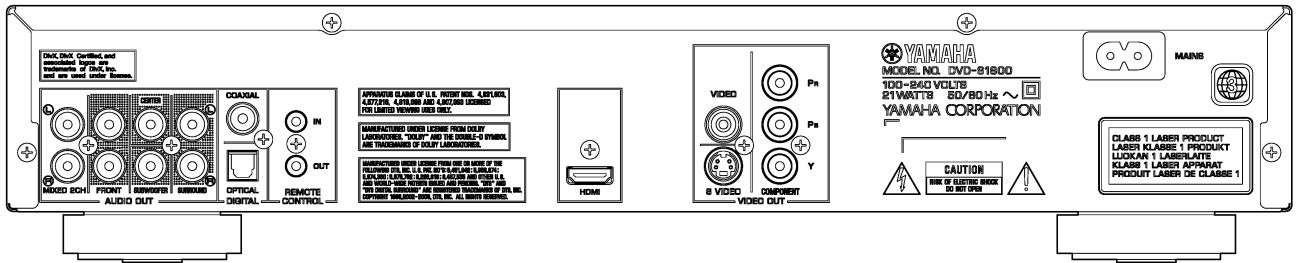
G model



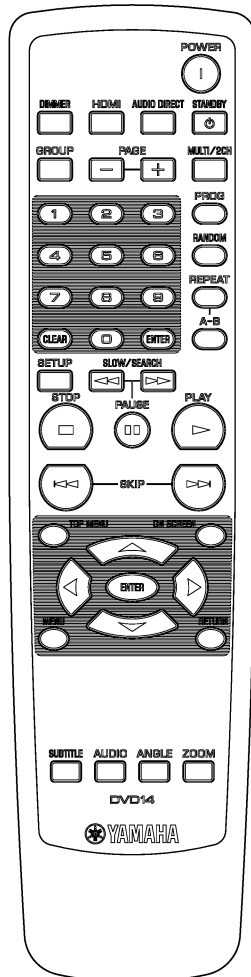
F model



L model



■ REMOTE CONTROL PANEL



■ SPECIFICATIONS

PLAYBACK SYSTEM

DVD-video
 DVD-audio
 DVD-R, DVD-RW
 DVD+R, DVD+RW, DVD+R DL
 Video CD, SVCD
 SA-CD multi-channel and SA-CD stereo
 CD
 Picture CD
 CD-R, CD-RW

VIDEO PERFORMANCE

Video (CVBS) output 1 Vpp into 75 ohms
 S-video output Y: 1 Vpp into 75 ohms
 C: 0.3 Vpp into 75 ohms
 Component video output Y: 1 Vpp into 75 ohms
 Pb/Cb, Pr/Cr: 0.7 Vpp into 75 ohms
 RGB (SCART) output (G, F models)
 0.7 Vpp into 75 ohms
 Black level shift (U model)
 On/Off

AUDIO FORMAT

Digital Dolby Digital/DTS/MPEG
 Compressed digital
 PCM 16, 20, 24 bits
 fs 44.1, 48, 88.2, 96 kHz
 MP3 (ISO 9660) 32 kbps to 320 kbps
 fs 16, 22.05, 24, 32, 44.1, 48 kHz
 WMA 64 kbps to 320 kbps
 mono, stereo
 Full decoding of Dolby Digital and DTS multi-channel sound
 Analog stereo sound
 Dolby surround compatible downmix from Dolby Digital multi-channel sound

AUDIO PERFORMANCE

DA converter 24 bits, 192 kHz
 Signal to noise (1 kHz) 115 dB
 Dynamic range (1 kHz) 105 dB
 DVD fs 96 kHz 2 Hz to 44 kHz
 fs 48 kHz 2 Hz to 22 kHz
 SVCD fs 48 kHz 2 Hz to 22 kHz
 fs 44.1 kHz 2 Hz to 20 kHz
 CD/VCD fs 44.1 kHz 2 Hz to 20 kHz
 Distortion and noise (1 kHz) 0.002 %

TV STANDARD

Number of lines PAL: 625, NTSC: 525
 Vertical frequency PAL: 50 Hz, NTSC: 60 Hz
 Playback Multistandard (PAL/NTSC)

CONNECTIONS

Video output Cinch (yellow) x 1
 S-video output Mini DIN, 4 pins x 1
 Component video output
 Y output Cinch (green) x 1
 Pb/Cb output Cinch (blue) x 1
 Pr/Cr output Cinch (red) x 1
 SCART (G, F models) Euroconnector x 1
 Digital output Coaxial x 1
 Optical x 1
 IEC60958 for CDDA/LPCM,
 IEC61937 for MPEG 1/2,
 Dolby Digital and DTS
 HDMI (Ver. 1.1) Type A x 1
 IEC60958 for CDDA/LPCM,
 IEC61937 for MPEG 1/2,
 Dolby Digital and DTS, PCM
 (PPCM) multi/2ch (DVD-audio)
 Audio output
 2 channel analog output
 MIXED 2CH L/R Cinch (white/red) x 1 pair
 Multi channel analog output
 FRONT L/R Cinch (white/red) x 1 pair
 SURROUND L/R Cinch (white/red) x 1 pair
 CENTER Cinch (black) x 1
 SUBWOOFER Cinch (black) x 1

GENERAL

Dimensions (W x H x D) 435 x 87 x 284.5 mm
 (17-1/8" x 3-7/16" x 11-3/16")
 Weight 3.3 Kg (7 lbs. 4 oz)
 Finish Gold color (K model)
 Black color (U, G, F models)
 Titanium color (G, F, L models)
 Power supply AC 120 V, 60 Hz (U model)
 AC 100-240 V, 50/60 Hz
 (K, L models)
 AC 230 V, 50 Hz (G, F models)
 Power consumption Approx. 21 W
 Standby power consumption < 0.5 W

ACCESSORIES

Remote control x 1
 Battery (AAA, R03, UM-4) x 2
 Power cable (2 m) x 1 (U, G, F, L models)
 Power cable (2 m) x 2 (K model)
 Video pin cable (1 m) x 1
 Audio pin cable (1 m) x 1

* Specifications are subject to change without prior notice.

U U.S.A. model
 K Korean model
 G European model
 F Russian model
 L Singapore model



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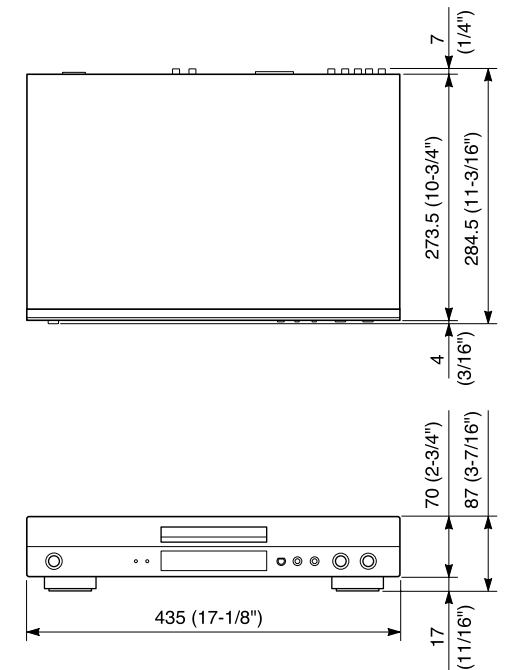
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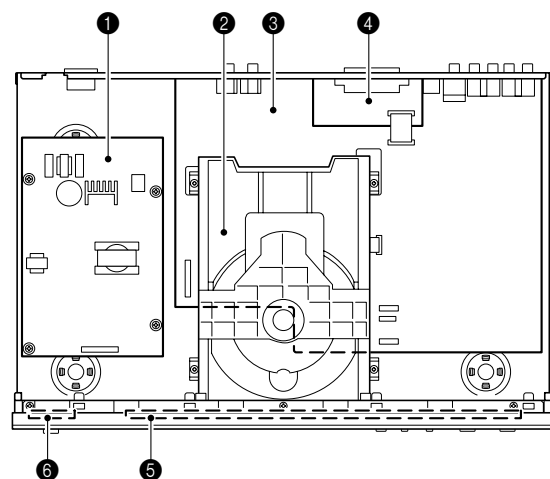
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• DIMENSIONS



Unit: mm (inch)

INTERNAL VIEW



- ❶ POWER SUPPLY UNIT
- ❷ DVD MECHANISM UNIT
- ❸ MAIN (1) P.C.B.
- ❹ MAIN (4) P.C.B. (G, F models)
- ❺ FRONT (1) P.C.B.
- ❻ FRONT (2) P.C.B.

TRADE MODE

In the TRADE mode, the tray open/close function is stopped temporarily.

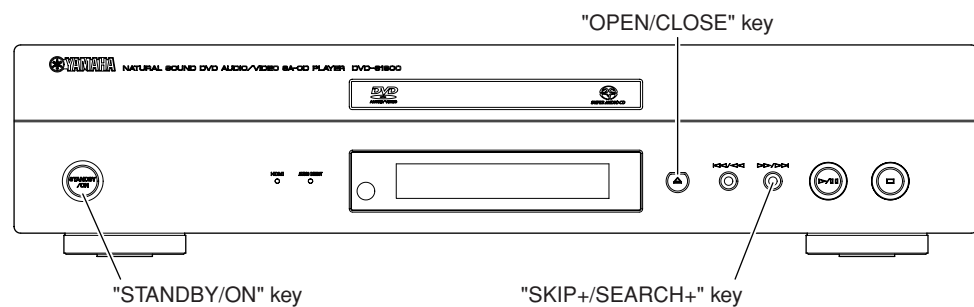
Setting TRADE mode

1. Connect the power cable of the main unit to the AC outlet.
2. Press the "STANDBY/ON" key of the main unit or remote controller to turn on the power.
3. Press the "OPEN/CLOSE" key of the main unit to open the tray.
4. Place a disc in the tray and press the "OPEN/CLOSE" key of the main unit to close the tray.
5. While pressing the "SKIP+/SEARCH+" key of the main unit and press the "STOP" key for 3 seconds or longer.
6. When the TRADE mode is set, [TRADE ON] is displayed which then returns to the normal display.

Note: Even after the TRADE mode is set, all functions remain the same as normal except the "OPEN/ CLOSE" key. Press the "OPEN/CLOSE" key, and [TRAY LOCKED] is displayed.

Canceling TRADE mode

1. Press the "STOP" key to discontinue reproduction.
2. While pressing the "SKIP+/SEARCH+" key of the main unit and press the "STOP" key for 3 seconds or longer.
3. When the TRADE mode is cancelled, [TRADE OFF] is displayed which then returns to the normal display.



ERROR MESSAGE

Display	Cause
NO DISC	When no disc is loaded in the tray.
UNKNOWN DISC	When a disc which cannot be played or recognized is loaded in the tray.

TROUBLESHOOTING

HDMI Reset

When no picture is displayed even though the main unit and TV monitor are connected with the HDMI cable

1. Press the "STOP" key of the main unit or on the remote control twice.
2. While pressing the "STOP" key of the main unit, press the "PLAY/PAUSE" key for 3 seconds or longer.
3. [HDMI RESET] is displayed of the main unit which then returns to the normal display.

VIDEO Reset

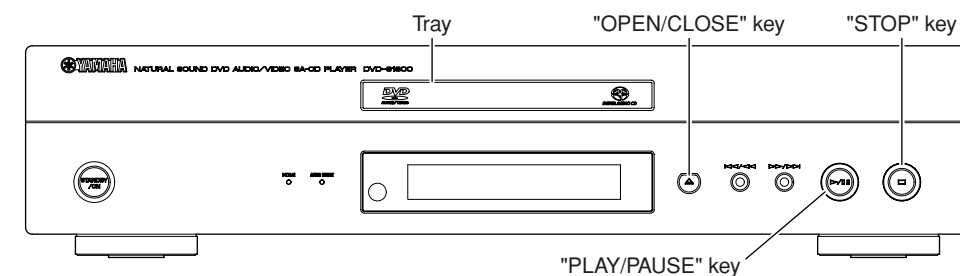
When no picture is displayed or picture is displayed but not properly even though the main unit and TV monitor are connected with the video pin cable or the like

1. Press the "OPEN/CLOSE" key to open the tray.
2. Press the "CLEAR" key on the remote control.
3. Press the "2", "5", "8" and "0" keys on the remote control.
4. Press the "AUDIO" key on the remote control.

Remote control



Main unit



MEMO



DVD-S1800



DISASSEMBLY PROCEDURES

(Remove parts in disassembly order as numbered.)
 Disconnect the power cable from the AC outlet.

1. Removal of Top Cabinet

- a. Remove 6 screws (①). (Fig. 1)
- b. Lift up the rear side of the top cover, then remove rearward. (Fig. 1)

2. Removal of DVD Mechanism Unit

- a. Eject the tray. (See "How to manually eject the tray".)
- b. Remove the tray lid upward and close the tray. (Fig. 1)
- c. Remove 2 screws (②). (Fig. 1)
- d. Turn the traverse gear in the arrow direction until the P.C.B. of the DVD mechanism unit is seen. (Fig. 2)
- e. Solder the lands in the P.C.B. of the DVD mechanism unit with the anti-static soldering iron. (Fig. 2)

Note

- After you have finished repairing , connect the flexible flat cable to CN11 in advance and then remove the solder from the short-circuit location with the anti-static soldering iron.

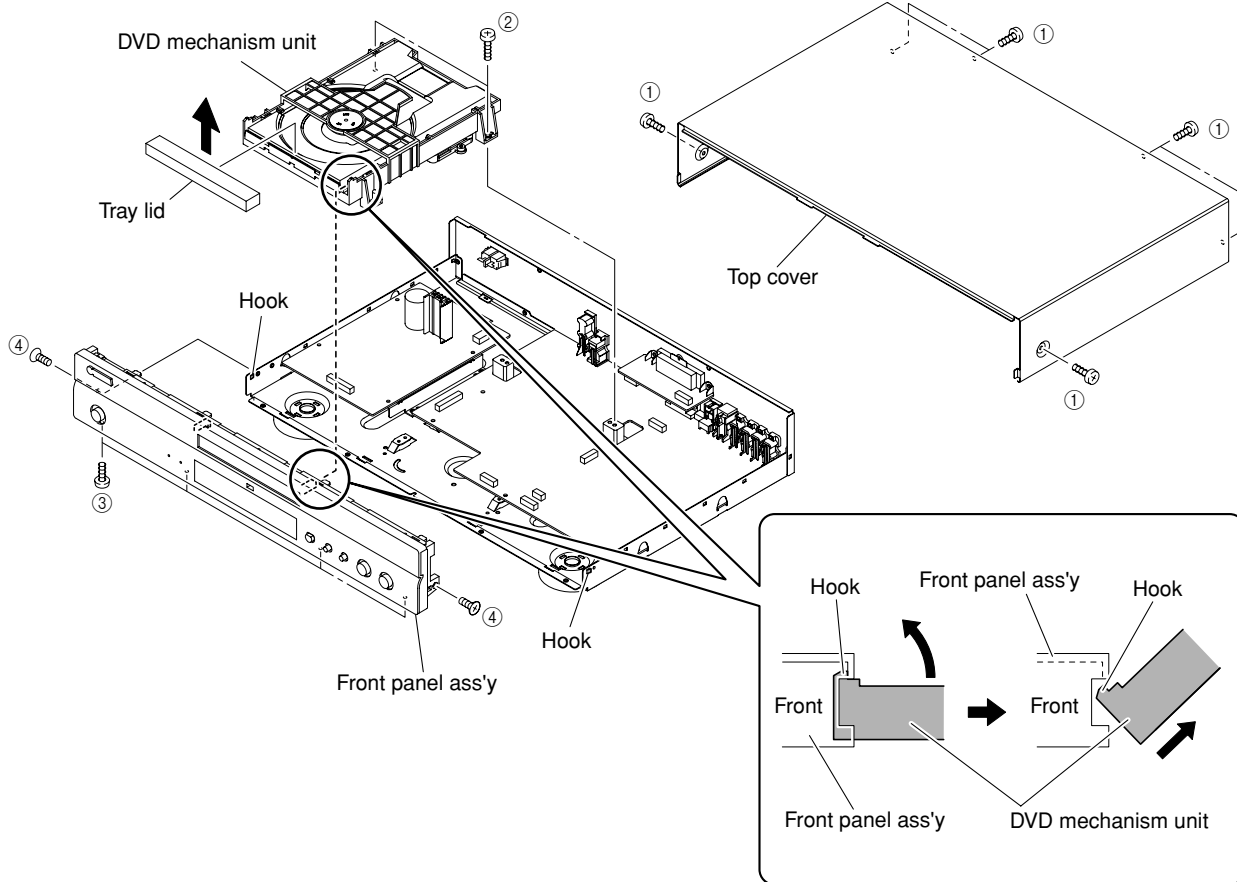


Fig. 1

- e. Remove CN11, CN12 and CN13. (Fig. 2)
- f. Lift up the rear side of the DVD mechanism unit, then remove 2 hooks and remove rearward. (Fig. 1)

3. Removal of Front Panel Ass'y

- a. Remove 4 screws (③). (Fig. 1)
- b. Remove 2 screws (④). (Fig. 1)
- c. Remove CX41. (Fig. 2)
- d. Remove 2 hooks and then remove the front panel ass'y forward. (Fig. 1)

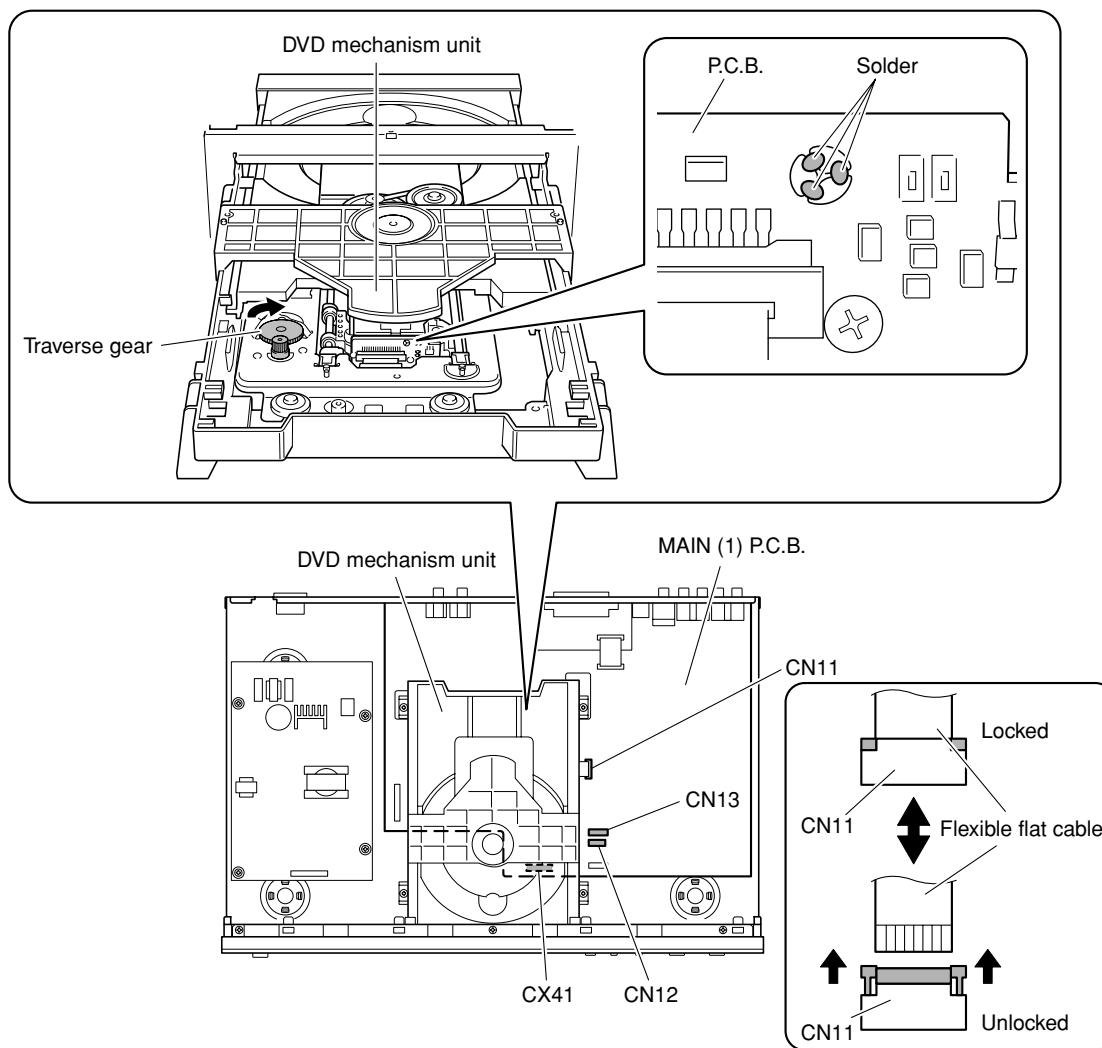
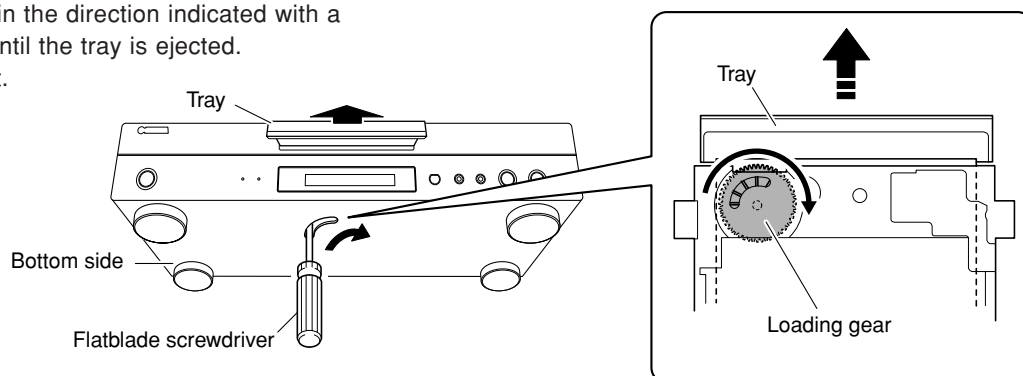


Fig. 2

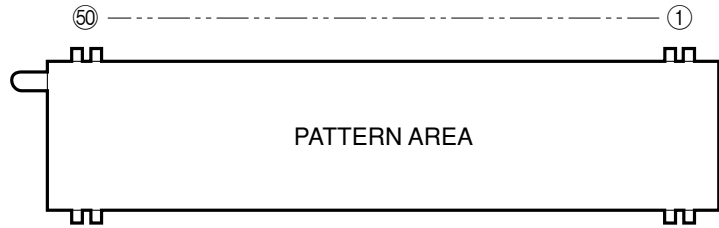
• How to manually eject the tray

- a. Turn the loading gear in the direction indicated with a flatblade screwdriver until the tray is ejected.
- b. Gently pull the tray out.



■ DISPLAY DATA

● F401 : HCA14SM16 (FRONT P.C.B.)



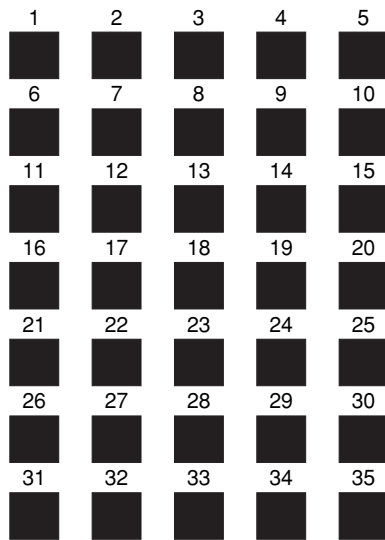
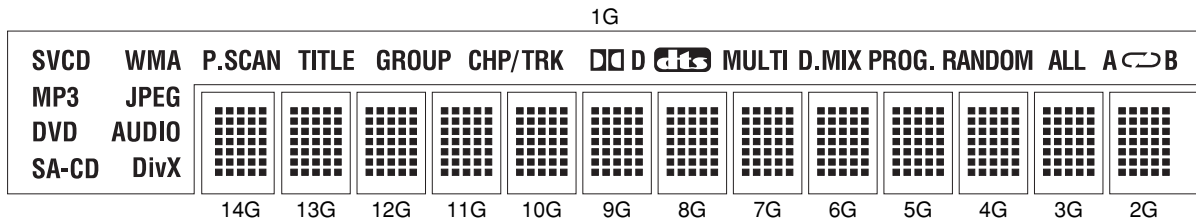
● PIN CONNECTION

Pin No.	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
Connection	F2	F2	NP	NP	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX

Pin No.	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Connection	NX	NX	NX	NX	NX	NX	NX	NX	NX	1G	NC	GR1	VDD	DIN	CLKB	CSB	RSTB	OSCO	OSCI	VEE	GND	NP	NP	F1	F1

Note : 1) F1, F2 Filament pin 2) NP No pin 3) NC No connection 4) NX No extended pin




● GRID ASSIGNMENT



(2G-14G)

DVD-S1800

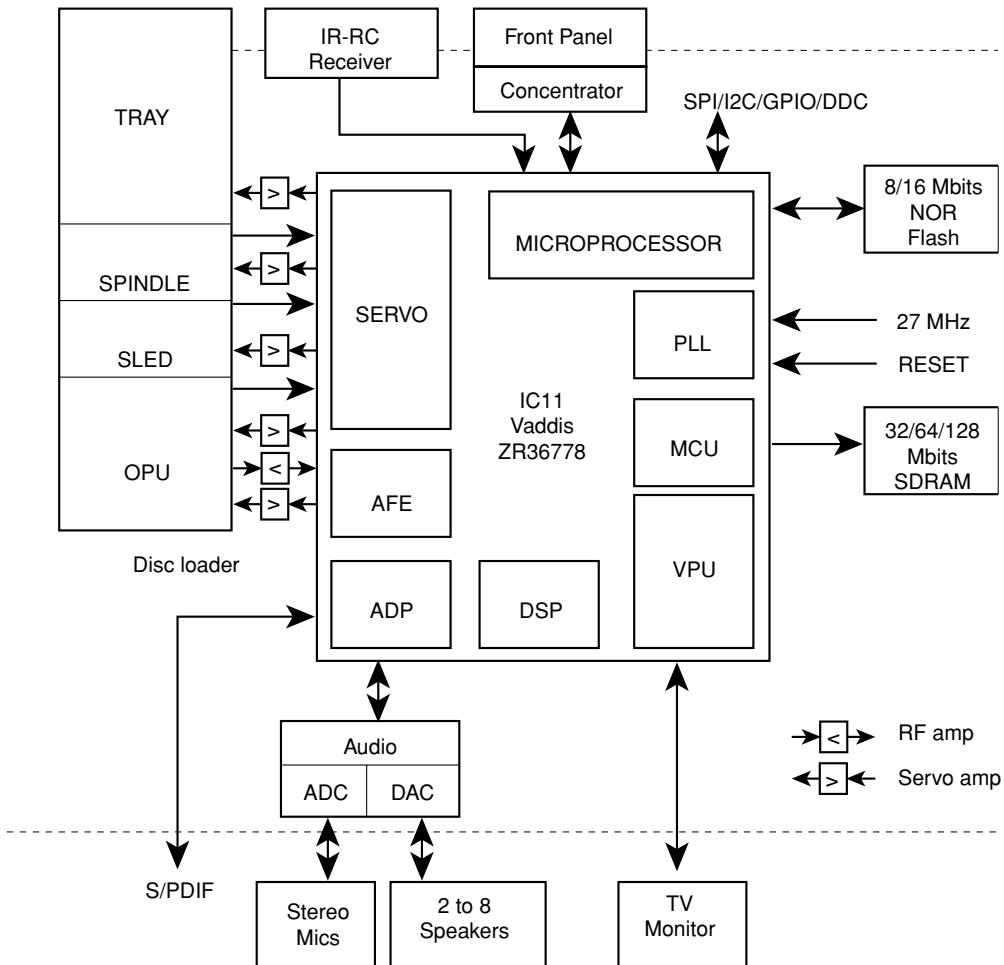
● ANODE CONNECTION

	GR14	GR13	GR12	GR11	GR10	GR9	GR8	GR7	GR6	GR5	GR4	GR3	GR2	GR1
	14G	13G	12G	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G
SG1	1	1	1	1	1	1	1	1	1	1	1	1	1	B
SG2	2	2	2	2	2	2	2	2	2	2	2	2	2	
SG3	3	3	3	3	3	3	3	3	3	3	3	3	3	A
SG4	4	4	4	4	4	4	4	4	4	4	4	4	4	ALL
SG5	5	5	5	5	5	5	5	5	5	5	5	5	5	RANDOM
SG6	6	6	6	6	6	6	6	6	6	6	6	6	6	PROG.
SG7	7	7	7	7	7	7	7	7	7	7	7	7	7	D.MIX
SG8	8	8	8	8	8	8	8	8	8	8	8	8	8	MULTI
SG9	9	9	9	9	9	9	9	9	9	9	9	9	9	
SG10	10	10	10	10	10	10	10	10	10	10	10	10	10	
SG11	11	11	11	11	11	11	11	11	11	11	11	11	11	
SG12	12	12	12	12	12	12	12	12	12	12	12	12	12	CHP/TRK
SG13	13	13	13	13	13	13	13	13	13	13	13	13	13	GROUP
SG14	14	14	14	14	14	14	14	14	14	14	14	14	14	TITLE
SG15	15	15	15	15	15	15	15	15	15	15	15	15	15	P.SCAN
SG16	16	16	16	16	16	16	16	16	16	16	16	16	16	WMA
SG17	17	17	17	17	17	17	17	17	17	17	17	17	17	JPEG
SG18	18	18	18	18	18	18	18	18	18	18	18	18	18	AUDIO
SG19	19	19	19	19	19	19	19	19	19	19	19	19	19	CD
SG20	20	20	20	20	20	20	20	20	20	20	20	20	20	V
SG21	21	21	21	21	21	21	21	21	21	21	21	21	21	S
SG22	22	22	22	22	22	22	22	22	22	22	22	22	22	MP3
SG23	23	23	23	23	23	23	23	23	23	23	23	23	23	DVD
SG24	24	24	24	24	24	24	24	24	24	24	24	24	24	DivX
SG25	25	25	25	25	25	25	25	25	25	25	25	25	25	SA-CD
SG26	26	26	26	26	26	26	26	26	26	26	26	26	26	
SG27	27	27	27	27	27	27	27	27	27	27	27	27	27	
SG28	28	28	28	28	28	28	28	28	28	28	28	28	28	
SG29	29	29	29	29	29	29	29	29	29	29	29	29	29	
SG30	30	30	30	30	30	30	30	30	30	30	30	30	30	
SG31	31	31	31	31	31	31	31	31	31	31	31	31	31	
SG32	32	32	32	32	32	32	32	32	32	32	32	32	32	
SG33	33	33	33	33	33	33	33	33	33	33	33	33	33	
SG34	34	34	34	34	34	34	34	34	34	34	34	34	34	
SG35	35	35	35	35	35	35	35	35	35	35	35	35	35	

DVD-S1800

IC DATA

IC11: ZR36778 (MAIN P.C.B.)
MPEG decoder



No.	Pin Functions	Direction	Description
1	SSCRXD	I	SSC data input
	GPCI/O[17]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP or FCU SW
	PM[15]	O	Probe mux data output
2	MEMCS[1]#	O	PNVM/SRAM chip select (active low) output
	GPCI/O[18]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW
3	VDDP	S	3.3 V digital periphery power supply
4,5	MEMAD [15,16]	O	PNVM/SRAM address bus outputs
	SYSIND[1,0]	I	General purpose system configuration indication input / Level sampled during RESET
6	MEMAD[14]	O	PNVM/SRAM address bus output
	GCLKSEL	I	GCLKPOUT or GCLKA function selection / Level sampled during RESET
7	MEMAD[13]	O	PNVM/SRAM address bus output
	FCUIF[29]	O	Flash card interface unit output signal
8	MEMAD[12]	O	PNVM/SRAM address bus output
	PLLCFGGA	I	Audio PLL configuration input / Level sampled during RESET / In normal operation the pin must be low during RESET
9	MEMDA[15]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[28]	I/O	Flash card interface unit I/O signal
10	MEMAD[11]	O	PNVM/SRAM address bus output
	PLLCFGP	I	Process PLL configuration input / Level sampled during RESET / In normal operation the pin must be low during RESET
11	MEMDA[7]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[9]	I/O	Flash card interface unit I/O signals
12	GNDP	S	Digital periphery ground of 3.3 V supply
13	MEMAD[10]	O	PNVM/SRAM address bus output
	FCUIF[20]	O	Flash card interface unit output signal
14	MEMDA[14]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[27]	I/O	Flash card interface unit I/O signal
15	MEMAD[9]	O	PNVM/SRAM address bus outputs
	FCUIF[19]	O	Flash card interface unit output signal
16	MEMDA[6]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[8]	I/O	Flash card interface unit I/O signals
17	MEMAD[8]	O	PNVM/SRAM address bus outputs
	FCUIF[18]	O	Flash card interface unit output signal
18-19	MEMDA[13,5]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[26,7]	I/O	Flash card interface unit I/O signals
20	MEMAD[20]	O	PNVM/SRAM address bus outputs
	MEMCS[2]#	O	PNVM/SRAM chip select (active low) output
21	GPCI/O[19]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW
	VDDP	S	3.3 V digital periphery power supply
22	MEMDA[12]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[25]	I/O	Flash card interface unit I/O signal
23	MEMWR#	O	PNVM/SRAM write enable (active low) output
	FCUIF[0]	O	Flash card interface unit output signal
24	MEMDA[4]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[6]	O	Flash card interface unit output signal
25	VDDC	S	1.8 V digital core power supply
26	MEMDA[11]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[24]	I/O	Flash card interface unit I/O signal
27	MEMDA[3]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[5]	I/O	Flash card interface unit I/O signals
28	MEMAD[19]	O	PNVM/SRAM address bus outputs
	PLLSEL	I	PLL frequency selection -108 MHz (low) or 135 MHz (high) / Level sampled during RESET
29	GNDC	S	Digital core ground of 1.8 V supply
30	MEMDA[10]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[23]	I/O	Flash card interface unit I/O signal
31	MEMAD[18]	O	PNVM/SRAM address bus output
32	GNDP	S	Digital periphery ground of 3.3 V supply
33	MEMDA[2]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[4]	I/O	Flash card interface unit I/O signals
34	MEMAD[17]	O	PNVM/SRAM address bus output
35	MEMDA[9]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[22]	I/O	Flash card interface unit I/O signal
36	MEMAD[7]	O	PNVM/SRAM address bus outputs
	FCUIF[17]	O	Flash card interface unit output signal
37	MEMDA[1]	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[3]	I/O	Flash card interface unit I/O signals
38	MEMAD[6]	O	PNVM/SRAM address bus outputs

No.	Pin Functions	Direction	Description
	FCUIF[16]	O	Flash card interface unit output signal
39	MEMDA[8] FCUIF[21]	I/O I/O	PNVM/SRAM bi-directional data bus Flash card interface unit I/O signal
40	MEMAD[5] FCUIF[15]	O O	PNVM/SRAM address bus outputs Flash card interface unit output signal
41	VDDP	S	3.3 V digital periphery power supply
42	MEMDA[0] FCUIF[2]	I/O O	PNVM/SRAM bi-directional data bus Flash card interface unit output signal
43	MEMAD[4] FCUIF[14]	I/O O	PNVM/SRAM address bus outputs Flash card interface unit output signal
44	MEMRD# FCUIF[1]	O I/O	PNVM/SRAM read enable (active low) output Flash card interface unit I/O signal
45-46	MEMAD[3, 2] FCUIF[13, 12]	O O	PNVM/SRAM address bus outputs Flash card interface unit output signal
47	MEMCS[0]#	O	PNVM/SRAM chip select (active low) output
48	MEMAD[1] FCUIF[11] BOOTSEL[2]	O O I	PNVM/SRAM address bus outputs Flash card interface unit output signals Microprocessor SW boot (and execute) source selection: (high, high) - For production testing; (high, low) - Flash+SRAM (for debug monitor); (low, high) - First debug UART (low, low) - Flash (low) or Level sampled during RESET
49	MEMAD[0] FCUIF[10] BOOTSEL[1]	O O I	PNVM/SRAM address bus outputs Flash card interface unit output signals Microprocessor SW boot (and execute) source selection: (high, high) - For production testing; (high, low) - Flash+SRAM (for debug monitor); (low, high) - First debug UART (low, low) - Flash (low) or Level sampled during RESET
50	GNDP	S	Digital periphery ground of 3.3 V supply
51	VDD-IP	S	3.3 V periphery reference voltage
52	VDDP	S	3.3 V digital periphery power supply
53-57	RAMADD [4, 3, 5, 2, 6]	O	SDRAM address bus output
58	VDDP	S	3.3 V digital periphery power supply
59-61	RAMADD [1, 7, 0]	O	SDRAM address bus output
62	GNDP	S	Digital periphery ground of 3.3 V supply
63	RAMADD[8]	O	SDRAM address bus output
64	VDDC	S	1.8 V digital core power supply
65	RAMADD[10]	O	SDRAM address bus output
66	GNDC	S	Digital core ground of 1.8 V supply
67	RAMADD[9]	O	SDRAM address bus output
68	VDDP	S	3.3 V digital periphery power supply
69	RAMADD[11]	O	SDRAM address bus output
70	RAMCS[0]# RAMBA[1]	O O	SDRAM chip select (active low) SDRAM bank select output
71	RAMBA[0]	O	SDRAM bank select output
72	GNDP	S	Digital periphery ground of 3.3 V supply
73	RAMCS[1]#	O	SDRAM chip select (active low) output
74	RAMRAS#	O	SDRAM row select (active low) output
75	RAMCAS#	O	SDRAM column select (active low) output
76	VDDP	S	3.3 V digital periphery power supply
77	RAMWE#	O	SDRAM write enable (active low) output
78	RAMDQM	O	SDRAM data masking (active high) output
79	GNDPCLK	S	Digital ground of filtered 3.3 V supply for PCLK
80	PCLK	O	SDRAM clock output (same as internal processing clock)
81	VDDPCLK	S	3.3 V filtered digital power supply for PCLK
82	RAMDAT[8]	I/O	SDRAM bi-directional data bus
83	GNDP	S	Digital periphery ground of 3.3 V supply
84-86	RAMDAT [7, 9, 6]	I/O	SDRAM bi-directional data bus
87	VDDP	S	3.3 V digital periphery power supply
88-90	RAMDAT [10, 5, 11]	I/O	SDRAM bi-directional data bus
91	GNDP	S	Digital periphery ground of 3.3 V supply

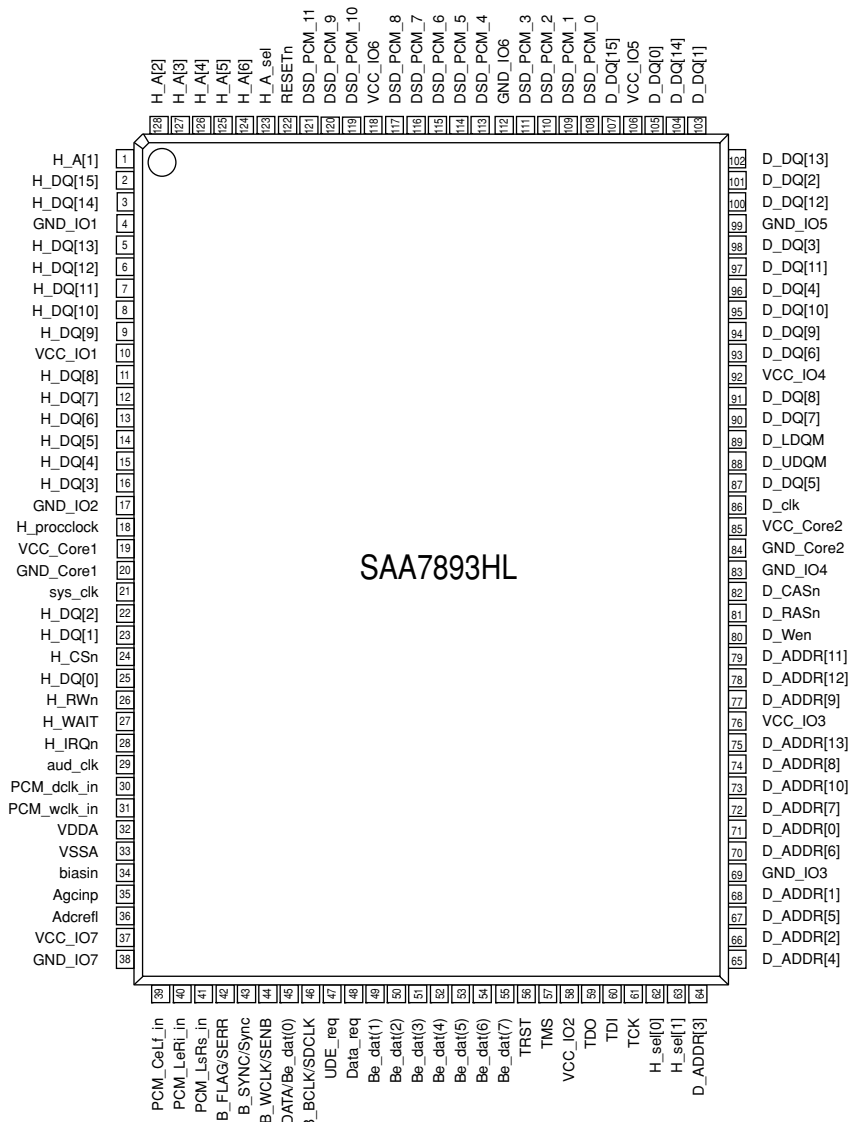
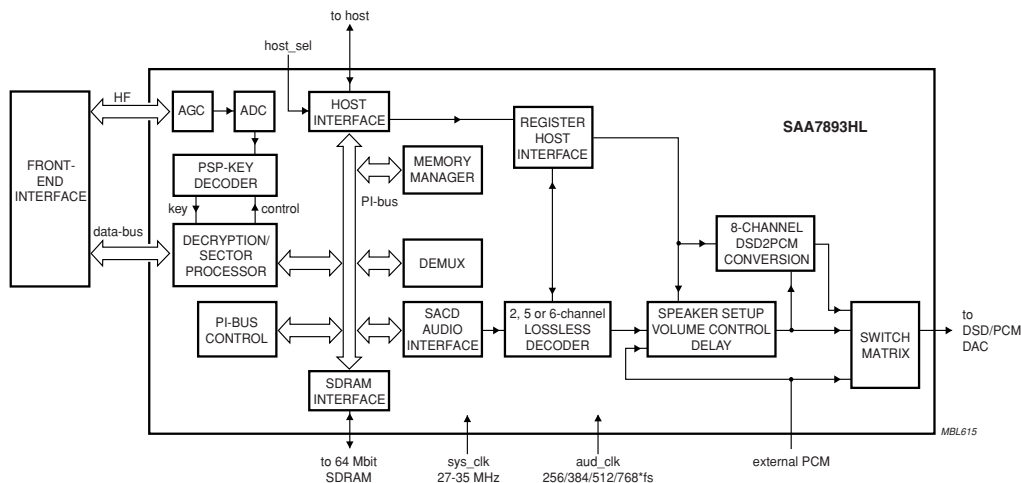
No.	Pin Functions	Direction	Description
92	RAMDAT[4]	I/O	SDRAM bi-directional data bus
93	VDDC	S	1.8 V digital core power supply
94	RAMDAT[12]	I/O	SDRAM bi-directional data bus
95	GNDC	S	Digital core ground of 1.8 V supply
96	RAMDAT[3]	I/O	SDRAM bi-directional data bus
97	VDDP	S	3.3 V digital periphery power supply
98-100	RAMDAT [13, 2, 14]	I/O	SDRAM bi-directional data bus
101	GNDP	S	Digital periphery ground of 3.3 V supply
102-104	RAMDAT [1, 15, 0]	I/O	SDRAM bi-directional data bus
105	VDDP	S	3.3 V digital periphery power supply
106	GPCI/O[20] CPUNMI SDATA[0] PM[0]	I/O I I O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW Microprocessor non-maskable interrupt input SERVO channel sample data input for AFE by-pass Probe mux data output
107	GNDP	S	Digital periphery ground of 3.3 V supply
108	ICGPCI/O[0] AOUT[3] SDATA[1] PM[1]	I/O O I O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the microprocessor Serial output of digital stereo audio SERVO channel sample data input for AFE by-pass Probe mux data output
109	IDGPCI/O[0] RAMCKE SDATA[2] PM[2]	I/O O I O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the DSP Clock enable signal to the SDRAM (for power down) SERVO channel sample data input for AFE by-pass Probe mux data output
110	S/PDIFOUT SDATA[3] PM[3]	O I O	S/PDIF transmitter output for digital coded or reconstructed audio data SERVO channel sample data input for AFE by-pass Probe mux data output
111	AOUT[2] GPCI/O[21] SDATA[4] PM[4]	O I/O I O	Serial outputs of digital stereo audio General purpose I/O, monitored/controlled by the microprocessor or DSP SW SERVO channel sample data inputs for AFE by-pass Probe mux data outputs
112	AOUT[1] GPCI/O[22] PM[5]	O I/O O	Serial output of digital stereo audio General purpose I/O, monitored/controlled by the microprocessor or DSP SW Probe mux data outputs
113	AOUT[0] SDATA[6] PM[6]	O I O	Serial output of digital stereo audio SERVO channel sample data input for AFE by-pass Probe mux data outputs
114	GPAI/O AOUT[3] IDGPCI/O[0] PM[7]	I/O O I/O O	General purpose I/O, monitored/controlled by the ADP SW Serial output of digital stereo audio General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the DSP Probe mux data output
115	ALRCLK	O	Digital audio left/right select output for the audio port / Square wave, at the sampling frequency / Programmable polarity
116	ABCLK	O	Digital audio bit-clock output / Data on AOUT and AIN is output or latched, respectively, with the rising or falling (programmable) edge of this clock
117	GNDP-A2	S	Digital ground filtered 3.3 V supply for AMCLK
118	AMCLK	I/O	Audio master clock I/O / 128, 192, 256 or 384 times the sampling frequency (programmable)
119	VDDP-A2	S	3.3 V filtered digital power supply for AMCLK
120	AIN GPCI/O[23] PM[8]	I I/O O	Serial input of digital stereo audio General purpose I/O, monitored/controlled by the microprocessor or DSP SW Probe mux data output
121	GNDC	S	Digital core ground of 1.8 V supply
122	VSYNC# HDFI GPI/O[24] DACTEST[9] PM[9]	O I I/O I O	SD digital video vertical sync output signal HD digital video field index input signal General purpose I/O, monitored/controlled by the microprocessor or DSP SW DACs test input Probe mux data output
123	VDDC	S	1.8 V digital core power supply
124	HSYNC# HDHS GPCI/O[25]	O I I/O	SD digital video horizontal sync output signal HD digital video horizontal sync input signal General purpose I/O, monitored/controlled by the microprocessor or DSP SW
125	GNDP	S	Digital periphery ground of 3.3 V supply
126	VCLKx2	O	Digital video clock output / 27,000 (for SD interlaced), 54,000 (SD progressive) or 135,000 (for HD) MHz

No.	Pin Functions	Direction	Description
	COSYNC ICGPCI/O[1]	O I/O	Composite sync output / Active only when component analog output is selected General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the microprocessor
127	VDDP	S	3.3 V digital periphery power supply
128	VID[7] GPCI/O[26]	O I/O	Digital 4: 2: 2 video luma/chroma output, interleaved U, Y V Y General purpose I/O, monitored/controlled by the microprocessor or DSP SW
129	VID[6] ICGPCI/O[2]	O I/O	Digital 4: 2: 2 video luma/chroma output, interleaved U, Y V Y General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the microprocessor
130	VID[5] IDGPCI[1]	O I/O	Digital 4: 2: 2 video luma/chroma output, interleaved U, Y V Y General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the DSP
131	GNDP	S	Digital periphery ground of 3.3 V supply
132	VID[4] GPCI/O[27]	O I/O	Digital 4: 2: 2 video luma/chroma output, interleaved U, Y V Y General purpose I/O, monitored/controlled by the microprocessor or DSP SW
133	VID[3] GPCI/O[28] SERVOCLK	O I/O O	Digital 4: 2: 2 video luma/chroma output, interleaved U, Y V Y General purpose I/O, monitored/controlled by the microprocessor or DSP SW SERVO channel clock output for AFE by-pass
134	VID[2] GPCI/O[29] SSEL[0]	O I/O O	Digital 4: 2: 2 video luma/chroma output, interleaved U, Y V Y General purpose I/O, monitored/controlled by the microprocessor or DSP SW SERVO channel select output for AFE by-pass
135	VDDP	S	3.3 V digital periphery power supply
136	VID[1] GPCI/O[30] SSEL[1]	O I/O O	Digital 4: 2: 2 video luma/chroma output, interleaved U, Y V Y General purpose I/O, monitored/controlled by the microprocessor or DSP SW SERVO channel output for AFE by-pass
137	VID[0] ICGPCI/O[3]	O I/O	Digital 4: 2: 2 video luma/chroma output, interleaved U, Y V Y General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the microprocessor
138	GNDP	S	Digital periphery ground of 3.3 V supply
139	GND A	S	Ground plane of internal PLL circuit
140	RESET#	ID	Reset input (active low)
141	VDDA	S	1.8 V power supply for internal PLL circuit
142	XO	AO	Output to a crystal that is connected to GCLKP If a crystal is not used at GCLKP, XO must be left not connected.
143	GCLKP	ID	27.000MHz clock or crystal input for main processing clock generation.
144	GCLKA GPCI/O[31] GCLKPOUT	ID I/O O	27.000MHz clock input for audio master clock generation. General purpose I/O, monitored/controlled by the microprocessor or DSP SW GCLKP output
145	VDDP	S	3.3 V digital periphery power supply
146	ICGPCI/O[4]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the microprocessor
147	S/PDIFIN[0] GPCI/O[33]	I I/O	S/PDIF receiver input for digital coded or reconstructed audio data General purpose I/O, monitored/controlled by the microprocessor or DSP SW
148	ICGPCI/O[5]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the microprocessor
149	S/PDIFIN[1] GPCI/O[34]	I I/O	S/PDIF receiver input for digital coded or reconstructed audio data General purpose I/O, monitored/controlled by the microprocessor or DSP SW
150	IDGPCI/O[3] FCUIF[33]	I/O I	General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the DSP Flash card interface unit input signal
151	GNDP	S	Digital periphery ground of 3.3 V supply
152	DUPRD0 GPCI/O[35]	I I/O	First debug UART data input General purpose I/O, monitored/controlled by the microprocessor or DSP SW
153	DUPTD0 GPCI/O[36]	O I/O	First debug UART data output General purpose I/O, monitored/controlled by the microprocessor or DSP SW
154	VDD-IP	S	3.3 V periphery reference voltage
155	DUPRD1 GPCI/O[37]	I I/O	Second debug UART data output General purpose I/O, monitored/controlled by the microprocessor or DSP SW
156	DUPTD1 GPCI/O[38]	O I/O	Second debug UART data output General purpose I/O, monitored/controlled by the microprocessor or DSP SW
157	GNDDACD	S	Ground for the video DACs 3.3 V analog power supply
158	CVBS/G/Y (DAC A)	AO	When the Vaddis 778 outputs composite (SCART or non-SCART) video, this line is CVBS output When the Vaddis 778 outputs RGB, this line is the Green output When the Vaddis 778 outputs YUV, this line is the Y output
159	CVBS/C (DAC D)	AO	When the other Vaddis 778 output are not SCART video, the output on this line can be either CVBS or C / the selection is independent of the specific selection of the other three DACs

No.	Pin Functions	Direction	Description
			When the Vaddis 778 outputs composite SCART video, this line is the Y output
160	VDDDAC	S	3.3 V analog power supply for the video DACs
161	Y/R/V (DAC B)	AO	When the Vaddis 778 outputs composite non-SCART video, this line is Y output When the Vaddis 778 output RGB, this line is the Red output When the Vaddis 778 outputs YUV, this line is the V output When the Vaddis 778 outputs composite SCART video, this line is the C output
162	C/B/U (DAC C)	AO	When the Vaddis 778 outputs composite (SCART or non-SCART) video, this line is C output When the Vaddis 778 outputs RGB, this line is the Blue output When the Vaddis 778 outputs YUV, this line is the U output
163	RSET	AI	Resistive load for gain adjustment of the DACs
164	GNDDACP	S	Ground for the video DACs 3.3 V analog power supply
165	GNDDABS2	S	Common ground for the video and SERVO DACs
166	GNDDACPS	S	Ground for the SERVO DAC 3.3 V analog power
167	DACDRIVE[0]	AO	Drive DACs output signal
168	VDDDACS	S	3.3 V SERVO DACs power supply
169	DACDRIVE[1]	AO	Drive DACs output signal
170	GNDDACDS	S	Ground for the SERVO DAC 3.3 V analog power supply
171	VDDAFERF	S	3.3 V analog RF (AFE) power supply
172	RFINP	AI	RF positive input signal (differential input) // RF input signal (single ended)
173	RFINN	AI	RF negative input signal (differential input) // RF reference input signal
174	GNDAFERF	S	Analog RF (AFE) ground of 3.3 V supply
175	VDDAFES	S	3.3 V analog SERVO (AFE) power supply
176	ADCIN[7]	AI	SERVO ADC input signal (e.g. from RF amplifier)
177	ADCIN[6]	AI	SERVO ADC input signal from RF amplifier
178-183	ADCIN[5-0]	AI	SERVO ADC input signal (e.g. from RF amplifier)
184,185	VBIASS[0, 1]	AI	Servo analog signal reference voltage inputs
186	GNDAFES	S	Analog SERVO (AFE) ground of 3.3 V supply
187	PWMACT[0] GPCI/O[39] DVDDAT[0] NRZDATA	O I/O I I	PWM0 output signal General purpose I/O, monitored/controlled by the microprocessor or DSP or FCU SW AV data input for FE by-pass NRZ data input for AFE and DRC by-pass
188	PWMACT[1] GPCI/O[40] DVDDAT[1] NRZCLK	O I/O I I	PWM1 output signal General purpose I/O, monitored/controlled by the microprocessor or DSP or FCU SW AV data input for FE by-pass NRZ clock input for AFE and DRC by-pass
189	PWMCO[0] GPCI/O[41] DVDDAT[2] NRZLOCK	O I/O I I	PWM2 output signal General purpose I/O, monitored/controlled by the microprocessor or DSP SW AV data input for FE by-pass NRZ lock input for AFE and DRC by-pass
190	GNDC	S	Digital core ground of 1.8 V supply
191	PWMCO[1] GPCI/O[42] DVDDAT[3] NRZDFCT	O I/O I I	PWM3 output signal General purpose I/O, monitored/controlled by the microprocessor or DSP SW AV data input for FE by-pass NRZ defect input for AFE and DRC by-pass
192	VDDC	S	1.8 V digital core power supply
193	PWMCO[2] GPCI/O[43] FCUIF[34] DVDDAT[4]	O I/O O I	PWM4 output signal General purpose I/O, monitored/controlled by the microprocessor or DSP SW Flash card interface unit input signal AV data input for FE by-pass
194	PWMCO[3] GPCI[44] FCUIF[35] IDGPCI/O[2] DVDDAT[5]	O I/O I/O I/O I	PWM5 output signal General purpose I/O, monitored/controlled by the microprocessor or DSP SW Flash card interface unit I/O signal General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the DSP AV data input for FE by-pass
195	GNDPWMS	S	SERVO PWMs ground of 3.3 V supply
196	PWMCO[4] GPCI/O[45] DVDDAT[6]	O I/O I	PWM6 output signal General purpose I/O, monitored/controlled by the microprocessor or DSP SW AV data input for FE by-pass
197	VDDPWMS	S	3.3 V SERVO PWM power supply
198	PWMCO[5] GPCI/O[46] FCUIF[36] DVDDAT[7]	O I/O I/O I	PWM7 output signal General purpose I/O, monitored/controlled by the microprocessor or DSP SW Flash card interface unit I/O signal AV data input for FE by-pass

No.	Pin Functions	Direction	Description
199	PWMC0[6]	O	PMW8 output signal
	IDGPCI/O[4]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[32]	I/O	Flash card interface unit I/O signal
	DVDSTRB	I	AV data input for FE by-pass
	RFDAT[4]	I	RF channel sample data inputs for AFE by-pass
200	DEFFCT	I/O	Disc defect input or output signal
	IDGPCI/O[5]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[37]	I/O	Flash card interface unit I/O signal
	DVDREQ	O	AV data request output for FE by-pass / Programmable polarity
201	ICGPI/O[6]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP or FCU SW When input, the pin can be used as general purpose external interrupt to the microprocessor
	DVDVALID	I	AV data valid input for FE by-pass / Programmable polarity
202	GNDP	S	Digital periphery ground of 3.3 V supply
203	ICGPI/O[7]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP or FCU SW When input, the pin can be used as general purpose external interrupt to the microprocessor
	DVDERR	I	AV error input for FE by-pass / Programmable polarity
204	VDDP	S	3.3 V digital periphery power supply
205	SLEDPULSE	I	Sled optical encoder input
	IDGPCI/O[6]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[30]	I	Flash card interface unit output signal
	DVDSOS	I	AV start of sector indication input for FE by-pass / Programmable polarity
206	SPIND LEPULSE	I	Spindle optical encoder input
	IDGPCI/O[7]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[31]	I/O	Flash card interface unit I/O signal
207	SSCCLK	I/O	SSC clock input signal
	GPCI/O[47]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP or FCU SW
208	SSCTXD	O	SSC data output signal
	GPCI/O[16]	I/O	General purpose I/O, monitored/controlled by the microprocessor or DSP SW

IC20: SAA7893HLC2 (MAIN P.C.B.)
DSD decoder



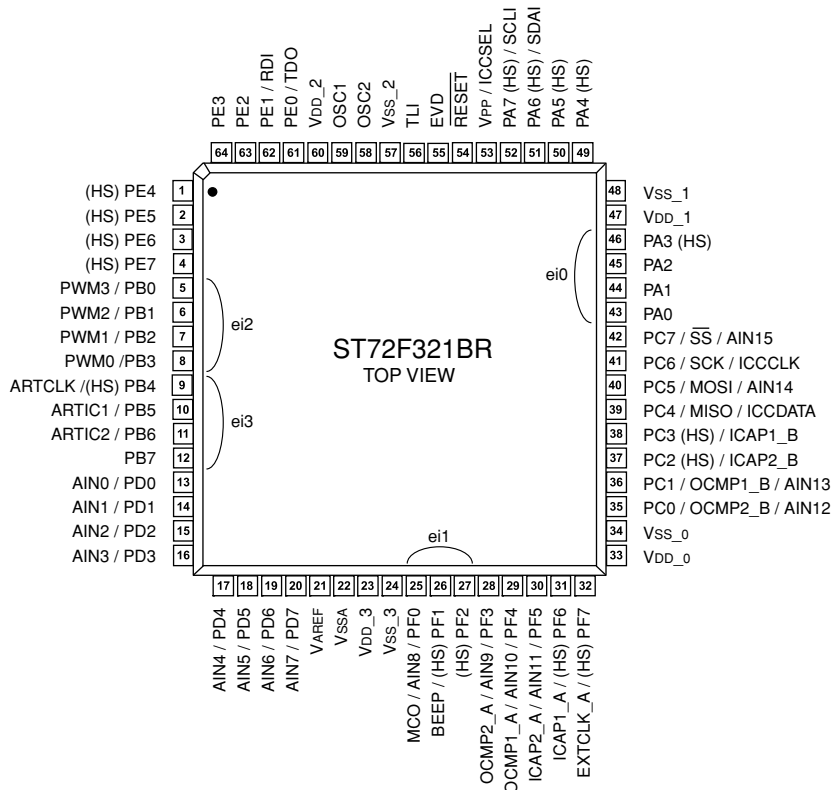
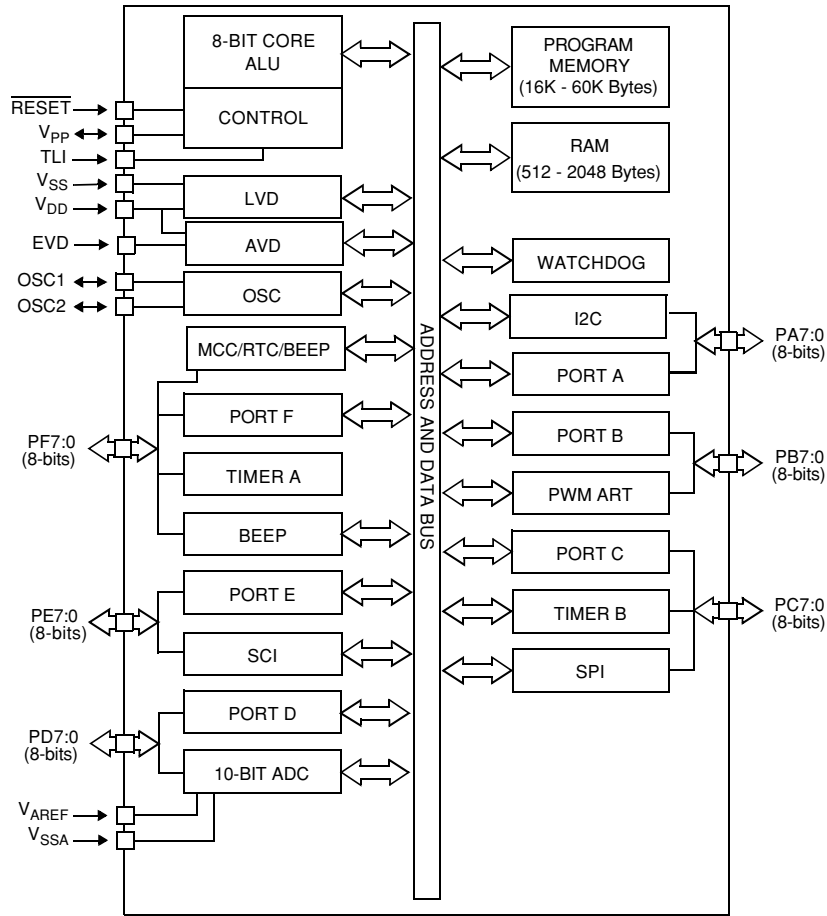
DVD-S1800

Pin.	Symbol	Type ^[1]	Description	Pin	Symbol	Type ^[1]	Description
1	H_A[1]	IN	Address bus	64	D_ADDR[3]	O10	SDRAM address bus
2	H_DQ[15]	I/O10	Data bus	65	D_ADDR[4]	O10	SDRAM address bus
3	H_DQ[14]	I/O10	Data bus	66	D_ADDR[2]	O10	SDRAM address bus
4	GND_IO1	GND_IO	GND I/O pads	67	D_ADDR[5]	O10	SDRAM address bus
5	H_DQ[13]	I/O10	Data bus	68	D_ADDR[1]	O10	SDRAM address bus
6	H_DQ[12]	I/O10	Data bus	69	GND_IO3	GND_IO	GND I/O pads
7	H_DQ[11]	I/O10	Data bus	70	D_ADDR[6]	O10	SDRAM address bus
8	H_DQ[10]	I/O10	Data bus	71	D_ADDR[0]	O10	SDRAM address bus
9	H_DQ[9]	I/O10	Data bus	72	D_ADDR[7]	O10	SDRAM address bus
10	VCC_IO1	VCC_IO1	Vcc I/O pads	73	D_ADDR[10]	O10	SDRAM address bus
11	H_DQ[8]	I/O10	Data bus	74	D_ADDR[8]	O10	SDRAM address bus
12	H_DQ[7]	I/O10	Data bus	75	D_ADDR[13]	O10	SDRAM address bus
13	H_DQ[6]	I/O10	Data bus	76	VCC_IO3	VCC_IO	Vcc I/O pads
14	H_DQ[5]	I/O10	Data bus	77	D_ADDR[9]	O10	SDRAM address bus
15	H_DQ[4]	I/O10	Data bus	78	D_ADDR[12]	O10	SDRAM address bus
16	H_DQ[3]	I/O10	Data bus	79	D_ADDR[11]	O10	SDRAM address bus
17	GND_IO2	GND_IO	GND I/O pads	80	D_Wen	O10	Read or write
18	H_procclk	IN	Host processor EMI interface clock	81	D_RASn	O10	Row address select; active LOW
19	VCC_Core1	VCC_core	Core supply voltage	82	D_CASn	O10	Column address select; active LOW
20	GND_Core1	GND_core	Core ground	83	GND_IO4	GND_IO	GND I/O pads
21	sys_clk	IN	System clock	84	GND_Core2	GND_core	Core ground
22	H_DQ[2]	I/O10	Data bus	85	VCC_Core2	VCC_core	Core supply voltage
23	H_DQ[1]	I/O10	Data bus	86	D_clk	O10	Clock signal needed for SDRAM
24	H_CSn	IN	Host chip select; active LOW	87	D_DQ[5]	I/O10	Data bus
25	H_DQ[0]	I/O10	Data bus	88	D_UDQM	O10	DQ mask enable (upper)
26	H_RWn	IN	Read = 1; Write = 0	89	D_LDQM	O10	DQ mask enable (lower)
27	H_WAIT	O10	Wait signal	90	D_DQ[7]	I/O10	Data bus
28	H_IRQn	O10	Interrupt request; active LOW	91	D_DQ[8]	I/O10	Data bus
29	aud_clk	IN	DSD audio clock	92	VCC_IO4	VCC_IO	Vcc I/O pads
30	PCM_dclk_in	IN	PCM data clock	93	D_DQ[6]	I/O10	Data bus
31	PCM_wclk_in	IN	PCM word clock	94	D_DQ[9]	I/O10	Data bus
32	VDDA	VDDCO	VDD of ADC	95	D_DQ[10]	I/O10	Data bus
33	VSSA	VSSCO	Vss of AGC and ADC; Connected to substrate	96	D_DQ[4]	I/O10	Data bus
34	biasin	APIO	Bias current input	97	D_DQ[11]	I/O10	Data bus
35	Agcinp	APIO	AGC positive input signal; HF in	98	D_DQ[3]	I/O10	Data bus
36	Adcrefl	APIO	ADC decoupling	99	GND_IO5	GND_IO	GND I/O pads
37	Vcc_IO7	VCC_IO	VCC I/O pads	100	D_DQ[12]	I/O10	Data bus
38	GND_IO7	GND_IO	GND I/O pads	101	D_DQ[2]	I/O10	Data bus
39	PCM_CeLf_in	IN	PCM data center or LFE	102	D_DQ[13]	I/O10	Data bus
40	PCM_LeRi_in	IN	PCM data left or right	103	D_DQ[1]	I/O10	Data bus
41	PCM_LsRs_in	IN	PCM data left or right surround	104	D_DQ[14]	I/O10	Data bus
42	B_FLAG/SERR	IN	I ² S-bus flag (EDC flag)	105	D_DQ[0]	I/O10	Data bus
43	B_SYNC/Sync	IN	Sector sync or absolute time sync	106	VCC_IO5	VCC_IO	Vcc IO pads
44	B_WCLK/SENB	IN	I ² S-bus word clock or UDE data sense from host	107	D_DQ[15]	I/O10	Data bus
45	B_DATA/Be_dat(0)	IN	I ² S-bus data or LSB data of parallel interface	108	DSD_PCM_0	O10	6-channel data output
46	B_BCLK/SDCLK	IN	I ² S-bus bit clock	109	DSD_PCM_1	O10	6-channel data output
47	UDE_req	IN	Host request data from front-end; routed via the SAA7893HL	110	DSD_PCM_2	O10	6-channel data output
48	Data_req	O10	Data request for UDE	111	DSD_PCM_3	O10	6-channel data output
49	Be_dat(1)	IN	Front-end parallel data interface	112	GND_IO6	GND_IO	GND I/O pads
50	Be_dat(2)	IN	Front-end parallel data interface	113	DSD_PCM_4	O10	6-channel data output
51	Be_dat(3)	IN	Front-end parallel data interface	114	DSD_PCM_5	O10	6-channel data output
52	Be_dat(4)	IN	Front-end parallel data interface	115	DSD_PCM_6	O10	6-channel data output
53	Be_dat(5)	IN	Front-end parallel data interface	116	DSD_PCM_7	O10	6-channel data output
54	Be_dat(6)	IN	Front-end parallel data interface	117	DSD_PCM_8	O10	2-channel data output
55	Be_dat(7)	IN	Front-end parallel data interface	118	VCC_IO6	VCC_IO	Vcc I/O pads
56	TRST	IN1	Boundary scan reset	119	DSD_PCM_10	O10	2-channel data output
57	TMS	IN1	Boundary scan mode select	120	DSD_PCM_9	O10	2-channel clock or control
58	VCC_IO2	VCC_IO	Vcc I/O pads	121	DSD_PCM_11	O10	2-channel data output
59	TDO	O10	Output	122	RESETn	IN	Asynchronous reset; active LOW
60	TDI	IN1	Boundary scan data input	123	H_A_sel	IN	Address select
61	TCK	IN	Boundary scan clock	124	H_A[6]	IN	Address bus
62	H_sel[0]	IN	Host select signals: SAD16, MAD16 and SAD08	125	H_A[5]	IN	Address bus
63	H_sel[1]	IN	Host select signals: SAD16, MAD16 and SAD08	126	H_A[4]	IN	Address bus
				127	H_A[3]	IN	Address bus
				128	H_A[2]	IN	Address bus

IC41: ST72F321BR (MAIN P.C.B.)
Microprocessor

* No replacement part available.

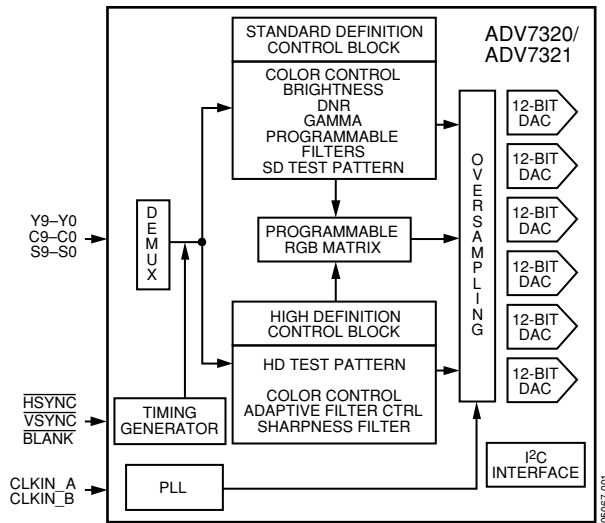
Device Block Diagram



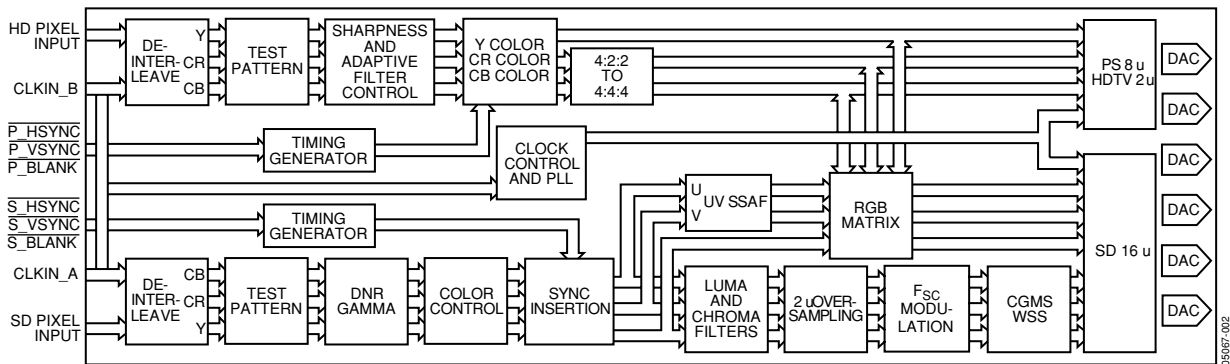
DVD-S1800

Pin no.	TQFP64	TQFP44	Pin Name	Type	Level		Port						Main function (afterreset)	Alternate function
					Input	Output	Input				Output			
							float	wpu	int	ana	OD	PP		
1	-	RS-232C_RTS	I/O	C _T	HS	X	X				X	X	Port E4	
2	-	RS-232C_CTS	I/O	C _T	HS	X	X				X	X	Port E5	
3	-	VFD_RESET	I/O	C _T	HS	X	X				X	X	Port E6	
4	-	N.C.	I/O	C _T	HS	X	X				X	X	Port E7	
5	2	REMOTE_IN/OUT	I/O	C _T		X		ei2			X	X	Port B0	PWM output 3
6	3	N.C.	I/O	C _T		X		ei2			X	X	Port B1	PWM output 2
7	4	N.C.	I/O	C _T		X		ei2			X	X	Port B2	PWM output 1
8	5	GND	I/O	C _T		X		ei2			X	X	Port B3	PWM output 0
9	6	GND	I/O	C _T	HS	X		ei3			X	X	Port B4	PWM-ART external clock
10	-	HDMI_DET.	I/O	C _T		X		ei3			X	X	Port B5	PWM-ART input capture 1
11	-	HDMI_INT.	I/O	C _T		X		ei3			X	X	Port B6	PWM-ART input capture 2
12	-	N.C.	I/O	C _T		X		ei3			X	X	Port B7	
13	7	KEY#1	I/O	C _T		X	X		X	X	X	X	Port D0	ADC analog input 0
14	8	KEY#2	I/O	C _T		X	X		X	X	X	X	Port D1	ADC analog input 1
15	9	N.C.	I/O	C _T		X	X		X	X	X	X	Port D2	ADC analog input 2
16	10	N.C.	I/O	C _T		X	X		X	X	X	X	Port D3	ADC analog input 3
17	11	PWR_CTL	I/O	C _T		X	X		X	X	X	X	Port D4	ADC analog input 4
18	12	A_MUTE	I/O	C _T		X	X		X	X	X	X	Port D5	ADC analog input 5
19	-	AVMUTE	I/O	C _T		X	X		X	X	X	X	Port D6	ADC analog input 6
20	-	INT/EXT_SEL	I/O	C _T		X	X		X	X	X	X	Port D7	ADC analog input 7
21	13	VAREF	I											Analog reference voltage for ADC
22	14	VSSA	S											Analog ground voltage
23	-	VDD_3	S											Digital main supply voltage
24	-	VSS_3	S											Digital ground voltage
25	15	REMOTE/BUS_IN	I/O	C _T		X		ei1	X	X	X	X	Port F0	Main clock out (fOSC/2) ADC analog input 8
26	16	REMOTE_OUT	I/O	C _T	HS	X		ei1			X	X	Port F1	Beep signal output
27	17	N.C.	I/O	C _T	HS	X		ei1			X	X	Port F2	
28	-	HDMI_RESET	I/O	C _T		X	X		X	X	X	X	Port F3	Timer A output compare 2 ADC analog input 9
29	18	FL_OFF_LED	I/O	C _T		X	X		X	X	X	X	Port F4	Timer A output compare 1 ADC analog input 10
30	-	HDMI_ON_LED	I/O	C _T		X	X		X	X	X	X	Port F5	Timer A input capture 2 ADC analog input 11
31	19	HDMI_LINK_LED	I/O	C _T	HS	X	X		X	X	X	X	Port F6	Timer A input capture 1
32	20	N.C.	I/O	C _T	HS	X	X				X	X	Port F7	Timer A external clock source
33	21	VDD_0	S											Digital main supply voltage
34	22	VSS_0	S											Digital ground voltage
35	23	N.C.	I/O	C _T		X	X		X	X	X	X	Port C0	Timer B output compare 2 ADC analog input 12
36	24	N.C.	I/O	C _T		X	X		X	X	X	X	Port C1	Timer B output compare 1 ADC analog input 13
37	25	N.C.	I/O	C _T	HS	X	X				X	X	Port C2	Timer B input capture 2
38	26	N.C.	I/O	C _T	HS	X	X				X	X	Port C3	Timer B input capture 1
39	27	DSP&DAC_IN	I/O	C _T		X	X				X	X	Port C4	SPI master in/slave out data ICC data input
40	28	DSP&DAC_OUT	I/O	C _T		X	X		X	X	X	X	Port C5	SPI master out/slave in data ADC analog input 14
41	29	ICCCLK	I/O	C _T		X	X				X	X	Port C6	SPI serial clock ICC clock output
42	-	DSP_FINTREQ.	I/O	C _T		X	X		X	X	X	X	Port C7	SPI slave select (active low) ADC analog input 15
43	-	PMCLK&DMCLK_SEL	I/O	C _T		X		ei0			X	X	Port A0	
44	-	MREQ	I/O	C _T		X		ei0			X	X	Port A1	
45	31	KEY W/U	I/O	C _T		X		ei0			X	X	Port A2	
46	32	MRESET	I/O	C _T	HS	X		ei0			X	X	Port A3	
47	33	VDD_1	S											Digital main supply voltage
48	34	VSS_1	S											Digital ground voltage
49	35	F_REQ	I/O	C _T	HS	X	X				X	X	Port A4	
50	36	GND	I/O	C _T	HS	X	X				X	X	Port A5	
51	37	I2C_DATA	I/O	C _T	HS	X					T		Port A6	I ² C data ¹⁾
52	38	I2C_CLK	I/O	C _T	HS	X					T		Port A7	I ² C clock ¹⁾
53	39	RS232(+12V)	I											Must be tied low. In flash programming mode, this pin acts as the programming voltage input VPP. See section 12.9.2 for more details. High voltage must not be applied to ROM devices.
54	-	RESET	I/O	C _T										Top priority non maskable interrupt
55	-	N.C.												External voltage detector
56	40	N.C.	I	C _T				X						Top level interrupt input pin
57	41	VSS_2	S											Digital ground voltage
58	42	OSC2	I/O											Resonator oscillator inverter output
59	43	OSC1	I											External clock input or resonator oscillator inverter input
60	44	VDD_2	S											Digital main supply voltage
61	1	RS-232C_TX	I/O	C _T		X	X				X	X	Port E0	SCI transmit data out
62	-	RS-232C_RX	I/O	C _T		X	X				X	X	Port E1	SCI receive data in
63	-	GND	I/O	C _T									Port E2	
64	-	N.C.	I/O	C _T		X	X				X	X	Port E3	

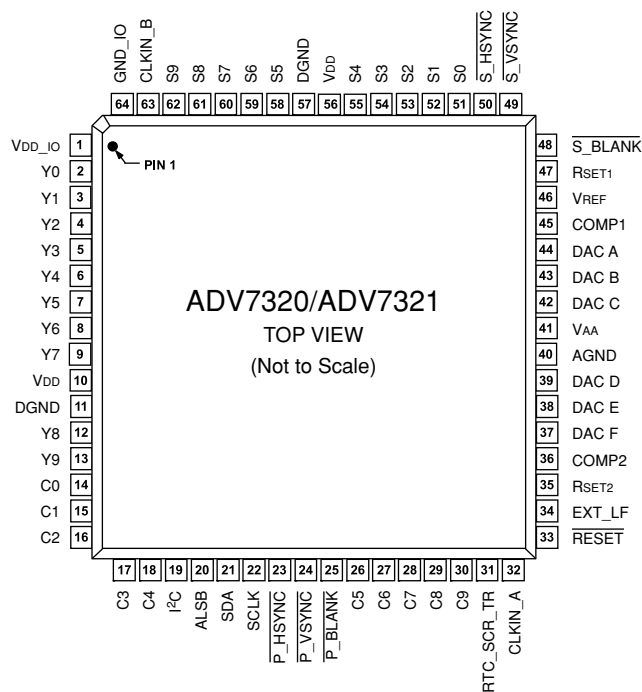
IC51: ADV7320KSTZ (MAIN P.C.B.)
Video encoder



Simplified Functional Block Diagram



Detailed Functional Block Diagram

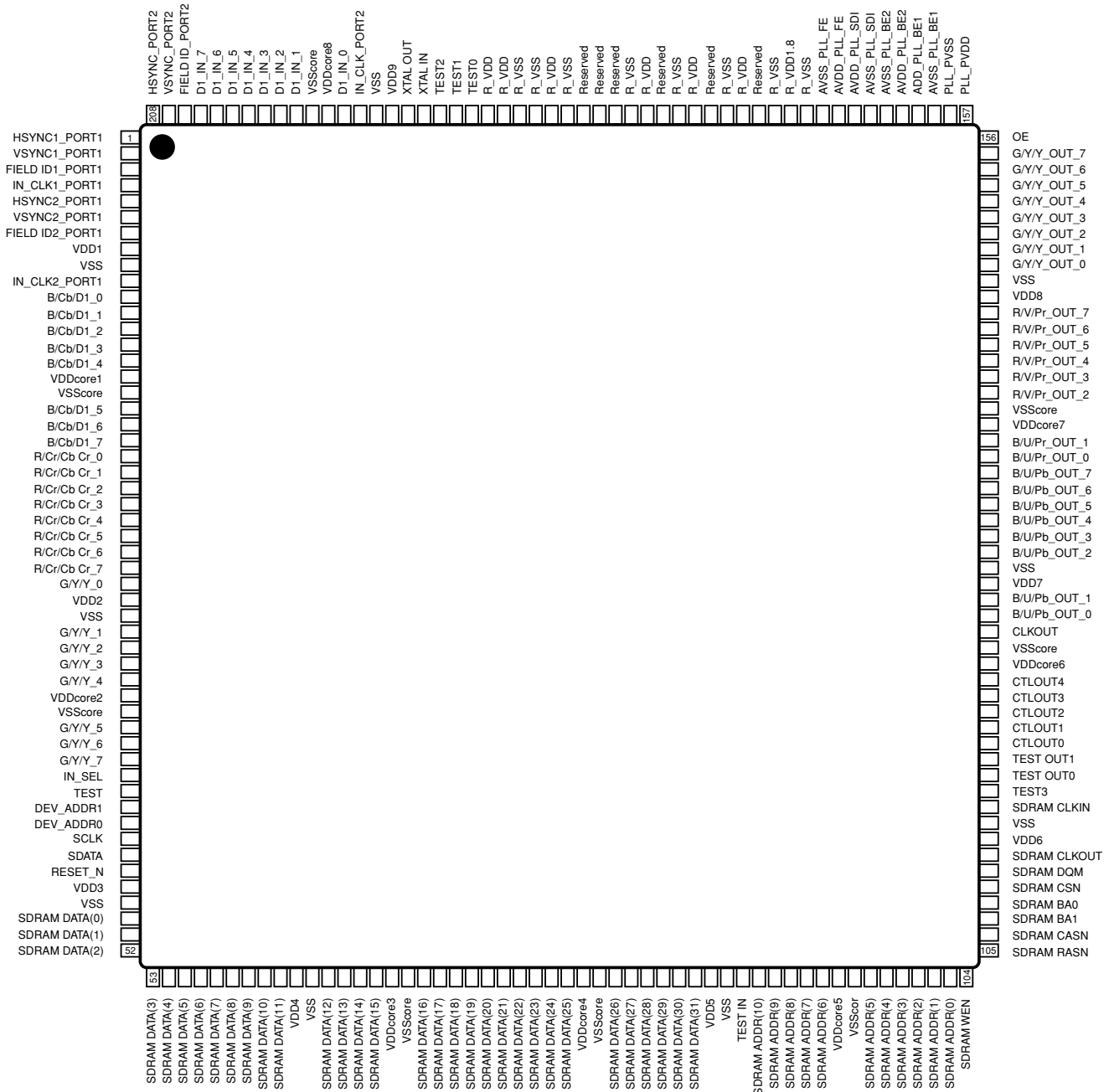


Pin No	Mnemonic	Input/Output	Description
1	VDD_IO	P	Power supply for digital inputs and outputs.
2	Y0	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
3	Y1	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
4	Y2	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
5	Y3	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
6	Y4	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
7	Y5	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
8	Y6	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
9	Y7	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
10	VDD	P	Digital power supply.
11	DGND	G	Digital ground.
12	Y8	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
13	Y9	I	SD or progressive scan/HDTV input port for Y data. Input port for interleaved progressive scan data. The LSB is set up on pin Y0. For 8-bit data input, LSB is set up on Y2.
14	C0	I	Progressive scan/HDTV input port 4:4:4 input mode. This port is used for the Cb [Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
15	C1	I	Progressive scan/HDTV input port 4:4:4 input mode. This port is used for the Cb [Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
16	C2	I	Progressive scan/HDTV input port 4:4:4 input mode. This port is used for the Cb [Blue/U] data. The LSB is set up on Pin C0. For 8-bit data input, LSB is set up on C2.
17	C3	I	Progressive Scan/HDTV Input Port 4:4:4 Input Mode. This port is used for the Cb [Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
18	C4	I	Progressive scan/HDTV input port 4:4:4 input mode. This port is used for the Cb [Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
19	XSPI/I ² C	I	This input pin must be tied high (VDD_IO) for the ADV7320/ADV7321 to interface over the I ² C port.
20	ALSB_SO	I	TTL Address Input. This signal sets up the LSB of the I ² C address. When this pin is tied low, the I ² C filter is activated, which reduces noise on the I ² C interface.
21	SDA_CLKSP	I/O	I ² C port serial data input/output.
22	SCLK_SI	I	I ² C port serial interface clock input.
23	XP_HSYNC	I	Video horizontal SYNC control signal for HD in simultaneous SD/HD mode and HD only mode.
24	XP_VSYNC	I	Video vertical SYNC control signal for HD in simultaneous SD/HD mode and HD only mode.
25	P_BLANK	I	Video blanking control signal for HD in simultaneous SD/HD mode and HD only mode.
26	C5	I	Progressive scan/HDTV input port 4:4:4 input mode. This port is used for the Cb [Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
27	C6	I	Progressive scan/HDTV input port 4:4:4 input mode. This port is used for the Cb [Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
28	C7	I	Progressive scan/HDTV input port 4:4:4 input mode. This port is used for the Cb [Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
29	C8	I	Progressive scan/HDTV input port 4:4:4 input mode. This port is used for the Cb [Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
30	C9	I	Progressive scan/HDTV input port 4:4:4 input mode. This port is used for the Cb [Blue/U] data. The LSB is set up on pin C0. For 8-bit data input, LSB is set up on C2.
31	RTC_SCR_TR	I	Multifunctional input. Real-time control (RTC) input, timing reset input, subcarrier reset input.
32	CLKIN_A	I	Pixel clock input for HD (74.25 MHz only, PS only (27 MHz), SD only (27 MHz)).
33	RESET	I	This input resets the on-chip timing generator and sets the ADV7320/ADV7321 into default register setting. RESET is an active low signal.
34	EXT_LF	I	External loop filter for the internal PLL.

Pin No	Mnemonic	Input/Output	Description
35	RSET2	I	A 3040 ohm resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
36	COMP2	O	Compensation pin for DACs. Connect 0.1 uF capacitor from COMP pin to V _{AA} .
37	DAC_F	O	In SD only mode: Chroma/Red/V analog output; in HD only mode and simultaneous HD/SD. Mode: Pb/Blue [HD] analog output.
38	DAC_E	O	In SD only mode: Luma/Blue/U analog output; in HD only mode and simultaneous HD/SD. Mode: Pr/Red analog output
39	DAC_D	O	In SD only mode: CVBS/Green/Y analog output; in HD only mode and simultaneous HD/SD. Mode: Y/Green [HD] analog output.
40	AGND	G	Analog ground.
41	V _{AA}	P	Analog power supply.
42	DAC_C	O	Luma/Red/V/Pr analog output.
43	DAC_B	O	Chroma/Blue/U/Pb analog output.
44	DAC_A	O	CVBS/Green/Y/Y analog output.
45	COMP1	O	Compensation pin for DACs. Connect 0.1 uF capacitor from COMP pin to V _{AA} .
46	V _{REF}	I/O	Optional external voltage reference input for DACs or voltage reference output (1.235 V).
47	RSET1	I	A 3040 ohm resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
48	XS_BLANK	I/O	Video blanking control signal for SD only.
49	XS_VSYNC	I/O	Video vertical SYNC control signal for SD only.
50	XS_HSYNC	I/O	Video horizontal SYNC control signal for SD only.
51	S0	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
52	S1	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
53	S2	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
54	S3	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
55	S4	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
56	V _{DD}	P	Digital power supply.
57	DGND	G	Digital ground.
58	S5	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
59	S6	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
60	S7	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
61	S8	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
62	S9	I	SD or progressive scan/HDTV input port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on pin S0. For 8-bit data input, LSB is set up on S2.
63	CLKIN_B	I	Pixel clock input. Requires a 27 MHz reference clock for progressive scan mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV mode. This clock is only used in dual modes.
64	GND_IO		Digital input/output ground.

IC61: FLI2310LFCF (MAIN P.C.B.)
Digital video converter

DVD-S1800



NOTES:
 1) *-The connection of these pins depends on the type of external SDRAM used. See Appendix 3
 2) For 16/20 bit Y and muxed C output modes see Appendix 2 for pin configuration

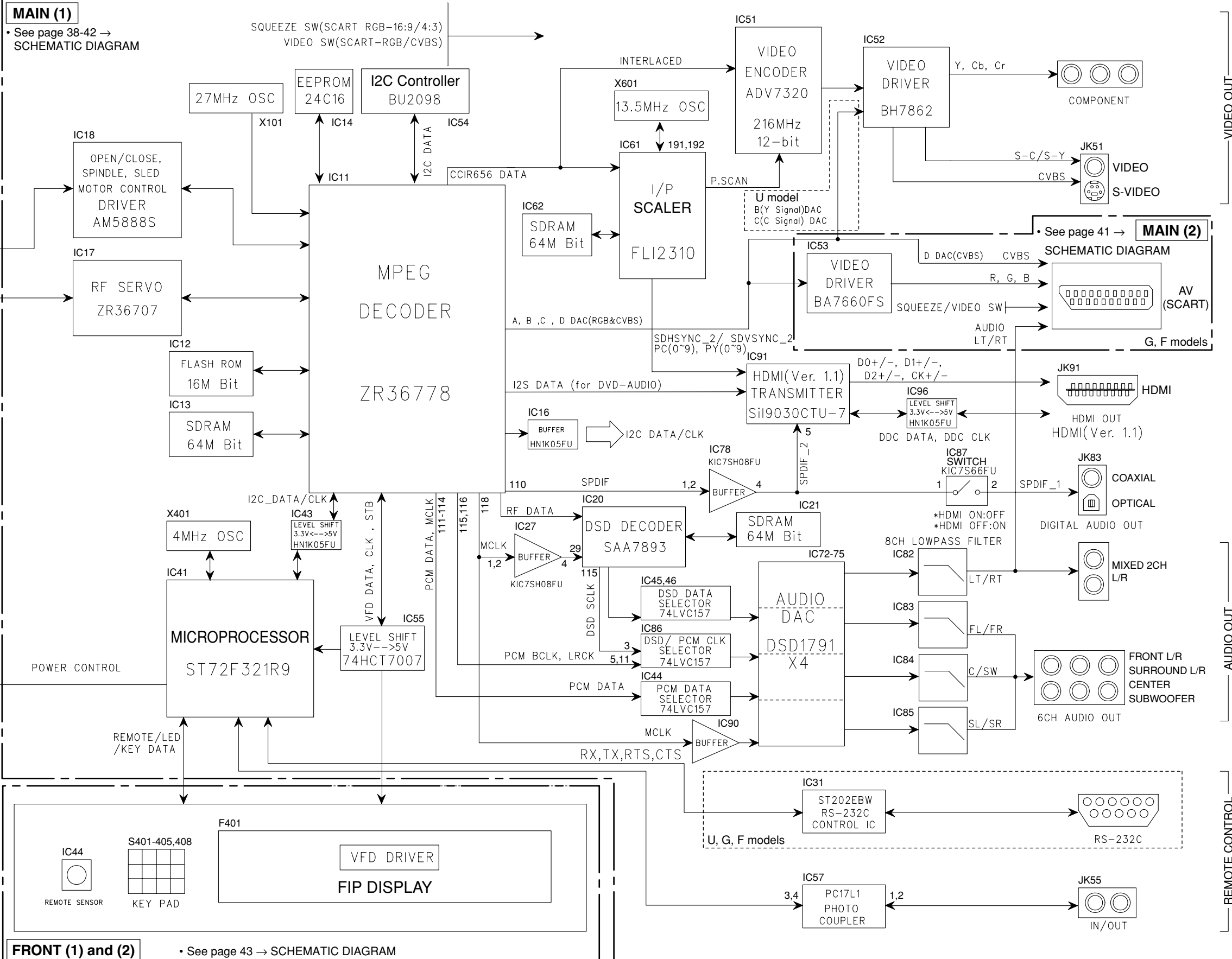
No.	Pin Name	I/O Type	Voltage Tolerance	Drive	Internal Pull-up/Pull-down	Description
1	HSYNC1_PORT1	Input	5v			Horizontal sync or reference - CTL1 of Port 1
2	VSYNC1_PORT1	Input	5v			Vertical sync or reference - CTL1 of Port 1
3	FIELD ID1_PORT1	Input	5v			Odd/Even field identification - CTL1 of Port 1
4	IN_CLK1_PORT1	Input	5v			Data clock input - CTL1 of Port 1
5	HSYNC2_PORT1	Input	5v			Horizontal sync or reference - CTL2 of Port 1
6	VSYNC2_PORT1	Input	5v			Vertical sync or reference - CTL2 of Port 1
7	FIELD ID2_PORT1	Input	5v			Odd/Even field identification - CTL2 of Port 1
8	VDD1	Power				3.3 V - Power pin for IO
9	VSS	Ground				Ground
10	IN_CLK2_PORT1	Input	5v			Data clock input - CTL2 of Port 1
11	B/Cb/D1_0	Input	5v			Port 1 - Digital video input (Blue/Cb/D1)
12	B/Cb/D1_1	Input	5v			Port 1 - Digital video input (Blue/Cb/D1)
13	B/Cb/D1_2	Input	5v			Port 1 - Digital video input (Blue/Cb/D1)
14	B/Cb/D1_3	Input	5v			Port 1 - Digital video input (Blue/Cb/D1)
15	B/Cb/D1_4	Input	5v			Port 1 - Digital video input (Blue/Cb/D1)
16	VDDcore1	Power				1.8 V - Power pin for core
17	VSScore	Ground				Ground
18	B/Cb/D1_5	Input	5v			Port 1 - Digital video input (Blue/Cb/D1)
19	B/Cb/D1_6	Input	5v			Port 1 - Digital video input (Blue/Cb/D1)
20	B/Cb/D1_7	Input	5v			Port 1 - Digital video input (Blue/Cb/D1)
21	R/Cr/Cb Cr_0	Input	5v			Port 1 - Digital video input (Red/Cr/CrCb)
22	R/Cr/Cb Cr_1	Input	5v			Port 1 - Digital video input (Red/Cr/CrCb)
23	R/Cr/Cb Cr_2	Input	5v			Port 1 - Digital video input (Red/Cr/CrCb)
24	R/Cr/Cb Cr_3	Input	5v			Port 1 - Digital video input (Red/Cr/CrCb)
25	R/Cr/Cb Cr_4	Input	5v			Port 1 - Digital video input (Red/Cr/CrCb)
26	R/Cr/Cb Cr_5	Input	5v			Port 1 - Digital video input (Red/Cr/CrCb)
27	R/Cr/Cb Cr_6	Input	5v			Port 1 - Digital video input (Red/Cr/CrCb)
28	R/Cr/Cb Cr_7	Input	5v			Port 1 - Digital video input (Red/Cr/CrCb)
29	G/Y/Y_0	Input	5v			Port 1 - Digital video input (Green/Y)
30	VDD2	Power				3.3 V - Power pin for IO
31	VSS	Ground				Ground
32	G/Y/Y_1	Input	5v			Port 1 - Digital video input (Green/Y)
33	G/Y/Y_2	Input	5v			Port 1 - Digital video input (Green/Y)
34	G/Y/Y_3	Input	5v			Port 1 - Digital video input (Green/Y)
35	G/Y/Y_4	Input	5v			Port 1 - Digital video input (Green/Y)
36	VDDcore2	Power				1.8 V - Power pin for core
37	VSScore	Ground				Ground
38	G/Y/Y_5	Input	5v			Port 1 - Digital video input (Green/Y)
39	G/Y/Y_6	Input	5v			Port 1 - Digital video input (Green/Y)
40	G/Y/Y_7	Input	5v			Port 1 - Digital video input (Green/Y)
41	IN_SEL	Output	5v	8mA		Output to select external video mux
42	TEST	Input	5v			Connect to ground
43	DEV_ADDR1	Input	5v			Device address setting 1
44	DEV_ADDR0	Input	5v			Device address setting 0
45	SCLK	I/O	5v	8mA		2-wire serial control bus clock
46	SDATA	I/O	5v	8mA		2-wire serial control bus data
47	RESET_N	Input	5v		PU	Reset
48	VDD3	Power				3.3 V - Power pin for IO
49	VSS	Ground				Ground
50	SDRAM DATA(0)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
51	SDRAM DATA(1)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
52	SDRAM DATA(2)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
53	SDRAM DATA(3)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
54	SDRAM DATA(4)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
55	SDRAM DATA(5)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
56	SDRAM DATA(6)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
57	SDRAM DATA(7)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
58	SDRAM DATA(8)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
59	SDRAM DATA(9)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
60	SDRAM DATA(10)	Tristate I/O	5v	4mA	PD	SDRAM data bus *

No.	Pin Name	I/O Type	Voltage Tolerance	Drive	Internal Pull-up/ Pull-down	Description
61	SDRAM DATA(11)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
62	VDD4	Power				3.3 V - Power pin for IO
63	VSS	Ground				Ground
64	SDRAM DATA(12)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
65	SDRAM DATA(13)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
66	SDRAM DATA(14)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
67	SDRAM DATA(15)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
68	VDDcore3	Power				1.8 V - Power pin for core
69	VSScore	Ground				Ground
70	SDRAM DATA(16)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
71	SDRAM DATA(17)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
72	SDRAM DATA(18)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
73	SDRAM DATA(19)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
74	SDRAM DATA(20)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
75	SDRAM DATA(21)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
76	SDRAM DATA(22)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
77	SDRAM DATA(23)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
78	SDRAM DATA(24)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
79	SDRAM DATA(25)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
80	VDDcore4	Power				1.8 V - Power pin for core
81	VSScore	Ground				Ground
82	SDRAM DATA(26)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
83	SDRAM DATA(27)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
84	SDRAM DATA(28)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
85	SDRAM DATA(29)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
86	SDRAM DATA(30)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
87	SDRAM DATA(31)	Tristate I/O	5v	4mA	PD	SDRAM data bus *
88	VDD5	Power				3.3 V - Power pin for IO
89	VSS	Ground				Ground
90	TEST IN	Input	5v			Test input - Connect to ground
91	SDRAM ADDR(10)	Tristate O/P	5v	8mA		SDRAM address bus *
92	SDRAM ADDR(9)	Tristate O/P	5v	8mA		SDRAM address bus *
93	SDRAM ADDR(8)	Tristate O/P	5v	8mA		SDRAM address bus *
94	SDRAM ADDR(7)	Tristate O/P	5v	8mA		SDRAM address bus *
95	SDRAM ADDR(6)	Tristate O/P	5v	8mA		SDRAM address bus *
96	VDDcore5	Power				1.8 V - Power pin for core
97	VSScor	Ground				Ground
98	SDRAM ADDR(5)	Tristate O/P	5v	8mA		SDRAM address bus *
99	SDRAM ADDR(4)	Tristate O/P	5v	8mA		SDRAM address bus *
100	SDRAM ADDR(3)	Tristate O/P	5v	8mA		SDRAM address bus *
101	SDRAM ADDR(2)	Tristate O/P	5v	8mA		SDRAM address bus *
102	SDRAM ADDR(1)	Tristate O/P	5v	8mA		SDRAM address bus *
103	SDRAM ADDR(0)	Tristate O/P	5v	8mA		SDRAM address bus *
104	SDRAM WEN	Tristate O/P	5v	8mA		SDRAM write enable *
105	SDRAM RASN	Tristate O/P	5v	8mA		SDRAM row address select *
106	SDRAM CASN	Tristate O/P	5v	8mA		SDRAM column address select *
107	SDRAM BA1	Tristate O/P	5v	8mA		SDRAM bank select 1 *
108	SDRAM BA0	Tristate O/P	5v	8mA		SDRAM bank select 0 *
109	SDRAM CSN	Tristate O/P	5v	4mA		SDRAM CS *
110	SDRAM DQM	Tristate O/P	5v	8mA		SDRAM DQM *
111	SDRAM CLKOUT	Output	5v	12mA		Clock out to SDRAM *
112	VDD6	Power				3.3 V - Power pin for IO
113	VSS	Ground				Ground
114	SDRAM CLKIN	Input	5v			Trace delayed SDRAM clock in
115	TEST3	Input				Test input -Connect to ground
116	TEST OUT0	Output		12mA		Test output - Leave open
117	TEST OUT1	Output		8mA		Test output - Leave open
118	CTLOUT0	Tristate O/P	5v	8mA		Control signal output selectable as HSync1/ CSync/HRef/Monitor coast
119	CTLOUT1	Tristate O/P	5v	8mA		Control signal output selectable as

No.	Pin Name	I/O Type	Voltage Tolerance	Drive	Internal Pull-up/Pull-down	Description
						VSync1/CRef/VRef/Film indicator
120	CTL0UT2	Tristate O/P	5v	8mA		Control signal output selectable as monitor Coast/HRef/VDD_en/HSync2
121	CTL0UT3	Tristate O/P	5v	8mA		Control signal output selectable as film Indicator/VRef/Backlight_en/VSync2
122	CTL0UT4	Tristate O/P	5v	8mA		Control signal output selectable as CRef/Field ID/CSync/Monitor coast
123	VDDcore6	Power				1.8 V - Power pin for core
124	VSScore	Ground				Ground
125	CLKOUT	Tristate O/P	5v	12mA		Output data rate clock
126	B/U/Pb_OUT_0	Tristate O/P	5v	8mA		Digital video output - Blue/U/Pb
127	B/U/Pb_OUT_1	Tristate O/P	5v	8mA		Digital video output - Blue/U/Pb
128	VDD7	Power				3.3 V - Power pin for IO
129	VSS	Ground				Ground
130	B/U/Pb_OUT_2	Tristate O/P	5v	8mA		Digital video output - Blue/U/Pb
131	B/U/Pb_OUT_3	Tristate O/P	5v	8mA		Digital video output - Blue/U/Pb
132	B/U/Pb_OUT_4	Tristate O/P	5v	8mA		Digital video output - Blue/U/Pb
133	B/U/Pb_OUT_5	Tristate O/P	5v	8mA		Digital video output - Blue/U/Pb
134	B/U/Pb_OUT_6	Tristate O/P	5v	8mA		Digital video output - Blue/U/Pb
135	B/U/Pb_OUT_7	Tristate O/P	5v	8mA		Digital video output - Blue/U/Pb
136	B/U/Pr_OUT_0	Tristate O/P	5v	8mA		Digital video output - Red/V/Pr
137	B/U/Pr_OUT_1	Tristate O/P	5v	8mA		Digital video output - Red/V/Pr
138	VDDcore7	Power				1.8 V - Power pin for core
139	VSScore	Ground				Ground
140	R/V/Pr_OUT_2	Tristate O/P	5v	8mA		Digital video output - Red/V/Pr
141	R/V/Pr_OUT_3	Tristate O/P	5v	8mA		Digital video output - Red/V/Pr
142	R/V/Pr_OUT_4	Tristate O/P	5v	8mA		Digital video output - Red/V/Pr
143	R/V/Pr_OUT_5	Tristate O/P	5v	8mA		Digital video output - Red/V/Pr
144	R/V/Pr_OUT_6	Tristate O/P	5v	8mA		Digital video output - Red/V/Pr
145	R/V/Pr_OUT_7	Tristate O/P	5v	8mA		Digital video output - Red/V/Pr
146	VDD8	Power				3.3 V - Power pin for IO
147	VSS	Ground				Ground
148	G/Y/Y_OUT_0	Tristate O/P	5v	8mA		Digital video output - Green/Y
149	G/Y/Y_OUT_1	Tristate O/P	5v	8mA		Digital video output - Green/Y
150	G/Y/Y_OUT_2	Tristate O/P	5v	8mA		Digital video output - Green/Y
151	G/Y/Y_OUT_3	Tristate O/P	5v	8mA		Digital video output - Green/Y
152	G/Y/Y_OUT_4	Tristate O/P	5v	8mA		Digital video output - Green/Y
153	G/Y/Y_OUT_5	Tristate O/P	5v	8mA		Digital video output - Green/Y
154	G/Y/Y_OUT_6	Tristate O/P	5v	8mA		Digital video output - Green/Y
155	G/Y/Y_OUT_7	Tristate O/P	5v	8mA		Digital video output - Green/Y
156	OE	Input	5v			Output data enable for digital video output
157	PLL_PVDD	Power				1.8 V - Power pin for PLL pads
158	PLL_PVSS	Ground				Ground for PLL pads
159	AVSS_PLL_BE1	Ground				PLL ground
160	AVDD_PLL_BE1	Power				1.8 V - Power pin for PLL
161	AVDD_PLL_BE2	Power				1.9 V - Power pin for PLL
162	AVSS_PLL_BE2	Ground				PLL ground
163	AVSS_PLL_SDI	Ground				PLL ground
164	AVDD_PLL_SDI	Power				1.8 V - Power pin for PLL
165	AVDD_PLL_FE	Power				1.9 V - Power pin for PLL
166	AVSS_PLL_FE	Ground				PLL ground
167	R_VSS	Ground				Ground
168	R_VDD1.8	Power				1.8 V
169	R_VSS	Ground				Ground
170	Reserved	-				Leave open
171	R_VDD	Power				3.3 V
172	R_VSS	Ground				Ground
173	Reserved	-				Leave open
174	R_VDD	Power				3.3 V
175	R_VSS	Ground				Ground

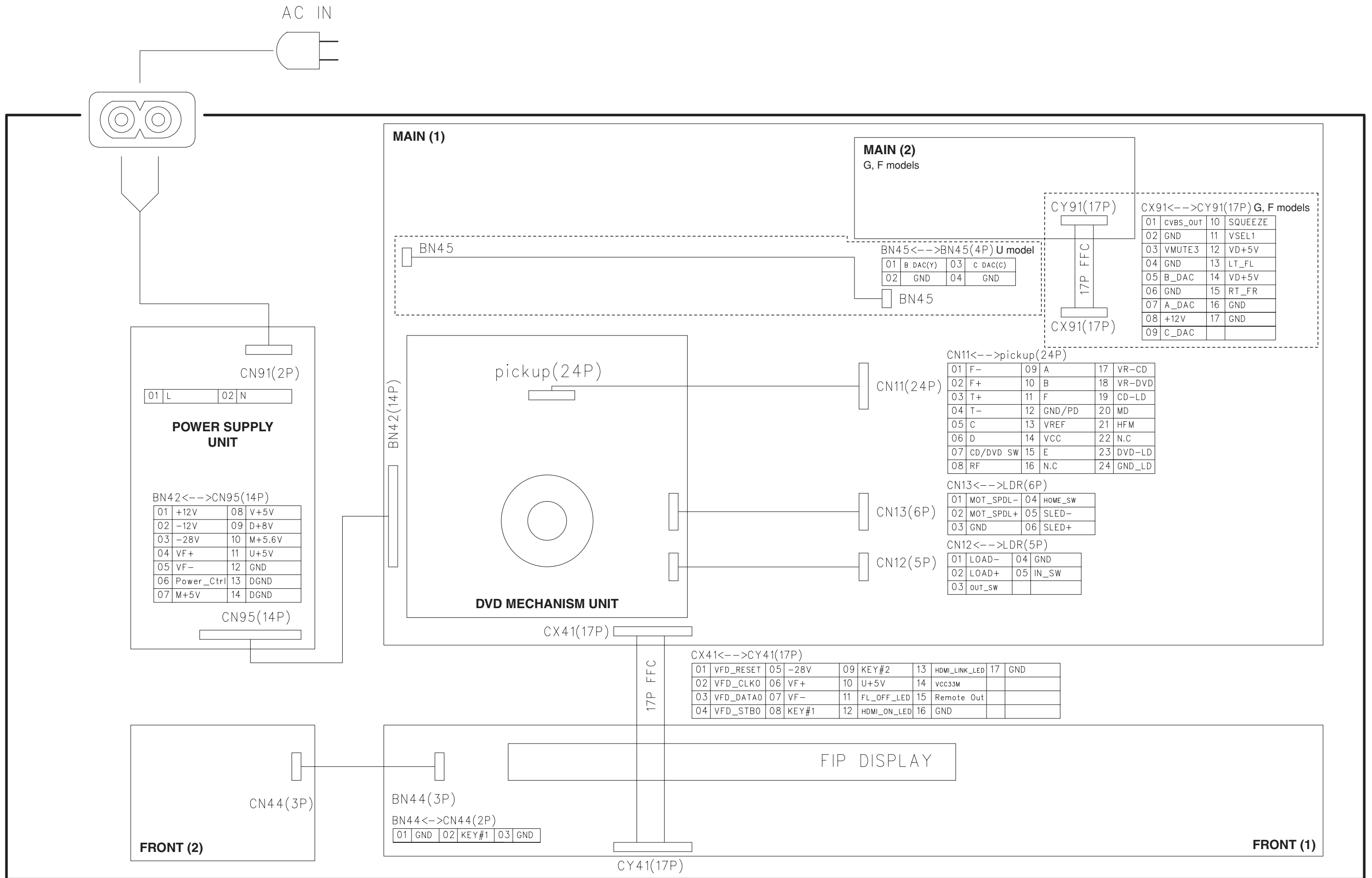
No.	Pin Name	I/O Type	Voltage Tolerance	Drive	Internal Pull-up/Pull-down	Description
176	Reserved	-				Leave open
177	R_VDD	Power				3.3 V
178	R_VSS	Ground				Ground
179	Reserved	-				Leave open
180	Reserved	-				Leave open
181	Reserved	-				Leave open
182	R_VSS	Ground				Ground
183	R_VDD	Power				3.3 V
184	R_VSS	Ground				Ground
185	R_VSS	Ground				Ground
186	R_VDD	Power				3.3 V
187	R_VDD	Power				3.3 V
188	TEST0	Input	5v			Test pin - Connect to ground
189	TEST1	Input	5v			Test pin - Connect to ground
190	TEST2	Input	5v			Test pin - Connect to ground
191	XTAL IN	Input				External parallel crystal oscillator
192	XTAL OUT	Output				External parallel crystal oscillator
193	VDD9	Power				3.3 V - Power pin for IO
194	VSS	Ground				Ground
195	IN_CLK_PORT2	Input	5v	4mA		Port2 - Data clock input
196	D1_IN_0	Input	5v	4mA		Port2 - ITU-R BT656 digital data input
197	VDDcore8	Power				1.8 V - Power pin for core
198	VSScore	Ground				Ground
199	D1_IN_1	Input	5v	4mA		Port2 - ITU-R BT656 digital data input
200	D1_IN_2	Input	5v	4mA		Port2 - ITU-R BT657 digital data input
201	D1_IN_3	Input	5v	4mA		Port2 - ITU-R BT658 digital data input
202	D1_IN_4	Input	5v	4mA		Port2 - ITU-R BT659 digital data input
203	D1_IN_5	Input	5v	4mA		Port2 - ITU-R BT660 digital data input
204	D1_IN_6	Input	5v	4mA		Port2 - ITU-R BT661 digital data input
205	D1_IN_7	Input	5v	4mA		Port2 - ITU-R BT662 digital data input
206	FIELD ID_PORT2	Input	5v	4mA		Port2 - Odd/Even field identification
207	VSYNC_PORT2	Input	5v	4mA		Port2 - Vertical sync or reference
208	HSYNC_PORT2	Input	5v	4mA		Port2 - Horizontal sync or reference

BLOCK DIAGRAM



1 ■ WIRING DIAGRAM

1
2
3
4
5
6
7

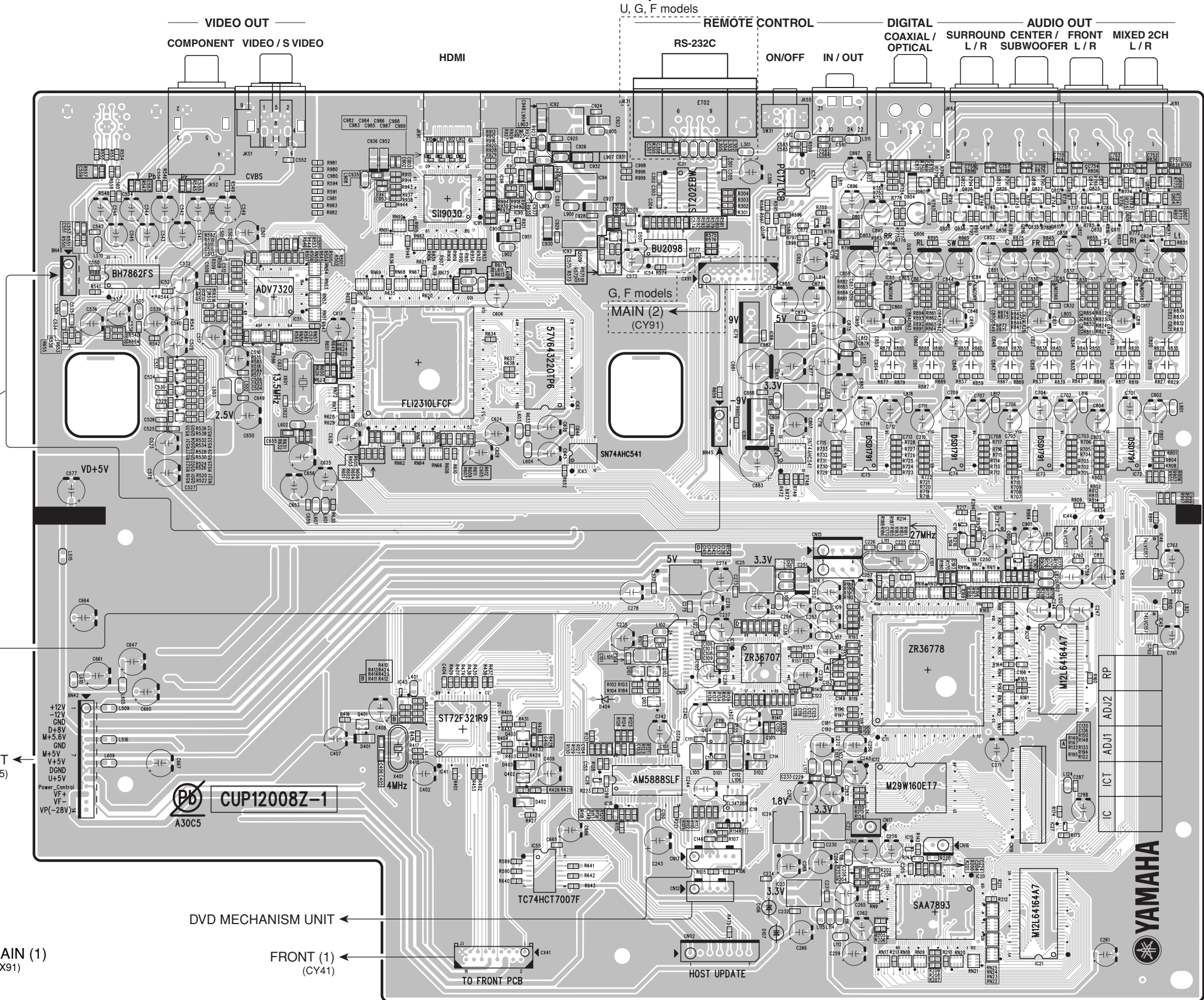
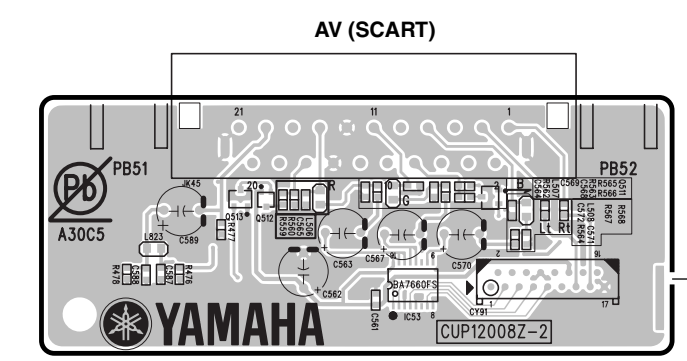


PRINTED CIRCUIT BOARDS

Note) The electrical parts available as servicing parts are those in the replacement parts list only. When replacement of any electrical part other than those in the list is necessary, replace the P.C.B. assembly which includes that part.

MAIN (1) P.C.B.
(Top view)

MAIN (2) P.C.B. (Top view)
G, F models



U model

DVD MECHANISM UNIT

POWER SUPPLY UNIT (CN95)

CUP12008Z-1
A30C5

DVD MECHANISM UNIT

FRONT (1) (CY41)

TO FRONT PCB

HOST UPDATE



A B C D E F G H I J

1

2

3

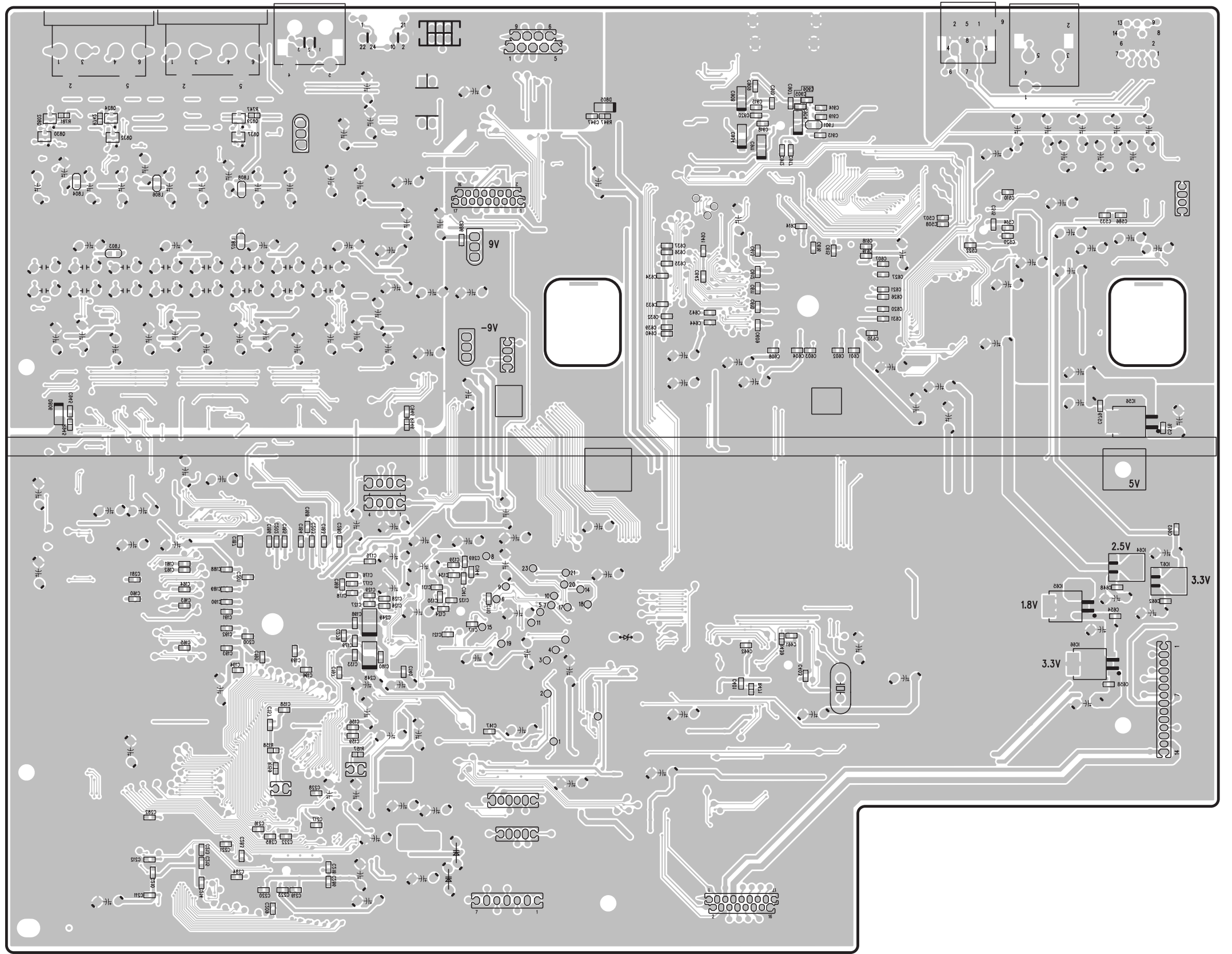
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5

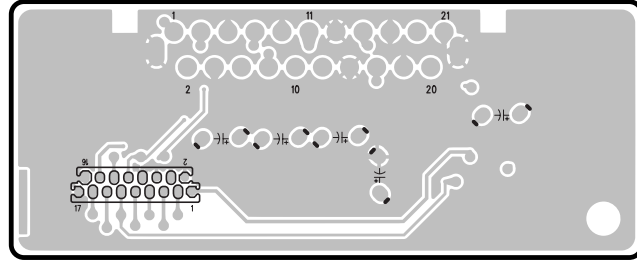
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7

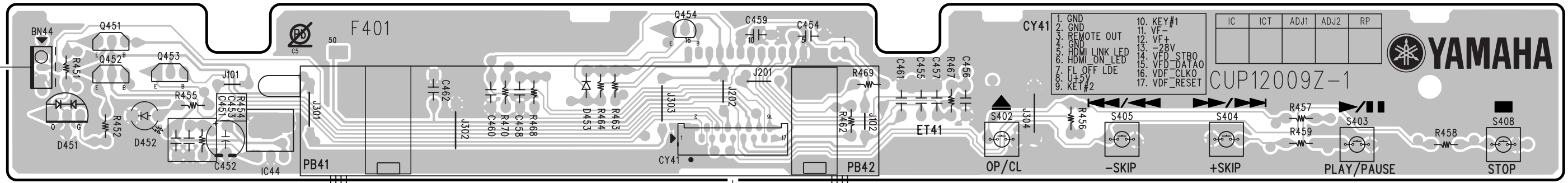
MAIN (1) P.C.B.
(Bottom view)



MAIN (2) P.C.B. (Bottom view)
G, F models

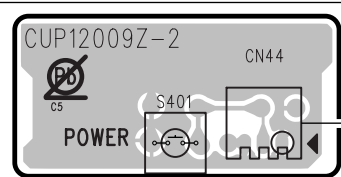


FRONT (1) P.C.B. (Top view)



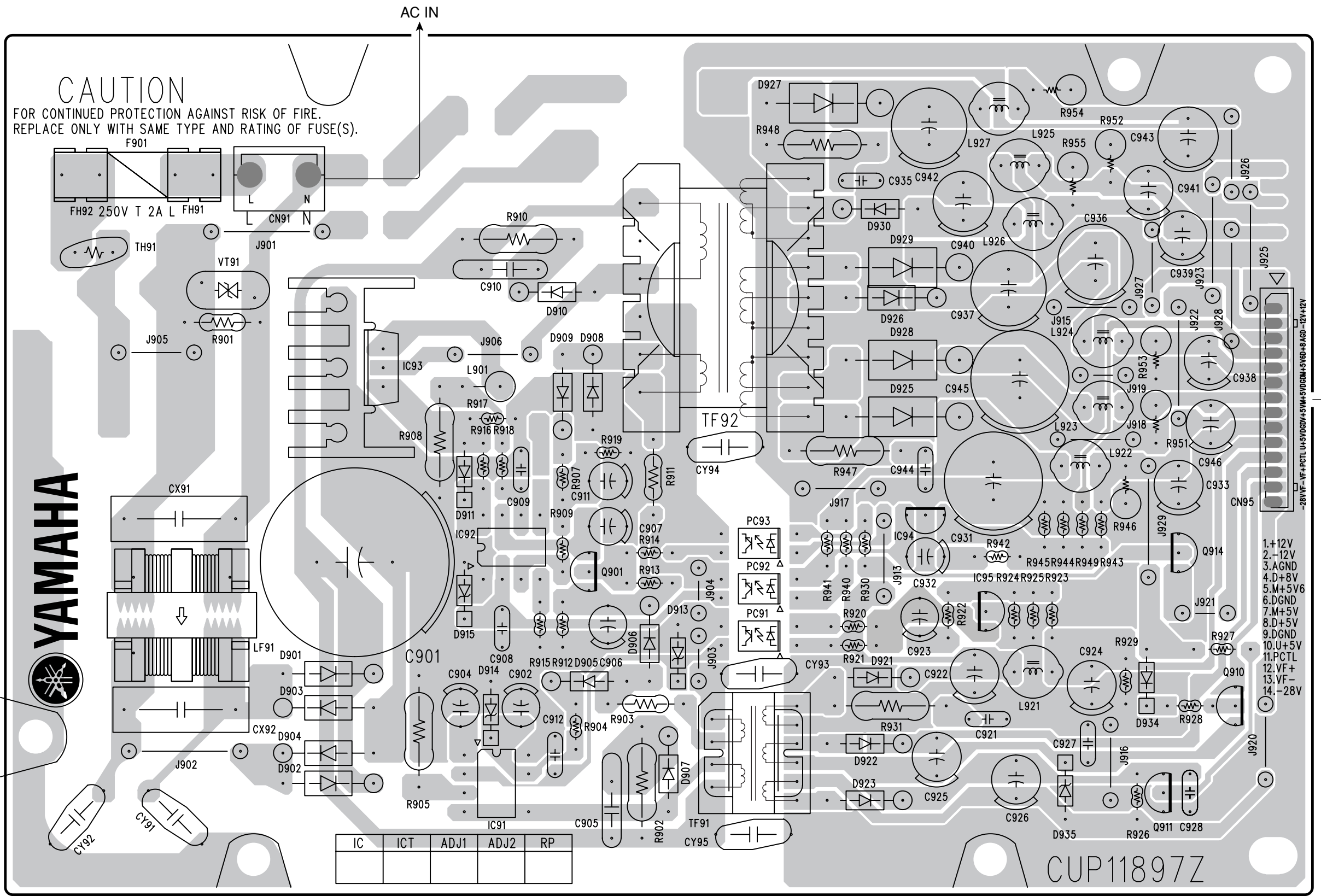
MAIN (1)
(CX41)

FRONT (2) P.C.B. (Top view)

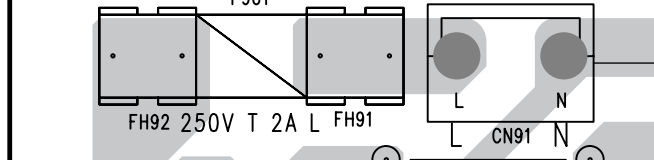


STANDBY
/ON

POWER SUPPLY UNIT (Top view)



CAUTION
 FOR CONTINUED PROTECTION AGAINST RISK OF FIRE,
 REPLACE ONLY WITH SAME TYPE AND RATING OF FUSE(S).



IC	ICT	ADJ1	ADJ2	RP

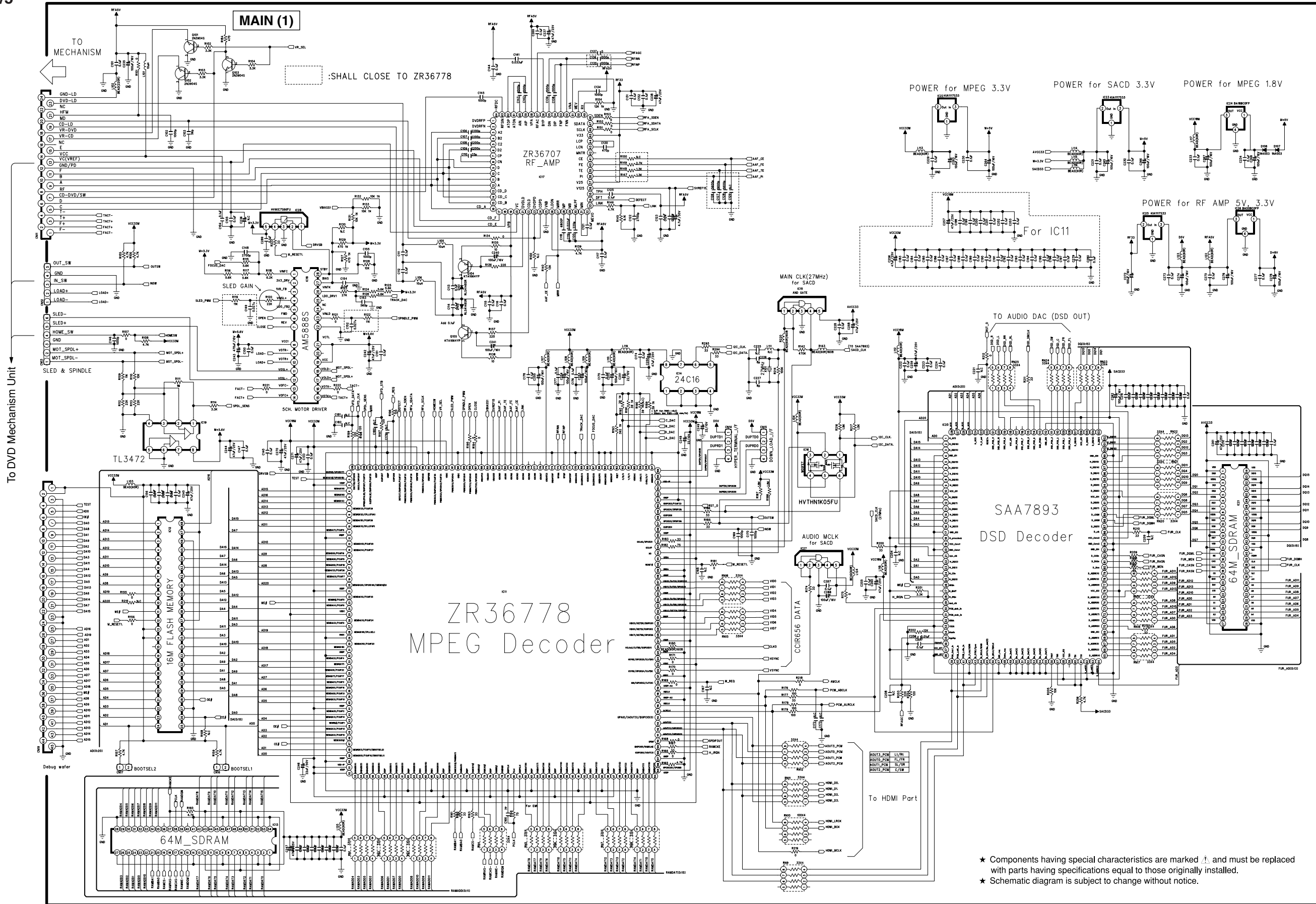
- 1.+12V
- 2.-12V
- 3.AGND
- 4.D+8V
- 5.M+5V6
- 6.DGND
- 7.M+5V
- 8.D+5V
- 9.DGND
- 10.U+5V
- 11.PCTL
- 12.VF+
- 13.VF-
- 14.-28V

CUP11897Z

SCHEMATIC DIAGRAMS

MAIN 1/5

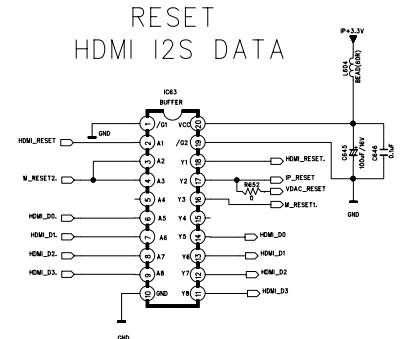
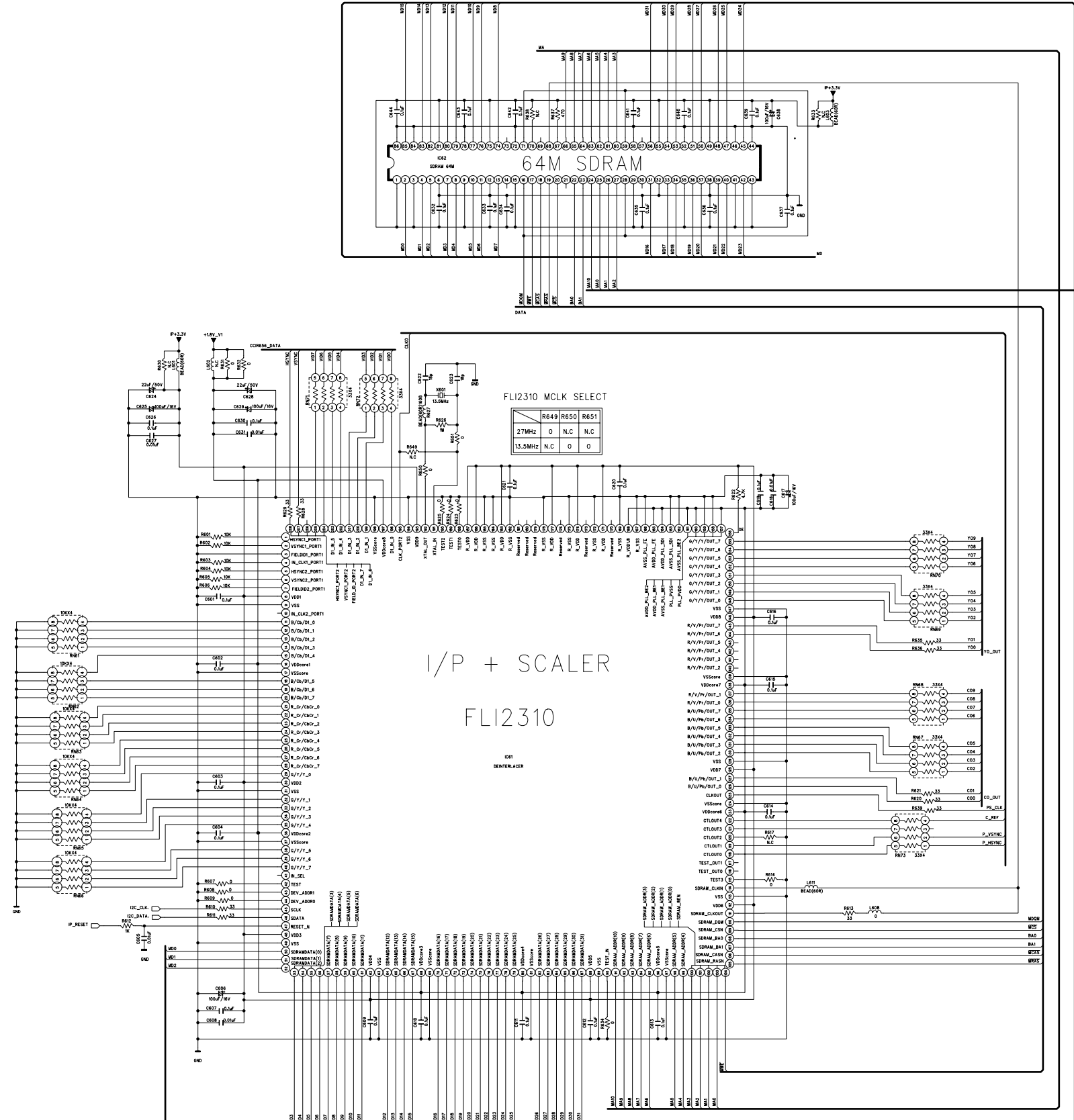
Note) The electrical parts available as servicing parts are those in the replacement parts list only. When replacement of any electrical part other than those in the list is necessary, replace the P.C.B. assembly which includes that part.



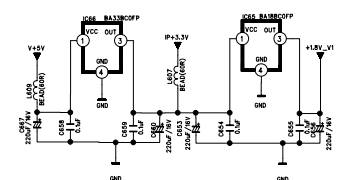
- ★ Components having special characteristics are marked Δ and must be replaced with parts having specifications equal to those originally installed.
- ★ Schematic diagram is subject to change without notice.

MAIN 2/5

MAIN (1)



POWER (I/P 3.3V, 1.8V)

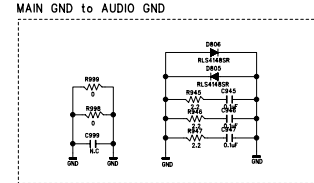


★ Components having special characteristics are marked Δ and must be replaced with parts having specifications equal to those originally installed.
 ★ Schematic diagram is subject to change without notice.

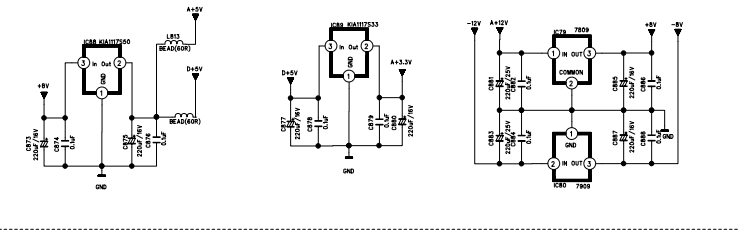
MAIN 3/5

MAIN (1)

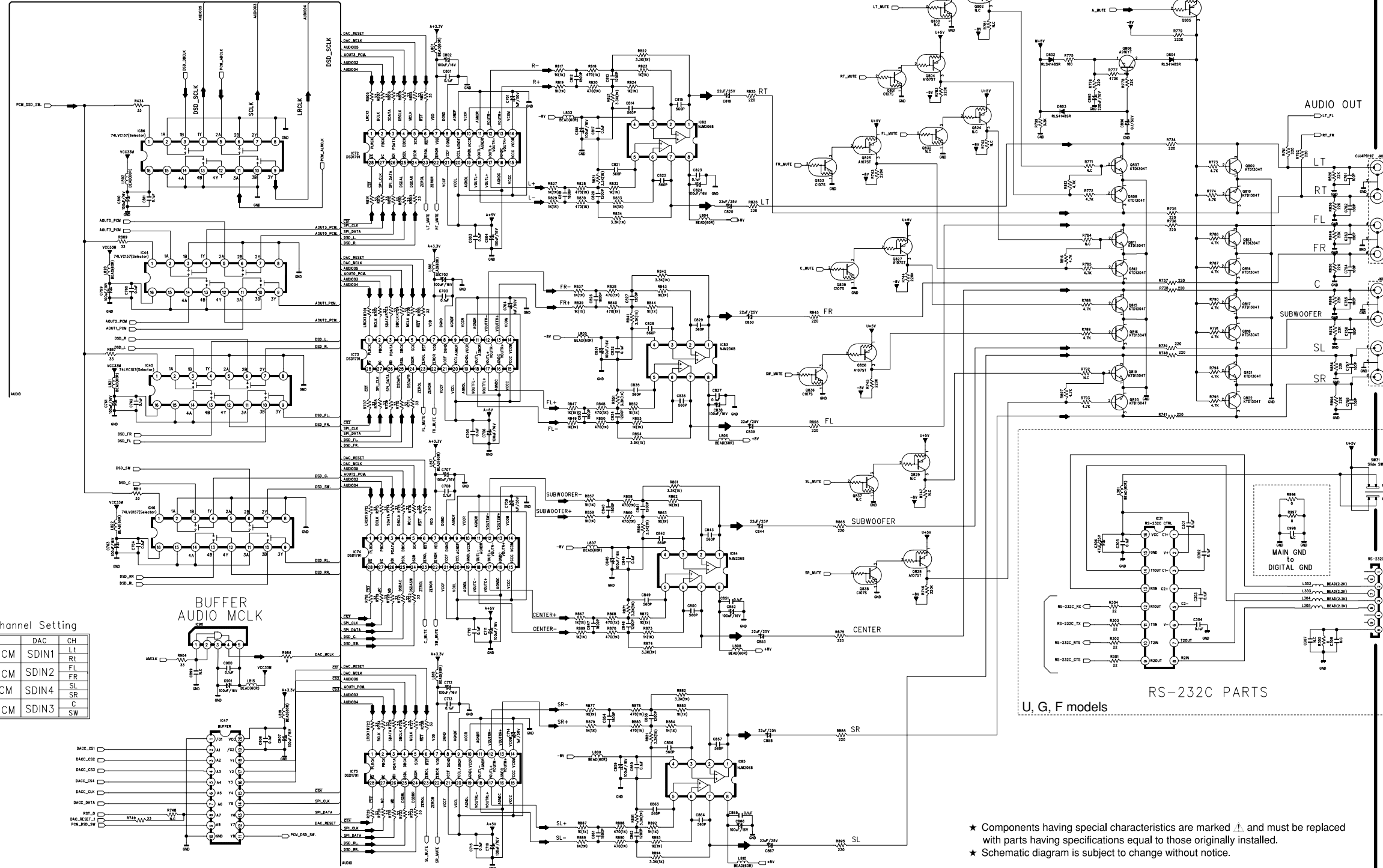
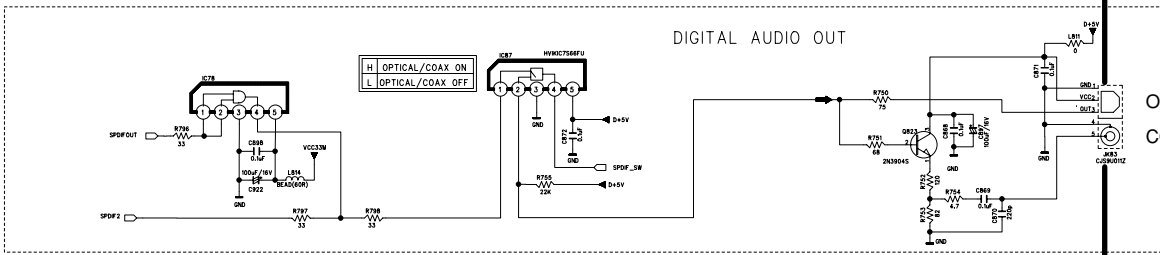
AUDIO PART



POWER(AUDIO DAC/OP AMP)



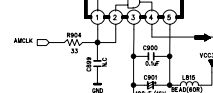
DIGITAL AUDIO OUT



AUDIO Channel Setting

MPEG	DAC	CH
AOUT3_PCM	SDIN1	LT
AOUT0_PCM	SDIN2	RT
AOUT1_PCM	SDIN4	FL
AOUT2_PCM	SDIN3	FR
		SL
		SR
		C
		SW

BUFFER AUDIO MCLK



OPTICAL COAXIAL

MIXED 2CH L/R

FRONT L/R

CENTER

SUBWOOFER

SURROUND L/R

ON/OFF

RS-232C

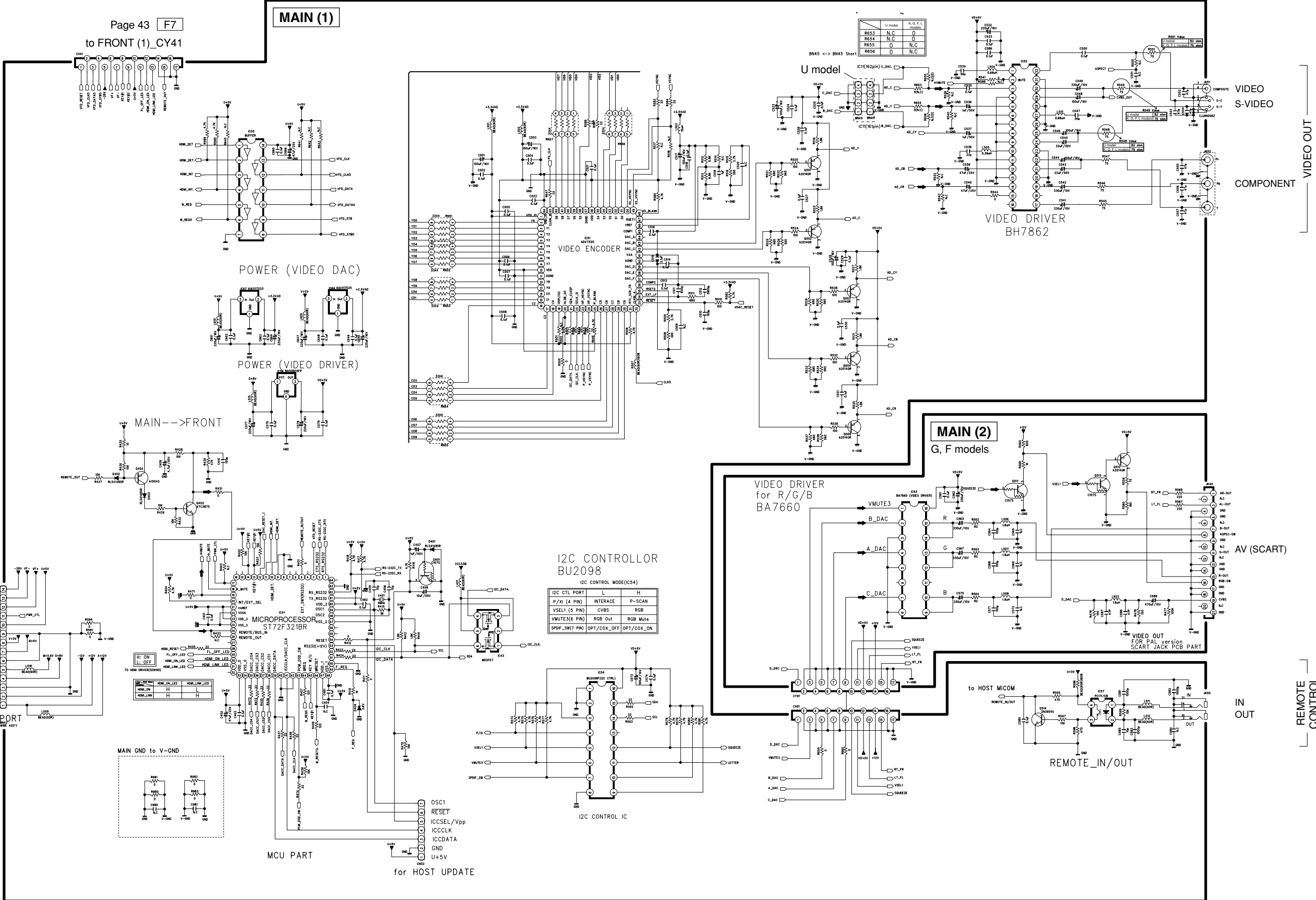
U, G, F models

RS-232C PARTS

- ★ Components having special characteristics are marked and must be replaced with parts having specifications equal to those originally installed.
- ★ Schematic diagram is subject to change without notice.

MAIN 4/5

★ Components having special characteristics are marked Δ and must be replaced with parts having specifications equal to those originally installed.
★ Schematic diagram is subject to change without notice.



Page 43 F7 to FRONT (1)_CY41

MAIN (1)

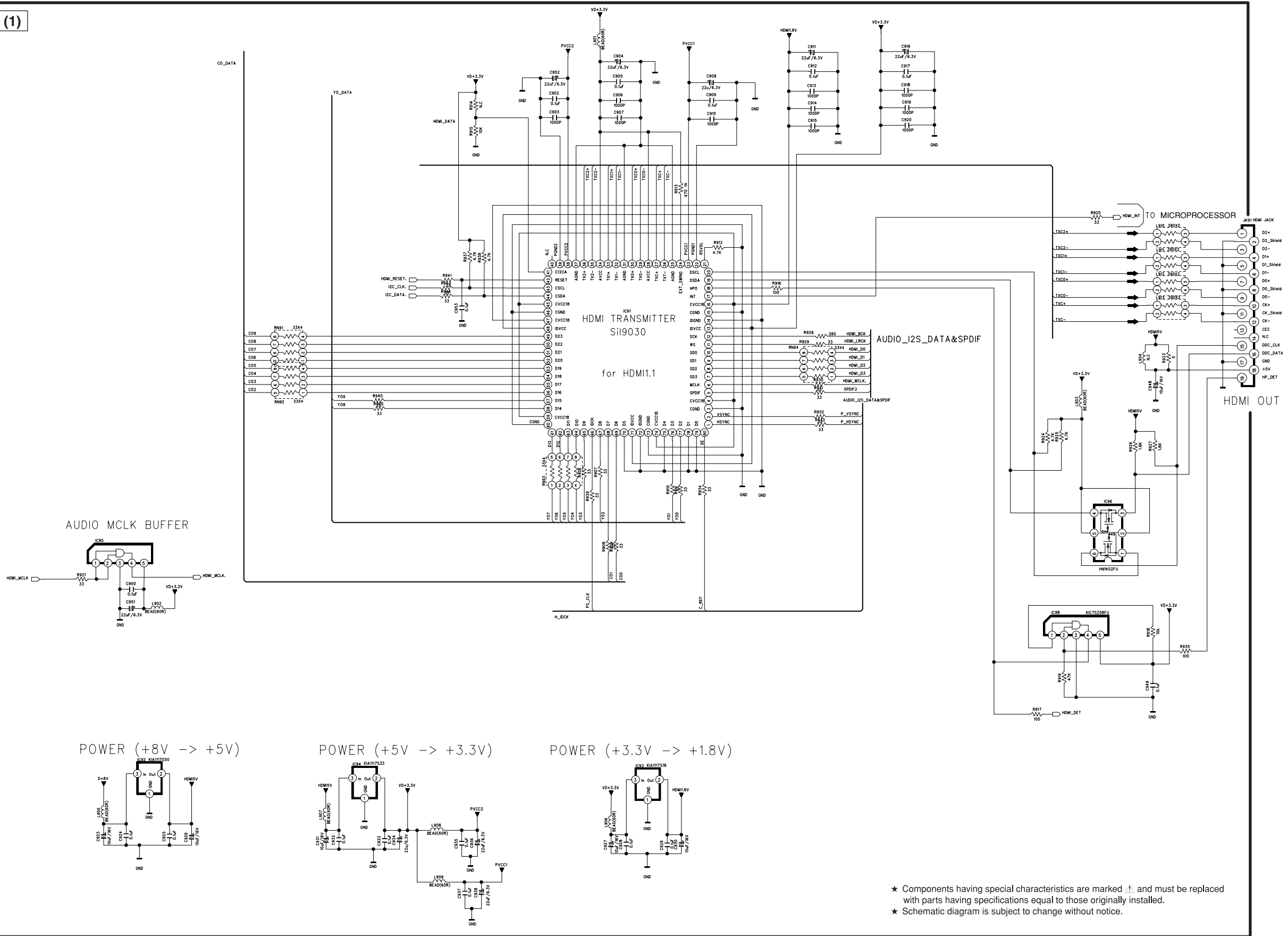
MAIN (2) G, F models


Page 44 J3 to POWER SUPPLY UNIT_CN95

MCU PART for HOST UPDATE

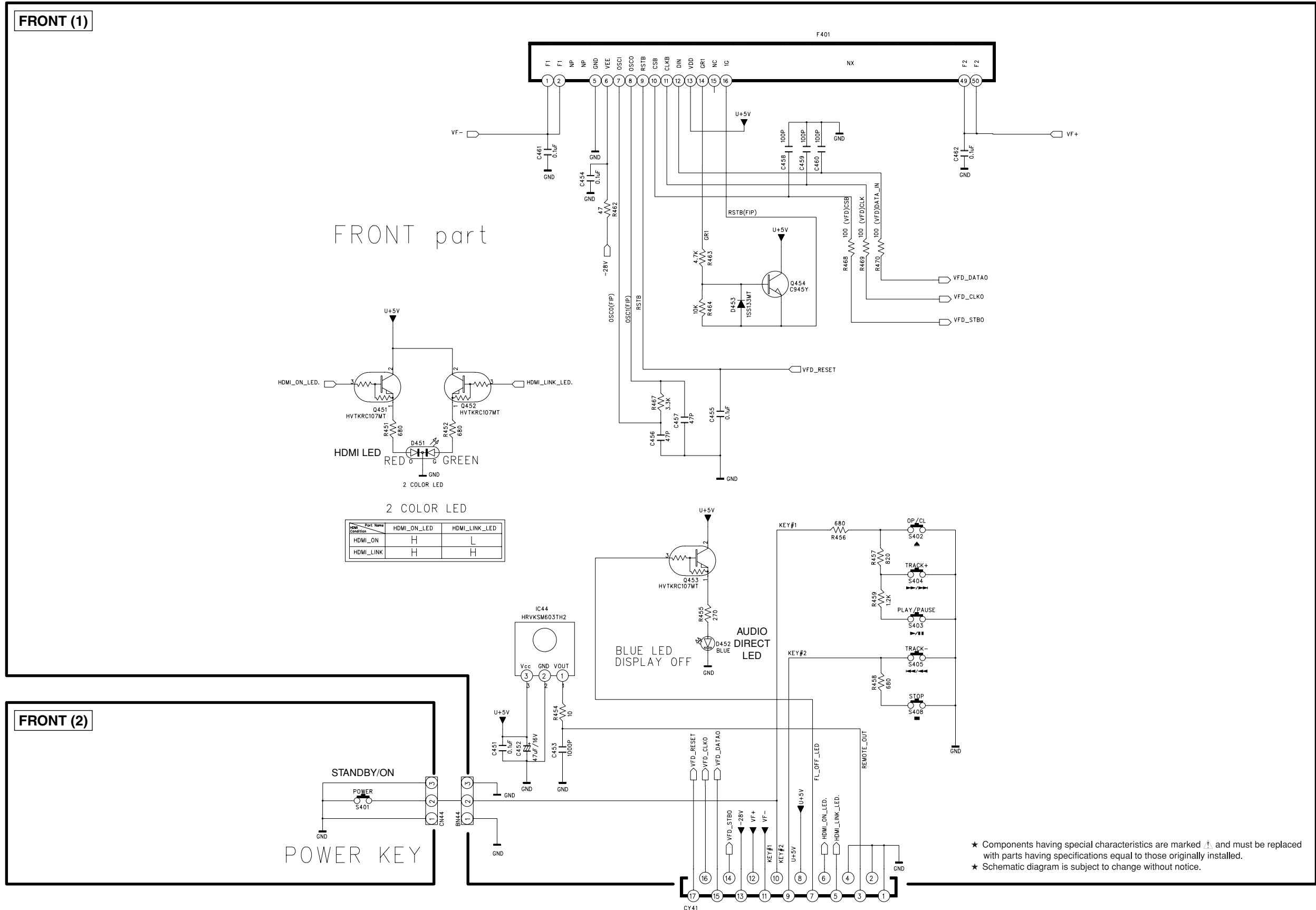
Page 44 J3 to POWER SUPPLY UNIT_CN95

MAIN (1)



★ Components having special characteristics are marked  and must be replaced with parts having specifications equal to those originally installed.
★ Schematic diagram is subject to change without notice.

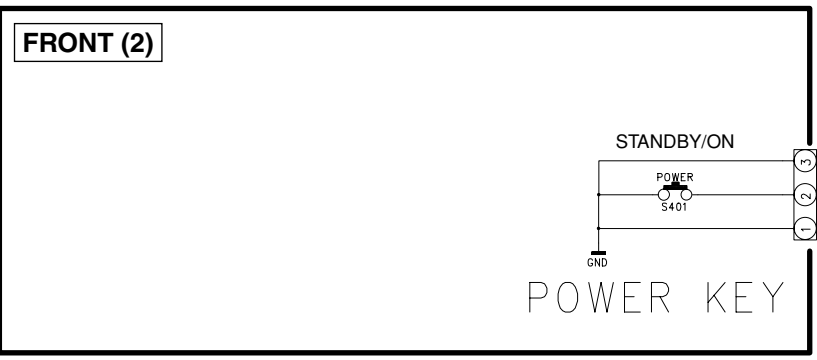
FRONT



FRONT part

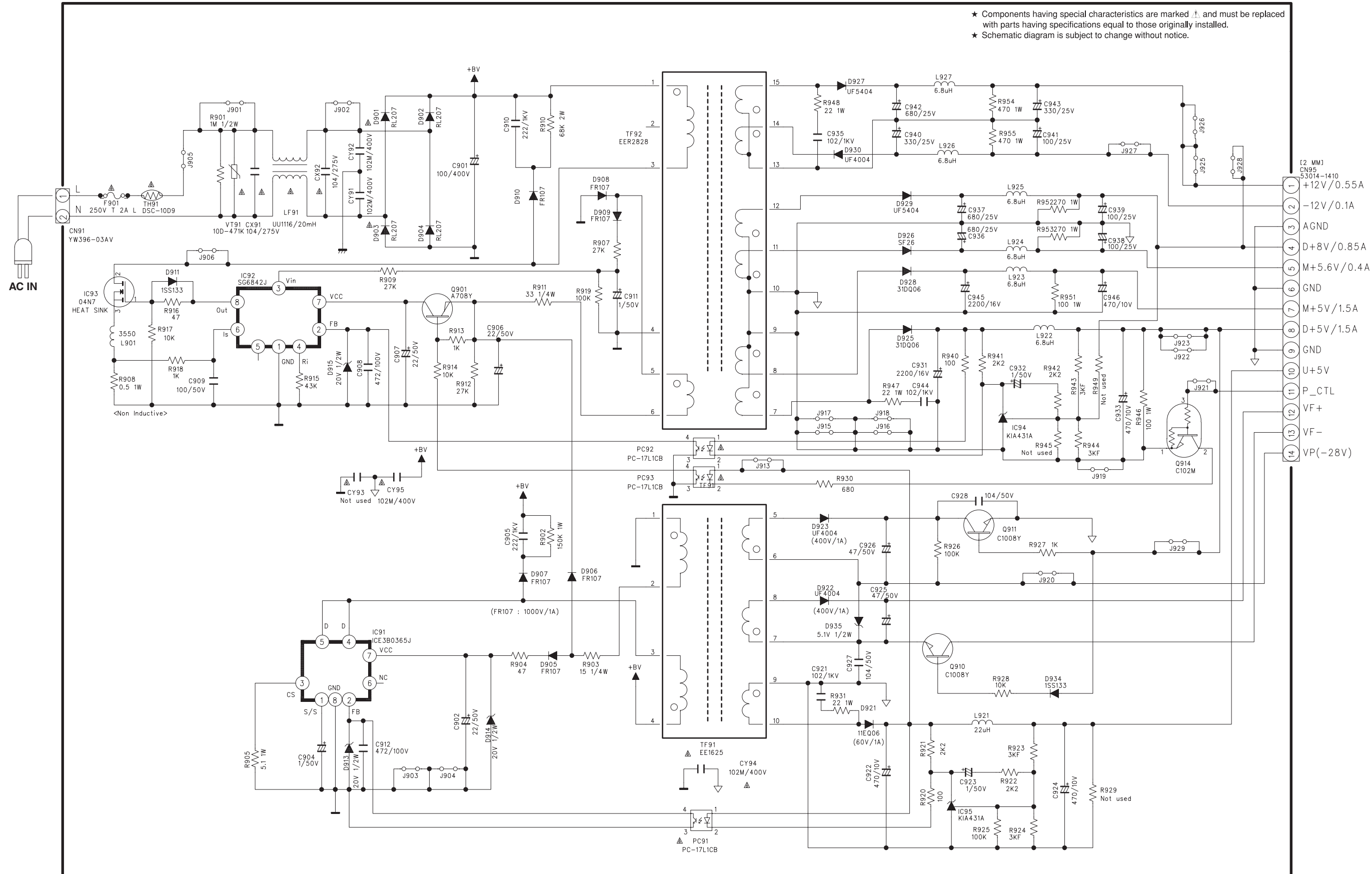
2 COLOR LED

Part Name	HDMI_ON_LED	HDMI_LINK_LED
HDMI_ON	H	L
HDMI_LINK	H	H



★ Components having special characteristics are marked Δ and must be replaced with parts having specifications equal to those originally installed.
 ★ Schematic diagram is subject to change without notice.

POWER SUPPLY UNIT



★ Components having special characteristics are marked Δ and must be replaced with parts having specifications equal to those originally installed.
 ★ Schematic diagram is subject to change without notice.

Page 41 B5
 to MAIN (1)_BN42

REPLACEMENT PARTS LIST

P.C.B. MAIN and P.C.B. FRONT

ELECTRICAL COMPONENT PARTS

WARNING

- Components having special characteristics are marked Δ and must be replaced with parts having specifications equal to those originally installed.

ABBREVIATIONS IN THIS LIST ARE AS FOLLOWS:

- | | |
|--|--|
| C.A.EL.CHP : CHIP ALUMI.ELECTROLYTIC CAP | L.EMIT : LIGHT EMITTING MODULE |
| C.CE : CERAMIC CAP | LED.DSPLY : LED DISPLAY |
| C.CE.ARRAY : CERAMIC CAP ARRAY | LED.INFRD : LED,INFRARED |
| C.CE.CHP : CHIP CERAMIC CAP | MODUL.RF : MODULATOR,RF |
| C.CE.ML : MULTILAYER CERAMIC CAP | PHOT.CPL : PHOTO COUPLER |
| C.CE.M.CHP : CHIP MULTILAYER CERAMIC CAP | PHOT.INTR : PHOTO INTERRUPTER |
| C.CE.SAFETY : RECOGNIZED CERAMIC CAP | PHOT.RFLCT : PHOTO REFLECTOR |
| C.CE.TUBLR : CERAMIC TUBULAR CAP | PIN.TEST : PIN,TEST POINT |
| C.CE.SMI : SEMI CONDUCTIVE CERAMIC CAP | PLST.RIVET : PLASTIC RIVET |
| C.EL : ELECTROLYTIC CAP | R.ARRAY : RESISTOR ARRAY |
| C.MICA : MICA CAP | R.CAR. : CARBON RESISTOR |
| C.ML.FLM : MULTILAYER FILM CAP | R.CAR.CHP : CHIP RESISTOR |
| C.MP : METALLIZED PAPER CAP | R.CAR.FP : FLAME PROOF CARBON RESISTOR |
| C.MYLAR : MYLAR FILM CAP | R.FUS : FUSABLE RESISTOR |
| C.MYLAR.ML : MULTILAYER MYLAR FILM CAP | R.MTL.CHP : CHIP METAL FILM RESISTOR |
| C.PAPER : PAPER CAPACITOR | R.MTL.FLM : METAL FILM RESISTOR |
| C.PLS : POLYSTYRENE FILM CAP | R.MTL.OXD : METAL OXIDE FILM RESISTOR |
| C.POL : POLYESTER FILM CAP | R.MTL.PLAT : METAL PLATE RESISTOR |
| C.POLY : POLYETHYLENE FILM CAP | RSNR.CE : CERAMIC RESONATOR |
| C.PP : POLYPROPYLENE FILM CAP | RSNR.CRYS : CRYSTAL RESONATOR |
| C.TNTL : TANTALUM CAP | R.TW.CEM : TWIN CEMENT FIXED RESISTOR |
| C.TNTL.CHP : CHIP TANTALUM CAP | R.CEMENT : CEMENT RESISTOR |
| C.TRIM : TRIMMER CAP | SCR.BND.HD : BIND HEAD B-TIGHT SCREW |
| CN : CONNECTOR | SCR.BW.HD : BW HEAD TAPPING SCREW |
| CN.BS.PIN : CONNECTOR,BASE PIN | SCR.CUP : CUP TIGHT SCREW |
| CN.CANNON : CONNECTOR,CANNON | SCR.TERM : SCREW TERMINAL |
| CN.DIN : CONNECTOR,DIN | SCR.TR : SCREW,TRANSISTOR |
| CN.FLAT : CONNECTOR,FLAT CABLE | SUPRT.PCB : SUPPORT,P.C.B. |
| CN.POST : CONNECTOR,BASE POST | SURG.PRTCT : SURGE PROTECTOR |
| COIL.MX.AM : COIL,AM MIX | SW.TACT : TACT SWITCH |
| COIL.AT.FM : COIL,FM ANTENNA | SW.LEAF : LEAF SWITCH |
| COIL.DT.FM : COIL,FM DETECT | SW.LEVER : LEVER SWITCH |
| COIL.MX.FM : COIL,FM MIX | SW.MICRO : MICRO SWITCH |
| COIL.OUTPT : OUTPUT COIL | SW.PUSH : PUSH SWITCH |
| DIOD.ARRAY : DIODE ARRAY | SW.RT.ENC : ROTARY ENCODER |
| DIODE.BRG : DIODE BRIDGE | SW.RT.MTR : ROTARY SWITCH WITH MOTOR |
| DIODE.CHP : CHIP DIODE | SW.RT : ROTARY SWITCH |
| DIODE.VAR : VARACTOR DIODE | SW.SLIDE : SLIDE SWITCH |
| DIOD.Z.CHP : CHIP ZENER DIODE | TERM.SP : SPEAKER TERMINAL |
| DIODE.ZENR : ZENER DIODE | TERM.WRAP : WRAPPING TERMINAL |
| DSCR.CE : CERAMIC DISCRIMINATOR | THRMST.CHP : CHIP THERMISTOR |
| FER.BEAD : FERRITE BEADS | TR.CHP : CHIP TRANSISTOR |
| FER.CORE : FERRITE CORE | TR.DGT : DIGITAL TRANSISTOR |
| FET.CHP : CHIP FET | TR.DGT.CHP : CHIP DIGITAL TRANSISTOR |
| FL.DSPLY : FLUORESCENT DISPLAY | TRANS : TRANSFORMER |
| FLTR.CE : CERAMIC FILTER | TRANS.PULS : PULSE TRANSFORMER |
| FLTR.COMB : COMB FILTER MODULE | TRANS.PWR : POWER TRANSFORMER ASS'Y |
| FLTR.LC.RF : LC FILTER,EMI | TUNER.AM : TUNER PACK,AM |
| GND.MTL : GROUND PLATE | TUNER.FM : TUNER PACK,FM |
| GND.TERM : GROUND TERMINAL | TUNER.PK : FRONT-ENDTUNER PACK |
| HOLDER.FUS : FUSE HOLDER | VR : ROTARY POTENTIOMETER |
| IC.PRTCT : IC PROTECTOR | VR.MTR : POTENTIOMETER WITH MOTOR |
| JUMPER.CN : JUMPER CONNECTOR | VR.SW : POTENTIOMETER WITH ROTARY SW |
| JUMPER.TST : JUMPER,TEST POINT | VR.SLIDE : SLIDE POTENTIOMETER |
| L.DTCT : LIGHT DETECTING MODULE | VR.TRIM : TRIMMER POTENTIOMETER |

Note) The electrical parts available as servicing parts are those in the replacement parts list only. When replacement of any electrical part other than those in the list is necessary, replace the P.C.B. assembly which includes that part.

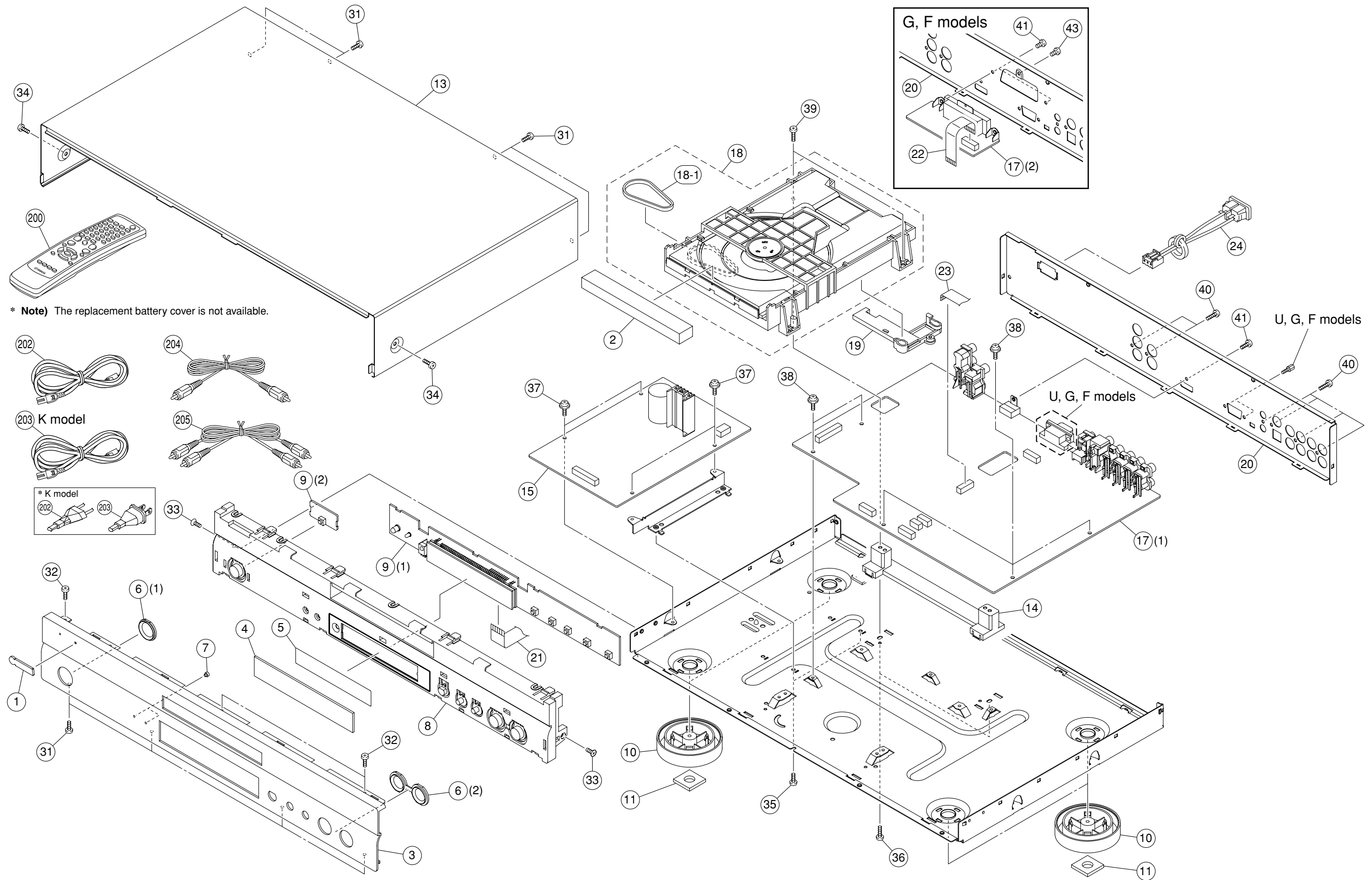
Ref. No.	Part No.	Description	Markets
*	AAX84140	P. C. B. MAIN	U
*	AAX84150	P. C. B. MAIN	KL
*	AAX84130	P. C. B. MAIN	GF
	IC11	AAX80840 IC	ZR36778
	IC13	AAX80810 IC	M12L64164A7T
	IC17	AAX80830 IC	ZR36707
	IC18	AAX80780 IC	AM5888SLF
	IC20	AAX80820 IC	SAA7893HLC2
	IC21	AAX80810 IC	M12L64164A7T
*	IC44-46	AAX80990 IC	74LVC157ADBR
	IC51	AAX80760 IC	ADV7320KSTZ
	IC52	AAX80740 IC	BH7862FS
	IC53	AAX80790 IC	BA7660FS
	IC61	AAX80770 IC	FL12310LFCF
	IC62	AAX80750 IC	57V643220TP6
*	IC72-75	AAX84110 IC	DSD1791DBRY
	IC82-85	AAX83130 IC	NJM2068MDTE1
*	IC86	AAX80990 IC	74LVC157ADBR
	JK31	AAX80150 CN. RS232C	D-SUB 9P UGF
*	JK45	AAX84160 CN. SCART	SCART 21P GF
	JK51	AAX80370 PIN JACK	S-VIDEO/VIDEO
	JK52	AAX80440 PIN JACK	COMPONENT 3P
	JK55	AAX80330 PIN JACK	REMOTE I/O 2P
	JK81	AAX80320 PIN JACK	4P L/R
	JK82	AAX80450 PIN JACK	4P C, SW, SUR. L/R
	JK83	AAX80360 CN. OPT/COA	OPT 1P/COAX 1P
	JK91	AAX80340 CN. HDM I	TYPE-A 19P
	SW31	AAX80380 SW. SLIDE	REMOTE ON/OFF UGF
*	AAX84120	P. C. B. FRONT	
	F401	AAX80850 DISPLAY	HCA14SM16
	IC44	AAX83550 SENSER. RC	KSM603TH2A
*	S401-405	AAX84170 SW. TACT	
*	S408	AAX84170 SW. TACT	

Ref. No.	Part No.	Description	Markets
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* New Parts

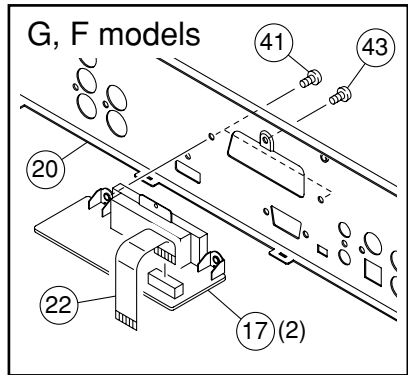
* New Parts

• OVERALL ASS'Y



* Note) The replacement battery cover is not available.

* K model
202 203



U, G, F models

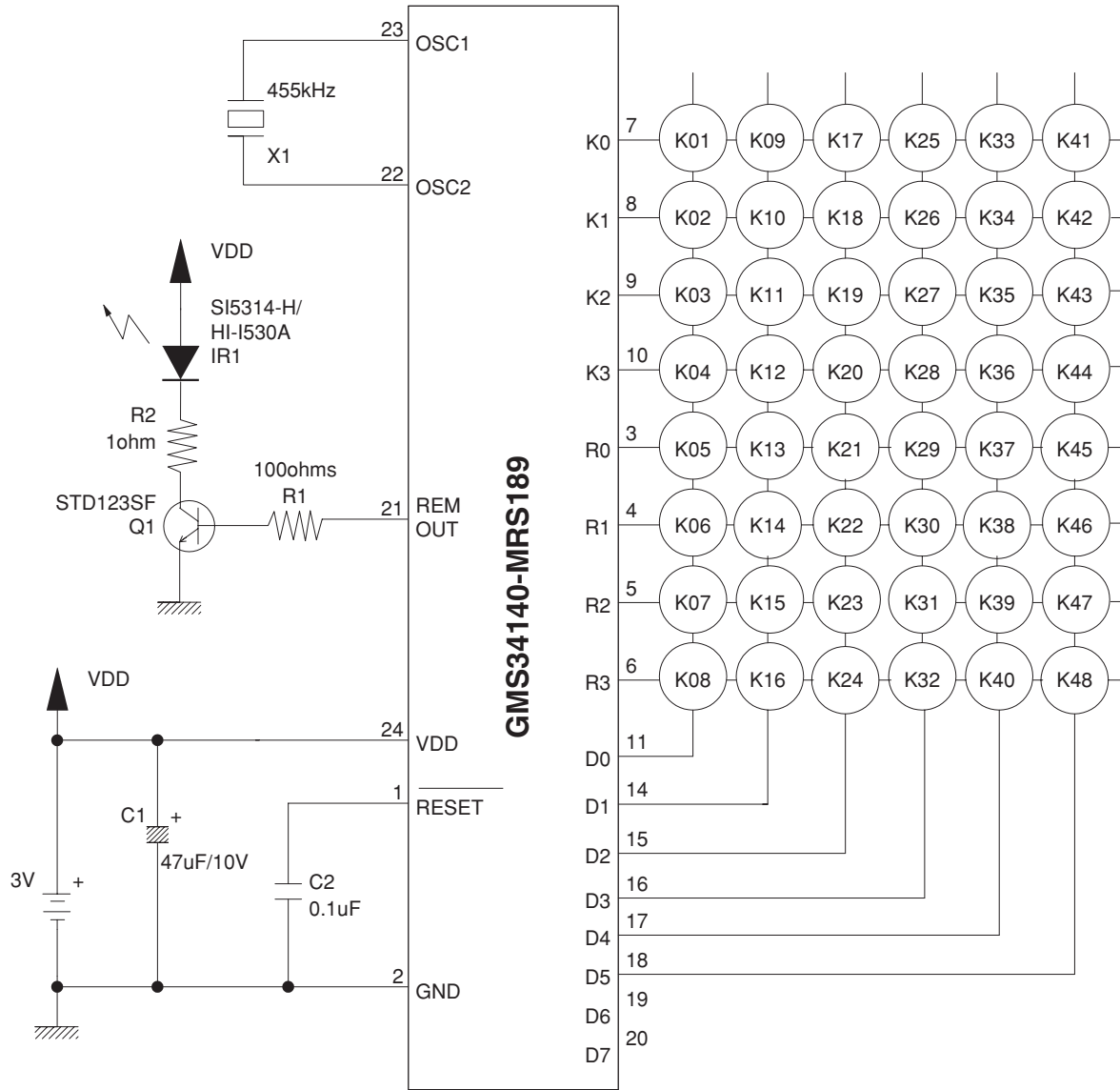
U, G, F models

Ref. No.	Part No.	Description	Remarks	Markets	
1	AAx80210	BADGE	GD	CGB1A167Y	
1	AAx80220	BADGE	BL, TI	CGB1A167Z	
2	AAx80400	DOOR (TRAY LID)	GD	CGR1A401M9YH54	
2	AAx80410	DOOR (TRAY LID)	BL	CGR1A401ZH53	
2	AAx80390	DOOR (TRAY LID)	TI	CGR1A401M7XH55	
3	AAx84200	FRONT PANEL	GD	CKM1A177YV55	
3	AAx84190	FRONT PANEL	BL	CKM1A177WC59	
3	AAx84180	FRONT PANEL	TI	CKM1A177UC60	
4	AAx80070	WINDOW		CGU1A395Z	
5	AAx80080	FILTER FIP		CMZ1A116Z	
6	AAx80200	ORNAMENT KNOB	GD	CGR1A402M9D6	
6	AAx80180	ORNAMENT KNOB	BL	CGR1A402K128	
6	AAx80190	ORNAMENT KNOB	TI	CGR1A402M7G41	
7	AAx80090	INDICATOR LED LENS		CGL1A253Z	
8	AAx80290	PANEL SUB	GD	CGW1A423M9YD6	
8	AAx80300	PANEL SUB	BL	CGW1A423ZK128	
8	AAx80280	PANEL SUB	TI	CGW1A423M7XG41	
9	AAx84120	P.C.B. ASS'Y	FRONT	COP12009B	
10	AAx78660	FOOT	GD	CKL1A192H57	
10	AAx78650	FOOT	BL, TI	CKL1A192H56	
11	AAx76760	CUSHION FOOT		CHG1A329	
13	AAx80040	TOP COVER	GD	CKC1A173D8	
13	AAx78320	TOP COVER	BL	CKC1A173B11	
13	AAx78330	TOP COVER	TI	CKC1A173G40	
14	AAx80310	SUPPORT DVD MECHANISM		CMH1A258	
15	AAx80690	POWER SUPPLY UNIT		COP11897B	
17	AAx84140	P.C.B. ASS'Y	MAIN	COP12008C	U
17	AAx84150	P.C.B. ASS'Y	MAIN	COP12008D	KL
17	AAx84130	P.C.B. ASS'Y	MAIN	COP12008B	GF
18	AAx80060	DVD MECHANISM UNIT		CADDVD27ZA	
18-1	AAx74670	BELT		CHG1A330	
19	AAx80270	GUIDE CABLE		CMH1A250	
20	AAx84220	PANEL REAR		CKF2A314X	U
20	AAx84230	PANEL REAR		CKF4A314V	K
20	AAx84210	PANEL REAR		CKF1A314Y	G
20	AAx87770	PANEL REAR		CKF1A314X	F
20	AAx84240	PANEL REAR		CKF4A314W	L
21	AAx80240	FLEXIBLE FLAT CABLE	17P 80mm P=1 A-A	CWC1B4A17A080A	
22	AAx80250	FLEXIBLE FLAT CABLE	17P 80mm P=1 A-B	CWC1B4A17A080B	GF
23	AAx80260	FLEXIBLE FLAT CABLE	24P 250mm P=0.5	CWC1G2A24G250B	
24	AAx80170	INLET ASS'Y	2P 100mm	CWZDVD37EUBN91A	
31	AAx74180	BIND HEAD BONDING B-T. SCREW	GD, TI 3x8 MFZN2W3	CTBD3+8JFC	
31	AAx80490	BIND HEAD BONDING B-T. SCREW	BL 3x8 MFZN2B3	CTBD3+8JFZR	
32	AAx80430	BIND HEAD SCREW	3x6 MFZN2B3	CTB3+6FFZR	
33	AAx80600	FLAT HEAD B-TIGHT SCREW	3x8 MFZN2Y	CTS3+8JR	
34	AAx73500	BIND HEAD B-TIGHT SCREW	GD, TI 3x8 MFZN2W3	CTB3+8JFC	
34	AAx78380	BIND HEAD B-TIGHT SCREW	BL 3x8 MFZN2B3	CTB3+8JFZR	
35	AAx80420	BIND HEAD B-TIGHT SCREW	3x6 MFZN2Y	CTB3+6JR	
36	AAx78400	BIND HEAD P-TIGHT SCREW	3x10 MFZN2B3	CTB3+10GFZR	
37	AAx80140	PW HEAD B-TIGHT SCREW	3x8 MFZN2Y	CTW3+8JR	
38	AAx80140	PW HEAD B-TIGHT SCREW	3x8 MFZN2Y	CTW3+8JR	
39	AAx78400	BIND HEAD P-TIGHT SCREW	3x10 MFZN2B3	CTB3+10GFZR	
40	AAx78400	BIND HEAD P-TIGHT SCREW	3x10 MFZN2B3	CTB3+10GFZR	
41	AAx80430	BIND HEAD SCREW	3x6 MFZN2B3	CTB3+6FFZR	
42	AAx78400	BIND HEAD P-TIGHT SCREW	3x10 MFZN2B3	CTB3+10GFZR	
43	AAx80700	SPECIAL SCREW		CHD1A055R	GF
		ACCESSORIES			
200	AAx80570	REMOTE CONTROL	DVD-14	CARTDVS1700	
202	AAx80620	POWER CABLE	2m 1pc	CJA2A085Z	U
202	AAx80640	POWER CABLE	2m 1pc	CJA2D089Z	K
202	AAx80630	POWER CABLE	2m 1pc	CJA2B020Z	GFL
203	AAx80660	POWER CABLE	2m 1pc	CJA2L090Z	K
204	AAx80580	VIDEO PIN CABLE	1P 1m 1pc	CJS4M033Z	
205	AAx80590	AUDIO PIN CABLE	2P 1m 1pc	CJS4N016Z	
		BATTERY	R03, AAA, UM-4 2pcs		

* New Parts

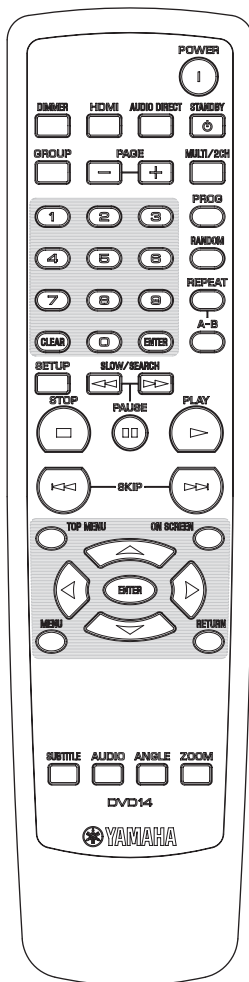
REMOTE CONTROL

• SCHEMATIC DIAGRAM

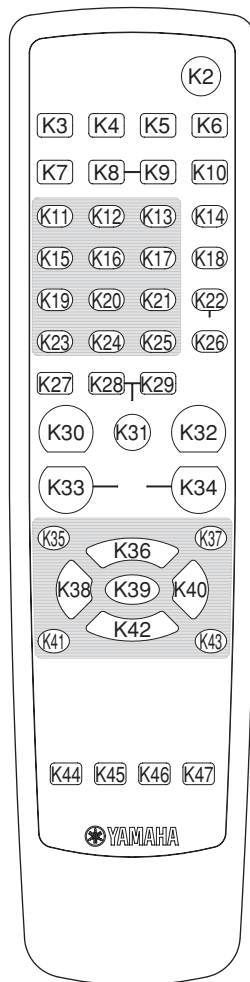


DVD-S1800

- PANEL



- KEY NO. LAYOUT



- KEY CODE

Key no.	Function	Custom code
K1	—	—
K2	POWER	7C-F6
K3	DIMMER	7C-A9
K4	HDMI	7C-E5
K5	AUDIO DIRECT	7C-D9
K6	STANDBY	7C-F7
K7	GROUP	7C-DD
K8	PAGE-	7C-DE
K9	PAGE+	7C-DF
K10	MULTI/2CH	7C-E1
K11	1	7C-94
K12	2	7C-95
K13	3	7C-96
K14	PROG	7C-A0
K15	4	7C-97
K16	5	7C-98
K17	6	7C-99
K18	RANDOM	7C-A1
K19	7	7C-9A
K20	8	7C-9B
K21	9	7C-9C
K22	REPEAT	7C-A3
K23	CLEAR	7C-9F
K24	0	7C-93
K25	ENTER	7C-B8
K26	A-B	7C-A4
K27	SETUP	7C-AC
K28	SLOW/SEARCH ◀	7C-86
K29	SLOW/SEARCH ▶	7C-87
K30	STOP ■	7C-85
K31	PAUSE ■■	7C-83
K32	PLAY ▶	7C-82
K33	SKIP ◀◀	7C-B9
K34	SKIP ▶▶	7C-BA
K35	TOP MENU	7C-B1
K36	▲	7C-B4
K37	ON SCREEN	7C-A6
K38	◀	7C-B5
K39	ENTER	7C-B8
K40	▶	7C-B6
K41	MENU	7C-B2
K42	▼	7C-B3
K43	RETURN	7C-B7
K44	SUBTITLE	7C-AA
K45	AUDIO	7C-AD
K46	ANGLE	7C-AE
K47	ZOOM	7C-D7