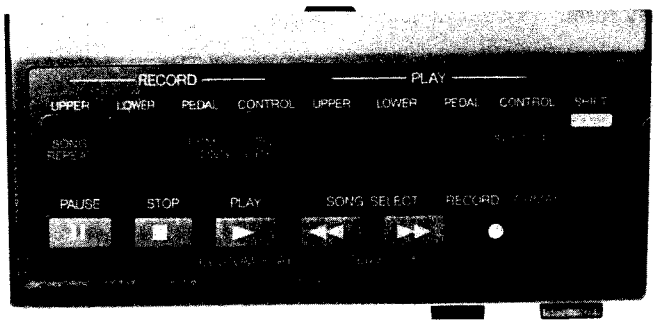
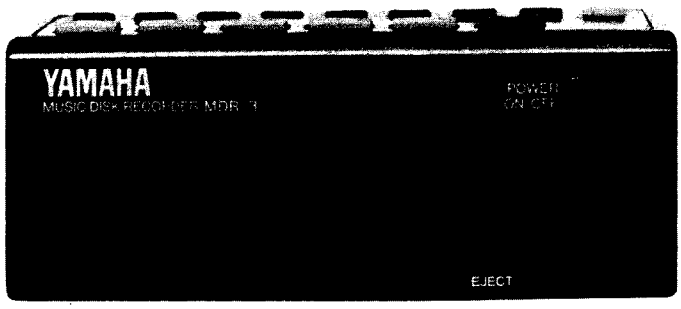
MUSIC DISK RECORDER

MDR-3/MDR-3P

SERVICE MANUAL

MDR3





[MDR-3 : U、C、H
MDR-3P : J]

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EL 001353 *Revised Edition*

YAMAHA CORP.

3.0K-86 Printed in Japan '88.11

IMPORTANT NOTICE

This manual has been provided for the use of authorized Yamaha Retailers and their service personnel. It has been assumed that basic service procedures inherent to the industry, and more specifically Yamaha Products, are already known and understood by the users, and have therefore not been restated.

WARNING: Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components and failure of the product to perform as specified. For these reasons, we advise all Yamaha product owners that all service required should be performed by an authorized Yamaha Retailer or the appointed service representative.

IMPORTANT: The presentation or sale of this manual to any individual or firm does not constitute authorization, certification, recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of Yamaha are continually striving to improve Yamaha products. Modifications are, therefore, inevitable and changes in specification are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING: Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

IMPORTANT: Turn the unit OFF during disassembly and parts replacement. Recheck all work before you apply power to the unit.

■SPECIFICATIONS（総合仕様）

Model:	Music Disk Recorder
Recording media:	3.5-inch microfloppy disks (2DD)
Disk format:	MSX-DOS (MS-DOS Ver. 1.25)
Memory capacity:	634k bytes / 16 songs maximum
Control:	RECORD/FORMAT, SONG SELECT/TEMPO +/▷▷,SONG SELECT / TEMPO –/◁◁, PLAY / CUSTOM PLAY, STOP, PAUSE. RECORD Section: UPPER / SONG REPEAT, LOWER, PEDAL / SONG COPY FROM, CONTROL / SONG COPY TO. PLAY Section: UPPER, LOWER, PEDAL, CONTROL / SONG DEL., SHIFT.
Display:	Four-digit seven-segment LED
Other coponents:	POWER switch, disk drive, EJECT button
Input/Output jacks:	MIDI IN, MIDI OUT, MIDI THRU, DC IN.
Rated input voltage:	10 V DC
rated input current:	Minimum 700 mA up to 1A
Rated power consumption:	7.5 W
External dimensions:	135 (W) x 200 (D) x 63.5 (H) mm
Weight:	1.3 kg
Accessories:	3.5-inch 2DD microfloppy disk x 1 MIDI cable (1.5m length) x 2 Auxiliary operation sheet
Options:	Mounting bracket BRT-3 (for use with the HS Series Electone) Power adaptor PA-3L or PA-4 (PA-40 for the USA)

[Reference: Names of the Created Files]

Registration files	MDR_nn.ROO
Event files	MDR_nn.EVT

*nn=00 to 15 (Song Nos. 01 to 16)

記憶装置	3.5インチ フロッピーディスクドライブ(2DD)
ディスクフォーマット	MSX-DOS(MS-DOS Ver.1.25)
メモリー容量	634Kバイト
最大録音曲数	16曲
パネルスイッチ	RECORD/FORMAT、SONG SELECT/TEMPO＋/▷▷、SONG SELECT/TEMPO－/◁◁、PLAY/CUSTOM PLAY、STOP、PAUSE レコードセクション：UPPER/SONG REPEAT、LOWER、PEDAL/SONG COPY FROM、CONTROL/SONG COPY TO プレイセクション：UPPER、LOWER、PEDAL、CONTROL/ SONG DEL.、SHIFT
表示器	4桁 7セグメントLED
その他のコントロール	パワースイッチ、ディスクドライブ、イジェクトボタン
入出力端子	MIDI IN、MIDI OUT、MIDI THRU、DC IN
定格入力電圧	DC 10V
定格電流	700mA
消費電力	7.5W
寸法(W×D×H)	135×200×63.5mm
重　量	1.3kg
付属品	3.5インチ 2DD マイクロフロッピーディスク×1 MIDI ケーブル(1.5m)×2 ACアダプター PA-3L ×1

● Hardware Specifications

CPU

HD63C03Y 12-MHz clock

ROM

μPD27C256AD-12 32K bytes (24K bytes used)

RAM

TC55257PL-12 32K bytes

Counter/Timer

μPD71054C

Counter #0: Used in MODE 3 for producing the MIDI baud rate

Counter #1: Used in MODE 2 for measuring the $F8 (MIDI) Clock intervals

Counter #2: Used in MODE 2 for hexadecimal incrementation

DMAC

M82C37A-5

4-MHz clock: 1-clock WAIT is provided when accessed as the slave device

Channel #0 : Not used

Channel #1 : Not used

Channel #2 : Not used

Channel #3 : Used between FDC ↔ MEMORY

FDC

WD 37C65

16-MHz clock : Software - compatible with NEC μPD765

FDD

ND352S-A

3-1/2" 2DD drive 1M byte capacity with an unformatted disk step rate: 6 ms

Display

GL3P412

Four digits Dynamic illumination controlled by the software

● ハード仕様

CPU

HD63C03Y クロック12MHz

ROM

μPD27C256AD-12 32KB(24KB使用)

RAM

TC55257PL-12 32KB

カウンタ・タイマ

μPD71054C

カウンタ#0 モード3で使用 MIDIボーレート作成用

カウンタ#1 モード2で使用 $F8(MIDI)クロック間隔測定用

カウンタ#2 モード2で使用 16逓倍用

DMAC

M82C37A-5

クロック4MHz スレーブとしてアクセスする時は、1 クロック WAITがはいる

チャンネル#0 未使用

チャンネル#1 未使用

チャンネル#2 未使用

チャンネル#3 FDC ⟷ MEMORYで使用

FDC

WD37C65 クロック16MHz NEC μPD765とソフトコンパチ

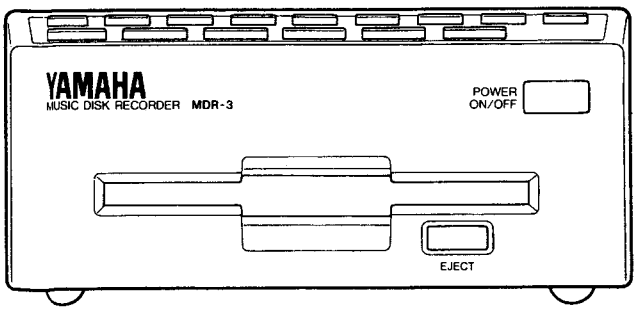
FDD

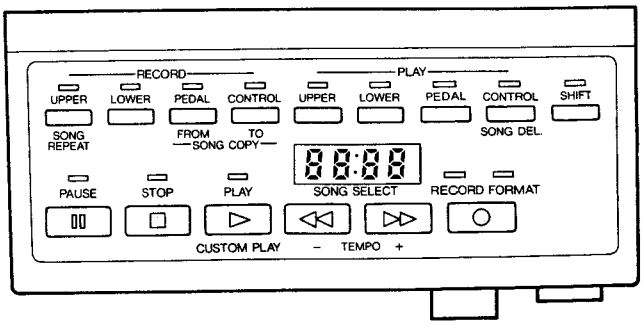
ND352S-A 3.5インチ2DD アンフォーマット時 1MB ステップレート 6mS

表示器

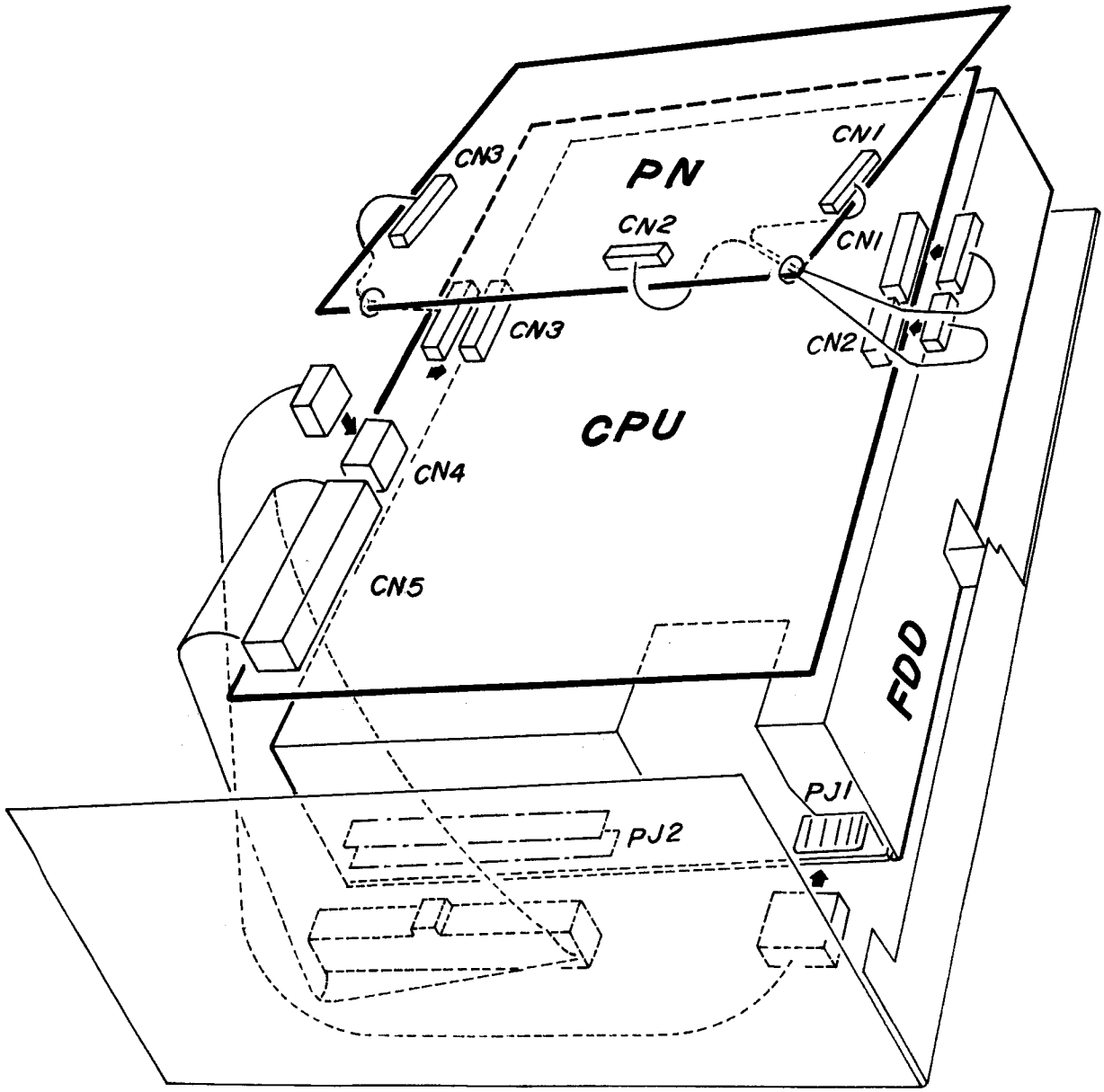
GL3P412 4桁 ソフトによるダイナミック点灯

■PANEL LAYOUT (パネルレイアウト)

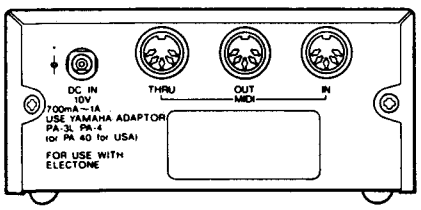




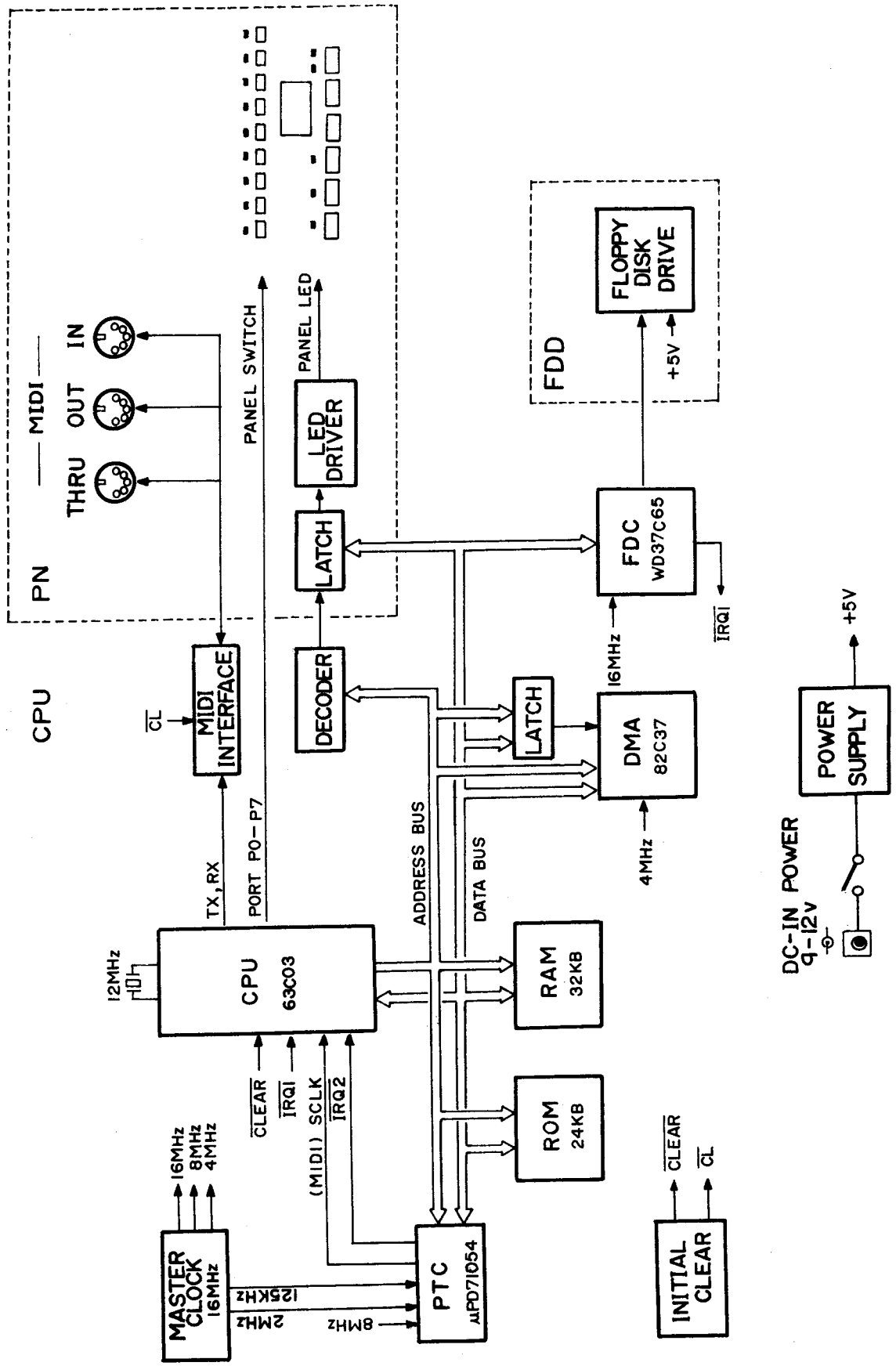
■CIRCUIT BOARD LAYOUT（ユニットレイアウト）



● Input/Output Jacks on the Rear Panel



■BLOCK DIAGRAM（ブロックダイアグラム）



■LSI DATA TABLE (LSI端子機能表)

● HD63C03YP (XB529001) MPU

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss	I	Ground	33	Vcc		DC Supply
2	XTAL	I	Clock	34	V 15	O	Address bus
3	EXTAL	I		35	A 14	O	
4	MP0	I	Mode program	36	A 13	O	
5	MP1	I		37	A 12	O	
6	$\overline{RES}$	I	Reset	38	A 11	O	
7	$\overline{STBY}$	I	Stand-by mode signal	39	A 10	O	
8	$\overline{NMI}$	I	Non-maskable interrupt	40	A 9	O	
9	P 20	I/O	Port 2	41	A 8	O	
10	P 21	I/O		42	Vss		Ground
11	P 22	I/O		43	A 7	O	Address bus
12	RX	I/O		44	A 6	O	
13	TX	I/O		45	A 5	O	
14	P 25	I/O		46	A 4	O	
15	P 26	I/O		47	A 3	O	
16	P 27	I/O		48	A 2	O	
17	$\overline{IRQ\ 1}$	I/O	Port 5	49	A 1	O	
18	$\overline{IRQ\ 2}$	I/O		50	A 0	O	
19	$\overline{MR}$	I/O		51	D 7	I/O	Data bus
20	$\overline{HALT}$	I/O		52	D 6	I/O	
21	P 54	I/O		53	D 5	I/O	
22	P 55	I/O		54	D 4	I/O	
23	P 56	I/O		55	D 3	I/O	
24	P 57	I/O		56	D 2	I/O	
25	P 60	I/O	Port 6	57	D 1	I/O	
26	P 61	I/O		58	D 0	I/O	
27	P 62	I/O		59	$\overline{BA}$	O	Bus available
28	P 63	I/O		60	$\overline{LIR}$	O	Load instruction resistor
29	P 64	I/O		61	$\overline{R/W}$	O	Read/Write control
30	P 65	I/O		62	$\overline{WR}$	O	Write
31	P 66	I/O		63	$\overline{RD}$	O	Read
32	P 67	I/O		64	E	O	Enable

● MSM82C37A-5RS (XE908A00) DMA (Programmable DMA Controller)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	$\overline{IOR}$	I/O	I/O read	21	DB 7	I/O	Data bus
2	$\overline{IOW}$	I/O	I/O write	22	DB 6	I/O	
3	$\overline{MEMR}$	O	Memory read	23	DB 5	I/O	
4	$\overline{MEMW}$	O	Memory write	24	DACK 1	O	DMA accept
5	NC			25	DACK 0	O	
6	READY	I	Ready	26	DB 4	I/O	Data bus
7	HLDA	I	Hold acknowledge	27	DB 3	I/O	
8	ADSTB	O	Address strobe	28	DB 2	I/O	
9	AEN	O	Address enable	29	DB 1	I/O	
10	HRQ	O	Hold request	30	DB 0	I/O	
11	$\overline{CS}$	I	Chip select	31	VCC		Power supply
12	CLK	I	Clock	32	A 0	I/O	Address bus
13	RESET	I	Reset	33	A 1	I/O	
14	DACK 2	O	DMA acknowledge	34	A 2	I/O	
15	DACK 3	O		35	A 3	I/O	
16	DREQ 3	I	DMA request	36	$\overline{EOP}$	I/O	End of process
17	DREQ 2	I		37	A 4	O	Address bus
18	DREQ 1	I		38	A 5	O	
19	DREQ 0	I		39	A 6	O	
20	VSS		Ground	40	A 7	O	

● μPD71054C (XC310A00) P.T.C (Programmable Timer Counter)

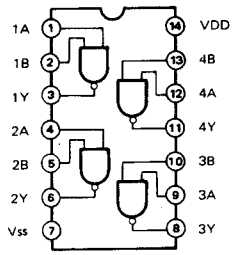
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	D 7	I/O	Data bus	13	OUT 1	O	Counter output 1
2	D 6	I/O		14	GATE 1	I	Counter gate 1
3	D 5	I/O		15	CLK 1	I	Counter clock 1
4	D 4	I/O		16	GATE 2	I	Counter gate 2
5	D 3	I/O		17	OUT 2	O	Counter output 2
6	D 2	I/O		18	CLK 2	I	Counter clock 2
7	D 1	I/O		19	A 0	I	Address bus
8	D 0	I/O		20	A 1	I	
9	CLK 0	I	Counter clock 0	21	$\overline{CS}$	I	Chip select
10	OUT 0	O	Counter output 0	22	$\overline{RD}$	I	Read strobe
11	GATE 0	I	Counter gate 0	23	$\overline{WR}$	I	Write strobe
12	GND		GND	24	VDD		Power supply

● WD37C65A (XE909A00) FDC (Floppy Disk Subsystem Controller)

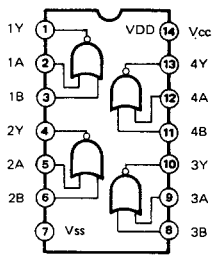
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	$\overline{RD}$	I	Read	21	CLK 2	I	Clock 2
2	$\overline{WR}$	I	Write	22	DRV	I	Drive type
3	$\overline{CS}$	I	Chip select	23	CLK 1	I	Clock 1
4	A 0	I	Address line	24	PCVAL	I	Precompensation value
5	$\overline{DACK}$	I	DMA acknowledge	25	$\overline{HS}$	O	Head select
6	TC	I	Terminal count	26	$\overline{WE}$	O	Write enable
7	DB 0	I/O	Data bus	27	$\overline{WD}$	O	Write data
8	DB 1	I/O		28	$\overline{DIRC}$	O	Direction
9	DB 2	I/O		29	$\overline{STEP}$	O	Step pulse
10	DB 3	I/O		30	$\overline{DS\ 1}$	O	Drive select 1
11	DB 4	I/O		31	$\overline{VSS}$		Ground
12	DB 5	I/O		32	$\overline{DS\ 2}$	O	Drive select 2
13	DB 6	I/O		33	$\overline{MO\ 1}$	O	Motor on 1
14	DB 7	I/O		34	$\overline{MO\ 2}$	O	Motor on 2
15	DMA	O	Direct memory access	35	$\overline{HDL}$	O	Head Loaded
16	$\overline{IRQ}$	O	Interrupt request	36	$\overline{RPM}$	O	Reduce write current, revolutions per minute
17	$\overline{LDOR}$	I	Load operations register	37	$\overline{WP}$	I	Write protected
18	LDCR	I	Load control register	38	$\overline{TR00}$	I	Track 00
19	$\overline{RST}$	I	Reset	39	$\overline{IDX}$	I	Index
20	$\overline{RDD}$	I	Read disk data	40	VCC		Power supply

■IC BLOCK DIAGRAM (ICブロック図)

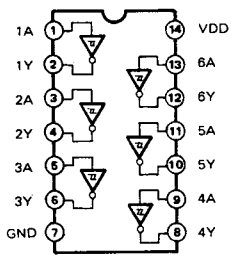
● TC74HC00P (IR000000)
Quad 2 Input NAND



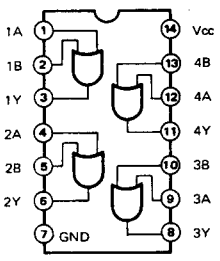
● TC74HC02P (IR000200)
Quad 2 Input NOR



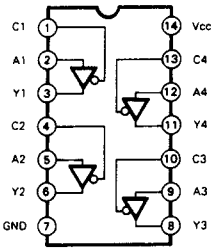
● TC74HC14P (IR001400)
Hex Inverter



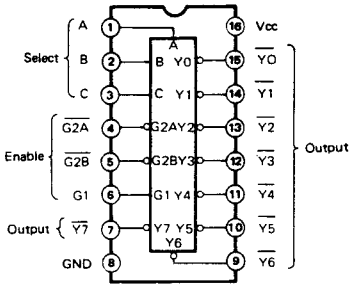
● TC74HC32P (IR003200)
Quad 2 Input OR



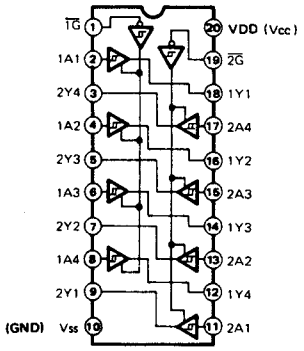
● TC74HC125P (IR012500)
Quad 3-State Bus Buffer



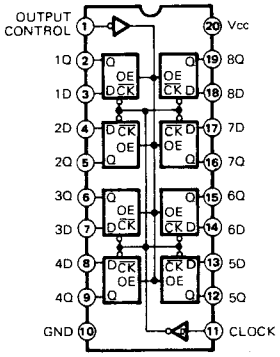
● TC74HCT138P (IR013800)
3 to 8 Demultiplexer



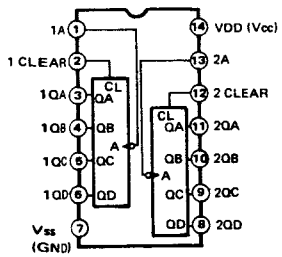
● TC74HC244P (IR024400)
Octal 3-State Bus Buffer



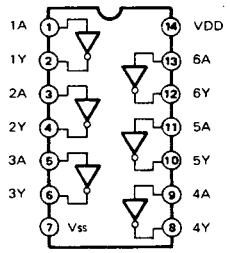
● TC74HC374P (IR037400)
Octal 3-State D-Type Flip-Flop



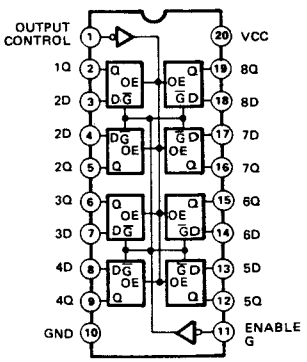
● TC74HC393P (IR039300)
Dual 4-Bit Binary Counter



● TC74HCT04P (XA830001)
Hex Inverter



● TC74HCT373 (XC750A00)
Octal 3-State D-Type Latch



■DISASSEMBLY PROCEDURE（分解手順）

1. Removal of Upper Case

- Remove the 2 screws Ⓐ (3x5 bind head screw). (Refer to Fig.1)
- Slide the upper case back, while pressing the front edge of the upper case down slightly. Then take it out of the unit.

1．アッパーケースの取外し方

●ネジⒶ2本(3×5バインド小ネジ)取り除きます。
(Fig.1参照)

●パネル上面を押さえながら、アッパーケースを後ろにスライドさせ取外します。

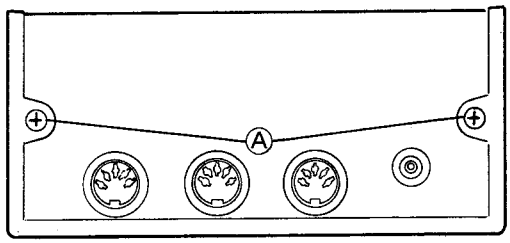


Fig. 1

Rear view of the unit　　(リアパネル側)

2. Removal of Panel

- Remove the upper case. (Refer to 1.)
- Remove the 2 screws Ⓑ (3x6 bind head screw). (Refer to Fig.2)
- Draw the panel ahead of the unit.
- After the connectors between the PN circuit board and CPU circuit board have been removed, the panel and PN circuit board can be taken out of the unit.

2．パネルの取外し方

●アッパーケースを取外します。(1項参照)

●ネジⒷ2本(3×6バインド小ネジ)を取除きます。
(Fig.2参照)

●パネルを前方に引き出します。

●PNシートとCPUシート間のコネクターを外すことによって、パネルはPNシートと一緒に外れます。

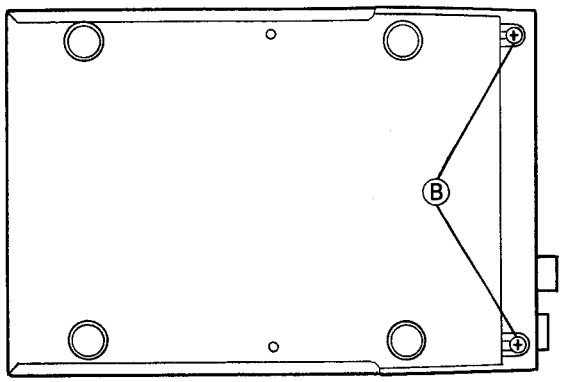


Fig. 2

Bottom view of the unit　　(底側より)

3. Removal of CPU Circuit Board.

- Remove the upper case. (Refer to 1.)
- Remove the panel. (Refer to 2.)
- Remove the 6 screws Ⓒ (3x5 bind head screw). (Refer to Fig. 3)
- Disconnect 2 connectors Ⓓ for the FDD unit, then remove the CPU circuit board from the unit. (Refer to Fig 3.)

3．CPUシートの取外し方

- アッパー・ケースを取外します。(1項参照)
- パネルを取外します。(2項参照)
- ネジⒸ6本3×5(バインド小ネジ)を取除きます。(Fig. 3参照)
- FDDへのコネクターⒹ2ヶを外し、CPUシートを取外します。(Fig. 3参照)

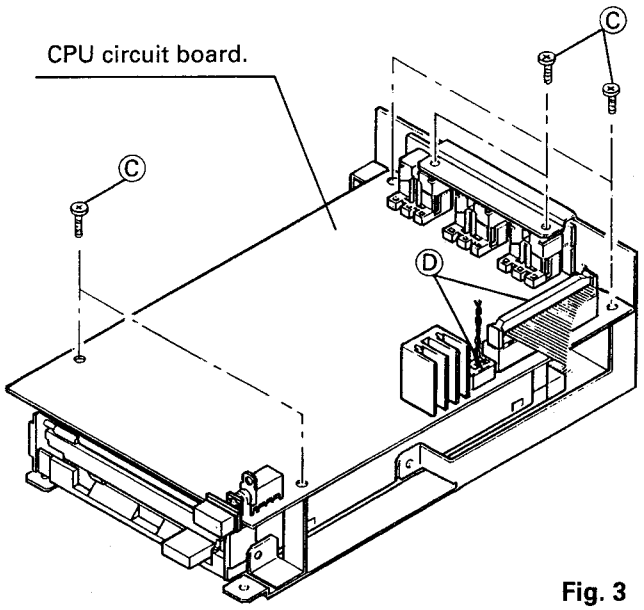


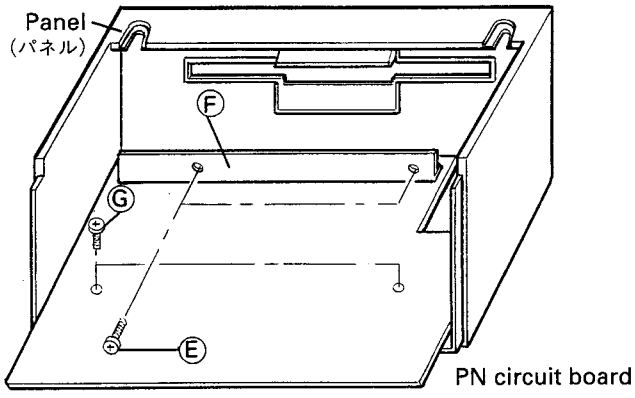
Fig. 3

4. Removal of PN Circuit Board

- Remove the upper case. (Refer to 1.)
- Remove the panel. (Refer to 2.)
- Remove the 2 screws Ⓔ (3x6 bind head tapping screw) and angle bracket Ⓕ.
- Remove the 2 screws Ⓖ (3x6 bind head tapping screw), then take the PN circuit board out of the panel with the rubber contact.

4．PNシートの取外し方

- アッパー・ケースを取外します。(1項参照)
- パネルを取外します。(2項参照)
- ネジⒺ2本(3×6バインドタッピングネジ)を取除き、基板受け金具Ⓕを取外します。
- ネジⒼ2本(3×6バインドタッピングネジ)を取除きPNシートを接点ゴムと一緒に取外します。(Fig. 4参照)

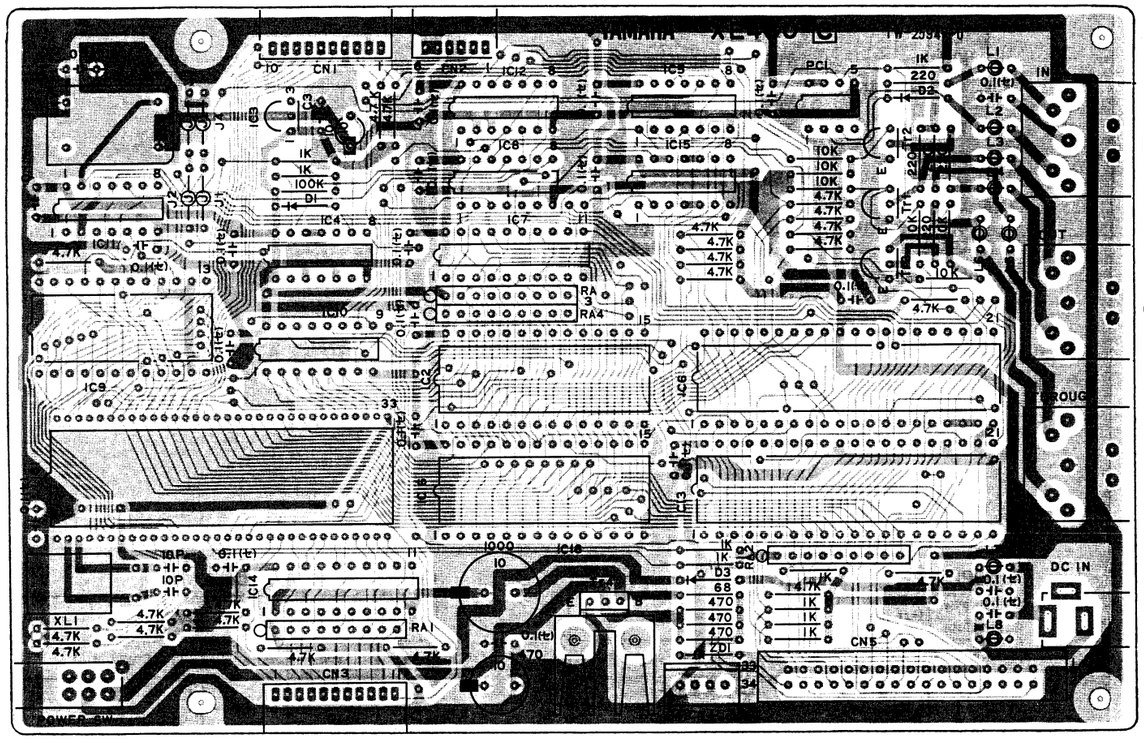


Inside view of the panel which up side down.

Fig. 4

■CIRCUIT BOARDS（シート基板図）

● CPU Curcuit Board



Components Side（部品側）

Notes)

* Circuit Board
CPU (VF307100) XE480D0

1. IC
IC 1: HD63C03YP (XB529001) MPU
IC 2: TC55257PL-12 (XD314A00) SRAM
IC 3: PST518B-2 (IG116200) SYSTEM RESET
IC 4: TC74HC14P (IR001400) INV
IC 5: TC74HC125P (IR012500) 3-BUFF
IC 6: MSM82C37A-5RS (XE908A00) DMA
IC 7: TC74HCT373 (XC750A00) D-LATCH
IC 8: TC74HCT04P (XA830001) INV
IC 9: μPD71054C (XC310A00) PTC
IC10: TC74HC138P (IR013800) DEC0-8
IC11: TC74HC393P (IR039300) CNT
IC12: TC74HC02P (IR000200) NOR
IC13: WD37C65A (XE909A00) FDC
IC14: TC74HC244P (IR024400) BUS. BUF
IC15: TC74HC00P (IR000000) NAND
IC16: μPC27C256AD-12 (XE941G00) EPROM 120n sec.
IC17, 18: TC74HC32P (IR003200) OR

2. Photo Coupler
PC 1: P2822 (VF099600)

3. Transistor
Tr 1 ~ 3: 2SC1815 Y (IC181520)
Tr 4: 2SD880 O, Y (ID088020)

4. Diode
D 1, 2: 1SS176 (IX000760)
D 3: 11ES4 (VB481900)

5. Zener Diode
ZD 1: MTZ5.6B 5.6V (VA007600)

6. Resistor Array
RA 1: EXB-F9E103J5 (VB187500)
RA 2 ~ 4: EXB-F9E472J5 (VB187300)

7. Semiconductive Cera. Cap.
Marked (ヒ): 0.1μF 16V (FZ004170)

8. Monolithic Cera. Cap.
Marked (ヒ): 0.1μF 50V Z (VB971200)

9. Quartz Crystal Unit
XL 1: 12.0M HC-18/U (VE463500)
XL 2: 16M TD308A (QU008200)

10. Coil
L 1 ~ 6, 9, 10: FL5R200QN 20μH (VB971100)
L 7, 8: SN3-205 10μH (GE901870)

11. Push Switch
SPPJ22941A U (VF678900) POWER

2NA-VF30720 ⚠

CPU **CN1**

Pin No.	Pin Name	Destination
1	$\overline{\text{LEDR}}$	PN – CN1 – 1
2	E	PN – CN1 – 2
3	$\overline{\text{LEDC}}$	PN – CN1 – 3
4	E	PN – CN1 – 4
5	D0	PN – CN1 – 5
6	D1	PN – CN1 – 6
7	D2	PN – CN1 – 7
8	D3	PN – CN1 – 8
9	D4	PN – CN1 – 9
10	D5	PN – CN1 – 10

CPU **CN2**

Pin No.	Pin Name	Destination
1	D6	PN – CN2 – 1
2	D7	PN – CN2 – 2
3	E	PN – CN2 – 3
4	E	PN – CN2 – 4
5	+5	PN – CN2 – 5
6	+5	PN – CN2 – 6

CPU **CN3**

Pin No.	Pin Name	Destination
1	C1	PN – CN3 – 1
2	C2	PN – CN3 – 2
3	P0	PN – CN3 – 3
4	P1	PN – CN3 – 4
5	P2	PN – CN3 – 5
6	P3	PN – CN3 – 6
7	P4	PN – CN3 – 7
8	P5	PN – CN3 – 8
9	P6	PN – CN3 – 9
10	P7	PN – CN3 – 10
11	$\overline{\text{CLEAR}}$	PN – CN3 – 11

CPU **CN4**

Pin No.	Pin Name	Destination
1	+5	FDD – PJ1 – 1
2	GND	FDD – PJ1 – 2
3	FG	FDD – PJ1 – 3
4	NC	

CPU **CN5**

Pin No.	Pin Name	Destination
1	GND	FDD – PJ2 – 1
2	$\overline{\text{DISK}}$	FDD – PJ2 – 2
3	GND	FDD – PJ2 – 3
4	NC	FDD – PJ2 – 4
5	GND	FDD – PJ2 – 5
6	NC	FDD – PJ2 – 6
7	GND	FDD – PJ2 – 7
8	$\overline{\text{IDX}}$	FDD – PJ2 – 8
9	GND	FDD – PJ2 – 9
10	$\overline{\text{SEL1}}$	FDD – PJ2 – 10
11	GND	FDD – PJ2 – 11
12	$\overline{\text{SEL2}}$	FDD – PJ2 – 12
13	GND	FDD – PJ2 – 13
14	NC	FDD – PJ2 – 14
15	GND	FDD – PJ2 – 15
16	$\overline{\text{MON}}$	FDD – PJ2 – 16
17	GND	FDD – PJ2 – 17
18	$\overline{\text{DIR}}$	FDD – PJ2 – 18
19	GND	FDD – PJ2 – 19
20	$\overline{\text{STEP}}$	FDD – PJ2 – 20
21	GND	FDD – PJ2 – 21
22	$\overline{\text{WD}}$	FDD – PJ2 – 22
23	GND	FDD – PJ2 – 23
24	$\overline{\text{WG}}$	FDD – PJ2 – 24
25	GND	FDD – PJ2 – 25
26	$\overline{\text{TR00}}$	FDD – PJ2 – 26
27	GND	FDD – PJ2 – 27
28	$\overline{\text{WPRT}}$	FDD – PJ2 – 28
29	GND	FDD – PJ2 – 29
30	$\overline{\text{RDD}}$	FDD – PJ2 – 30
31	GND	FDD – PJ2 – 31
32	$\overline{\text{SIDE}}$	FDD – PJ2 – 32
33	GND	FDD – PJ2 – 33
34	$\overline{\text{RDY}}$	FDD – PJ2 – 34

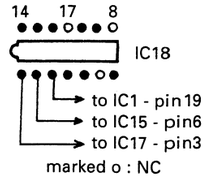
FDD **PJ1**

Pin No.	Pin Name	Destination
1	+5	CPU – CN4 – 1
2	GND	CPU – CN4 – 2
3	FG	CPU – CN4 – 3
4	NC	

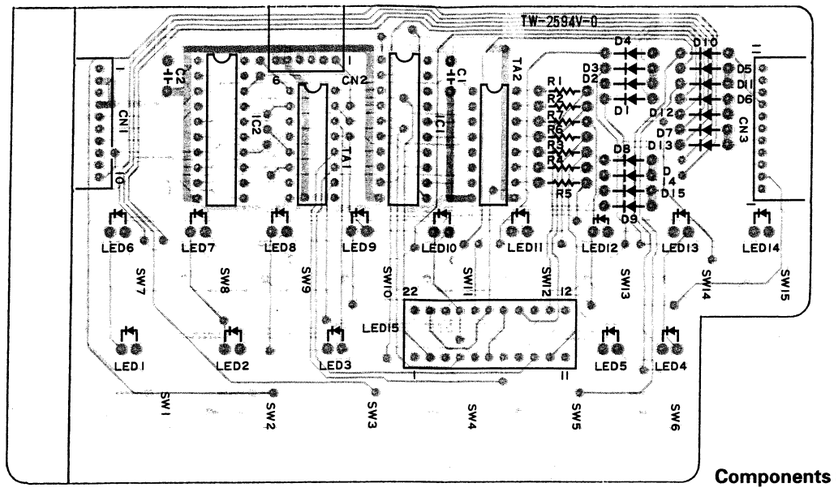
FDD **PJ2**

Pin No.	Pin Name	Destination
1	GND	CPU – CN5 – 1
2	$\overline{\text{DISK}}$	CPU – CN5 – 2
3	GND	CPU – CN5 – 3
4	NC	CPU – CN5 – 4
5	GND	CPU – CN5 – 5
6	NC	CPU – CN5 – 6
7	GND	CPU – CN5 – 7
8	$\overline{\text{IDX}}$	CPU – CN5 – 8
9	GND	CPU – CN5 – 9
10	$\overline{\text{SEL1}}$	CPU – CN5 – 10
11	GND	CPU – CN5 – 11
12	$\overline{\text{SEL2}}$	CPU – CN5 – 12
13	GND	CPU – CN5 – 13
14	NC	CPU – CN5 – 14
15	GND	CPU – CN5 – 15
16	$\overline{\text{MON}}$	CPU – CN5 – 16
17	GND	CPU – CN5 – 17
18	$\overline{\text{DIR}}$	CPU – CN5 – 18
19	GND	CPU – CN5 – 19
20	$\overline{\text{STEP}}$	CPU – CN5 – 20
21	GND	CPU – CN5 – 21
22	$\overline{\text{WD}}$	CPU – CN5 – 22
23	GND	CPU – CN5 – 23
24	$\overline{\text{WG}}$	CPU – CN5 – 24
25	GND	CPU – CN5 – 25
26	$\overline{\text{TR00}}$	CPU – CN5 – 26
27	GND	CPU – CN5 – 27
28	$\overline{\text{WPRT}}$	CPU – CN5 – 28
29	GND	CPU – CN5 – 29
30	$\overline{\text{RDD}}$	CPU – CN5 – 30
31	GND	CPU – CN5 – 31
32	$\overline{\text{SIDE}}$	CPU – CN5 – 32
33	GND	CPU – CN5 – 33
34	$\overline{\text{RDY}}$	CPU – CN5 – 34

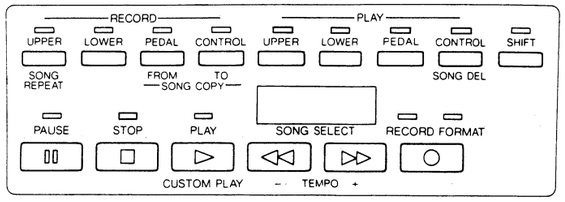
* IC18 is located on IC17.
（IC18はIC17の上に重ねて取付ける）



● PN Circuit Board



Components Side（部品側）



Notes)

* Circuit Board
PN (VF307200) XE479D0

1. IC
   IC 1, 2: TC74HC374P (IR037400) D.FF
2. Transistor Array
   TA 1: TD62505P (VF343800)
   TA 2: TD62503P (IG111000)
3. Diode
   D 1 ~ 15: 1SS176 (IX000760)
4. LED
   LED 1, 2, 4~14: TLS211 RE (VB167000)
   LED 3: TLG211 GR (VB167100) PLAY
5. LED Display
   LED 15: GL3P412 (VF343900)
6. Monolithic Cera. Cap.
   Marked ( ): 0.1µF 50V Z (VB971200)

CPU **CN1**

Pin No.	Pin Name	Destination
1	$\overline{\text{LEDR}}$	CPU – CN1 – 1
2	E	CPU – CN1 – 2
3	$\overline{\text{LEDC}}$	CPU – CN1 – 3
4	E	CPU – CN1 – 4
5	D0	CPU – CN1 – 5
6	D1	CPU – CN1 – 6
7	D2	CPU – CN1 – 7
8	D3	CPU – CN1 – 8
9	D4	CPU – CN1 – 9
10	D5	CPU – CN1 – 10

CPU **CN2**

Pin No.	Pin Name	Destination
1	D6	CPU – CN2 – 1
2	D7	CPU – CN2 – 2
3	E	CPU – CN2 – 3
4	E	CPU – CN2 – 4
5	+5	CPU – CN2 – 5
6	+5	CPU – CN2 – 6

CPU **CN3**

Pin No.	Pin Name	Destination
1	C1	CPU – CN3 – 1
2	C2	CPU – CN3 – 2
3	P0	CPU – CN3 – 3
4	P1	CPU – CN3 – 4
5	P2	CPU – CN3 – 5
6	P3	CPU – CN3 – 6
7	P4	CPU – CN3 – 7
8	P5	CPU – CN3 – 8
9	P6	CPU – CN3 – 9
10	P7	CPU – CN3 – 10
11	$\overline{\text{CLEAR}}$	CPU – CN3 – 11

2NA-VF30720 ⚠

■DISK FORMAT

1. The disk format conforms to MSX-DOS (MS-DOS, Version 1.25).
2. The four formats listed below are supported:

	Single-sided 80 TPI 9 sectors/ track	Double-sided 80 TPI 9 sectors/ track	Single-sided 80 TPI 8 sectors/ track	Double-sided 80 TPI 8 sectors/ track
FAT ID	$F8	$F9	$FA	$FB
Bytes/ sector	512	512	512	512
Bytes/ disk	360 K	720 K	320 K	640 K
Sectors/ cluster	2	2	2	2
Sector/ FAT	2	3	1	2
Total sectors	720	1440	640	1280

3. The default disk format of MDR-3 (P) is the double-sided, 80 TPI (tracks per inch), 9 sectors/track format.
4. When a disk is formatted by MDR-3 (P) , $00 is written to all sectors of the disk, then:

① The following data (IPL) is written to Sector 1 of Track 0:

■ディスクフォーマット

1．ディスクフォーマットは、MSX-DOS(MS-DOS Ver. 1.25)に準拠。

2．次の4種類のフォーマットをサポートする。

	80トラック片面 9セクター/トラック	80トラック片面 9セクター/トラック	80トラック片面 8セクター/トラック	80トラック片面 8セクター/トラック
FAT ID	$F8	$F9	$FA	$FB
バイト/セクター	512	512	512	512
バイト/ディスク	360K	720K	320K	640K
セクター/クラスタ	2	2	2	2
セクター/FAT	2	3	1	2
全セクター数	720	1440	640	1280

3．MDR3 (P)で初期化を行うと、80トラック両面9セクター／トラックのフォーマットになる。

4．MDR3 (P)で初期化を行った時、全セクターに$00を書き込んだ後、

①トラック0、セクタ1には、次のデータ(1PL) が書き込まれる。

```
ADR.    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
--------+-----------------------------------------------
00000000 00 00 00 4D 44 52 2D 33 20 20 20 00 02 02 01 00  ...MDR-3   .....
00000010 02 70 00 A0 05 F9 D3 00 09 00 02 00 00 00 00 00  .p..............
00000020 39 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000050 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000080 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000090 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000000A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000000B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000000C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000000D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000000E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000000F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000100 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000110 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000120 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000130 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000140 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000150 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000160 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000170 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000180 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
00000190 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000001A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000001B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000001C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000001D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000001E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
000001F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 55 AA  ..............U.
```

② The following data (FAT) is written to Sectors 2 and 5 of Track 0:

②トラック０、セクタ２とセクタ５には次のデータ(FAT)が書き込まれる。

ADR.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
00000000	F9	FF	FF	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000010	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000020	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000030	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000070	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000080	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000090	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000000A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000000B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000000C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000000D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000000E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000000F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000100	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000110	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000120	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000130	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000140	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000150	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000160	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000170	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000180	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
00000190	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000001A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000001B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000001C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000001D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000001E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....
000001F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.....

■LOADING AND EXECUTION OF IPL

1. The IPL (Initial Program Loader) should only be loaded and executed while the MDR-3 (P) is in STOP status with a disk installed.
2. The procedure for returning control to the MDR-3 (P) functions is performed using the currently loaded program. For example, hold down [SHIFT] while you press [CONTROL] in the PLAY section.
3. First, the data stored in Sector 1 of Track 0 is read then written to Address $7E00. Next, Address $0200. Next, Address $7E03 is checked; if it has been written with the eight characters "MDR-3", the data stored in Address $7E20 is called.

■IPLロードの方法と実行

1．STOP状態でディスクがはいった時に必ずロードし実行する。
2．MDR 3 (P)の機能に戻る時は、ロードされたプログラム側で行う。例えば〔SHIFT〕を押し －PLAY－の〔CONTROL〕を押す。
3．トラック０のセクター１を＄７Ｅ００番地へ読みだし、＄７Ｅ０３番地から"MDR-3" と８文字書かれていたら＄７Ｅ２０をコールする。

■FILE FORMAT

1. MDR-3 (P) disks are 100% compatible with the MDR-2P disks.
2. Operating system such as MS-DOS or MSX-DOS process data in cluster units which consist of two sectors per cluster. To enable high-speed reading and writing operations, however, the MDR-3 (P) processes data in block units which consist of four consecutive sectors per block.
   * Consequently, even if the total capacity of a disk is 720K bytes, the existence of unused sectors results in an actual storage capacity of 634K bytes.
3. The 112 files can be processed on one disk, and a maximum of 16 songs can be recorded per disk.
4. The filenames of the files created by MDR-3 (P) consist of the two types below:

① "MDR _ xx. ROO"
During normal recording, the Exclusive Messages which are contained in the Registration data received from the Electone are recorded in their original format.
During normal playback, the contents of this file are transmitted.

② "MDR _ xx. EVT"
The MIDI messages that were received during recording are recorded in ESEQ format.
* "xx" corresponds to a Song No. from "00" to "15" (Song No. 1=00).
* The ESEQ format is a format defined by Yamaha for use in recording Performance data.

■ファイルフォーマット

1．MDR 3 (P)のディスクは、MDR-2 Pのディスクと完全に互換性をもつ。
2．MS-DOSやMSX-DOSなどでは、2セクターをまとめて1クラスターとしてクラスター単位で扱っているが、MDR 3 (P)ではディスクを高速に読み書きするために、連続した4セクターをまとめて1ブロックとしブロック単位で扱う。
   ＊したがって、ディスクの全容量は720KBとなっていても、未使用セクターができ実際には634KBになる。
3．管理できるファイル数は112個。SONG数は16曲録音できます。
4．MDR 3 (P)で作られるファイル名は、次の2種類

①"MDR_xx. ROO"
ノーマル録音時にエレクトーンより受信したレジストレーションのエクスクルーシブメッセージが、そのまま録音されている。ノーマル再生時には、このファイルの内容が送信される。

②"MDR_xx. EVT"
録音時に受信したMIDIメッセージが、ESEQフォーマットで録音される。
＊xxは曲番に対応し"００－１５"（曲１が００）
＊ESEQフォーマットとは、ヤマハ社内で定められた演奏データの記録フォーマット。

■LED MATRIX　　■LEDマトリクス

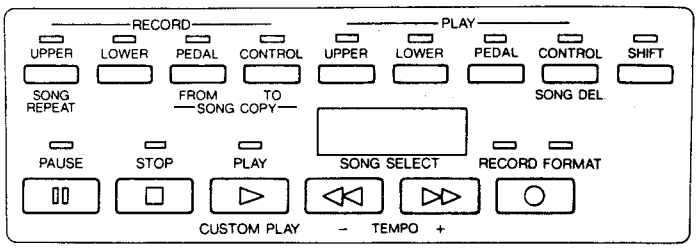
	C7	C6	C5	C4	C3	C2	C1	C0
R0	---	g0	f0	e0	d0	c0	b0	a0
R1	---	g1	f1	e1	d1	c1	b1	a1
R2	---	g2	f2	e2	d2	c2	b2	a2
R3	---	g3	f3	e3	d3	c3	b3	a3
R4	---	---	---	---	LC	UC	---	---
R5	---	PLAY PEDAL	PLAY LOWER	PLAY UPPER	REC. CONTROL	REC. PEDAL	REC. LOWER	REC. UPPER
R6	---	SHIFT	PLAY CONTROL	RECORD	FORMAT	PLAY	STOP	PAUSE

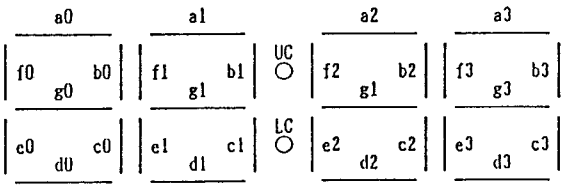
The digit is selected by R0 to R7, and the segment is selected at C0 to C7.

R0～S7で桁を選びC0～C7でセグメントを選ぶ

R0: Writes $01 to Address $9400.　　R0 ——> $9400に$01を書く
R1: Writes $02 to Address $9400.　　R1 ——> $9400に$02を書く
R2: Writes $04 to Address $9400.　　R2 ——> $9400に$04を書く
R3: Writes $08 to Address $9400.　　R3 ——> $9400に$08を書く
R4: Writes $10 to Address $9400.　　R4 ——> $9400に$10を書く
R5: Writes $20 to Address $9400.　　R5 ——> $9400に$20を書く
R6: Writes $42 to Address $9400.　　R6 ——> $9400に$40を書く

C0: Bit 0 of Address $9000, Lights up when "1".　　C0 ——> $9000のビット0　"1"で点灯
C0: Bit 1 of Address $9000, Lights up when "1".　　C1 ——> $9000のビット1　"1"で点灯
C0: Bit 2 of Address $9000, Lights up when "1".　　C2 ——> $9000のビット2　"1"で点灯
C0: Bit 3 of Address $9000, Lights up when "1".　　C3 ——> $9000のビット3　"1"で点灯
C0: Bit 4 of Address $9000, Lights up when "1".　　C4 ——> $9000のビット4　"1"で点灯
C0: Bit 5 of Address $9000, Lights up when "1".　　C5 ——> $9000のビット5　"1"で点灯
C0: Bit 6 of Address $9000, Lights up when "1".　　C6 ——> $9000のビット6　"1"で点灯
C0: Bit 7 of Address $9000, Lights up when "1".　　C7 ——> $9000のビット7　"1"で点灯





■SWITCH MATRIX

	Port 6								
Port 5		D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
	D 4	SHIFT	PLAY CONTROL	RECORD	<<	>>	PLAY	STOP	PAUSE
	D 5		REC. LOWER PLAY PEDAL	REC. PEDAL PLAY LOWER	PLAY UPPER	REC. CONTROL	REC. PEDAL	REC. LOWER	REC. UPPER

Port 5 ($15): Set to output
Port 6 ($17): Set to input

To check the status of the SHIFT switch, output "0" to Bit 4 of Port 5, then read Port 6 to check the contents of Bit 7. (If Bit 7 is 0, [SHIFT] has been pressed.)

■スイッチマトリクス

ポート5 ($15) 出力にセット
ポート6 ($17) 入力にセット

SHIFT SW を調べる時にはポート5のビット4に0を出力し、ポート6を読みビット7を調べる。(0の時SWが押されている) 同様にUPPER SWを調べる時には、ポート5のビット5に0を出力し、ポート6を読みビット1を調べる。

■DISK INPUT/OUTPUT

Port 2							
D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
READY	DISK	---	---	---	---	---	---

READY: The Ready signal of the FDD (floppy disk drive). The FDD is ready when READY is "0".

DISK: The Disk Change signal of the FDD.
* This signal becomes "1" when a disk is installed in the FDD and step pulses are being received.
* This signal becomes "0" as soon as the disk is removed.

■ディスク用I/O

READY…… FDDのレディ信号　0の時レディ
＊FDDはディスクが挿入されていて、モーターがオンされると0にする。

DISK ……FDDのディスクチェンジ信号　0の時チェンジ
＊FDDはディスクが挿入されていて、ステップパルスを受け取ると1にする。
＊ディスクが取り出されると、すぐに0になる。

■ERROR MESSAGES

Message	Meaning
"CF 01"	The floppy disk was ejected during play.
"CF 02"	The directory on the disk is full.
"CF 06"	The data that have been played is too much for recording.
"CF 07"	The floppy disk is defected.
"CF 08"	An error occured during MIDI data input/output.
"CF 09"	Memory error (RAM)
"InSt"	There is no disk in the drive.
"Fort"	The disk format is compatible with the MDR 3.
"Prot"	The disk's write protect slider is set to protect. You have tried to copy the copy protected disk.
"FULL"	There is no more space on the disk.
"EPty"	There is no song on the disk.

■エラーメッセージ

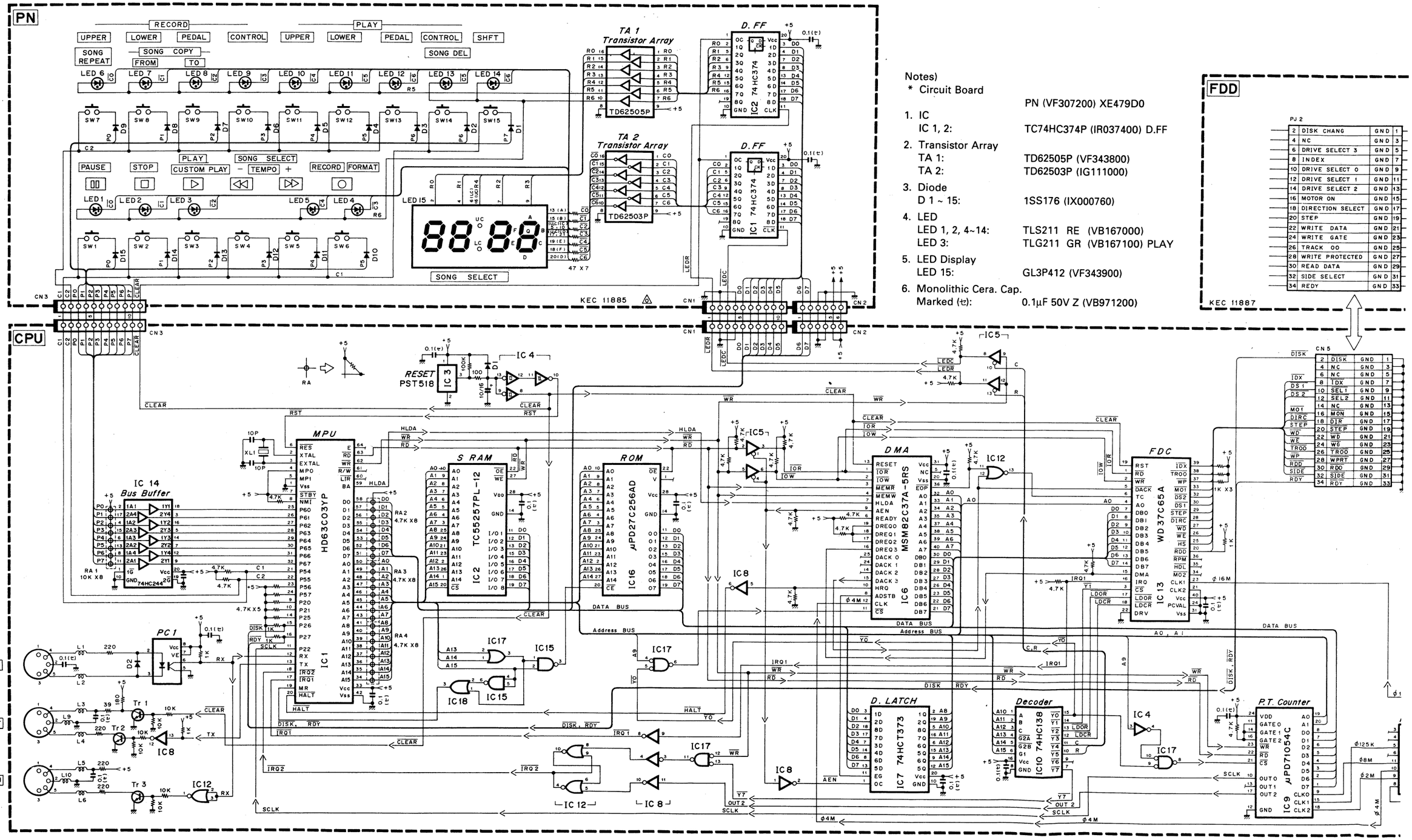
表　示	メッセージの意味
"cF01"	フロッピーディスクを演奏中にフロッピーディスクを取りだした場合
"cF02"	ディレクトリーが一杯 ファイルの属性が違う
"cF06"	演奏中の曲のデータが多すぎて録音できない
"cF07"	フロッピーディスクの不良 フォーマットできない
"cF08"	MIDIの送受信エラー ＊ハード的なエラー
"cF09"	メモリーエラー(RAM)
"InSt"	フロッピーディスクの未挿入
"Fort"	MDR－3用として初期化されない
"Prot"	ライトプロテクト状態になっている。 コピープロテクトの掛かったディスクをコピーしようとした。
"FULL"	ディスクが一杯 16曲共すでにディスクに録音されている。(SONG COPY)
"EPtY"	1曲もディスクに録音されていない。 (SONG COPY)

MUSIC DISK RECORDER MDR-3/MDR-3P
MIDI Implementation Chart/MIDI Implemantation Chart

Function		Transmitted	Recognized	Remarks
Basic Channel	Default Changes	all channels ×	all channels ×	not Basic ch.
Mode	Default Messages Altered	Mode 1 **********	Mode 1 **********	
Note Number	 True Voice	0-127 **********	0-127	
Velocity	Note ON Note OFF	○ 9nH, v=0-127 ○ 8nH, v=0-127	○ 9nH, v=0-127 ○ 8nH, v=0-127	
After Touch	Key's CH's	○ ○	○ ○	
Pitch Bender		○	○	
Control Change	0-63 64-121	○ ○	○ ○	
Program Change	 True #	○ **********	○	
System Exclusive		○	○	
System Common	Song Pos Song Sel Tune	○ ○ ○	○ ○ ○	
System Real Time	Clock Commands	○ ○	○ ○	
Aux Messages	Local ON/OFF All Notes OFF Active Sense Reset	○ ○ ○ ○	○ ○ × ○	
Notes				

Mode 1: OMNI ON, POLY Mode 2: OMNI ON, MONO ○: Yes
Mode 3: OMNI OFF, POLY Mode 4: OMNI OFF, MONO ×: No

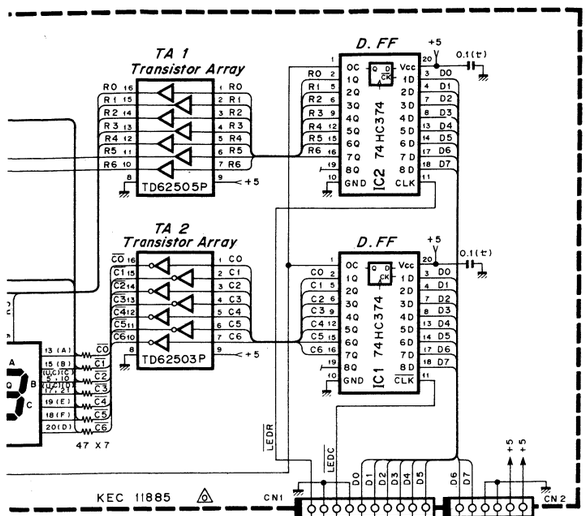
■MDR3 OVERALL CIRCUIT DIAGRAM（総回路図）



Notes)

* Circuit Board — PN (VF307200) XE479D0

1. IC
   IC 1, 2: TC74HC374P (IR037400) D.FF
2. Transistor Array
   TA 1: TD62505P (VF343800)
   TA 2: TD62503P (IG111000)
3. Diode
   D 1 ~ 15: 1SS176 (IX000760)
4. LED
   LED 1, 2, 4~14: TLS211 RE (VB167000)
   LED 3: TLG211 GR (VB167100) PLAY
5. LED Display
   LED 15: GL3P412 (VF343900)
6. Monolithic Cera. Cap.
   Marked (ㅌ): 0.1μF 50V Z (VB971200)



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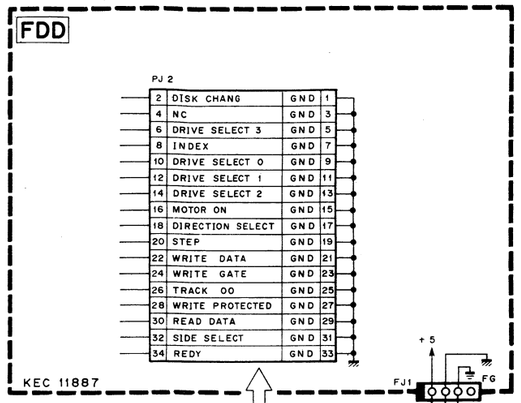
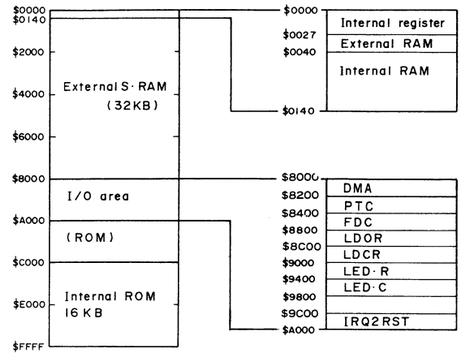
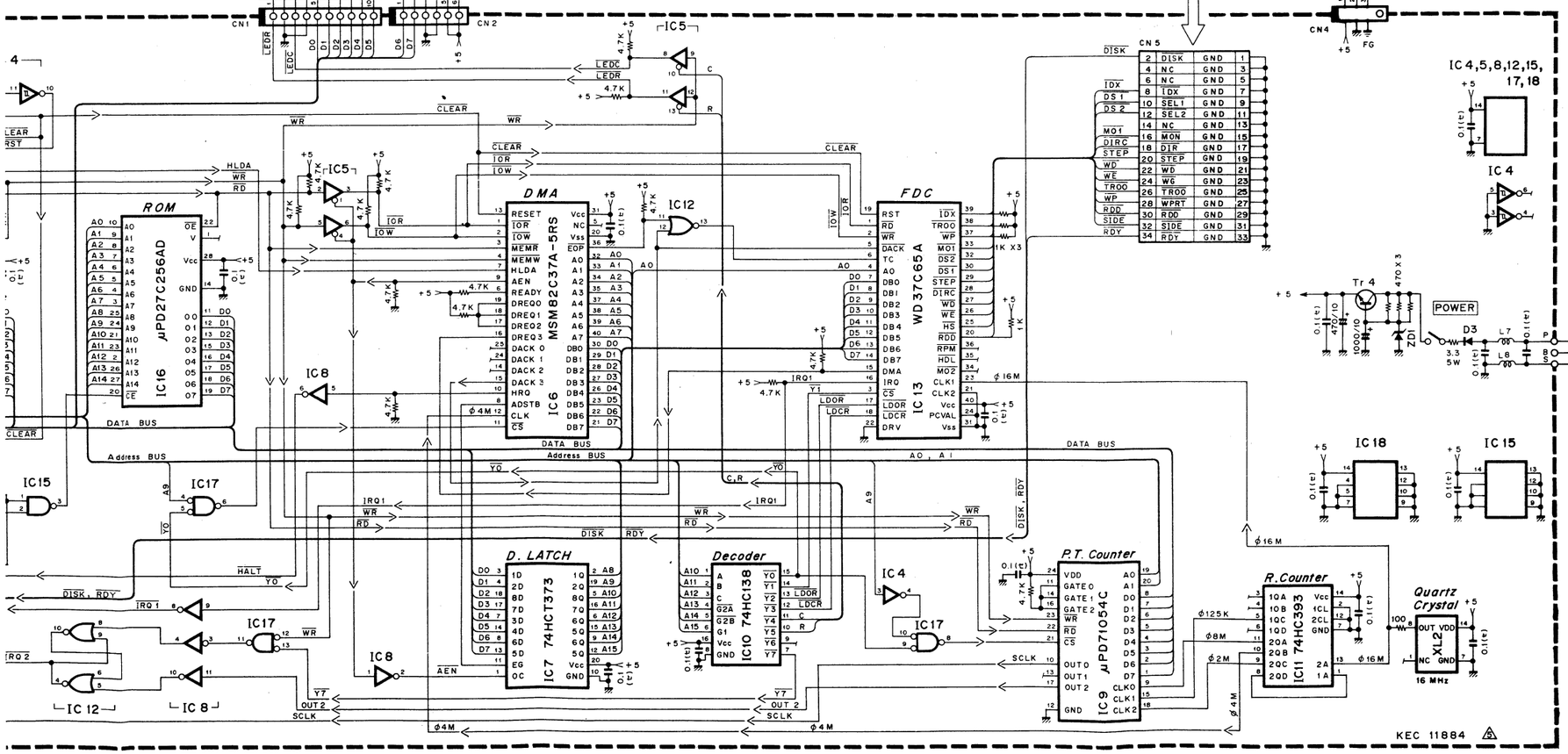


Memory map



DMA	M82C37A-5
FDC	WD37C65
LDOR	FDC operation register
LDCR	FDC control register
LED·R	LED digit select
LED·C	LED segment
PTC	µPD71054C
IRQ2RST	IRQ2 reset



Notes)
* Circuit Board
CPU (VF307100) XE480D0

1. IC
IC 1: HD63C03YP (XB529001) MPU
IC 2: TC55257PL-12 (XD314A00) SRAM
IC 3: PST518B-2 (IG116200) SYSTEM RESET
IC 4: TC74HC14P (IR001400) INV
IC 5: TC74HC125P (IR012500) 3-BUFF
IC 6: MSM82C37A-5RS (XE908A00) DMA
IC 7: TC74HCT373 (XC750A00) D-LATCH
IC 8: TC74HCT04P (XA830001) INV
IC 9: µPD71054C (XC310A00) PTC
IC10: TC74HC138P (IR013800) DEC0-8
IC11: TC74HC393P (IR039300) CNT
IC12: TC74HC02P (IR000200) NOR
IC13: WD37C65A (XE909A00) FDC
IC14: TC74HC244P (IR024400) BUS. BUF
IC15: TC74HC00P (IR000000) NAND
IC16: µPC27C256AD-12 (XE941G00) EPROM 120n sec.
IC17, 18: TC74HC32P (IR003200) OR
2. Photo Coupler
PC 1: P2822 (VF099600)
3. Transistor
Tr 1 ~ 3: 2SC1815 Y (IC181520)
Tr 4: 2SD880 O, Y (ID088020)
4. Diode
D 1, 2: 1SS176 (IX000760)
D 3: 11ES4 (VB481900)
5. Zener Diode
ZD 1: MTZ5.6B 5.6V (VA007600)
6. Resistor Array
RA 1: EXB-F9E103J5 (VB187500)
RA 2 ~ 4: EXB-F9E472J5 (VB187300)
7. Semiconductive Cera. Cap.
Marked (ŧ): 0.1µF 16V (FZ004170)
8. Monolithic Cera. Cap.
Marked (ŧ): 0.1µF 50V Z (VB971200)
9. Quartz Crystal Unit
XL 1: 12.0M HC-18/U (VE463500)
XL 2: 16M TD308A (QU008200)
10. Coil
L 1 ~ 6, 9, 10: FL5R200QN 20µH (VB971100)
L 7, 8: SN3-205 10µH (GE901870)
11. Push Switch
SPPJ22941A U (VF678900) POWER

MUSIC DISK RECORDER

MDR-3/MDR-3P

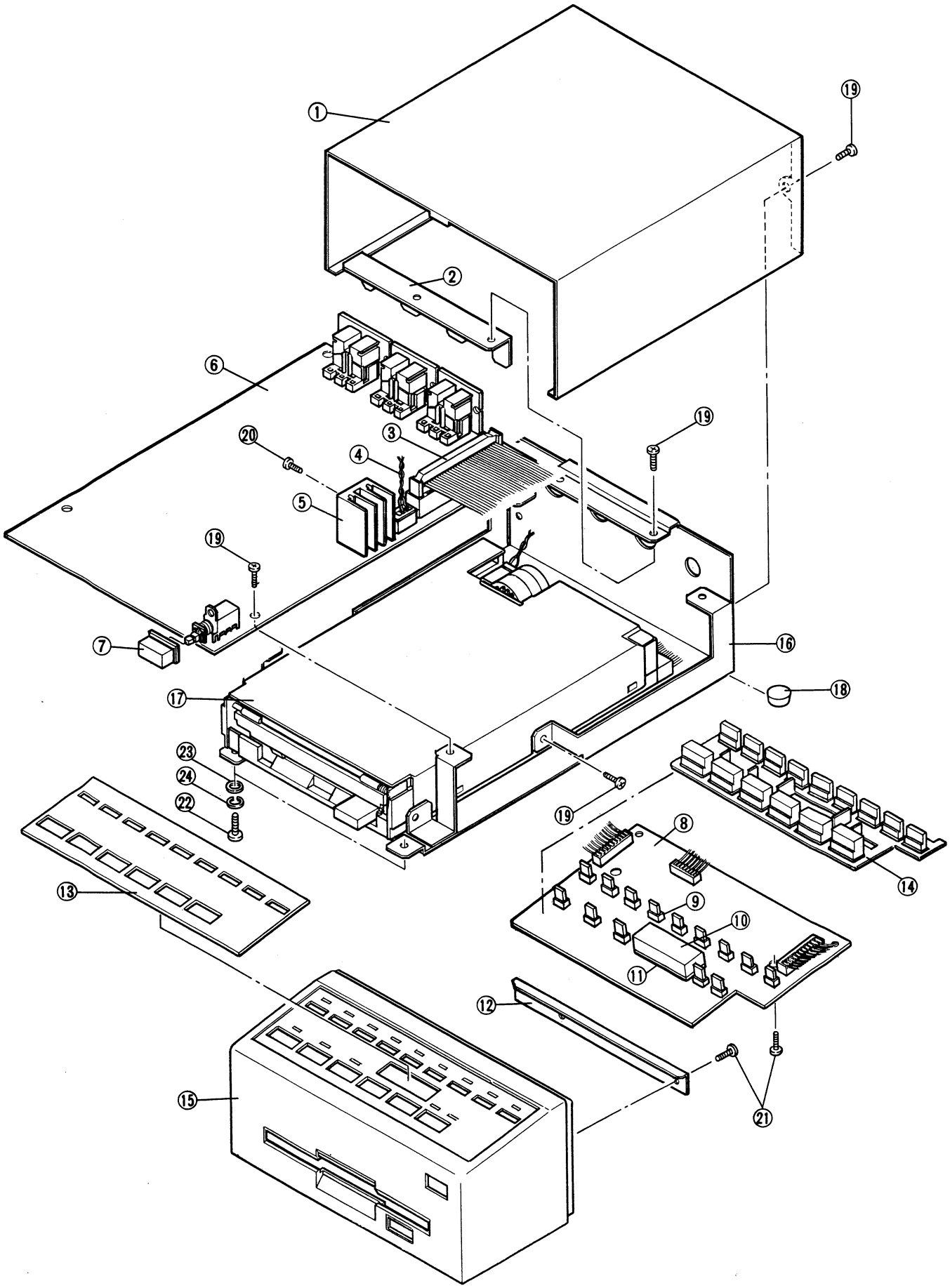
PARTS LIST

[MDR-3 : U、C、H
MDR-3 P : J]

Notes DESTINATION ABBREVIATIONS

J	: Japanese model	A	: Australian model
U	: U.S.A. model	E	: European model
C	: Canadian model	D	: West German model
X	: General model	B	: British model
M	: South African model	I	: Indonesian model
H	: North European model		

■OVERALL ASSEMBLY（総組立）



■OVERALL ASSEMBLY（総組立）

	Ref. No.	Part No.	Description		部品名	Remarks	ランク
*	1	VF705200	Upper Case		上ケース		08
*	2	VF705400	Holder,MIDI		ＭＩＤＩ固定金具		02
*	3	VB295200	Cable,FD		ＦＤ束線		04
*	4	VB295400	Cable,FC2		ＦＣ２束線		07
*	5	VF679100	Heat Sink	OSH-1622-SP	ヒートシンク		03
*	6	VF307100	Circuit Board	CPU	ＣＰＵシート		36
*	7	VF705700	Button	GY	ボタン（Ｐ）		01
*	8	VF307200	Circuit Board	PN	ＰＮシート		13
	9	CB055980	LED Holder		ＬＥＤホルダー		01
*	10	VF343900	LED Display	GL3P412	ＬＥＤディスプレイ		08
*	11	VG616600	LED Spacer		ＬＥＤスペーサー		
*	12	VF705500	Angle Bracket		基板受け金具		01
*	13	VF706200	Sheet		シート		05
*	14	VF705800	Rubber Contact		接点ゴム		06
*	15	VF706000	Panel		パネル		06
*	16	VF706100	Lower Case		下ケース		09
*	17	VF637700	FDD,3.5inch	ND-352S-A	３．５インチＦＤＤ	4261G5K	31
	18	CB034480	Stopper	BL	ストッパー（Ｂ）		01
	19	ED330056	Bind Head Screw	3.0X5 ZMC2BL	バインド小ネジ		01
	20	ED030086	Bind Head Screw	3.0X8 ZMC2Y	バインド小ネジ		01
	21	ET030066	Bind Head Tapping Screw	3.0X6 ZMC2Y	ﾊﾞｲﾝﾄﾞﾀｯﾋﾟﾝｸﾞﾈｼﾞ		01
	22	EA330066	Pan Head Screw	3.0X6 ZMC2BL	ナベ小ネジ		01
	23	EV203300	Flat Washer	φ3.0 FCM3BL	平座金		01
	24	EV303306	Spring Washer	φ3.0 ZMC2BL	バネ座金		01

＊：New Parts（新規部品）

ランク：Japan Only

■ELECTRICAL PARTS（電気部品）

Ref. No.	Part No.	Description		部品名	Remarks	ランク
＊＊	VF307100	Circuit Board	CPU	CPUシート		36
＊＊	VF307200	Circuit Board	PN	PNシート		13
＊＊	VF307100	Circuit Board	CPU	CPUシート		36
	IG116200	IC	PST518B-2	IC	SYSTEM RESET	04
	IR000000	IC	TC74HC00P	IC	NAND	03
	IR000200	IC	TC74HC02P	IC	NOR	03
	IR001400	IC	TC74HC14P	IC	INV	05
	IR012500	IC	TC74HC125P	IC	3-BUFF	03
	IR024400	IC	TC74HC244P	IC	BUS.BUF	07
	IR039300	IC	TC74HC393P	IC	CNT	04
	XA830001	IC	TC74HCT04P	IC	INV	03
＊	XC750A00	IC	TC74HCT373	IC	D-LATCH	04
	IR013800	IC	TC74HC138P	IC	DECO-8	05
	XB529001	IC	HD63C03YP	IC	MPU	13
＊＊	XC310A00	IC	μPD71054C	IC	PTC	06
＊＊＊	XE908A00	IC	MSM82C37A-5RS	IC	DMA	08
＊＊	XE909A00	IC	WD37C65A	IC	FDC	12
	XD314A00	IC	TC55257PL-12	IC	SRAM	13
＊＊	XE941G00	IC	μPC27C256AD12	IC	EPROM 12nsec.	
	IR003200	IC	TC74HC32P	IC	OR	03
＊＊	VF099600	Photo Coupler	P2822	フォトカプラ		05
	IC181520	Transistor	2SC1815 Y	トランジスタ		03
	ID088020	Transistor	2SD880 O,Y	トランジスタ		03
	VB481900	Diode	11ES4	ダイオード		01
	IX000760	Diode	1SS176	ダイオード		01
	VA007600	Zener Diode	MTZ5.6B 5.6V	ツェナーダイオード		01
	HM553220	Wire Wound Resistor	3.3Ω 5W	セメント抵抗		02
	VB187300	Resistor Array	EXB-F9E472J5	抵抗アレイ		01
	VB187500	Resistor Array	EXB-F9E103J5	抵抗アレイ		01
	UJ129100	Electrolytic Cap.	1000μF 10.0V	ケミコン		02
	FZ004170	Semiconductive Cera. Cap.	0.1μF 16V	半導体セラコン		01
	VB971200	Monolithic Cera. Cap.	0.1μF 50V Z	積層セラコン		01
	VB971100	Coil	FL5R200QN 20μH	コイル		01
	GE901870	Coil	SN3-205 10μH	コイル		03
	VE463500	Quartz Crystal Unit	12.0M AT-49	水晶振動子		03
	QU008200	Quartz Crystal Unit	16M TD308A	水晶振動子		10
＊	VG798700	Push Switch	SPPJ22966A U	プッシュスイッチ	POWER	
	LB500590	DIN Jack	5P TCS4650-	DINジャック	MIDI IN/OUT/THR	02
	LB302260	Connector	HEC0470	電源コネクタ	DC IN	02
＊	VF307200	Circuit Board	PN	PNシート		13
	IR037400	IC	TC74HC374P	IC	D.FF	06
	IG111000	Transistor Array	TD62503P	トランジスタアレイ		03
＊	VF343800	Transistor Array	TD62505P	トランジスタアレイ		03
	IX000760	Diode	1SS176	ダイオード		01
	VB167000	LED	TLS211 RE	LED		01
	VB167100	LED	TLG211 GR	LED	PLAY	01
＊＊	VF343900	LED Display	GL3P412	LEDディスプレイ		08
＊＊	VG616600	LED Spacer		LEDスペーサー		
	CB055980	LED Holder		LEDホルダー		01
	VB971200	Monolithic Cera. Cap.	0.1μF 50V Z	積層セラコン		01

＊：New Parts（新規部品）

ランク：Japan Only