mLAN EXPANSION BOARD

mLAN16E

SERVICE MANUAL

■ **CONTENTS (目次)**

SY 011725
20040325-49800

YAMAHA
HAMAMATSU, JAPAN

Copyright (c) Yamaha Corporation. All rights reserved. PDF-K247 '04.03

IMPORTANT NOTICE

This manual has been provided for the use of authorized Yamaha Retailers and their service personnel. It has been assumed that basic service procedures inherent to the industry, and more specifically Yamaha Products, are already known and understood by the users, and have therefore not been restated.

WARNING : Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components and failure of the product to perform as specified. For these reasons, we advise all Yamaha product owners that all service required should be performed by an authorized Yamaha Retailer or the appointed service representative.

IMPORTANT : This presentation or sale of this manual to any individual or firm does not constitute authorization certification, recognition of any applicable technical capabilities, or establish a principal-agent relationship of any form.

The data provided is belived to be accurate and applicable to the unit(s) indicated on the cover. The research engineering, and service departments of Yamaha are continually striving to improve Yamaha products. Modifications are, therefore, inevitable and changes in specification are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING : Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground bus in the unit (heavy gauge black wires connect to this bus.)

IMPORTANT : Turn the unit OFF during disassembly and parts replacement. Recheck all work before you apply power to the unit.

WARNING: CHEMICAL CONTENT NOTICE!

The solder used in the production of this product contains LEAD. In addition, other electrical/electronic and/or plastic (Where applicable) components may also contain traces of chemicals found by the California Health and Welfare Agency (and possibly other entities) to cause cancer and/or birth defects or other reproductive harm.

DO NOT PLACE SOLDER, ELECTRICAL/ELECTRONIC OR PLASTIC COMPONENTS IN YOUR MOUTH FOR ANY REASON WHAT SO EVER!

Avoid prolonged, unprotected contact between solder and your skin! When soldering, do not inhale solder fumes or expose eyes to solder/flux vapor!

If you come in contact with solder or components located inside the enclosure of this product, wash your hands before handling food.

■ WARNING

Components having special characteristics are marked ⚠ and must be replaced with parts having specification equal to those originally installed.

⚠ 印の商品は、安全を維持するために重要な部品です。交換する場合は、安全のために必ず指定の部品をご使用ください。

■ SPECIFICATIONS

Functions

Data Rate	S400, S200	(Automatically set by included mLAN Graphic Patchbay.)
Audio Inputs and Outputs		
	16 Ins, 16 Outs	(4 Stereo Ins, 16 Outs when MOTIF ES is connected.)
Sampling rate	44.1kHz, 48kHz, 88.2kHz, 96kHz (+6%, –10%)	
		(Enables you to match other sampling frequencies in the network without changing the rate on the mother unit.)
MIDI connectors 6 Ins, 6 Outs		(4 Ins, 4 Outs when MOTIF ES is con-nected.)
Wordclock Transition Speed setting		
Slow/Fast mode		(Specified by included mLAN Graphic Patchbay or Auto Connector.)

Display

LED	ACTIVE (blue)

Jacks

To IEEE1394	6-pin x 2
To Mother	100P

Dimensions

127(W) x 164.5(D) x 36(H) mm

Weight

325g (excluding mother unit connecting cables)
415g (including mother unit connecting cables)

■ 総合仕様

機能

Data Rate	**S400,S200**	**（付属の mLAN Graphic Patchbay により、自動設定）**
Audio 入出力	**16In 16Out**	**（MOTIF ES に接続した場合、4StereoIN 、16OUT ）**
対応サンプリング周波数		
	44.1kHz 、48kHz 、88.2kHz 、96kHz (+6%, － 10%)	
		（マザー機のFs を変更することなく、mLAN上の種々のFs とインターフェース可能）
MIDI 入出力ポート数		
	6In 6Out	**（MOTIF ES に接続した場合、4IN 、4OUT ）**
PLL 応答性切替	**slow/fast**	
		（付属の mLAN Graphic Patchbay または mLAN Auto Connector により設定可能）

表示

LED	**ACTIVE(青）**

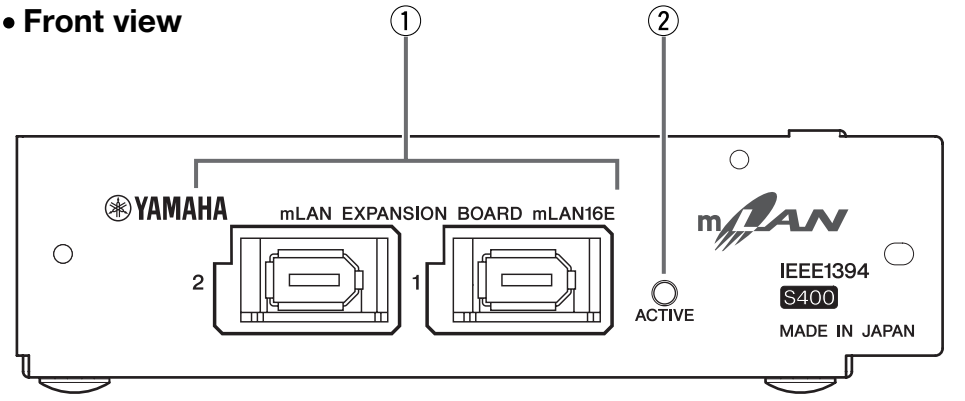
接続端子

To IEEE1394	**6Pin x 2**
To Mother	**100P**

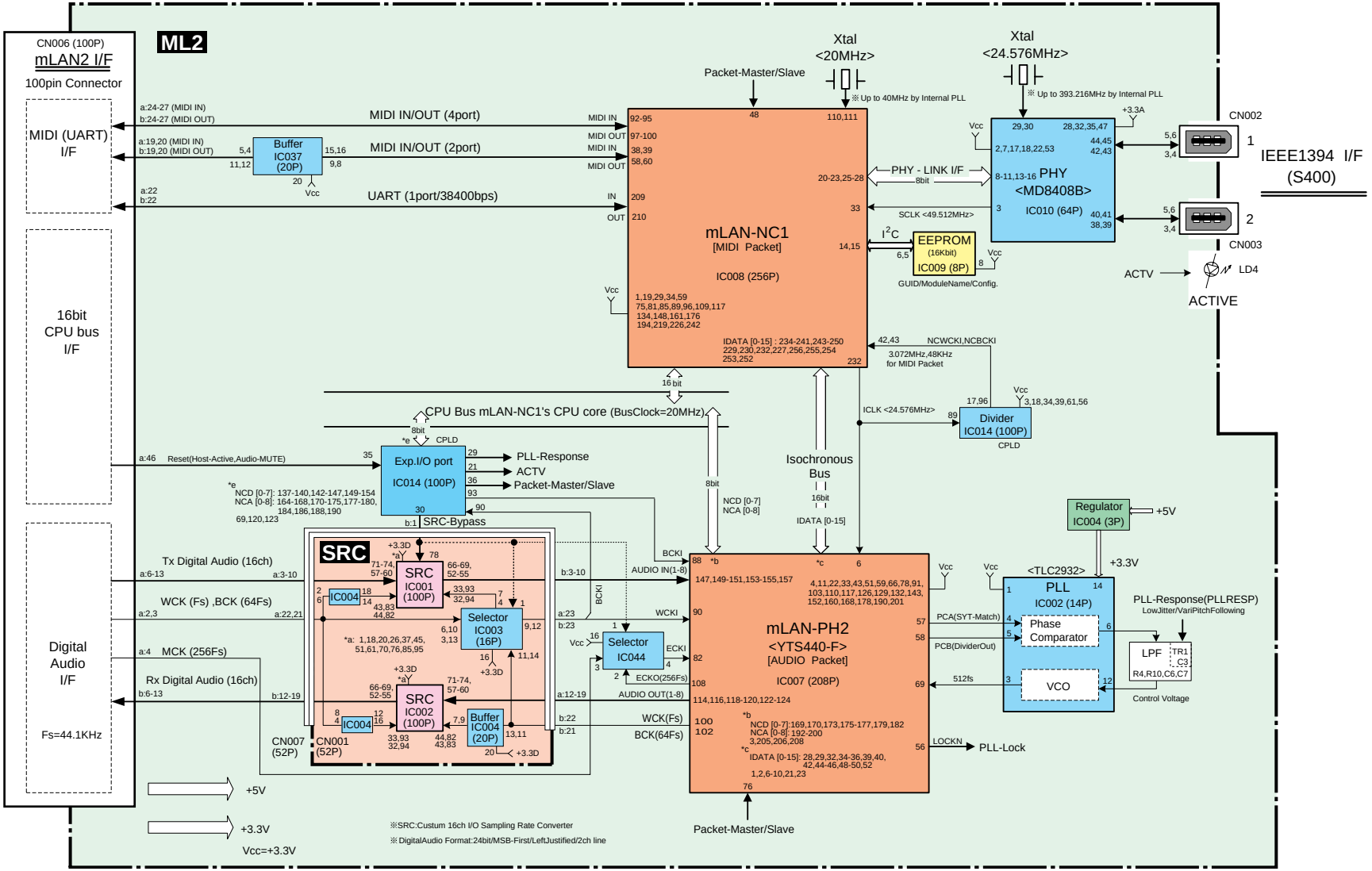
寸法、重量	**127mm (W)x 164.5mm (D)x 36mm (H)**
	325g （マザー接続用ケーブル無し）,415g （マザー接続用ケーブル付き）

■ PANEL LAYOUT（パネルレイアウト）

• Front view

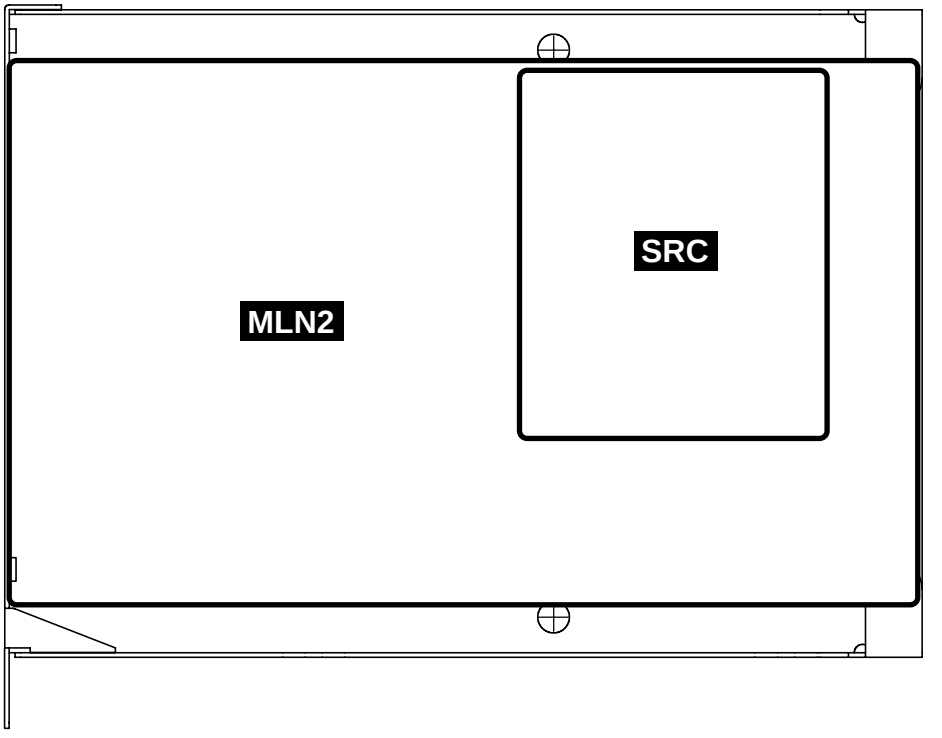


① mLAN (EEE1394) connectors（mLAN（IEEE1394）端子）
② ACTIVE lamp（アクティブ ランプ）


ML2
CN006 (100P)
mLAN2 I/F
100pin Connector
MIDI (UART) I/F
16bit CPU bus I/F
Digital Audio I/F
Fs=44.1KHz
MIDI IN/OUT (4port)
MIDI IN/OUT (2port)
UART (1port/38400bps)
Buffer IC037 (20P)
Xtal <20MHz>
※Up to 40MHz by Internal PLL
Packet-Master/Slave
Xtal <24.576MHz>
※ Up to 393.216MHz by Internal PLL
mLAN-NC1
[MIDI Packet]
IC008 (256P)
PHY - LINK I/F
8bit
PHY <MD8408B>
IC010 (64P)
SCLK <49.512MHz>
I2C
EEPROM (16Kbit) IC009 (8P)
GUID/ModuleName/Config.
CN002
CN003
IEEE1394 I/F (S400)
ACTV
LD4
ACTIVE
IDATA [0-15] : 234-241,243-250 229,230,232,227,256,255,254 253,252
NCWCKI,NCBCKI
3.072MHz,48KHz for MIDI Packet
ICLK <24.576MHz>
Divider IC014 (100P)
CPU Bus mLAN-NC1's CPU core (BusClock=20MHz)
Isochronous Bus
Exp.I/O port IC014 (100P)
Reset(Host-Active,Audio-MUTE)
PLL-Response
ACTV
Packet-Master/Slave
SRC-Bypass
NCD [0-7]: 137-140,142-147,149-154
NCA [0-8]: 164-168,170-175,177-180, 184,186,188,190
69,120,123
NCD [0-7]
NCA [0-8]
IDATA [0-15]
Regulator IC004 (3P)
+5V
+3.3V
<TLC2932>
PLL IC002 (14P)
PLL-Response(PLLRESP)
LowJitter/VariPitchFollowing
Phase Comparator
VCO
LPF
R4,R10,C6,C7
Control Voltage
PCA(SYT-Match)
PCB(DividerOut)
512fs
LOCKN
PLL-Lock
mLAN-PH2
<YTS440-F>
[AUDIO Packet]
IC007 (208P)
SRC
SRC IC001 (100P)
SRC IC002 (100P)
IC004
Selector IC003 (16P)
Selector IC044
Buffer IC004 (20P)
CN001 (52P)
CN007 (52P)
Tx Digital Audio (16ch)
WCK (Fs) ,BCK (64Fs)
MCK (256Fs)
Rx Digital Audio (16ch)
BCKI
WCKI
ECKI
ECKO(256Fs)
AUDIO IN(1-8)
AUDIO OUT(1-8)
WCK(Fs)
BCK(64Fs)
Vcc=+3.3V
※SRC:Custum 16ch I/O Sampling Rate Converter
※DigitalAudio Format:24bit/MSB-First/LeftJustified/2ch line

■ CIRCUIT BOARD LAYOUT（ユニットレイアウト）

• **Top view**



■ DISASSEMBLY PROCEDURE（分解手順）

1. SRC Circuit Board
(Time required: About 1 minutes)

1-1. Remove the two (2) double locking spacers. The SRC circuit board can then be removed. (Photo. 1)

2. SRC Circuit Board
(Time required: About 1 minutes)

2-1. Remove the SRC circuit board. (See Procedure 1.)

2-2. Remove the two (2) screw marked [30] and the two (2) screw marked [40]. The MLN2 circuit board can then be removed. (Photo. 1, 2)

1. SRC シート (所要時間:約１分)

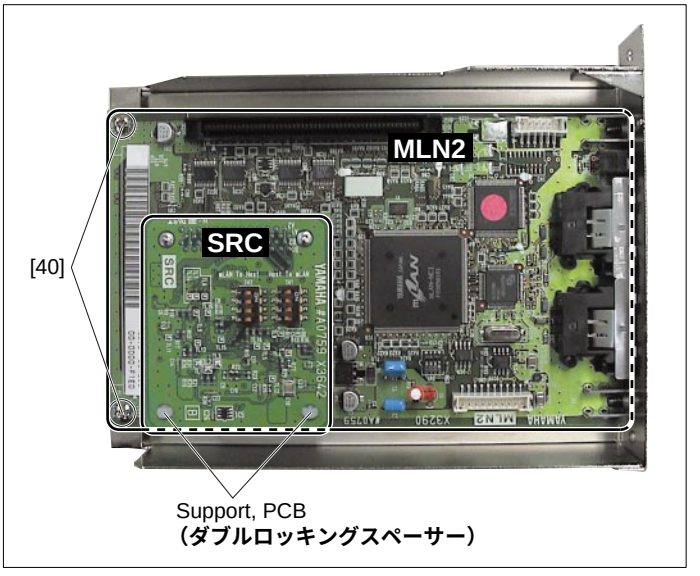
1-1. ダブルロッキングスペーサー２ケ所を外し、SRC シートを外します。(写真１)

2. MLN2 シート (所要時間:約１分)

2-1. SRC シートを外します。(１項参照)

2-2. [30]のネジ2本と[40] のネジ2本を外し、MLN2シートを外します。(写真１, 2)

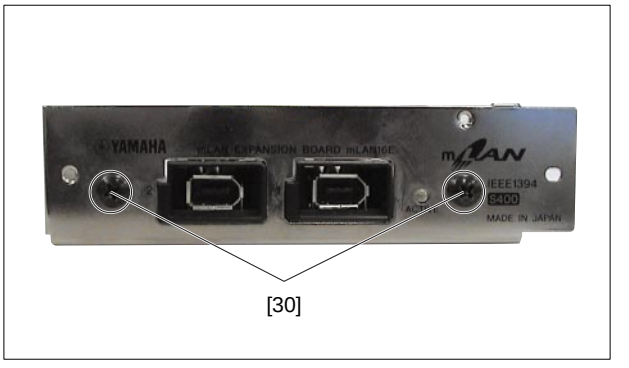
• **Top view**



[40]: Bind Head Tapping Screw-B（＋バインドBタイト）
3.0X6 MFNI33 (VZ544100)

Photo. 1（写真1）

• **Front view**



[30]: Bind Head Tapping Screw-S（＋バインドSタイト）
4.0X8 MFZN2BL (V6655200)

Photo. 2（写真2）

■ LSI PIN DESCRIPTION (LSI 端子機能表)

● S1L54423F21B000 (X4072A00) SRC16

SRC: IC001,002

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	VDD	-	Power supply +3.3V	51	VDD	-	Power supply +3.3V
2	JUMPSEL	I	Digital PLL sensitivity select	52	BOSD3	O	Serial data output for B block
3	TABLESEL	I	Digital PLL capture speed select	53	BOSD2	O	Serial data output for B block
4	SCANENB	I	Test pin (GND connect with normal)	54	BOSD1	O	Serial data output for B block
5	ATPGENE	I	Test pin (GND connect with normal)	55	BOSD0	O	Serial data output for B block
6	VSS	-	Ground	56	VSS	-	Ground
7	PLLTEST	I	Test pin (GND connect with normal)	57	BISD3	I	Serial data input for B block
8	PLLRESN	I	Reset input (Master clock PLL)	58	BISD2	I	Serial data input for B block
9	PLLVSS	-	Ground (Master clock PLL)	59	BISD1	I	Serial data input for B block
10	MVDD	-	Power supply (Digital)	60	BISD0	I	Serial data input for B block
11	PLLVSS	-	Ground (Master clock PLL)	61	VDD	-	Power supply +3.3V
12	AVDD	-	Power supply (Analog)	62	DIVSEL1	I	Clock frequency for DIVCLK0 terminal
13	PLLCHGO	O	Output signal for external filter of master clock PLL	63	DIVSEL0	I	Clock frequency for DIVCLK0 terminal
14	LPVSS	I	Input signal for external filter of master clock PLL	64	DIVCLK0	O	Master clock output
15	PLLBP	I	Test pin (GND connect with normal)	65	VSS	-	Ground
16	VSS	-	Ground (Digital)	66	AOSD3	O	Serial data output for A block
17	EXTCLK1	I	Input for master clock PLL	67	AOSD2	O	Serial data output for A block
18	VDD	-	Power supply +3.3V (Digital)	68	AOSD1	O	Serial data output for A block
19	EXTCLK0	O	Output XO terminal	69	AOSD0	O	Serial data output for A block
20	VDD	-	Power supply +3.3V	70	VDD	-	Power supply +3.3V
21	TESTENB	I	Test pin (GND connect with normal)	71	AISD3	I	Serial data input for A block
22	TESTIP0	I	Test pin (GND connect with normal)	72	AISD2	I	Serial data input for A block
23	TESTIP1	I	Test pin (GND connect with normal)	73	AISD1	I	Serial data input for A block
24	TESTIP2	I	Test pin (GND connect with normal)	74	AISD0	I	Serial data input for A block
25	VSS	-	Ground	75	VSS	-	Ground
26	VDD	-	Power supply +3.3V	76	VDD	-	Power supply +3.3V
27	PHASEMATCH	I	Phase muching mode ON/OFF	77	AODAMPN	I	Damp output data for A block
28	VSS	-	Ground	78	AIBYPASS	I	Bypass for A block input/output
29	XI	I	Crystal osc. input	79	AISFTUP0	I	Shiftup for A block input data
30	XO	O	Crystal osc. output	80	AISFTUP1	I	Shiftup for A block input data
31	VSS	-	Ground	81	VSS	-	Ground
32	BOBCLK	I/O	Bit clock input/output for B block data output	82	AILRCK	I/O	Word clock input/output for A block input data
33	BOLRCK	I/O	Word clock input/output for B block data output	83	AIBCLK	I/O	Bit clock input/output for A block input data
34	BOFMT2	I	Data output format for B block	84	A_WCK_OK	O	Lock frag for A block input/output
35	BOFMT1	I	Data output format for B block	85	VDD	-	Power supply +3.3V
36	BOFMT0	I	Data output format for B block	86	AIFMT0	I	Data input format for A block
37	VDD	-	Power supply +3.3V	87	AIFMT1	I	Data input format for A block
38	BIFMT2	I	Data input format for B block	88	AIFMT2	I	Data input format for A block
39	BIFMT1	I	Data input format for B block	89	VSS	-	Ground
40	BIFMT0	I	Data input format for B block	90	AOFMT0	I	Data output format for A block
41	VSS	-	Ground	91	AOFMT1	I	Data output format for A block
42	B_WCK_OK	O	Lock frag for B block input/output	92	AOFMT2	I	Data output format for A block
43	BIBCLK	I/O	Bit clock input/output for B block data input	93	AOLRCK	I/O	Word clock input/output for A block output data
44	BILRCK	I/O	Word clock input/output for B block data input	94	AOBCLK	I/O	Bit clock input/output for A block output data
45	VDD	-	Power supply +3.3V	95	VDD	-	Power supply +3.3V
46	BISFTUP1	I	Shiftup for B block input data	96	REGDAT	I	Data input for serial register
47	BISFTUP0	I	Shiftup for B block input data	97	REGCLK	I	Clock input for serial register
48	BIBYPASS	I	Bypass for B block input/output	98	REGENB	I	Enable signal input for serial register
49	BODAMPN	I	Damp output data for B block	99	ICN	I	Initial clear input
50	VSS	-	Ground	100	VSS	-	Ground

● **YTS440B-FZ** (X3009B00)**mLAN-PH2** (mLAN™ Packet Handler 2)

MLN2: IC007

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	IRERRN	I	Isochronous packet error flag input (Low active)	105	BCK128O	O	Bit clock output for digital audio output (128Fs)
2	IRCVN	I	Isochronous reception enable input (Low active)	106	MCKO	O	Master clock output for digital audio output (64Fs to 384Fs)
3	IRXN	I	Isochronous reception data enable input (Low active)	107	VSS	-	Ground
4	VDD	-	+3.3 V	108	ECKO	O	Bit clock output for reception to outside (128Fs or 256Fs)
5	VSS	-	Ground	109	EWCKO	O	Word clock output for reception to outside (Fs)
6	ICLK	I	Isochronous master clock input (24.576MHz)	110	VDD	-	+3.3 V
7	CYCLEOUT	I	Isochronous cycle out signal input	111	PCLK	O	Parallel data transfer clock output (128Fs or 256Fs)
8	ICS	I	Isochronous cycle start signal input	112	VSS	-	Ground
9	CT	I	Isochronous cycle timer enable input	113	NC	-	
10	ITXN	I	Isochronous transmission data enable input (Low active)	114	PDIO0	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
11	VDD	I	+3.3 V	115	NC	-	
12	VSS	I	Ground	116	PDIO1	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
13	NC	-		117	VDD	-	+3.3 V
14	NC	-		118	PDIO2	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
15	SCANE	I	Input for LSI test (usually connected to ground)	119	PDIO3	I/O	
16	TSTI0	I		120	PDIO4	I/O	
17	TSTI1	I	Input for LSI test (usually connected to ground)	121	VSS	-	Ground
18	TSTI2	I		122	PDIO5	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
19	TSTI3	I		123	PDIO6	I/O	
20	VSS	-	Ground	124	PDIO7	I/O	
21	ITREQN	OD	Isochronous transmission request output (Low active)	125	NC	-	
22	VDD	-	+3.3 V	126	VDD	-	+3.3 V
23	IEOPN	OD	Isochronous transmission packet test data signal output (Low active)	127	NC	-	
24	NC	-		128	NC	-	
25	NC	-		129	VDD	-	+3.3 V
26	NC	-		130	VSS	-	Ground
27	VSS	-	Ground	131	NC	-	
28	IDATA0	I/O	Isochronous data input/output	132	VDD	-	3.3 V
29	IDATA1	I/O		133	NC	-	
30	NC	-		134	PDIO8	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
31	NC	-		135	PDIO9	I/O	
32	IDATA2	I/O	Isochronous data input/output	136	NC	-	
33	VDD	-	+3.3 V	137	PDIO10	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
34	IDATA3	I/O	Isochronous data input/output	138	VSS	-	
35	IDATA4	I/O		139	PDIO11	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
36	IDATA5	I/O		140	PDIO12	I/O	
37	VSS	-	Ground	141	NC	-	
38	NC	-		142	PDIO13	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
39	IDATA6	I/O	Isochronous data input/output	143	VDD	-	+3.3 V
40	IDATA7	I/O		144	PDIO14	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
41	NC	-		145	NC	-	
42	IDATA8	I/O	Isochronous data input/output	146	PDIO15	I/O	Digital audio output (when PAR is "0") or parallel data bus (lower 16 bits) (when PAR is "1")
43	VDD	-	+3.3 V	147	PDIO16	I/O	Digital audio input (when PAR is "0") or parallel data bus (upper 16 bits) (when PAR is "1")
44	IDATA9	I/O	Isochronous data input/output	148	VSS	-	Ground
45	IDATA10	I/O		149	PDIO17	I/O	Digital audio input (when PAR is "0") or parallel data bus (upper 16 bits) (when PAR is "1")
46	IDATA11	I/O		150	PDIO18	I/O	
47	VSS	-	Ground	151	PDIO19	I/O	
48	IDATA12	I/O	Isochronous data input/output	152	VDD	-	+3.3 V
49	IDATA13	I/O		153	PDIO20	I/O	Digital audio input (when PAR is "0") or parallel data bus (upper 16 bits) (when PAR is "1")
50	IDATA14	I/O		154	PDIO21	I/O	
51	VDD	-	+3.3 V	155	PDIO22	I/O	
52	IDATA15	I/O	Isochronous data input/output	156	VSS	-	Ground
53	SEQO	O	Loop connection output when 2 to 4 chips are used simultaneously	157	PDIO23	I/O	Digital audio input (when PAR is "0") or parallel data bus (upper 16 bits) (when PAR is "1")
54	DBC	O	DBC timing output	158	PDIO24	I/O	
55	VSS	-	Ground	159	PDIO25	I/O	
56	LOCKN	O	PLL lock flag output (Low active)	160	VDD	-	+3.3 V
57	PCA	O	Output for PLL external phase comaparator	161	PDIO26	I/O	Digital audio input (when PAR is "0") or parallel data bus (upper 16 bits) (when PAR is "1")
58	PCB	O	Output for PLL external phase comaparator	162	PDIO27	I/O	
59	VDD	-	+3.3 V	163	PDIO28	I/O	
60	TSTI4	I	Input for LSI test (usually connected to ground)	164	VSS	-	Ground
61	TSTI5	I		165	PDIO29	I/O	Digital audio input (when PAR is "0") or parallel data bus (upper 16 bits) (when PAR is "1")
62	TSTI6	I		166	PDIO30	I/O	
63	TSTI7	I		167	PDIO31	I/O	
64	NC	-		168	VDD	-	3.3 V
65	TXE	I/O	Enable output (for master), input (for slave) for multi-chip transmission	169	HD0	I/O	Data input/output
66	VDD	-	+3.3 V	170	HD1	I/O	
67	NC	-		171	NC	-	
68	VSS	-	Ground	172	NC	-	
69	VCOCLK	I	PLL external VCO clock input	173	HD2	I/O	Data input/output
70	SVCO0	I	VCO frequency setting input	174	VSS	-	Ground
71	SVCO1	I	VCO frequency setting input	175	HD3	I/O	Data input/output
72	SMCK0	I	MCKO clock division rate setting input	176	HD4	I/O	
73	NC	-		177	HD5	I/O	
74	NC	-		178	VDD	-	+3.3 V
75	SMCK1	I	MCKO clock division rate setting input	179	HD6	I/O	Data input/output
76	SLV	I	0: Master, 1: Slave when 2 to 4 chips are used simultaneously	180	NC	-	
77	SEQI	I	Loop connection input when 2 to 4 chips are used simultaneously	181	NC	-	
78	VDD	-	+3.3 V	182	HD7	I/O	Data input/output
79	NC	-		183	IRQN	OD	Interrupt request output (Low active)
80	NC	-		184	VSS	-	Ground
81	VSS	-	Ground	185	NC	-	
82	ECKI	I	Bit clock inout for receptin from outside (128Fs or 256Fs)	186	TSTI12	I	Input for LSI test (usually connected to ground)
83	EWCKI	I	Word clock input for reception from output (Fs)	187	TSTI13	I	
84	PAR	I	Selection of serial, parallel input/output, 0: Serial, 1: Parallel	188	NC	-	
85	PDIR	I	Parallel data direction input, 0: Input, 1: Output	189	TSTI14	I	Input for LSI test (usually connected to ground)
86	PDE	I	Parallel data enable input	190	VDD	-	+3.3 V
87	BCK128I	I	Bit clock input for digital audio input (128Fs)	191	VSS	-	Ground
88	BCKI	I	Bit clock input for digital audio input (32Fs to 128Fs)	192	HA0	I	Address input
89	NC	-		193	HA1	I	Address input
90	WCKI	I	Word clock input for digitral audio input (Fs)	194	HA2	I	Address input
91	VDD	-	+3.3 V	195	HA3	I	Address input
92	VSS	-	Ground	196	HA4	I	Address input
93	SWCK	I/O	Word clock output (for master), input (for slave) for multi-chip transmission	197	HA5	I	Address input
94	TSTI8	I	Input for LSI test (usually connected to ground)	198	HA6	I	Address input
95	TSTI9	I		199	HA7	I	Address input
96	TSTI10	I		200	HA8	I	Address input
97	TSTI11	I		201	VDD	-	+3.3 V
98	VSS	-	Ground	202	VSS	-	Ground
99	NC	-		203	NC	-	
100	WCKOD	O	Delay output of WCKO (Fs)	204	ICN	I	Initial clear input (Low active)
101	WCKO	O	Word clock output for digital audio output (Fs)	205	CSN	I	Chip select input (Low active)
102	BCKO	O	Bit clock output for digital audio output (64Fs)	206	WRN	I	Write enable input (Low active)
103	VDD	-	+3.3 V	207	NC	-	
104	NC	-		208	RDN	I	Read enable input (Low active)

● **mLAN-NC1** (X2150A00) mLAN™ Link Controller

MLN2: IC008

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	VDD		Power terminal	66	MCKO	O	Master clock output for digital audio output
2	TEST5	I	Test terminal	67	WCKOD	O	Delayed output of WCKO
3	TEST4	I	Test terminal	68	IEC958O	O	IEC60958 signal output from built-in DIT
4	TEST3	I	Test terminal	69	INT R SEL	I	Selection of PLL division rate setting bit for SYT
5	TEST2	I	Test terminal	70	SEL MCK1	I	MCKO division rate setting bit 1
6	TEST1	I	Test terminal	71	SEL MCK0	I	MCKO division rate setting bit 0
7	SCANE	I	Test terminal	72	SEL VCO1	I	Division rate setting bit 1 for SYT PLL
8	TRST	I	JTAG terminal	73	SEL VCO0	I	Division rate setting bit 0 for SYT PLL
9	TMS	I	JTAG terminal	74	AUX1	I	External VCO clock input for SYT PLL
10	TCK	I	JTAG terminal	75	VDD		Power terminal
11	VSS		Ground terminal	76	PCA	O	External phase comparator output for SYT PLL
12	TDO	O	JTAG terminal	77	PCB	O	External phase comparator output for SYT PLL
13	TDI	I	JTAG terminal	78	LOCKN1	O	Lock flag output for SYT PLL
14	SCL	O	EEPROM serial clock	79	VSS		Ground terminal
15	SDA	I/O	EEPROM serial data	80	VCO 01 CLK	I	External VCXO input for digital PLL1 (SYT)
16	ASYNCFLG	I/O	Asynchronous flag	81	VDD		Power terminal
17	ISOFLG	I/O	Isochronous flag	82	PLL 01 Pump SK	TRI	Pump signal to sink current for PLL1
18	BUSRST	O	Bus reset	83	VSS		Ground terminal
19	VDD		Power terminal	84	PLL 01 Pump SC	TRI	Pump signal to source current for PLL1
20	D7	I/O	PHY I/F data bus	85	VDD		Power supply terminal
21	D6	I/O	PHY I/F data bus	86	VCO 02 CLK	I	External VCO input for digital PLL2 (SYT)
22	D5	I/O	PHY I/F data bus	87	VSS		Ground terminal
23	D4	I/O	PHY I/F data bus	88	PLL 02 Pump SK	TRI	Pump signal to sink current for PLL2
24	VSS		Ground terminal	89	VDD		Power terminal
25	D3	I/O	PHY I/F data bus	90	PLL 02 Pump SC	TRI	Pump signal to source current for PLL2
26	D2	I/O	PHY I/F data bus	91	VSS		Ground terminal
27	D1	I/O	PHY I/F data bus	92	MI0	I	MIDI input 0
28	D0	I/O	PHY I/F data bus	93	MI1	I	MIDI input 1
29	VDD		Power terminal	94	MI2	I	MIDI input 2
30	CTL1	I/O	PHY-LINK control: Control signal for interface with PHY chip	95	MI3	I	MIDI input 3
				96	VDD		Power supply terminal
31	CTL0	I/O	PHY-LINK control: Control signal for interface with PHY chip	97	MO0	O	MIDI output 0
				98	MO1	O	MIDI output 1
32	VSS		Ground terminal	99	MO2	O	MIDI output 2
33	SCLK	I	Master clock	100	MO3	O	MIDI output 3
34	VDD		Power terminal	101	VSS		Ground terminal
35	LREQ	O	Link request	102	DIR SCK	O	To SCK of built-in DIR5
36	VSS		Ground terminal	103	DIR SO	O	To SI of built-in DIR5
37	LPS	O	Link power status	104	DIR SI	I(PU)	To SO of built-in DIR5
38	DAI0	I	Digital audio input 0 /MIDI input 4	105	DIR CSN	O	To /CS of built-in DIR5
39	DAI1	I	Digital audio input 1 /MIDI input 5	106	DIR INT	I	To INT of built-in DIR5
40	DAI2	I	Digital audio input 2 /MIDI input 6	107	DIR LOCKN	I	To /LOCK of built-in DIR5
41	DAI3	I	Digital audio input 3 /MIDI input 7	108	ERR BS	I	To ERR/BS of built-in DIR5
42	BCKI	I	Bit clock input for digital audio input	109	VDD		Power terminal
43	WCKI	I	Word clock input for digital audio input	110	XTAL(OSC3)	I	MPU clock oscillation circuit terminal
44	DITI	I	Audio data input when using built-in DIT separately	111	XTAL(OSC4)	O	MPU clock oscillation circuit output terminal
45	DIT MCI	I	Master clock input when using built-in DIT separately (128Fs clock)	112	VSS		Ground terminal
				113	DBL V	I	To DBL/V of built-in DIR5
46	DIT BCI	I	Bit clock input when using built-in DIT separately (32Fs to 128Fs)	114	FS128 C	I	To FS128/C built-in of DIR5
				115	SYNC U	I	To SYNC/U built-in of DIR5
47	DIT WCI	I	Word clock input when using built-in DIT separately	116	DIR SDI	I	To SDO of built-in DIR5
				117	VDD		Power terminal
48	SLV	I	Master: L, Slave : H when using a multiple number of packet handler chips simultaneously, fixed at Low when using mLAN-NC1 only	118	WRH#	I/O	Write enable high: host data bus write signal
				119	WAIT#	I/O	External bus wait signal
				120	WRL#	I/O	Write enable low: host data bus write signal
49	SEQI	I	Loop connection input pin when using a multiple number of packet handler chips simultaneously, fixed at Low when using mLAN-NC1 only	121	PLLC	I	Capacitor connection terminal for MPU oscillation PLL circuit
				122	VSS		Ground terminal
50	VSS		Ground terminal	123	RD#	I/O	Read enable : host data bus read signal
51	ECKI	I	Bit clock input for audio signal receiving (128Fs clock)	124	RESET#	I	Hardware reset signal
52	EWCKI	I	Word clock input for audio signal receiving	125	BCLK	O	MPU bus clock output signal
53	EWCKI2	I	Word clock input for PSC4 function	126	VSS		Ground terminal
54	ECKI2	I	Bit clock input for PSC4 function (128Fs clock)	127	DMAEND0#	I/O	DMA END signal
55	SEQO	O	Loop connection output pin when using a multiple number of packet handler chips simultaneously	128	DREQ# mLAN	I/O	In 8415 mode, data request output when transferring DMA of Non-Audio RxFIFO#0 and in standalone mode, MPU K50/DMAREQ0 signal
56	ECKO	O	Bit clock output for audio signal receiving (128Fx)	129	DACK# mLAN	I/O	In 8415 mode, acknowledge input when transferring DMA of Non-Audio RxFIFO#0 and in standalone mode, MPU P32/DMADACK0 signal
57	EWCKO	O	Word clock output for audio signal receiving				
58	DAO0	O	Digital audio output 0/MIDI output 4				
59	VDD		Power terminal	130	CS# mLAN/CE9#	I/O	In 8415 mode, chip select input of PH1 block from microprocessor and in standalone mode, MPUCE9 signal
60	DAO1	O	Digital audio output 1/MIDI output 5				
61	DAO2	O	Digital audio output 2/MIDI output 6				
62	DAO3	O	Digital audio output 3/MIDI output 7	131	BUSGET#	I/O	MPU bus GET signal
63	BCKO	O	Bit clock output for digital audio output (64Fs clock)	132	BUSACK#	I/O	MPU bus ACK signal
64	VSS		Ground terminal	133	BUSREQ#	I/O	MPU bus REQ signal
65	WCKO	O	Word clock output for digital audio output	134	VDD		Power terminal

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
135	IRQ# mLAN	I/O	In 8415 mode, interrupt request output from PH1 block to microprocessor	205	P00/SRXD1	I/O	General purpose port 00/serial I/F
				206	P01/STXD1	I/O	General purpose port 01/serial I/F
136	CE8#	TRI	MPU CE8 signal	207	P02/SCLK1#	I/O	General purpose port 02/serial I/F
137	CPU D0	I/O	MPU data bus	208	P03/SRDY1#	I/O	General purpose port 03/serial I/F
138	CPU D1	I/O	MPU data bus	209	P04/SRXD2	I/O	General purpose port 04/serial I/F
139	CPU D2	I/O	MPU data bus	210	P05/STXD2	I/O	General purpose port 05/serial I/F
140	CPU D3	I/O	MPU data bus	211	P06/SCLK2#	I/O	General purpose port 06/serial I/F
141	VSS		Ground terminal	212	P07/SRDY2#	I/O	General purpose port 07/serial I/F
142	CPU D4	I/O	MPU data bus	213	INT3#	O	LINK section interrupt signal
143	CPU D5	I/O	MPU data bus	214	GPIO[0]	I/O	LINK section general purpose input/output signal
144	CPU D6	I/O	MPU data bus	215	GPIO[1]	I/O	LINK section general purpose input/output signal
145	CPU D7	I/O	MPU data bus	216	TXE	I/O	Enable output (SLV:L), input (SLV:H)for multi chip transmission
146	CPU D8	I/O	MPU data bus				
147	CPU D9	I/O	MPU data bus	217	SWCK	I/O	Word clock output (SLV:L), input (SLV:H) for multi chip transmission
148	VDD		Power terminal				
149	CPU D10	I/O	MPU data bus	218	X2SPD#	I	Double speed mode
150	CPU D11	I/O	MPU data bus	219	VDD		Power terminal
151	CPU D12	I/O	MPU data bus	220	LINKON	I	LinkOn input signal
152	CPU D13	I/O	MPU data bus	221	DIRECT	I	PHY I/F direct select signal
153	CPU D14	I/O	MPU data bus	222	CS# LINK	I	LINK section chip select signal
154	CPU D15	I/O	MPU data bus	223	INT1# LINK	I/O	In 8415 mode, LINK section interrupt signal 1 and in standalone mode, MPU P26 signal
155	VSS		Ground terminal				
156	CE4#	TRI	MPU CE4 signal	224	INT2# LINK	I/O	In 8415 mode, LINK section interrupt signal 2 and in standalone mode, MPU P27 signal
157	MISC0	I/O	General purpose input/output terminal				
158	MISC1	I/O	General purpose input/output terminal	225	VSS		Ground terminal
159	MISC2	I/O	General purpose input/output terminal	226	BUSMASTER	I	MPU bus master
160	CE10EX#	I/O	MPU CE10EX signal	227	CYCLEOUT	I/O	In normal mode: Iso cycle output. When only PH1 at work: Isochronous cycle OUT signal input
161	VDD		Power terminal				
162	NMI#	I	MPU NMI signal	228	VDD		Power terminal
163	TST	I	Test terminal	229	IRERR#	I/O	In normal mode: Isochronous packet error flag. When only PH1 at work: Isochronous packet error flag input
164	CPU A19	I/O	MPU address bus				
165	CPU A18	I/O	MPU address bus				
166	CPU A17	I/O	MPU address bus	230	IRCV#	I/O	In normal mode: Isochronous packet reception enable. When only PH1 at work: Isochronous reception enable input
167	CPU A16	I/O	MPU address bus				
168	CPU A15	I/O	MPU address bus				
169	VSS		Ground terminal	231	IRX#	I/O	In normal mode: Isochronous reception data enable. When only PH1 at work: Isochronous reception data enable input
170	CPU A14	I/O	MPU address bus				
171	CPU A13	I/O	MPU address bus				
172	CPU A12	I/O	MPU address bus	232	ICLK	I/O	In normal mode: Isochronous bus master clock. When only PH1 at work: Isochronous master clock input
173	CPU A11	I/O	MPU address bus				
174	CPU A10	I/O	MPU address bus				
175	CPU A9	I/O	MPU address bus	233	VSS		Ground terminal
176	VDD		Power terminal	234	IDATA15	I/O	Isochronous data bus
177	CPU A8	I/O	MPU address bus	235	IDATA14	I/O	Isochronous data bus
178	CPU A7	I/O	MPU address bus	236	IDATA13	I/O	Isochronous data bus
179	CPU A6	I/O	MPU address bus	237	IDATA12	I/O	Isochronous data bus
180	CPU A5	I/O	MPU address bus	238	IDATA11	I/O	Isochronous data bus
181	CPU A4	I/O	MPU address bus	239	IDATA10	I/O	Isochronous data bus
182	CPU A23	I/O	MPU address bus	240	IDATA9	I/O	Isochronous data bus
183	VSS		Ground terminal	241	IDATA8	I/O	Isochronous data bus
184	CPU A3	I/O	MPU address bus	242	VDD		Power terminal
185	CPU A22	I/O	MPU address bus	243	IDATA7	I/O	Isochronous data bus
186	CPU A2	I/O	MPU address bus	244	IDATA6	I/O	Isochronous data bus
187	CPU A21	I/O	MPU address bus	245	IDATA5	I/O	Isochronous data bus
188	CPU A1	I/O	MPU address bus	246	IDATA4	I/O	Isochronous data bus
189	CPU A20	I/O	MPU address bus	247	IDATA3	I/O	Isochronous data bus
190	CPU A0	I/O	MPU address bus	248	IDATA2	I/O	Isochronous data bus
191	EA10MD0	I	MPU area 10 boot mode select signal	249	IDATA1	I/O	Isochronous data bus
192	EA10MD1	I	MPU area 10 boot mode select signal	250	IDATA0	I/O	Isochronous data bus
193	EA10MD2	I	MPU area 10 boot mode select signal	251	VSS		Ground terminal
194	VDD		Power terminal	252	ITX#	I/O	In normal mode: Isochronous transmission data enable. When only PH1 at work: Isochronous transmission data enable input
195	DSIO	I/O	Serial input/output terminal for debugging				
196	P14/DCLK	I/O	General purpose port 14/serial input/output terminal for debugging	253	IEOP#	I/O	In normal mode: if other NC1 or PH2 is cascade connected: Isochronous transmission packet end. When only PH1 at work: Isochronous transmission packet end output
197	P13/DPC0	I/O	General purpose port 13/serial input/output terminal for debugging				
198	P12/DST2	I/O	General purpose port 12/serial input/output terminal for debugging	254	ITREQ#	I/O	In normal mode: if other NC1 or PH2 is cascade connected: Isochronous transmission request. When only PH1 at work: Isochronous transmission request output
199	P11/DST1	I/O	General purpose port 11/serial input/output terminal for debugging				
200	P10/DST0	I/O	General purpose port 10/serial input/output terminal for debugging	255	CT	I/O	In normal mode: cycle timer enable. When only PH1 at work: Isochronous cycle timer enable input
201	VSS		Ground terminal				
202	PLLS0	I	MPU PLL setting terminal	256	ICS	I/O	In normal mode: Isochronous Cycle Start Packet transmission/reception timing output. When only PH1 at work: isochronous cycle start signal input
203	PLLS1	I	MPU PLL setting terminal				
204	TEST6 TVEP	I	Test terminal				

● **XCR3064XL-10 VQ100C** (X3628D00) **CPLD** (Complex Programmable Logic Device) MLN2: IC014

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	NC	-	(Unconnected)	48	I/O309	O	Output terminal which is write enable (L active) for the flash memory assigned to CE9 zone of mLAN-NC1
2	NC	-	(Unconnected)				
3	VCC	I	Power supply (3.3V)	49	NC	-	(Unconnected)
4	I/O209/TDI	I	Terminal for loading data	50	NC	-	(Unconnected)
5	NC	-	(Unconnected)	51	VCC	I	Power supply (+3.3V)
6	I/O210	I	Terminal for reading 8th bit setting of DIP switch	52	I/O308	O	Output terminal which is output enable (L active) for SRAM assigned to CE9 zone of mLAN-NC1
7	NC	-	(Unconnected)				
8	I/O211	I	Terminal for reading 7th bit setting of DIP switch	53	NC	-	(Unconnected)
9	I/O212	I	Terminal for reading 6th bit setting of DIP switch	54	I/O307	O	Output terminal which is write enable (L active) for SRAM assigned to CE9 zone of mLAN-NC1
10	I/O213	I	Terminal for reading 5th bit setting of DIP switch				
11	PORT_EN	I	Terminal for selecting functions of pins No.4, 15, 62, 73 Connecting this terminal to GND changes the function of these pins into data loading only	55	NC	-	(Unconnected)
				56	I/O306	O	Output terminal which is high byte enable (L active) for SRAM assigned to CE9 zone of mLAN-NC1
12	I/O214	I	Terminal for reading 4th bit setting of DIP switch	57	I/O305	O	Output terminal which is low byte enable (L active) for SRAM assigned to CE9 zone of mLAN-NC1
13	I/O215	I	Terminal for reading 3rd bit setting of DIP switch				
14	I/O216	I	Terminal for reading 2nd bit setting of DIP switch	58	I/O304	I	Connected to pin No.130 (/CE9) of mLAN-NC1
15	I/O401/TMS	I	Terminal for loading data	59	GND	I	GND
16	I/O402	I	Terminal for reading 1st bit setting of DIP switch	60	I/O303	I	Connected to pin No.118 (/WRH) of mLAN-NC1
17	I/O403	O	Terminal for outputting clock as a result of ICLK (24.576MHz) output from mLAN-NC1 divided by 8. This clock is connected to pin No.42 (BCKI) of mLAN-NC1.	61	I/O302	I	Connected to pin No.120 (/WRL) of mLAN-NC1
				62	I/O301/TCK	I	Terminal for loading data
				63	I/O116	I	Connected to pin No.123 (/RD) of mLAN-NC1
18	VCC	I	Power supply (+3.3V)	64	I/O115	I	Connected to pin No.190 (CPU A0) of mLAN-NC1
19	I/O404	O	Output terminal of control signal to select clock for outputting audio signal from mLAN-PH2. (H level: Clock usable for up to Fs=96K is selected, L level: Clock unusable for Fs=96K is selected) [Default on L level]	65	I/O114	I	Connected to pin No.187 (CPU A21) of mLAN-NC1
				66	VCC	I	Power supply (+3.3V)
				67	I/O113	I	Connected to pin No.189 (CPU A20) of mLAN-NC1
				68	I/O112	I	Connected to pin No.164 (CPU A19) of mLAN-NC1
20	I/O405	O	Terminal used so that inappropriate data immediately after turning on the power is not output from MLN2 circuit board against MIDI signal output from mLAN-NC1. (H level: Invalid data is output, L level: Valid data is output)	69	I/O111	O	Chip select signal of mLAN-PH2 is output. Connected to pin No.205 of mLAN-PH2.
				70	NC	-	(Unconnected)
				71	I/O110	I	Connected to pin No.156 (/CE4) of mLAN-NC1
21	I/O406	O	This terminal changes to H level when MLN2 circuit board operates normally as node of mLAN.	72	NC	-	(Unconnected)
				73	I/O109/TD0	O	Terminal for loading data
22	NC	-	(Unconnected)	74	GND	I	GND
23	I/O407	I	Word clock output from pin No.101 (WCKO)of mLAN-PH2 is inputted. Used for audio signal mute circuit.	75	I/O108	I/O	Connected to pin No.145 (CPU D7) of mLAN-NC1
				76	I/O107	I/O	Connected to pin No.144 (CPU D6) of mLAN-NC1
24	NC	-	(Unconnected)	77	NC	-	(Unconnected)
25	I/O408	I	Word clock inputted to pin No.90 (WCKI)of mLAN-PH2 is inputted. Used for audio signal mute circuit.	78	NC	-	(Unconnected)
				79	I/O106	I/O	Connected to pin No.143 (CPU D5) of mLAN-NC1
26	GND	I	Connected to GND	80	I/O105	I/O	Connected to pin No.142 (CPU D4) of mLAN-NC1
27	NC	-	(Unconnected)	81	I/O104	I/O	Connected to pin No.140 (CPU D3) of mLAN-NC1
28	NC	-	(Unconnected)	82	VCC	I	Power supply (+3.3V)
29	I/O409	O	Used to select response characteristic of PLL connected to mLAN-PH2. (H level: Low jitter characteristic, L level:High-speed response) [Default on H level]	83	I/O103	I/O	Connected to pin No.139 (CPU D2) of mLAN-NC1
				84	I/O102	I/O	Connected to pin No.138 (CPU D1) of mLAN-NC1
				85	I/O101	I/O	Connected to pin No.137 (CPU D0) of mLAN-NC1
30	I/O410	O	Used to control whether or not to bypass sampling frequency converter of SRC board when SRC board is installed to CN7 of MLN2 circuit board. (H level: Bypassing, L level: Not bypassing) [Default on L level]	86	GND	I	GND
				87	IN3/CLK3	I	Any MIDI signal output by mLAN-NC1 is inputted. Connected to pin No.58 (DA0[0]) of mLAN-NC1.
				88	IN2/CLK2	I	Connected to pin No.185 (CPU A22) of mLAN-NC1
				89	IN1/CLK1	I	Clock output from pin No.232 (ICLK) of mLAN-NC1 is inputted.
31	I/O411	O	When clock to output audio signals from mLAN-PH2 is not appropriate, outputs signal indicating that audio signals are not subject to synchronization is output.	90	IN0/CLK0	I	Bit clock (64Fs or 256Fs) from the main unit with MLN2 circuit board installed is inputted.
				91	VCC	I	Power supply (+3.3V)
32	I/O412	I	H level signal is inputted when using word clock output from MLN2 circuit board as clock source of the main unit.	92	I/O201	O	Clock (128Fs or 64Fs) as a result of division of the clock inputted to pin No.90 is output. Connected to pin No.87 (BCK128I) of mLAN-PH2
33	I/O413	O	When selected as word clock master among mLAN units, signal requesting to select the clock other then word clock output from MLN2 circuit board as clock source to the main unit. (H level: Word clock output from MLN2 circuit board is used as the source, L level: Clock other than the word clock output from MLN2 circuit board is used as the source)	93	I/O202	O	Clock (64Fs) as a result of division of the clock inputted to pin No.90 is output. Connected to pin No.88 (BCKI) of mLAN-PH2
				94	I/O203	O	Depending on operation condition, either lock signal of PLL connected to mLAN-PH2 or lock signal detected by firmware of mLAN-NC1 is output.
34	VCC	I	Power supply (+3.3V)	95	GND	I	Connected to GND
35	I/O414	I	Reset signal (L active) from the main unit with the MLN2 circuit board installed is inputted.	96	I/O204	O	Clock as a result of dividing ICLK (24.576MHz) output by mLAN-NC1 by 512 is output. Connected to pin No.43 (WCKI) of mLAN-NC1
36	I/O415	O	When executing packet transmission in mLAN, signal to select mLAN-NC1 or mLAN-PH2 for master operation is output. (H level: mLAN-PH2 for master operation, L level: mLAN-NC1 for master operation) [Default on L level]	97	I/O205	I	Terminal to operate internal divider so that clock output from pin No.92 and No.93 become 128Fs and 64Fs respectively when clock inputted to pin No.90 is 256Fs. When set to H level, clock is output from pins No.92 and No.93 without being divided. In such case, 64Fs clock is inputted to pin No.90.
37	I/O416	I	Reset signal (L active) output by reset IC on MLN2 circuit board is inputted.				
38	GND	I	GND	98	I/O206	I	Lock signal of PLL connected to mLAN-PH2 is inputted.
39	VCC	I	Power supply (+3.3V)	99	I/O207	O	Mute control signal of audio signal sent from the main unit with MLN2 circuit board installed is output. (H level: Muting executed)
40	I/O316	O	This terminal changes to H level when MLN2 circuit board becomes route node of IEEE1349.	100	I/O208	O	Mute control signal of audio signal sent to the main unit with MLN2 circuit board installed is output. (H level: Muting executed)
41	I/O315	I	Connected to pin No.255 (CT) of mLAN-NC1				
42	I/O314	O	Connected to pin No.3 (IRXN) of mLAN-PH2				
43	GND	I	GND				
44	I/O313	I	Connected to pin No.229 (/IRERR) of mLAN-NC1				
45	I/O312	I	Connected to pin No.231 (/IRX) of mLAN-NC1				
46	I/O311	I	Connected to pin No.230 (/IRCV) of mLAN-NC1				
47	I/O310	O	Output terminal which is output enable (L active) for the flash memory assigned to CE9 zone of mLAN-NC1				

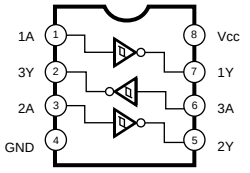
● **MD8408B** (XZ762A00) **PHY** (Physical Layer)

MLN2: IC010

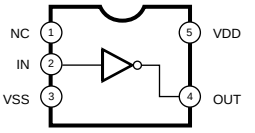
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	LREQ	I	Link request	35	AVDD1	-	Analog power supply 1
2	DVDD	-	Digital power supply	36	TpBias1	O	A cable bias output terminal
3	SCLK	O	49.152MHz link system clock	37	TpBias0	O	
4	DVSS	-	Digital ground	38	TpB1n	I/O	A negative-phase-sequence I/O terminal
5	CTL0	I/O	PHY-Link interface control signals	39	TpB1p	I/O	A positive-phase-sequence I/O terminal
6	CTL1	I/O		40	TpA1n	I/O	A negative-phase-sequence I/O terminal
7	DVDD	-	Digital power supply	41	TpA1p	I/O	A positive-phase-sequence I/O terminal
8	D0	I/O	PHY-Link interface data signals	42	TpB0n	I/O	A negative-phase-sequence I/O terminal
9	D1	I/O		43	TpB0p	I/O	A positive-phase-sequence I/O terminal
10	D2	I/O		44	TpA0n	I/O	A negative-phase-sequence I/O terminal
11	D3	I/O		45	TpA0p	I/O	A positive-phase-sequence I/O terminal
12	DVSS	-	Digital ground	46	AGND	-	Analog ground
13	D4	I/O	PHY-Link interface data signals	47	AVDD2	-	Analog power supply 2
14	D5	I/O		48	DVSS	-	Digital ground
15	D6	I/O		49	Disabled1	I	These pin define the initial value of the disable bits in the PHY port status page after a hardware reset, and the condition of the terminal of the level is reflected.
16	D7	I/O					
17	DVDD	-	Digital power supply				
18	DVDD	-		50	Disabled0	I	
19	TEST0	I	Test mode control terminals	51	S200	I	Phy Speed Control signal
20	TEST1	I		52	LDSEL	I	Timing setting terminal for the PHY-Link interface
21	DVSS	-	Digital ground	53	DVDD	-	Digital power supply
22	DVDD	-	Digital power supply	54	En_Accel	I	This bit defines the initial value of the Enab_accel bit after a hardware reset
23	DVSS	-	Digital ground				
24	Purb	I	External capacitor connection terminal for power-up reset	55	En_Multi	I	This bit defines the initial value of the Enab_multi bit after hardware reset
25	AGND	-	Analog ground	56	SR	I	Suspend/Resume function control signal
26	NC	-	Non connection	57	DIRECT	I	Defines operation mode setting terminal for the PHY-Link interface
27	NC	-					
28	AVDD1	-	Analog power supply 1	58	DVSS	-	Digital ground
29	XEXT	I/O	For crystal connections. Connection	59	LinkOn	O	Link-On signal output
30	XTAL	I/O	terminals for quartz crystal oscillators.	60	PC2	I	Power Class
31	AGND	-	Analog ground.	61	PC1	I	
32	AVDD1	-	Analog power supply 1	62	PC0	I	
33	CPS	I	A terminal for Cable Power Status detection	63	CMC	I	Configuration management capable setting terminal
34	AGND	-	Analog ground	64	LPS	I	Link power status

■ IC BLOCK DIAGRAM（IC ブロック図）

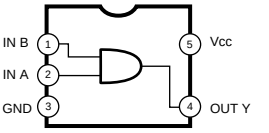
● **TC7W14F TE12L** (XR336A00)
Triple Inverter
MLN2: IC001,021



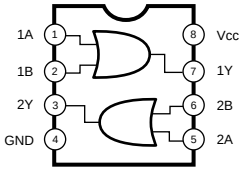
● **TC7S04F** (XM182A00)
Inverter Gate
MLN2: IC041



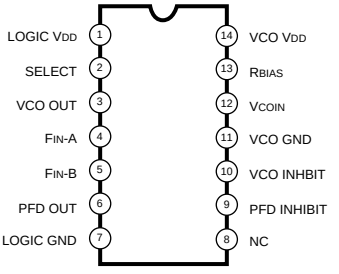
● **TC7SH08FU** (XR680A00)
2 Input AND Gate
MLN2: IC017

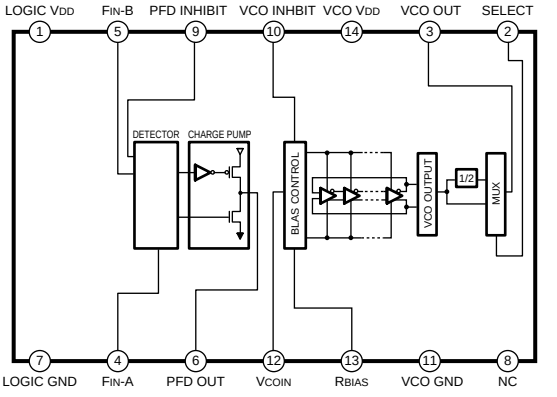


● **TC7W32FU (TE12L)** (XQ173A00)
Dual 2 Input OR Gate
MLN2: IC038,045

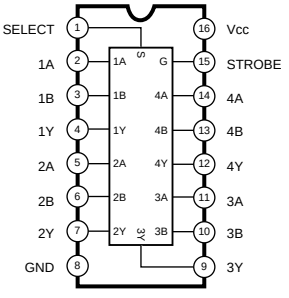


● **TLC2932IPWR** (XV064A00)
PLL
MLN2: IC002

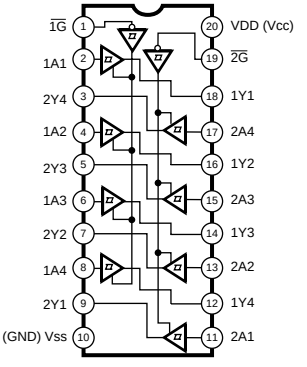




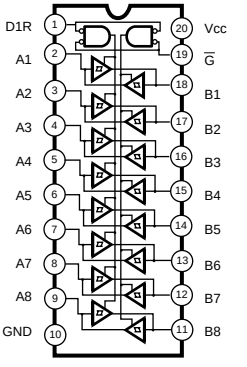
● **TC74VHC157FT**(X0199A00)
Quad 2 to 1 Multiplexer
MLN2: IC044
SRC: IC003



● **HD74LVC244ATELL**(X2308A00)
Octal 3-State Bus Buffer
MLN2: IC036,040
SRC: IC004

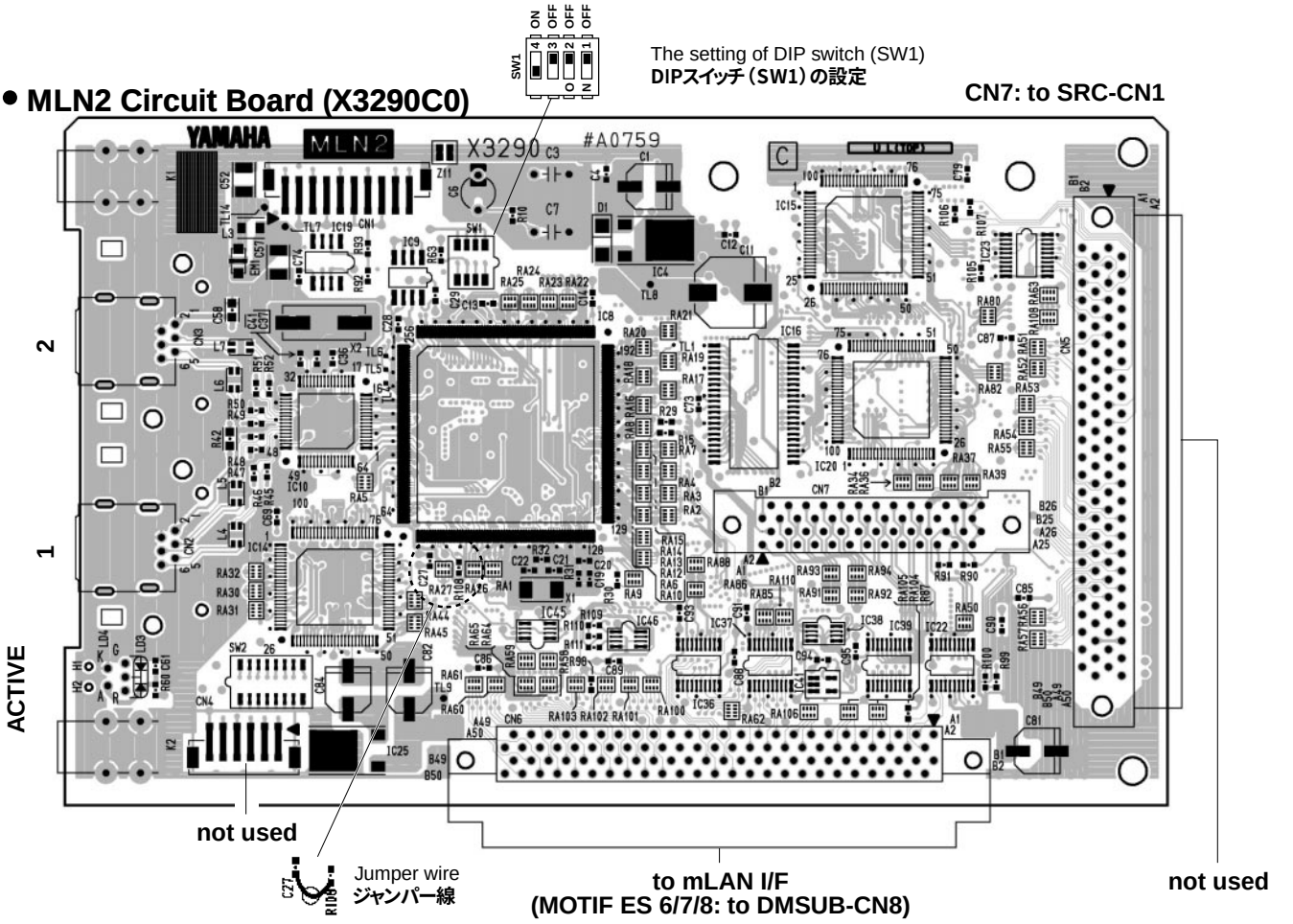


● **HD74LVC245ATELL**(XW148A00)
● **SN74LVC245APWR**(XZ287A00)
Octal 3-State Bus Transceiver
MLN2: IC022,026,035,039

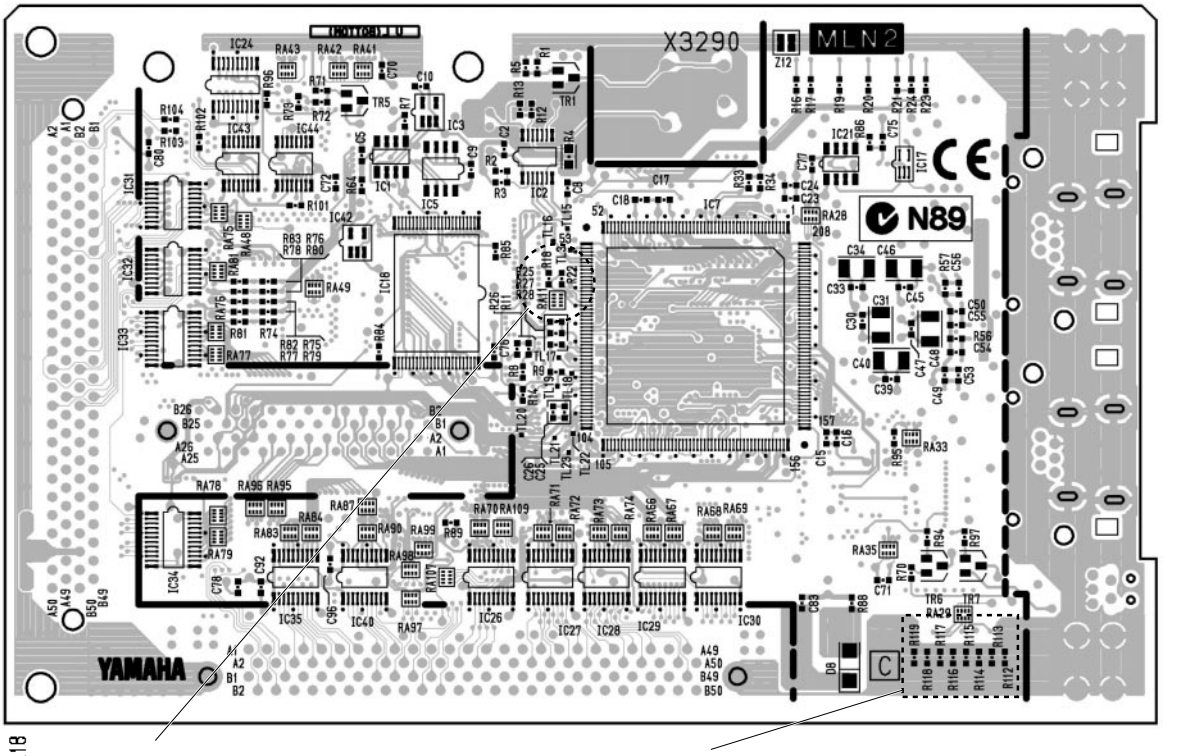


■ CIRCUIT BOARDS（シート基板図）

• MLN2 Circuit Board (X3290C0)



Component side（部品側）

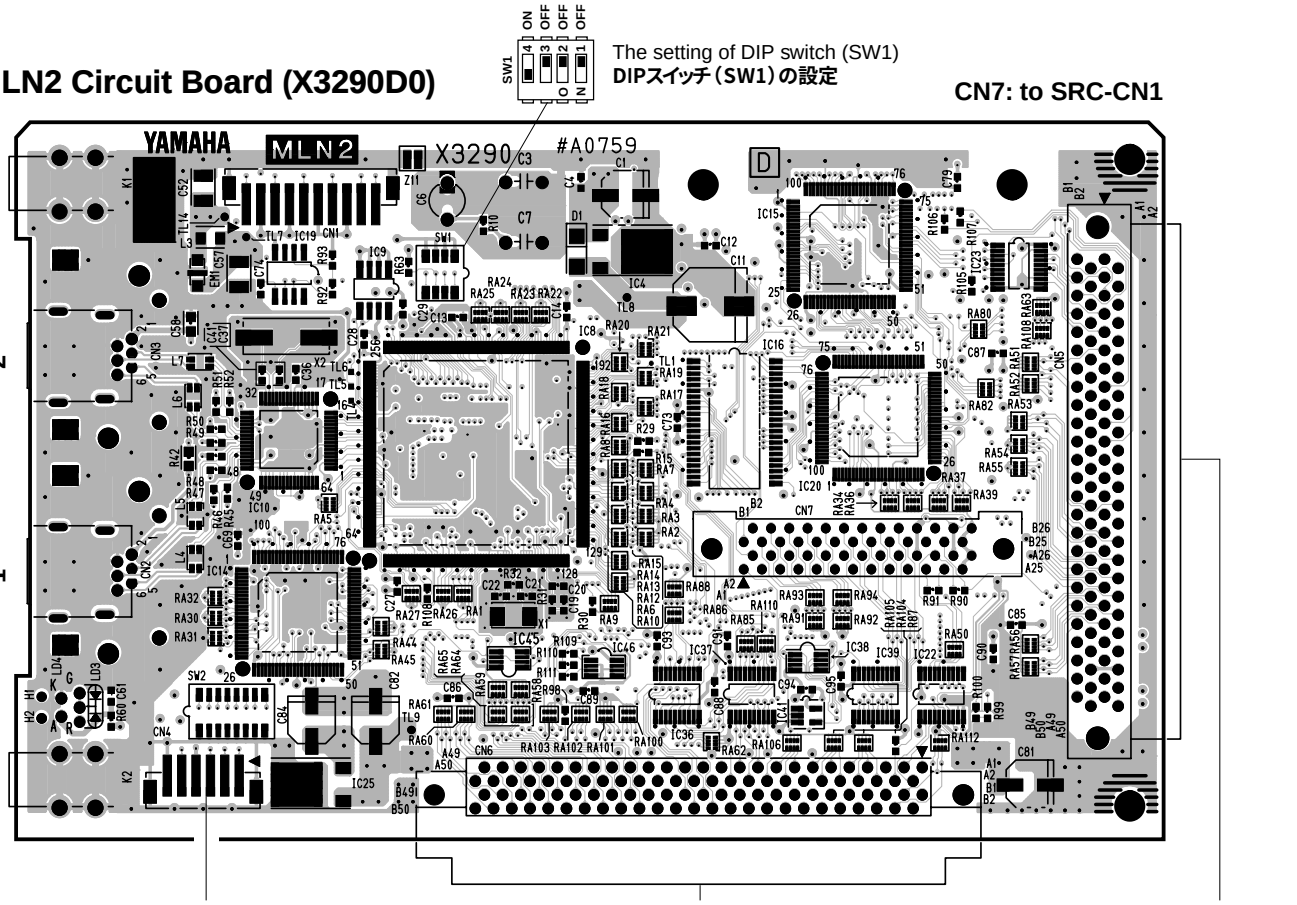


R18 is diagonally mounted.
R18は斜めに実装されています。

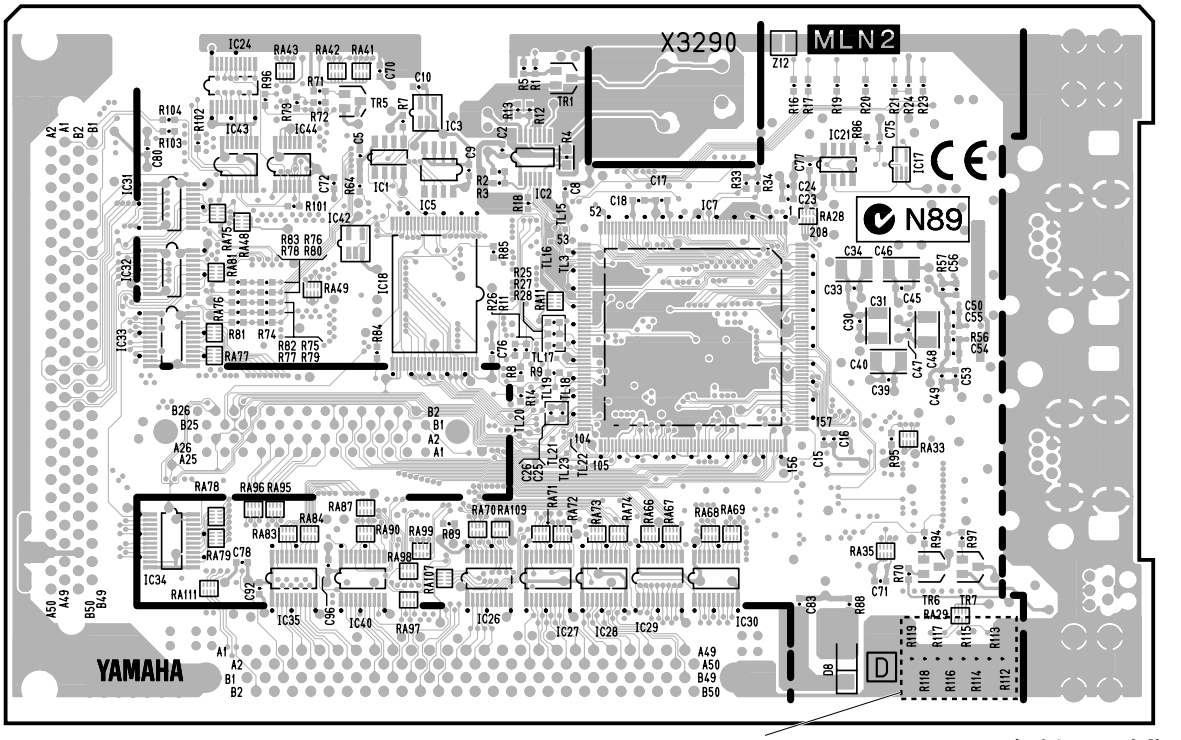
Model discrimination R113 install (mLAN16E)
（モデル識別:R113実装（mLAN16E））

Pattern side（パターン側）

• MLN2 Circuit Board (X3290D0)



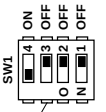
Component side（部品側）



Model discrimination R113 install (mLAN16E)
（モデル識別:R113実装（mLAN16E））

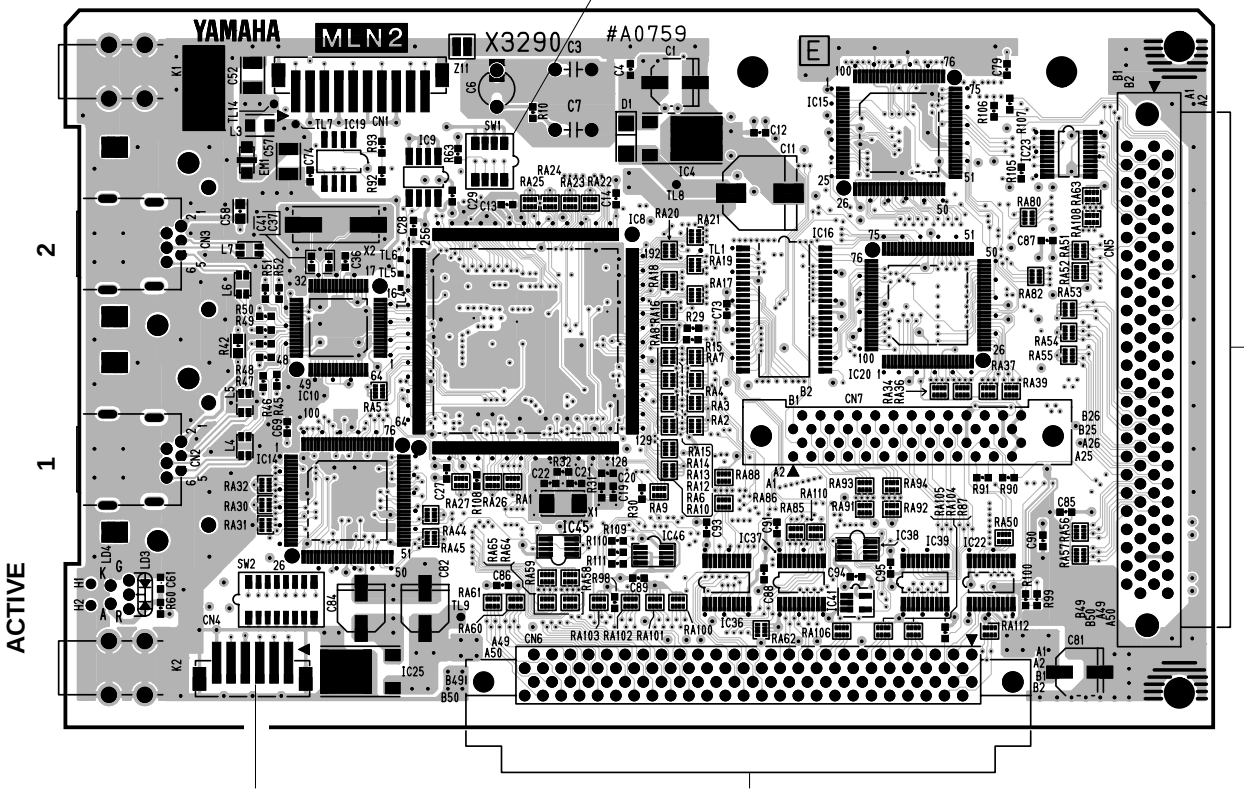
Pattern side（パターン側）

• MLN2 Circuit Board (X3290E0)



The setting of DIP switch (SW1)
DIPスイッチ（SW1）の設定

CN7: to SRC-CN1

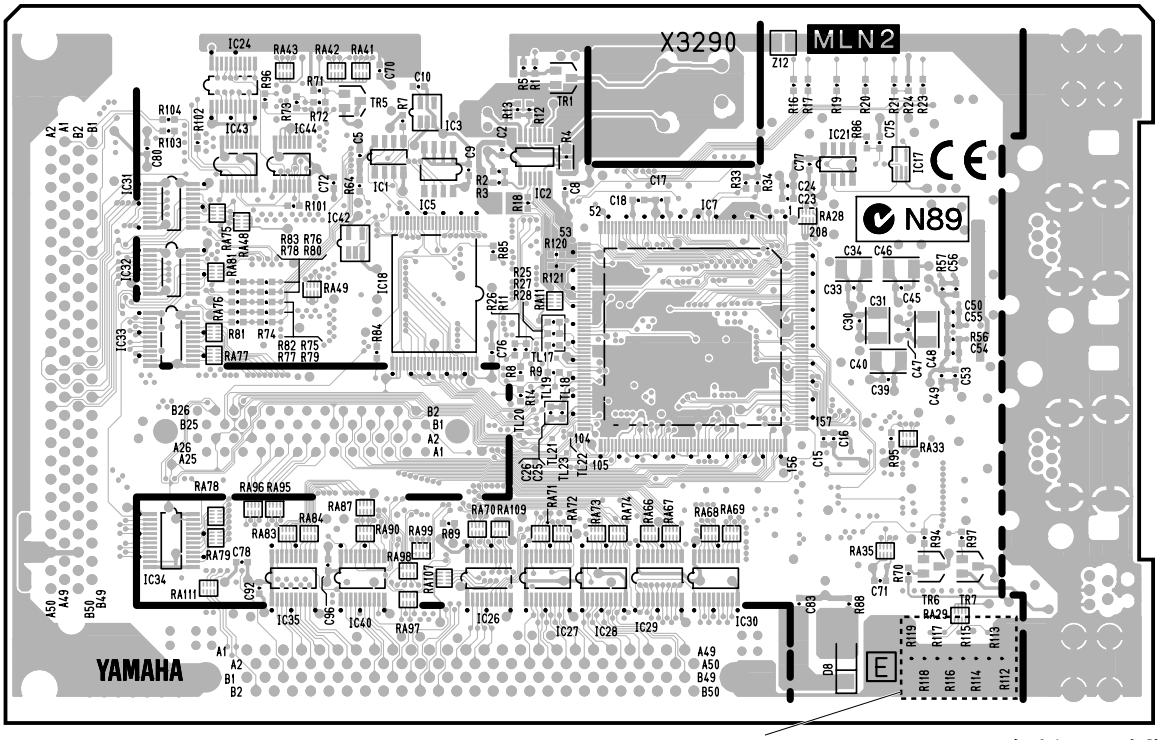


not used

mLAN I/F
(MOTIF ES 6/7/8: to DMSUB-CN8)

not used

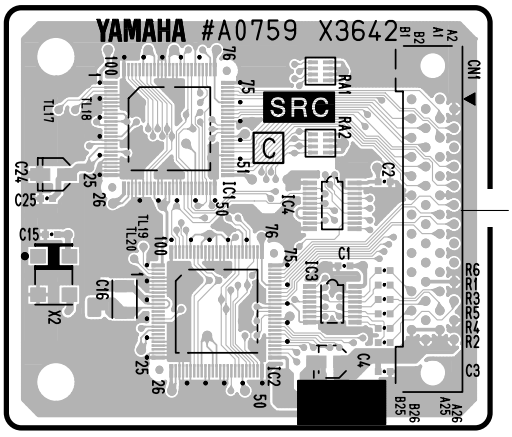
Component side（部品側）



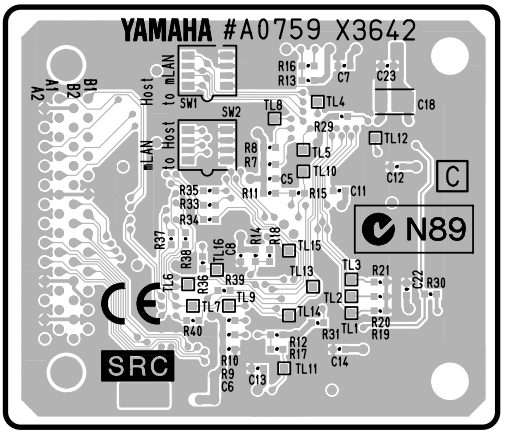
Model discrimination R113 install (mLAN16E)
（モデル識別:R113実装（mLAN16E））

Pattern side（パターン側）

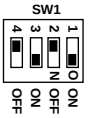
• SRC Circuit Board



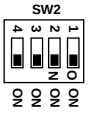
Component side（部品側）



Pattern side（パターン側）



The setting of DIP switch (SW1)
DIPスイッチ（SW1）の設定



The setting of DIP switch (SW2)
DIPスイッチ（SW2）の設定

Note: See parts list for details of circuit board component parts.
注：シートの部品詳細はパーツリストをご参照ください。

000-000000-0 ⚠1

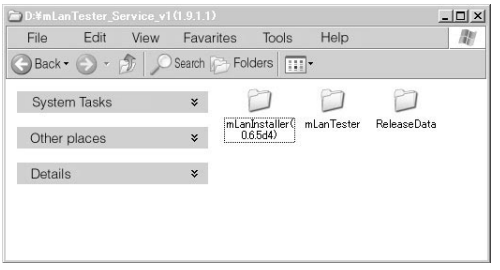
TEST PROGRAM

It is necessary to install Software *1 only for the mLAN inspection should install one (mLAN Tools 2.0 only for inspection) in PC before this isnpection is done.

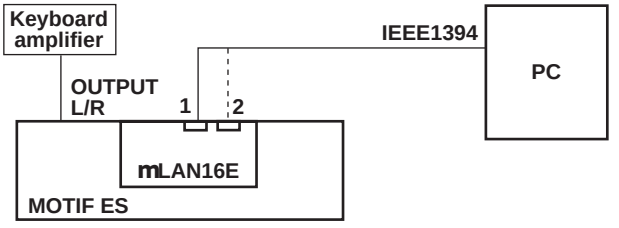
Equipment:

1) MOTIF ES (6, 7, or 8)
2) IEEE 1394 cable
3) Personal computer (PC)
   (DOS/V type with Windows XP Professional):
   - CPU clock: 2.2G or faster
   - System memory of 512MB or more.
   - Single Processor
   - OHCI compliant IEEE1394 terminal, or equivalent terminal in expansion slot card.
   - Recommended 800 x 600 dot display or higher resolution.
4) Key board amplifier (including connection cable) or headphone.

*1 Software only for the mLAN inspection
Please download it on the download page on the YSISS homepage. (YSISS URL>>http://plaza.yamaha.co.jp/YSISS/exindex.nsf)
The following folders are contained in the exclusive mLAN inspection software.



Connection Diagram:



* Both of the mLAN Terminals 1 and 2 should be tested.

Preparation:

A. Installing mLAN Tools 2.0 only for inspection

1) Turn off the power of MOTIF ES (with mLAN 16E).
2) Turn on the power of DOS/V PC to start-up Windows XP Professional.
3) Open "mLANInstaller" folder contained in the exclusive mLAN inspection software that has been downloaded, and execute in the following order: [mLANInstaller] → [mLANdrv] → setup

✻ **Double-clicking the "setup" program executes the installation of the mLAN Tools 2.0 only for inspection.**

B. Configuration of Windows XP

1) Deactivate antivirus software.
2) Deactivate the Windows automatic update function.
3) Choose "System" in Control Panel and then "Advanced", "Performance", and "Performance options". Then, select "Adjust for best performance" in "Visual effect".
4) Choose "System" in Control Panel and then "Advanced", "Performance", and "Advanced". Then, set the Processor scheduling at "Background services" in Performance Options.
5) Adjust settings to prevent screen saver activation, or to stop the power saving function of the monitor.

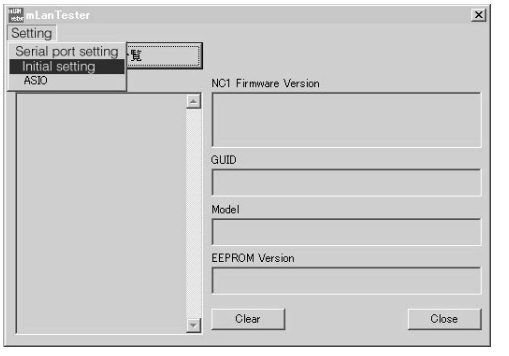
C. Preparing for Inspection

Connect DOS/V PC and MOTIF ES with IEEE 1394 cable, and turn on the power of MOTIF ES.
Double-click the "Start_mLanTester_for_Service.vbs" contained in the "mLan Tester" folder to display the inspection screen.

✻ **When mLAN MIDI IN or mLAN MIDI OUT driver install message appears, execute the installation procedure following the instruction in the window.**

D. Setting

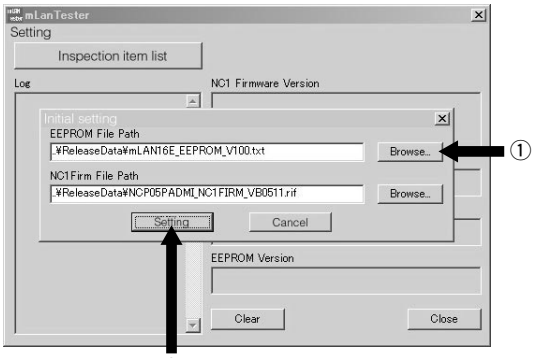
Click "Setting" on the screen, choose and click the "Initial Setting".

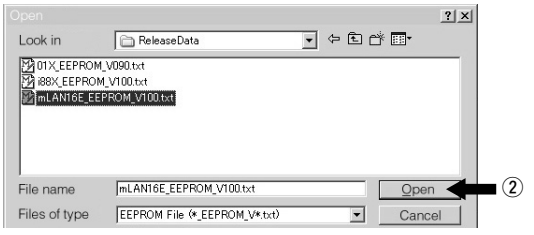


[Setting the EEPROM File Path]

- Click on the "Browse" button in the upper part of the screen(①). Open Release Data folder and select mLAN16E_EEPROM. Click on the "Open" button (②). Click on the "Setting" button (③).

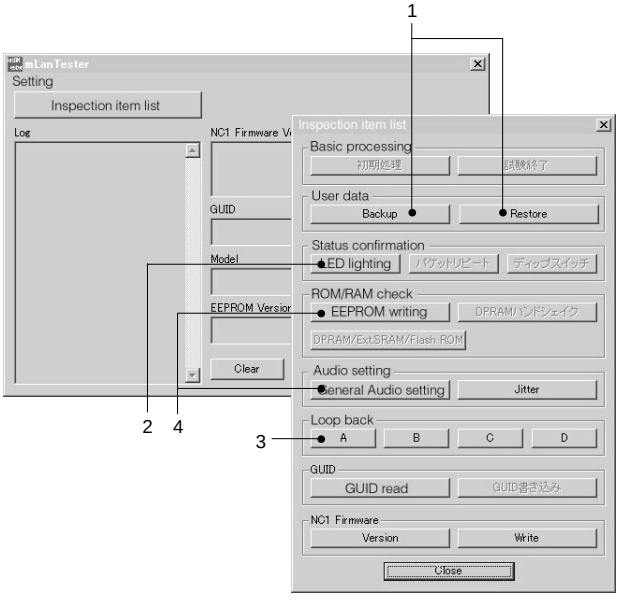
  * Usually, the setting for NCIFirm File Path is not required. (It is not necessary to write the NCI Firmware in normal condition)





Inspection:

Click on "Inspection Item List" button, and the inspection item list will appear.

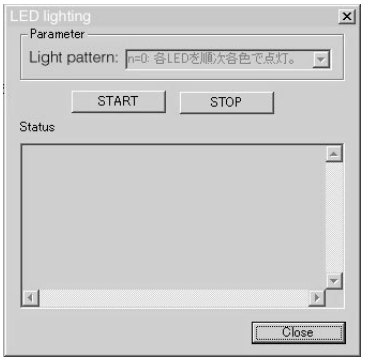


1. Backup/Restore

Click on "Backup" button to save internal data at an appropriate location on the PC. Once the inspection is completed, click on "Restore" button to put back the data from the saved location to the original place.

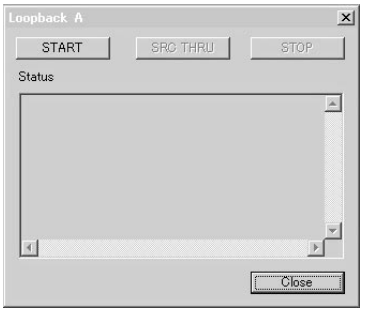
2. LED Lighting

Click on "LED lighting" button to open the LED lighting screen shown below. Click on "START" button on this screen. Check that "ACTIVE" light on mLAN16E blinks.



3. Loopback Setting

Click on Loopback "A" button ("A" is the button for mLAN16E) to open the Loopback A screen shown below. Click on "START" button on the screen to start the loopback mode. Inspection of mLAN16E should be performed in this loopback mode on MOTIF ES.



When error is displayed:

Error 1: mLAN device not found. Check the electrical connection.

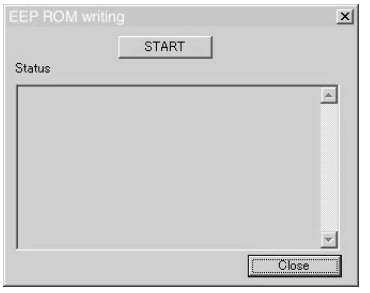
Error 2: Audio Loopback failed. Perform loopback setting again.

Error 3: MIDI Loopback failed. Perform loopback setting again.

4. Other

- EEPROM Writing

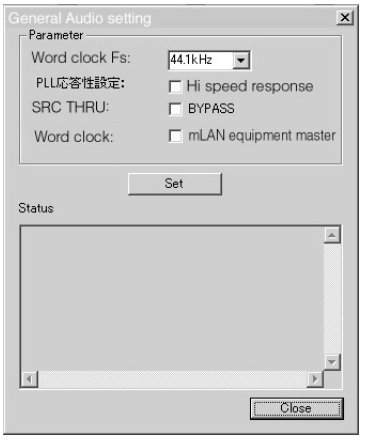
  Click on "EEPROM writing" button to open the EEPROM writing screen shown below. Click on "START" button to restore the initial setting (original data set at the factory). (Usually this operation is not required.)



- General Audio Setting

  Click on "General Audio Setting" button to open the setting screen, which allows the setting on the items shown below.

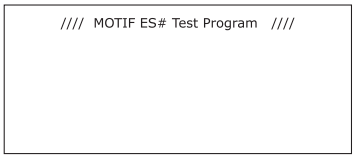
  Word clock Fs (44.1kHz / 48kHz), PLL response, SRC THRU, and Work clock master can be changed.



Testing Operation on MOTIF ES

A. Test Entry

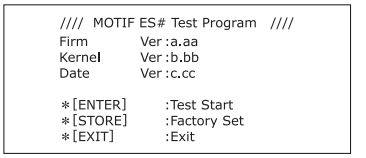
Following model name is displayed in the first line on the screen.



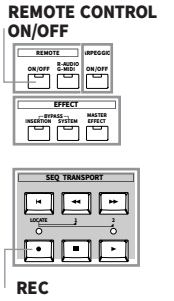
:MOTIF ES6 ... 6
:MOTIF ES7 ... 7
:MOTIF ES8 ... 8

(The same applies in the following description.)

Turn on the power while pressing the buttons [REMOTE CONTROL ON/OFF] + [REC] to display the screen shown below. Then, press [ENTER] button to enter into the test program.



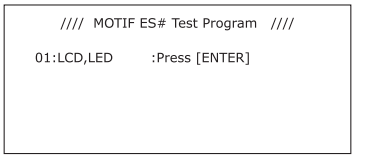
a.aa :Firm version
b.bb :Kernel version
c.cc :Data version

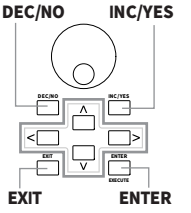


The "EXIT" screen appears if [EXIT] button is pressed while the screen shown above is displayed.

B. Testing Procedure

The following screen appears after you enter into the test program.





Choose "27 : mLAN" using the buttons [DEC/NO] and [INC/YES].

Press [ENTER] button to execute the test of the selected number ("27 : mLAN").

* Make sure that the Loopback setting is made on the PC.

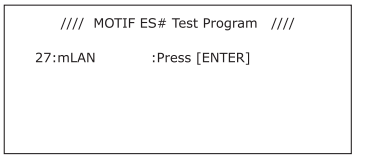
C. How to proceed the testing when "No Good" decision is made.

If "No Good" decision is made, press [EXIT] button to go back to the waiting state for selecting the test item.

D. mLAN Check

Choose "27 : mLAN".

(Initial Display)



(Testing Procedure)
Transmission of signals between mLAN16E and mLAN I/F inside of MOTIF ES is checked by this test.
Connect the external PC and mLAN16E using IEEE1394 cable. Exclusive inspection software should be launched on the PC prior to the connection. Then, send Audio/MIDI/ControlSerial signal from MOTIF ES, and make them Echo Back. Check the condition of Echo Back signals on MOTIF ES.
Send particular series of data via the two SIO4 in MOTIF ES, and check that identical series of data are received within the certain period of time.
Sound the SWP50 (Slave), Loopback the Audio data at mLAN16E, send them back via SWP50 (Slave) to SWP50 (Master), and then output to DAC.

1. Board Connection Test

Detect if mLAN16E is installed or not.

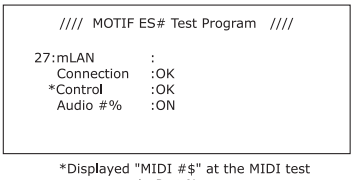
2. MIDI/ControlSerial Test

Verify the correct Echo Back by transferring the test pattern (90 40 7F) from the main unit to MIDI 4ch and ControlSerial 1ch.

1) MIDI #1: Echo Back test for MIDI port 1.
2) MIDI #2: Echo Back test for MIDI port 2.
3) MIDI #3: Echo Back test for MIDI port 3.
4) MIDI #4: Echo Back test for MIDI port 4.
5) Control: Echo Back test for ControlSerial

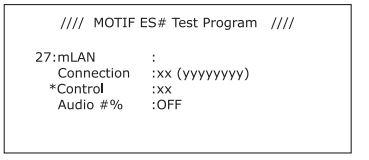
3. Audio Test

Eight lines of Audio input / output from MORIF ES is tested.
Specifically, send the sine wave from MOTIF ES into the eight Audio input / output lines in turn, and verify the proper EchoBack of the sine waves to each Audio input.
After the input of sine waves, the relevant signals are converted from digital to analog and sent to STEREO OUT for the output.
(Audio ch is switched at every 0.5 seconds approximately.)
(Testing procedure)
Check the EchoBack for MIDI/Serial.
Listen to the sound from Output L, R coming out of the speaker.
(No sound is produced from Rch)



*Displayed "MIDI #$" at the MIDI test
$:Port No.
% :Audio No.

(Check Items)
Items 1) and 2) are auto-detected by the main body. Check the test results shown on the LCD.
If the test is failed, the error factors are shown on the display.
For the item 3), confirm that the sine waves produce sound by means of audibility.
(Intermittent sound is produced)
(Display of detection results)
OK : No message appears on the screen.
NG : (Error factor : No Board)



xx :OK/NG notation
*Each of connection/MIDI #$/control

(How to terminate the test)
Press [EXIT] to terminate the sound. The screen is changed to the waiting state for selecting the test item.

■ テストプログラム

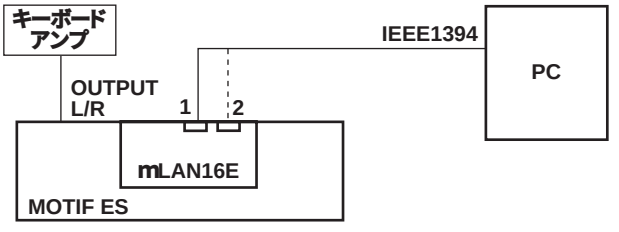
この検査を行なう前に、PCへmLAN検査専用ソフト*1（検査専用mLAN Tools 2.0）をインストールする必要があります。

準備するもの

1) MOTIF ES （6/7/8 のいずれか）
2) IEEE1394 ケーブル
3) PC
（WindowsXP Professionalをインストールした DOS/V タイプ）
・CPU クロック：2.2G 以上の CPU 搭載
・512MB 以上のシステムメモリー
・Single Processor
・OHCI 準拠 IEEE1394 端子を装備、または拡張スロットカードにて同等の端子を装備
・ディスプレイは 800 x 600 dot 以上を推奨
4) キーボードアンプ（接続ケーブルを含む）またはヘッドホーン

*1 mLAN 検査専用ソフト
CSセンターホームページのダウンロードページからダウンロードしてください。
mLAN 検査専用ソフトの中には、下記のホルダーが入っています。

接続



* mLAN 端子 1, 2 どちらも検査してください。

準備

A. 検査専用 mLAN Tools 2.0 のインストール

1) MOTIF ES（mLAN16E搭載）の電源をOFFにします。
2) DOS/V パソコンの電源を ON にし、Windows XP Professional を立ち上げます。
3) ダウンロードした mLAN 検査専用ソフトの mLanInstaller ホルダーを選び、下記の通り実行します。[mLANInstaller]→[mLANdrv]→ setup
※ setup をダブルクリックすれば検査専用 mLAN Tools 2.0 がインストールされます。

B. Windows XP の設定

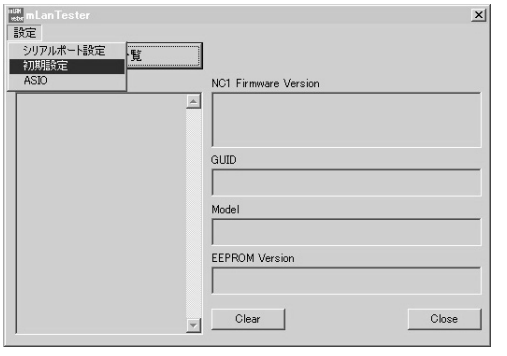
1) ウィルス検出ソフトは起動しないようにしておきます。
2) Windows の自動更新をしないようにしておきます。
3) コントロールパネルのシステム→詳細設定→パフォーマンス→パフォーマンスオプション設定の視覚効果を「パフォーマンスを優先にする」にします。
4) コントロールパネルのシステム→詳細設定→パフォーマンス→パフォーマンスオプション設定にある詳細設定のプロセッサのスケジュールを「バックグラウンドサービス」に設定します。
5) Sleep しないように、スクリーンセーバーが起動しないようにしたり、モニターの省電源機能が働かないようにしておきます。

C. 検査準備

DOS/V パソコンと MOTIF ES を IEEE1394 ケーブルで接続し、MOTIF ES の電源を ON にします。
mLan Tester ホルダー内の "Start_mLanTester_for_Service.vbs" をダブルクリックして検査ツール（mLAN Tester）を立ち上げます。
※ mLAN MIDI IN, mLAN MIDI OUT ドライバーインストールのメッセージが表示される場合は、画面の指示に従って実行してください。

D. 設定

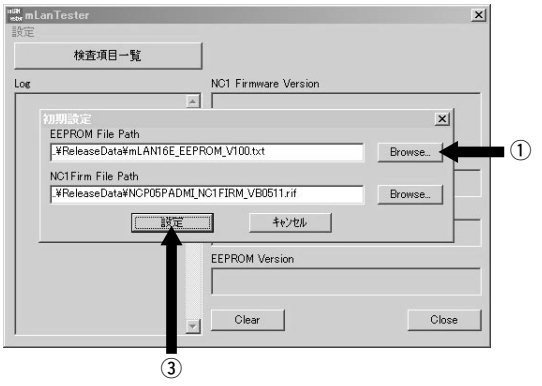
画面の "設定" をクリックし "初期設定" を選択し、クリックします。

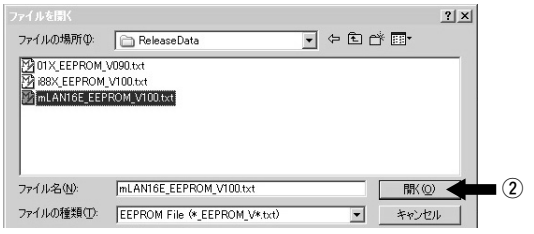


[EEPROM File Path を設定します。]

- **上側の Browse ボタンをクリックして（①）ReleaseData ホルダー内の mLAN16E_EEPROM を選択し、"開く" ボタンをクリックします。（②）その後 "設定" ボタンをクリックします。（③）**

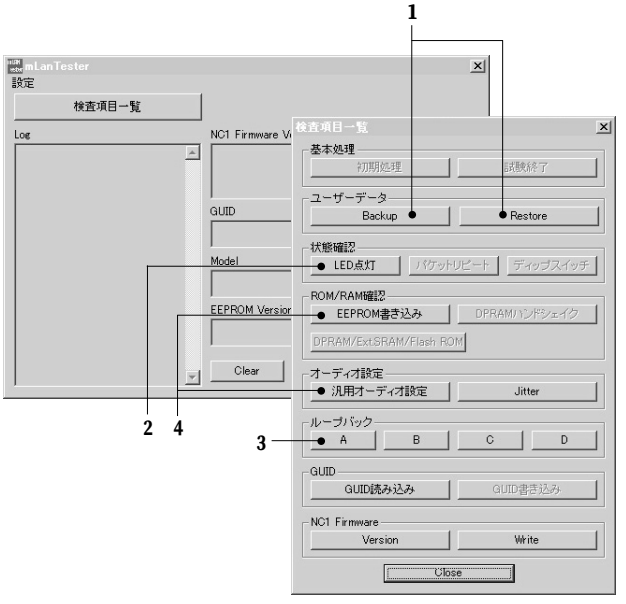
*** NC1Firm File Path の設定は、通常は必要ありません。（通常は NC1 Firmware の書き込みは行ないません。）**





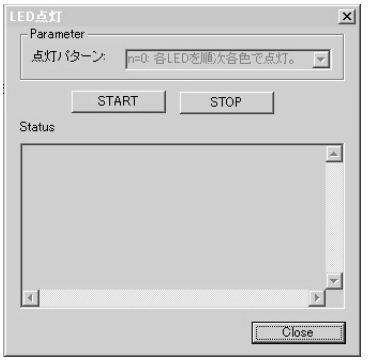
検査

"検査項目一覧" ボタンをクリックすれば、検査項目一覧が表示されます。

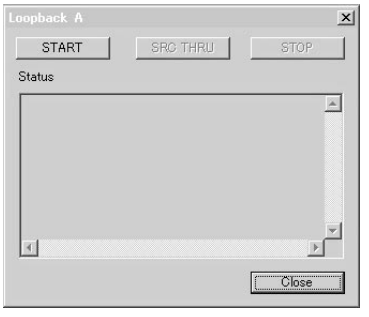


1. **Backup/Restore**
   "Backup" ボタンをクリックして、PC 内の適当な場所に内部のデータを保存します。すべての検査終了後、"Restore" ボタンをクリックして保存した場所からデータを元にもどします。

2. **LED 点灯**
   "LED 点灯" ボタンをクリックして、次の LED 点灯画面で "ＳＴＡＲＴ" ボタンをクリックします。その時、mLAN16E の ACTIVE が点滅することを確認します。



3. **ループバックの設定**
   ループバック "A" ボタンを押します。("A" は mLAN16E 用のボタンです。）次の Loopback A 画面で "START" ボタンをクリックすればループバックの状態となります。この状態の時に MOTIF ES 側で mLAN16E の検査を行ないます。



エラー表示が出た場合

エラー 1：mLAN 機器が見つかりません。接続を確認してください。

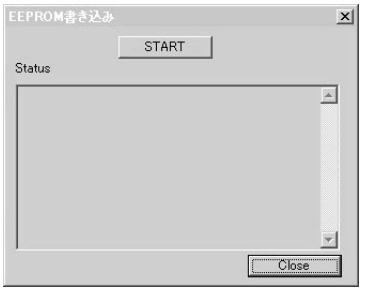
エラー 2：Audio Loopback に失敗しました。再度ループバック設定を行なってください。

エラー 3：MIDI Loopback に失敗しました。再度ループバック設定を行なってください。

4. その他

・EEPROM 書き込み

EEPROM 書き込みボタンをクリックし、次の EEPROM 書き込み画面で "START" ボタンをクリックすれば、初期設定（工場出荷のデータ）されます。（通常この検査は必要ありません。）



・汎用オーディオ設定

"汎用オーディオ設定" ボタンをクリックして、設定画面から下記の項目の設定が可能です。

ワードクロック周波数（44.1kHz/48kHz）、PLL 応答性、SRC の THRU、ワードクロックマスター切替等を変更することが出来ます。

MOTIF ES 側での操作

A. テストエントリー

画面表示の先頭に表示されるモデル名は下記になります。

```
//// MOTIF ES# Test Program ////
```

:MOTIF ES6 ... 6
:MOTIF ES7 ... 7
:MOTIF ES8 ... 8

（以下同様とします。）

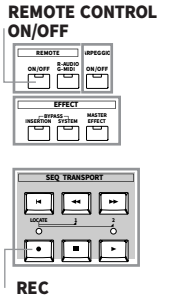
[REMOTE CONTROL ON/OFF] + [REC]のスイッチを押しながら電源オンすると、次の画面が表示されます。

[ENTER]ボタンを押すと、テストプログラムに入ります。

```
//// MOTIF ES# Test Program ////
Firm        Ver :a.aa
Kernel      Ver :b.bb
Date        Ver :c.cc

*[ENTER]    :Test Start
*[STORE]    :Factory Set
*[EXIT]     :Exit
```

a.aa :Firm version
b.bb :Kernel version
c.cc :Data version

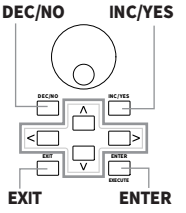


この画面の状態で、[EXIT]を押すと、"EXIT" 画面が表示されます。

B. テストの進め方

テストにエントリーすると、次の画面が表示されます。

```
//// MOTIF ES# Test Program ////
01:LCD,LED      :Press [ENTER]
```



[DEC/NO]、[INC/YES]を使用して "27 : mLAN" を選択します。

[ENTER]を押すと、現在選択されているテストナンバー（"27 : mLAN"）が実行されます。

* PC 側はループバック設定が必要です。

C. NG と判断した時のテストの進め方

NG と判断した場合は[EXIT]ボタンを押すと、テスト項目選択待ち状態になります。

D. mLAN チェック

27 : mLAN を選択します。

（最初の表示）

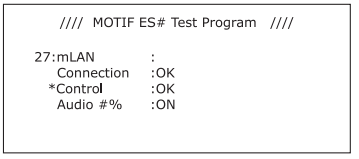
```
//// MOTIF ES# Test Program ////
27:mLAN         :Press [ENTER]
```

（テスト内容）
mLAN16E と MOTIF ES 内 mLAN I/F 間との信号のやり取りをテストします。
外部に専用アプリケーションを起動させた PC と 1394 ケーブルにて mLAN16E を接続し、MOTIF ES 側より送信した Audio/MIDI/ControlSerial 信号を EchoBack させ、MOTIF ES 側でその状況を確認します。
MOTIF ES 内にある SIO4(2 個)経由特定のデータ群を送信し、一定時間内に同一のデータ群が受信されることを確認します。
SWP50（Slave側）を発音させmLAN16E側にてLoopbackしたAudioデータをSWP50（Slave 側）-SWP50（Master 側）と経由させ DAC に出力します。

1. ボード接続テスト
   mLAN16E の有無を検出します。

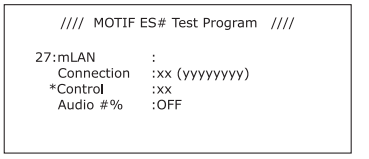
2. MIDI/ControlSerial テスト
   本体より MIDI 4ch 、ControlSerial 1ch にテストパターン（90 40 7F）を転送し、正しく EchoBack されるかどうかを確認します。
   1）MIDI #1 : MIDI port 1 の Echo Back 試験
   2）MIDI #2 : MIDI port 2 の Echo Back 試験
   3）MIDI #3 : MIDI port 3 の Echo Back 試験
   4）MIDI #4 : MIDI port 4 の Echo Back 試験
   5）Control : ControlSerial の Echo Back 試験

3. Audio テスト
MOTIF ESからAudio入出力8系統のテストをします。
具体的には、MOTIF ES より Audio 出力 8 系統に対して順次、正弦波を出力し、それを各 Audio 入力へ Echo Back される事を確認します。
入力された正弦波は、信号を DA 変換して、STEREO OUT へ出力します。
（audio ch は、約 0.5 秒毎に切り替わります）
（テスト方法）
MIDI/Serial の Echo Back 結果を確認します。
OutputL,R からの音をスピーカーで聞きます。
（Rch 側は発音しません）



*Displayed "MIDI #$" at the MIDI test
$:Port No.
% :Audio No.

（チェック項目）
1）2）は本体が自動判定するため、LCD のテスト結果を確認します。
NG 時、その要因を表示します。
3）は聴感にて正弦波が発音されることを確認します。
（断続音が発音されます。）
（判定結果の表示）
OK 表示なし
NG（Error 要因 : No Board）



xx :OK/NG notation
*Each of connection/MIDI #$/control

（テストの終了方法）
[EXIT] を押すと、発音は終了し、項目選択状態になります。

mLAN EXPANSION BOARD

mLAN16E

PARTS LIST

■ CONTENTS（目次）

Notes : DESTINATION ABBREVIATIONS

A : Australian model	M : South African model
B : British model	O : Chinese model
C : Canadian model	Q : South-east Asia model
D : German model	T : Taiwan model
E : European model	U : U.S.A. model
F : French model	V : General export model (110V)
H : North European model	W: General export model (220V)
I : Indonesian model	N,X: General export model
J : Japanese model	Y : Export model
K : Korean model	

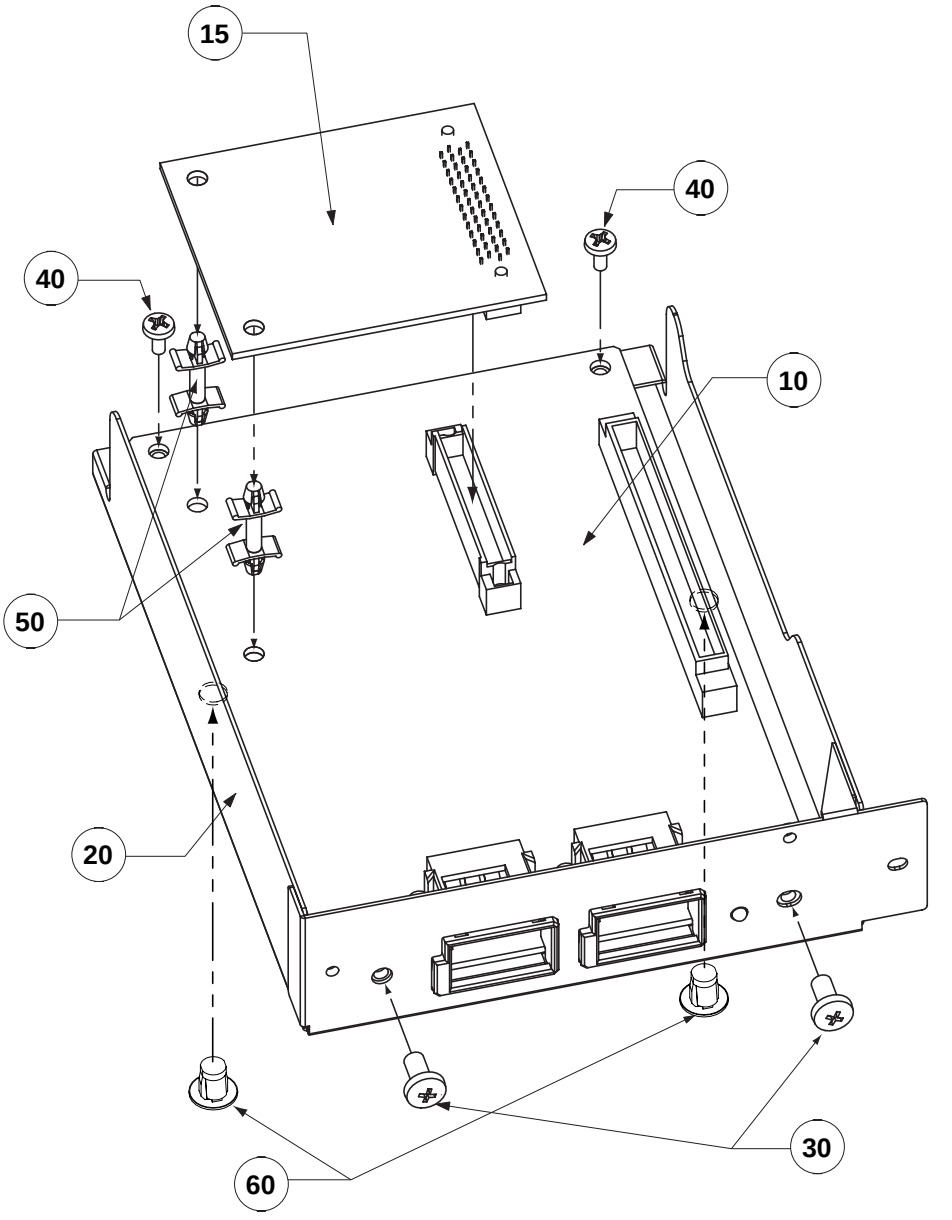
■ WARNING

Components having special characteristics are marked ⚠ and must be replaced with parts having specification equal to those originally installed.

⚠ 印の部品は、安全を維持するために重要な部品です。交換する場合は、安全のために必ず指定の部品をご使用ください。

- The numbers “QTY” show quantities for each unit.
- The parts with “--” in “PART NO.” are not available as spare parts.
- This mark “ } ” in the REMARKS column means these parts are interchangeable.
- The second letter of the shaded ( ) part number is O, not zero.
- The second letter of the shaded ( ) part number is I, not one.
- **部品価格ランクは、変更になることがあります。**
- **QTY欄に記されている数字は、各ユニット当たりの使用個数です。**
- **PART NO.が “ -- ” の部品は、サービス用部品として準備されておりません。**
- **REMARKS欄の「 } 」マークの部品は、併用部品です。**
- **網掛けの付いたPART NO. の2番目の文字は「ゼロ」ではなく、「オー」です。**
- **網掛けの付いたPART NO. の2番目の文字は「イチ」ではなく、「アイ」です。**

■ OVERALL ASSEMBLY（総組立）



	REF NO.	PART NO.	DESCRIPTION		部品名	REMARKS	QTY	RANK
			OVERALL ASSEMBLY		総組立	mLAN16E		
		--	Overall Assembly		総組立	J, W, O (WA46900)		
*	10	**WA979200**	Circuit Board	MLN2	ＭＬＮ２シート			
*	15	**WA979500**	Circuit Board	SRC	ＳＲＣシート			
*	20	**WA469200**	Angle	16E	アングル１６Ｅ印刷品			09
	30	**V6655200**	Bind Head Tapping Screw-S	4.0X8 MFZN2BL	＋バインドＳタイト		2	
	40	**VZ544100**	Bind Head Tapping Screw-B	3.0X6 MFNI33	＋バインドＢタイト		2	01
*	50	**V9121500**	Support, PCB	WLS-14-0	ダブルロッキングスペーサ		2	01
	60	**V3638800**	Spacer	KGPS-6RF	カードスペーサー			01
			ACCESSORIES		付属品			
*		**WD045200**	Connector Assembly	mLAN16E	線材Ａｓｓ’ｙ			
*		**X4149B00**	Optical Disk	Tool for mLAN16E	光ディスク			

*: New Parts

RANK: Japan only

■ ELECTRICAL PARTS（電気部品）

	REF NO.	PART NO.	DESCRIPTION		部品名	REMARKS	QTY	RANK
			ELECTRICAL PARTS		電気部品	mLAN16E		
*		**WA979200**	Circuit Board	MLN2	ＭＬＮ２シート	(X3290C0/D0/E0)		
*		**WA979500**	Circuit Board	SRC	ＳＲＣシート	(WB10130)(X3642C0)		
*		**WA979200**	Circuit Board	MLN2	ＭＬＮ２シート	(X3290C0/D0/E0)		
*	10	**V6708900**	Escutcheon	1394 B	１３９４エスカッションＢ		2	02
	20	**V4880400**	Label	FOR IEEE1394	ＧＵＩＤバーコードラベル			02
	30	**V4450100**	LED Spacer	LM	ＬＥＤスペーサー縦２連			04
	40	**V6700600**	Contact	UPPER	接触子（上）		2	03
	50	**V6700700**	Contact	LOWER	接触子（下）		2	02
	60	**VG893800**	Bind Head Tapping Screw-P	2.0X6 MFZN2BL	＋バインドＰタイト		4	01
*	70	**WB869600**	LED Support Assembly	LM #A0733	ＬＥＤサポートＡｓｓ'ｙ			02
	C0001	**UF038100**	Electrolytic Cap. (chip)	100 16V	チップケミコン			01
	C0002	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0003	**VE326600**	Monolithic Mylar Capacitor	0.33 50V J	積層マイラーコン			01
	C0004	**US035100**	Ceramic Capacitor-B (chip)	0.1000 16V K	チップセラ（Ｂ）			01
	C0005	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0006	**VR575400**	Electrolytic Cap.	10.00 16.0V	ケミコン　低漏れ電流形			01
	C0007	**VE326400**	Monolithic Mylar Capacitor	0.22 50V J	積層マイラーコン			01
	C0008	**US035100**	Ceramic Capacitor-B (chip)	0.1000 16V K	チップセラ（Ｂ）			01
	C0010	**US035100**	Ceramic Capacitor-B (chip)	0.1000 16V K	チップセラ（Ｂ）			01
	C0011	**UF138470**	Electrolytic Cap. (chip)	470 16V UUR1C4	チップケミコン			02
	C0012	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	-0014	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0015	**US062220**	Ceramic Capacitor-SL(chip)	220P 50V J	チップセラ（ＳＬ）			01
	C0016	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0017	**US062220**	Ceramic Capacitor-SL(chip)	220P 50V J	チップセラ（ＳＬ）			01
	C0018	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0019	**US062100**	Ceramic Capacitor-SL(chip)	100P 50V J	チップセラ（ＳＬ）			01
	C0020	**US061100**	Ceramic Capacitor-CH(chip)	10P 50V D	チップセラ（ＣＨ）			01
	-0022	**US061100**	Ceramic Capacitor-CH(chip)	10P 50V D	チップセラ（ＣＨ）			01
	C0023	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0024	**US062220**	Ceramic Capacitor-SL(chip)	220P 50V J	チップセラ（ＳＬ）			01
	C0025	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0026	**US062220**	Ceramic Capacitor-SL(chip)	220P 50V J	チップセラ（ＳＬ）			01
	C0027	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	-0030	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
*	C0031	**V9980700**	Monolithic Ceramic Cap.	22.000 6.3V K 3225	チップ積層セラコン			02
	C0033	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
*	C0034	**V9980700**	Monolithic Ceramic Cap.	22.000 6.3V K 3225	チップ積層セラコン			02
	C0036	**US135100**	Ceramic Capacitor-F (chip)	0.1000 16V Z	チップセラ（Ｆ）			01
	C0037	**US060600**	Ceramic Capacitor-CH(chip)	6P 50V D	チップセラ（ＣＨ）			
	C0039	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
*	C0040	**V9980700**	Monolithic Ceramic Cap.	22.000 6.3V K 3225	チップ積層セラコン			02
	C0041	**US060600**	Ceramic Capacitor-CH(chip)	6P 50V D	チップセラ（ＣＨ）			
	C0045	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
*	C0046	**V9980700**	Monolithic Ceramic Cap.	22.000 6.3V K 3225	チップ積層セラコン			02
	C0047	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
*	C0048	**V9980700**	Monolithic Ceramic Cap.	22.000 6.3V K 3225	チップ積層セラコン			02
	C0049	**US135330**	Ceramic Capacitor-F (chip)	0.3300 16V Z	チップセラ（Ｆ）			01
	C0050	**US135330**	Ceramic Capacitor-F (chip)	0.3300 16V Z	チップセラ（Ｆ）			01
*	C0052	**V9980700**	Monolithic Ceramic Cap.	22.000 6.3V K 3225	チップ積層セラコン			02
	C0053	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0054	**US062270**	Ceramic Capacitor-SL(chip)	270P 50V J	チップセラ（ＳＬ）			01
	C0055	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0056	**US062270**	Ceramic Capacitor-SL(chip)	270P 50V J	チップセラ（ＳＬ）			01
*	C0057	**V9980700**	Monolithic Ceramic Cap.	22.000 6.3V K 3225	チップ積層セラコン			02
	C0058	**UB044100**	Monolithic Ceramic Cap.	F 0.010 50V Z	チップ積層セラコン			01
	C0061	**US135100**	Ceramic Capacitor-F (chip)	0.1000 16V Z	チップセラ（Ｆ）			01
	C0069	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0071	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0074	**US135330**	Ceramic Capacitor-F (chip)	0.3300 16V Z	チップセラ（Ｆ）			01
	C0075	**US135330**	Ceramic Capacitor-F (chip)	0.3300 16V Z	チップセラ（Ｆ）			01
	C0077	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0078	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0081	**UF038100**	Electrolytic Cap. (chip)	100 16V	チップケミコン			01
	C0088	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	C0091	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	-0096	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（Ｂ）			01
	CN002	**VZ562700**	Connector	IEEE1394 6P SE	コネクタ	1		03

※: New Parts

RANK: Japan only

	REF NO.	PART NO.	DESCRIPTION		部品名	REMARKS	QTY	RANK
	CN003	**VZ562700**	Connector	IEEE1394 6P SE	コネクタ	2		03
	CN006	**WB086600**	Header	8830E 100P TE	ヘッダー			05
*	CN007	**WA037000**	Connector Plug	8800 52P TE	コネクタープラグ			05
	D0001	**VS597600**	Diode	RB160L-40 TE25	ダイオード			01
	IC001	**XR336A00**	IC	TC7W14F TE12L	IC	INVERTER		02
	IC002	**XV064A00**	IC	TLC2932IPWR	IC	PLL		06
	IC003	**XY568A00**	IC	RN5VD30CA-TR	IC	REGULATOR +3V		02
	IC004	**XS516A00**	IC	UPC2933T-E1	IC	REGULATOR +3.3V		03
*	IC007	**X3009B00**	IC	YTS440B-FZ	IC	mLAN-PH2		16
*	IC008	**X2150A00**	IC	mLAN-NC1	IC	Link controller		20
*	IC009	**X3484A00**	IC	24LC16BT-I/SN	IC	EEPROM 16K		03
*	IC010	**XZ762A00**	IC	MD8408B	IC	PHY		08
*	IC014	**X3628D00**	IC	XCR3064XL-10	IC	CPLD		
	IC017	**XR680A00**	IC	TC7SH08FU	IC	AND		
*	IC019	**X4182A00**	IC	M51957AFP	IC	SYSTEM RESET		01
	IC021	**XR336A00**	IC	TC7W14F TE12L	IC	INVERTER		02
	IC022	**XW148A00**	IC	HD74LVC245ATELL	IC	TRANSCEIVER		02
	IC022	**XZ287A00**	IC	SN74LVC245APWR	IC			02
	IC026	**XW148A00**	IC	HD74LVC245ATELL	IC	TRANSCEIVER		02
	IC026	**XZ287A00**	IC	SN74LVC245APWR	IC			02
	IC035	**XW148A00**	IC	HD74LVC245ATELL	IC	TRANSCEIVER		02
	IC035	**XZ287A00**	IC	SN74LVC245APWR	IC			02
*	IC036	**X2308A00**	IC	HD74LVC244ATELL	IC	BUFFER		03
	IC037	**XW148A00**	IC	HD74LVC245ATELL	IC	TRANSCEIVER		02
	IC037	**XZ287A00**	IC	SN74LVC245APWR	IC			02
	IC038	**XQ173A00**	IC	TC7W32FU(TE12L)	IC	OR		01
	IC039	**XW148A00**	IC	HD74LVC245ATELL	IC	TRANSCEIVER		02
	IC039	**XZ287A00**	IC	SN74LVC245APWR	IC			02
*	IC040	**X2308A00**	IC	HD74LVC244ATELL	IC	BUFFER		03
	IC041	**XM182A00**	IC	TC7S04F	IC	INVERTER		01
	IC044	**X0199A00**	IC	TC74VHC157FT	IC	MULTIPLEXER		01
	IC045	**XQ173A00**	IC	TC7W32FU(TE12L)	IC	OR		01
	K0001	**VI474400**	Terminal Plate		ターミナル金具			01
	K0002	**VI474400**	Terminal Plate		ターミナル金具			01
*	L0003	**V9980400**	Chip Inductance	10U NLFC252018T10	チップインダクタ			01
*	L0004	**WA626200**	Chip Choke Coil	DLW31SN161SQ2L	チップチョークコイル			03
*	-0007	**WA626200**	Chip Choke Coil	DLW31SN161SQ2L	チップチョークコイル			03
	LD004	**V4133400**	LED Blue	SELU2E10C	LED	ACTIVE		04
	R0001	**RD356330**	Carbon Resistor (chip)	3.3K 63M J	チップ抵抗			01
	R0003	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	R0004	**VI194900**	Metal Film Resistor (chip)	1.0K 1/10 D	チップ金被抵抗			01
	R0005	**RD358100**	Carbon Resistor (chip)	100.0K 63M J	チップ抵抗			01
	R0007	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
	R0010	**RF355100**	Carbon Resistor (chip)	100.0 D 1608	チップ抵抗			01
	R0013	**RF356270**	Carbon Resistor (chip)	2.7K D 1608	チップ抵抗			01
	R0016	**RD354330**	Carbon Resistor (chip)	33.0 63M J	チップ抵抗			01
	R0017	**RD354330**	Carbon Resistor (chip)	33.0 63M J	チップ抵抗			01
	R0018	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	R0019	**RD354330**	Carbon Resistor (chip)	33.0 63M J	チップ抵抗			01
	-0021	**RD354330**	Carbon Resistor (chip)	33.0 63M J	チップ抵抗			01
	R0023	**RD354330**	Carbon Resistor (chip)	33.0 63M J	チップ抵抗			01
	R0024	**RD356470**	Carbon Resistor (chip)	4.7K 63M J	チップ抵抗			01
	R0026	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	-0028	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	R0029	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
	R0030	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
	R0031	**RD356470**	Carbon Resistor (chip)	4.7K 63M J	チップ抵抗			01
	R0032	**RD359100**	Carbon Resistor (chip)	1.0M 63M J	チップ抵抗			01
	R0033	**RD355510**	Carbon Resistor (chip)	510.0 63M J	チップ抵抗			01
	R0034	**RD355510**	Carbon Resistor (chip)	510.0 63M J	チップ抵抗			01
	R0042	**VK581700**	Metal Film Resistor (chip)	200.0K 1/10 D	チップ金被抵抗			01
	R0045	**RF354560**	Carbon Resistor (chip)	56.0 D 1608	チップ抵抗			01
	-0052	**RF354560**	Carbon Resistor (chip)	56.0 D 1608	チップ抵抗			01
	R0056	**VZ750900**	Carbon Resistor (chip)	5.1K 1608	チップ抵抗			01
	R0057	**VZ750900**	Carbon Resistor (chip)	5.1K 1608	チップ抵抗			01
	R0060	**RD355470**	Carbon Resistor (chip)	470.0 63M J	チップ抵抗			01
	R0063	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
	R0086	**RD355100**	Carbon Resistor (chip)	100.0 63M J	チップ抵抗			01
	R0089	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
	R0092	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01

*: New Parts

RANK: Japan only

	REF NO.	PART NO.	DESCRIPTION		部品名	REMARKS	QTY	RANK
	R0093	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
	R0096	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	R0097	**RD356270**	Carbon Resistor (chip)	2.7K 63M J	チップ抵抗			01
	R0100	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	R0108	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	-0110	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	R0113	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	R0120	**RF354100**	Carbon Resistor (chip)	10.0 D 1608	チップ抵抗			01
	R0121	**RF354100**	Carbon Resistor (chip)	10.0 D 1608	チップ抵抗			01
*	RA001	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	-011	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA012	**WA512000**	Chip Resistor Array	CN1E4KTTD101J	チップ抵抗アレイ			01
*	-021	**WA512000**	Chip Resistor Array	CN1E4KTTD101J	チップ抵抗アレイ			01
*	RA022	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	-027	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA028	**WA516000**	Chip Resistor Array	CN1E4KTTD472J	チップ抵抗アレイ			01
*	RA029	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	-035	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA044	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA045	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA050	**WA511200**	Chip Resistor Array	CN1E4KTTD470J	チップ抵抗アレイ			01
*	RA062	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA070	**WA511200**	Chip Resistor Array	CN1E4KTTD470J	チップ抵抗アレイ			01
*	RA083	**WA511200**	Chip Resistor Array	CN1E4KTTD470J	チップ抵抗アレイ			01
*	RA084	**WA511200**	Chip Resistor Array	CN1E4KTTD470J	チップ抵抗アレイ			01
*	RA086	**WA511200**	Chip Resistor Array	CN1E4KTTD470J	チップ抵抗アレイ			01
*	RA087	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA088	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA090	**WA511200**	Chip Resistor Array	CN1E4KTTD470J	チップ抵抗アレイ			01
*	RA091	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA092	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA098	**WA509500**	Chip Resistor Array	CN1E4KTTD000J	チップ抵抗アレイ			01
*	RA099	**WA511200**	Chip Resistor Array	CN1E4KTTD470J	チップ抵抗アレイ			01
*	RA104	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	-107	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA109	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
*	RA110	**WA516800**	Chip Resistor Array	CN1E4KTTD103J	チップ抵抗アレイ			01
	RA112	**WA509500**	Chip Resistor Array	CN1E4KTTD000J	チップ抵抗アレイ			01
	SW001	**V6771900**	Jumper Wire	CHS-04 TA1	ジャンパー SW			03
	TR001	**VJ927100**	Transistor	2SC2712 Y	トランジスタ			01
	TR007	**VJ927100**	Transistor	2SC2712 Y	トランジスタ			01
*	X0001	**V9995800**	Quartz Crystal Unit	20M Q22FA365000710	水晶振動子			03
*	X0002	**V9885200**	Quartz Crystal Unit	24.576MHz AT-51CD2	水晶振動子			02
*		**WA979500**	Circuit Board	SRC	SRC シート	(WB10130)(X3642C0)		
	C0001	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（B）			01
	-0003	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（B）			01
	C0004	**UF037100**	Electrolytic Cap. (chip)	10 16V	チップケミコン			01
	C0005	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（B）			01
	-0008	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（B）			01
	C0011	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（B）			01
	-0015	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（B）			01
*	C0016	**V9980700**	Monolithic Ceramic Cap.	22.000 6.3V K 3225	チップ積層セラコン			02
*	C0018	**V9980700**	Monolithic Ceramic Cap.	22.000 6.3V K 3225	チップ積層セラコン			02
	C0022	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（B）			01
	C0023	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（B）			01
	C0024	**UF037100**	Electrolytic Cap. (chip)	10 16V	チップケミコン			01
	C0025	**US064100**	Ceramic Capacitor-B (chip)	0.0100 50V K	チップセラ（B）			01
*	CN001	**WA036900**	Connector Receptacle	8800 52P TE	コネクターレセプタクル			05
*	IC001	**X4072A00**	IC	S1L54423F21B000	IC	SRC16		09
*	IC002	**X4072A00**	IC	S1L54423F21B000	IC	SRC16		09
	IC003	**X0199A00**	IC	TC74VHC157FT	IC	MULTIPLEXER		01
*	IC004	**X2308A00**	IC	HD74LVC244ATELL	IC	BUFFER		03
	R0001	**RD354470**	Carbon Resistor (chip)	47.0 63M J	チップ抵抗			01
	R0002	**RD354470**	Carbon Resistor (chip)	47.0 63M J	チップ抵抗			01
	R0003	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	-0010	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
	R0011	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
	-0014	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
	R0015	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01

*: New Parts

RANK: Japan only

REF NO.	PART NO.	DESCRIPTION		部品名	REMARKS	QTY	RANK
-0021	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
R0029	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
R0030	**RD354470**	Carbon Resistor (chip)	47.0 63M J	チップ抵抗			01
R0031	**RD357100**	Carbon Resistor (chip)	10.0K 63M J	チップ抵抗			01
R0033	**RD354470**	Carbon Resistor (chip)	47.0 63M J	チップ抵抗			01
-0038	**RD354470**	Carbon Resistor (chip)	47.0 63M J	チップ抵抗			01
R0039	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
R0040	**RD350000**	Carbon Resistor (chip)	0 63M J	チップ抵抗			01
RA001	**RE047100**	Resistor Array	10KX4	抵抗アレイ			01
RA002	**RE047100**	Resistor Array	10KX4	抵抗アレイ			01
SW001	**V6771900**	Jumper Wire	CHS-04 TA1	ジャンパーSW	Host To mLAN		03
SW002	**V6771900**	Jumper Wire	CHS-04 TA1	ジャンパーSW	mLAN To Host		03
X0002	**V6931900**	Quartz Crystal Unit	24.576MHz DS0751SV	水晶発振器			05

※: New Parts

RANK: Japan only

mLAN EXPANSION BOARD

mLAN16E

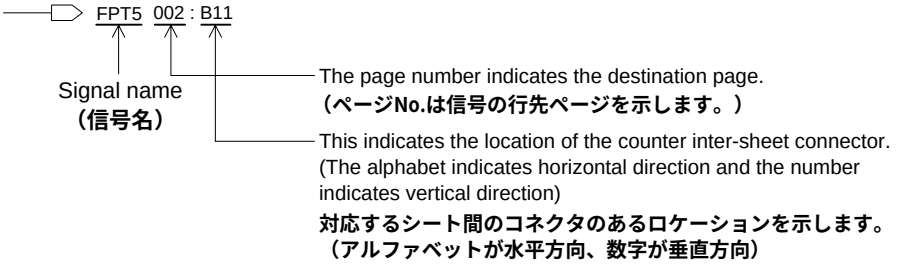
CIRCUIT DIAGRAM

■ CONTENTS（目次）

CIRCUIT DIAGRAM（回路図）

Notation for Circuit Diagrams（回路図表記上の注意）

1. How to identify inter-sheet connectors（シート間コネクタの読み方について）



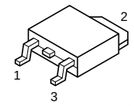
Note: See parts list for details of circuit board component parts.

注：シートの部品詳細はパーツリストをご参照ください。

■ MLN2 CIRCUIT DIAGRAM 001 (mLAN16E)

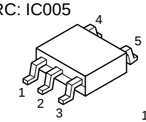
mLAN16E

- µPC2933T-E1 (XS516A00)
  REGULATOR +3.3V
  MLN2: IC004



1: V in
2: GND
3: V out

- RN5VD30CA-TR(XY568A00)
  REGULATOR +3V
  SRC: IC005



1: OUT
2: V_{DD}
3: GND
4: FB
5: NC
6: C_D

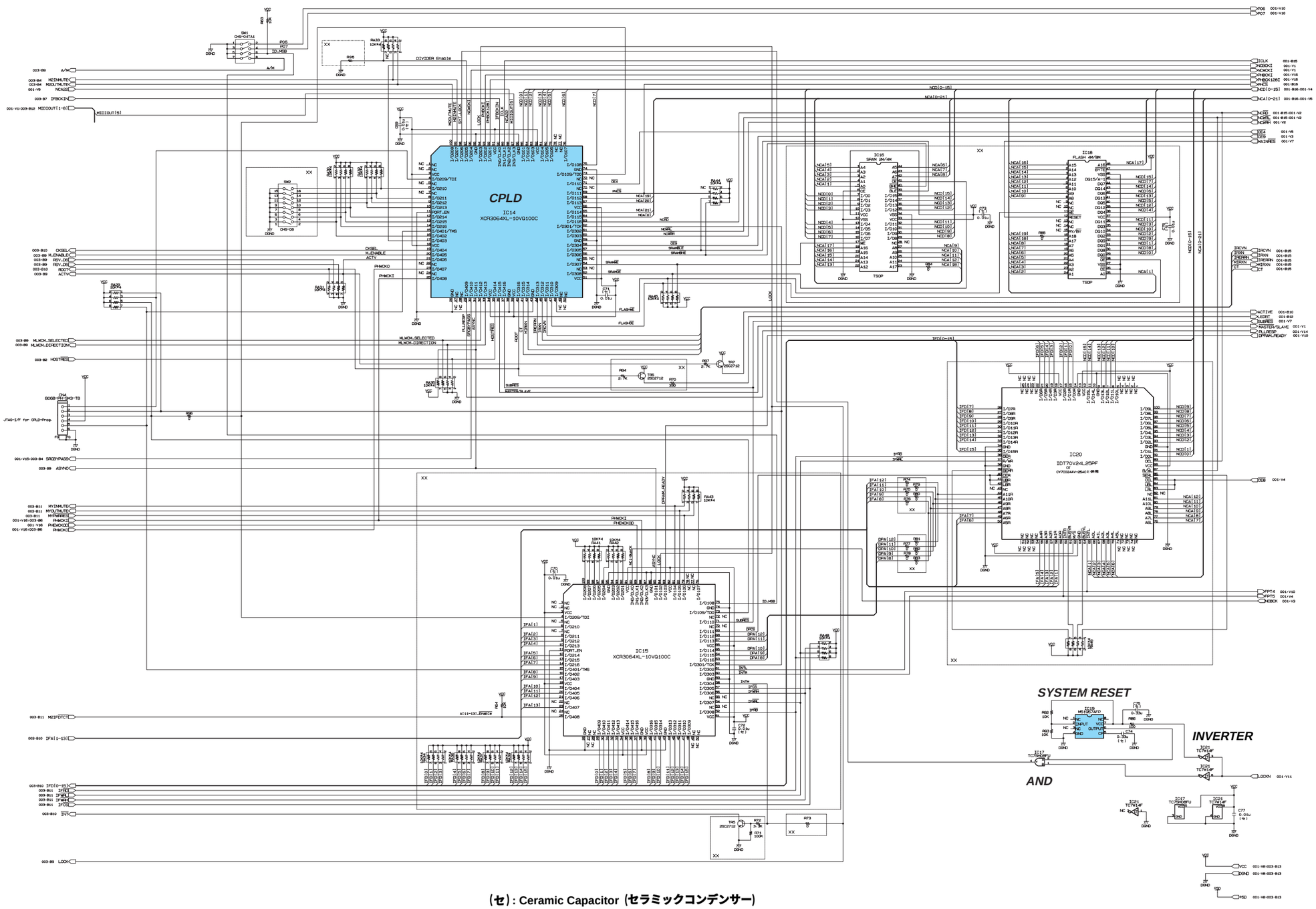
（セ）: Ceramic Capacitor（セラミックコンデンサー）
（マ）: Mylar Capacitor（マイラーコンデンサー）
金被1/16W: Carbon Resistor (chip) (チップ抵抗)
XX : not installed (実装しない)

28CC1-8827928-1 6

■ MLN2 CIRCUIT DIAGRAM 001 (mLAN16E)

■ MLN2 CIRCUIT DIAGRAM 002 (mLAN16E)

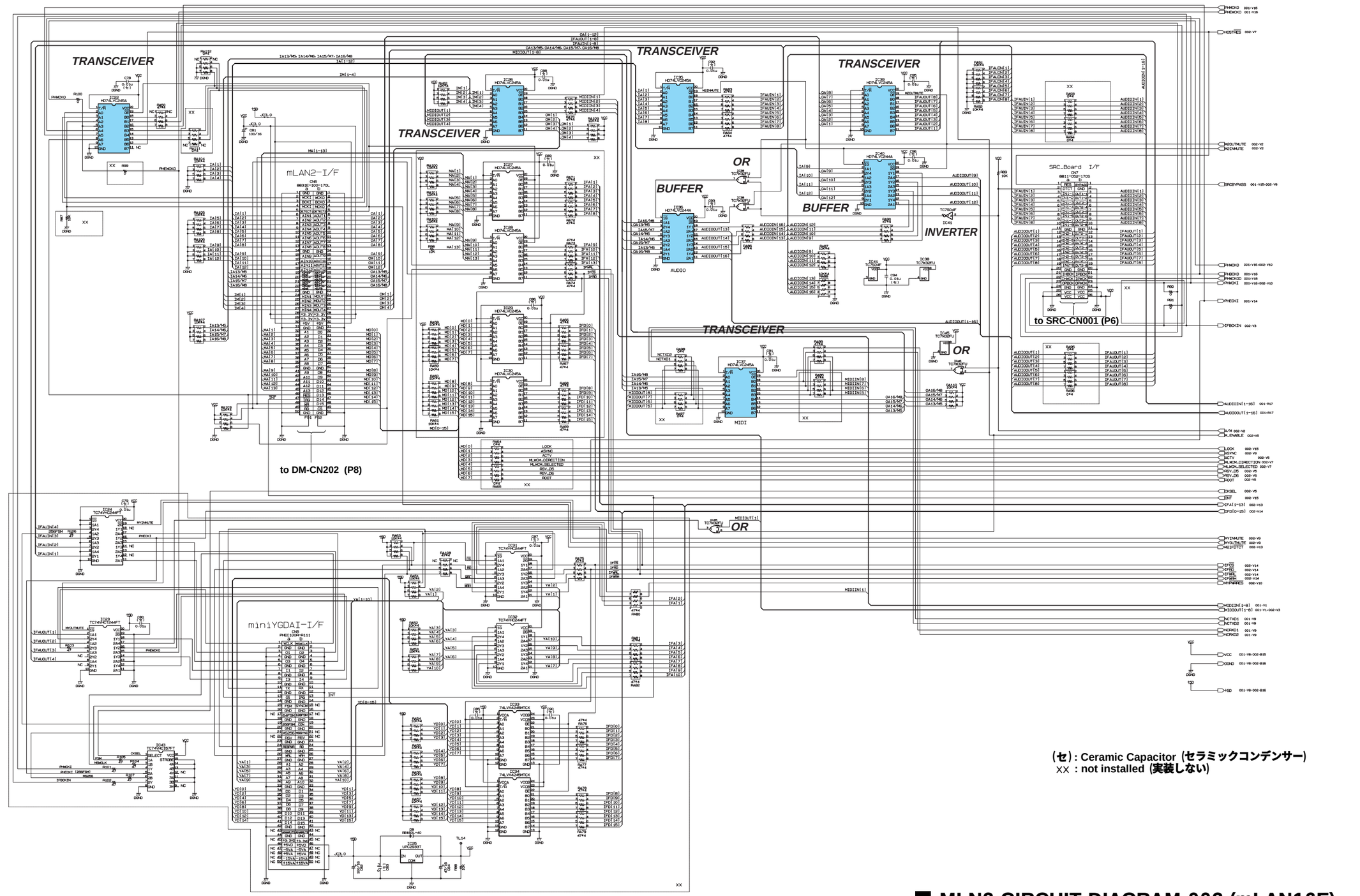
mLAN16E



(セ) : Ceramic Capacitor (セラミックコンデンサー)
XX : not installed (実装しない)

■ MLN2 CIRCUIT DIAGRAM 002 (mLAN16E)

■ MLN2 CIRCUIT DIAGRAM 003 (mLAN16E)



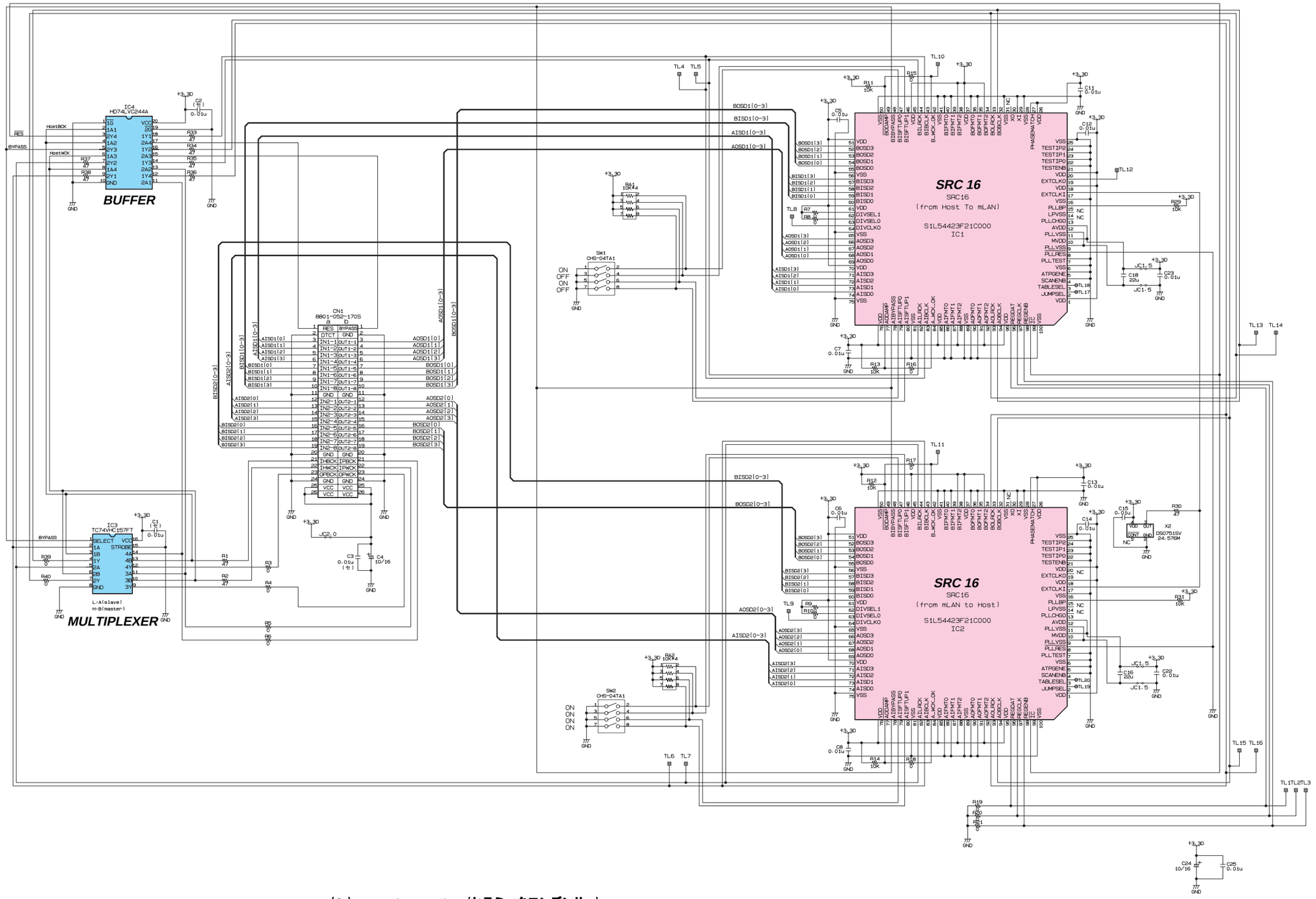
(セ) : Ceramic Capacitor (セラミックコンデンサー)
XX : not installed (実装しない)

28CC-8827928-3△2

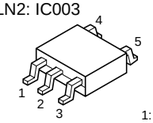
■ MLN2 CIRCUIT DIAGRAM 003 (mLAN16E)

■ SRC CIRCUIT DIAGRAM (mLAN16E)

mLAN16E



- RN5VD30CA-TR(XY568A00)
  REGULATOR +3V
  MLN2: IC003



(セ) : Ceramic Capacitor (セラミックコンデンサー)
∗∗ : not installed (実装しない)
金被1/16W : Carbon Resistor (chip) (チップ抵抗)

28CC1-8829056-1 ⚠3

■ SRC CIRCUIT DIAGRAM (mLAN16E)